Memory Stick™ INTERCONNECT EXTENDER CHIPSET WITH LVDS
SN65LVDT14 – ONE DRIVER PLUS FOUR RECEIVERS
SN65LVDT41 – FOUR DRIVERS PLUS ONE RECEIVER

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Integrated 110-Ω Nominal Receiver Line Termination Resistor**
- **Operate From a Single 3.3-V Supply**
- **Greater Than 125-Mbps Data Rate**
- **Flow-Through Pinout**
- **LVTTL-Compatible Logic I/Os**
- **ESD Protection on Bus Pins Exceeds 12 kV**
- **Meet or Exceed Requirements of ANSI/TIA/EIA-644A Standard for LVDS**
- **20-Pin Thin Shrink Small-Outline Package (PW) With 26-Mil Terminal Pitch**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Memory Stick™ Interface Extensions With Long Interconnects Between Host and Memory Stick**
- **Serial Peripheral Interface™ (SPI™) Interface Extension to Allow Long Interconnects Between Master and Slave**
- **MultiMediaCard™ (MMC) Interface in SPI Mode**
- **General-Purpose Asymmetric Bidirectional Communication**

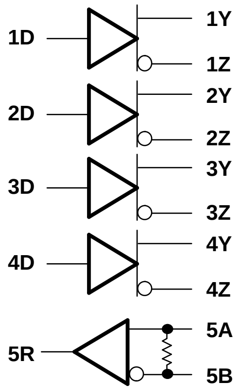
DESCRIPTION

The SN65LVDT14 combines one LVDS line driver with four terminated LVDS line receivers in one package. It is designed to be used at the Memory Stick™ end of an LVDS-based Memory Stick interface extension.

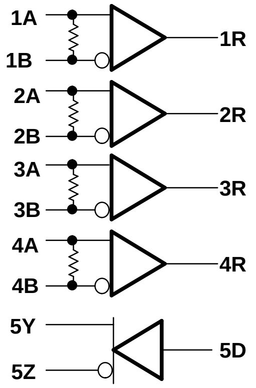
The SN65LVDT41 combines four LVDS line drivers with a single terminated LVDS line receiver in one package. It is designed to be used at the host end of an LVDS-based Memory Stick interface extension.

Serial Peripheral Interface, SPI are trademarks of Motorola.
MultiMediaCard is a trademark of MultiMediaCard Association.
Memory Stick is a trademark of Sony.

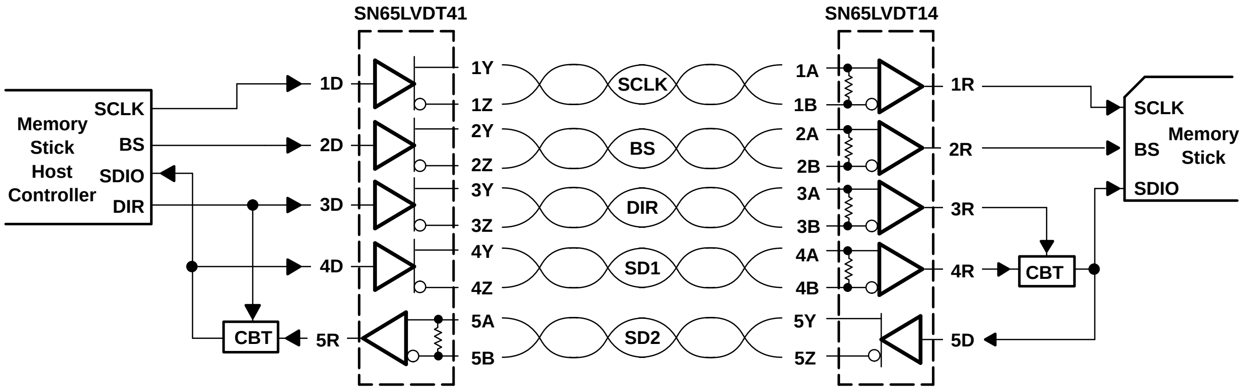
SN65LVDT41 LOGIC DIAGRAM (POSITIVE LOGIC)



SN65LVDT14 LOGIC DIAGRAM (POSITIVE LOGIC)



TYPICAL MEMORY STICK INTERFACE EXTENSION



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				SN65LVDT14, SN65LVDT41		UNIT
				MIN	MAX	
V_{CC}	Supply voltage range(2)			–0.5	4	V
	Input voltage range	D or R		–0.5	6	V
		A, B, Y, or Z		–0.5	4	
	Electrostatic discharge	Human-Body Model(3)	A, B, Y, Z, and GND		±12	KV
			All pins		±8	
		Charged-Device Model(4)	All pins		±500	V
	Continuous total power dissipation			See Dissipation Rating Table		
	Storage temperature range			–65	150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s				260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A

(4) Tested in accordance with JEDEC Standard 22, Test Method C101

Package Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	OPERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
PW	774 mW	6.2 mW/°C	402 mW	154 mW

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 1)	$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	V
				$V_{CC} - 0.8$	
T_A	Operating free-air temperature	–40		125	°C

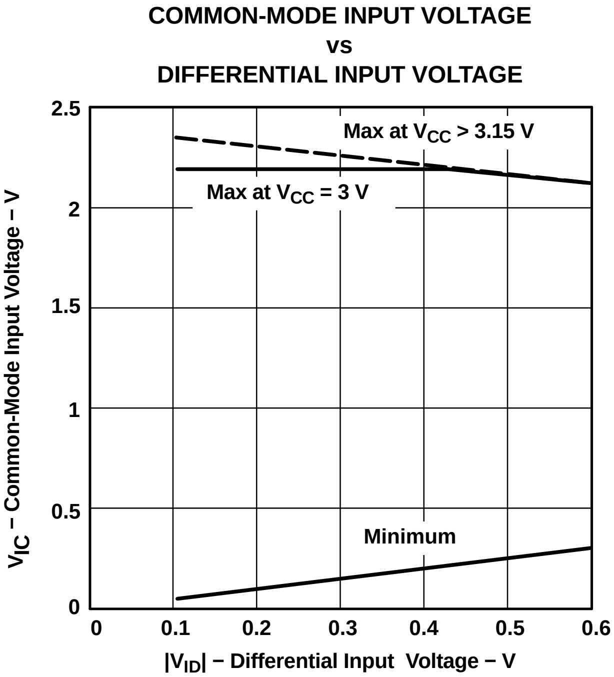


Figure 1. V_{IC} vs V_{ID} and V_{CC}

Receiver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold	See Figure 2 and Table 1	–100			mV
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I = 0 V and V_I = 2.4 V, Other input open			±40	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V, V_I = 2.4 V			±40	µA
C_i	Input capacitance, A or B input to GND	$V_I = A \sin 2\pi ft + CV$		5		pF
Z_t	Termination impedance	V_{ID} = 0.4 sin2.5E09 t V	88		132	Ω

(1) All typical values are at 25°C and with a 3.3-V supply.

Driver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 3 and Figure 5	247	340	454	mV
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage magnitude between logic states	R_L = 100 Ω, See Figure 3 and Figure 5	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 6	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 6	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 6		50		mV
I_{IH}	High-level input current	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±24	mA
		V_{OD} = 0 V(2)			±12	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±1	µA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) This parameter is GBD over industrial temperature range.

Device Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current	SN65LVDT14	Driver R_L = 100 Ω, Driver V_I = 0.8 V or 2 V, Receiver V_I = ±0.4 V		25	mA
		SN65LVDT41			35	

Receiver Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 10 pF, See Figure 4	1	2.6	4.8	ns
t_{PHL}	Propagation delay time, high- to low-level output		1	2.6	4.8	ns
t_r	Output signal rise time		0.15		1.4	ns
t_f	Output signal fall time		0.15		1.4	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			150	750	ps
$t_{sk(o)}$	Output skew(1)			100	550	ps
$t_{sk(pp)}$	Part-to-part skew(2)				1	ns

(1) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all the receivers of a single device with all of their inputs connected together.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Driver Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 7	0.9	1.7	3.9	ns
t_{PHL}	Propagation delay time, high- to low-level output		0.9	1.6	3.9	ns
t_r	Differential output signal rise time		0.26		1.2	ns
t_f	Differential output signal fall time		0.26		1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			150	750	ps
$t_{sk(o)}$	Output skew(1)			80	400	ps
$t_{sk(pp)}$	Part-to-part skew(2)				1.5	ns

(1) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

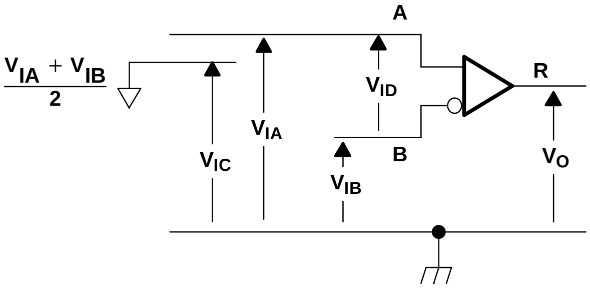


Figure 2. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGE		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

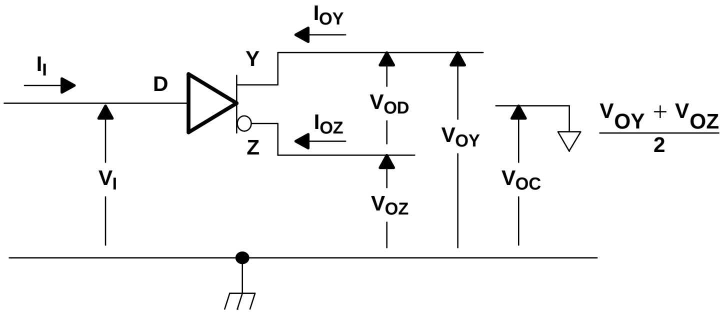
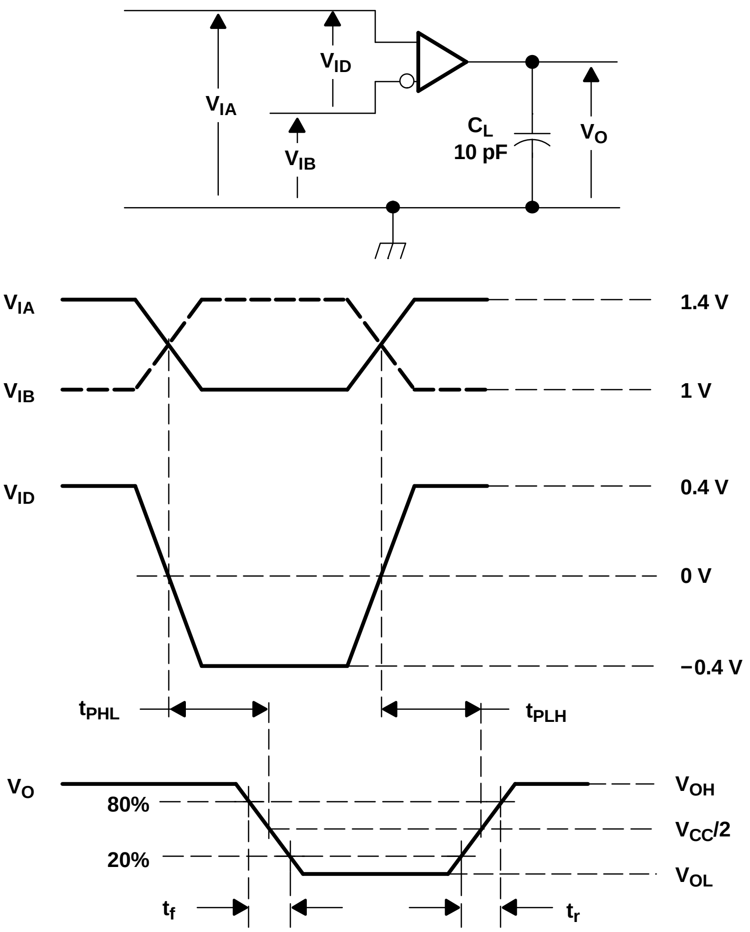


Figure 3. Driver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ± 0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Receiver Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

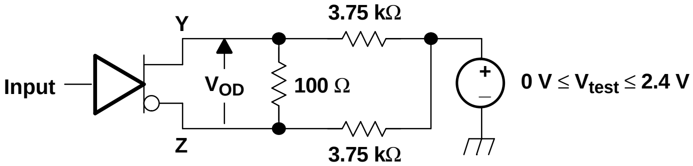
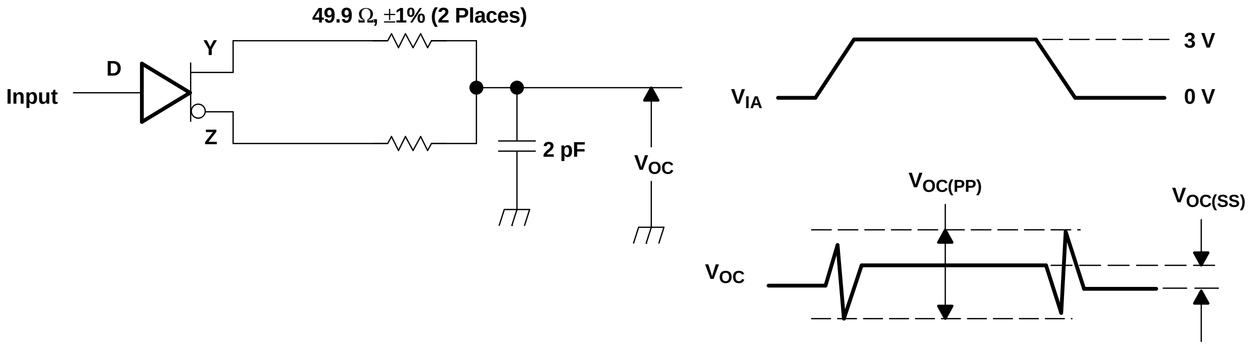
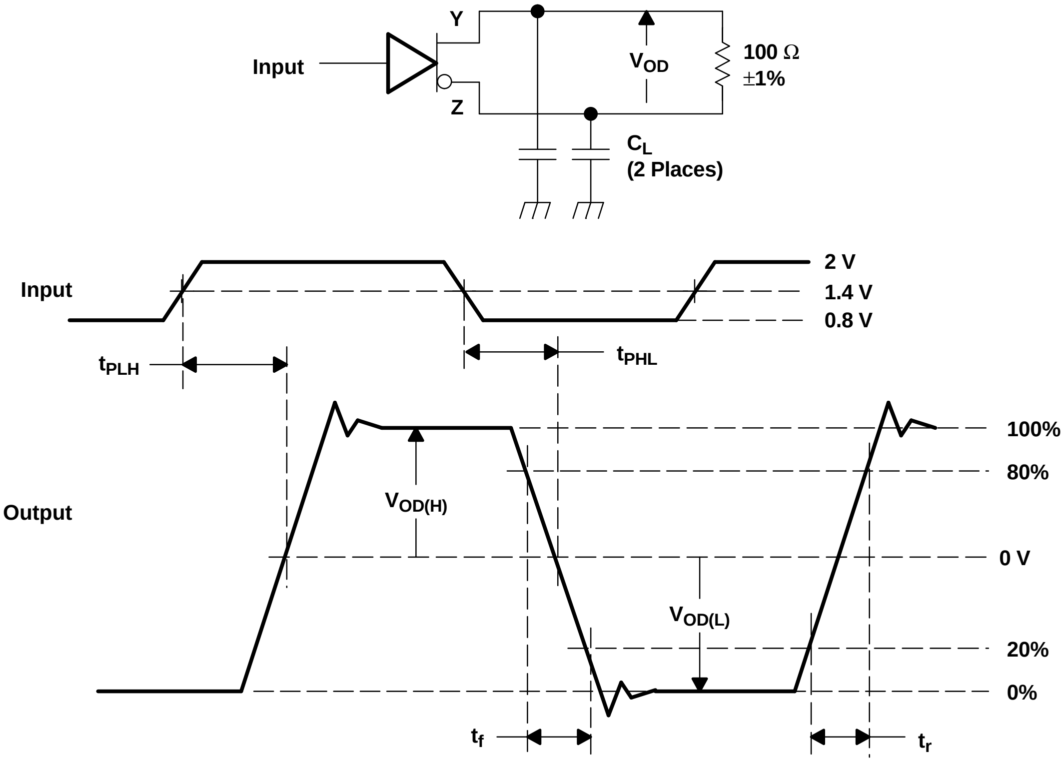


Figure 5. Driver VDO Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 µs. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 1 GHz.

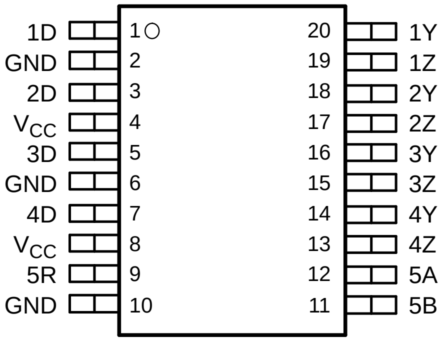
Figure 6. Test Circuit and Definitions for Driver Common-Mode Output Voltage



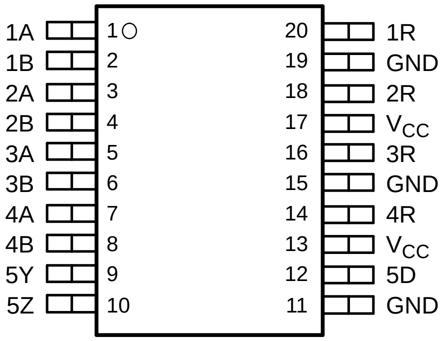
A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ± 0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 7. Test Circuit, Timing, and Voltage Definitions for Differential Output Signal

SN65LVDT41 (Marked as LVDT41)



SN65LVDT14 (Marked as LVDT14)



FUNCTION TABLES

RECEIVER[1]

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
$-100 \text{ mV} < V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

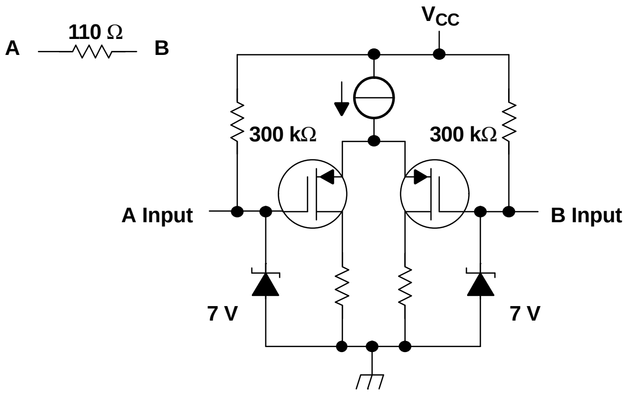
(1) H = high level, L = low level,
? = indeterminate

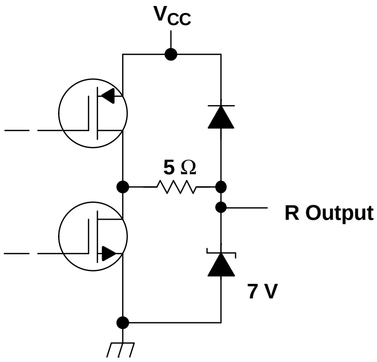
DRIVER[1]

INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

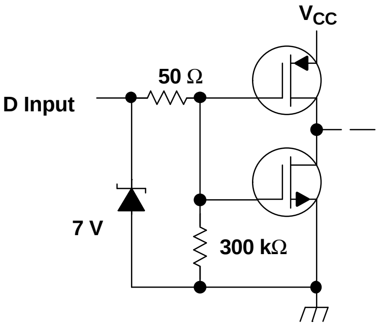
(1) H = high level, L = low level

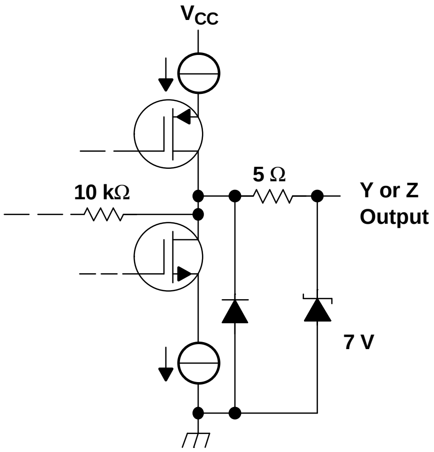
RECEIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





DRIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





TYPICAL CHARACTERISTICS
Receiver

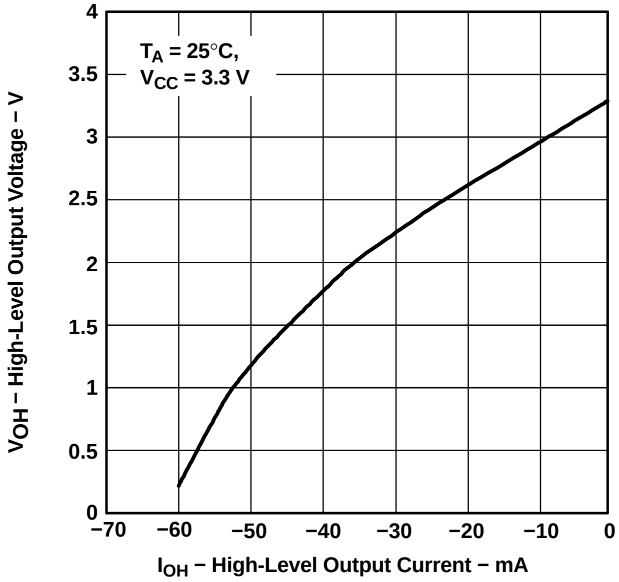

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 8.

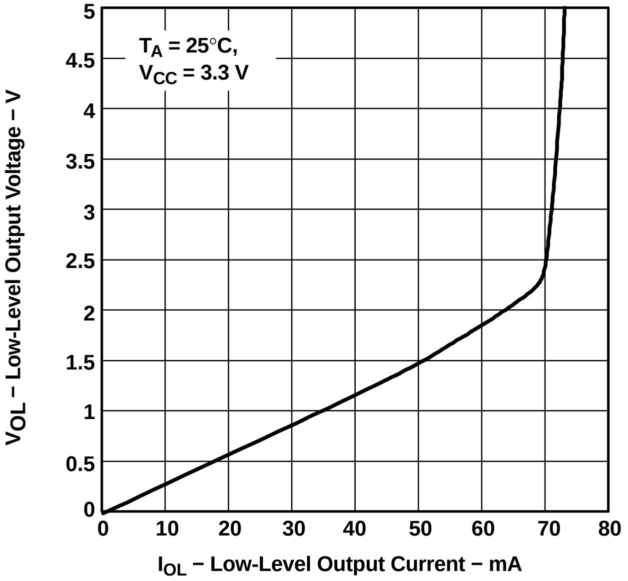

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 9.

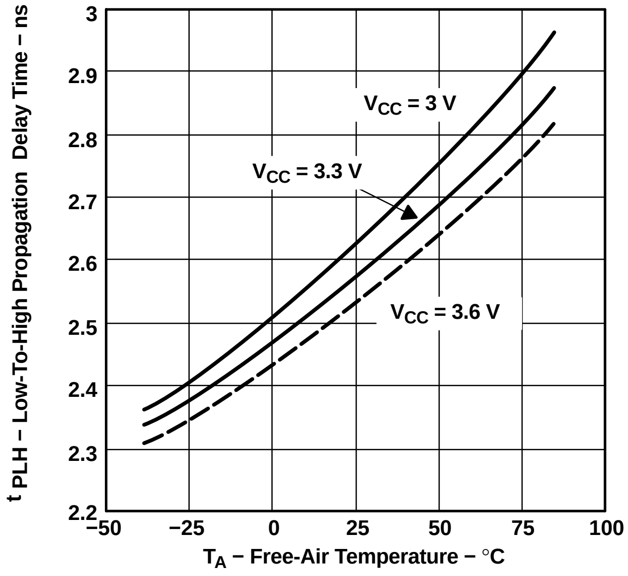

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 10.

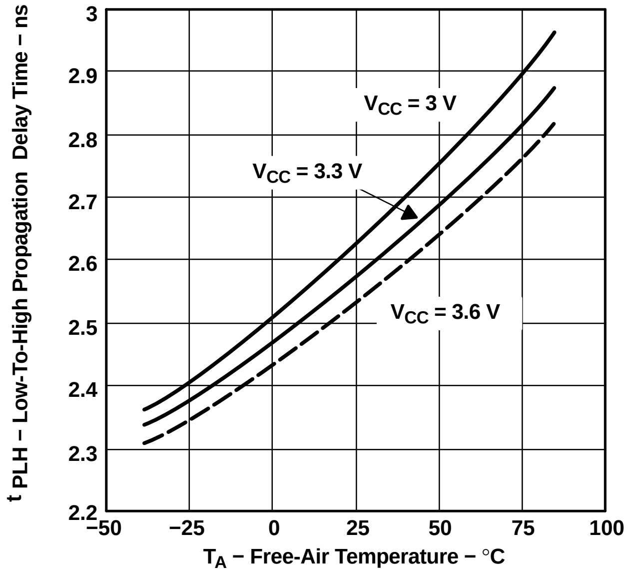

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 11.

TYPICAL CHARACTERISTICS
Driver

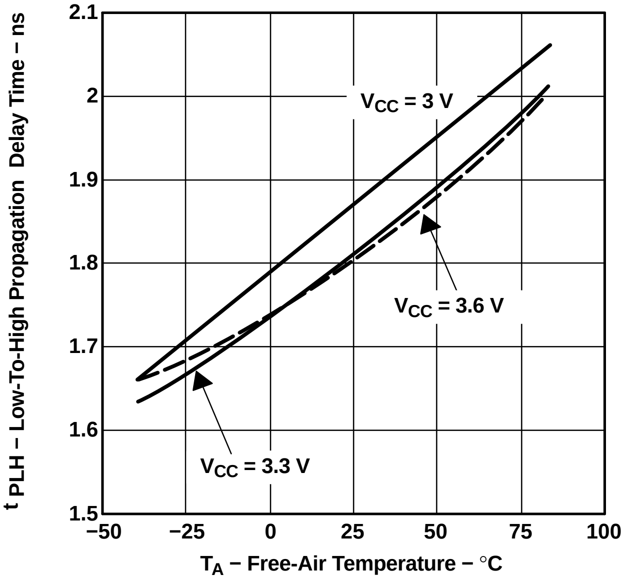

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 12.

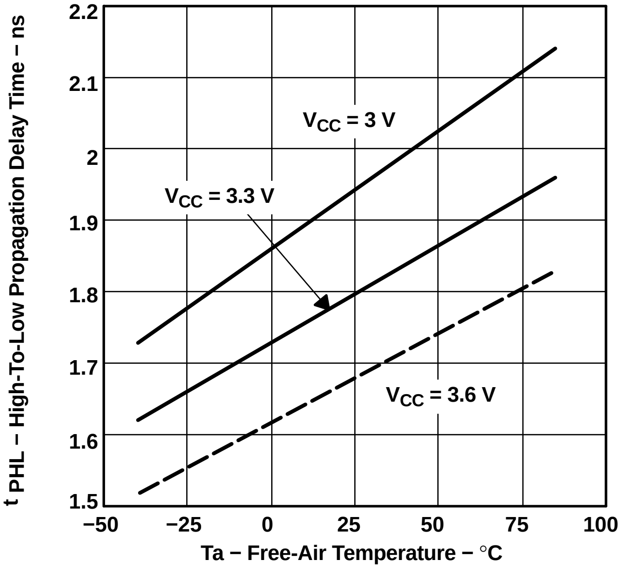

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 13.

APPLICATION INFORMATION

Extending the Memory Stick Interface Using LVDS Signaling Over Differential Transmission Cables

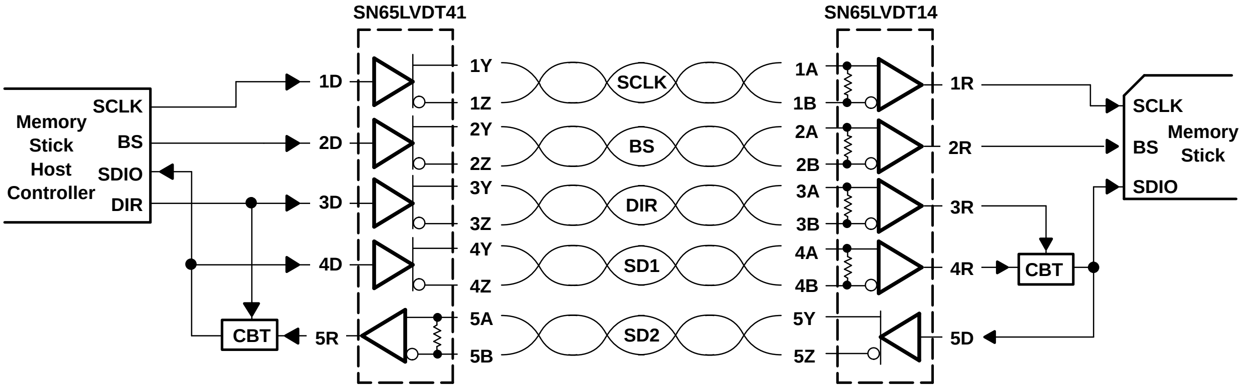


Figure 14. System-Level Block Diagram

The Memory Stick signaling interface operates in a master-slave architecture, with three active signal lines. The host (master) supplies a clock (SCLK) and bus-state (BS) signal to control the operation of the system. The SCLK and BS signals are unidirectional (simplex) from the host to the Memory Stick. The serial data input/output (SDIO) signal is a bidirectional (half-duplex) signal used to communicate both control and data information between the host and the Memory Stick. The direction of data control is managed by the host through a combination of BS line states and control information delivered to the Memory Stick.

The basic Memory Stick interface is capable of operating only over short distances due to the single-ended nature of the digital I/O signals. Such a configuration is entirely suitable for compact and portable devices where there is little if any separation between the host and the Memory Stick. In applications where a greater distance is needed between the host controller and the Memory Stick, it is necessary to utilize a different signaling method, such as low-voltage differential signaling, or LVDS. LVDS, as specified by the TIA/EIA-644-A standard, provides several benefits when compared to alternative long-distance signaling technologies: low radiated emissions, high noise immunity, low power consumption, and inexpensive interconnect cables.

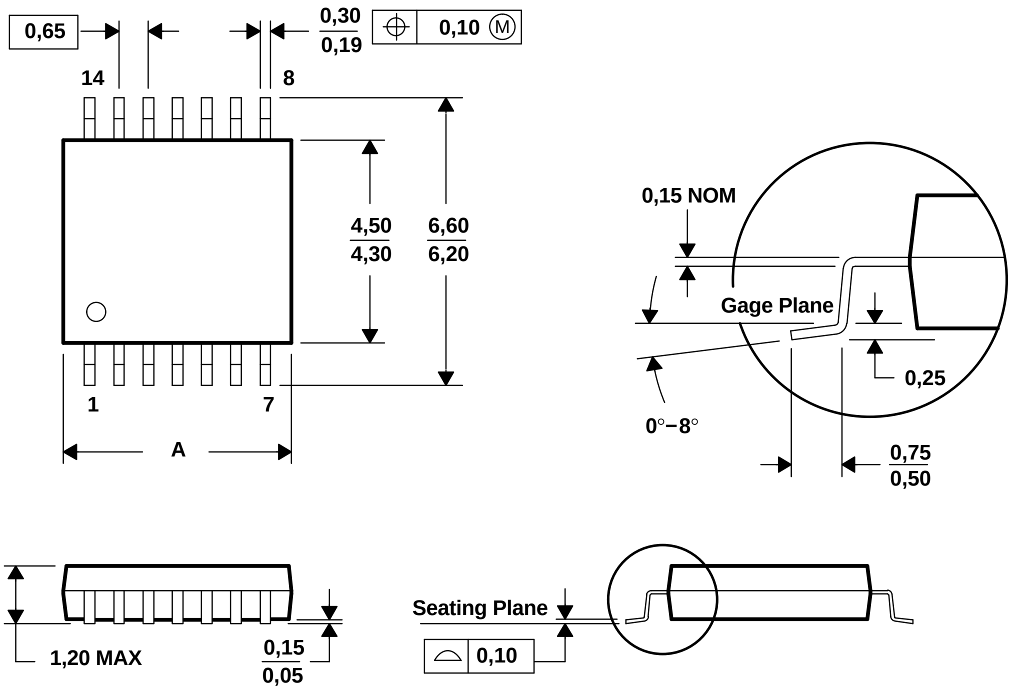
This device pair provides the necessary LVDS drivers and receivers specifically targeted at implementing a Memory Stick interconnect extension. It utilizes simplex links for the SCLK and BS signals and two simplex links for the SDIO data. The half-duplex SDIO data is split into two simplex streams under control of the host processor by means of the direction (DIR) signal. The DIR signal also is carried from the host to the Memory Stick on a simplex LVDS link.

The switching of the SDIO signal-flow direction in the single-ended interfaces is managed by electronic switch devices, identified by the CBT symbol in Figure 7. A suggested CBT device for this application is the TI SN74CBTLV1G125. These devices are available in space-saving SOT-23 or SC-70 packages.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



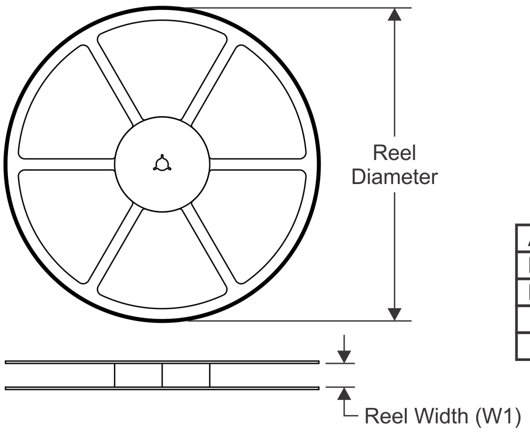
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

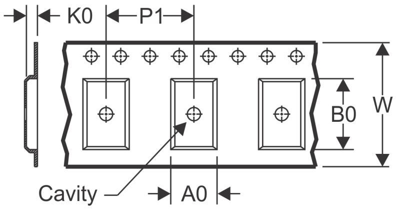
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TAPE AND REEL INFORMATION

REEL DIMENSIONS

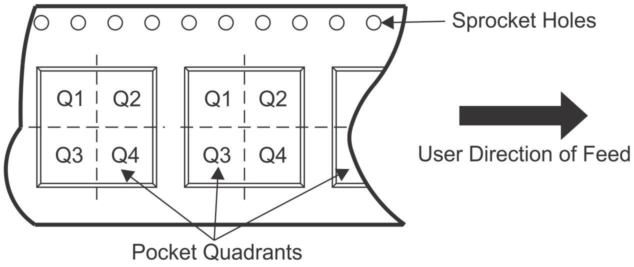


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

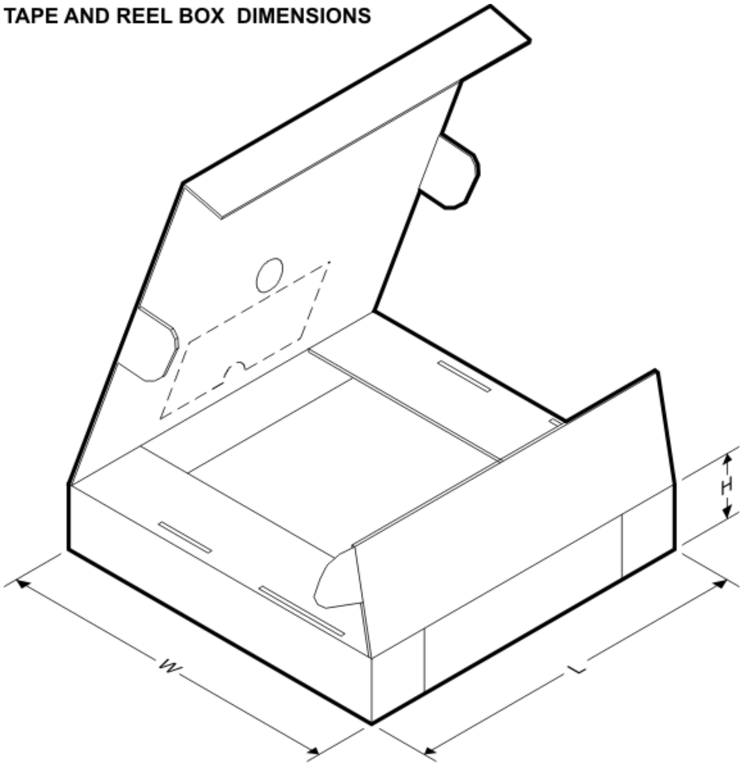
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDT14QPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN65LVDT41QPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

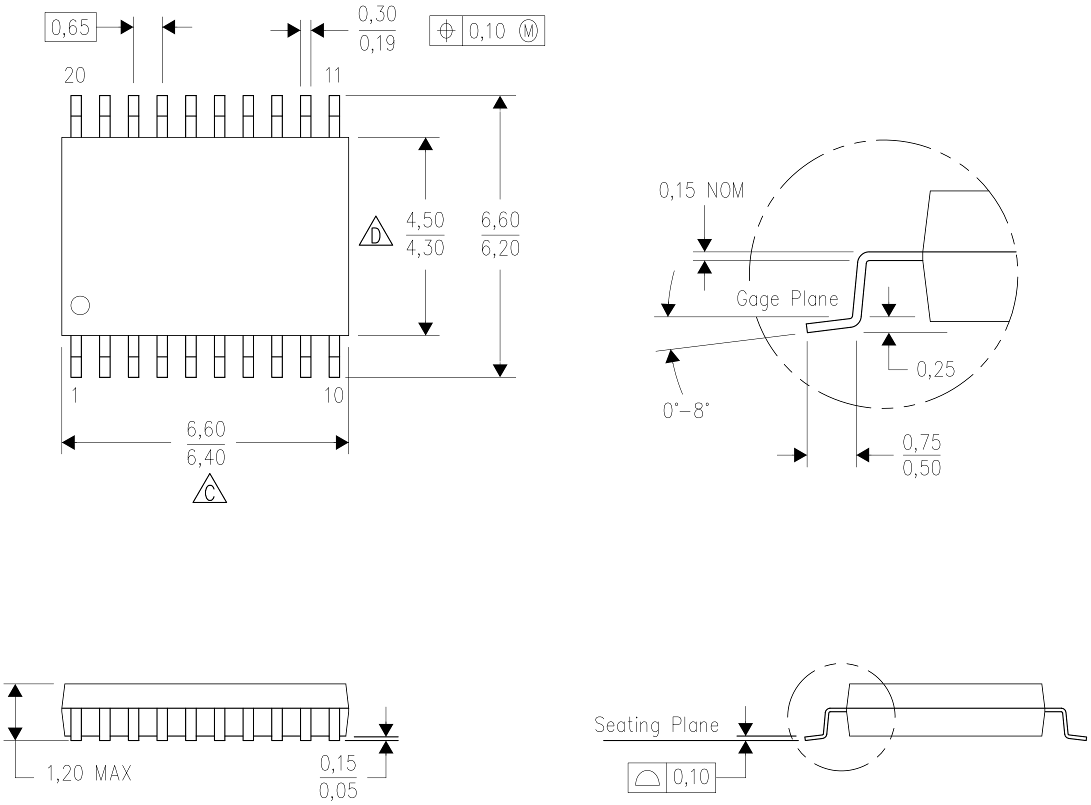
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

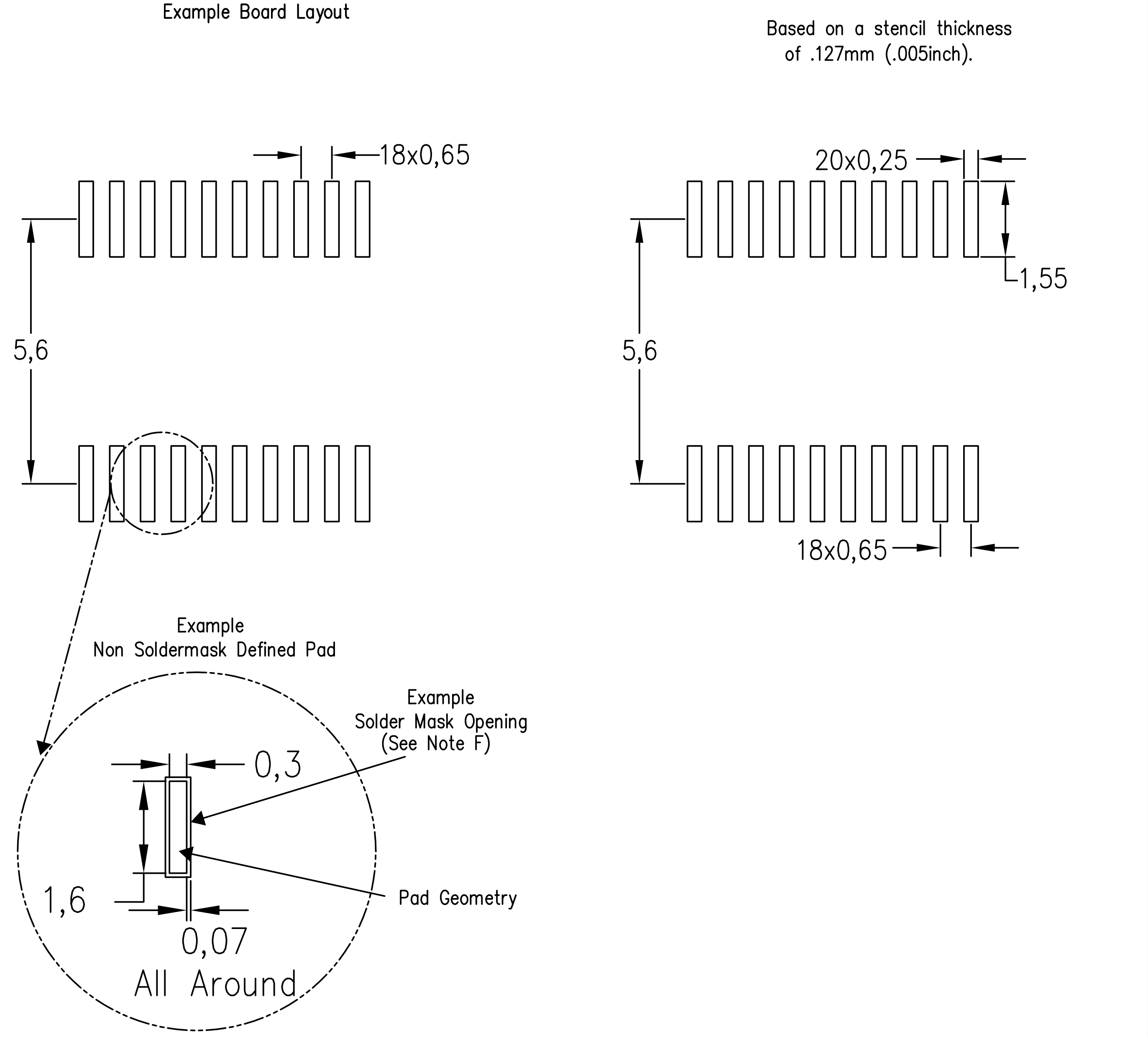
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDT14QPWREP	TSSOP	PW	20	2000	367.0	367.0	38.0
SN65LVDT41QPWREP	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4211284–5/F 12/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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