

## 16-Channel, Constant-Current LED Driver

Check for Samples: [TLC59281](#)

### FEATURES

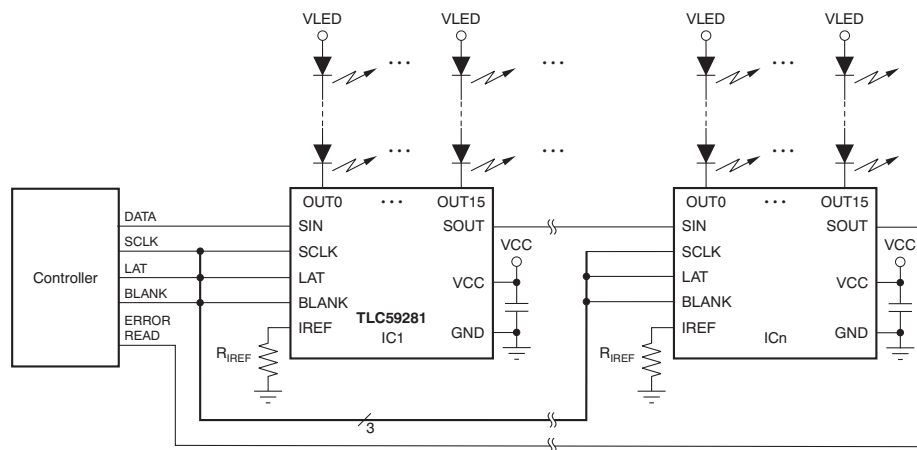
- 16 Channels, Constant-Current Sink Output with On/Off Control
- 35-mA Capability (Constant-Current Sink)
- 10-ns High-Speed Constant-Current Switching Transient Time
- Low On-Time Error
- LED Power-Supply Voltage up to 17 V
- $V_{CC} = 3.0\text{ V to }5.5\text{ V}$
- Constant-Current Accuracy:
  - Channel-to-Channel =  $\pm 1\%$
  - Device-to-Device =  $\pm 1\%$
- CMOS Logic Level I/O
- 35-MHz Data Transfer Rate
- 20-ns BLANK Pulse Width
- Operating Temperature:  $-40^{\circ}\text{C to }+85^{\circ}\text{C}$

### APPLICATIONS

- LED Video Displays
- Message Boards
- Illumination

### DESCRIPTION

The TLC59281 is a 16-channel, constant-current sink LED driver. Each channel can be turned on/off by writing serial data to an internal register. The constant-current value of all 16 channels is set by a single external resistor.



Typical Application Circuit (Multiple Daisy-Chained TLC59281s)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

| PRODUCT  | PACKAGE-LEAD    | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|----------|-----------------|-----------------|---------------------------|
| TLC59281 | SSOP-24/QSOP-24 | TLC59281DBQR    | Tape and Reel, 2500       |
|          |                 | TLC59281DBQ     | Tube, 50                  |
| TLC59281 | QFN-24          | TLC59281RGER    | Tape and Reel, 3000       |
|          |                 | TLC59281RGE     | Tape and Reel, 250        |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER           |                                 |                             | TLC59281                      | UNIT |
|---------------------|---------------------------------|-----------------------------|-------------------------------|------|
| V <sub>CC</sub>     | Supply voltage: V <sub>CC</sub> |                             | –0.3 to +6.0                  | V    |
| I <sub>OUT</sub>    | Output current (dc)             | OUT0 to OUT15               | 40                            | mA   |
| V <sub>IN</sub>     | Input voltage range             | SIN, SCLK, LAT, BLANK, IREF | –0.3 to V <sub>CC</sub> + 0.3 | V    |
| V <sub>OUT</sub>    | Output voltage range            | SOUT                        | –0.3 to V <sub>CC</sub> + 0.3 | V    |
|                     |                                 | OUT0 to OUT15               | –0.3 to +18                   | V    |
| T <sub>J(MAX)</sub> | Operating junction temperature  |                             | +150                          | °C   |
| T <sub>STG</sub>    | Storage temperature range       |                             | –55 to +150                   | °C   |
| ESD rating          | Human body model (HBM)          |                             | 2                             | kV   |
|                     | Charged device model (CDM)      |                             | 500                           | V    |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) All voltage values are with respect to network ground terminal.

### DISSIPATION RATINGS

| PACKAGE               | OPERATING FACTOR<br>ABOVE T <sub>A</sub> = +25°C | T <sub>A</sub> < +25°C<br>POWER RATING | T <sub>A</sub> = +70°C<br>POWER RATING | T <sub>A</sub> = +85°C<br>POWER RATING |
|-----------------------|--|--|--|--|
| SSOP-24/QSOP-24       | 14.3 mW/°C                                       | 1782 mW                                | 1140 mW                                | 927 mW                                 |
| QFN-24 <sup>(1)</sup> | 24.8 mW/°C                                       | 3106 mW                                | 1988 mW                                | 1615 mW                                |

- (1) The package thermal impedance is calculated in accordance with JESD51-5.

## RECOMMENDED OPERATING CONDITIONS

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.

| PARAMETER  |                                      | TEST CONDITIONS | TLC59281              |     |                       | UNIT |
|--|--------------------------------------|-----------------|-----------------------|-----|-----------------------|------|
|  |                                      |                 | MIN                   | NOM | MAX                   |      |
| DC Characteristics: V <sub>CC</sub> = 3 V to 5.5 V |                                      |                 |                       |     |                       |      |
| V <sub>CC</sub>                                    | Supply voltage                       |                 | 3.0                   |     | 5.5                   | V    |
| V <sub>O</sub>                                     | Voltage applied to output            | OUT0 to OUT15   |                       |     | 17                    | V    |
| V <sub>IH</sub>                                    | High-level input voltage             |                 | 0.7 × V <sub>CC</sub> |     | V <sub>CC</sub>       | V    |
| V <sub>IL</sub>                                    | Low-level input voltage              |                 | GND                   |     | 0.3 × V <sub>CC</sub> | V    |
| I <sub>OH</sub>                                    | High-level output current            | SOUT            |                       |     | −1                    | mA   |
| I <sub>OL</sub>                                    | Low-level output current             | SOUT            |                       |     | 1                     | mA   |
| I <sub>OLC</sub>                                   | Constant output sink current         | OUT0 to OUT15   | 2                     |     | 35                    | mA   |
| T <sub>A</sub>                                     | Operating free-air temperature range |                 | −40                   |     | +85                   | °C   |
| T <sub>J</sub>                                     | Operating junction temperature range |                 | −40                   |     | +125                  | °C   |
| AC Characteristics: V <sub>CC</sub> = 3 V to 5.5 V |                                      |                 |                       |     |                       |      |
| f <sub>CLK</sub> (SCLK)                            | Data shift clock frequency           | SCLK            |                       |     | 35                    | MHz  |
| T <sub>WH0</sub>                                   | Pulse duration                       | SCLK            | 10                    |     |                       | ns   |
| T <sub>WL0</sub>                                   |                                      | SCLK            | 10                    |     |                       | ns   |
| T <sub>WH1</sub>                                   |                                      | LAT             | 20                    |     |                       | ns   |
| T <sub>WH2</sub>                                   |                                      | BLANK           | 20                    |     |                       | ns   |
| T <sub>WL2</sub>                                   |                                      | BLANK           | 20                    |     |                       | ns   |
| T <sub>SU0</sub>                                   |                                      | Setup time      | SIN−SCLK↑             | 4   |                       |      |
| T <sub>SU1</sub>                                   | LAT↑−SCLK↑                           |                 | 100                   |     |                       | ns   |
| T <sub>H0</sub>                                    | Hold time                            | SIN−SCLK↑       | 3                     |     |                       | ns   |
| T <sub>H1</sub>                                    |                                      | LAT↑−SCLK↑      | 10                    |     |                       | ns   |

## ELECTRICAL CHARACTERISTICS

At  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ . Typical values at  $V_{CC} = 3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

| PARAMETER         |  | TEST CONDITIONS   | TLC59281       |           |          | UNIT          |
|-------------------|--|---|----------------|-----------|----------|---------------|
|                   |  |   | MIN            | TYP       | MAX      |               |
| $V_{OH}$          | High-level output voltage                                  | $I_{OH} = -1\text{ mA}$ at SOUT   | $V_{CC} - 0.4$ |           | $V_{CC}$ | V             |
| $V_{OL}$          | Low-level output voltage                                   | $I_{OL} = 1\text{ mA}$ at SOUT  | 0              |           | 0.4      | V             |
| $I_{IN}$          | Input current  | $V_{IN} = V_{CC}$ or GND at SIN, SCLK, LAT, and BLANK   | -1             |           | 1        | $\mu\text{A}$ |
| $I_{CC1}$         | Supply current ( $V_{CC}$ )                                | SIN/SCLK/LAT = low, BLANK = high, $V_{OUTn} = 1\text{ V}$ , $R_{REF} = 27\text{ k}\Omega$   |                | 1         | 2        | mA            |
| $I_{CC2}$         |  | SIN/SCLK/LAT = low, BLANK = high, $V_{OUTn} = 1\text{ V}$ , $R_{REF} = 3\text{ k}\Omega$  |                | 4.5       | 8        | mA            |
| $I_{CC3}$         |  | SIN/SCLK/LAT/BLANK = low, $V_{OUTn} = 1\text{ V}$ , $R_{REF} = 3\text{ k}\Omega$  |                | 7         | 18       | mA            |
| $I_{CC4}$         |  | SIN/SCLK/LAT/BLANK = low, $V_{OUTn} = 1\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$  |                | 16        | 40       | mA            |
| $I_{OLC}$         | Constant output current                                    | All $OUTn = \text{ON}$ , $V_{OUTn} = V_{OUTfix} = 1\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$ (see Figure 6), at OUT0 to OUT15   | 31             | 34        | 37       | mA            |
| $I_{OLKG}$        | Output leakage current                                     | All $OUTn$ for constant-current driver, all outputs off BLANK = high, $V_{OUTn} = V_{OUTfix} = 17\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$ (see Figure 6), at OUT0 to OUT15 |                |           | 0.1      | $\mu\text{A}$ |
| $\Delta I_{OLC}$  | Constant-current error (channel-to-channel) <sup>(1)</sup> | All $OUTn = \text{ON}$ , $V_{OUTn} = V_{OUTfix} = 1\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$ at OUT0 to OUT15   |                | $\pm 1$   | $\pm 3$  | %             |
| $\Delta I_{OLC1}$ | Constant-current error (device-to-device) <sup>(2)</sup>   | All $OUTn = \text{ON}$ , $V_{OUTn} = V_{OUTfix} = 1\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$ at OUT0 to OUT15   |                | $\pm 1$   | $\pm 6$  | %             |
| $\Delta I_{OLC2}$ | Line regulation <sup>(3)</sup>                             | All $OUTn = \text{ON}$ , $V_{OUTn} = V_{OUTfix} = 1\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$ at OUT0 to OUT15   |                | $\pm 0.5$ | $\pm 1$  | %/V           |
| $\Delta I_{OLC3}$ | Load regulation <sup>(4)</sup>                             | All $OUTn = \text{ON}$ , $V_{OUTn} = 1\text{ V}$ to $3\text{ V}$ , $V_{OUTfix} = 1\text{ V}$ , $R_{REF} = 1.5\text{ k}\Omega$ , at OUT0 to OUT15                              |                | $\pm 1$   | $\pm 3$  | %/V           |
| $V_{REF}$         | Reference voltage output                                   | $R_{REF} = 1.5\text{ k}\Omega$  | 1.16           | 1.20      | 1.24     | V             |

(1) The deviation of each output from the average of OUT0–OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta (\%) = \left[ \frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15})}{16}} - 1 \right] \times 100$$

(2) The deviation of the OUT0–OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta (\%) = \left[ \frac{\frac{(I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right] \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(\text{IDEAL})} = 42 \times \left[ \frac{1.20}{R_{REF}} \right]$$

(3) Line regulation is calculated by this equation:

$$\Delta (\%/V) = \left[ \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})} \right] \times \frac{100}{5.5\text{ V} - 3.0\text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta (\%/V) = \left[ \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})} \right] \times \frac{100}{3\text{ V} - 1\text{ V}}$$

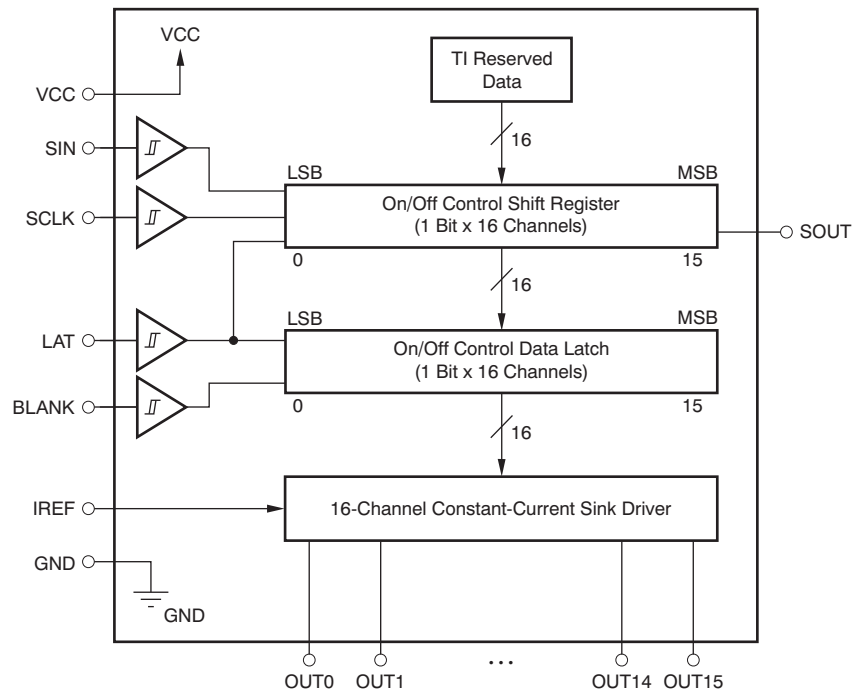
## SWITCHING CHARACTERISTICS

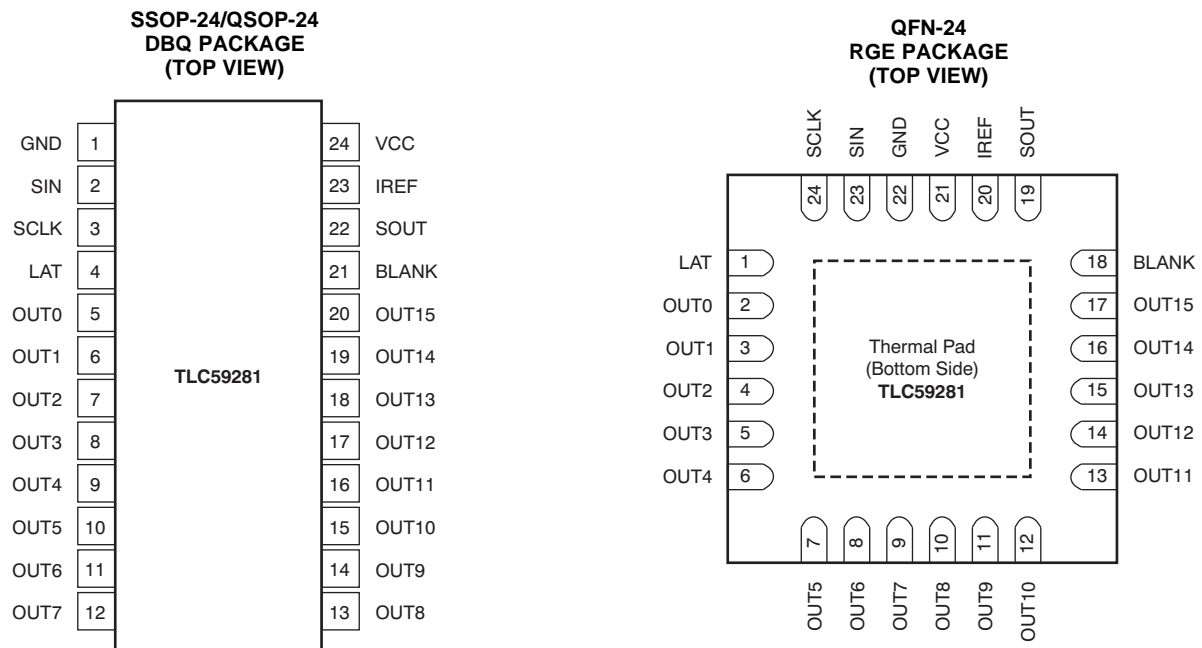
At  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $C_L = 15\text{ pF}$ ,  $R_L = 130\ \Omega$ ,  $R_{IREF} = 1.5\text{ k}\Omega$ , and  $V_{LED} = 5.5\text{ V}$ . Typical values at  $V_{CC} = 3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

| PARAMETER     |                                     | TEST CONDITIONS  | TLC59281 |     |     | UNIT |
|---------------|-------------------------------------|--|----------|-----|-----|------|
|               |                                     |  | MIN      | TYP | MAX |      |
| $t_{R0}$      | Rise time                           | SOUT (see Figure 5)  |          | 5   | 15  | ns   |
| $t_{R1}$      |                                     | OUTn (see Figure 4)  |          | 10  | 30  | ns   |
| $t_{F0}$      | Fall time                           | SOUT (see Figure 5)  |          | 5   | 15  | ns   |
| $t_{F1}$      |                                     | OUTn (see Figure 4)  |          | 10  | 30  | ns   |
| $t_{D0}$      | Propagation delay time              | SCLK↑ to SOUT  |          | 8   | 20  | ns   |
| $t_{D1}$      |                                     | LAT↑ or BLANK↓ to OUTn sink current on (see Figure 10)                                 |          | 12  | 30  | ns   |
| $t_{D2}$      |                                     | LAT↑ or BLANK↑ to OUTn sink current off (see Figure 10)                                |          | 12  | 30  | ns   |
| $t_{ON\_ERR}$ | Output on-time error <sup>(1)</sup> | On/off latch data = all '1', 20 ns BLANK low level one-shot pulse input (see Figure 4) | -8       |     | +8  | ns   |

(1) Output on-time error ( $t_{ON\_ERR}$ ) is calculated by the formula:  $t_{ON\_ERR} (\text{ns}) = t_{OUT\_ON} - \text{BLANK low level one-shot pulse width } (T_{WL2})$ .  $t_{OUT\_ON}$  indicates the actual on-time of the constant-current driver.

## FUNCTIONAL BLOCK DIAGRAM



**DEVICE INFORMATION**

NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB pattern.

## TERMINAL FUNCTIONS

| TERMINAL |     |     | I/O | DESCRIPTION   |
|----------|-----|-----|-----|---|
| NAME     | DBQ | RGE |     |   |
| SIN      | 2   | 23  | I   | Serial data input for driver on/off control. When SIN = high level, data '1' are written into LSB of the on/off control shift register at the rising edge of SCLK.  |
| SCLK     | 3   | 24  | I   | Serial data shift clock. Schmitt buffer input. All data in the on/off control shift register are shifted toward the MSB by 1-bit synchronization of SCLK. A rising edge on SCLK is allowed 100 ns after a rising edge of LAT.   |
| LAT      | 4   | 1   | I   | Edge triggered latch. The data in the on/off control data shift register are transferred to the on/off control data latch at this rising edge. At the same time, the data in the on/off control shift register are replaced with TI reserved data for production test. LAT must be toggled only once after the shift data are updated to avoid the on/off control latch data being replaced with TI reserved data in the shift register. The reserved data is not a fixed number. |
| BLANK    | 21  | 18  | I   | Blank, all outputs. When BLANK = high level, all constant-current outputs (OUT0–OUT15) are forced off. When BLANK = low level, all constant-current outputs are controlled by the on/off control data in the data latch.  |
| IREF     | 23  | 20  | I/O | Constant-current value setting, OUT0–OUT15 sink constant-current is set to desired value by connection to an external resistor between IREF and GND.  |
| SOUT     | 22  | 19  | O   | Serial data output. This output is connected to the MSB of the on/off data shift register. SOUT data changes at the rising edge of SCLK.  |
| OUT0     | 5   | 2   | O   | Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.   |
| OUT1     | 6   | 3   | O   | Constant-current output   |
| OUT2     | 7   | 4   | O   | Constant-current output   |
| OUT3     | 8   | 5   | O   | Constant-current output   |
| OUT4     | 9   | 6   | O   | Constant-current output   |
| OUT5     | 10  | 7   | O   | Constant-current output   |
| OUT6     | 11  | 8   | O   | Constant-current output   |
| OUT7     | 12  | 9   | O   | Constant-current output   |
| OUT8     | 13  | 10  | O   | Constant-current output   |
| OUT9     | 14  | 11  | O   | Constant-current output   |
| OUT10    | 15  | 12  | O   | Constant-current output   |
| OUT11    | 16  | 13  | O   | Constant-current output   |
| OUT12    | 17  | 14  | O   | Constant-current output   |
| OUT13    | 18  | 15  | O   | Constant-current output   |
| OUT14    | 19  | 16  | O   | Constant-current output   |
| OUT15    | 20  | 17  | O   | Constant-current output   |
| VCC      | 24  | 21  | —   | Power-supply voltage  |
| GND      | 1   | 22  | —   | Power ground  |

## PARAMETER MEASUREMENT INFORMATION

### PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

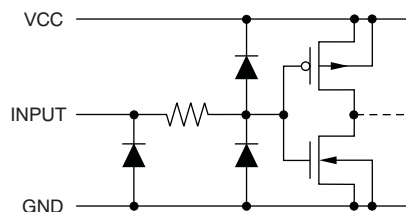


Figure 1. SIN, SCLK, LAT, BLANK

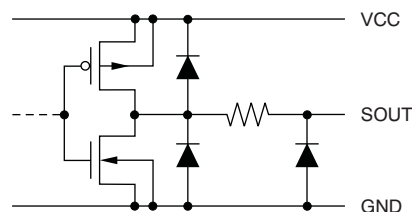


Figure 2. SOUT

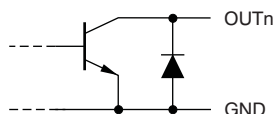
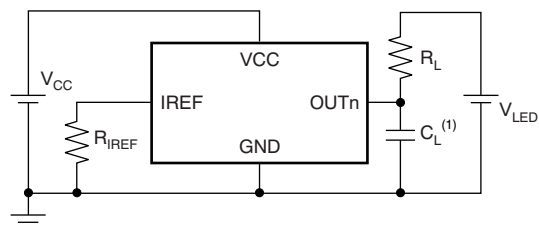


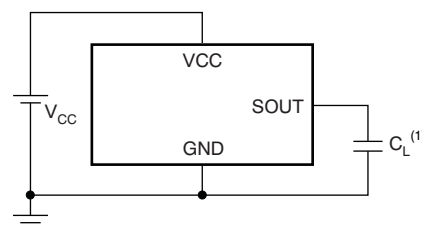
Figure 3. OUT0 Through OUT15

### TEST CIRCUITS



(1)  $C_L$  includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUTn



(1)  $C_L$  includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for SOUT

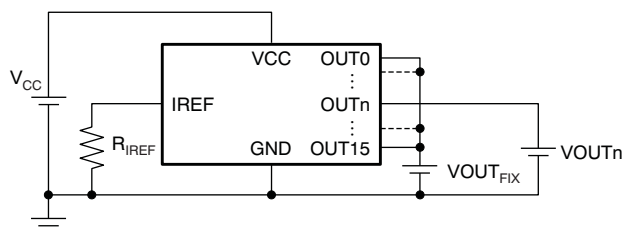
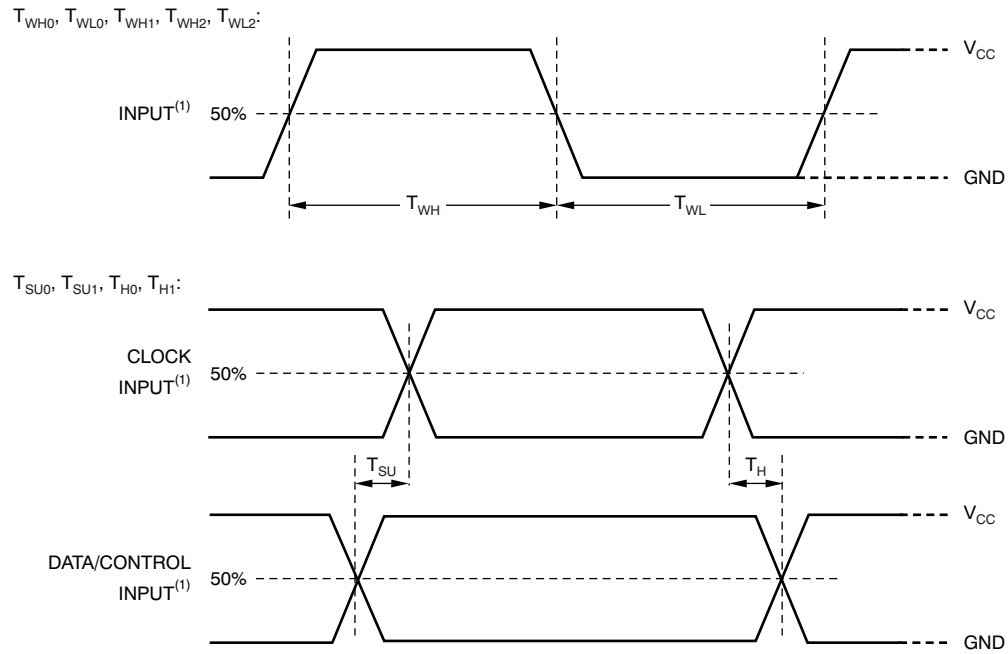


Figure 6. Constant-Current Test Circuit for OUTn

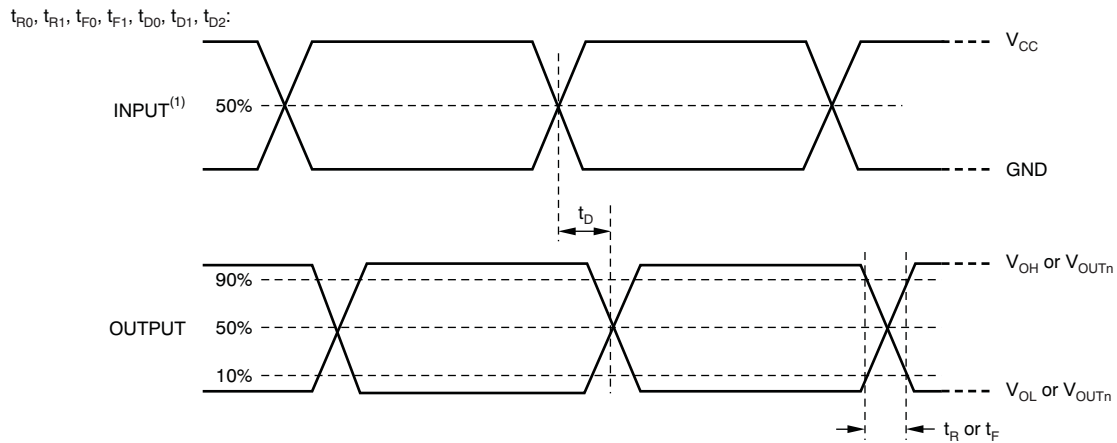


## TIMING DIAGRAMS



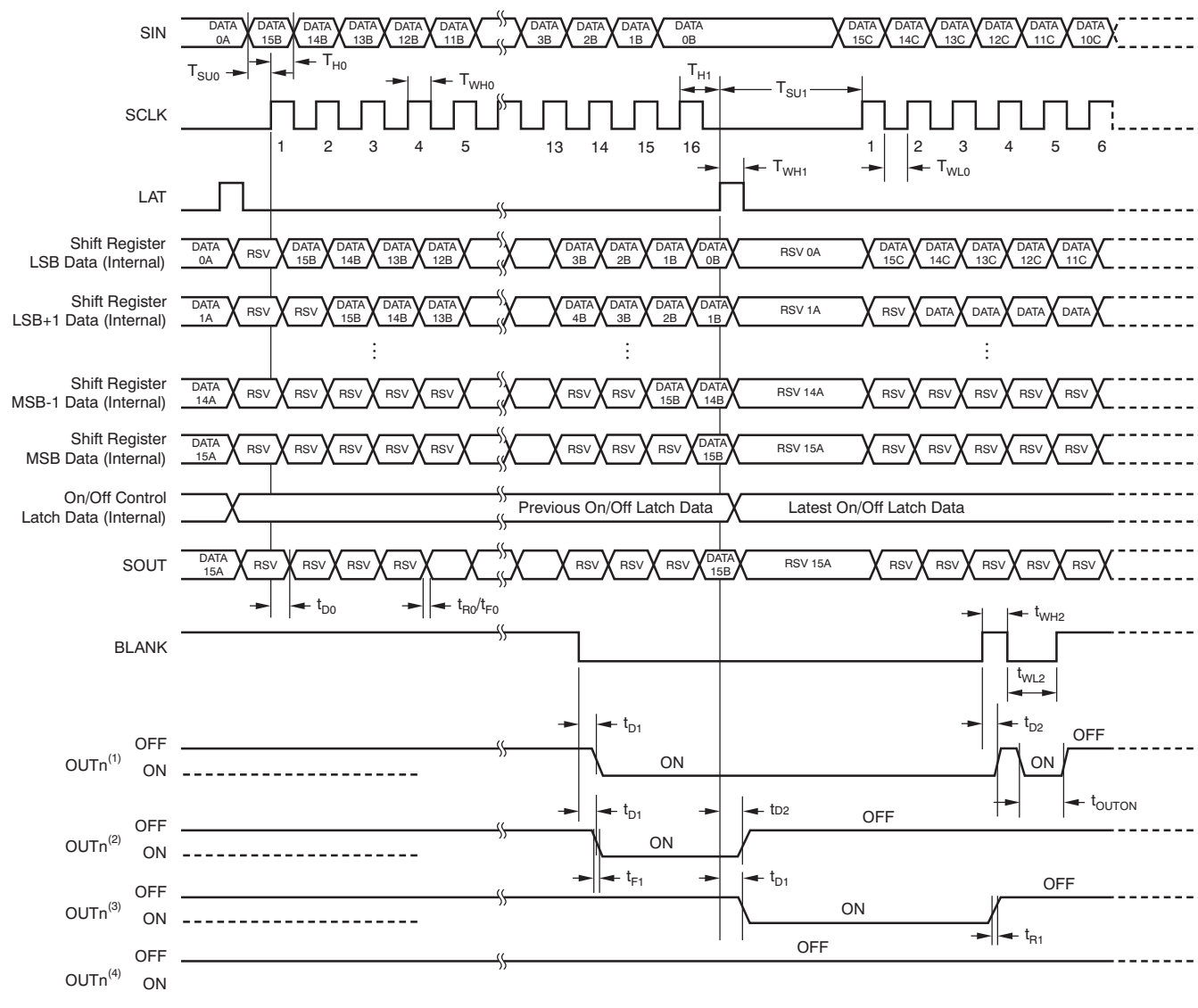
(1) Input pulse rise and fall time is 1 ns to 3 ns.

**Figure 7. Input Timing**



(1) Input pulse rise and fall time is 1 ns to 3 ns.

**Figure 8. Output Timing**



- (1) On/off latched data are '1'.
- (2) On/off latched data are changed from '1' to '0' at the second LAT signal.
- (3) On/off latched data are changed from '0' to '1' at the second LAT signal.
- (4) On/off latched data are '0'.

**Figure 9. Timing Diagram**

## TYPICAL CHARACTERISTICS

At  $V_{CC} = 3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**REFERENCE RESISTOR  
vs OUTPUT CURRENT**

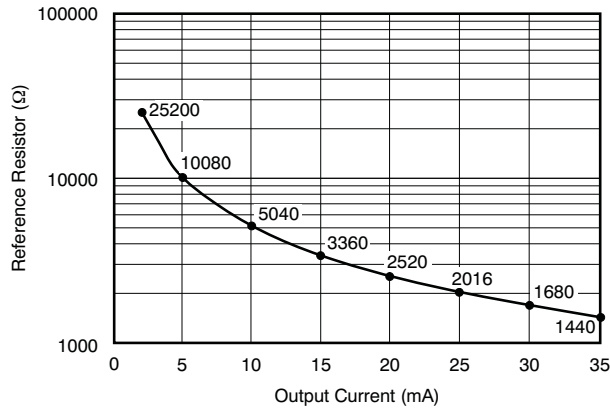


Figure 10.

**POWER DISSIPATION RATE  
vs FREE-AIR TEMPERATURE**

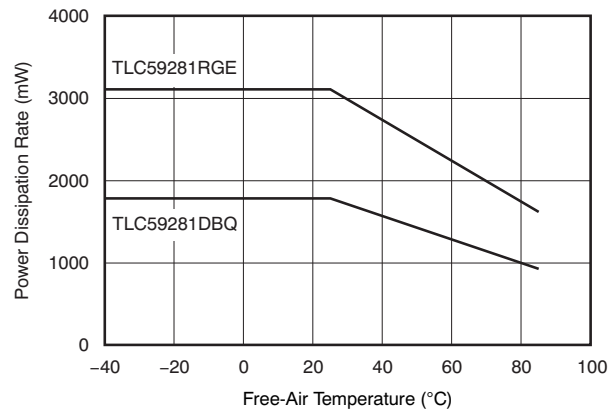


Figure 11.

**OUTPUT CURRENT vs  
OUTPUT VOLTAGE**

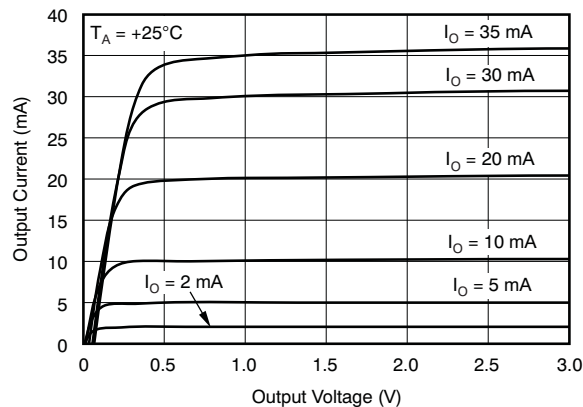


Figure 12.

**OUTPUT CURRENT vs  
OUTPUT VOLTAGE**

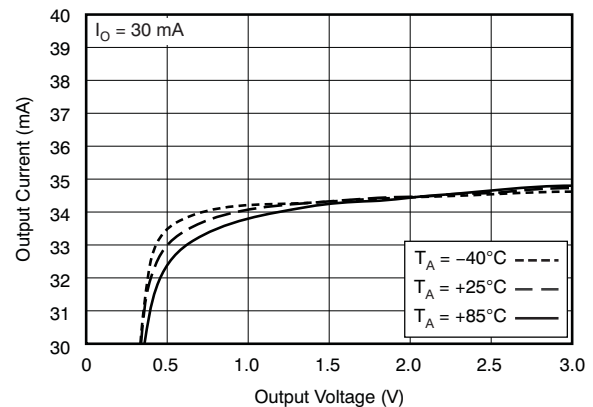


Figure 13.

**$\Delta I_{OLC}$  vs AMBIENT TEMPERATURE**

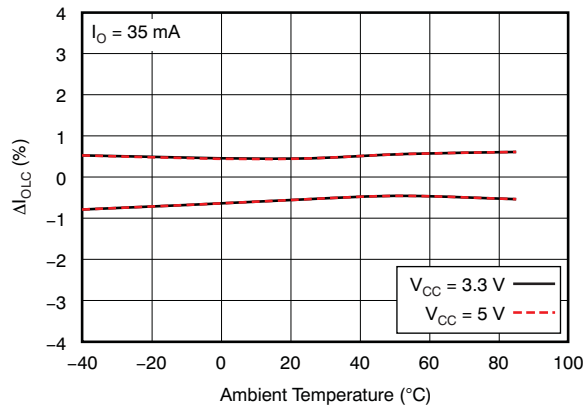


Figure 14.

**$\Delta I_{OLC}$  vs OUTPUT CURRENT**

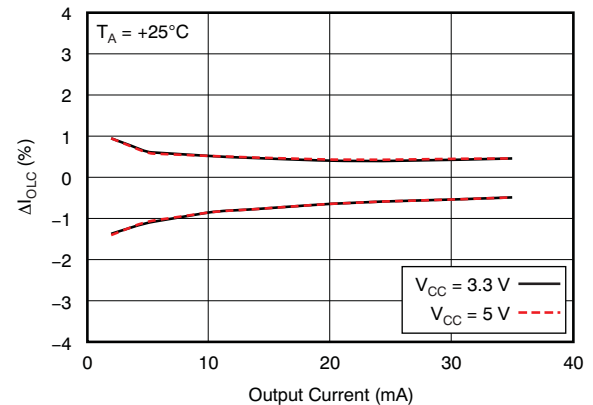
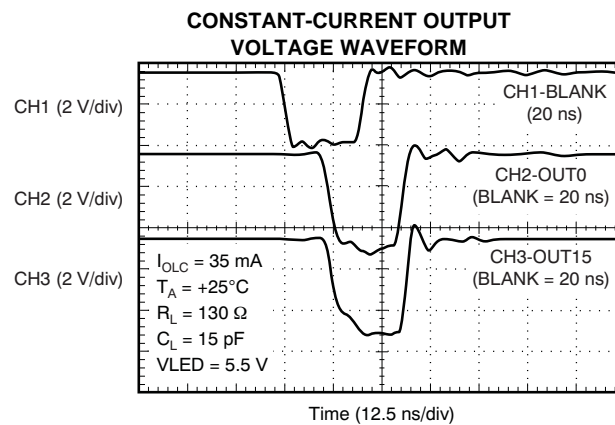


Figure 15.

**TYPICAL CHARACTERISTICS (continued)**

At  $V_{CC} = 3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise noted.



**Figure 16.**

## DETAILED DESCRIPTION

### SETTING FOR THE CONSTANT SINK CURRENT VALUE

The constant-current values are determined by an external resistor ( $R_{IREF}$ ) placed between IREF and GND. The resistor ( $R_{IREF}$ ) value is calculated by [Equation 1](#).

$$R_{IREF} \text{ (k}\Omega\text{)} = \frac{V_{IREF} \text{ (V)}}{I_{OLC} \text{ (mA)}} \times 42$$

Where:

$V_{IREF}$  = the internal reference voltage on the IREF pin (typically 1.20 V) (1)

$I_{OLC}$  must be set in the range of 2 mA to 35 mA. The constant sink current characteristic for the external resistor value is shown in [Figure 10](#). [Table 1](#) describes the constant-current output versus external resistor value.

**Table 1. Constant-Current Output versus External Resistor Value**

| $I_{OLCMax}$ (mA, Typical) | $R_{IREF}$ (k $\Omega$ ) |
|----------------------------|--------------------------|
| 35                         | 1.44                     |
| 30                         | 1.68                     |
| 25                         | 2.02                     |
| 20                         | 2.52                     |
| 15                         | 3.36                     |
| 10                         | 5.04                     |
| 5                          | 10.1                     |
| 2                          | 25.2                     |

### CONSTANT-CURRENT DRIVER ON/OFF CONTROL

When BLANK is low, the corresponding output is turned on if the data in the on/off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in [Table 2](#).

**Table 2. On/Off Control Data Truth Table**

| ON/OFF CONTROL LATCH DATA | CONSTANT-CURRENT OUTPUT STATUS |
|---------------------------|--------------------------------|
| 0                         | Off                            |
| 1                         | On                             |

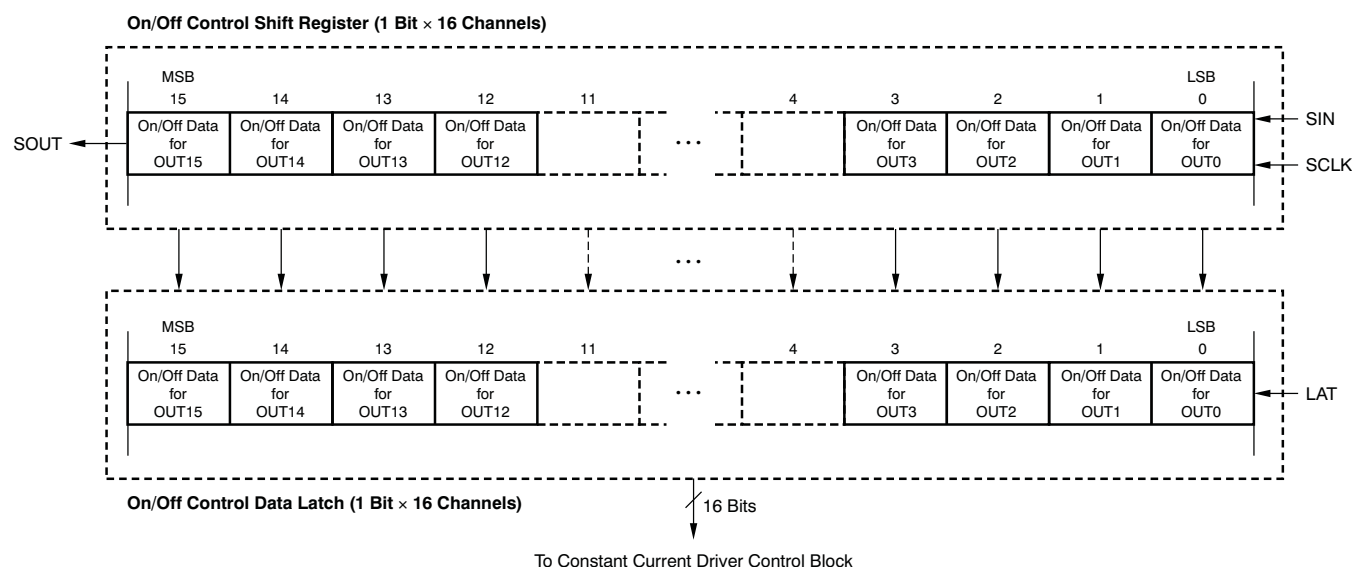
When the IC is initially powered on, the data in the on/off control shift register and data latch are not set to the respective default value. Therefore, the on/off control data must be written to the data latch before turning the constant-current output on. BLANK should be at a high level when powered on because the constant-current may be turned on as a result of random data in the on/off control latch.

The on/off data corresponding to any unconnected OUTn outputs should be set to '0' before turning on the remaining outputs. Otherwise, the supply current ( $I_{CC}$ ) increases while the LEDs are on.

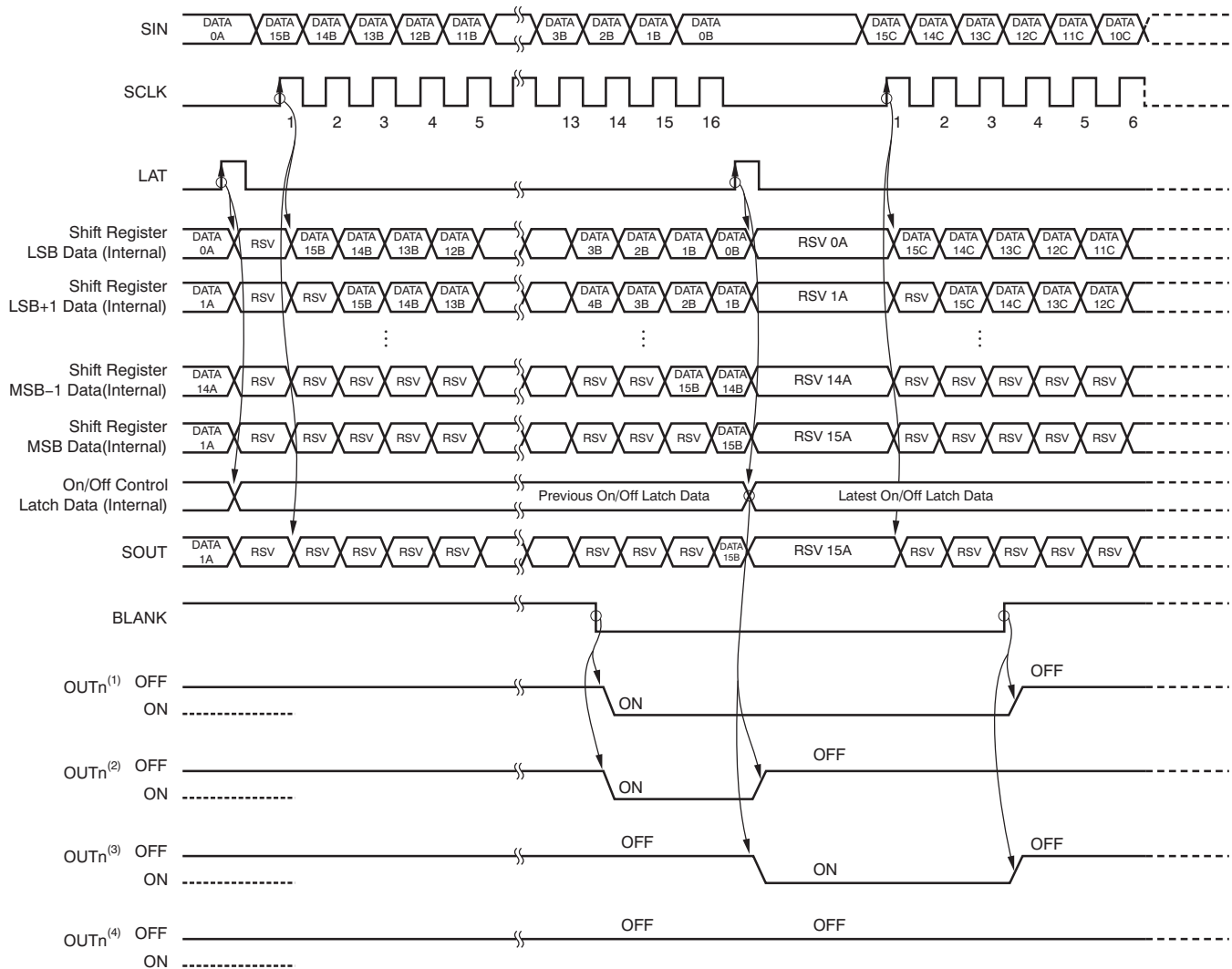
## REGISTER CONFIGURATION

The TLC59281 has an on/off control data shift register and data latch. Both the on/off control shift register and latch are 16 bits long and are used to turn the constant-current drivers on and off. Figure 17 shows the shift register and latch configuration. The data at the SIN pin is shifted in to the LSB of the shift register at the rising edge of the SCLK pin; SOUT data change at the rising edge of SCLK. The timing diagram for data writing is shown in Figure 18. The driver on/off is controlled by the data in the on/off control data latch.

The on/off data are latched into the data latch by a rising edge of LAT after the data are written into the on/off control shift register by SIN and SCLK. At the same time, the data in the on/off control shift register are replaced with TI reserved data for production test. Therefore, LAT must be input only once after the on/off data update to avoid the on/off control data latch being replaced with TI reserved data in the shift register. When the IC initially powers on, the data in the on/off control shift register and latch are not set to the default values; on/off control data must be written to the on/off control data latch before turning the constant-current output on. BLANK should be high when the IC is powered on because the constant-current may be turned on at that time as a result of random values in the on/off data latch. All constant-current outputs are forced off when BLANK is high.



**Figure 17. On/Off Control Shift Register and Latch Configuration**



- (1) On/off latched data are '1'.
- (2) On/off latched data are changed from '1' to '0' at the second LAT signal.
- (3) On/off latched data are changed from '0' to '1' at the second LAT signal.
- (4) On/off latched data are '0'.

**Figure 18. On/Off Control Operation**

## LAYOUT CONSIDERATIONS

The output current transient time in the TLC59281 is very fast. In addition, all outputs turn on or off at the same time to minimize the output on-time error. This high current demand can cause GND to shift in the entire system, and lead to false triggering of signals. To overcome this issue, design all GND lines to be as wide and short as possible in order to reduce parasitic inductance and resistance.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (September 2010) to Revision B | Page |
|--|------|
|--|------|

- |  |    |
|--|----|
| • Added <i>Layout Considerations</i> section ..... | 15 |
|--|----|

| Changes from Original (January 2010) to Revision A | Page |
|--|------|
|--|------|

- |  |   |
|--|---|
| • Changed SO-24 to SSOP-24/QSOP-24 in Package/Ordering Information table ..... | 2 |
| • Changed SO-24 to SSOP-24/QSOP-24 in Dissipation Ratings table .....          | 2 |
| • Changed SO-24 to SSOP-24/QSOP-24 in DBQ pinout .....                         | 6 |



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TLC59281DBQ      | ACTIVE        | SSOP         | DBQ                | 24   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | TLC59281                 | <a href="#">Samples</a> |
| TLC59281DBQR     | ACTIVE        | SSOP         | DBQ                | 24   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | TLC59281                 | <a href="#">Samples</a> |
| TLC59281RGE      | PREVIEW       |              |                    | 24   |             | TBD                        | Call TI          | Call TI              | -40 to 85    |                          |                         |
| TLC59281RGER     | ACTIVE        | VQFN         | RGE                | 24   | 3000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | TLC<br>59281             | <a href="#">Samples</a> |
| TLC59281RGET     | ACTIVE        | VQFN         | RGE                | 24   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  |              | TLC<br>59281             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC59281RGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TLC59281RGET | VQFN         | RGE             | 24   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

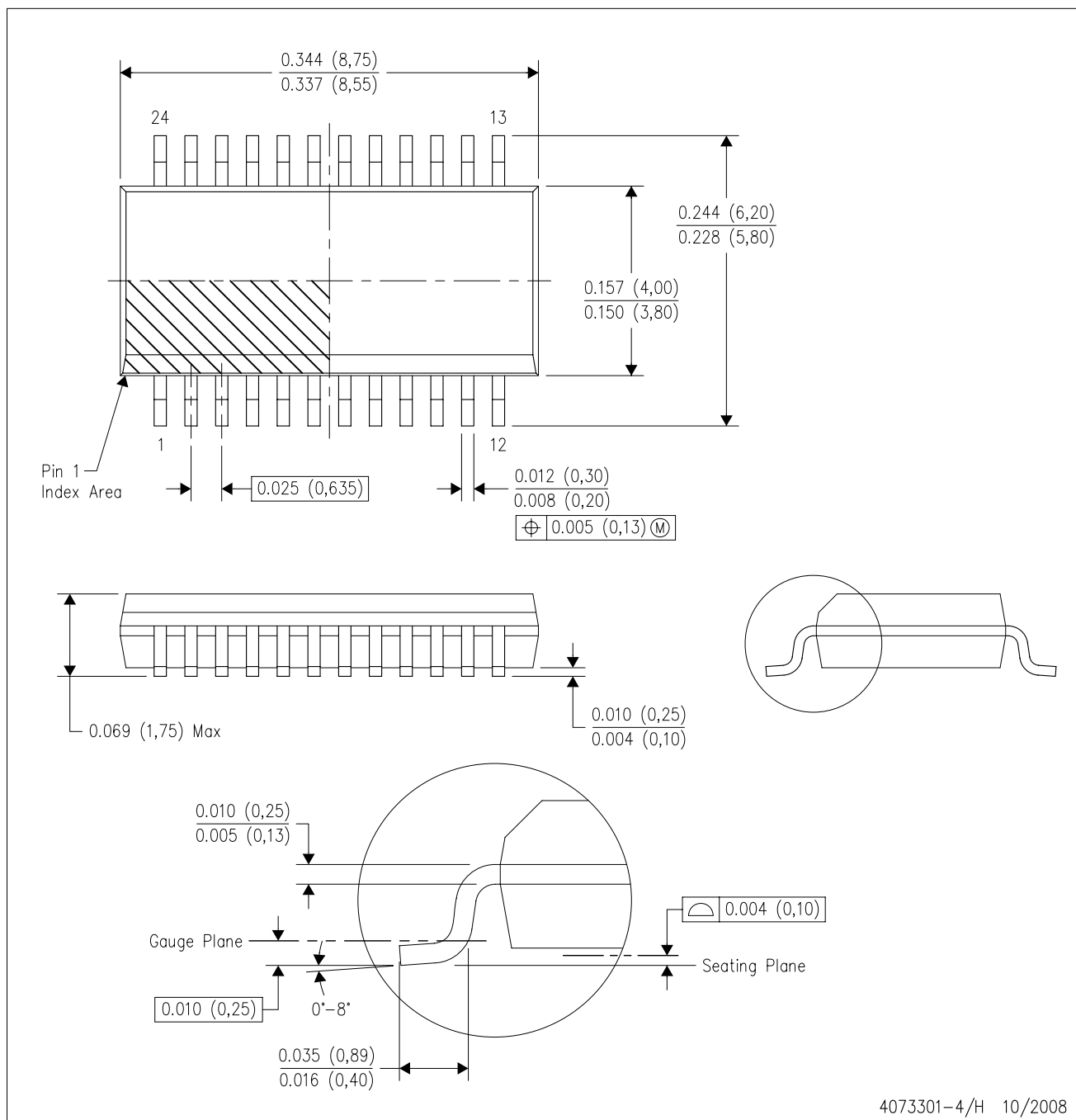


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC59281RGER | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 35.0        |
| TLC59281RGET | VQFN         | RGE             | 24   | 250  | 210.0       | 185.0      | 35.0        |

DBQ (R-PDSO-G24)

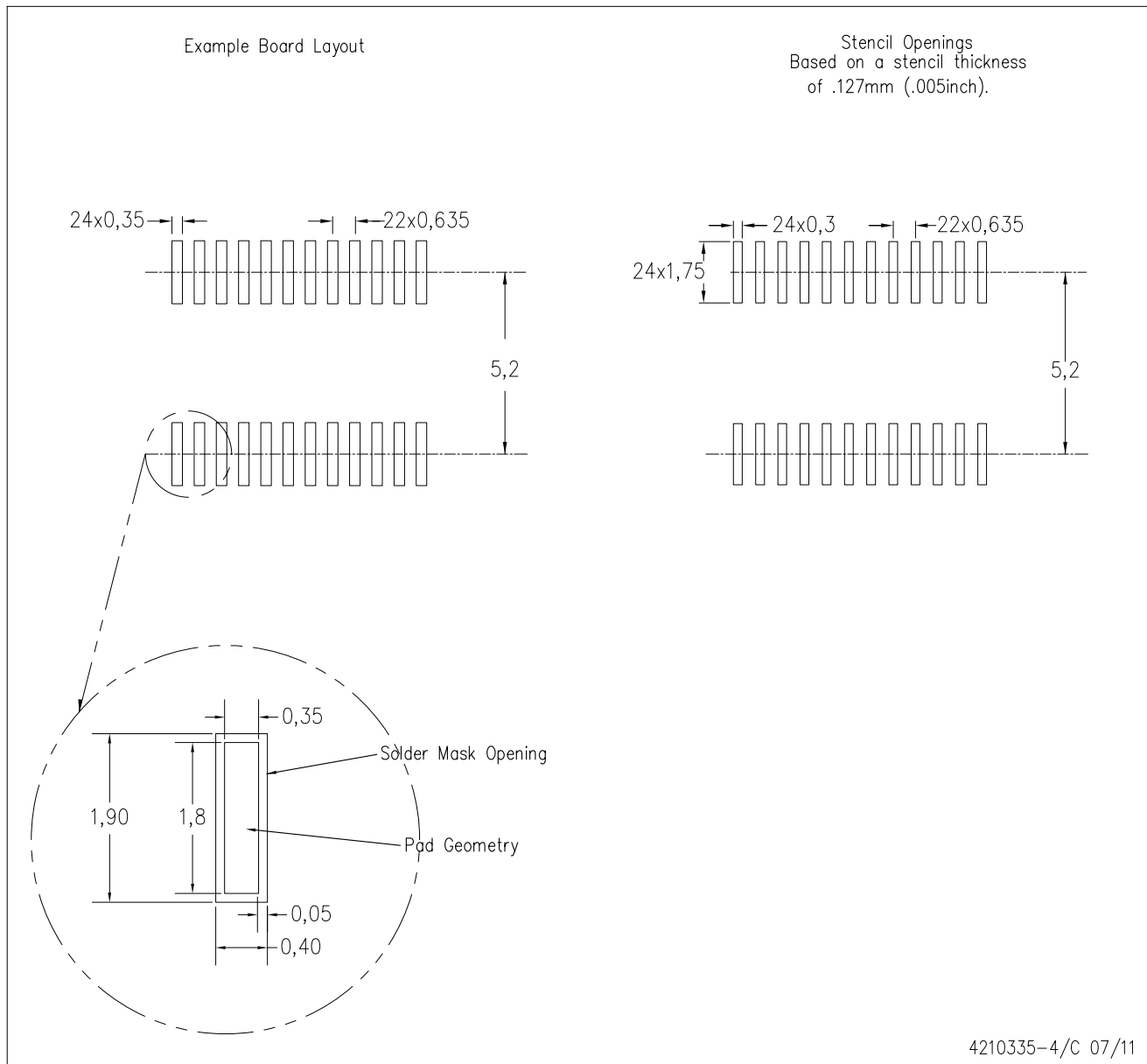
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

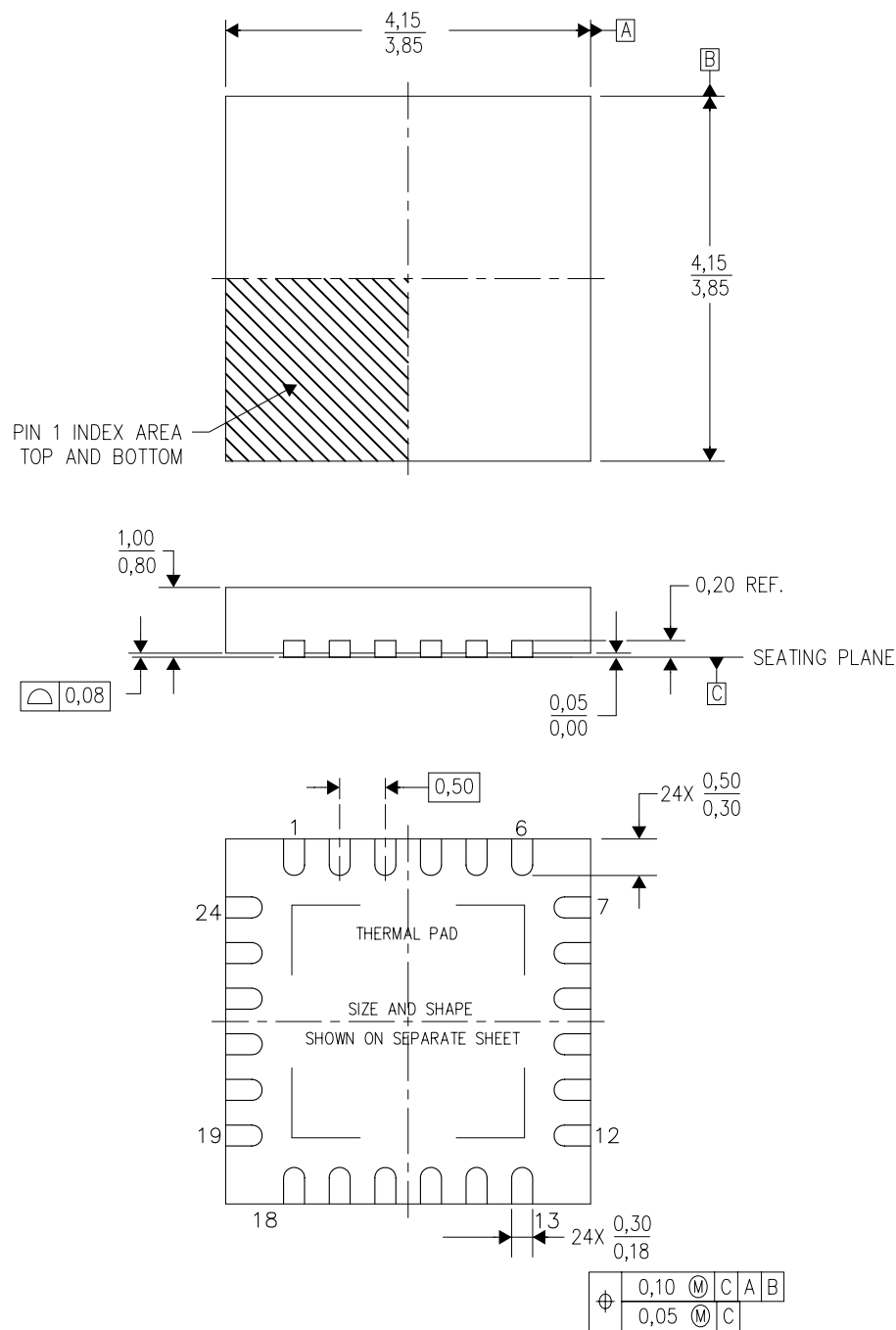
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

RGE (S-PVQFN-N24)

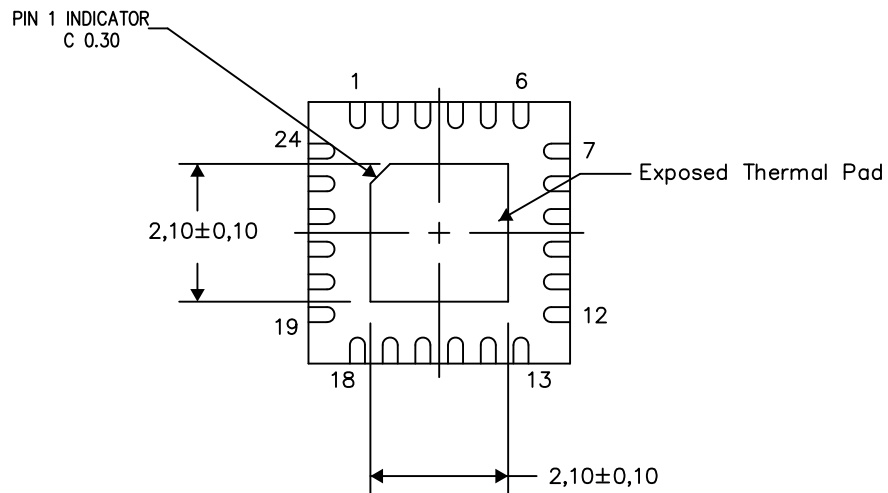
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

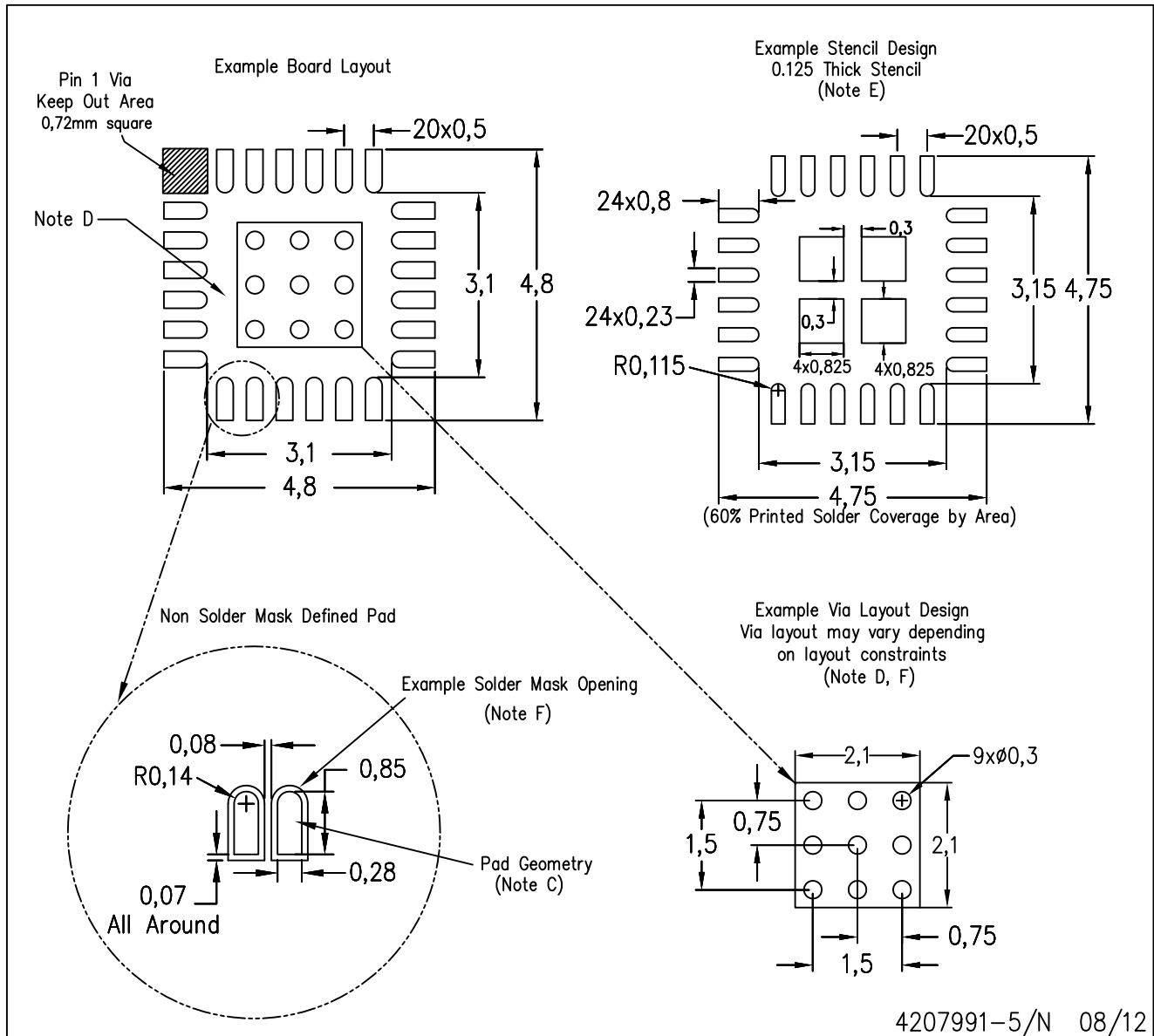
4206344-6/AC 03/13

NOTES: A. All linear dimensions are in millimeters



RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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