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R8C/22 Group, R8C/23 Group
Hardware Manual

RENESAS MCU
R8C FAMILY / R8C/2x SERIES

Hardware Manual

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/22 Group and R8C/23 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Technology Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/22 Group, R8C/23 Group Datasheet	REJ03B0097
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/22 Group, R8C/23 Group Hardware Manual	This hardware manual
Software manual	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Technology Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

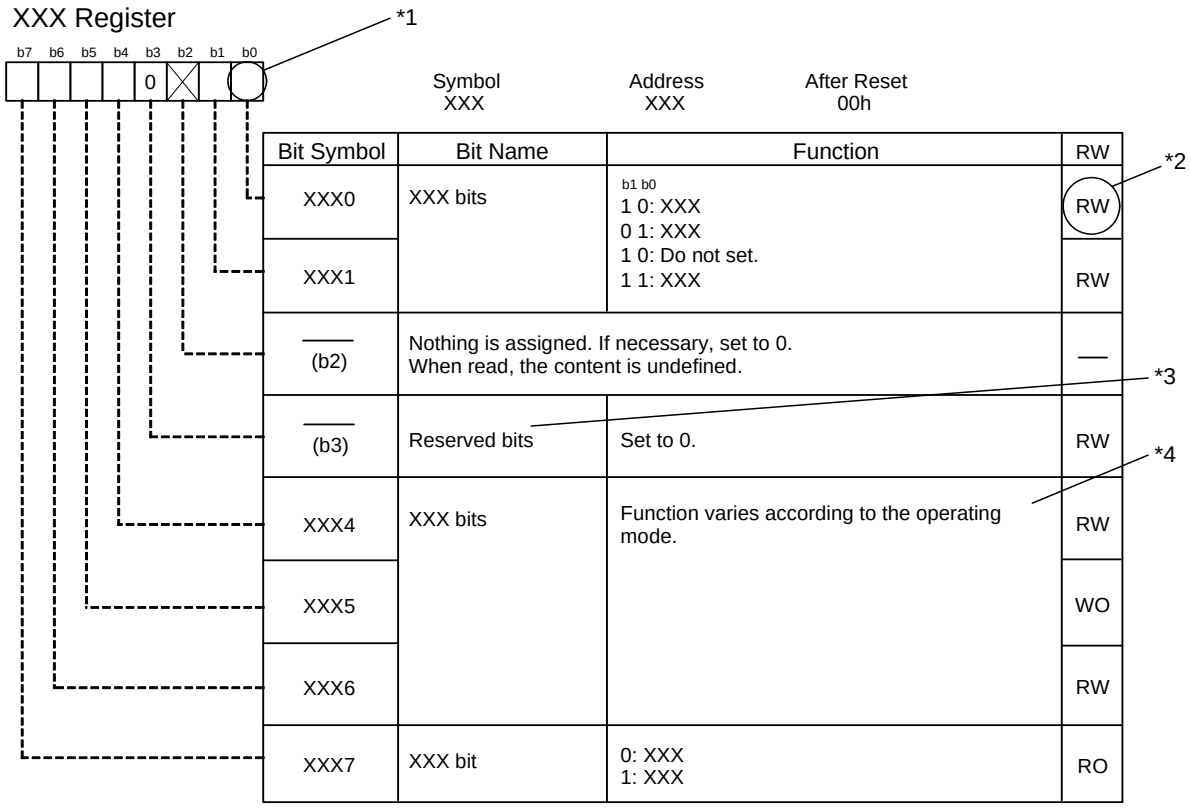
(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.



*1

Blank: Set to 0 or 1 according to the application.
0: Set to 0.
1: Set to 1.
X: Nothing is assigned.

*2

RW: Read and write.
RO: Read only.
WO: Write only.
–: Nothing is assigned.

*3

- Reserved bit
  Reserved bit. Set to specified value.

*4

- Nothing is assigned
  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value
  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.
  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input / Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver / Transmitter
VCO	Voltage Controlled Oscillator

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0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	69
0005h	Processor Mode Register 1	PM1	69
0006h	System Clock Control Register 0	CM0	73
0007h	System Clock Control Register 1	CM1	74
0008h			
0009h			
000Ah	Protect Register	PRCR	95
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	75
000Dh	Watchdog Timer Reset Register	WDTR	125
000Eh	Watchdog Timer Start Register	WDTS	125
000Fh	Watchdog Timer Control Register	WDC	124
0010h	Address Match Interrupt Register 0	RMAD0	117
0011h			
0012h			
0013h	Address Match Interrupt Enable Register	AIER	117
0014h	Address Match Interrupt Register 1	RMAD1	117
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protect Mode Register	CSPR	125
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	76
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	76
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0034h			
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0037h	Voltage Monitor 2 Circuit Control Register	VW2C	40
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0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

Address	Register	Symbol	Page
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0041h			
0042h			
0043h	CAN0 Wake Up Interrupt Control Register	C01WKIC	101
0044h	CAN0 Successful Reception Interrupt Control Register	C0RECIC	101
0045h	CAN0 Successful Transmission Interrupt Control Register	C0TRMIC	101
0046h	CAN0 State/Error Interrupt Control Register	C01ERRIC	101
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	102
0049h	Timer RD1 Interrupt Control Register	TRD1IC	102
004Ah	Timer RE Interrupt Control Register	TREIC	101
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	101
004Eh	A/D Conversion Interrupt Control Register	ADIC	101
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register	SSUIC/IICIC	102
0050h			
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0052h	UART0 Receive Interrupt Control Register	S0RIC	101
0053h	UART1 Transmit Interrupt Control Register	S1TIC	101
0054h	UART1 Receive Interrupt Control Register	S1RIC	101
0055h	INT2 Interrupt Control Register	INT2IC	103
0056h	Timer RA Interrupt Control Register	TRAIC	101
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	101
0059h	INT1 Interrupt Control Register	INT1IC	103
005Ah	INT3 Interrupt Control Register	INT3IC	103
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	103
005Eh			
005Fh			
0060h			
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0062h			
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0064h			
0065h			
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NOTE:
1. Blank columns are all reserved space. No access is allowed.

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00A0h	UART0 Transmit/Receive Mode Register	U0MR	278
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00A6h	UART0 Receive Buffer Register	U0RB	277
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00E0h	Port P0 Register	P0	55
00E1h	Port P1 Register	P1	55
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NOTE:

1. Blank columns are all reserved space. No access is allowed.

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1. Blank columns are all reserved space. No access is allowed.

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135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	78
1360h	CAN0 Slot 0: Identifier/DLC		372, 373
1361h			
1362h			
1363h			
1364h			
1365h			
1366h	CAN0 Slot 0: Data Field		
1367h			
1368h			
1369h			
136Ah			
136Bh			
136Ch			
136Dh			
136Eh	CAN0 Slot 0: Time Stamp		
136Fh			
1370h	CAN0 Slot 1: Identifier/DLC		
1371h			
1372h			
1373h			
1374h			
1375h			
1376h	CAN0 Slot 1: Data Field		
1377h			
1378h			
1379h			
137Ah			
137Bh			
137Ch			
137Dh			
137Eh	CAN0 Slot 1: Time Stamp		
137Fh			

NOTE:

1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Page
1380h	CAN0 Slot 2: Identifier/DLC		372, 373
1381h			
1382h			
1383h			
1384h			
1385h			
1386h	CAN0 Slot 2: Data Field		
1387h			
1388h			
1389h			
138Ah			
138Bh			
138Ch			
138Dh			
138Eh	CAN0 Slot 2: Time Stamp		
138Fh			
1390h	CAN0 Slot 3: Identifier/DLC		
1391h			
1392h			
1393h			
1394h			
1395h			
1396h	CAN0 Slot 3: Data Field		
1397h			
1398h			
1399h			
139Ah			
139Bh			
139Ch			
139Dh			
139Eh	CAN0 Slot 3: Time Stamp		
139Fh			
13A0h	CAN0 Slot 4: Identifier/DLC		
13A1h			
13A2h			
13A3h			
13A4h			
13A5h			
13A6h	CAN0 Slot 4: Data Field		
13A7h			
13A8h			
13A9h			
13AAh			
13ABh			
13ACh			
13ADh			
13AEh	CAN0 Slot 4: Time Stamp		
13AFh			
13B0h	CAN0 Slot 5: Identifier/DLC		
13B1h			
13B2h			
13B3h			
13B4h			
13B5h			
13B6h	CAN0 Slot 5: Data Field		
13B7h			
13B8h			
13B9h			
13BAh			
13BBh			
13BCh			
13BDh			
13BEh	CAN0 Slot 5: Time Stamp		
13BFh			

Address	Register	Symbol	Page
13C0h	CAN0 Slot 6: Identifier/DLC		372, 373
13C1h			
13C2h			
13C3h			
13C4h			
13C5h			
13C6h	CAN0 Slot 6: Data Field		
13C7h			
13C8h			
13C9h			
13CAh			
13CBh			
13CCh			
13CDh			
13CEh	CAN0 Slot 6: Time Stamp		
13CFh			
13D0h	CAN0 Slot 7: Identifier/DLC		
13D1h			
13D2h			
13D3h			
13D4h			
13D5h			
13D6h	CAN0 Slot 7: Data Field		
13D7h			
13D8h			
13D9h			
13DAh			
13DBh			
13DCh			
13DDh			
13DEh	CAN0 Slot 7: Time Stamp		
13DFh			
13E0h	CAN0 Slot 8: Identifier/DLC		
13E1h			
13E2h			
13E3h			
13E4h			
13E5h			
13E6h	CAN0 Slot 8: Data Field		
13E7h			
13E8h			
13E9h			
13EAh			
13EBh			
13ECh			
13EDh			
13EEh	CAN0 Slot 8: Time Stamp		
13EFh			
13F0h	CAN0 Slot 9: Identifier/DLC		
13F1h			
13F2h			
13F3h			
13F4h			
13F5h			
13F6h	CAN0 Slot 9: Data Field		
13F7h			
13F8h			
13F9h			
13FAh			
13FBh			
13FCh			
13FDh			
13FEh	CAN0 Slot 9: Time Stamp		
13FFh			

NOTE:

1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Page
1400h	CAN0 Slot 10: Identifier/DLC		372, 373
1401h			
1402h			
1403h			
1404h			
1405h			
1406h	CAN0 Slot 10: Data Field		
1407h			
1408h			
1409h			
140Ah			
140Bh			
140Ch			
140Dh			
140Eh	CAN0 Slot 10: Time Stamp		
140Fh			
1410h	CAN0 Slot 11: Identifier/DLC		
1411h			
1412h			
1413h			
1414h			
1415h			
1416h	CAN0 Slot 11: Data Field		
1417h			
1418h			
1419h			
141Ah			
141Bh			
141Ch			
141Dh			
141Eh	CAN0 Slot 11: Time Stamp		
141Fh			
1420h	CAN0 Slot 12: Identifier/DLC		
1421h			
1422h			
1423h			
1424h			
1425h			
1426h	CAN0 Slot 12: Data Field		
1427h			
1428h			
1429h			
142Ah			
142Bh			
142Ch			
142Dh			
142Eh	CAN0 Slot 12: Time Stamp		
142Fh			
1430h	CAN0 Slot 13: Identifier/DLC		
1431h			
1432h			
1433h			
1434h			
1435h			
1436h	CAN0 Slot 13: Data Field		
1437h			
1438h			
1439h			
143Ah			
143Bh			
143Ch			
143Dh			
143Eh	CAN0 Slot 13: Time Stamp		
143Fh			

Address	Register	Symbol	Page
1440h	CAN0 Slot 14: Identifier/DLC		372, 373
1441h			
1442h			
1443h			
1444h			
1445h			
1446h	CAN0 Slot 14: Data Field		
1447h			
1448h			
1449h			
144Ah			
144Bh			
144Ch			
144Dh			
144Eh	CAN0 Slot 14: Time Stamp		
144Fh			
1450h	CAN0 Slot 15: Identifier/DLC		
1451h			
1452h			
1453h			
1454h			
1455h			
1456h	CAN0 Slot 15: Data Field		
1457h			
1458h			
1459h			
145Ah			
145Bh			
145Ch			
145Dh			
145Eh	CAN0 Slot 15: Time Stamp		
145Fh			
1460h	CAN0 Global Mask Register	C0GMR	374
1461h			
1462h			
1463h			
1464h			
1465h			
1466h	CAN0 Local Mask A Register	C0LMAR	
1467h			
1468h			
1469h			
146Ah			
146Bh			
146Ch	CAN0 Local Mask B Register	C0LMBR	
146Dh			
146Eh			
146Fh			
1470h			
1471h			
1472h			
1473h			
1474h			
1475h			

FFFFh	Option Function Select Register	OFS	30, 124, 420

NOTE:
1. Blank columns are all reserved space. No access is allowed.

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using the R8C CPU core and is packaged in a 48-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed. This MCU is equipped with one CAN module and suited to in-vehicle or FA networking.
Furthermore, the data flash (1 KB x 2 blocks) is embedded in the R8C/23 Group.
The difference between R8C/22 and R8C/23 Groups is only the existence of the data flash. Their peripheral functions are the same.

1.1 Applications

Automotive, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/22 Group and Table 1.2 outlines the Functions and Specifications for R8C/23 Group.

Table 1.1 Functions and Specifications for R8C/22 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/22 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	CAN module	1 channel with 2.0B specification: 16 slots
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupt	Internal: 14 sources, External: 6 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(D, J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 12.5 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 6.0 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

Table 1.2 Functions and Specifications for R8C/23 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.4 Product Information for R8C/23 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I^2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (Timer RA, UART0)
	CAN module	1 channel with 2.0B specification: 16 slots
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 14 sources, External: 6 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(D, J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 12.5 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 6.0 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash)
		1,000 times (program ROM)
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I^2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

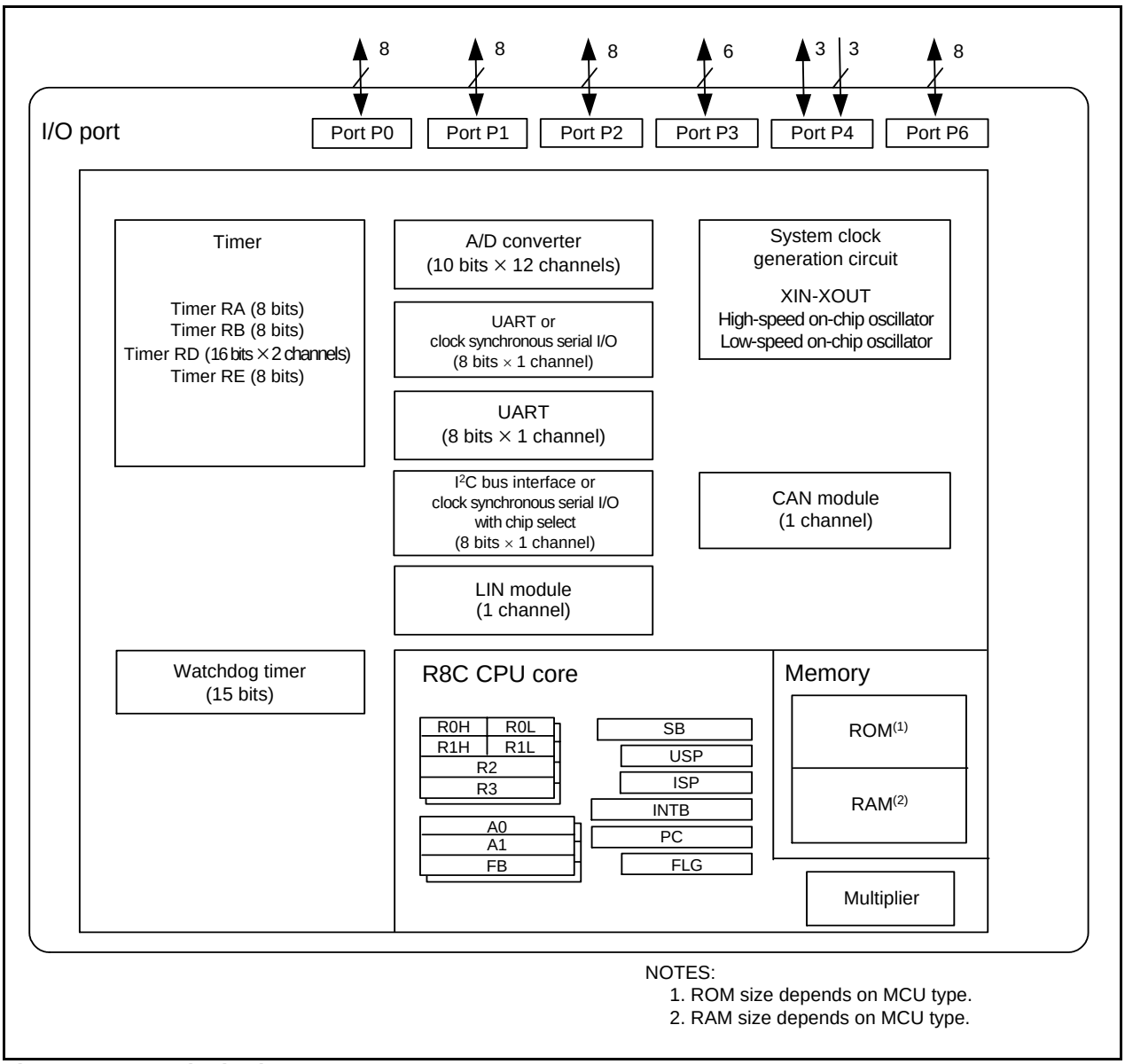


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/22 Group and Table 1.4 lists Product Information for R8C/23 Group.

Table 1.3 Product Information for R8C/22 Group **Current of Aug. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21226DFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21227DFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228DFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F21226JFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	J version	
R5F21227JFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228JFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AJFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CJFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		
R5F21226KFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	K version	
R5F21227KFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228KFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AKFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CKFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.

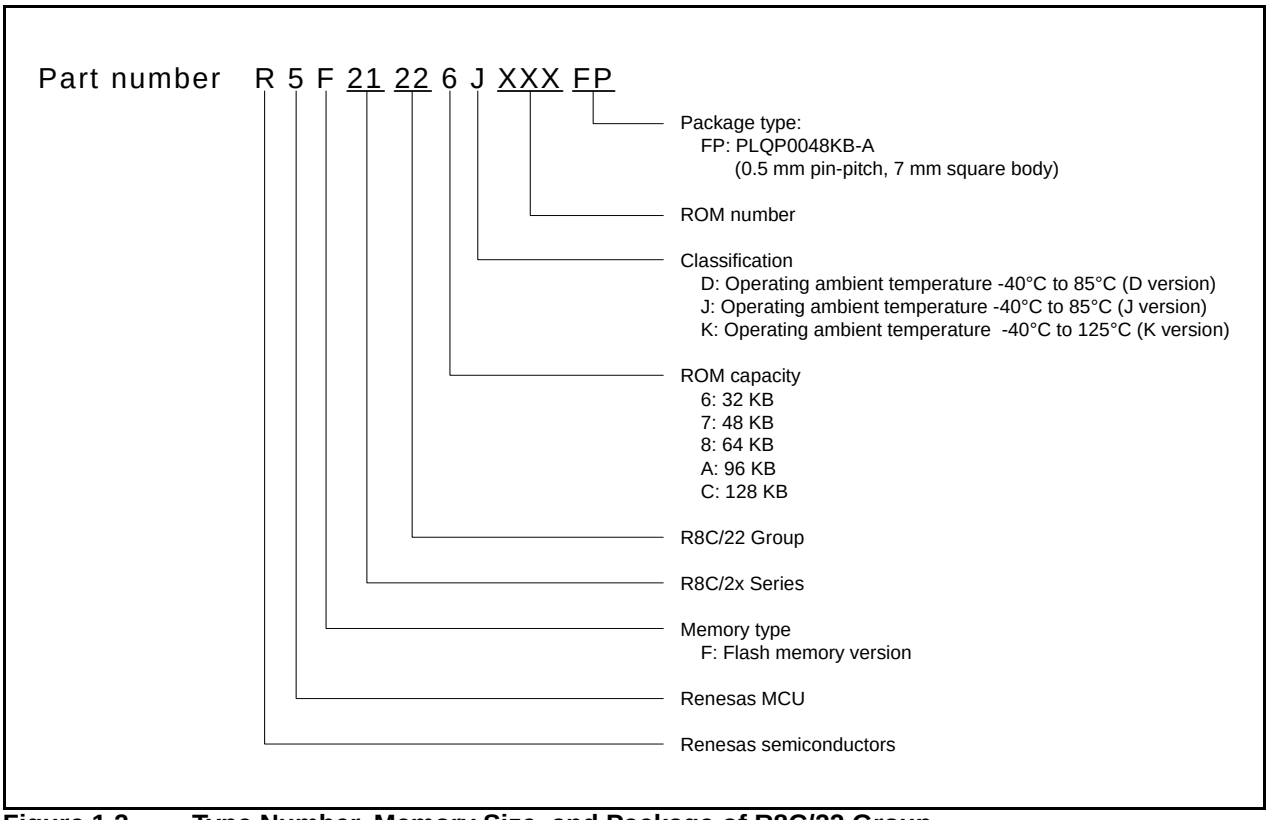


Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group

Table 1.4 Product Information for R8C/23 Group Current of Aug. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data Flash				
R5F21236DFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21237DFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238DFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F21236JFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	J version	
R5F21237JFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238JFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AJFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CJFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		
R5F21236KFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	K version	
R5F21237KFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238KFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AKFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CKFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.

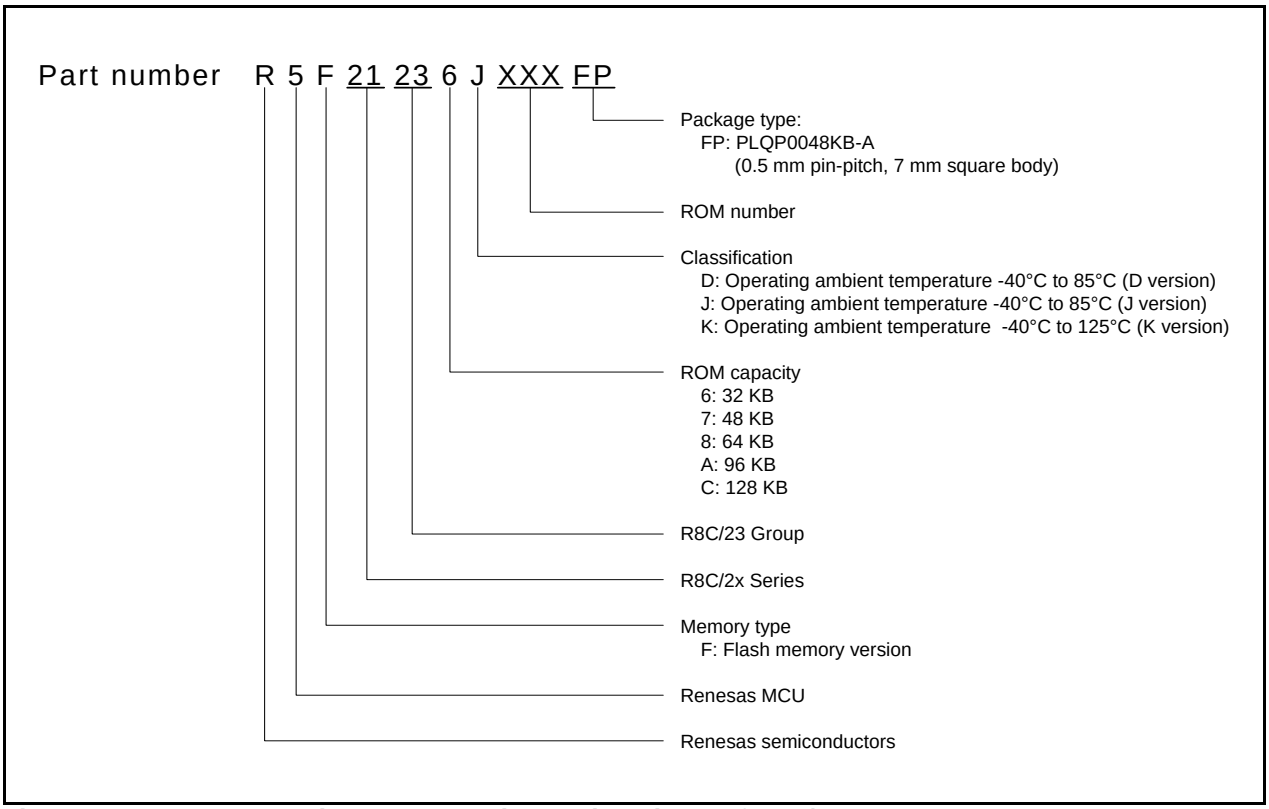
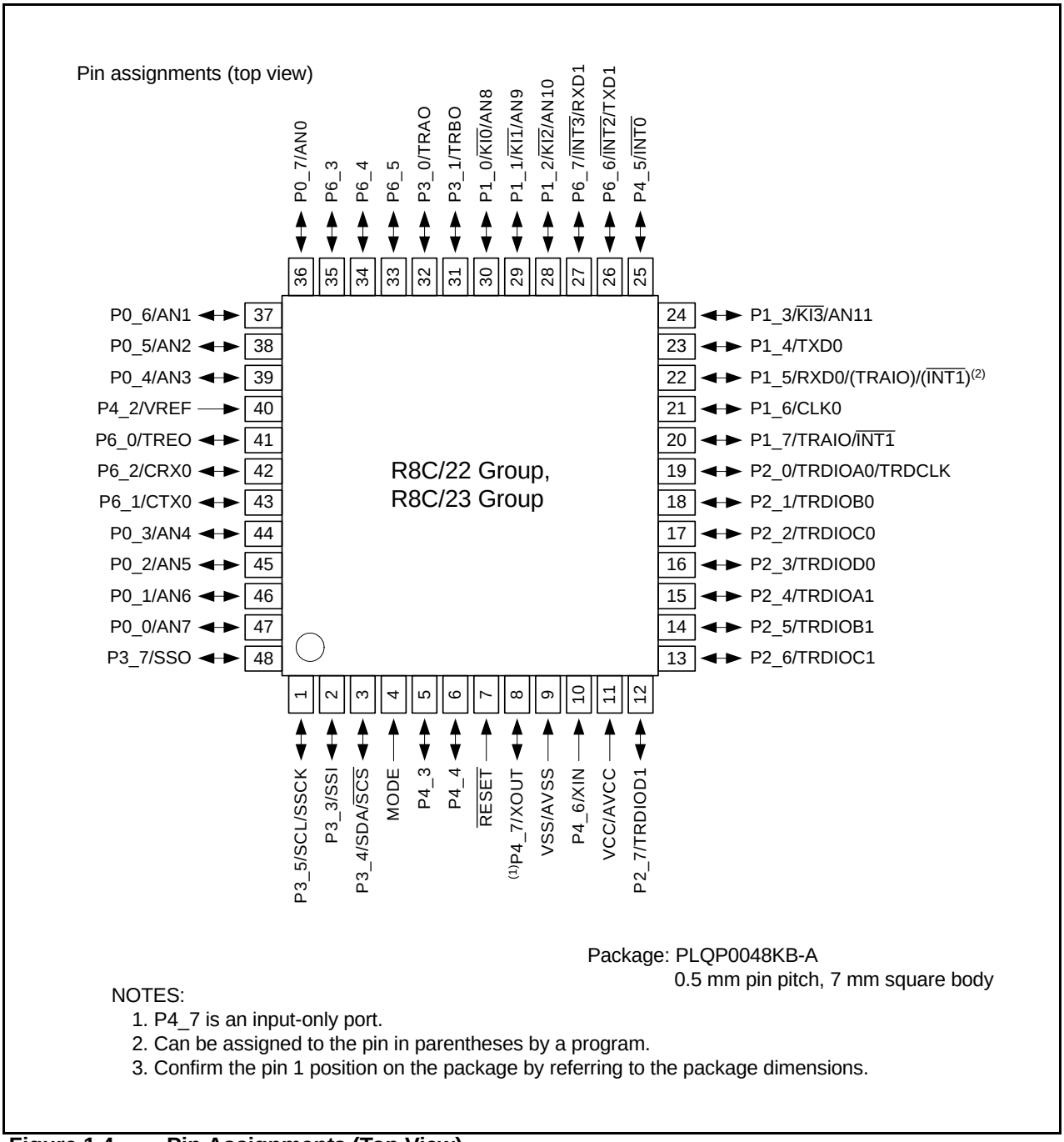


Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).



Package: PLQP0048KB-A
0.5 mm pin pitch, 7 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists the Pin Functions and Table 1.6 lists the Pin Name Information by Pin Number.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Applies the power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN Clock Input	XIN	I	These pins are provided for the XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XIN Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	O	Divided clock output pin.
Serial Interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0, RXD1	I	Serial data input pins.
	TXD0, TXD1	O	Serial data output pins.
I^2C Bus Interface	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
Clock Synchronous Serial I/O with Chip Select	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
CAN Module	CRX0	I	CAN data input pin.
	CTX0	O	CAN data output pin.
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter.
A/D Converter	AN0 to AN11	I	Analog input pins to A/D converter.
I/O Port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port contains an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by a program.
Input Port	P4_2, P4_6, P4_7	I	Input only ports.

I: Input O: Output I/O: Input and output

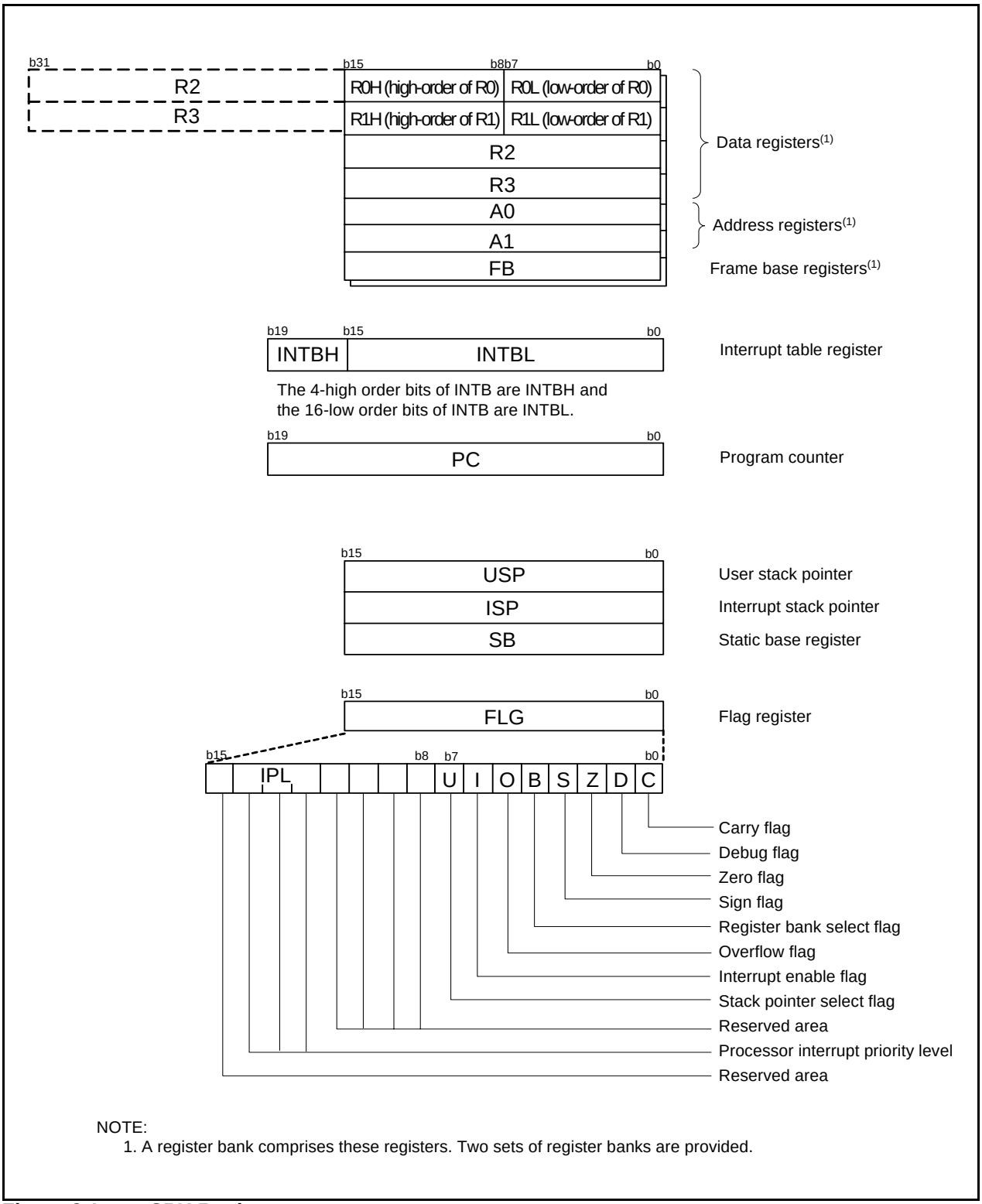
Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules						
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C Bus Interface	CAN Module	A/D Converter
1		P3_5				SSCK	SCL		
2		P3_3				SSI			
3		P3_4				$\overline{SCS}$	SDA		
4	MODE								
5		P4_3							
6		P4_4							
7	$\overline{RESET}$								
8	XOUT	P4_7							
9	VSS/AVSS								
10	XIN	P4_6							
11	VCC/AVCC								
12		P2_7		TRDIOD1					
13		P2_6		TRDIOC1					
14		P2_5		TRDIOB1					
15		P2_4		TRDIOA1					
16		P2_3		TRDIOD0					
17		P2_2		TRDIOC0					
18		P2_1		TRDIOB0					
19		P2_0		TRDIOA0/TRDCLK					
20		P1_7	$\overline{INT1}$	TRAIO					
21		P1_6			CLK0				
22		P1_5	($\overline{INT1}$)(1)	(TRAIO)(1)	RXD0				
23		P1_4			TXD0				
24		P1_3	$\overline{KI3}$						AN11
25		P4_5	$\overline{INT0}$	$\overline{INT0}$					
26		P6_6	$\overline{INT2}$		TXD1				
27		P6_7	$\overline{INT3}$		RXD1				
28		P1_2	$\overline{KI2}$						AN10
29		P1_1	$\overline{KI1}$						AN9
30		P1_0	$\overline{KI0}$						AN8
31		P3_1		TRBO					
32		P3_0		TRAO					
33		P6_5							
34		P6_4							
35		P6_3							
36		P0_7							AN0
37		P0_6							AN1
38		P0_5							AN2
39		P0_4							AN3
40	VREF	P4_2							
41		P6_0		TREO					
42		P6_2						CRX0	
43		P6_1						CTX0	
44		P0_3							AN4
45		P0_2							AN5
46		P0_1							AN6
47		P0_0							AN7
48		P3_7				SSO			

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.



NOTE:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3.
R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0.
A1 can be combined with A0 to be used a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB, a 20-bit register, indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.
The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU status.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation resulted in 0; otherwise, 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, 0.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is 0. The register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation resulted in an overflow; otherwise, 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

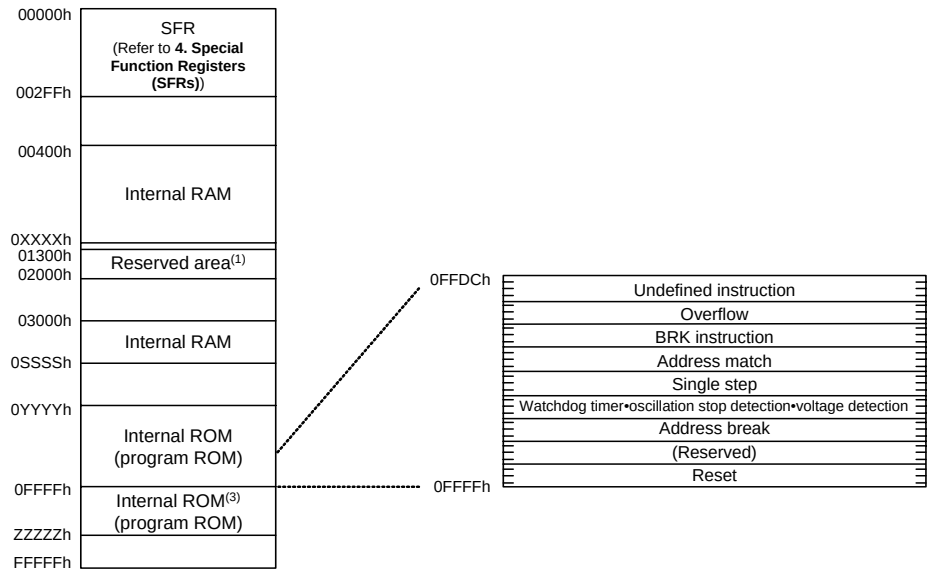
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/22 Group

Figure 3.1 shows a Memory Map of R8C/22 Group. The R8C/22 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh and 01300h to 0147Fh (SFR area for CAN). The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future user and cannot be accessed by users.



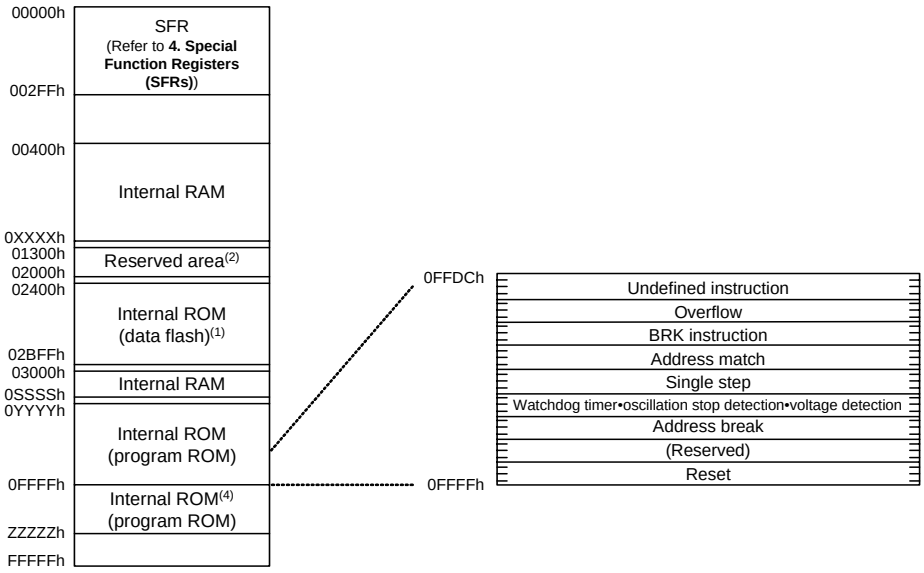
NOTES:
1. SFR area for CAN is allocated addresses 01300h to 0147Fh.
2. The blank regions are reserved. Do not access locations in these regions.
3. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21226DFP, R5F21226JFP, R5F21226KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21227DFP, R5F21227JFP, R5F21227KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21228DFP, R5F21228JFP, R5F21228KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2122AJFP, R5F2122AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2122CJFP, R5F2122CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.1 Memory Map of R8C/22 Group

3.2 R8C/23 Group

Figure 3.2 shows a Memory Map of R8C/23 Group. The R8C/23 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh and 01300h to 0147Fh (SFR area for CAN). The peripheral function control registers are allocated them. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. SFR area for CAN is allocated addresses 01300h to 0147Fh.
3. The blank regions are reserved. Do not access locations in these regions.
4. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21236DFP, R5F21236JFP, R5F21236KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21237DFP, R5F21237JFP, R5F21237KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21238DFP, R5F21238JFP, R5F21238KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2123AJFP, R5F2123AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2123CJFP, R5F2123CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.2 Memory Map of R8C/23 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function.
Table 4.1 to Table 4.13 list the SFR Information.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protect Mode Register	CSPR	00h 10000000b[8]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[6]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[7]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h			
0039h			
003Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1.
4. Power-on reset, voltage monitor 1 reset or the LVD0ON bit in the OFS register is set to 0.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.
6. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b7.
7. Software reset, the watchdog timer rest, and the voltage monitor 2 reset do not affect other than the b0 and b6.
8. The CSPROINI bit in the OFS register is 0.

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h	CAN0 Wake Up Interrupt Control Register	C01WKIC	XXXXX000b
0044h	CAN0 Successful Reception Interrupt Control Register	C0RECIC	XXXXX000b
0045h	CAN0 Successful Transmission Interrupt Control Register	C0TRMIC	XXXXX000b
0046h	CAN0 State/Error Interrupt Control Register	C01ERRIC	XXXXX000b
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register[2]	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)[1]

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H/IIC Bus Control Register 1[2]	SSCRH/ICCR1	00h
00B9h	SS Control Register L/IIC Bus Control Register 2[2]	SSCRL/ICCR2	01111101b
00BAh	SS Mode Register/IIC Bus Mode Register 1[2]	SSMR/ICMR	00011000b
00BBh	SS Enable Register/IIC Bus Interrupt Enable Register[2]	SSER/ICIER	00h
00BCh	SS Status Register/IIC Bus Status Register[2]	SSSR/ICSR	00h/0000X000b
00BDh	SS Mode Register 2/Slave Address Register[2]	SSMR2/SAR	00h
00BEh	SS Transmit Data Register/IIC Bus Transmit Data Register[2]	SSTDR/ICDRT	FFh
00BFh	SS Receive Data Register/IIC Bus Receive Data Register[2]	SSRDR/ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)(1)

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			

01FDh			
01FEh			
01FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)(1)

Address	Register	Symbol	After reset
1300h	CAN0 Message Control Register 0	C0MCTL0	00h
1301h	CAN0 Message Control Register 1	C0MCTL1	00h
1302h	CAN0 Message Control Register 2	C0MCTL2	00h
1303h	CAN0 Message Control Register 3	C0MCTL3	00h
1304h	CAN0 Message Control Register 4	C0MCTL4	00h
1305h	CAN0 Message Control Register 5	C0MCTL5	00h
1306h	CAN0 Message Control Register 6	C0MCTL6	00h
1307h	CAN0 Message Control Register 7	C0MCTL7	00h
1308h	CAN0 Message Control Register 8	C0MCTL8	00h
1309h	CAN0 Message Control Register 9	C0MCTL9	00h
130Ah	CAN0 Message Control Register 10	C0MCTL10	00h
130Bh	CAN0 Message Control Register 11	C0MCTL11	00h
130Ch	CAN0 Message Control Register 12	C0MCTL12	00h
130Dh	CAN0 Message Control Register 13	C0MCTL13	00h
130Eh	CAN0 Message Control Register 14	C0MCTL14	00h
130Fh	CAN0 Message Control Register 15	C0MCTL15	00h
1310h	CAN0 Control Register	C0CTLR	X0000001b
1311h			XX0X0000b
1312h	CAN0 Status Register	C0STR	00h
1313h			X0000001b
1314h	CAN0 Slot Status Register	C0SSTR	00h
1315h			00h
1316h	CAN0 Interrupt Control Register	C0ICR	00h
1317h			00h
1318h	CAN0 Extended ID Register	C0IDR	00h
1319h			00h
131Ah	CAN0 Configuration Register	C0CONR	XXh
131Bh			XXh
131Ch	CAN0 Receive Error Count Register	C0RECR	00h
131Dh	CAN0 Transmit Error Count Register	C0TECR	00h
131Eh			
131Fh			
1320h			
1321h			
1322h			
1323h			
1324h			
1325h			
1326h			
1327h			
1328h			
1329h			
132Ah			
132Bh			
132Ch			
132Dh			
132Eh			
132Fh			
1330h			
1331h			
1332h			
1333h			
1334h			
1335h			
1336h			
1337h			
1338h			
1339h			
133Ah			
133Bh			
133Ch			
133Dh			
133Eh			
133Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)(1)

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		XXh
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h	CAN0 Slot 1: Data Field		XXh
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)(1)

Address	Register	Symbol	After reset
1380h	CAN0 Slot 2: Identifier/DLC		XXh
1381h			XXh
1382h			XXh
1383h			XXh
1384h			XXh
1385h			XXh
1386h	CAN0 Slot 2: Data Field		XXh
1387h			XXh
1388h			XXh
1389h			XXh
138Ah			XXh
138Bh			XXh
138Ch			XXh
138Dh			XXh
138Eh	CAN0 Slot 2: Time Stamp		XXh
138Fh			XXh
1390h	CAN0 Slot 3: Identifier/DLC		XXh
1391h			XXh
1392h			XXh
1393h			XXh
1394h			XXh
1395h			XXh
1396h	CAN0 Slot 3: Data Field		XXh
1397h			XXh
1398h			XXh
1399h			XXh
139Ah			XXh
139Bh			XXh
139Ch			XXh
139Dh			XXh
139Eh	CAN0 Slot 3: Time Stamp		XXh
139Fh			XXh
13A0h	CAN0 Slot 4: Identifier/DLC		XXh
13A1h			XXh
13A2h			XXh
13A3h			XXh
13A4h			XXh
13A5h			XXh
13A6h	CAN0 Slot 4: Data Field		XXh
13A7h			XXh
13A8h			XXh
13A9h			XXh
13AAh			XXh
13ABh			XXh
13ACh			XXh
13ADh			XXh
13AEh	CAN0 Slot 4: Time Stamp		XXh
13AFh			XXh
13B0h	CAN0 Slot 5: Identifier/DLC		XXh
13B1h			XXh
13B2h			XXh
13B3h			XXh
13B4h			XXh
13B5h			XXh
13B6h	CAN0 Slot 5: Data Field		XXh
13B7h			XXh
13B8h			XXh
13B9h			XXh
13BAh			XXh
13BBh			XXh
13BCh			XXh
13BDh			XXh
13BEh	CAN0 Slot 5: Time Stamp		XXh
13BFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)(1)

Address	Register	Symbol	After reset
13C0h	CAN0 Slot 6: Identifier/DLC		XXh
13C1h			XXh
13C2h			XXh
13C3h			XXh
13C4h			XXh
13C5h			XXh
13C6h	CAN0 Slot 6: Data Field		XXh
13C7h			XXh
13C8h			XXh
13C9h			XXh
13CAh			XXh
13CBh			XXh
13CCh			XXh
13CDh			XXh
13CEh	CAN0 Slot 6: Time Stamp		XXh
13CFh			XXh
13D0h	CAN0 Slot 7: Identifier/DLC		XXh
13D1h			XXh
13D2h			XXh
13D3h			XXh
13D4h			XXh
13D5h			XXh
13D6h	CAN0 Slot 7: Data Field		XXh
13D7h			XXh
13D8h			XXh
13D9h			XXh
13DAh			XXh
13DBh			XXh
13DCh			XXh
13DDh			XXh
13DEh	CAN0 Slot 7: Time Stamp		XXh
13DFh			XXh
13E0h	CAN0 Slot 8: Identifier/DLC		XXh
13E1h			XXh
13E2h			XXh
13E3h			XXh
13E4h			XXh
13E5h			XXh
13E6h	CAN0 Slot 8: Data Field		XXh
13E7h			XXh
13E8h			XXh
13E9h			XXh
13EAh			XXh
13EBh			XXh
13ECh			XXh
13EDh			XXh
13EEh	CAN0 Slot 8: Time Stamp		XXh
13EFh			XXh
13F0h	CAN0 Slot 9: Identifier/DLC		XXh
13F1h			XXh
13F2h			XXh
13F3h			XXh
13F4h			XXh
13F5h			XXh
13F6h	CAN0 Slot 9: Data Field		XXh
13F7h			XXh
13F8h			XXh
13F9h			XXh
13FAh			XXh
13FBh			XXh
13FCh			XXh
13FDh			XXh
13FEh	CAN0 Slot 9: Time Stamp		XXh
13FFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
1400h	CAN0 Slot 10: Identifier/DLC		XXh
1401h			XXh
1402h			XXh
1403h			XXh
1404h			XXh
1405h			XXh
1406h	CAN0 Slot 10: Data Field		XXh
1407h			XXh
1408h			XXh
1409h			XXh
140Ah			XXh
140Bh			XXh
140Ch			XXh
140Dh			XXh
140Eh	CAN0 Slot 10: Time Stamp		XXh
140Fh			XXh
1410h	CAN0 Slot 11: Identifier/DLC		XXh
1411h			XXh
1412h			XXh
1413h			XXh
1414h			XXh
1415h			XXh
1416h	CAN0 Slot 11: Data Field		XXh
1417h			XXh
1418h			XXh
1419h			XXh
141Ah			XXh
141Bh			XXh
141Ch			XXh
141Dh			XXh
141Eh	CAN0 Slot 11: Time Stamp		XXh
141Fh			XXh
1420h	CAN0 Slot 12: Identifier/DLC		XXh
1421h			XXh
1422h			XXh
1423h			XXh
1424h			XXh
1425h			XXh
1426h	CAN0 Slot 12: Data Field		XXh
1427h			XXh
1428h			XXh
1429h			XXh
142Ah			XXh
142Bh			XXh
142Ch			XXh
142Dh			XXh
142Eh	CAN0 Slot 12: Time Stamp		XXh
142Fh			XXh
1430h	CAN0 Slot 13: Identifier/DLC		XXh
1431h			XXh
1432h			XXh
1433h			XXh
1434h			XXh
1435h			XXh
1436h	CAN0 Slot 13: Data Field		XXh
1437h			XXh
1438h			XXh
1439h			XXh
143Ah			XXh
143Bh			XXh
143Ch			XXh
143Dh			XXh
143Eh	CAN0 Slot 13: Time Stamp		XXh
143Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.13 SFR Information (13)(1)

Address	Register	Symbol	After reset
1440h	CAN0 Slot 14: Identifier/DLC		XXh
1441h			XXh
1442h			XXh
1443h			XXh
1444h			XXh
1445h			XXh
1446h	CAN0 Slot 14: Data Field		XXh
1447h			XXh
1448h			XXh
1449h			XXh
144Ah			XXh
144Bh			XXh
144Ch			XXh
144Dh			XXh
144Eh	CAN0 Slot 14: Time Stamp		XXh
144Fh			XXh
1450h	CAN0 Slot 15: Identifier/DLC		XXh
1451h			XXh
1452h			XXh
1453h			XXh
1454h			XXh
1455h			XXh
1456h	CAN0 Slot 15: Data Field		XXh
1457h			XXh
1458h			XXh
1459h			XXh
145Ah			XXh
145Bh			XXh
145Ch			XXh
145Dh			XXh
145Eh	CAN0 Slot 15: Time Stamp		XXh
145Fh			XXh
1460h	CAN0 Global Mask Register	C0GMR	XXh
1461h			XXh
1462h			XXh
1463h			XXh
1464h			XXh
1465h			XXh
1466h	CAN0 Local Mask A Register	C0LMAR	XXh
1467h			XXh
1468h			XXh
1469h			XXh
146Ah			XXh
146Bh			XXh
146Ch	CAN0 Local Mask B Register	C0LMBR	XXh
146Dh			XXh
146Eh			XXh
146Fh			XXh
1470h			XXh
1471h			XXh
1472h			
1473h			
1474h			
1475h			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Resets

There are resets: hardware reset, power-on reset, voltage monitor 1 reset, voltage monitor 2 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset(1)	VCC rises
Voltage monitor 1 reset(1)	VCC falls (monitor voltage: Vdet1)
Voltage monitor 2 reset(1)	VCC falls (monitor voltage: Vdet2)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

NOTE:
1. Because this product is under development, specifications may be changed.

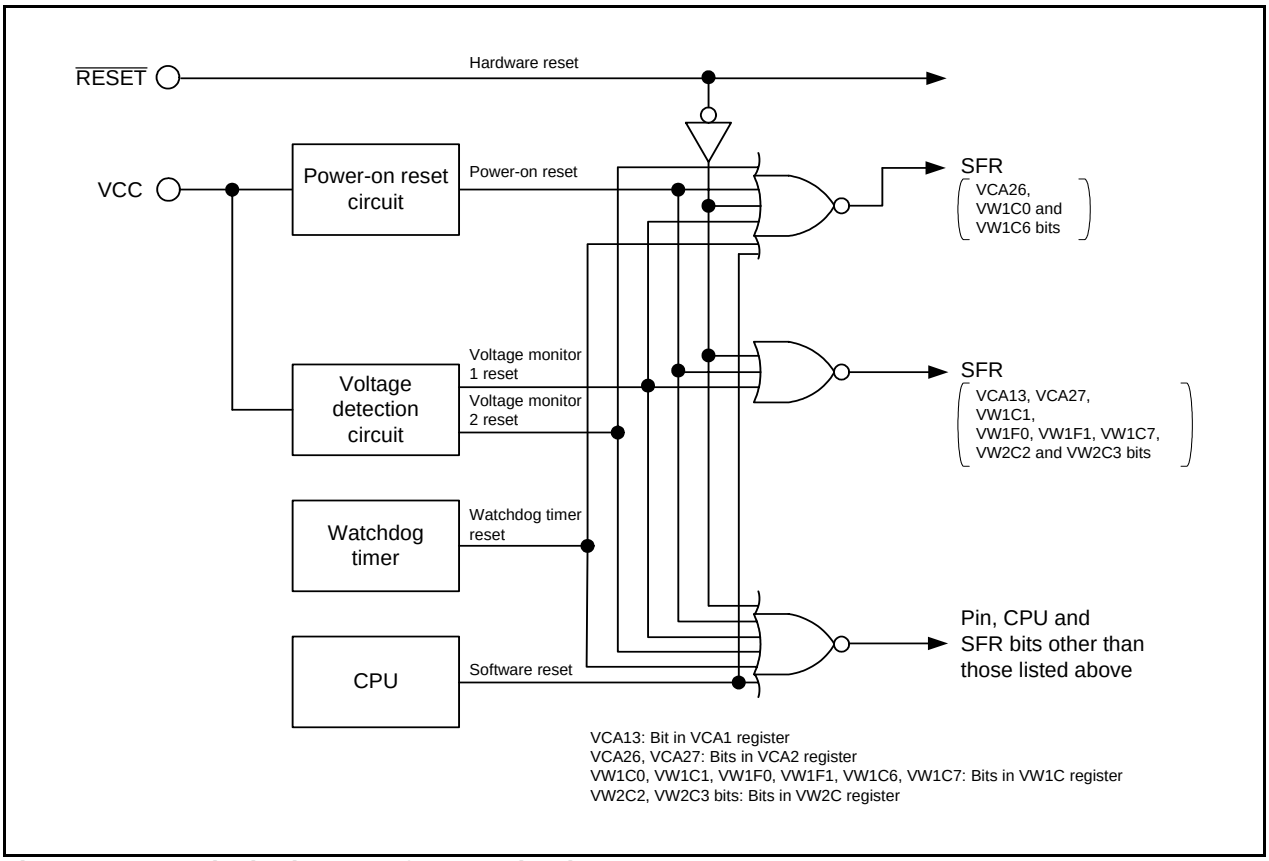


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 lists the Pin Functions after Reset, Figure 5.2 shows CPU Register Status after Reset, Figure 5.3 shows Reset Sequence, and Figure 5.4 shows the OFS Register.

Table 5.2 Pin Functions after Reset

Pin Name	Pin Functions
P0, P1, P2	Input port
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port
P4_2 to P4_7	Input port
P6	Input port

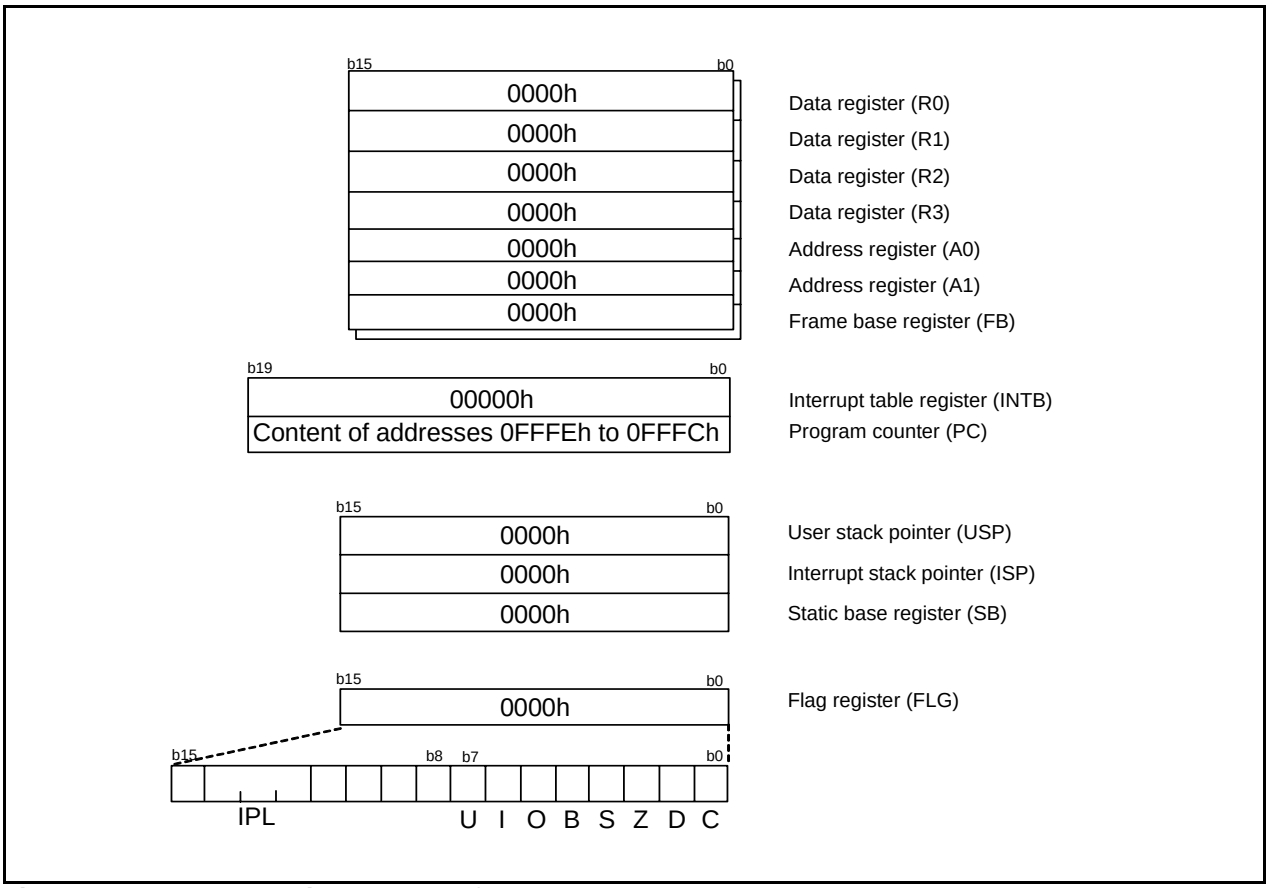
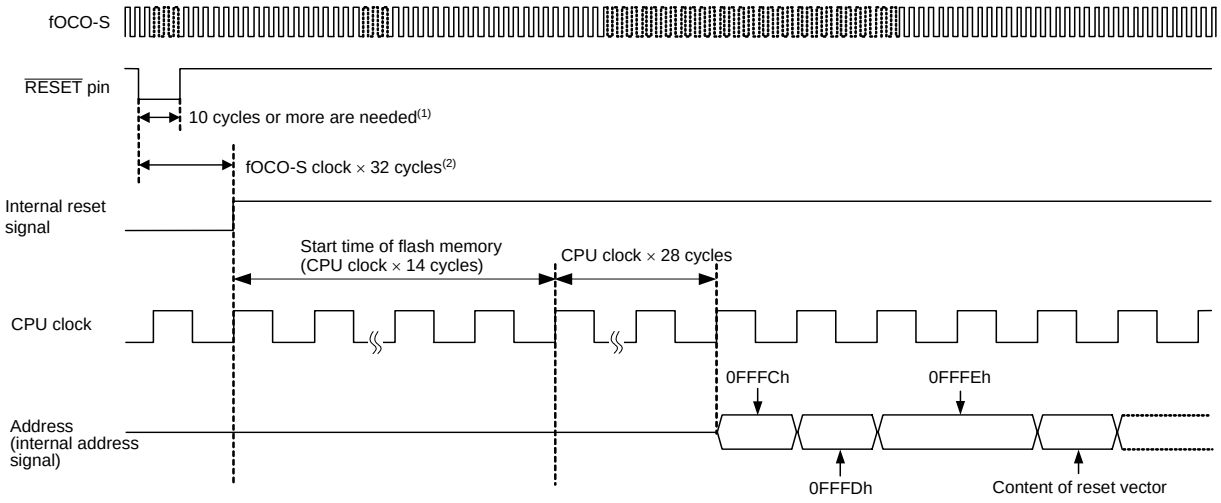


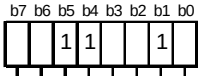
Figure 5.2 CPU Register Status after Reset



NOTES:
1. Hardware reset.
2. When the "L" input width to the RESET pin is set to fOCO-S clock × 32 cycles or more, setting the RESET pin to "H" also sets the internal reset signal to "H" at the same.

Figure 5.3 Reset Sequence

Option Function Select Register(1)



Symbol: OFS — Address: 0FFFFh — Before Shipment: FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b5-b4)	Reserved bits	Set to 1	RW
LVD1ON	Voltage detection circuit start bit(2)	0 : Voltage monitor 1 reset enabled after reset 1 : Voltage monitor 1 reset disabled after reset	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. To use the power-on reset, set the LVD1ON bit to 0 (voltage monitor 1 reset enabled after reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 5.4 OFS Register

5.1 Hardware Reset

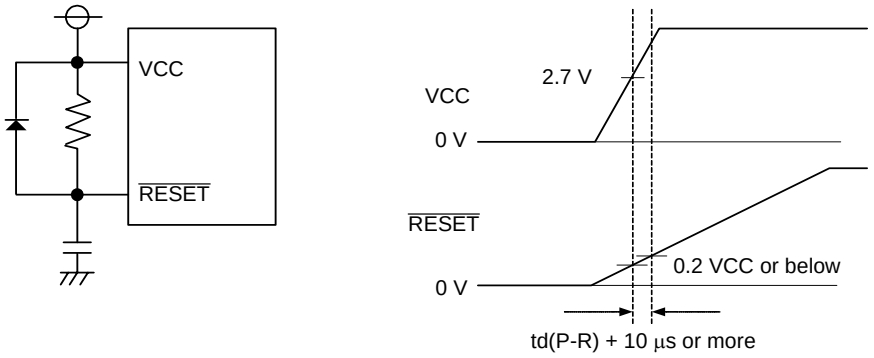
A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the power supply voltage meets the recommended performance condition, the pins, CPU, and SFR are reset (refer to **Table 5.2 Pin Functions after Reset**). When the input level applied to the $\overline{\text{RESET}}$ pin changes “L” to “H”, the program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divided-by-8 is automatically selected for the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after reset.
The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” during writing to the internal RAM, the internal RAM will be in indeterminate state.
Figure 5.5 shows the Example of Hardware Reset Circuit and Operation and Figure 5.6 shows the Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.1.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10µs or more.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

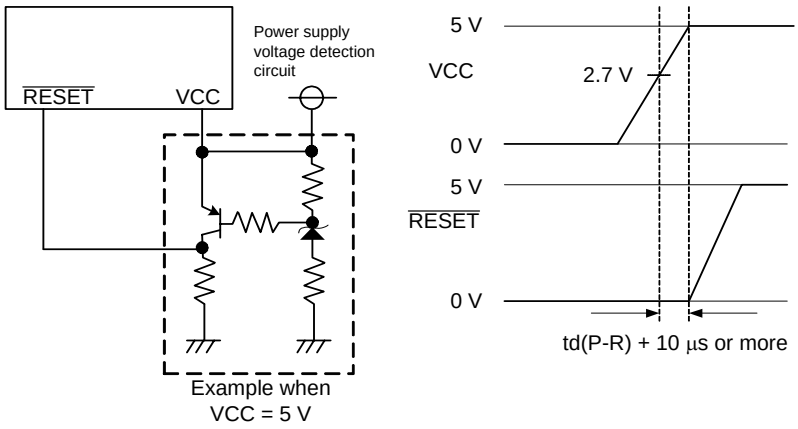
5.1.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the power supply voltage increase until it meets the recommended performance condition.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **21. Electrical Characteristics**).
(4) Wait for 10µs or more.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



NOTE:
1. Refer to **21. Electrical Characteristics.**

Figure 5.5 Example of Hardware Reset Circuit and Operation



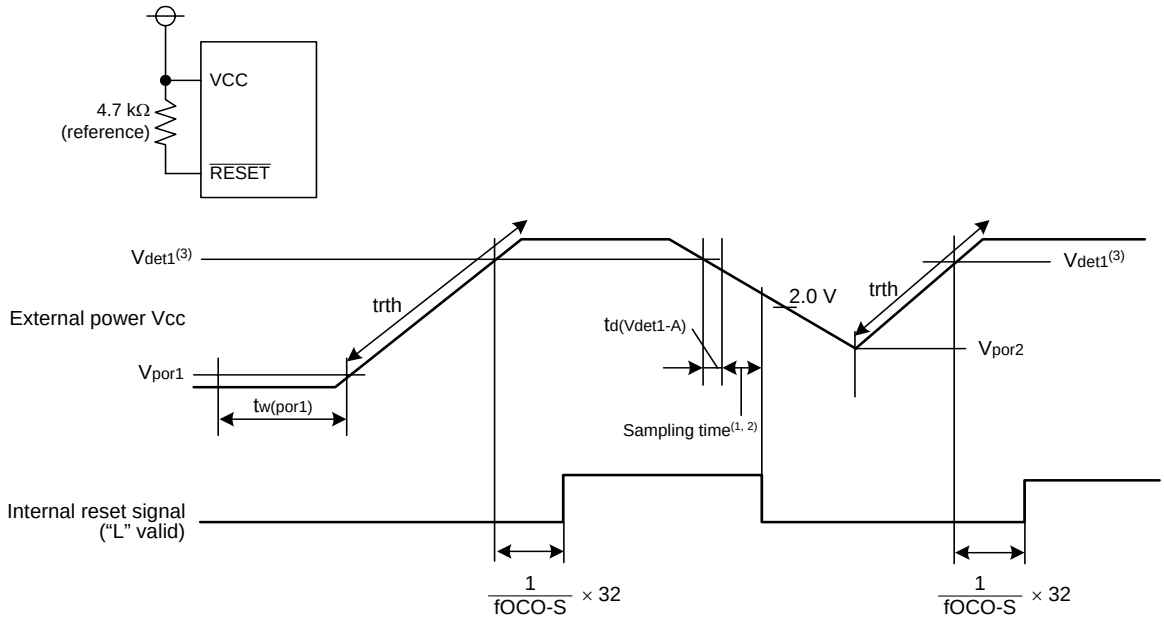
NOTE:
1. Refer to **21. Electrical Characteristics.**

Figure 5.6 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.2 Power-On Reset Function(1)

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFR. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8VCC or more.
When the input voltage to the VCC pin reaches to the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock divide-by-8 is automatically selected for the CPU after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after power-on reset.
The voltage monitor 0 reset is enabled after power-on reset.
Figure 5.7 shows the Example of Power-On Reset Circuit and Operation.

NOTE:
1. When using power-on reset function, set the LVD1ON bit to 0 (voltage monitor 1 reset enabled after reset).



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. Vdet1 indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** for details.
4. Refer to **21. Electrical Characteristics**.
5. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0 (voltage monitor 1 reset enabled after reset), bits VW1C0 and VW1C6 in the VW1C register to 1 (enable) and the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

Figure 5.7 Example of Power-On Reset Circuit and Operation

5.3 Voltage Monitor 1 Reset

A reset is applied using the on-chip voltage detection 1 circuit. The voltage detection 1 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet1.
When the input voltage to the VCC pin reaches to the Vdet1 level or below, the pins, CPU, and SFR are reset.
And when the input voltage to the VCC pin reaches to the Vdet1 level or above, count operation of the low-speed on-chip oscillator clock starts. When the operation counts the low-speed on-chip oscillator clock for 32 times, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock divide-by-8 is automatically selected for the CPU after reset.
The LVD1ON bit in the OFS register can select to enable or disable voltage monitor 1 reset after a reset.
To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, bits VW1C0 and VW1C6 in the VW1C register to 1, the VCA bit in the VCA2 register to 1.
The LVD1ON bit cannot be changed by a program. When setting the LVD1ON bit, write 0 (voltage monitor 1 reset enabled after reset) or 1 (voltage monitor 1 reset disabled after reset) to the bit 6 of address 0FFFFh using a flash programmer. Refer to **Figure 5.4 OFS Register** for details of the OFS register.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after voltage monitor 1 reset.
The internal RAM is not reset. When the input voltage to the VCC pin reaches to the Vdet1 level or below during writing to the internal RAM, the internal RAM is in indeterminate state.
Refer to **6. Voltage Detection Circuit** for details of voltage monitor 1 reset.

5.4 Voltage Monitor 2 Reset

A reset is applied using the on-chip voltage detection 2 circuit. The voltage detection 2 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet2.
When the input voltage to the VCC pin drops to the Vdet2 level or below, the pins, CPU, and SFR are reset and the program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divide-by-8 is automatically selected for the CPU clock.
The voltage monitor 2 does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset. When the input voltage to the VCC pin reaches to the Vdet2 level or below during writing to the internal RAM, the internal RAM is in indeterminate state.
Refer to **6. Voltage Detection Circuit** for details of voltage monitor 2 reset.

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFR if the watchdog timer underflows. Then the program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divide-by-8 is automatically selected for the CPU clock.
The watchdog timer reset does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset. When the watchdog timer underflows, the internal RAM is in indeterminate state.
Refer to **13. Watchdog Timer** for watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFR. The program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divide-by-8 is automatically selected for the CPU clock.
The software reset does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset.

6. Voltage Detection Circuit

The voltage detection circuit is a circuit to monitor the input voltage to the VCC pin. This circuit monitors the VCC input voltage by the program. And the voltage monitor 1 reset, voltage monitor 2 interrupt and voltage monitor 2 reset can be used.
Table 6.1 lists the Specifications of Voltage Detection Circuit and Figures 6.1 to 6.3 show the Block Diagrams. Figures 6.4 to 6.6 show the Associated Registers.

Table 6.1 Specifications of Voltage Detection Circuit

Item		Voltage Detection 1	Voltage Detection 2
VCC Monitor	Voltage to monitor	Vdet1	Vdet2
	Detection target	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Monitor	None	VCA13 bit in VCA1 register
			Whether VCC is higher or lower than Vdet2
Process When Voltage Is Detected	Reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset at Vdet1 > VCC; Restart CPU operation at VCC > Vdet1	Reset at Vdet2 > VCC Restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 2 interrupt
			Interrupt request at Vdet2 > VCC and VCC > Vdet2 when digital filter is enabled; Interrupt request at Vdet2 > VCC or VCC > Vdet2 when digital filter is disabled
Digital Filter	Switch enabled/disabled	Available	Available
	Sampling time	(Divide-by-n of fOCO-S) x 4 n: 1, 2, 4 and 8	(Divide-by-n of fOCO-S) x 4 n: 1, 2, 4 and 8

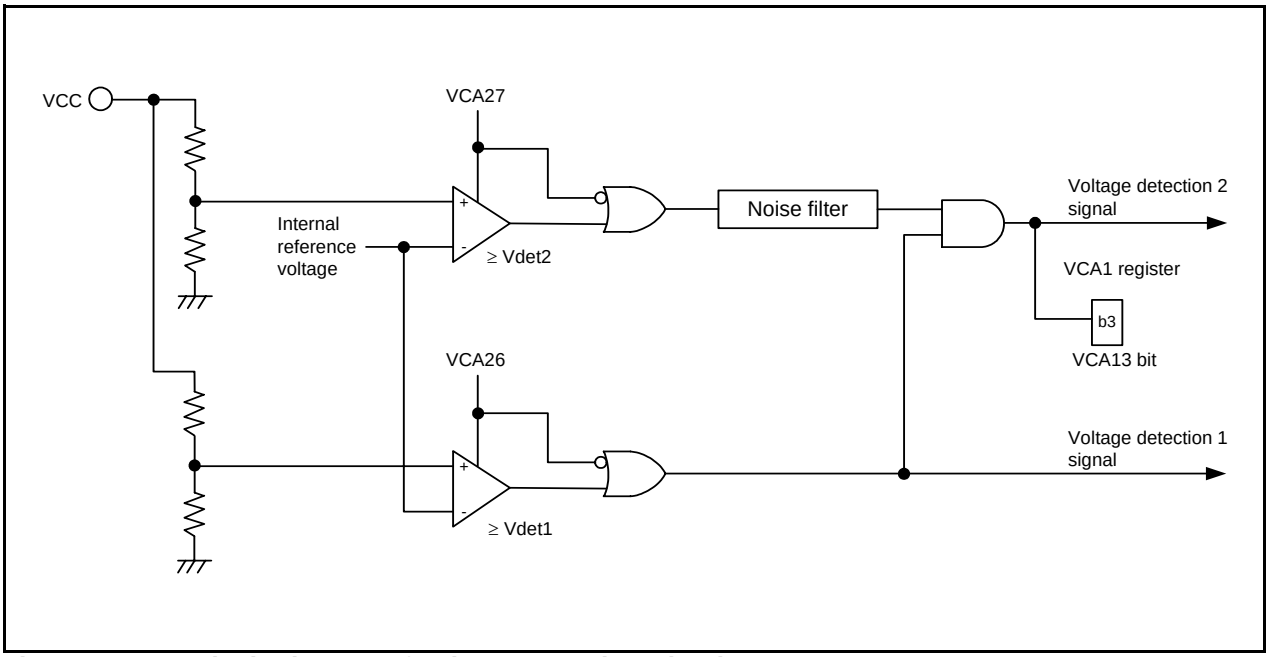


Figure 6.1 Block Diagram of Voltage Detection Circuit

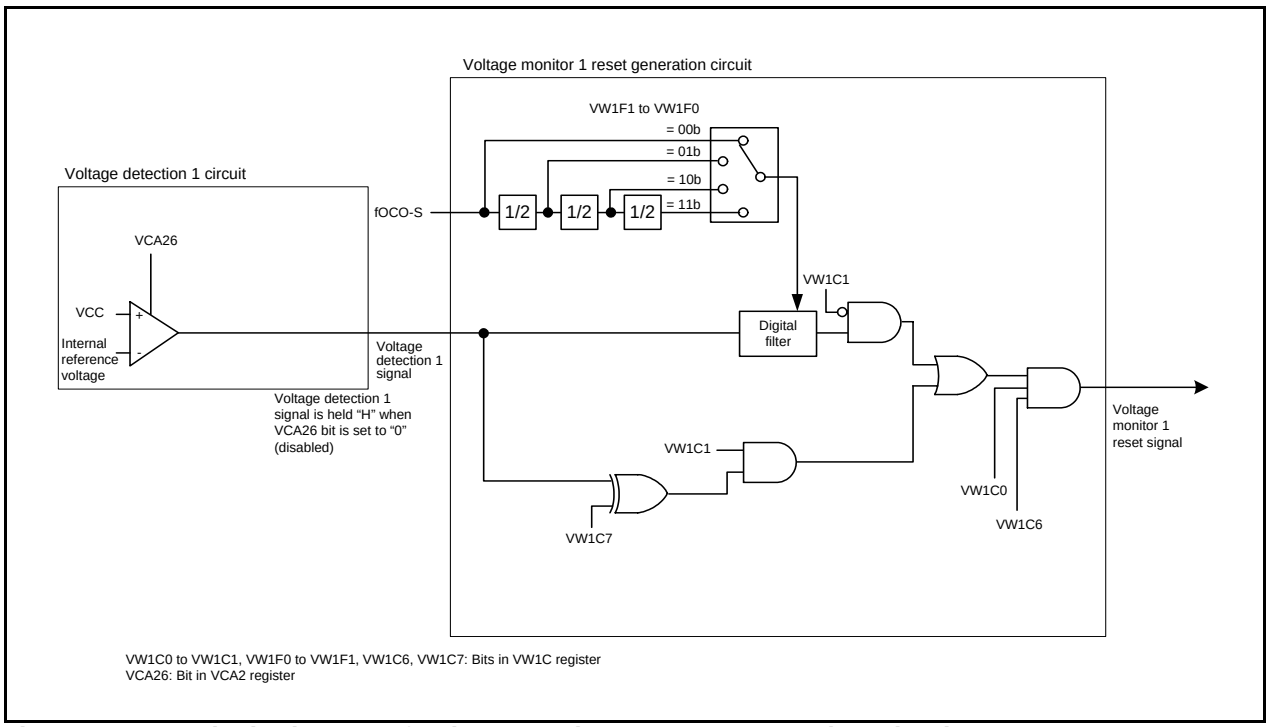


Figure 6.2 Block Diagram of Voltage Monitor 1 Reset Generation Circuit

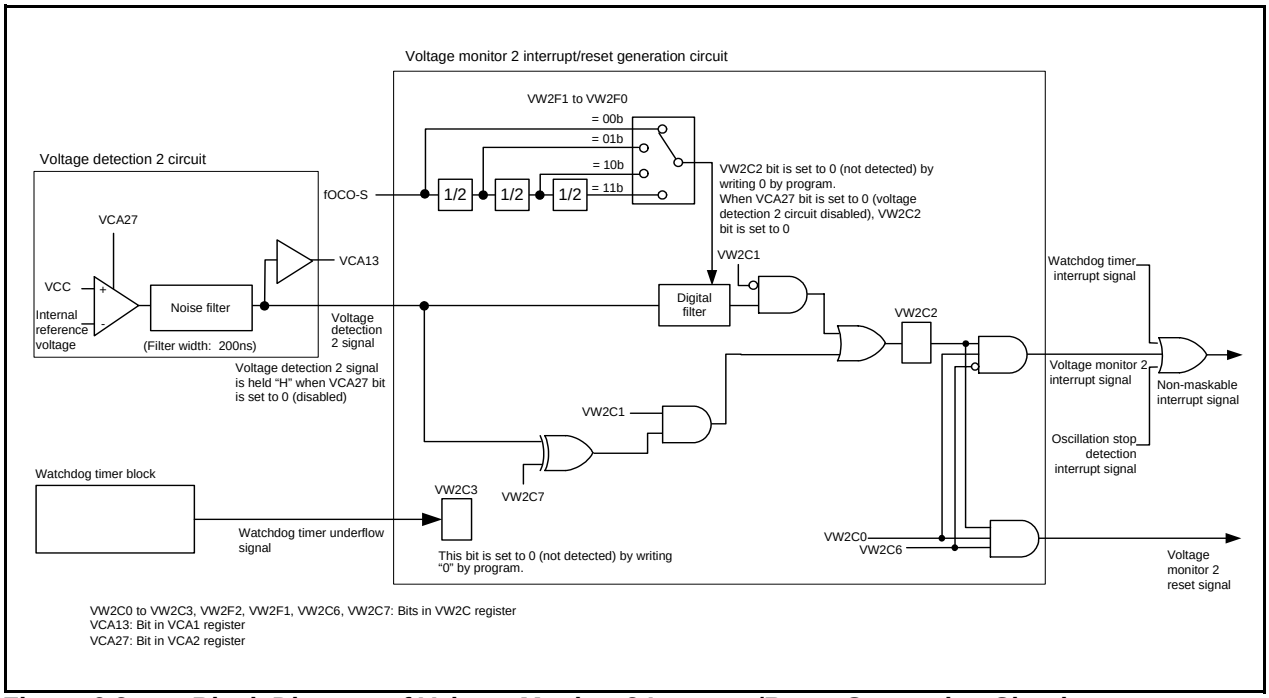
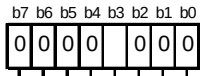


Figure 6.3 Block Diagram of Voltage Monitor 2 Interrupt/Reset Generation Circuit

Voltage Detection Register 1

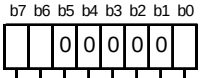


Symbol	Address	After Reset(2)
VCA1	0031h	00001000b

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0	RW
VCA13	Voltage detection 2 signal monitor flag(1)	0 : VCC < Vdet2 1 : VCC ≥ Vdet2 or voltage detection 2 circuit disabled	RO
— (b7-b4)	Reserved bits	Set to 0	RW

NOTES:
1. The VCA13 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). The VCA13 bit is set to 1 (VCC ≥ Vdet 2) when the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled).
2. The software reset, watchdog timer reset and voltage monitor 2 reset do not affect the VCA1 register.

Voltage Detection Register 2(1)



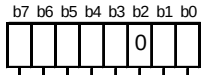
Symbol	Address	After Reset(4)
VCA2	0032h	The LVD1ON bit in the OFS register is set to 1: 00h Power-on reset, voltage monitor 1 reset or the LVD1ON bit in the OFS register is set to 0: 01000000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(5)	0 : Disables low consumption 1 : Enables low consumption	RW
— (b5-b1)	Reserved bits	Set to 0	RW
VCA26	Voltage detection 1 enable bit(2)	0 : Voltage detection 1 circuit disabled 1 : Voltage detection 1 circuit enabled	RW
VCA27	Voltage detection 2 enable bit(3)	0 : Voltage detection 2 circuit disabled 1 : Voltage detection 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (enables writing) before writing to the VCA2 register.
2. When using the voltage monitor 1 reset, set the VCA26 bit to 1.
   After the VCA26 bit is set from 0 to 1, the voltage detection circuit elapses for td(E-A) before starting operation.
3. When using the voltage monitor 2 interrupt/reset or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is from 0 to 1, the voltage detection circuit elapses for td(E-A) before starting operation.
4. The VCA27 bit remains unchanged after software reset, watchdog timer reset, and voltage monitor 2 reset.
5. Use the VCA20 bit only when entering to wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.11 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

Figure 6.4 Registers VCA1 and VCA2

Voltage Monitor 1 Circuit Control Register (1)



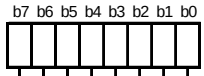
Symbol	Address	After Reset(2)
VW1C	0036h	The LVD1ON bit in the OFS register is set to 1: 0000X000b Power-on reset, voltage monitor 1 reset or the LVD1ON bit in the OFS register is set to 0: 0100X001b

Bit Symbol	Bit Name	Function	RW
VW1C0	Voltage monitor 1 reset enable bit(3)	0 : Disable 1 : Enable	RW
VW1C1	Voltage monitor 1 digital filter disable mode select bit	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW1C2	Reserved bit	Set to 0	RW
— (b3)	Reserved bit	When read, the content is undefined.	RO
VW1F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divide-by-1 0 1 : fOCO-S divide-by-2 1 0 : fOCO-S divide-by-4 1 1 : fOCO-S divide-by-8	RW
VW1F1			RW
VW1C6	Voltage monitor 1 circuit mode select bit	When the VW1C0 bit is set to 1 (enables voltage monitor 1 reset), set to 1.	RW
VW1C7	Voltage monitor 1 reset generation condition select bit(4)	When the VW1C1 bit is set to 1 (digital filter disabled mode), set to 1.	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enable) before writing to the VW1C register.
2. The value other than the VW1CO and VW1C6 bits remains unchanged after software reset, watchdog timer reset, and voltage monitor 2 reset.
3. The VW1C0 bit is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disable), when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled).
4. The VW1C7 bit is enabled when the VW1C1 bit is set to 1 (digital filter disabled mode).

Figure 6.5 VW1C Register

Voltage Monitor 2 Circuit Control Register (1)



Symbol	Address	After Reset(8)
VW2C	0037h	00h

Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/reset enable bit(6)	0 : Disable 1 : Enable	RW
VW2C1	Voltage monitor 2 digital filter disabled mode select bit(2)	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW2C2	Voltage change detection flag(3,4,8)	0 : Not detected 1 : Vdet2 pass detected	RW
VW2C3	WDT detection flag(4,8)	0 : Not detected 1 : Detected	RW
VW2F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divide-by-1 0 1 : fOCO-S divide-by-2 1 0 : fOCO-S divide-by-4 1 1 : fOCO-S divide-by-8	RW
VW2F1			RW
VW2C6	Voltage monitor 2 circuit mode select bit(5)	0 : Voltage monitor 2 interrupt mode 1 : Voltage monitor 2 reset mode	RW
VW2C7	Voltage monitor 2 interrupt/reset generation condition select bit(7,9)	0 : When VCC reaches Vdet2 or above 1 : When VCC reaches Vdet2 or below	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (enables writing) before writing to the VW2C register. When writing the VW2C register, the VW2C2 bit may be set to 1. Set the VW2C2 bit to 0 after writing the VW2C register.
2. When the voltage monitor 2 interrupt is used to exit stop mode and to return again, write 0 to the VW2C1 bit before writing 1.
3. This bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When writing 0 by a program, it is set to 0 (it remains unchanged even if it is set to 1).
5. This bit is enabled when the VW2C0 bit is set to 1 (voltage monitor 2 interrupt/enables reset).
6. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disable) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled).
7. The VW2C7 bit is enabled when the VW2C1 bit is set to 1 (digital filter disabled mode).
8. The VW2C2 and VW2C3 bits remain unchanged in the software reset, watchdog timer reset and voltage monitor 2 reset.
9. When the VW2C6 bit is set to 1 (voltage monitor 2 reset mode), set the VW2C7 bit to 1 (when VCC reaches to Vdet2 or below) (do not set to 0).

Figure 6.6 VW2C Register

6.1 VCC Input Voltage

6.1.1 Monitoring Vdet1

Vdet1 cannot be monitored.

6.1.2 Monitoring Vdet2

Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled). After td(E-A) has elapsed (refer to **21. Electrical Characteristics**), Vdet2 can be monitored by the VCA13 bit in the VCA1 register.

6.2 Voltage Monitor 1 Reset

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Reset and Figure 6.7 shows an Example of Voltage Monitor 1 Reset Operation. To use the voltage monitor 1 reset to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Reset

Step	When Using Digital Filter	When Not Using Digital Filter
1	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled)	
2	Wait for td(E-A)	
3	Select the sampling clock of the digital filter by the VW1F0 to VW1F1 bits in the VW1C register	Set the VW1C7 bit in the VW1C register to 1
4(1)	Set the VW1C1 bit in the VW1C register to “0” (digital filter enabled)	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled)
5(1)	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode)	
6	Set the VW1C2 bit in the VW1C register to 0	
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
8	Wait for the sampling clock of the digital filter x 4 cycles	– (no wait time)
9	Set the VW1C0 bit in the VW1C register to 1 (enables voltage monitor 1 reset)	

NOTE:
1. When the VW1C0 bit is set to 0, procedures 3, 4 and 5 can be executed simultaneously (with 1 instruction).

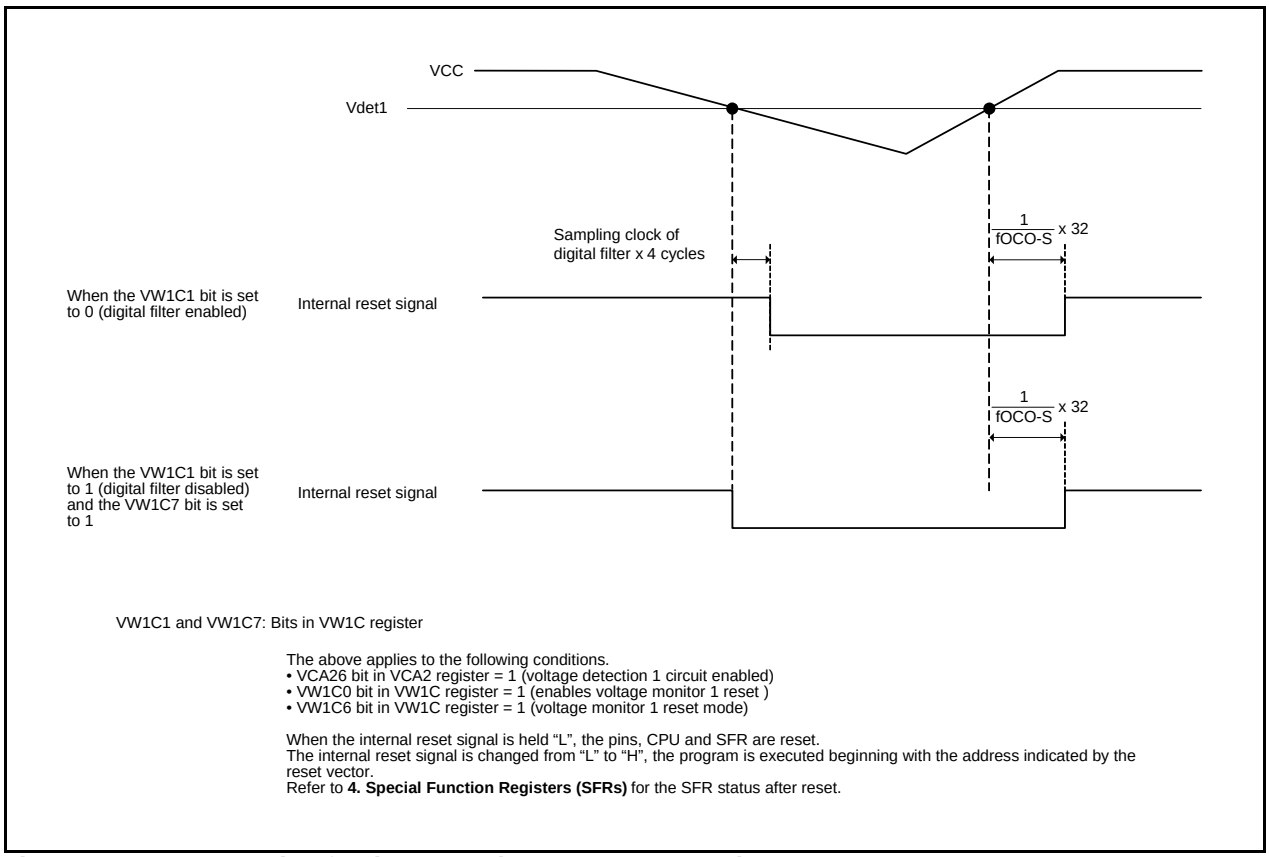


Figure 6.7 Example of Voltage Monitor 1 Reset Operation

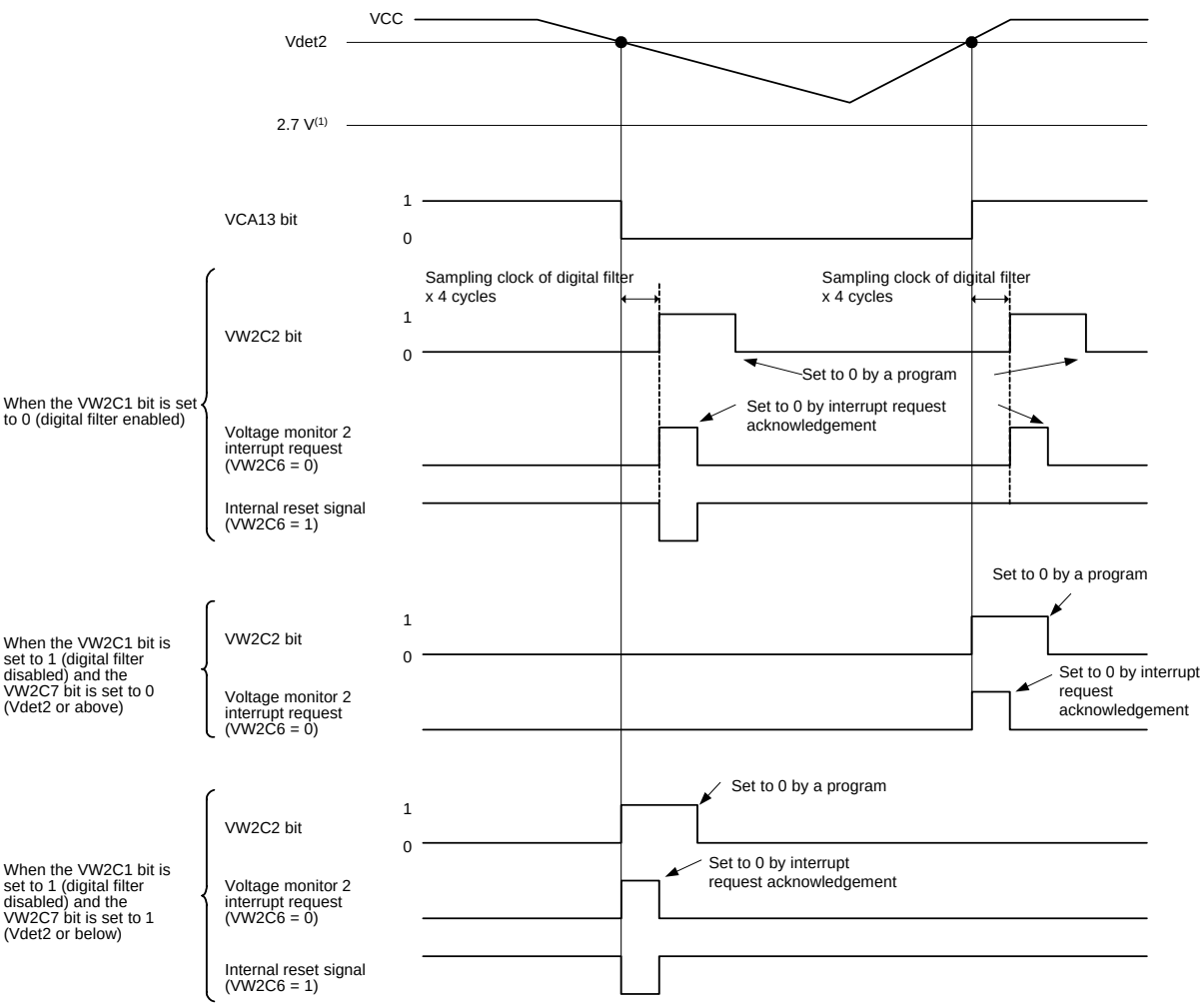
6.3 Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset. Figure 6.8 shows an Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Operation. To use the voltage monitor 2 interrupt or voltage monitor 2 reset to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset

Step	When Using Digital Filter		When Not Using Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled)			
2	Wait for td(E-A)			
3	Select the sampling clock of the digital filter by the VW2F0 to VW2F1 bits in the VW2C register		Select the timing of the interrupt and reset request by the VW2C7 bit in the VW2C register(1)	
4(2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled)		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled)	
5(2)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode)	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode)	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode)
6	Set the VW2C2 bit in the VW2C register to 0 (passing of Vdet2 is not detected)			
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)		–	
8	Wait for the sampling clock of the digital filter x 4 cycles		– (no wait time)	
9	Set the VW2C0 bit in the VW2C register to 1 (enables voltage monitor 2 interrupt/reset)			

NOTES:
1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is set to 0, steps 3, 4, and 5 can be executed simultaneously (with 1 instruction).



VCA13 : Bit in VCA1 register
VW2C1, VW2C2, VW2C6, VW2C7 : Bit in VW2C register

The above applies to the following conditions.
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (enables voltage monitor 2 interrupt and voltage monitor 2 reset)

NOTE:
1. When the voltage monitor 1 reset is not used, set the power supply to VCC ≥ 2.7.

Figure 6.8 Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Operation

7. Programmable I/O Ports

There are 41 programmable Input/Output ports (I/O ports) P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, and P6. Also, P4_6 and P4_7 can be used as input-only ports if the XIN clock oscillation circuit is not used, and the P4_2 can be used as an input-only port if the A/D converter is not used.

Table 7.1 Overview of Programmable I/O Ports

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister
P0 to P2, P6	I/O	CMOS3 state	Set every bit	Set every 4 bits(1)
P3_0, P3_1, P3_3 to P3_5, P3_7	I/O	CMOS3 state	Set every bit	Set every 3 bits(1)
P4_3	I/O	CMOS3 state	Set every bit	Set every bit(1)
P4_4, P4_5	I/O	CMOS3 state	Set every bit	Set every 2 bits(1)
P4_2(2) P4_6, P4_7(3)	I	(No output function)	None	None

NOTES:
1. In input mode, whether the internal pull-up resistor is connected or not can be selected by the PUR0 and PUR1 registers.
2. When the A/D converter is not used, these ports can be used as the input port only.
3. When the XIN clock oscillation circuit is not used, these ports can be used as the input port only.

7.1 Functions of Programmable I/O Ports

The PDi_j (i = 0 to 4, 6, j = 0 to 7) bit in the PDi register controls I/O of the ports P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, and P6. The Pi register consists of a port latch to hold output data and a circuit to read pin state.

Figures 7.1 to 7.7 show the Configurations of Programmable I/O Ports. Table 7.2 lists the Functions of Programmable I/O Ports. Also, Figure 7.9 shows the PDi (i = 0 to 4 and 6) Registers. Figure 7.10 shows the Pi (i = 0 to 4 and 6) Registers, Figure 7.11 shows the Registers PUR0 and PUR1 and Figure 7.12 shows the PMR Register.

Table 7.2 Functions of Programmable I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register(1)	
	When PDi_j bit is set to 0 (input mode)	When PDi_j bit is set to 1 (output mode)
Reading	Read pin input level	Read the port latch
Writing	Write to the port latch	Write to the port latch. The value written in the port latch, it is output from the pin.

i = 0 to 4, 6, j = 0 to 7

NOTE:
1. Nothing is assigned to bits PD3_2, PD3_6, PD4_0 to PD4_2, PD4_6, and PD4_7.

7.2 Effect on Peripheral Functions

Programmable I/O ports function as I/O of peripheral functions (refer to **Table 1.6 Pin Name Information by Pin Number**).

Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 4, 6 j = 0 to 7). Refer to descriptions of each function for how to set peripheral functions.

Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 4, 6 j = 0 to 7)

I/O of Peripheral Functions	PDi_j Bit Setting of Port shared with Pin
Input	Set this bit to 0 (input mode).
Output	This bit can be set to both 0 or 1 (output regardless of the port setting)

7.3 Pins Other than Programmable I/O Ports

Figure 7.8 shows the Configuration of I/O Pins.

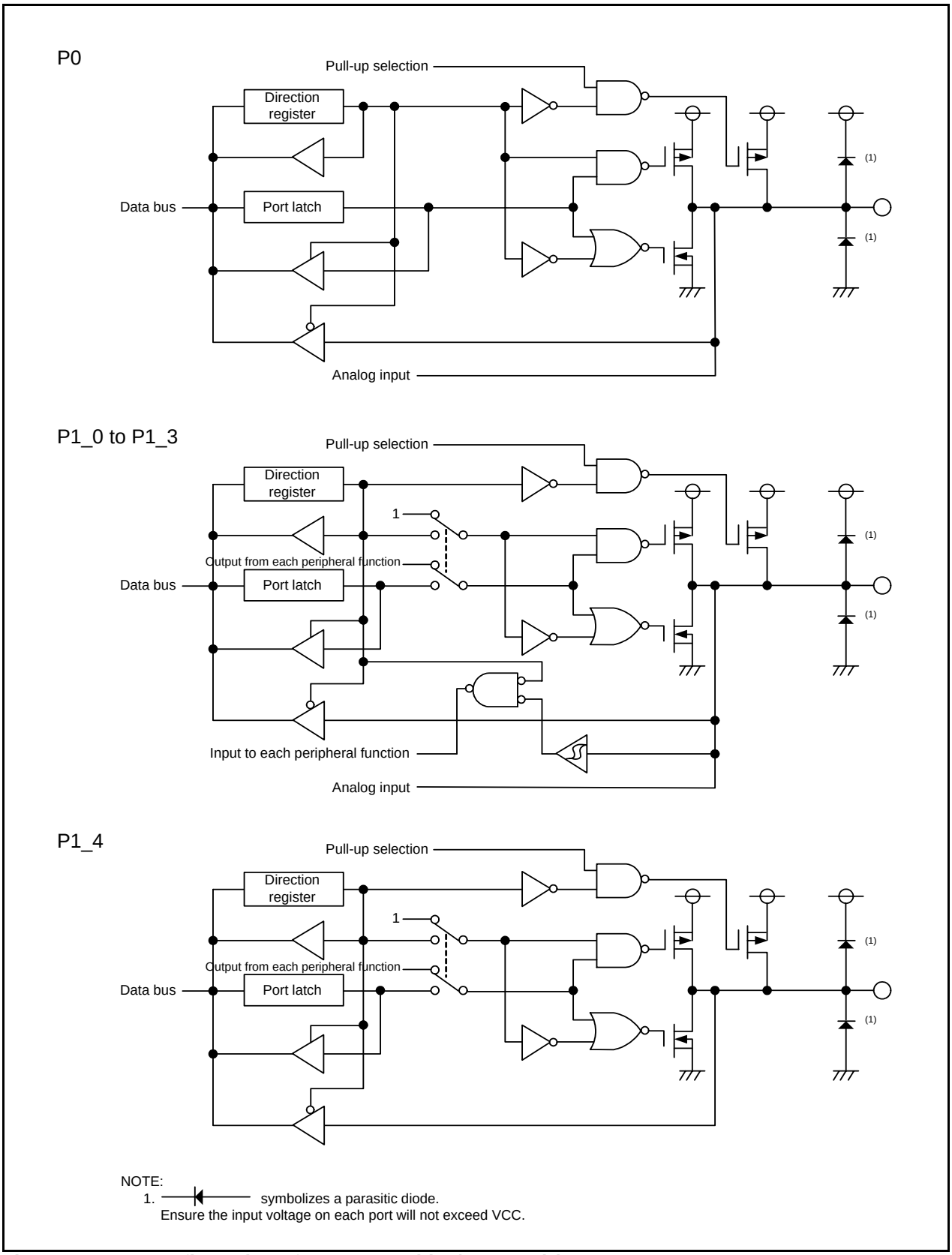


Figure 7.1 Configuration of Programmable I/O Ports (1)

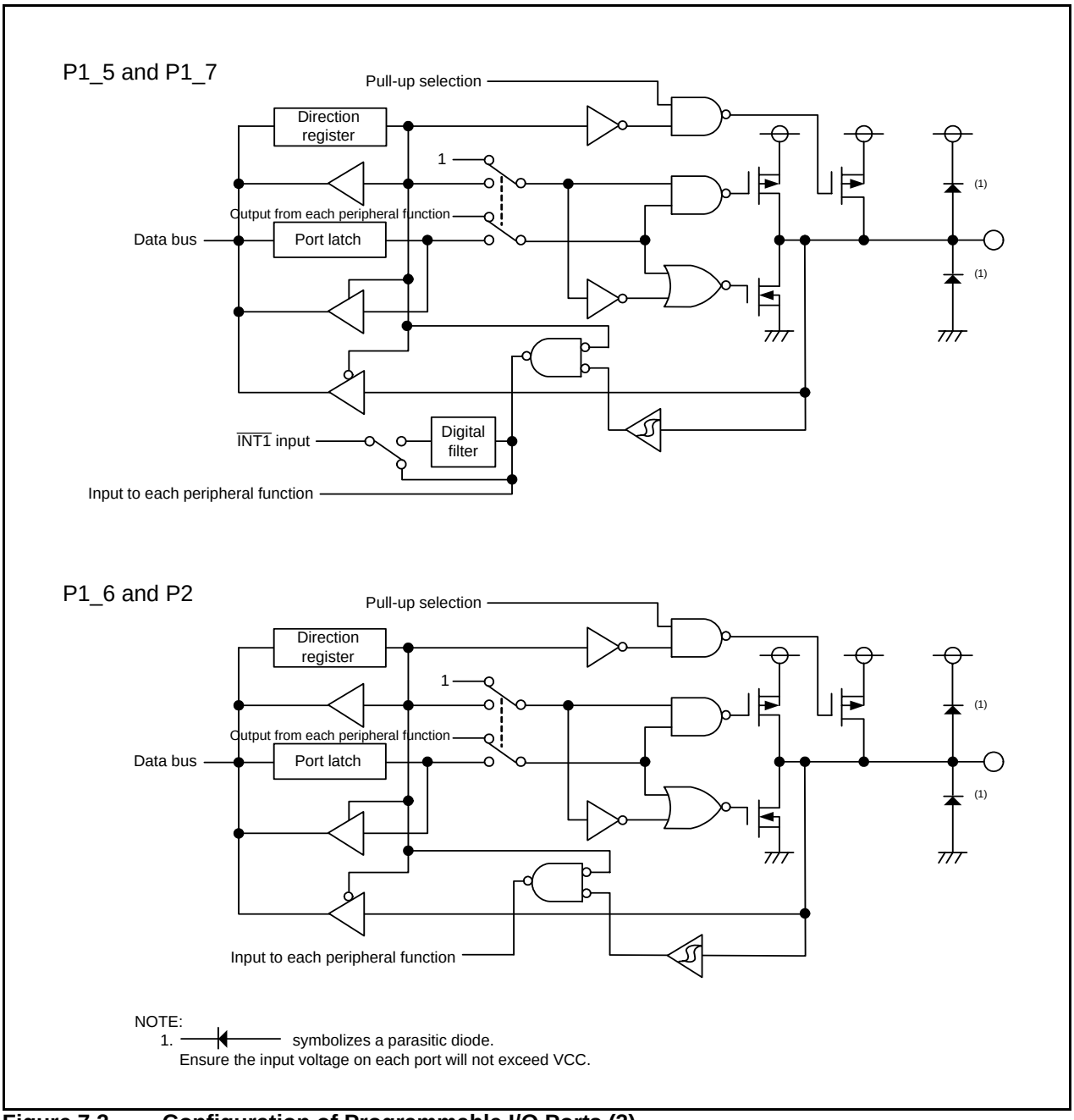


Figure 7.2 Configuration of Programmable I/O Ports (2)

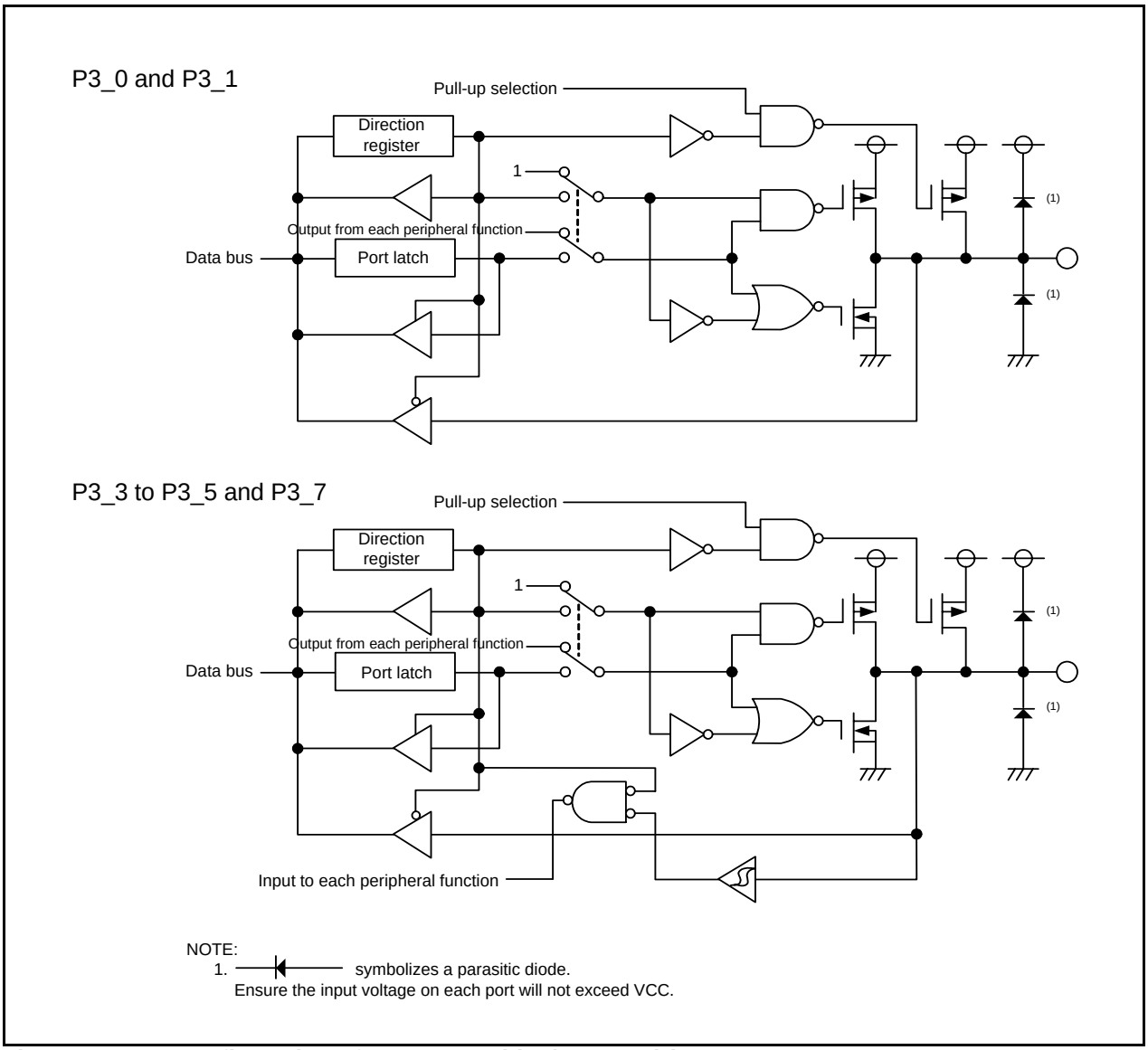


Figure 7.3 Configuration of Programmable I/O Ports (3)

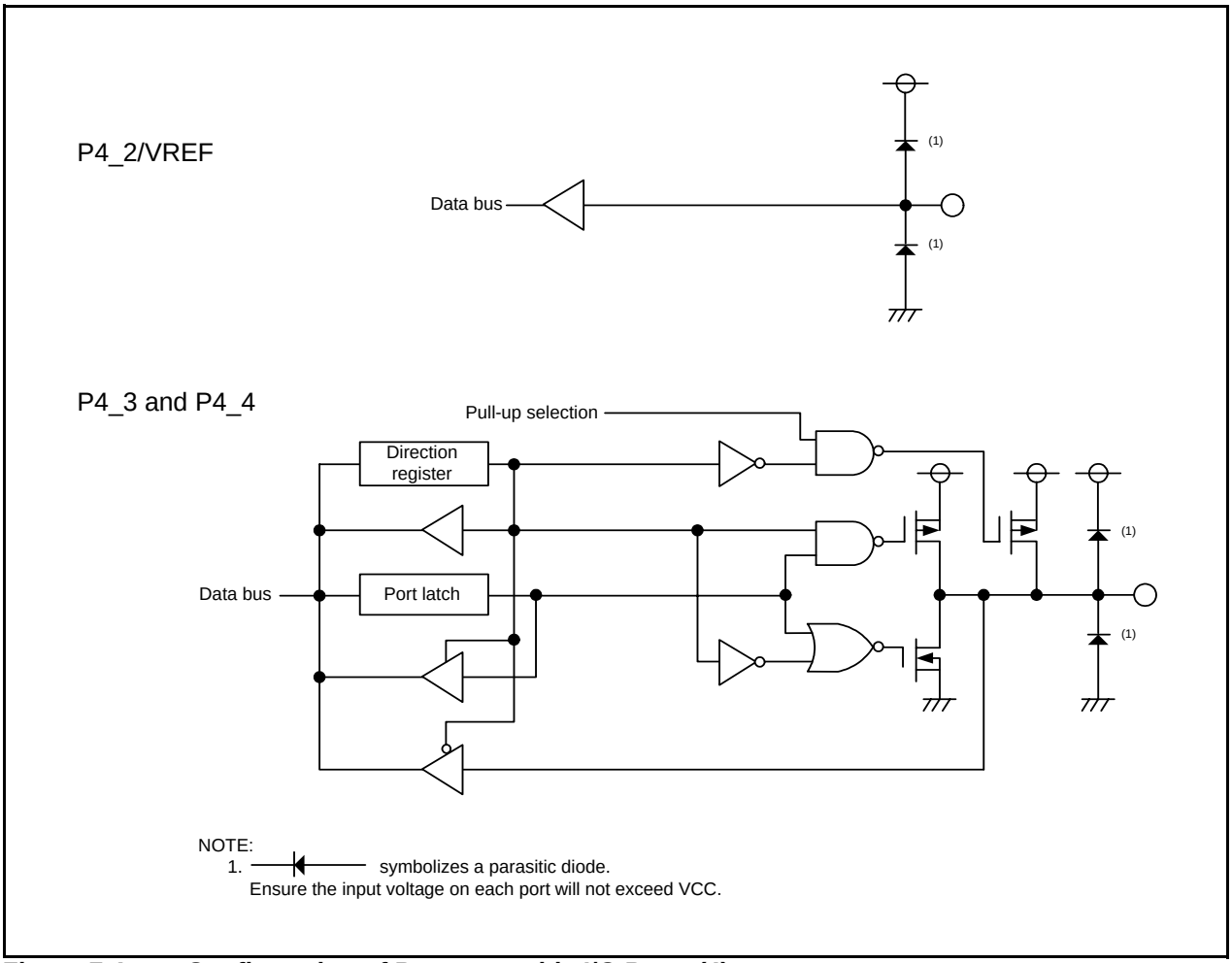
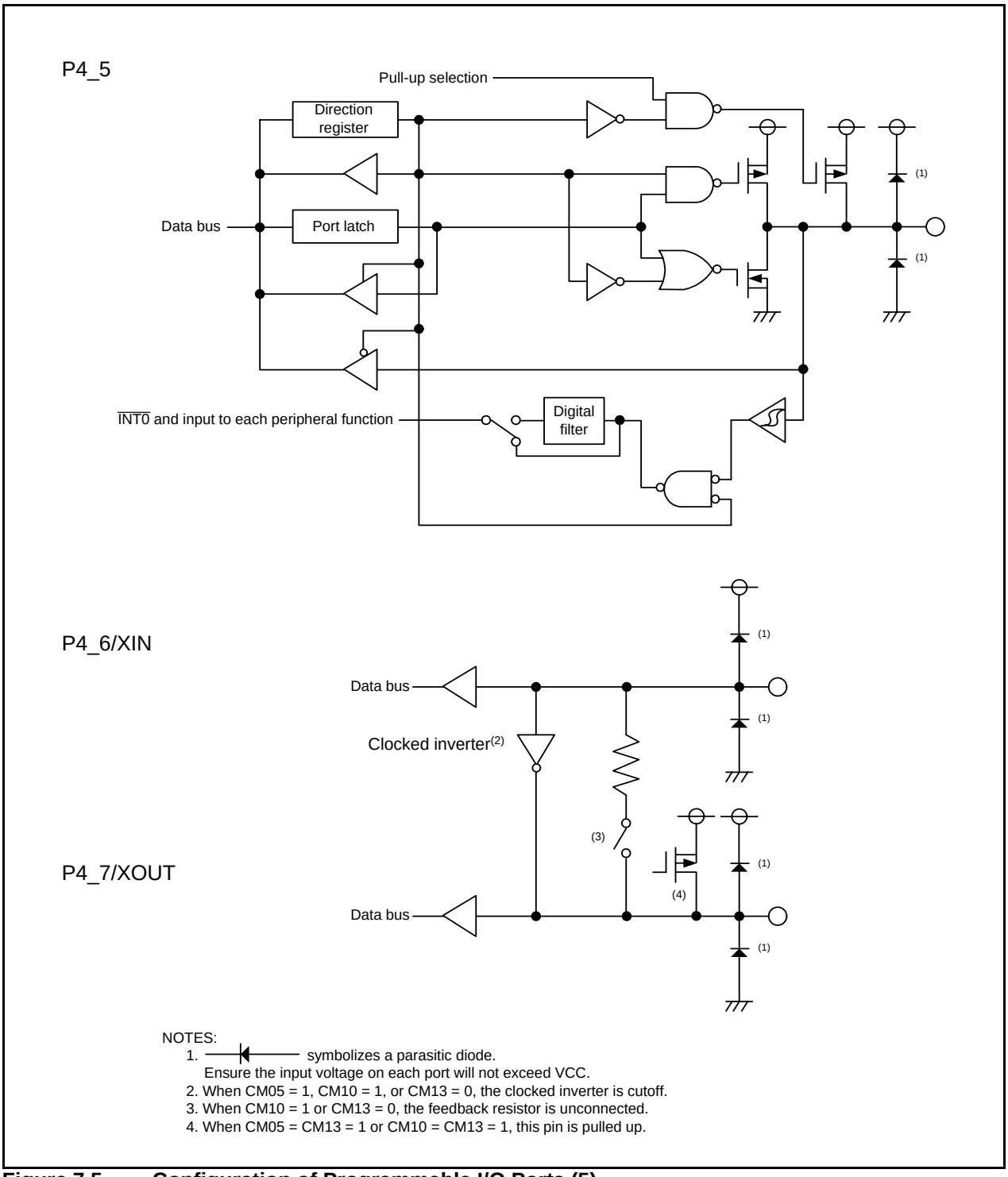


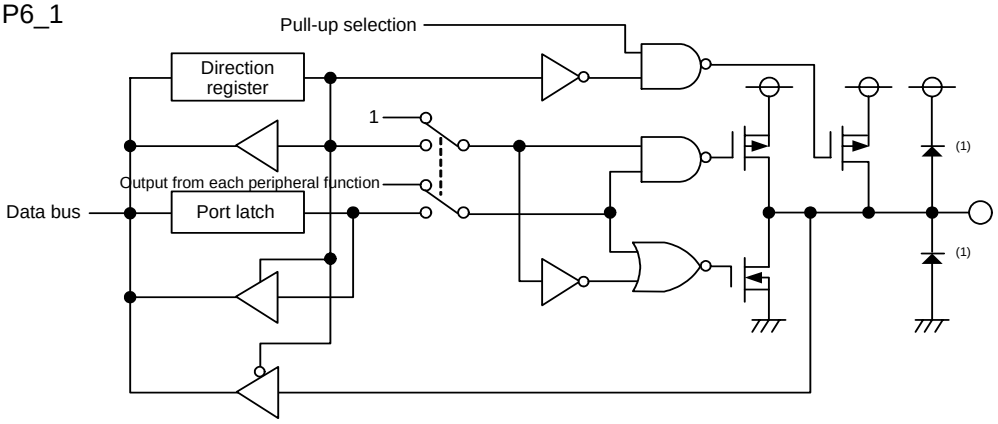
Figure 7.4 Configuration of Programmable I/O Ports (4)



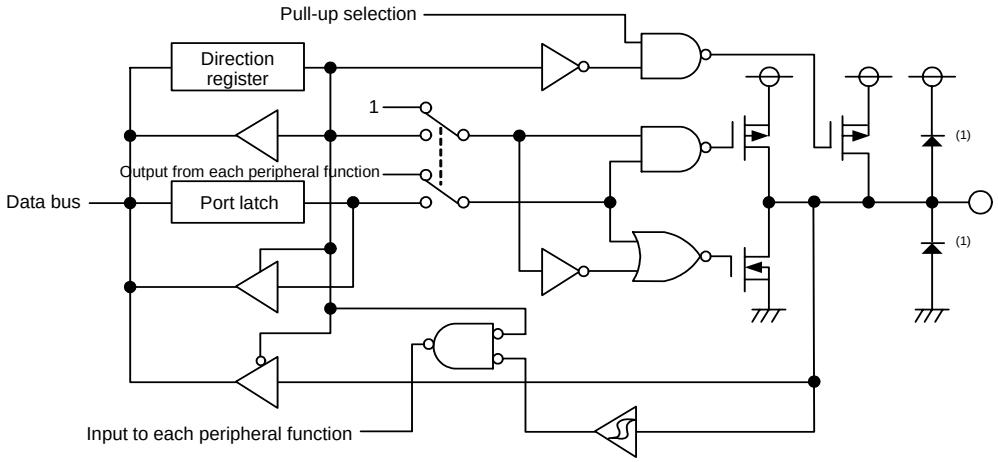
NOTES:
1. ⟵ symbolizes a parasitic diode.
   Ensure the input voltage on each port will not exceed VCC.
2. When CM05 = 1, CM10 = 1, or CM13 = 0, the clocked inverter is cutoff.
3. When CM10 = 1 or CM13 = 0, the feedback resistor is unconnected.
4. When CM05 = CM13 = 1 or CM10 = CM13 = 1, this pin is pulled up.

Figure 7.5 Configuration of Programmable I/O Ports (5)

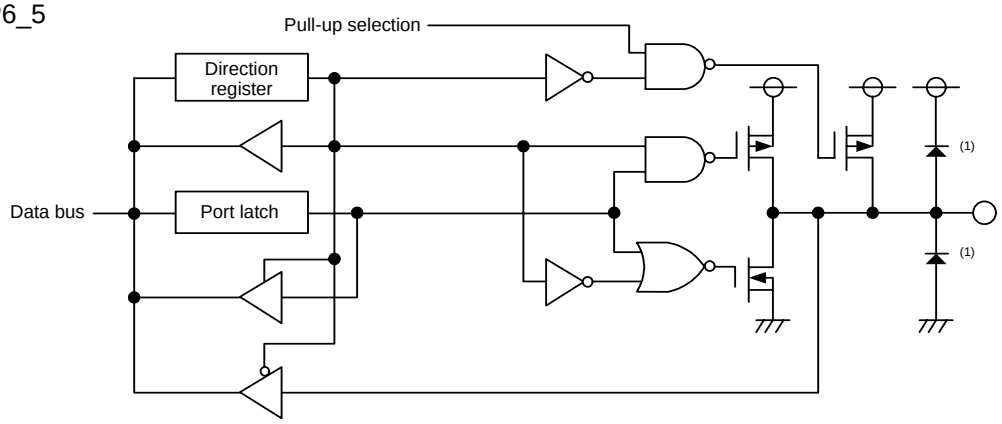
P6_0 and P6_1



P6_2



P6_3 to P6_5



NOTE:
1. symbolizes a parasitic diode.
Ensure the input voltage on each port will not exceed VCC.

Figure 7.6 Configuration of Programmable I/O Ports (6)

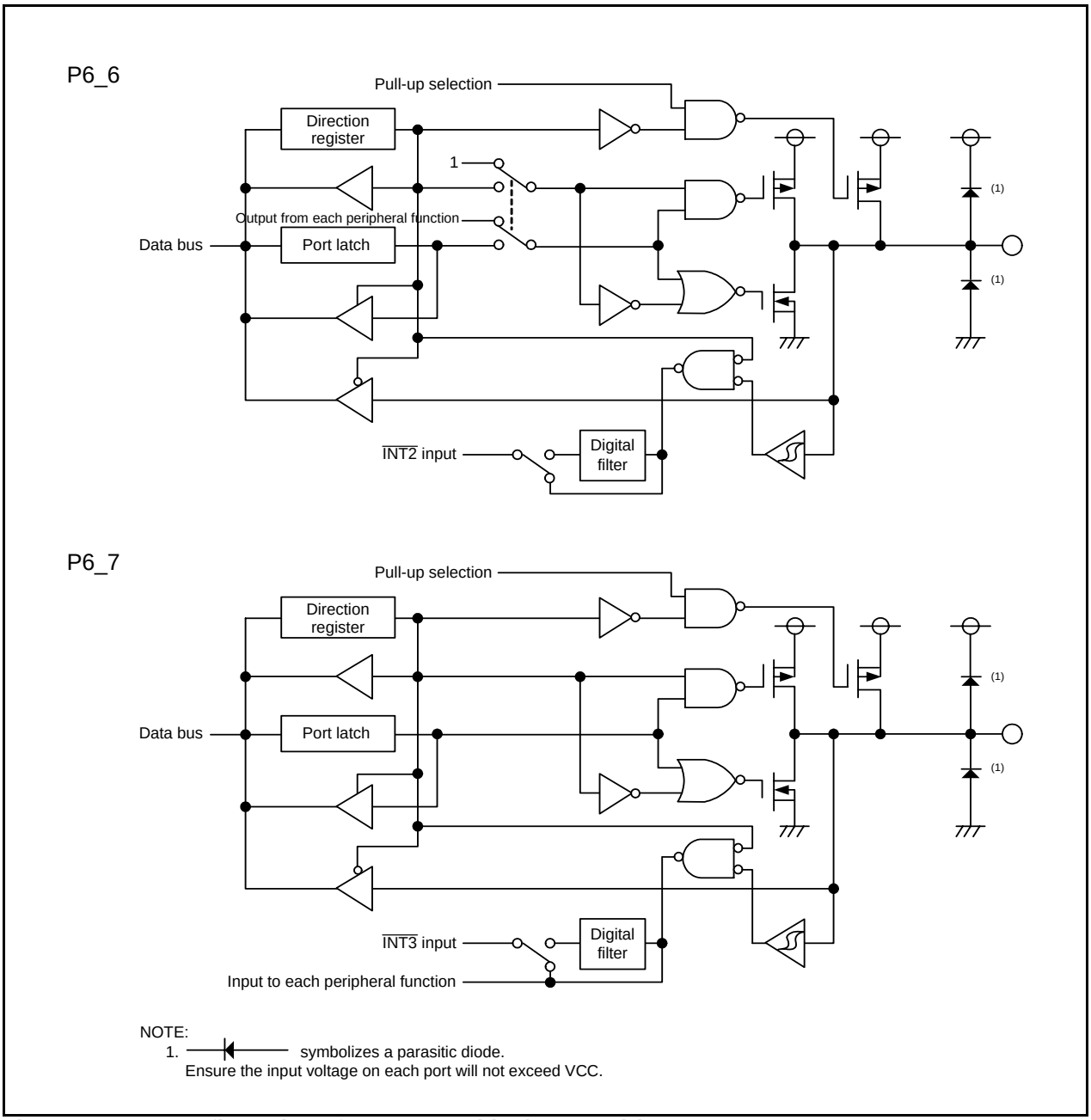


Figure 7.7 Configuration of Programmable I/O Ports (7)

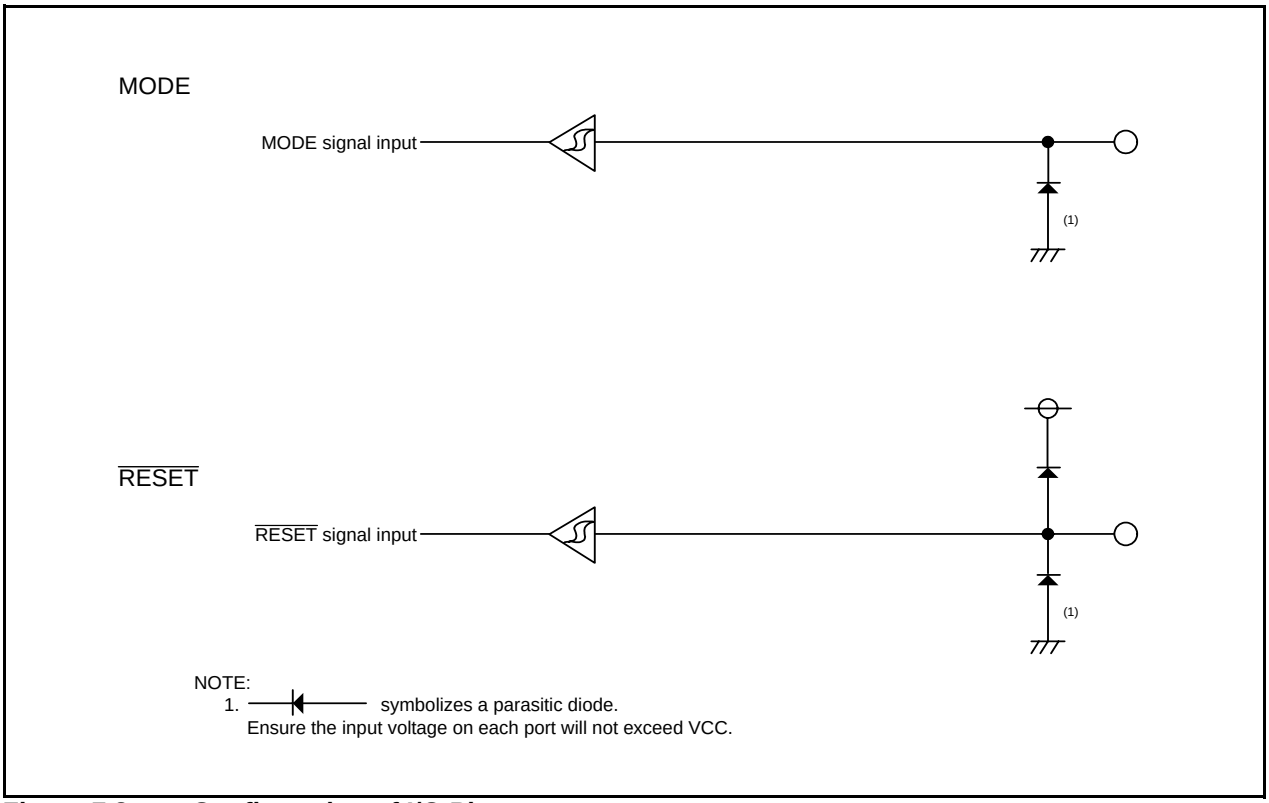


Figure 7.8 Configuration of I/O Pins

Port Pi Direction Register (i = 0 to 4, 6)(1,2)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
PD0(3)	00E2h	00h
PD1	00E3h	00h
PD2	00E6h	00h
PD3	00E7h	00h
PD4	00EAh	00h
PD6	00EEh	00h

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi_0 direction bit	0 : Input mode (functions as an input port) 1 : Output mode (functions as an output port)	RW
PDi_1	Port Pi_1 direction bit		RW
PDi_2	Port Pi_2 direction bit		RW
PDi_3	Port Pi_3 direction bit		RW
PDi_4	Port Pi_4 direction bit		RW
PDi_5	Port Pi_5 direction bit		RW
PDi_6	Port Pi_6 direction bit		RW
PDi_7	Port Pi_7 direction bit		RW

NOTES:
1. Nothing is assigned to the PD3_2 and PD3_6 bits in the PD3 register. When writing to the PD3_2 and PD3_6 bits , write 0 (input mode). When read, its content is 0.
2. Nothing is assigned to the PD4_0 to PD4_2, PD4_6 and PD4_7 bits in the PD4 register. When writing to the PD4_0 to PD4_2, PD4_6 and PD4_7 bits in the PD4 register, write 0 (input mode). When read, its content is 0.
3. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).

Figure 7.9 PDi (i = 0 to 4 and 6) Registers

Port Pi Register (i = 0 to 4, 6)(1,2)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
P0	00E0h	Indeterminate
P1	00E1h	Indeterminate
P2	00E4h	Indeterminate
P3	00E5h	Indeterminate
P4	00E8h	Indeterminate
P6	00ECh	Indeterminate

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi_0 bit	The pin level on any I/O port which is set for input mode can be read by reading the corresponding bit in this register. The pin level on any I/O port which is set for output mode can be controlled by writing to the corresponding bit in this register. 0 : "L" level 1 : "H" level	RW
Pi_1	Port Pi_1 bit		RW
Pi_2	Port Pi_2 bit		RW
Pi_3	Port Pi_3 bit		RW
Pi_4	Port Pi_4 bit		RW
Pi_5	Port Pi_5 bit		RW
Pi_6	Port Pi_6 bit		RW
Pi_7	Port Pi_7 bit		RW

NOTES:
1. Nothing is assigned to the P3_2 and P3_6 bits in the P3 register. When writing to the P3_2 and P3_6 bits, write 0 ("L" level). When read, its content is 0.
2. Nothing is assigned to the P4_0 and P4_1 bits in the P4 register. When write to the P4_0 and P4_1 bits, write 0 ("L" level). When read, its content is 0.

Figure 7.10 Pi (i = 0 to 4 and 6) Registers

Pull-Up Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
PUR0	00FCh	00h

Bit Symbol	Bit Name	Function	RW
PU00	P0_0 to P0_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU01	P0_4 to P0_7 pull-up(1)		RW
PU02	P1_0 to P1_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU03	P1_4 to P1_7 pull-up(1)		RW
PU04	P2_0 to P2_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU05	P2_4 to P2_7 pull-up(1)		RW
PU06	P3_0, P3_1, and P3_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU07	P3_4 to P3_5, and P3_7 pull-up(1)		RW

NOTE:
1. When this bit is set to 1 (pulled up), the pin whose direct bit is set to 0 (input mode) is pulled up.

Pull-Up Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
X	X			0	0		

Symbol	Address	After Reset
PUR1	00FDh	XX00XX00b

Bit Symbol	Bit Name	Function	RW
PU10	P4_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU11	P4_4 and P4_5 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
— (b3-b2)	Reserved bits	Set to 0	RW
PU14	P6_0 to P6_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU15	P6_4 to P6_7 pull-up(1)		RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When this bit is set to 1 (pulled up) and the pin whose direct bit is set to 0 (input mode), the pin is pulled up.

Figure 7.11 Registers PUR0 and PUR1

Port Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0			0	0	0	0

Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0	—
U1PINSEL	Port TXD1/RXD1 switch bit	0 : I/O port P6_6, P6_7 1 : TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0	—
IICSEL	SSU/I²C bus switch bit	0 : SSU function selects 1 : I²C bus function selects	RW

Figure 7.12 PMR Register

7.4 Port Settings

Table 7.4 to Table 7.47 list the port settings.

Table 7.4 Port P0_0/AN7

Register	PD0	ADCON0				Function
Bit	PD0_0	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	1	1	0	A/D converter input (AN7)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.5 Port P0_1/AN6

Register	PD0	ADCON0				Function
Bit	PD0_1	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	1	0	0	A/D converter input (AN6)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.6 Port P0_2/AN5

Register	PD0	ADCON0				Function
Bit	PD0_2	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	0	1	0	A/D converter input (AN5)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.7 Port P0_3/AN4

Register	PD0	ADCON0				Function
Bit	PD0_3	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	0	0	0	A/D converter input (AN4)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.8 Port P0_4/AN3

Register	PD0	ADCON0				Function
Bit	PD0_4	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	1	1	0	A/D converter input (AN3)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.9 Port P0_5/AN2

Register	PD0	ADCON0				Function
Bit	PD0_5	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	1	0	0	A/D converter input (AN2)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.10 Port P0_6/AN1

Register	PD0	ADCON0				Function
Bit	PD0_6	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	0	1	0	A/D converter input (AN1)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.11 Port P0_7/AN0

Register	PD0	ADCON0				Function
Bit	PD0_7	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	0	0	0	A/D converter input (AN0)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.12 Port P1_0/$\overline{\text{KI0}}$/AN8

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_0	KI0EN	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{\text{KI0}}$ input
	0	X	1	0	0	1	A/D converter input (AN8)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.13 Port P1_1/$\overline{\text{KI1}}$/AN9

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_1	KI1EN	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{\text{KI1}}$ input
	0	X	1	0	1	1	A/D converter input (AN9)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.14 Port P1_2/$\overline{KI2}$/AN10

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_2	KI2EN	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{KI2}$ input
	0	X	1	1	0	1	A/D converter input (AN10)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.15 Port P1_3/$\overline{KI3}$/AN11

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_3	KI3EN	CH2	CH1	CH0	ADGSEL0	
Setting value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{KI3}$ input
	0	X	1	1	1	1	A/D converter input (AN11)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.16 Port P1_4/TXD0

Register	PD1	U0MR			Function
Bit	PD1_4	SMD2	SMD1	SMD0	
Setting value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	0	0	1	TXD0 output(2)
		1	0	0	
		1	0	1	
		1	1	0	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the NCH bit in the U0C0 register to 1.

Table 7.17 Port P1_5/RXD0/(TRAIO)/($\overline{INT1}$)

Register	PD1	TRAIOC		TRAMR			INTEN	Function
Bit	PD1_5	TIOSEL	TOPCR	TMOD2	TMOD1	TMOD0	INT1EN	
Setting value	0	0	X	X	X	X	X	Input port(1)
		X	1	X	X	X		
		X	X	Other than 001b				
	1	0	X	X	X	X	X	Output port
		X	1	X	X	X		
		X	X	Other than 001b				
	0	X	X	Other than 001b			X	RXD0 input
		0	X	0	0	1		
	0	1	X	Other than 001b			X	TRAIO input
	0	1	X	Other than 001b			1	TRAIO/$\overline{INT1}$ input
	X	1	0	0	0	1	X	TRAIO pulse output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.18 Port P1_6/CLK0

Register	PD1	U0MR				Function
Bit	PD1_6	SMD2	SMD1	SMD0	CKDIR	
Setting value	0	Other than 001b			X	Input port(1)
		X	X	X	1	
	1	Other than 001b			X	Output port
	0	X	X	X	1	CLK0 (external clock) input
	X	0	0	1	0	CLK0 (internal clock) output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.19 Port P1_7/TRAIO/$\overline{\text{INT1}}$

Register	PD1	TRAIOC		TRAMR			INTEN	Function
Bit	PD1_7	TIOSEL	TOPCR	TMOD2	TMOD1	TMOD0	INT1EN	
Setting value	0	0	X	X	X	X	X	Input port(1)
		X	1	X	X	X		
		X	X	Other than 001b				
	1	1	X	X	X	X	X	Output port
		X	1	X	X	X		
		X	X	Other than 001b				
	0	0	X	Other than 001b			X	TRAIO input
	0	0	X	Other than 001b			1	TRAIO/$\overline{\text{INT1}}$ input
	X	0	0	0	0	1	X	TRAIO pulse output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.20 Port P2_0/TRDIOA0/TRDCLK

Register	PD2	TRDOER1	TRDFCR				TRDIORA0			Function
Bit	PD2_0	EA0	CMD1	CMD0	STCLK	PWM3	IOA2	IOA1	IOA0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	0	1	1	X	X	Timer mode (input capture function)
	0	X	X	X	1	1	0	0	0	External clock input (TRDCLK)
	X	0	0	0	0	0	X	X	X	PWM3 mode waveform output
	X	0	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1
NOTE:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.21 Port P2_1/TRDIOB0

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORA0			Function
Bit	PD2_1	EB0	CMD1	CMD0	PWM3	PWMB0	IOB2	IOB1	IOB0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	0	X	X	X	X	PWM3 mode waveform output
	X	0	0	0	1	1	X	X	X	PWM mode waveform output
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1
NOTE:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.22 Port P2_2/TRDIOC0

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
Bit	PD2_2	EC0	CMD1	CMD0	PWM3	PWMC0	IOC2	IOC1	IOC0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	1	1	X	X	X	PWM mode waveform output
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1

NOTE:

1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.23 Port P2_3/TRDIOD0

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
Bit	PD2_3	ED0	CMD1	CMD0	PWM3	PWMD0	IOD2	IOD1	IOD0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	1	1	X	X	X	PWM mode waveform output
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1

NOTE:

1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.24 Port P2_4/TRDIOA1

Register	PD2	TRDOER1	TRDFCR			TRDIORA1			Function
Bit	PD2_4	EA1	CMD1	CMD0	PWM3	IOA2	IOA1	IOA0	
Setting value	0	1	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	Output port
	0	X	0	0	1	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	Complementary PWM mode waveform output
			1	1					
	X	0	0	1	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)
						0	1	X	

X: 0 or 1

NOTE:

1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.25 Port P2_5/TRDIOB1

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORA1			Function
Bit	PD2_5	EB1	CMD1	CMD0	PWM3	PWMB1	IOB2	IOB1	IOB0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	1	1	X	X	X	PWM mode waveform output
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1
NOTE:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.26 Port P2_6/TRDIOC1

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
Bit	PD2_6	EC1	CMD1	CMD0	PWM3	PWMC1	IOC2	IOC1	IOC0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	1	1	X	X	X	PWM mode waveform output
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1
NOTE:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.27 Port P2_7/TRDIOD1

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
Bit	PD2_7	ED1	CMD1	CMD0	PWM3	PWMD1	IOD2	IOD1	IOD0	
Setting value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	1	1	X	X	X	PWM mode waveform output
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							0	1	X	

X: 0 or 1
NOTE:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.28 Port P3_0/TRAO

Register	PD3	TRAIOC	Function
Bit	PD3_0	TOENA	
Setting value	0	0	Input port(1)
	1	0	Output port
	X	1	TRAO output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 7.29 Port P3_1/TRBO

Register	PD3	TRBMR		TRBIOC	Function
Bit	PD3_1	TMOD1	TMOD0	TOCNT	
Setting value	0	0	0	X	Input port(1)
	1	0	0	X	Output port
	X	01b		1	
	X	Other than 00b		0	TRBO output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 7.30 Port P3_3/SSI

Register	PD3	Clock Synchronous Serial I/O with Chip Select (Refer to **Table 16.4 Association between Communication Modes and I/O Pins**.)		PMR	Function
Bit	PD3_3	SSI output control	SSI input control	IICSEL	
Setting value	0	0	0	0	Input port(1)
	0	X	X	1	
	1	0	0	0	Output port(2)
	1	X	X	1	
	X	0	1	0	SSI input
	X	1	0	0	SSI output(2)

X: 0 or 1
NOTES:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the SOOS bit in the SSMR2 register to 1 when this pin functions as output.

Table 7.31 Port P3_4/SDA/$\overline{\text{SCS}}$

Register	PD3	SSMR2		PMR	ICCR1	Function
Bit	PD3_4	CSS1	CSS0	IICSEL	ICE	
Setting value	0	0	0	0	X	Input port(1)
	0	0	0	X	0	
	1	0	0	0	X	Output port(2)
	1	0	0	X	0	
	X	0	1	0	X	$\overline{\text{SCS}}$ input
	X	1	0	0	X	$\overline{\text{SCS}}$ output(2)
		1	1			
	X	X	X	1	1	SDA input/output

X: 0 or 1
NOTES:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the CSOS bit in the SSMR2 register to 1 when this pin functions as output.

Table 7.32 Port P3_5/SCL/SSCK

Register	PD3	Clock Synchronous Serial I/O with Chip Select (Refer to **Table 16.4 Association between Communication Modes and I/O Pins**.)		PMR	ICCR1	Function
Bit	PD3_5	SSCK output control	SSCK input control	IICSEL	ICE	
Setting value	0	0	0	0	X	Input port(1)
	0	0	0	X	0	
	1	0	0	0	X	Output port(2)
	1	0	0	X	0	
	X	0	1	0	0	SSCK input
	X	1	0	0	0	SSCK output(2)
	X	1	0	1	1	SCL input/output

X: 0 or 1
NOTES:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the CSOS bit in the SSMR2 register to 1 when this pin functions as output.

Table 7.33 Port P3_7/SSO

Register	PD3	Clock Synchronous Serial I/O with Chip Select (Refer to **Table 16.4 Association between Communication Modes and I/O Pins**.)		SSMR2	PMR	Function
Bit	PD3_7	SSO output control	SSO input control	SOOS	IICSEL	
Setting value	0	0	0	X	0	Input port(1)
	0	X	X	X	1	
	1	0	0	0	0	Output port
	1	X	X	0	1	
	X	0	1	0	0	SSO input
	X	1	0	0	0	SSO output (CMOS output)
	X	1	0	1	0	SSO output (N-channel open-drain output)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.

Table 7.34 Port P4_2/VREF

Register	ADCON1	Function
Bit	VCUT	
Setting value	0	Input port
	1	Input port/VREF input

Table 7.35 Port P4_3

Register	PD4	Function
Bit	PD4_3	
Setting value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU10 bit in the PUR0 register to 1.

Table 7.36 Port P4_4

Register	PD4	Function
Bit	PD4_4	
Setting value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU11 bit in the PUR0 register to 1.

Table 7.37 Port P4_5/$\overline{\text{INT0}}$

Register	PD4	INTEN	Function
Bit	PD4_5	INT0EN	
Setting value	0	X	Input port(1)
	1	X	Output port
	0	1	$\overline{\text{INT0}}$ input

X: 0 or 1
NOTE:
1. Pulled up by setting the PU11 bit in the PUR0 register to 1.

Table 7.38 Port P4_6/XIN

Register	CM1		CM0	Circuit specifications		Function
Bit	CM13	CM10	CM05	Oscillation buffer	Feedback resistor	
Setting value	0	X	X	OFF	OFF	Input port
	1	0	0	ON	ON	XIN-XOUT oscillation
	1	0	1	OFF	ON	External XIN input
	1	1	0	OFF	OFF	XIN-XOUT oscillation stop
	1	1	1	OFF	OFF	XIN-XOUT oscillation stop

X: 0 or 1

Table 7.39 Port P4_7/XOUT

Register	CM1		CM0	Circuit specifications		Function
Bit	CM13	CM10	CM05	Oscillation buffer	Feedback resistor	
Setting value	0	X	X	OFF	OFF	Input port
	1	0	0	ON	ON	XIN-XOUT oscillation
	1	0	1	OFF	ON	XOUT is “H” pull-up
	1	1	0	OFF	OFF	XIN-XOUT oscillation stop
	1	1	1	OFF	OFF	XIN-XOUT oscillation stop

X: 0 or 1

Table 7.40 Port P6_0/TREO

Register	PD6	TRECR1	Function
Bit	PD6_0	TOENA	
Setting value	0	0	Input port(1)
	1	0	Output port
	X	1	TREO output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU14 bit in the PUR0 register to 1.

Table 7.41 Port P6_1/CTX0

Register	PD6	C0CTLR	Function
Bit	PD6_1	PortEn	
Setting value	0	0	Input port(1)
	1	0	Output port
	X	1	CTX0 output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU14 bit in the PUR0 register to 1.

Table 7.42 Port P6_2/CRX0

Register	PD6	C0CTLR	Function
Bit	PD6_2	PortEn	
Setting value	0	0	Input port(1)
	1	0	Output port
	X	1	CRX0 input

X: 0 or 1
NOTE:
1. Pulled up by setting the PU14 bit in the PUR0 register to 1.

Table 7.43 Port P6_3

Register	PD6	Function
Bit	PD6_3	
Setting value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU14 bit in the PUR0 register to 1.

Table 7.44 Port P6_4

Register	PD6	Function
Bit	PD6_4	
Setting value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU15 bit in the PUR0 register to 1.

Table 7.45 Port P6_5

Register	PD6	Function
Bit	PD6_5	
Setting value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU15 bit in the PUR0 register to 1.

Table 7.46 Port P6_6/$\overline{\text{INT2}}$/TXD1

Register	PD6	PMR	U1MR			U1C0	INTEN	Function
Bit	PD6_6	U1PINSEL	SMD2	SMD1	SMD0	NCH	INT2EN	
Setting value	0	X	0	0	0	X	X	Input port(1)
		0	X	X	X			
	1	X	0	0	0	X	X	Output port
		0	X	X	X			
	0	X	X	X	X	X	1	$\overline{\text{INT2}}$ input
	X	1	0	0	1	0	X	TXD1 output (CMOS output)
			1	0	0			
			1	0	1			
			1	1	0			
	X	1	0	0	1	1	X	TXD1 output (N-channel open-drain output)
			1	0	0			
			1	0	1			
			1	1	0			

X: 0 or 1
NOTE:
1. Pulled up by setting the PU15 bit in the PUR0 register to 1.

Table 7.47 Port P6_7/$\overline{\text{INT3}}$/RXD1

Register	PD6	PMR	INTEN	Function
Bit	PD6_7	U1PINSEL	INT3EN	
Setting value	0	X	X	Input port(1)
	1	X	X	Output port
	0	X	1	$\overline{\text{INT3}}$ input
	0	1	X	RXD1 input

X: 0 or 1
NOTE:
1. Pulled up by setting the PU15 bit in the PUR0 register to 1.

7.5 Unassigned Pin Handling

Table 7.48 lists Unassigned Pin Handling.

Table 7.48 Unassigned Pin Handling

Pin Name	Connection
Ports P0 to P2, P3_0, P3_1, P3_3 to P3_7, P4_3 to P4_5, P6	• After setting to input mode, connect every pin to VSS via a resistor (pull-down) or connect every pin to VCC via a resistor (pull-up).(2) • After setting to output mode, leave these pins open.(1,2)
Ports P4_6, P4_7	Connect to VCC via a resistor (pull-up)(2)
Port P4_2/VREF	Connect to VCC
$\overline{\text{RESET}}$(3)	Connect to VCC via a resistor (pull-up)(2)

NOTES:
1. If these ports are set to output mode and left open, they remain input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) as possible.
3. When power-on reset function is in use.

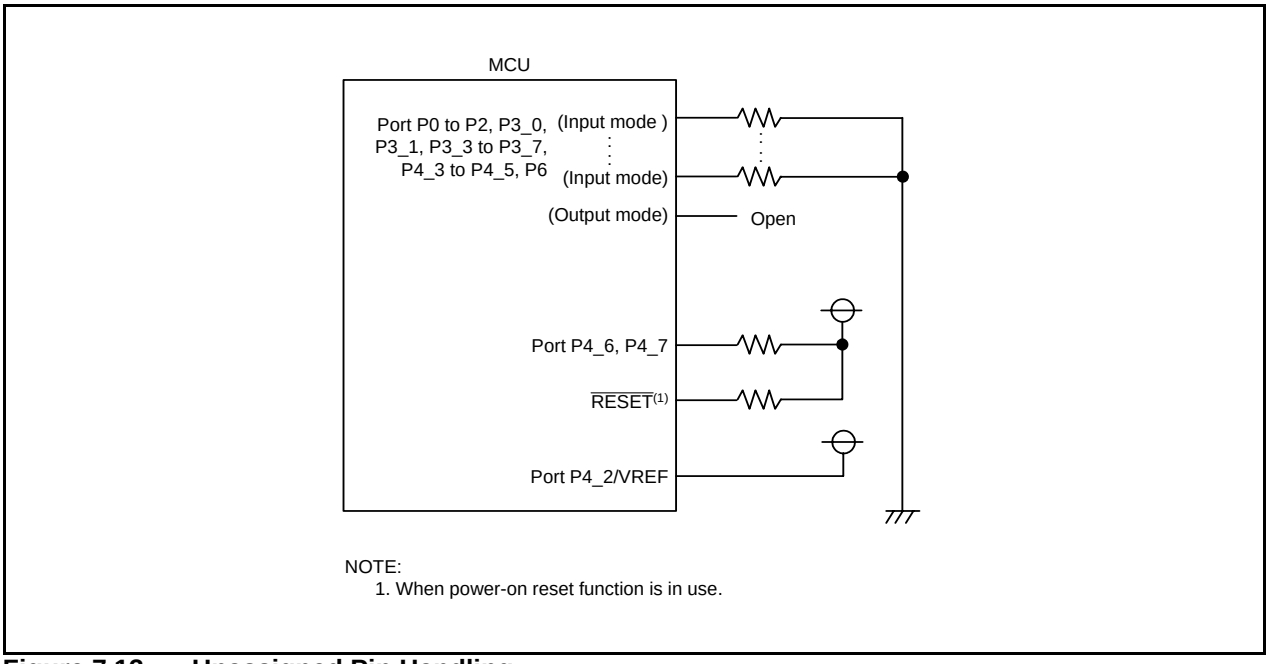


Figure 7.13 Unassigned Pin Handling

8. Processor Mode

8.1 Processor Modes

Single-chip mode can be selected as processor mode.
Table 8.1 lists Features of Processor Mode. Figure 8.1 shows the PM0 Register and Figure 8.2 shows the PM1 Register.

Table 8.1 Features of Processor Mode

Processor Mode	Accessible Areas	Pins Assignable as I/O Port Pins
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

Processor Mode Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
×	×	×	×	×	0	0	0

Symbol: PM0 | Address: 0004h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0	RW
PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, its content is 0.	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Set the PRC1 bit in the PRCR register to 1 (enables writing) before rewriting to the PM0 register.

Figure 8.1 PM0 Register

Processor Mode Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	×	×	×	×	×	0	0

Symbol: PM1 | Address: 0005h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
PM12	WDT interrupt/reset switch bit	0 : Watchdog timer interrupt 1 : Watchdog timer reset(2)	RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b7)	Reserved bit	Set to 0	RW

NOTES :
1. Set the PRC1 bit in the PRCR register to 1 (enables writing) before rewriting to the PM1 register.
2. The PM12 bit is set to 1 by a program (it remains unchanged even if it is set to 0).
When the CSPRO bit in the CSPR register is set to 1 (selects count source protect mode), the PM12 bit is automatically set to 1.

Figure 8.2 PM1 Register

9. Bus

The bus cycles differ when accessing ROM/RAM, and when accessing SFR.
Table 9.1 lists Bus Cycles by Access Space of the R8C/22 Group and Table 9.2 lists Bus Cycles by Access Space of the R8C/23 Group.
The ROM/RAM and SFR are connected to the CPU through an 8-bit bus. When accessing in word-(16 bits) unit, these area are accessed twice in 8-bit unit.
Table 9.3 lists Access Unit and Bus Operations.

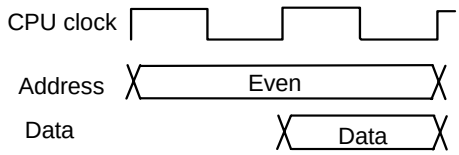
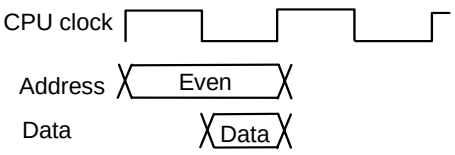
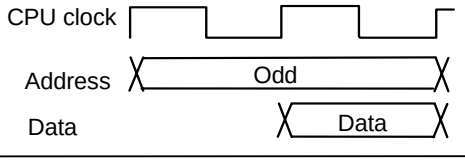
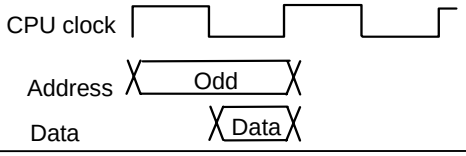
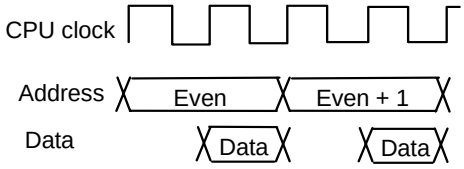
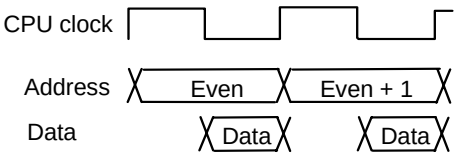
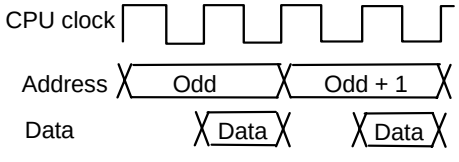
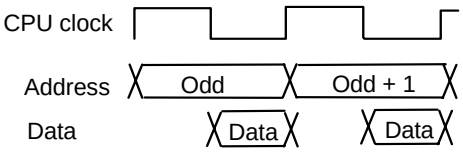
Table 9.1 Bus Cycles by Access Space of the R8C/22 Group

Access Area	Bus Cycle
SFR	2 cycles of CPU clock
ROM/RAM	1 cycle of CPU clock

Table 9.2 Bus Cycles by Access Space of the R8C/23 Group

Access Area	Bus Cycle
SFR/Data flash	2 cycles of CPU clock
Program ROM/RAM	1 cycle of CPU clock

Table 9.3 Access Unit and Bus Operations

Area	SFR, data flash	ROM (program ROM), RAM
Even address byte access		
Odd address byte access		
Even address word access		
Odd address word access		

However, only following SFRs are connected with the 16-bit bus:
Timer RD: registers TRDi (i = 0, 1), TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, data flash, even address byte access” in Table 9.3 Access Unit and Bus Operations, and 16-bit data is accessed at a time.

10. Clock Generation Circuit

The clock generation circuit has:

- XIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator

Table 10.1 lists Specifications of Clock Generation Circuit. Figure 10.1 shows a Clock Generation Circuit. Figures 10.2 to 10.8 show clock-associated registers.

Table 10.1 Specifications of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	On-Chip Oscillator	
		High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Use of Clock	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when XIN clock stops oscillating
Clock Frequency	0 to 20 MHz	Approx. 40 MHz(3)	Approx. 125 kHz
Connectable Oscillator	• Ceramic resonator • Crystal oscillator	–	–
Oscillator Connect Pins	XIN, XOUT(1)	–(1)	–(1)
Oscillation Stop, Restart Function	Usable	Usable	Usable
Oscillator Status After Reset	Stop	Stop	Oscillate
Others	Externally generated clock can be input(2)	–	–

NOTES:

1. These pins can be used as P4_6 and P4_7 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit is not used.
2. Set the CM05 bit in the CM0 register to 1 (main clock stops) and the CM13 bit in the CM1 register to 1 (XIN-XOUT pin) when the external clock is input.
3. The clock frequency is automatically set to up to 20 MHz by a driver when using the high-speed on-chip oscillator as the CPU clock source.

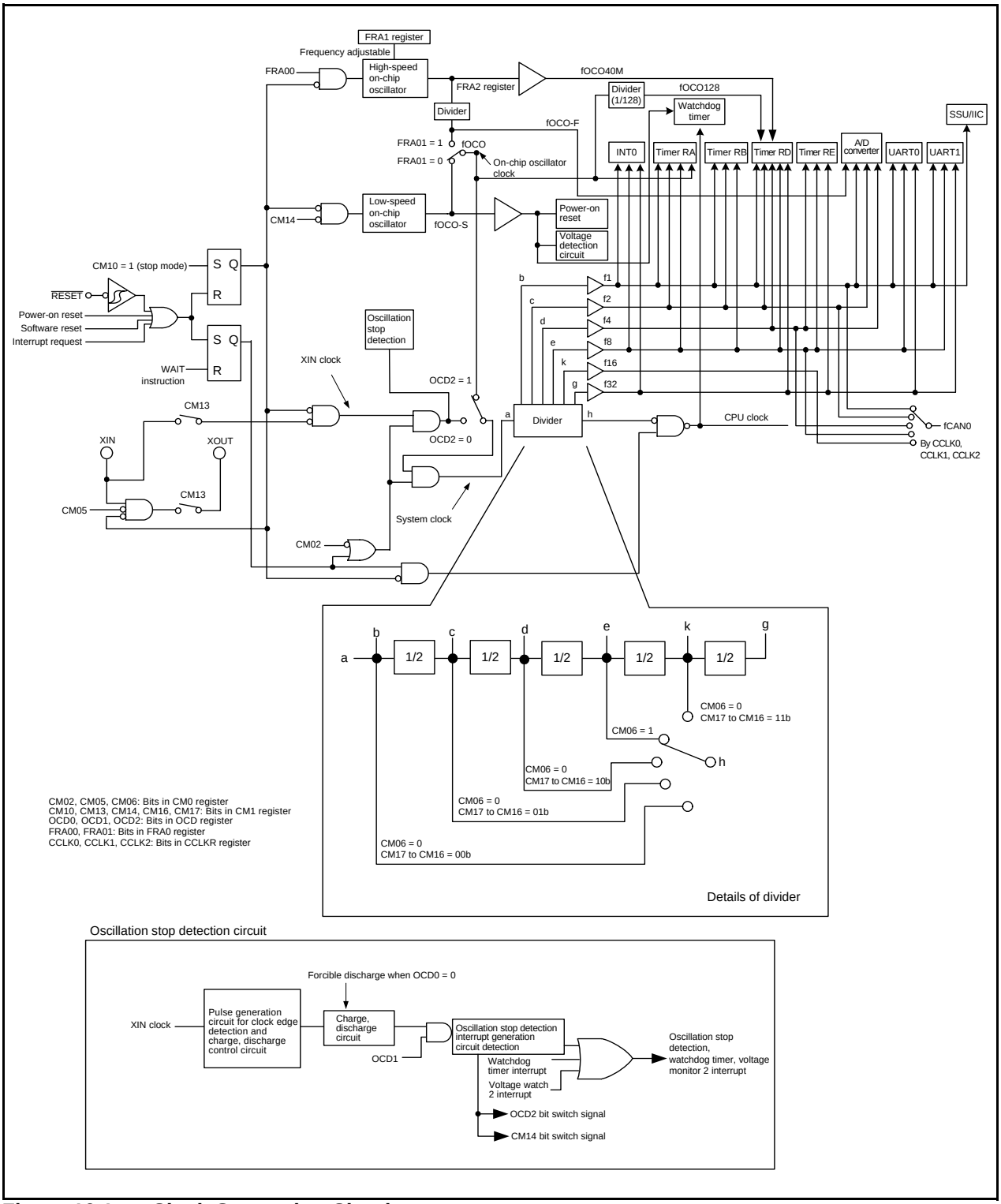


Figure 10.1 Clock Generation Circuit

System Clock Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
0			0	1		0	0

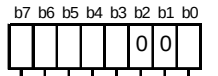
Symbol	Address	After Reset
CM0	0006h	01101000b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
CM02	WAIT peripheral function clock stop bit	0 : Peripheral function clock does not stop in wait mode 1 : Peripheral function clock stops in wait mode	RW
— (b3)	Reserved bit	Set to 1	RW
— (b4)	Reserved bit	Set to 0	RW
CM05	XIN clock (XIN-XOUT) stop bit(2,4)	0 : XIN clock oscillates 1 : XIN clock stops(3)	RW
CM06	System clock division select bit 0(5)	0 : Enables CM16, CM17 1 : Divide-by-8 mode	RW
— (b7)	Reserved bit	Set to 0	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (enables writing) before rewriting to the CM0 register.
2. The CM05 bit is to stop the XIN clock when the high-speed on-chip oscillator mode, low-speed on-chip oscillator mode is selected. Do not use this bit for whether the XIN clock is stopped. To stop the XIN clock, set the bits in the following orders:
   (a) Set the OCD0 and OCD1 bits in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (selects on-chip oscillator clock).
3. During external clock input, only the clock oscillation buffer is turned off and clock input is acknowledged.
4. P4_6 and P4_7 can be used as input ports when the CM05 bit is set to 1 (XIN clock stops) and the CM13 bit in the CM1 register is set to 0 (P4_6, P4_7).
5. When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Figure 10.2 CM0 Register

System Clock Control Register 1(1)



Symbol	Address	After Reset
CM1	0007h	00100000b

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit(4,7,8)	0 : Oscillates clock 1 : Stops all clocks (stop mode)	RW
— (b2-b1)	Reserved bits	Set to 0	RW
CM13	Port XIN-XOUT switch bit(7,9)	0 : Input ports P4_6, P4_7 1 : XIN-XOUT pin	RW
CM14	Low-speed on-chip oscillation stop bit(5,6,8)	0 : Low-speed on-chip oscillator on 1 : Low-speed on-chip oscillator off	RW
CM15	XIN-XOUT drive capacity select bit(2)	0 : Low 1 : High	RW
CM16	System clock division select bits 1(3)	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (enables writing) before rewriting to the CM1 register.
2. When entering stop mode, the CM15 bit is set to 1 (drive capacity high).
3. When the CM06 bit is set to 0 (CM16, CM17 bits enabled), the CM16 to CM17 bits become enabled.
4. If the CM10 bit is 1 (stop mode), the internal feedback resistor becomes disabled.
5. When the OCD2 bit is set to 0 (selects XIN clock), the CM14 bit is set to 1 (stops low-speed on-chip oscillator). When the OCD2 bit is set to 1 (selects on-chip oscillator clock), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if it is set to 1.
6. When using the low voltage 2 detection interrupt (when using the digital filter), set the CM14 bit to 0 (low-speed on-chip oscillator on).
7. When the CM10 bit is set to 1 (stop mode) and the CM13 bit is set to 1 (XIN-XOUT pin), the XOUT (P4_7) pin becomes “H”. When the CM13 bit is set to 0 (input ports, P4_6, P4_7), the P4_7 (XOUT) enters input mode.
8. In count source protect mode (Refer to **13.2 Count Source Protection Mode Enabled**), the value remains unchanged even if the CM10 and CM14 bits are set.
9. Once the CM13 bit is set to 1, it can not to 0 in a program.

Figure 10.3 CM1 Register

Oscillation Stop Detection Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

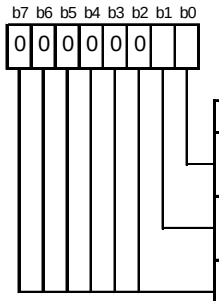
Symbol: OCD | Address: 000Ch | After Reset: 00000100b

Bit Symbol	Bit Name	Function	RW
OCD0	Oscillation stop detection enable bit(7)	0 : Oscillation stop detection function disabled(2) 1 : Oscillation stop detection function enabled	RW
OCD1	Oscillation stop detection interrupt enable bit	0 : Disable(2) 1 : Enable	RW
OCD2	System clock select bit(4)	0 : Selects XIN clock(7) 1 : Selects on-chip oscillator clock(3)	RW
OCD3	Clock monitor bit(5,6)	0 : XIN clock oscillates 1 : XIN clock stops	RO
— (b7-b4)	Reserved bits	Set to 0	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (enables writing) before rewriting to the OCD register.
2. Set the OCD1 to OCD0 bits to 00b before entering stop and high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stops). Set the OCD1 to OCD0 bits to 00b when the FRA01 bit in the FRA0 register is set to 1 (selects high-speed on-chip oscillator).
3. The CM14 bit is set to 0 (low-speed on-chip oscillator on) if the OCD2 bit is set to 1 (selects on-chip oscillator clock).
4. The OCD2 bit is automatically set to 1 (selects on-chip oscillator clock) if a XIN clock oscillation stop is detected while the OCD1 to OCD0 bits are set to 11b. If the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged when writing 0 (selects XIN clock).
5. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
6. The OCD3 bit remains 0 (XIN clock oscillates) if the OCD1 to OCD0 bits are set to 00b.
7. Refer to **Figure 10.14 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Figure 10.4 OCD Register

High-Speed On-Chip Oscillator Control Register 0(1)

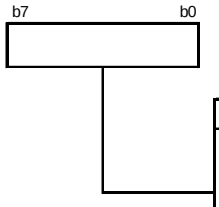


Symbol	Address	After Reset
FRA0	0023h	00h

Bit Symbol	Bit Name	Function	RW
FRA00	High-speed on-chip oscillator enable bit	0 : High-speed on-chip oscillator off 1 : High-speed on-chip oscillator on	RW
FRA01	High-speed on-chip oscillator select bit(2)	0 : Selects low-speed on-chip oscillator(3) 1 : Selects high-speed on-chip oscillator	RW
— (b7-b2)	Reserved bits	Set to 0	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (enables writing) before rewriting to the FRA0 register.
2. Change the FRA01 bit under the following conditions.
   • FRA00 = 1 (high-speed on-chip oscillation)
   • The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   • Bits FRA22 to FRA20 in the FRA2 register
   All divide ratio mode settings are supported when VCC = 3.0 V to 5.5 V (D, J version) 000b to 111b
   Divide ratio of 4 or more when VCC = 2.7 V to 5.5 V and K version 010b to 111b
3. When setting the FRA01 bit to 0 (selects low-speed on-chip oscillator), do not set the FRA00 bit to 0 (40MHz on-chip oscillator off) at the same time.
   Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

High-Speed On-Chip Oscillator Control Register 1(1)



Symbol	Address	After Reset
FRA1	0024h	When Shipping

Function	RW
The frequency of high-speed on-chip oscillator is adjusted with bits 0 to 7. High-speed on-chip oscillator frequency = 40 MHz (FRA1 register = value when shipping) Set the value of the FRA1 register to smaller, the frequency will be higher Set the value of the FRA1 register to larger, the frequency will be lower(2)	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting to the FRA1 register.
   When adjusting the FRA1 register, set the value of the FRA1 register to 40 MHz and below.
2. When changing the values of the FRA1 register, adjust the FRA1 register so that the frequency of the high-speed on-chip oscillator clock will be 40 MHz or less.

Figure 10.5 Registers FRA0 and FRA1

High-Speed On-Chip Oscillator Control Register 2(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

Symbol	Address	After Reset
FRA2	0025h	00h

Bit Symbol	Bit Name	Function	RW
FRA20	High-speed on-chip oscillator frequency switching bits(2)	The division of high-speed on-chip oscillator clock can be selected. b2 b1 b0 0 0 0 : Divide-by-2 mode(3) 0 0 1 : Divide-by-3 mode(3) 0 1 0 : Divide-by-4 mode 0 1 1 : Divide-by-5 mode 1 0 0 : Divide-by-6 mode 1 0 1 : Divide-by-7 mode 1 1 0 : Divide-by-8 mode 1 1 1 : Divide-by-9 mode	RW
FRA21			RW
FRA22			RW
— (b7-b3)	Reserved bits	Set to 0	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (enables writing) before rewriting to the FRA2 register.
2. Since the value after reset is 000b, set 010b to 111b on the K version products.
3. Do not set on the K version products.

Figure 10.6 FRA2 Register

Voltage Detection Register 2(1)

b7	b6	b5	b4	b3	b2	b1	b0
		0	0	0	0	0	

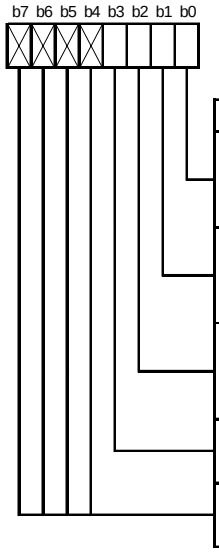
Symbol	Address	After Reset(4)
VCA2	0032h	The LVD1ON bit in the OFS register is set to 1: 00h Power-on reset, voltage monitor 1 reset or the LVD1ON bit in the OFS register is set to 0: 01000000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(5)	0 : Disables low consumption 1 : Enables low consumption	RW
— (b5-b1)	Reserved bits	Set to 0	RW
VCA26	Voltage detection 1 enable bit(2)	0 : Voltage detection 1 circuit disabled 1 : Voltage detection 1 circuit enabled	RW
VCA27	Voltage detection 2 enable bit(3)	0 : Voltage detection 2 circuit disabled 1 : Voltage detection 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (enables writing) before writing to the VCA2 register.
2. When using the voltage monitor 1 reset, set the VCA26 bit to 1.
   After the VCA26 bit is set from 0 to 1, the voltage detection circuit elapses for td(E-A) before starting operation.
3. When using the voltage monitor 2 interrupt/reset or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is from 0 to 1, the voltage detection circuit elapses for td(E-A) before starting operation.
4. The VCA27 bit remains unchanged after software reset, watchdog timer reset, and voltage monitor 2 reset.
5. Use the VCA20 bit only when entering to wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.11 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

Figure 10.7 VCA2 Register

CAN0 Clock Select Register(1)



Symbol	Address	After Reset
CCLKR	135Fh	00h

Bit Symbol	Bit Name	Function	RW
CCLK0	CAN0 clock select bits(2)	b2 b1 b0 0 0 0 : No division 0 0 1 : Divide-by-2 mode 0 1 0 : Divide-by-4 mode 0 1 1 : Divide-by-8 mode 1 0 0 : Divide-by-16 mode 1 0 1 : 1 1 0 : Do not set 1 1 1 :	RW
CCLK1			RW
CCLK2			RW
CCLK3	CAN0 CPU interface sleep bit(3)	0 : CAN0 CPU interface operating 1 : CAN0 CPU interface in sleep	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

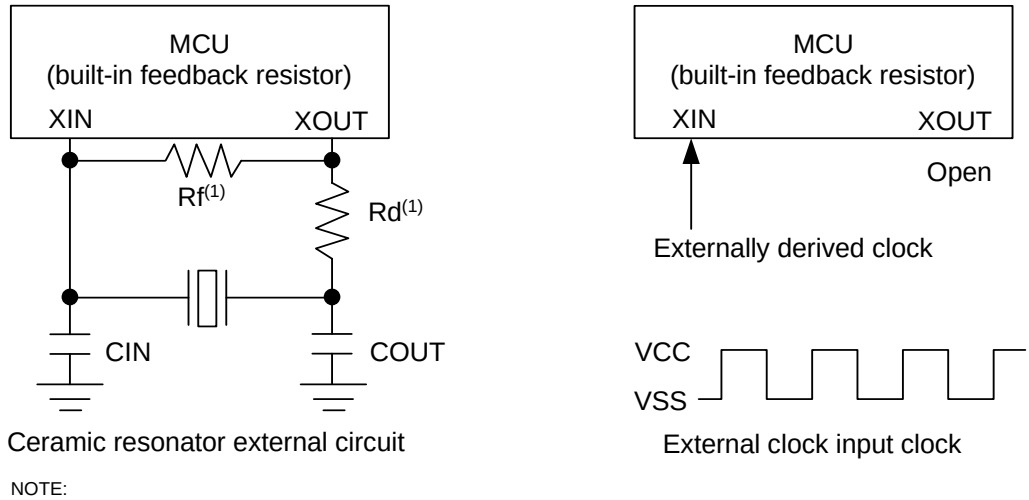
NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (enables writing) before rewriting to the CCLKR register.
2. Set to the CCLK2, CCLK1, CCLK0 bits, only when the Reset bit in the C0CTLR register is 1 (reset/initialization mode).
3. When set the CCLK3 bit to 1 (CAN0 CPU interface operating), set to the Sleep bit in the C0CTLR register to 1 before setting the CCLK3 bit.

Figure 10.8 CCLKR Register

The following describes the clocks generated by the clock generation circuit.

10.1 XIN Clock

This clock is supplied by a XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between the XIN and XOUT pins. The XIN clock oscillation circuit contains a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed in the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XIN pin.
Figure 10.9 shows Examples of XIN Clock Connection Circuit. During or after reset, the XIN clock stops.
The XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock on) after setting the CM13 bit in the CM1 register to 1 (XIN- XOUT pin).
To use the XIN clock for the CPU clock source, set the OCD2 bit in the OCD register to 0 (select XIN clock) after the XIN clock is oscillating stably.
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (stop XIN clock) if the OCD2 bit is set to 1 (select on-chip oscillator clock).
When the clocks externally generated to the XIN pin are input, a XIN clock does not stop if setting the CM05 bit to 1. If necessary, use an external circuit to stop the clock.
In stop mode, all clocks including the XIN clock stop. Refer to **10.4 Power Control** for details.



NOTE:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the maker of the oscillator.
Use high drive when oscillation starts and, if it is necessary to switch the oscillation drive capacity, do so after oscillation stabilizes.
When the oscillation drive capacity is set to low, check that oscillation is stable. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip, insert a feedback resistor between XIN and XOUT following the instruction.

Figure 10.9 Examples of XIN Clock Connection Circuit

10.2 On-Chip Oscillator Clocks

This clock is supplied by an on-chip oscillator. The on-chip oscillator contains a high-speed on-chip oscillator and a low-speed on-chip oscillator. Either an on-chip oscillator clock is selected by the FRA01 bit in the FRA0 register.

10.2.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, and fOCO-S.

After reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator by divide-by-8 is selected for the CPU clock.

If the XIN clock stops oscillating when the OCD1 to OCD0 bits in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating, supplying the necessary clock for the MCU.

The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. The application products must be designed with sufficient margin to accommodate the frequency range.

10.2.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-F and fOCO40M.

To use the high-speed on-chip oscillator clock as the clock source of the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows;

All divide ratio mode settings are supported when VCC = 3.0 V to 5.5 V (D, J version) 000b to 111b

Divide ratio of 4 or more when VCC = 2.7 V to 5.5 V and K version 010b to 111b

After reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. The oscillation starts by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on). The frequency can be adjusted by the FRA1 and FRA2 registers.

Since there are differences in the amount of frequency adjustment among the bits in the FRA1 register, make adjustments by changing the settings of individual bits.

Adjust the amount of high-speed on-chip oscillator frequency to 40 MHz and below by setting the FRA1 register.

10.3 CPU Clock and Peripheral Function Clock

There are two type clocks: a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. Refer to **Figure 10.1 Clock Generation Circuit**.

10.3.1 System Clock

The system clock is a clock source for the CPU and peripheral function clocks. The XIN clock or on-chip oscillator clock can be selected.

10.3.2 CPU Clock

The CPU clock is an operating clock for the CPU and watchdog timer.
The system clock can be the divide-by-1 (no division), 2, 4, 8 or 16 to produce the CPU clock. Use the CM06 bit in the CM0 register and the CM16 to CM17 bits in the CM1 register to select the value of the division.
After reset, the low-speed on-chip oscillator clock divided-by-8 provides the CPU clock.
When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

10.3.3 Peripheral Function Clock (f1, f2, f4, f8, f32, and fCAN0)

The peripheral function clock is operating clock for the peripheral functions.
The clock fi (i = 1, 2, 4, 8, 32) is generated by the system clock divided-by-i. The clock fi is used for timers RA, RB, RD, RE, serial interface, A/D converter and CAN module.
The clock fCAN0 is generated by the f1 clock divided-by-1(no-division), -2, -4, -8, or -16, and is used for CAN module.
When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode), the clock fi and fCAN0 stop.(1)

NOTE:
1. fCAN0 clock stops at high level in CAN0 sleep mode.

10.3.4 fOCO

fOCO is operating clocks for the peripheral functions.
The fOCO run at the same frequency as the on-chip oscillator clock and can be used as the source for the timer RA.
When the WAIT instruction is executed, the clocks fOCO does not stop.

10.3.5 fOCO40M

fOCO40M is used as the count source for the timer RD. The fOCO40M is generated by the high-speed on-chip oscillator and provided by setting the FRA00 bit to 1.
When the WAIT instruction is executed, the clock fOCO40M does not stop.
fOCO40M can be used with supply voltage VCC = 3.0 to 5.5V.

10.3.6 fOCO-F

fOCO-F is used as the count source for the AD converter. The fOCO-F is generated by the high-speed on-chip oscillator and provided by setting the FRA00 bit to 1.
When the WAIT instruction is executed, the clock fOCO-F does not stop.

10.3.7 fOCO-S

fOCO-S is an operating clock for the watchdog timer and voltage detection circuit. When setting the CM14 bit to 0 (low-speed on-chip oscillator on) using the clock generated by the low-speed on-chip oscillator, the fOCO-S can be provided. When the WAIT instruction is executed or in count source protect mode of the watchdog timer, the clock fOCO-S does not stop.

10.3.8 fOCO128

fOCO128 is generated by fOCO divided-by-128. The clock fOCO128 is used for capture signal of timer RD (channel 0).

10.4 Power Control

There are three power control modes. All modes other than wait and stop modes are referred to as standard operating mode.

10.4.1 Standard Operating Mode

Standard operating mode is further separated into three modes.
In standard operating mode, the CPU clock and the peripheral function clock are supplied to operate the CPU and the peripheral function clocks. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. When unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source after switching needs to be stabilized and oscillated. If the new clock source is the XIN clock, allow sufficient wait time in a program until an oscillation is stabilized before exiting.

Table 10.2 Settings and Modes of Clock Associated Bits

Modes		OCD Register	CM1 Register			CM0 Register		FRA0 Register	
		OCD2	CM17, CM16	CM14	CM13	CM06	CM05	FRA01	FRA00
High-speed clock mode	No division	0	00b	–	1	0	0	–	–
	Divide-by-2	0	01b	–	1	0	0	–	–
	Divide-by-4	0	10b	–	1	0	0	–	–
	Divide-by-8	0	–	–	1	1	0	–	–
	Divide-by-16	0	11b	–	1	0	0	–	–
High-speed on-chip oscillator mode	No division	1	00b	–	–	0	–	1	1
	Divide-by-2	1	01b	–	–	0	–	1	1
	Divide-by-4	1	10b	–	–	0	–	1	1
	Divide-by-8	1	–	–	–	1	–	1	1
	Divide-by-16	1	11b	–	–	0	–	1	1
Low-speed on-chip oscillator mode	No division	1	00b	0	–	0	–	0	–
	Divide-by-2	1	01b	0	–	0	–	0	–
	Divide-by-4	1	10b	0	–	0	–	0	–
	Divide-by-8	1	–	0	–	1	–	0	–
	Divide-by-16	1	11b	0	–	0	–	0	–

–: can be 0 or 1, no change in outcome.

10.4.1.1 High-Speed Clock Mode

The XIN clock divided-by-1 (no division), -2, -4, -8, or -16 provides the CPU clock. Set the CM06 bit to 1 (divide-by-8 mode) when transiting to high-speed on-chip oscillator mode, low-speed on-chip oscillator mode.
If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), the fOCO can be used for timers RA.
When the FRA00 bit is set to 1, fOCO40M can be used for timer RD.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the watchdog timer and voltage detection circuit.

10.4.1.2 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided-by-1 (no division), -2, -4, -8 or -16 provides the CPU clock. Set the CM06 bit to 1 (divide-by-8) when transiting to high-speed clock mode.
If the FRA00 bit is set to 1, fOCO40M can be used for timer RD.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the watchdog timer and voltage detection circuit.

10.4.1.3 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) or the FRA01bit in the FRA0 register is set to 0, the low-speed on-chip oscillator provides the on-chip oscillator clock.
The on-chip oscillator clock divided-by-1 (no division), -2, -4, -8 or -16 provides the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. Set the CM06 bit to 1 (divide-by-8 mode) when transiting to high-speed clock mode. When the FRA00 bit is set to 1, fOCO40M can be used for timer RD. When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the watchdog timer and voltage detection circuit.
In this mode, stopping the XIN clock and high-speed on-chip oscillator, and setting the FMR47 bit in the FMR4 register to 1 (flash memory low consumption current read mode enabled) enables low consumption operation.
To enter wait mode from low-speed on-chip oscillator mode, setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled) enables lower consumption current in wait mode.
When enabling reduced internal power consumption using the VCA20 bit, follow **Figure 10.11 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

10.4.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU operated in the CPU clock and the watchdog timer when count source protection mode is disabled stops. The XIN clock and on-chip oscillator clock do not stop and the peripheral functions using these clocks maintain operating.

10.4.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, f32, and fCAN0 clocks stop in wait mode. The power consumption can be reduced.

10.4.2.2 Entering Wait Mode

The MCU enters wait mode when the WAIT instruction is executed.
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction.
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.

10.4.2.3 Pin Status in Wait Mode

The I/O port is the status before wait mode was entered is maintained.

10.4.2.4 Exiting Wait Mode

The MCU exits wait mode by a hardware reset or peripheral function interrupt. When using a hardware reset to exit wait mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to 000b (interrupts disabled) before executing the WAIT instruction.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), all peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop operating and the peripheral functions operated by external signals can be used to exit wait mode.
Table 10.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 10.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial Interface Interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Clock Synchronous Serial I/O with Chip Select Interrupt / I^2C Bus Interface Interrupt	Usable in all modes	– (Do not use)
Key Input Interrupt	Usable	Usable
A/D Conversion Interrupt	Usable in one-shot mode	– (Do not use)
Timer RA Interrupt	Usable in all modes	Can be used if there is no filter in event counter mode. Usable by selecting fOCO as count source.
Timer RB Interrupt	Usable in all modes	– (Do not use)
Timer RD Interrupt	Usable in all modes	Usable by selecting fOCO40M as count source
Timer RE Interrupt	Usable in all modes	– (Do not use)
$\overline{INT}$ Interrupt	Usable	Usable ($\overline{INT0}$ to $\overline{INT3}$ can be used if there is no filter.)
Voltage Monitor 2 Interrupt	Usable	Usable
Oscillation Stop Detection Interrupt	Usable	– (Do not use)
CAN0 Wake-Up Interrupt	Usable in CAN sleep mode	Usable in CAN sleep mode

Figure 10.10 shows the Time from Wait Mode to Interrupt Routine Execution.
When using a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level to the ILVL2 to ILVL0 bits in the interrupt control register of the peripheral function interrupts to use for exiting wait mode. Set the ILVL2 to ILVL0 bits of the peripheral function interrupts not to use for exiting wait mode to 000b (disables interrupt).
(2) Set the I flag to 1.
(3) Operate the peripheral function to use for exiting wait mode.

When exiting by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register as described in Figure 10.10.
The CPU clock, when exiting wait mode by a peripheral function interrupt, is the same clock as the CPU clock when the WAIT instruction is executed.

FMR0 Register FMSTP Bit	Time until Flash Memory is Activated (T1)	Time until CPU Clock is Supplied (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	Period of system clock × 12 cycles + 30 μs (max.)	Period of CPU clock × 6 cycles	Period of CPU clock × 20 cycles	Following total time is the time from wait mode until an interrupt routine is executed.
1 (flash memory stops)	Period of system clock × 12 cycles	Same as above	Same as above	

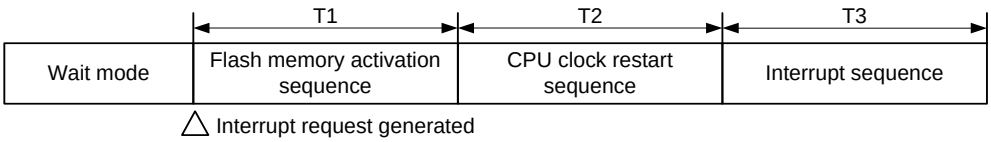
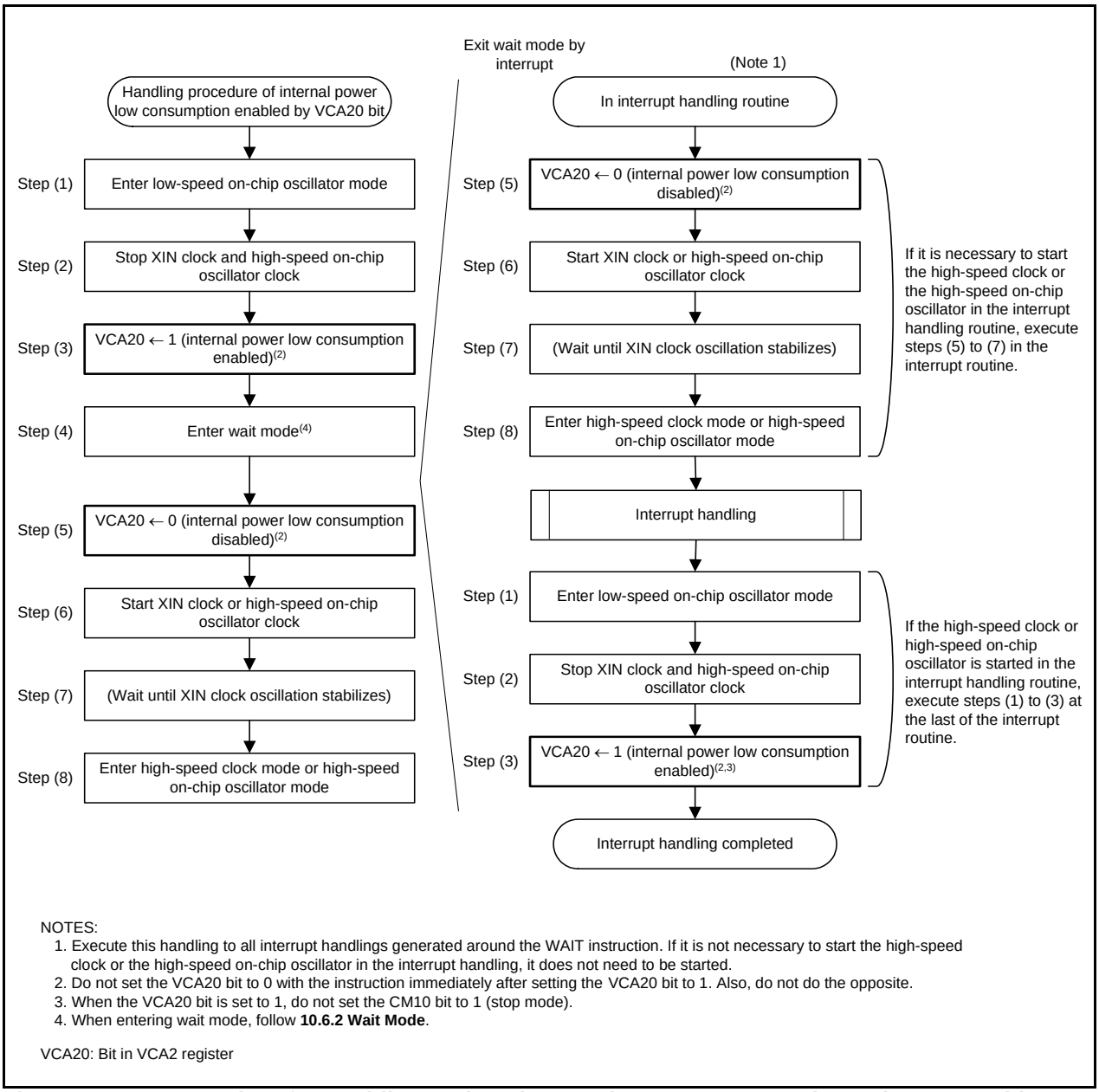


Figure 10.10 Time from Wait Mode to Interrupt Routine Execution

10.4.2.5 Reducing Internal Power Consumption

Internal power consumption can be reduced by using low-speed on-chip oscillator mode.
Figure 10.11 shows the Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit.
When enabling reduced internal power consumption using the VCA20 bit, follow **Figure 10.11 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.



NOTES:
1. Execute this handling to all interrupt handlings generated around the WAIT instruction. If it is not necessary to start the high-speed clock or the high-speed on-chip oscillator in the interrupt handling, it does not need to be started.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When entering wait mode, follow **10.6.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 10.11 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit

10.4.3 Stop Mode

Since the oscillator circuits stop in wait mode, the CPU clock and peripheral function clock stop and the CPU and peripheral functions clocked by these clocks stop operating. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the internal RAM is maintained.
The peripheral functions clocked by external signals maintain operating.
Table 10.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 10.4 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key Input Interrupt	–
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ Interrupt	Can be used if there is no filter
Timer RA Interrupt	When there is no filter and external pulse is counted in event counter mode
Serial Interface Interrupt	When external clock is selected
Voltage Monitor 2 Interrupt	Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)
CAN0 Wake-Up Interrupt	Usable in CAN sleep mode

10.4.3.1 Entering Stop Mode

The MCU enters stop mode by setting the CM10 bit in the CM1 register to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode) and the CM15 bit in the CM10 register is set to 1 (drive capability HIGH of XIN clock oscillator circuit).
When using stop mode, set the OCD1 to OCD0 bits to 00b before entering stop mode.

10.4.3.2 Pin Status in Stop Mode

The status before entering wait mode is maintained.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pins), the XOUT(P4_7) pin is held “H”. When the CM13 bit is set to 0 (input port P4_6 and P4_7), the P4_7(XOUT) is held in input status.

10.4.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
When using a reset to exit stop mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to 000b (disables interrupts) before setting the CM10 bit to 1.
Figure 10.12 shows the Time from Stop Mode to Interrupt Routine Execution.
When using a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level to the ILVL2 to ILVL0 bits of the peripheral function interrupts to use for exiting stop mode. Set the ILVL2 to ILVL0 bits of the peripheral function interrupts not to use for exiting stop mode to 000b (disables interrupt).
(2) Set the I flag to 1.
(3) Operates the peripheral function to use for exiting stop mode.
When exiting by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply is started.

If the clock used immediately before stop mode is a system clock and stop mode is exited by a peripheral function interrupt, the CPU clock becomes the previous system clock divided by 8.

FMR0 Register FMSTP Bit	Time until Flash Memory is Activated (T2)	Time until CPU Clock is Supplied (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	Period of system clock × 12 cycles + 30 µs (max.)	Period of CPU clock × 6 cycles	Period of CPU clock × 20 cycles	Following total time of T0 to T4 is the time from wait mode until an interrupt routine is executed.
1 (flash memory stops)	Period of system clock × 12 cycles	Same as above	Same as above	

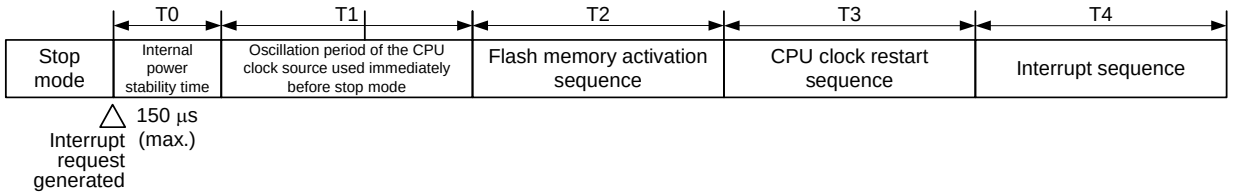


Figure 10.12 Time from Stop Mode to Interrupt Routine Execution

Figure 10.13 shows the State Transitions in Power Control Mode.

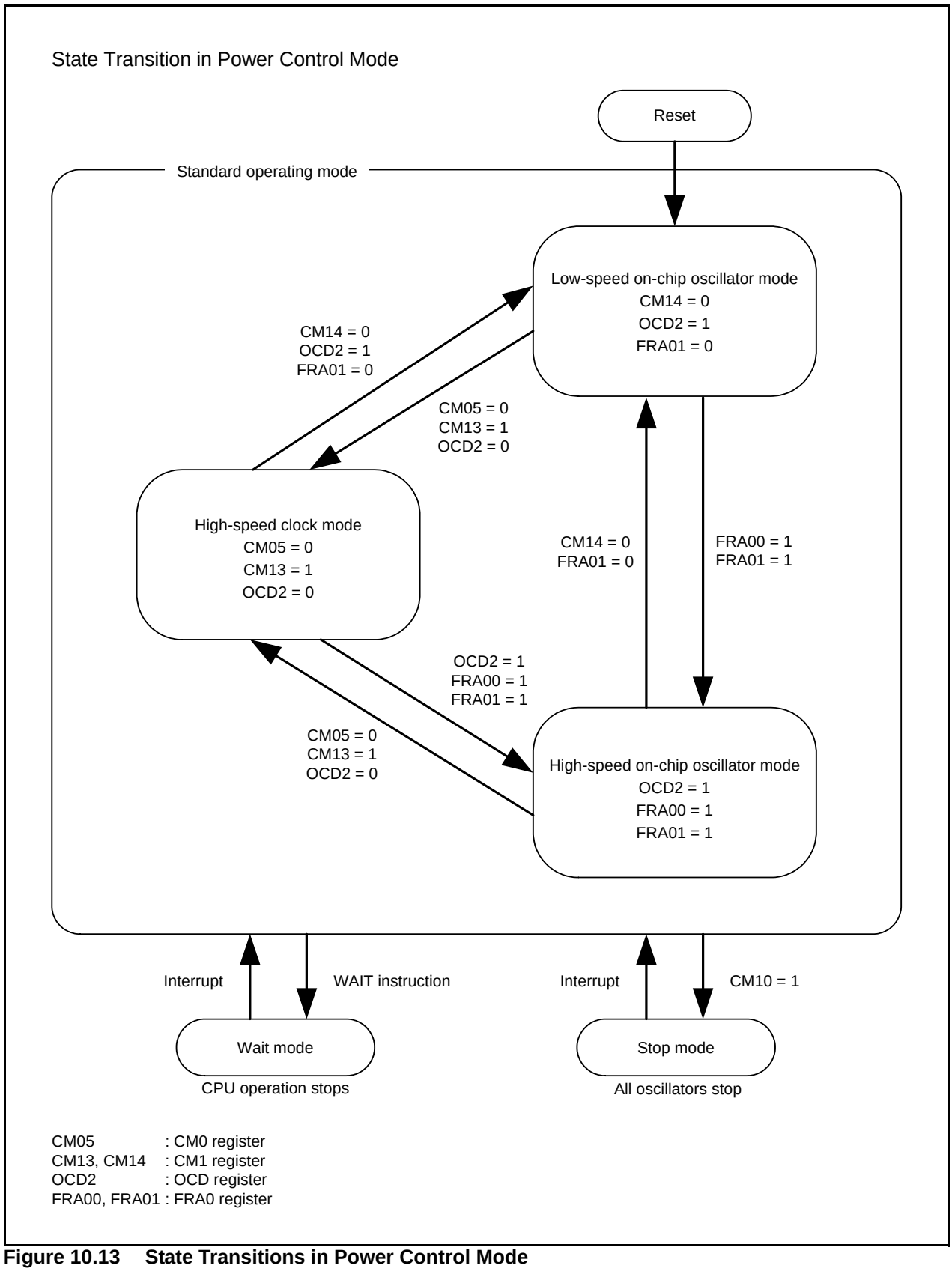


Figure 10.13 State Transitions in Power Control Mode

10.5 Oscillation Stop Detection Function

The oscillation stop detection function is a function to detect the stop of the XIN clock oscillating circuit. The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 10.5 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and the OCD1 to OCD0 bits are set to 11b, the system is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated

Table 10.5 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation Stop Detection Clock and Frequency Bandwidth	f(XIN) ≥ 2 MHz
Enabled Condition for Oscillation Stop Detection Function	Set OCD1 to OCD0 bits to 11b
Operation at Oscillation Stop Detection	Oscillation stop detection interrupt is generated

10.5.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares the vector with the voltage monitor 2 interrupt and the watchdog timer interrupt. When using the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt cause needs to be determined.
  Table 10.6 lists the Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, and Voltage Monitor 2 Interrupts.
  Figure 10.15 shows an Example of Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock is re-oscillated after oscillation stop, switch the XIN clock to the clock source of the CPU clock and peripheral functions by a program.
  Figure 10.14 shows the Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock.
- To enter wait mode while using the oscillation stop detection function, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function preparing to stop the XIN clock by the external cause, set the OCD1 to OCD0 bits to 00b when the XIN clock stops or oscillates in the program, that is stop mode is selected or the CM05 bit is changed.
- This function cannot be used when the XIN clock frequency is less than 2 MHz. Set the OCD1 to OCD0 bits to 00b.
- When using the low-speed on-chip oscillator clock for the CPU clock and clock sources of peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and the OCD1 to OCD0 bits to 11b.
  When using the high-speed on-chip oscillator clock for the CPU clock and clock sources of peripheral functions after detecting the oscillation stop, set the FRA00 bit to 1 (high-speed on-chip oscillator on) and the FRA01 bit to 1 (high-speed on-chip oscillator selected) and the OCD1 to OCD0 bits to 11b.

Table 10.6 Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, and Voltage Monitor 2 Interrupts

Generated Interrupt Source	Bit Showing Interrupt Cause
Oscillation Stop Detection ((a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) OCD1 to OCD0 bits in OCD register = 11b and the OCD2 bit = 1
Watchdog Timer	VW2C3 bit in VW2C register = 1
Voltage Monitor 2	VW2C2 bit in VW2C register = 1

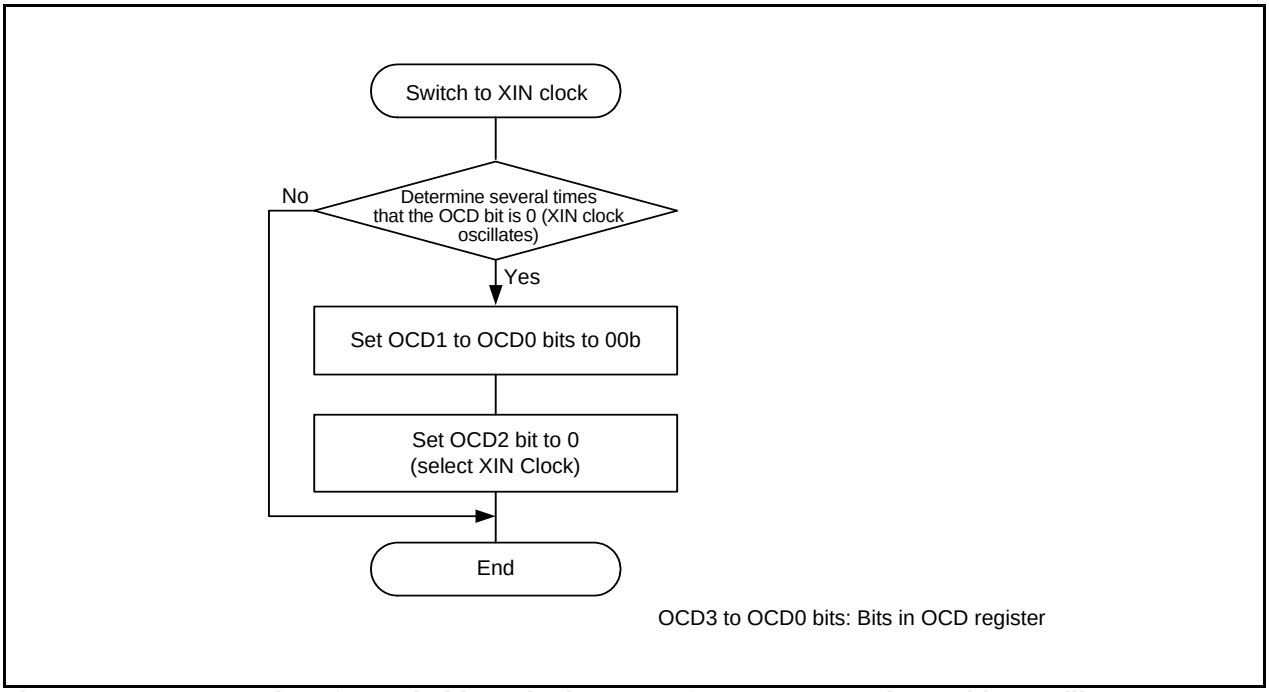


Figure 10.14 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock

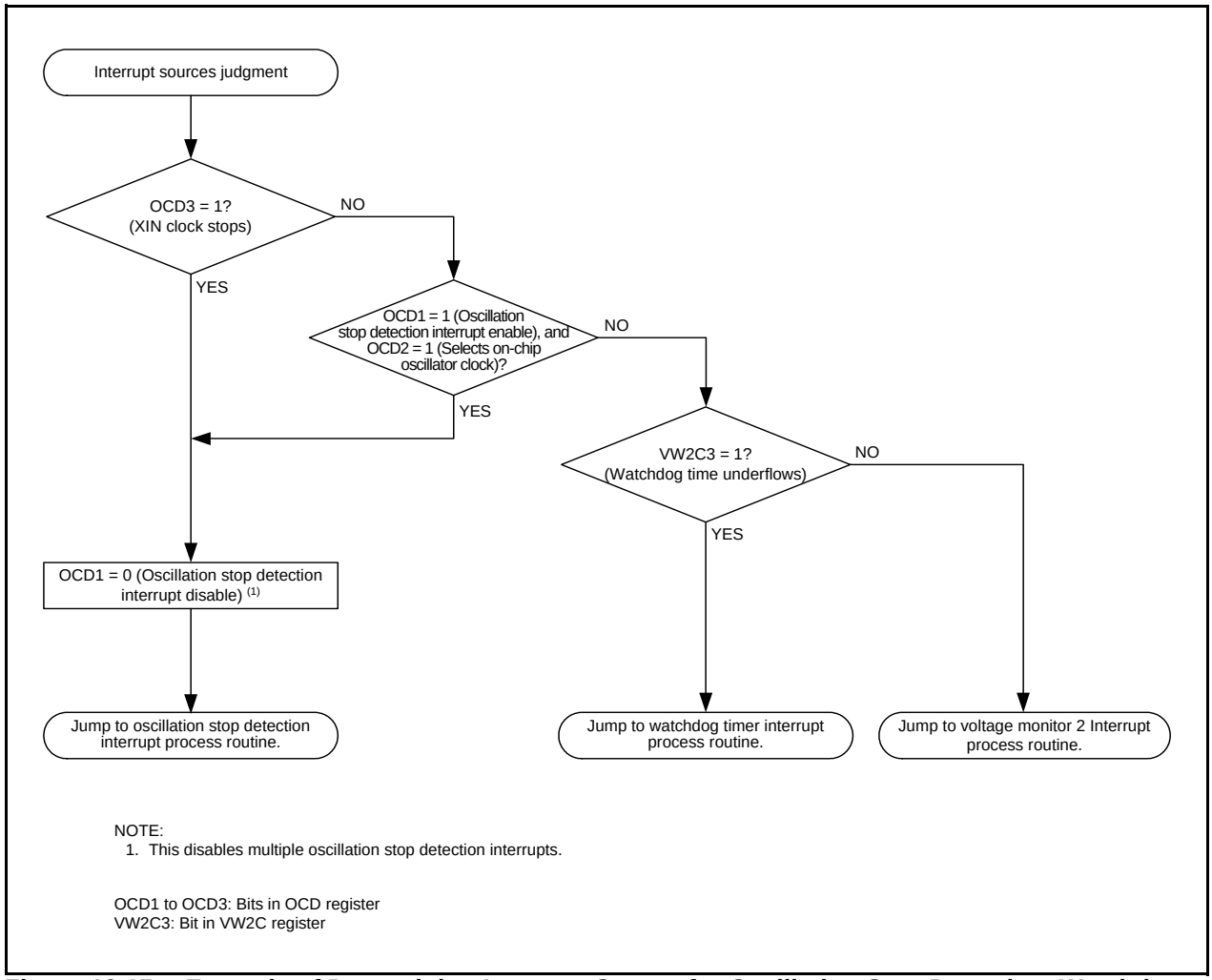


Figure 10.15 Example of Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

10.6 Notes on Clock Generation Circuit

10.6.1 Stop Mode

When entering stop mode, set the FMR01 bit to “0” (CPU rewrite mode disabled) and the CM10 bit to “1” (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit in the CM1 register to “1” (stop mode) and the program stops. Insert at least 4 NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to “1”.

• Example to enter stop mode

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        BSET    0,PRCR          ; Protect disabled
        FSET    I               ; Enable interrupt
        BSET    0,CM1           ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

10.6.2 Wait Mode

When entering wait mode, set the FMR01 bit to “0” (CPU rewrite mode disabled) and execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

• Example to execute the WAIT instruction

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

10.6.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is less than 2 MHz, set the OCD1 to OCD0 bits to 00b.

10.6.4 Oscillation Circuit Constants

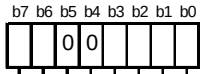
Ask the maker of the oscillator to specify the beat oscillation circuit constants on your system.

11. Protection

Protection function protects important registers from being easily overwritten when a program runs out of control. Figure 11.1 shows the PRCR Register. The following lists the registers protected by the PRCR register.

- Registers protected by PRC0 bit: CM0, CM1, OCD, FRA0, FRA1, FRA2, and CCLKR registers
- Registers protected by PRC1 bit: PM0 and PM1 registers
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: VCA2, VW1C and VW2C registers

Protect Register



Symbol: PRCR | Address: 000Ah | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
PRC0	Protect bit 0	Writing to the CM0, CM, OCD, FRA0, FRA1, FRA2, and CCLKR registers is enabled 0 : Disables writing 1 : Enables writing	RW
PRC1	Protect bit 1	Writing to the PM0 and PM1 registers is enabled 0 : Disables writing 1 : Enables writing	RW
PRC2	Protect bit 2	Writing to the PD0 register is enabled 0 : Disables writing 1 : Enables writing(1)	RW
PRC3	Protect bit 3	Writing to the VCA2, VW1C and VW2C registers is enabled 0 : Disables writing 1 : Enables writing	RW
— (b5-b4)	Reserved bits	Set to 0	RW
— (b7-b6)	Reserved bits	When read, the content is 0.	RO

NOTE:
1. This bit is set to 0 after writing 1 to the PRC2 bit and executing writing to any address. Since the other bits are not set to 0, set to 0 by a program.

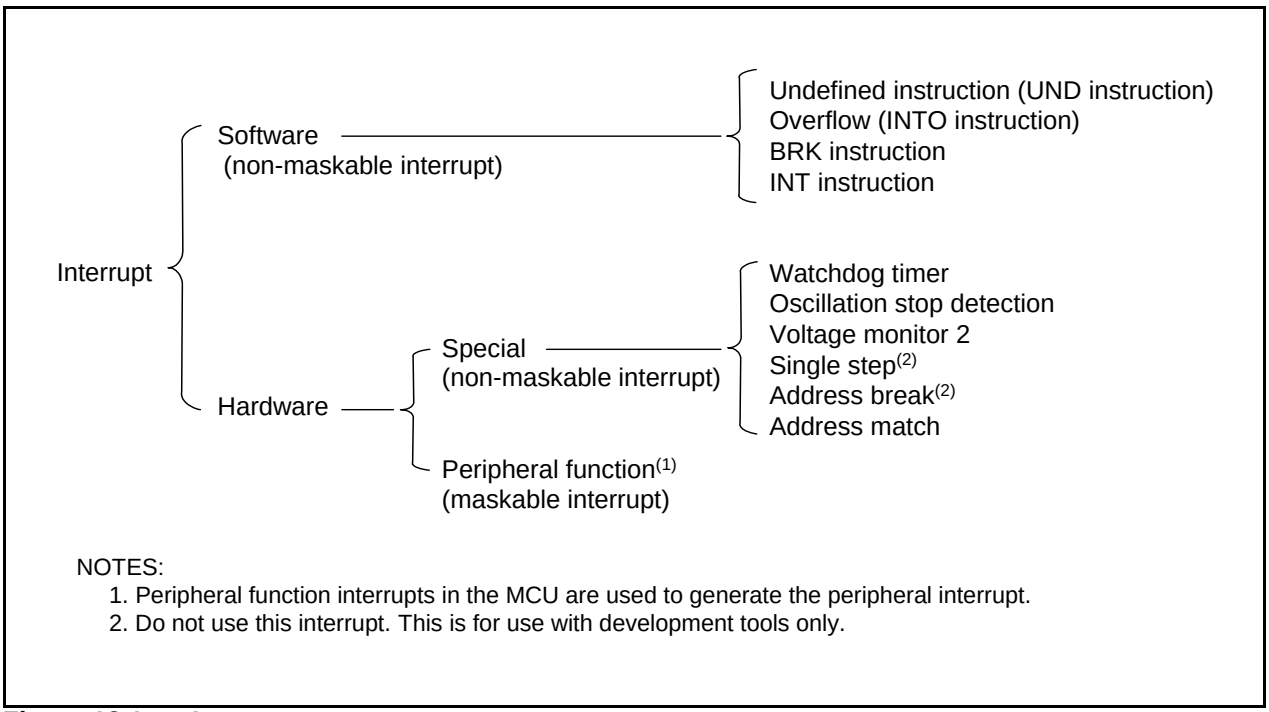
Figure 11.1 PRCR Register

12. Interrupts

12.1 Interrupt Overview

12.1.1 Types of Interrupts

Figure 12.1 shows the Interrupts.



NOTES:
1. Peripheral function interrupts in the MCU are used to generate the peripheral interrupt.
2. Do not use this interrupt. This is for use with development tools only.

Figure 12.1 Interrupts

- Maskable interrupt: The interrupt enable flag (I flag) enables or disables these interrupt. The interrupt priority order can be changed based on the interrupt priority level.
- Non-maskable interrupt: The interrupt enable flag (I flag) does not enable or disable an interrupt. The interrupt priority order based on interrupt priority level cannot be changed.

12.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. The software interrupts are non-maskable interrupts.

12.1.2.1 Undefined Instruction Interrupt

The undefined instruction interrupt is generated when the UND instruction is executed.

12.1.2.2 Overflow Interrupt

The overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions to set the O flag are:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB

12.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

12.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. The INT instruction can select software interrupt numbers 0 to 63. Software interrupt numbers 3 to 31 are assigned to the peripheral function interrupt. Therefore, the MCU executes the same interrupt routine when the INT instruction is executed as when a peripheral function interrupt is generated. In software interrupt numbers 0 to 31, the U flag is saved to the stack during instruction execution and set the U flag to 0 (ISP selected) before executing an interrupt sequence. The U flag is restored from the stack when returning from the interrupt routine. In software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

12.1.3 Special Interrupts

Special interrupts are non-maskable interrupts.

12.1.3.1 Watchdog Timer Interrupt

The watchdog timer interrupt is generated by the watchdog timer. For details, refer to **13. Watchdog Timer**.

12.1.3.2 Oscillation Stop Detection Interrupt

Oscillation Stop Detection Interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **10. Clock Generation Circuit**.

12.1.3.3 Voltage Monitor 2 Interrupt

The voltage monitor 2 interrupt is generated by the voltage detection circuit. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.4 Single-Step Interrupt, and Address Break Interrupt

Do not use the single-step interrupt. For development tools only.

12.1.3.5 Address Match Interrupt

The address match interrupt is generated immediately before executing an instruction that is stored into an address indicated by the RMAD0 to RMAD1 registers when the AIER0 or AIER1 bit in the AIER register which is set to 1 (address match interrupt enable).
For details of the address match interrupt, refer to **12.5 Address Match Interrupt**.

12.1.4 Peripheral Function Interrupt

The peripheral function interrupt is generated by the internal peripheral function of the MCU and a maskable interrupt. Refer to **Table 12.2 Relocatable Vector Tables** for sources of the peripheral function interrupt. For details of the peripheral function, refer to the description of each peripheral function.

12.1.5 Interrupts and Interrupt Vector

There are 4 bytes in one vector. Set the starting address of interrupt routine in each vector table. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows the Interrupt Vector.

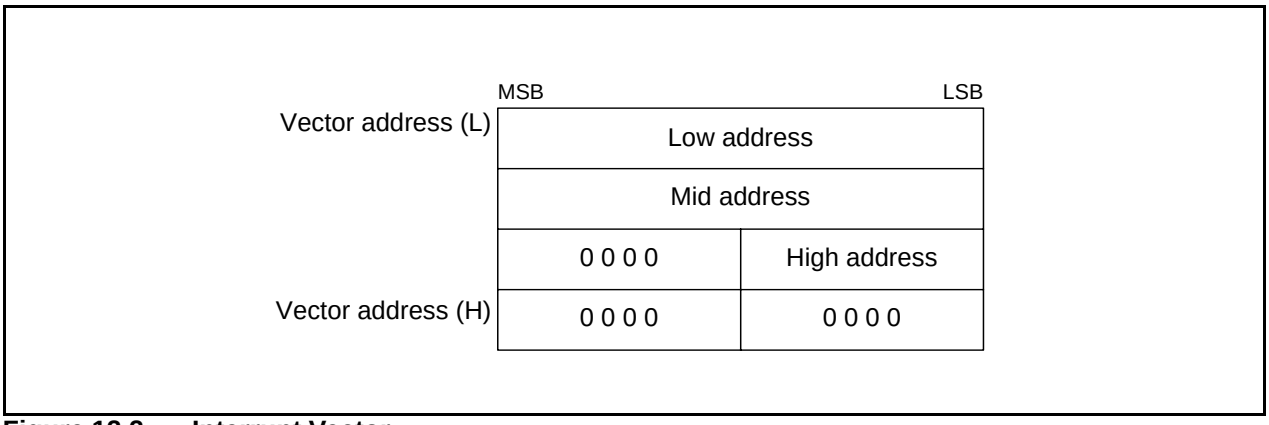


Figure 12.2 Interrupt Vector

12.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 12.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **20.3 Functions to Prevent Rewriting of Flash Memory**.

Table 12.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined Instruction	0FFDCh to 0FFDFh	Interrupt on UND instruction	R8C/Tiny Series software manual
Overflow	0FFE0h to 0FFE3h	Interrupt on INTO instruction	
BRK Instruction	0FFE4h to 0FFE7h	If the content of address 0FFE7h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address Match	0FFE8h to 0FFEBh		12.5 Address Match Interrupt
Single Step(1)	0FFECh to 0FFEFh		
Watchdog Timer Oscillation Stop Detection Voltage Monitor 2	0FFF0h to 0FFF3h		13. Watchdog Timer 10. Clock Generation Circuit 6. Voltage Detection Circuit
Address Break(1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

NOTE:
1. Do not use the single-step interrupt. For development tools only.

12.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes from the starting address set in the INTB register. Table 12.2 lists the Relocatable Vector Tables.

Table 12.2 Relocatable Vector Tables

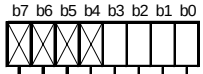
Interrupt Source	Vector Address(1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK Instruction(3)	+0 to +3 (0000h to 0003h)	0	–	R8C/Tiny Series Software Manual
– (Reserved)		1 to 2	–	
CAN0 Wake-up	+12 to +15 (000Ch to 000Fh)	3	C01WKIC	18. CAN Module
CAN0 Successful receive	+16 to +19 (0010h to 0013h)	4	C0RECIC	
CAN0 Successful transmit	+20 to +23 (0014h to 0017h)	5	C0TRMIC	
CAN0 Error	+24 to +27 (0018h to 001Bh)	6	C01ERRIC	
– (Reserved)		7	–	–
Timer RD (Channel 0)	+32 to +35 (0020h to 0023h)	8	TRD0IC	14.3 Timer RD
Timer RD (Channel 1)	+36 to +39 (0024h to 0027h)	9	TRD1IC	
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC	14.4 Timer RE
– (Reserved)		11 to 12	–	–
Key Input	+52 to +55 (0034h to 0037h)	13	KUPIC	12.3 Key Input Interrupt
A/D	+56 to +59 (0038h to 003Bh)	14	ADIC	19. A/D Converter
Clock Synchronous Serial I/O with Chip Select/I^{2}C bus Interface(2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/IICIC	16.2 Clock Synchronous Serial I/O with Chip Select (SSU), 16.3 I^{2}C Bus Interface
– (Reserved)		16	–	–
UART0 Transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	15. Serial Interface
UART0 Receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
UART1 Transmit	+76 to +79 (004Ch to 004Fh)	19	S1TIC	
UART1 Receive	+80 to +83 (0050h to 0053h)	20	S1RIC	
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	12.2 $\overline{\text{INT}}$ Interrupt
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC	14.1 Timer RA
– (Reserved)		23	–	–
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	14.2 Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	12.2 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
– (Reserved)		27	–	–
– (Reserved)		28	–	–
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	12.2 $\overline{\text{INT}}$ Interrupt
– (Reserved)		30	–	–
– (Reserved)		31	–	–
Software Interrupt(3)	+128 to +131 (0080h to 0083h) to +252 to +255 (00FCh to 00FFh)	32 to 63	–	R8C/Tiny Series Software Manual

NOTES:
1. These addresses are relative to those in the INTB register.
2. The IICSEL bit in the PMR register switches functions.
3. The I flag does not disable these interrupts.

12.1.6 Interrupt Control

The following describes enable/disable the maskable interrupts and set the priority order to acknowledge. The contents explained does not apply to the nonmaskable interrupts.
Use the I flag in the FLG register, IPL and the ILVL2 to ILVL0 bits in each interrupt control register to enable/ disable the maskable interrupts. Whether an interrupt is requested is indicated by the IR bit in each interrupt control register.
Figure 12.3 shows the Interrupt Control Register, Figure 12.4 shows Registers TRD0IC, TRD1IC, SSUIC, and IICIC and Figure 12.5 shows the Registers INT0IC to INT3IC.

Interrupt Control Register(2)



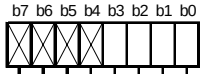
Symbol	Address	After Reset
C01WKIC	0043h	XXXXX000b
C0RECIC	0044h	XXXXX000b
C0TRMIC	0045h	XXXXX000b
C01ERRIC	0046h	XXXXX000b
TREIC	004Ah	XXXXX000b
KUPIC	004Dh	XXXXX000b
ADIC	004Eh	XXXXX000b
S0TIC	0051h	XXXXX000b
S0RIC	0052h	XXXXX000b
S1TIC	0053h	XXXXX000b
S1RIC	0054h	XXXXX000b
TRAIC	0056h	XXXXX000b
TRBIC	0058h	XXXXX000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RW(1)
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.		—

NOTES:
1. Only 0 can be written to the IR bit. Do not write 1.
2. Rewrite the interrupt control register, rewrite it when the interrupt request which is applicable for its register is not generated. Refer to **12.7.5 Changing Interrupt Control Register Contents**.

Figure 12.3 Interrupt Control Register

Interrupt Control Register(1)



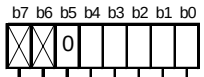
Symbol	Address	After Reset
TRD0IC	0048h	XXXXX000b
TRD1IC	0049h	XXXXX000b
SSUIC/IICIC(2)	004Fh	XXXXX000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RO
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. To rewrite the interrupt control register, rewrite it when the interrupt request which is applicable for its register is not generated. Refer to **12.7.5 Changing Interrupt Control Register Contents**.
2. The IICSEL bit in the PMR register switches functions.

Figure 12.4 Registers TRD0IC, TRD1IC, SSUIC, and IICIC

INTi Interrupt Control Register (i = 0 to 3)(2)



Symbol	Address	After Reset
INT2IC	0055h	XX00X000b
INT1IC	0059h	XX00X000b
INT3IC	005Ah	XX00X000b
INT0IC	005Dh	XX00X000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RW(1)
POL	Polarity switch bit(4)	0 : Selects falling edge 1 : Selects rising edge(3)	RW
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. Only 0 can be written to the IR bit. (Do not write 1.)
2. Rewrite the interrupt control register, rewrite it when the interrupt request which is applicable for its register is not generated. Refer to **12.7.5 Changing Interrupt Control Register Contents**.
3. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (selects falling edge).
4. The IR bit may be set to 1 (requests interrupt) when the POL bit is rewritten. Refer to **12.7.4 Changing Interrupt Sources**.

Figure 12.5 Registers INT0IC to INT3IC

12.1.6.1 I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to 1 (enabled) enables the maskable interrupt. Setting the I flag to 0 (disabled) disables all maskable interrupts.

12.1.6.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (= interrupt not requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
Operations of the IR bit vary by Timer RD interrupt, clock synchronous serial I/O interrupt with chip select or I^2C bus interface interrupt.
For details, refer to **12.6 Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupts and I^2C bus Interface Interrupts (Interrupts with Multiple Interrupt Request Sources)**.

12.1.6.3 Bits ILVL2 to ILVL0 and IPL

Interrupt priority levels can be set using the ILVL2 to ILVL0 bits.
Table 12.3 lists the Settings of Interrupt Priority Levels and Table 12.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are conditions under which an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, ILVL2 to ILVL0 bits and IPL are independent of each other. They do not affect one another.

Table 12.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 Bits	Interrupt Priority Level	Priority Order
000b	Level 0 (interrupt disabled)	–
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	High

Table 12.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Levels
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

12.1.6.4 Interrupt Sequence

An interrupt sequence is performed between an interrupt request acknowledgement and interrupt routine execution.

When an interrupt request is generated while an instruction is executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, in regards to the SMOVB, SMOVF, SSTR or RMPA instruction, if an interrupt request is generated while executing the instruction, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as follows.

Figure 12.6 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU gets interrupt information (interrupt number and interrupt request level) by reading the address 00000h. The IR bit for the corresponding interrupt is set to 0 (interrupt not requested)(2).

(2) The FLG register immediately before entering the interrupt sequence is saved to the CPU internal temporary register(1).

(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (disables interrupts).
The D flag is set to 0 (disables single-step interrupt).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.

(4) The CPU's internal temporary register(1) is saved to the stack.

(5) The PC is saved to the stack.

(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.

(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, the instructions are

NOTES:
1. This register cannot be used by user.

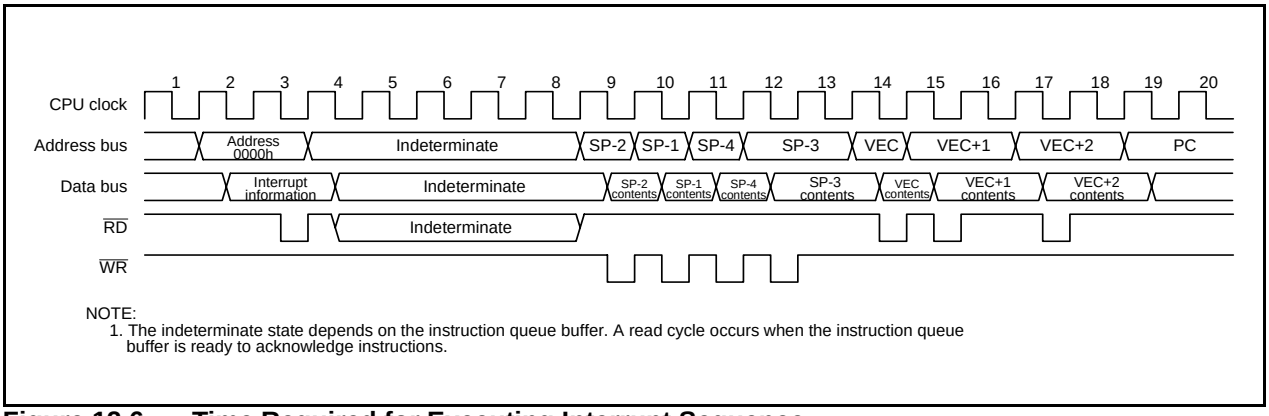
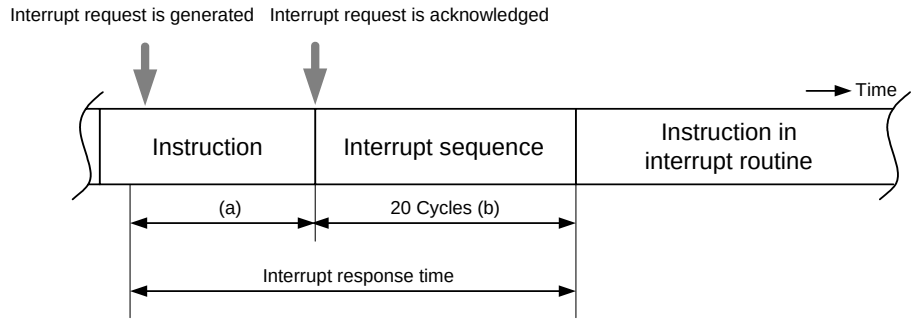


Figure 12.6 Time Required for Executing Interrupt Sequence

2. For operations of the IR bit, refer to **12.6 Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupts and I²C bus Interface Interrupts (Interrupts with Multiple Interrupt Request Sources)**.

12.1.6.5 Interrupt Response Time

Figure 12.7 shows an Interrupt Response Time. The interrupt response time is the period between an interrupt request generation and the execution of the first instruction in an interrupt routine. An interrupt response time includes the period between an interrupt request generation and the completed execution of an instruction (refer to (a) in **Figure 12.7**) and the period required to perform an interrupt sequence (20 cycles, refer to (b) in **Figure 12.7**).



(a) Period between an interrupt request generation and the completed execution of an instruction. The length of this time varies depending on the instruction being executed. The DIVX instruction requires the longest time; 30 cycles (no wait and when the register is set as the divisor)
(b) 21 cycles for address match and single-step interrupts.

Figure 12.7 Interrupt Response Time

12.1.6.6 IPL Change when Interrupt Request is Acknowledged

When an interrupt request of a maskable interrupt is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt and special interrupt request are acknowledged, the level listed in Table 12.5 is set to the IPL.
Table 12.5 lists the IPL Value When Software or Special Interrupt Is Acknowledged.

Table 12.5 IPL Value When Software or Special Interrupt Is Acknowledged

Interrupt Sources	Value Set to IPL
Watchdog Timer, Oscillation Stop Detection, Voltage Monitor 2, Address Break	7
Software, Address Match, Single-Step	Not changed

12.1.6.7 Saving a Register

In the interrupt sequence, the FLG register and PC are saved to the stack.
After 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, extended to 16 bits, are saved to the stack, the 16 low-order bits in the PC are saved.
Figure 12.8 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers are saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used(1) with 1 instruction.

NOTE:
1. Selectable from the R0, R1, R2, R3, A0, A1, SB and FB registers.

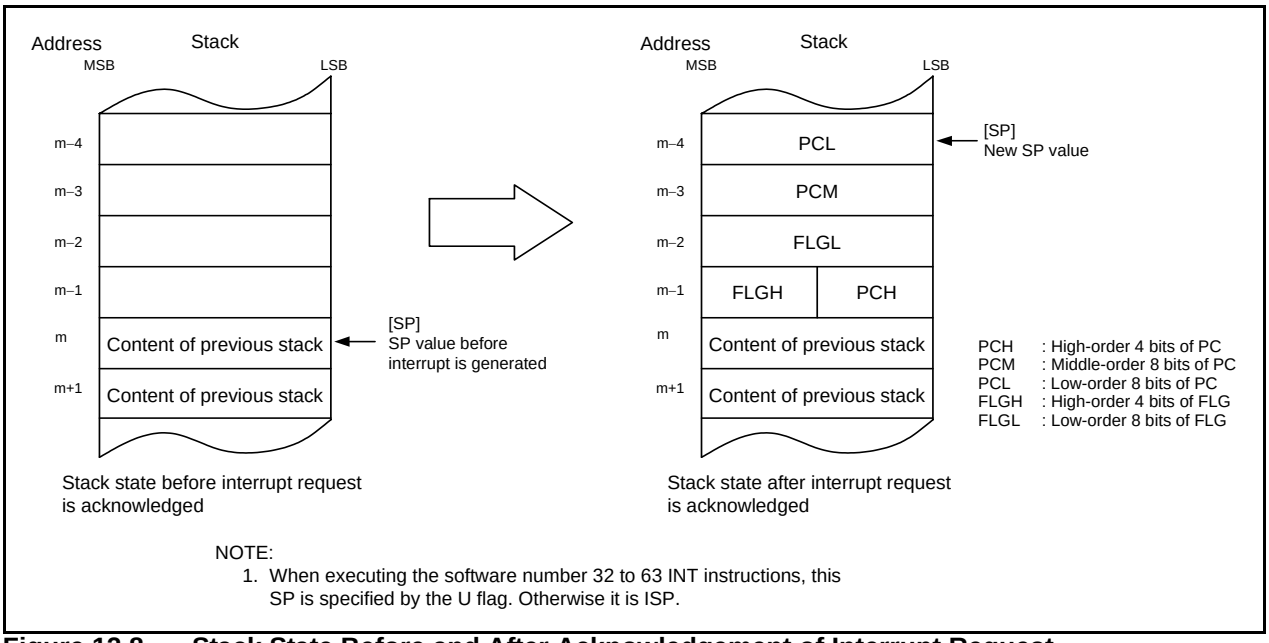


Figure 12.8 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation which is performed in the interrupt sequence is saved in 8 bits every 4 steps.
Figure 12.9 shows the Register Saving Operation.

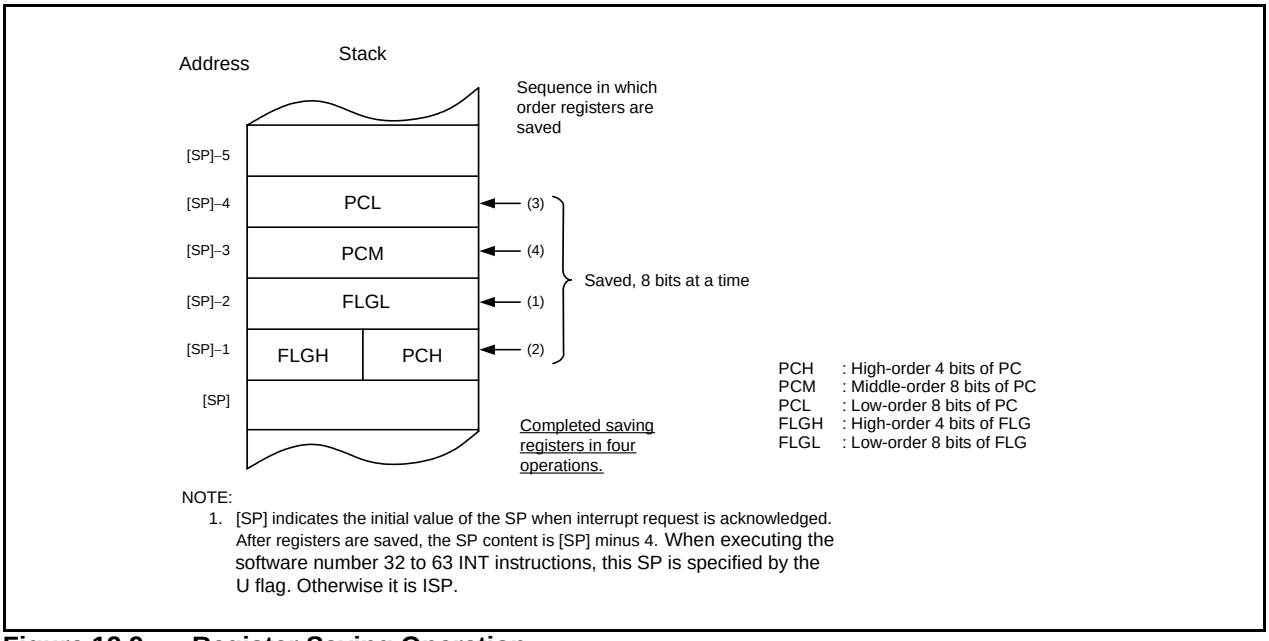


Figure 12.9 Register Saving Operation

12.1.6.8 Returning from an Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved to the stack, are automatically returned. The program, executed before the interrupt request has been acknowledged, starts running again.
Return the register saved by a program in an interrupt routine using the POPM instruction or others before the REIT instruction.

12.1.6.9 Interrupt Priority

If two or more interrupt requests are generated while executing one instruction, the interrupt with the higher priority is acknowledged.
Set the ILVL2 to ILVL0 bits to select the desired priority level for maskable interrupts (peripheral functions). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupt acknowledged in hardware.
The priority levels of special interrupts such as reset (reset has the highest priority) and watchdog timer are set by hardware.
Figure 12.10 shows the Priority Levels of Hardware Interrupts.
The interrupt priority does not affect software interrupts. The MCU jumps to the interrupt routine when the instruction is executed.

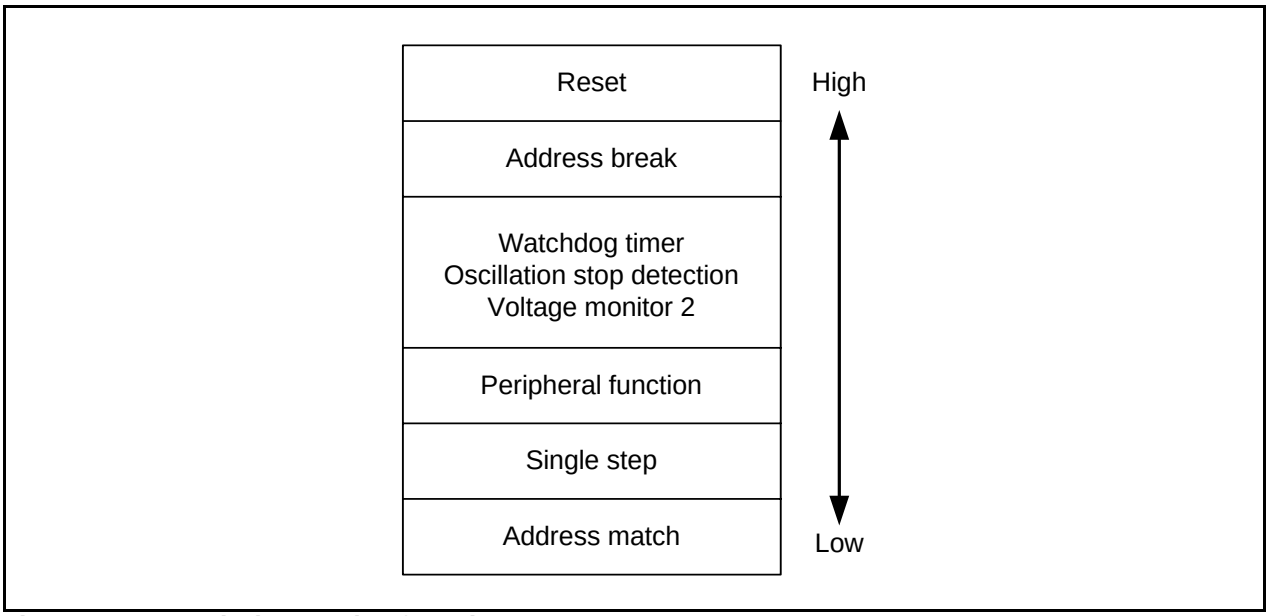


Figure 12.10 Priority Levels of Hardware Interrupts

12.1.6.10 Interrupt Priority Judgement Circuit

The interrupt priority judgement circuit selects the highest priority interrupt.
Figure 12.11 shows the Interrupt Priority Level Judgement Circuit.

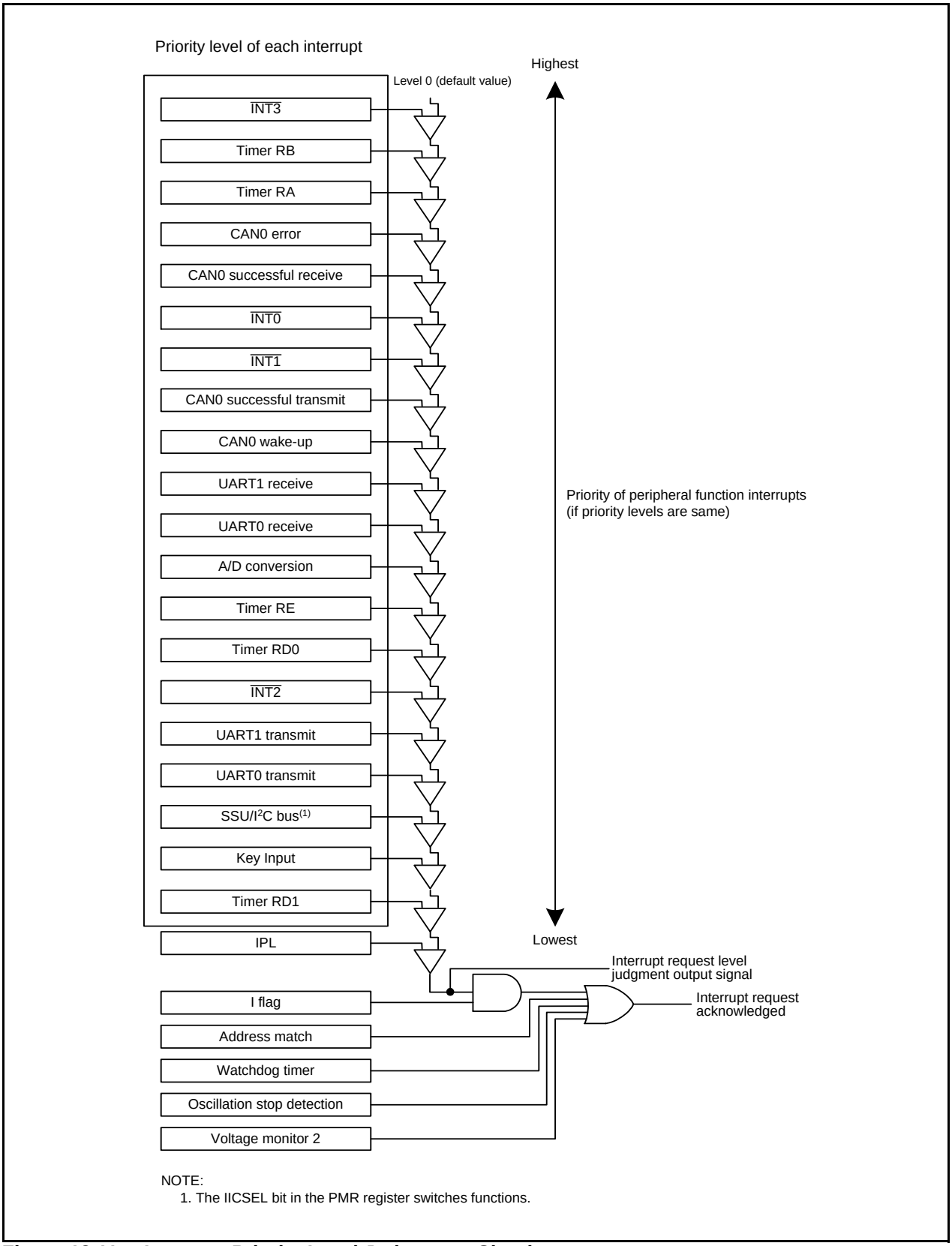


Figure 12.11 Interrupt Priority Level Judgement Circuit

12.2 $\overline{\text{INT}}$ Interrupt

12.2.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. When using the $\overline{\text{INTi}}$ interrupt, the INTiEN bit in the INTEN register is set to 1 (enable). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.
Inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff of timer RD and shared with the external trigger input of timer RB.
Figure 12.12 shows the INTEN Register. Figure 12.13 shows the INTF Register.

External Input Enable Register

b7 b6 b5 b4 b3 b2 b1 b0

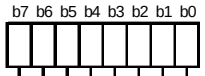
Symbol	Address	After Reset
INTEN	00F9h	00h

Bit Symbol	Bit Name	Function	RW
INT0EN	$\overline{\text{INT0}}$ input enable bit	0 : Disable 1 : Enable	RW
INT0PL	$\overline{\text{INT0}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW
INT1EN	$\overline{\text{INT1}}$ input enable bit	0 : Disable 1 : Enable	RW
INT1PL	$\overline{\text{INT1}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW
INT2EN	$\overline{\text{INT2}}$ input enable bit	0 : Disable 1 : Enable	RW
INT2PL	$\overline{\text{INT2}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW
INT3EN	$\overline{\text{INT3}}$ input enable bit	0 : Disable 1 : Enable	RW
INT3PL	$\overline{\text{INT3}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW

NOTES:
1. When setting the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (selects falling edge).
2. The IR bit in the INTiIC register may be set to 1 (requests interrupt) when the INTiPL bit is rewritten. Refer to **12.7.4 Changing Interrupt Sources**.

Figure 12.12 INTEN Register

$\overline{\text{INT}}$ Input Filter Select Register



Symbol	Address	After Reset
INTF	00FAh	00h

Bit Symbol	Bit Name	Function	RW
INT0F0	$\overline{\text{INT0}}$ input filter select bits	b1 b0 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT0F1			RW
INT1F0	$\overline{\text{INT1}}$ input filter select bits	b3 b2 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT1F1			RW
INT2F0	$\overline{\text{INT2}}$ input filter select bits	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT2F1			RW
INT3F0	$\overline{\text{INT3}}$ input filter select bits	b7 b6 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT3F1			RW

Figure 12.13 INTF Register

12.2.2 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected by the INTiF1 to INTiF0 bits in the INTF register. The IR bit in the INTiIC register is set to 1 (interrupt requested) when the $\overline{\text{INTi}}$ level is sampled for every sampling clock and the sampled input level matches three times.
Figure 12.14 shows the Configuration of $\overline{\text{INTi}}$ Input Filter. Figure 12.15 shows Operating Example of $\overline{\text{INTi}}$ Input Filter.

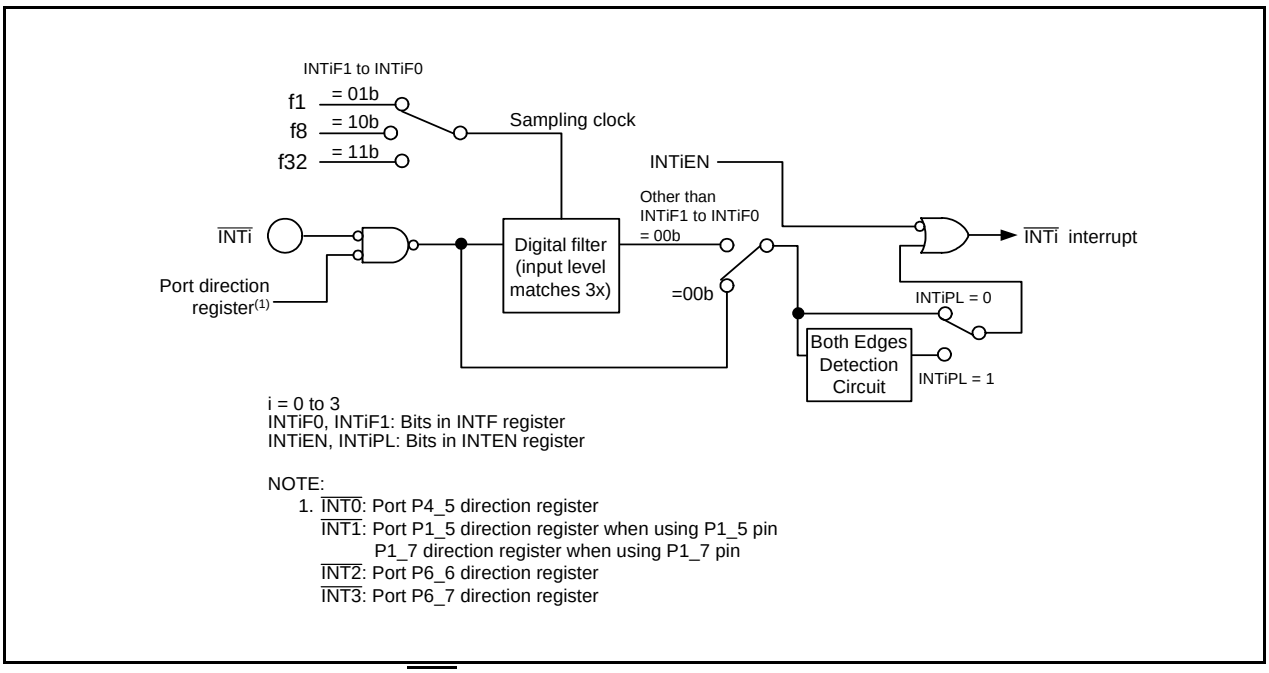


Figure 12.14 Configuration of $\overline{\text{INTi}}$ Input Filter

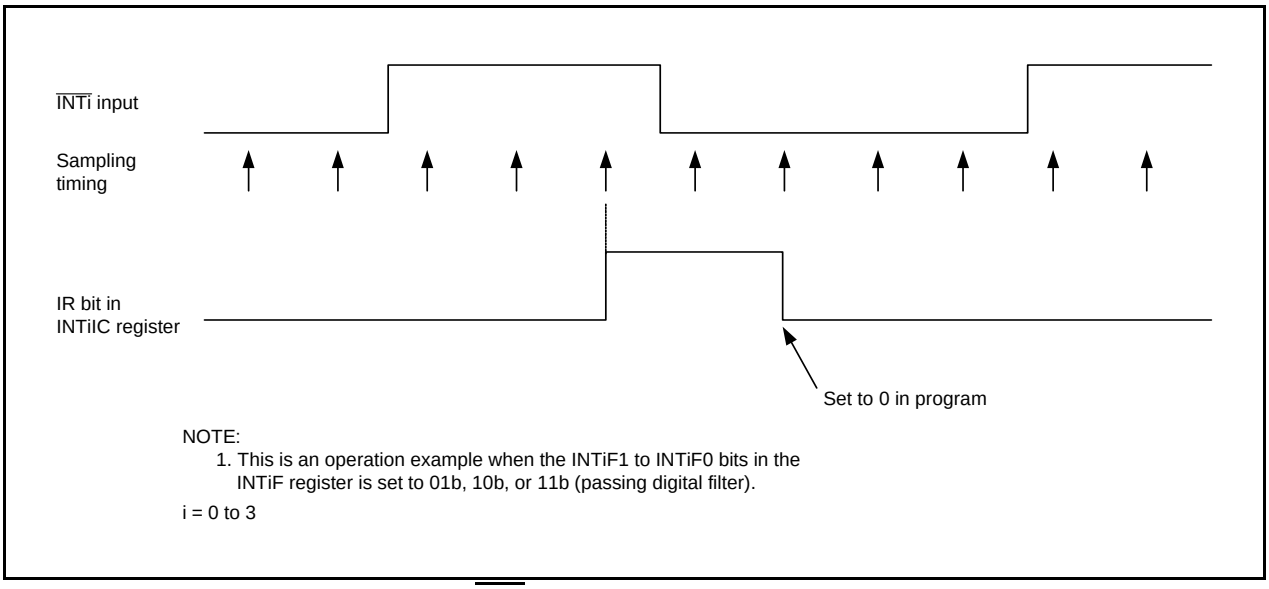


Figure 12.15 Operating Example of $\overline{\text{INTi}}$ Input Filter

12.3 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of the $\overline{K10}$ to $\overline{K13}$ pins. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN (i = 0 to 3) bit in the KIEN register can select whether the pins are used as $\overline{KIi}$ input. The KIiPL bit in the KIEN register can select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin which sets the KIiPL bit to 0 (falling edge), the input of the other $\overline{K10}$ to $\overline{K13}$ pins are not detected as interrupts. Also, when inputting "H" to the $\overline{KIi}$ pin which sets the KIiPL bit to 1 (rising edge), the input of the other $\overline{K10}$ to $\overline{K13}$ pins are not detected as interrupts.

Figure 12.16 shows a Block Diagram of Key Input Interrupt.

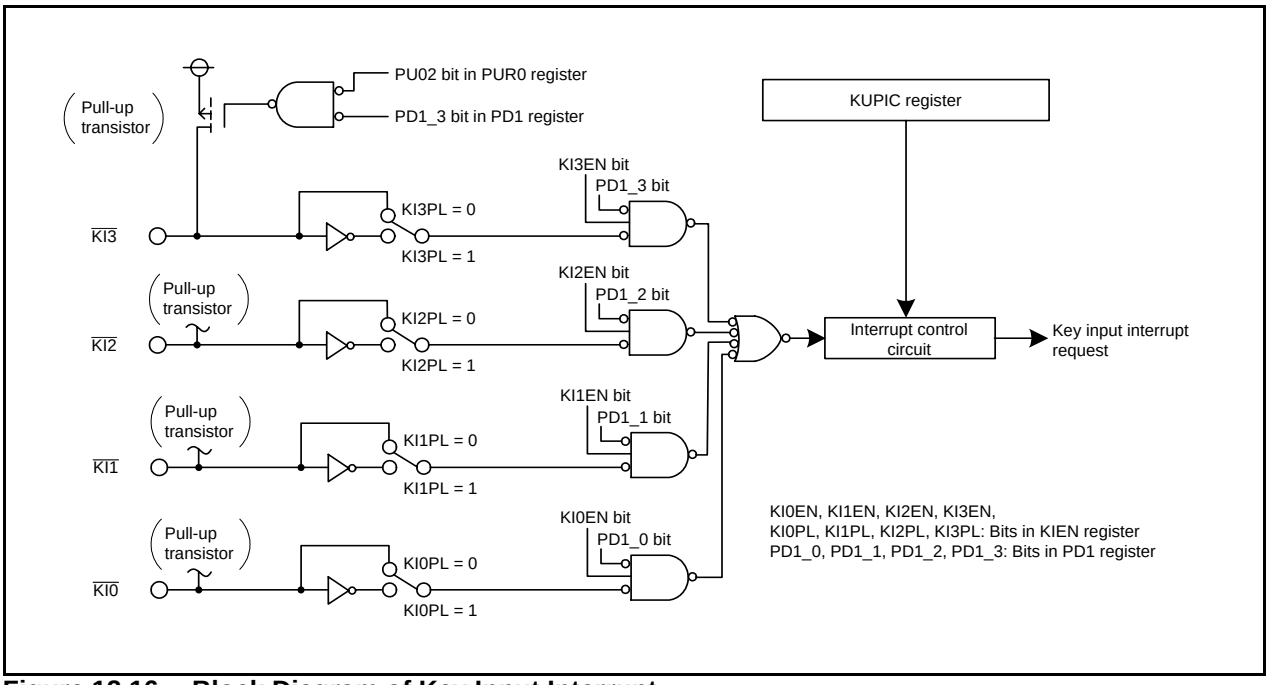
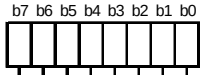


Figure 12.16 Block Diagram of Key Input Interrupt

Key Input Enable Register(1)



Symbol	Address	After Reset
KIEN	00FBh	00h

Bit Symbol	Bit Name	Function	RW
KI0EN	KI0 input enable bit	0 : Disable 1 : Enable	RW
KI0PL	KI0 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI1EN	KI1 input enable bit	0 : Disable 1 : Enable	RW
KI1PL	KI1 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI2EN	KI2 input enable bit	0 : Disable 1 : Enable	RW
KI2PL	KI2 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI3EN	KI3 input enable bit	0 : Disable 1 : Enable	RW
KI3PL	KI3 input polarity select bit	0 : Falling edge 1 : Rising edge	RW

NOTE:
1. The IR bit in the KUPIC register may be set to 1 (requests interrupt) when the KIEN register is rewritten. Refer to **12.7.4 Changing Interrupt Sources**.

Figure 12.17 KIEN Register

12.4 CAN0 Wake-Up Interrupt

A CAN0 wake-up interrupt request is generated by a falling edge of the CRX pin. The CAN0 wake-up interrupt is enabled when the PortEn bit is 1 (CTX/CRX function) and Sleep bit is 1 (Sleep mode enabled) in the C0CTLR register.

Figure 12.18 shows the Block Diagram of CAN0 Wake-Up Interrupt.

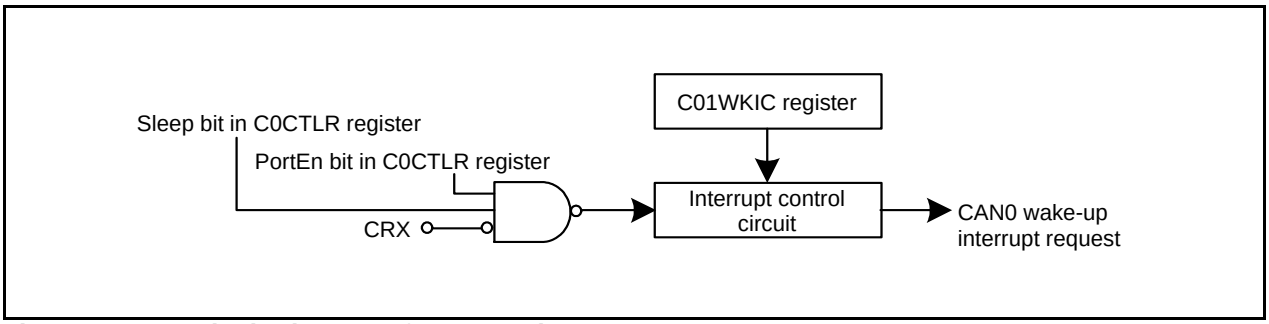


Figure 12.18 Block Diagram of CAN0 Wake-Up Interrupt

12.5 Address Match Interrupt

An address match interrupt request is generated immediately before executing the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used for a break function of the debugger. When using the on-chip debugger, do not set an address match interrupt (the AIER, RMAD0 to RMAD1 registers, and relocatable vector tables) in a user system.

Set the starting address of any instruction in the RMADi register. The AIER0 and AIER1 bits in the AIER0 register can select to enable or disable the interrupt. The I flag and IPL do not affect the address match interrupt. The value of the PC (refer to **12.1.6.7 Saving a Register** for the value of the PC) which is saved to the stack when an address match interrupt is acknowledged varies depending on the instruction at the address indicated by the RMADi register (the appropriate return address is not pushed on the stack). When returning from the address match interrupt, return by one of the following:

- Change the content of the stack and use the REIT instruction.
- Use an instruction such as POP to restore the stack as it was before an interrupt request was acknowledged. And then use a jump instruction.

Table 12.6 lists the Value of PC Saved to Stack when Address Match Interrupt is Acknowledged. Figure 12.19 shows the Registers AIER and RMAD0 to RMAD1.

Table 12.6 Value of PC Saved to Stack when Address Match Interrupt is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved(1)
• Instruction with 2-byte operation code(2) • Instruction with 1-byte operation code(2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (However, dest = A0 or A1)	Address indicated by RMADi register + 2
Instructions other than the above	Address indicated by RMADi register + 1

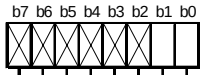
NOTES:

1. Refer to the **12.1.6.7 Saving a Register** for the PC value saved.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual (REJ09B0001)**. **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 12.7 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address Match Interrupt 0	AIER0	RMAD0
Address Match Interrupt 1	AIER1	RMAD1

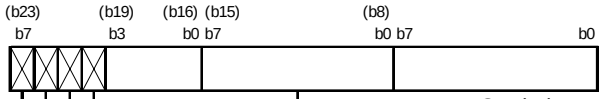
Address Match Interrupt Enable Register



Symbol	Address	After Reset
AIER	0013h	00h

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Disable 1 : Enable	RW
AIER1	Address match interrupt 1 enable bit	0 : Disable 1 : Enable	RW
— (b7-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Address Match Interrupt Register i (i = 0 or 1)



Symbol	Address	After Reset
RMAD0	0012h-0010h	000000h
RMAD1	0016h-0014h	000000h

Function	Setting Range	RW
Address setting register for address match interrupt	00000h to FFFFFh	RW

— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—

Figure 12.19 Registers AIER and RMAD0 to RMAD1

12.6 Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupts and I²C bus Interface Interrupts (Interrupts with Multiple Interrupt Request Sources)

Timer RD (channel 0), timer RD (channel 1), clock synchronous serial I/O with chip select and I²C bus interface have several interrupt request sources and an interrupt request is generated by the logical OR of several interrupt request sources and the logical OR is reflected in the IR bit in the interrupt control register. Therefore, these peripheral functions which have the status register of its own interrupt request sources (status register) and the enable register of the interrupt request sources (enable register) control the generations of the interrupt request (change of the IR bit in the interrupt control register). Table 12.8 lists the Registers Associated with Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupt, and I²C bus Interface Interrupt and Figure 12.20 shows the Block Diagram of Timer RD Interrupt.

Table 12.8 Registers Associated with Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupt, and I²C bus Interface Interrupt

		Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RD	Channel 0	TRDSR0	TRDIER0	TRD0IC
	Channel 1	TRDSR1	TRDIER1	TRD1IC
Clock Synchronous Serial I/O with Chip Select		SSSR	SSER	SSUIC
I²C Bus Interface		ICSR	ICIER	IICIC

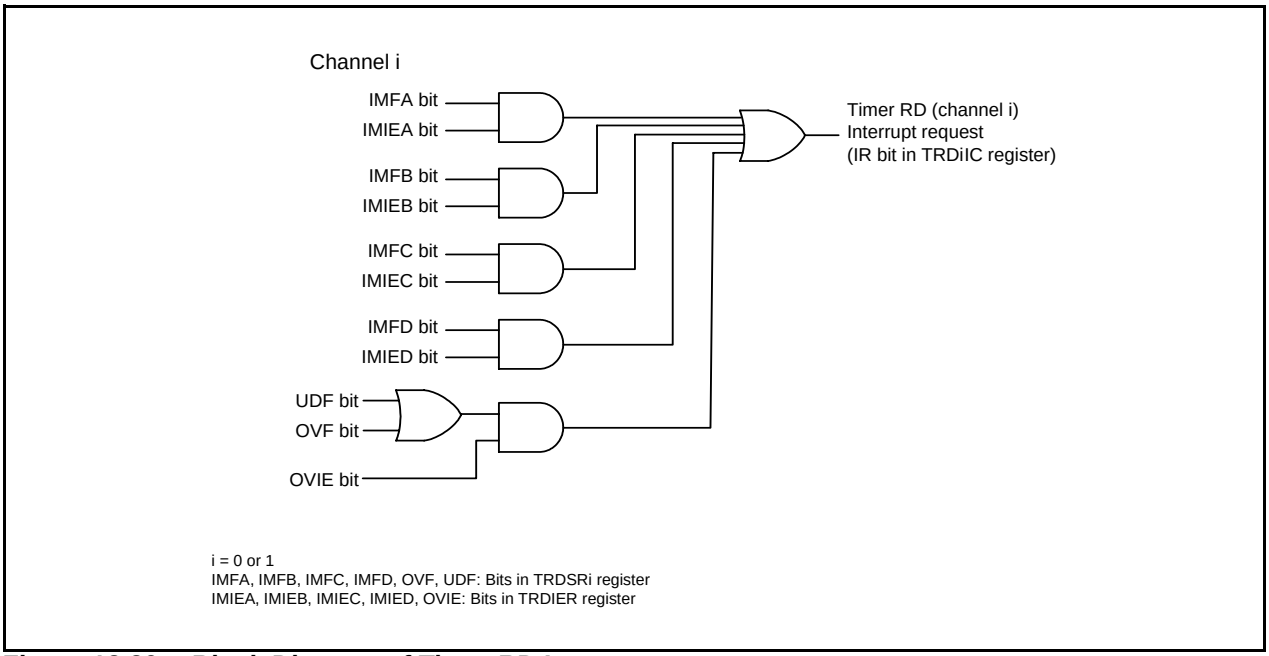


Figure 12.20 Block Diagram of Timer RD Interrupt

Controlling an interrupt with the I flag, IR bit, ILVL0 to ILVL2 bits and IPL by Timer RD (channel 0), Timer RD (channel 1), clock synchronous serial I/O with chip select and I^2C bus interface is the same as that by other maskable interrupts. However, since an interrupt source is generated based on multiple interrupt request sources, there are the following differences from other maskable interrupts:

- When bits in the enable register corresponding to set bits in the status register to 1 are set to 1 (enable interrupt), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or bits in the enable register corresponding to bits in the status register, or both of them are set to 0, the IR bit is set to 0 (interrupt not requested). Basically, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained. Also, the IR bit is not set to 0 although 0 is written to the IR bit.
- Since each bit in the status register is not automatically set to 0 even if the interrupt is acknowledged. Therefore, the IR bit is not also automatically set to 0 when the interrupt is acknowledged. Set each bit in the status register to 0 in the interrupt routine. Refer to the status register figure how to set each bit in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, determine by the status register which request source causes an interrupt.

Refer to chapters of each peripheral function (**14.3 Timer RD**, **16.2 Clock Synchronous Serial I/O with Chip Select (SSU)** and **16.3 I^2C Bus Interface**) for the status register and enable register.
Refer to **12.1.6 Interrupt Control** for the interrupt control register.

12.7 Notes on Interrupts

12.7.1 Reading Address 00000h

Do not read the address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to 0.
If the address 00000h is read in a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause a problem that the interrupt is canceled, or an unexpected interrupt is generated.

12.7.2 SP Setting

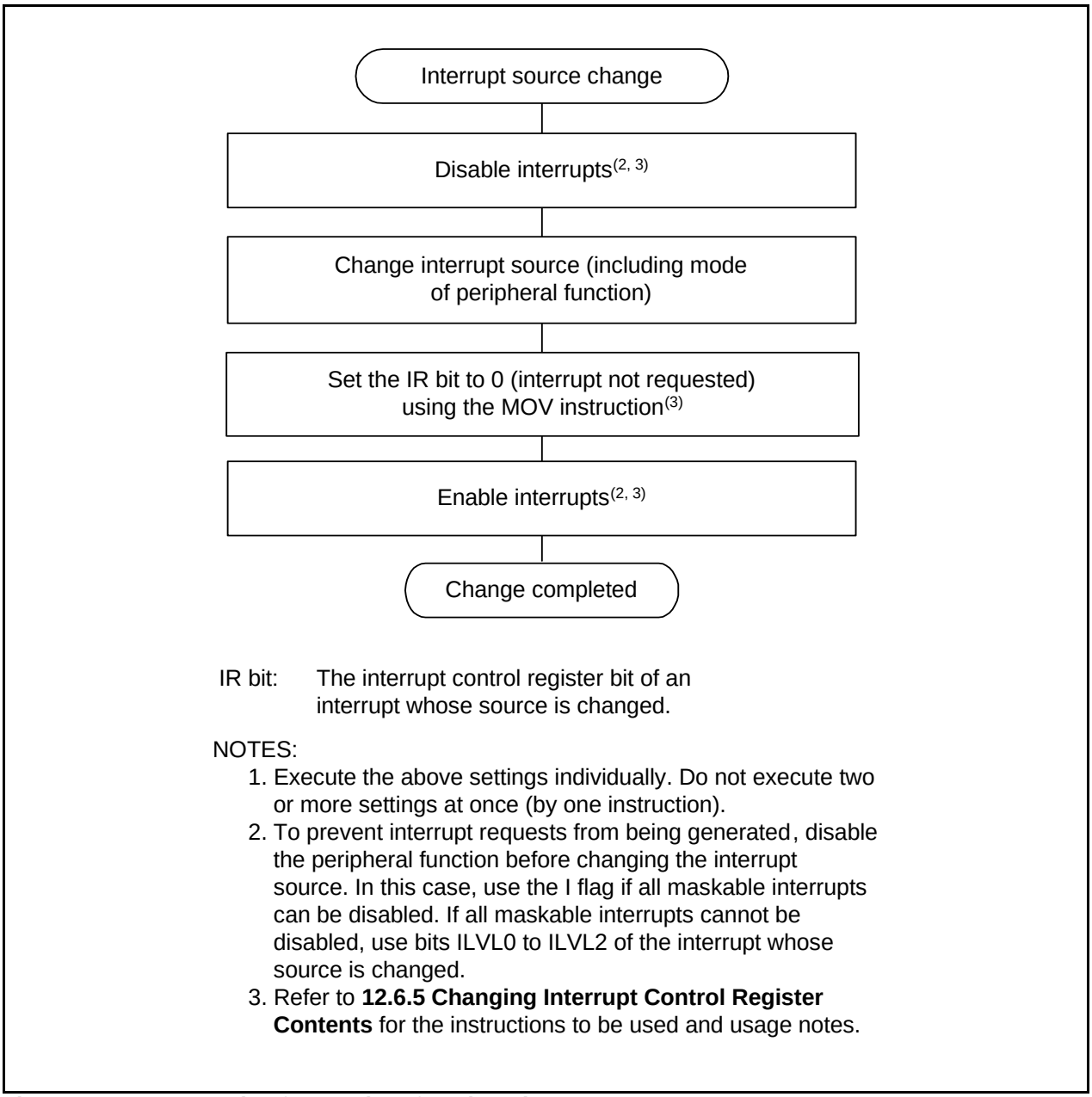
Set any value in the SP before an interrupt is acknowledged. The SP is set to 0000h after reset. Therefore, if an interrupt is acknowledged before setting any value in the SP, the program may run out of control.

12.7.3 External Interrupt and Key Input Interrupt

Either an “L” level or an “H” level of width shown in the Electrical Characteristics is necessary for the signal input to the $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ pins and $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ pins regardless of the CPU clocks. For details, refer to **Table 21.19 External Interrupt INTi (i = 0 to 3) Input**, **Table 21.25 External Interrupt INTi (i = 0 to 3) Input**.

12.7.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. When using an interrupt, set the IR bit to 0 (no interrupt requested) after changing the interrupt source. In addition, the changes of interrupt sources include all sources that change the interrupt sources assigned to individual software interrupt numbers, polarities, and timing. Therefore, when a mode change of the peripheral functions involves interrupt sources, edge polarities, and timing, Set the IR bit to 0 (no interrupt requested) after the change. Refer to each peripheral function for the interrupts caused by the peripheral functions.
Figure 12.21 shows an Example of Procedure for Changing Interrupt Sources.



IR bit: The interrupt control register bit of an interrupt whose source is changed.

NOTES:
1. Execute the above settings individually. Do not execute two or more settings at once (by one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled. If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 of the interrupt whose source is changed.
3. Refer to **12.6.5 Changing Interrupt Control Register Contents** for the instructions to be used and usage notes.

Figure 12.21 Example of Procedure for Changing Interrupt Sources

12.7.5 Changing Interrupt Control Register Contents

(a) Each interrupt control register can only be changed while interrupt requests corresponding to that register are not generated. If interrupt requests may be generated, disable the interrupts before changing the interrupt control register.

(b) When changing any interrupt control register after disabling interrupts, be careful with the instructions to be used.
When changing any bit other than IR bit
If an interrupt request corresponding to that register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register.
Instructions to use: AND, OR, BCLR, BSET
When changing IR bit
If the IR bit is set to 0 (interrupt not requested), it may not be set to 0 depending on the instruction to be used. Therefore, use the MOV instruction to set the IR bit to 0.

(c) When disabling interrupts using the I flag, set the I flag according to the following sample programs. Refer to (b) for the change of interrupt control registers in the sample programs.

Sample programs 1 to 3 are preventing the I flag from being set to 1 (interrupt enables) before changing the interrupt control register for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag being set to 1 before interrupt control register is changed

```
INT_SWITCH1:
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set TRAIC register to 00h
    NOP                 ;
    NOP
    FSET    I           ; Enable interrupts
```

Example 2: Use dummy read to have FSET instruction wait

```
INT_SWITCH2:
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set TRAIC register to 00h
    MOV.W   MEM,R0      ; Dummy read
    FSET    I           ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

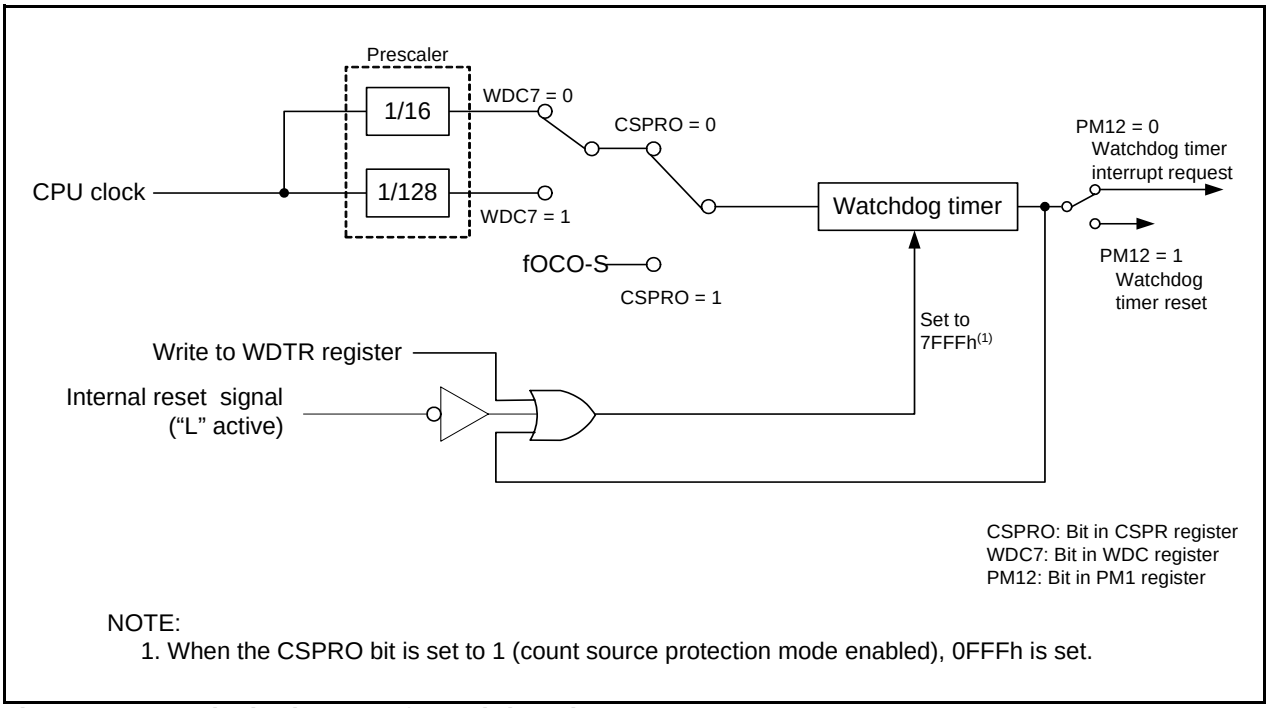
```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set TRAIC register to 00h
    POPC    FLG         ; Enable interrupts
```

13. Watchdog Timer

The watchdog timer is a function to detect when the program is out of control. To use the watchdog timer is recommend for improving reliability of a system. The watchdog timer contains a 15-bit counter and can select count source protection mode is enabled or disabled.
Table 13.1 lists the Count Source Protection Mode
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 13.1 shows the Block Diagram of Watchdog Timer, Figure 13.2 shows Registers OFS and WDC and Figure 13.3 shows Registers WDTR, WDTS, and CSPR.

Table 13.1 Count Source Protection Mode

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count Source	CPU clock	Low-speed on-chip oscillator clock
Count Operation	Decrement	
Count Start Condition	Either of following can be selected • After reset, count starts automatically • Count starts by writing to WDTS register	
Count Stop Condition	Stop mode, wait mode	None
Reset Condition of Watchdog Timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow	
Operation at the Time of Underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset



NOTE:
1. When the CSPRO bit is set to 1 (count source protection mode enabled), 0FFFh is set.

Figure 13.1 Block Diagram of Watchdog Timer

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
		1	1			1	

Symbol	Address	Before Shipment
OFS	0FFFFh	FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b5-b4)	Reserved bits	Set to 1	RW
LVD1ON	Voltage detection circuit start bit(2)	0 : Voltage monitor 1 reset enabled after reset 1 : Voltage monitor 1 reset disabled after reset	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. To use the power-on reset, set the LVD1ON bit to 0 (voltage monitor 1 reset enabled after reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Watchdog Timer Control Register

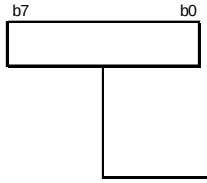
b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol	Address	After Reset
WDC	000Fh	00X11111b

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	High-order bits of watchdog timer		RO
— (b5)	Reserved bits	Set to 0. When read, the content is undefined.	RW
— (b6)	Reserved bits	Set to 0	RW
WDC7	Prescaler select bit	0 : Divide-by-16 1 : Divide-by-128	RW

Figure 13.2 Registers OFS and WDC

Watchdog Timer Reset Register

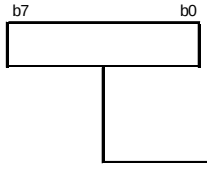


Symbol	Address	After Reset
WDTR	000Dh	Indeterminate

Function	RW
When writing 00h before writing FFh, the watchdog timer is reset.(1) The default value of the watchdog timer is set to 7FFFh when count source protection mode is disabled and 0FFFh when count source protection mode is enabled.(2)	WO

NOTES:
1. Do not generate an interrupt between 00h and the FFh writings.
2. When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), 0FFFh is set to the watchdog timer.

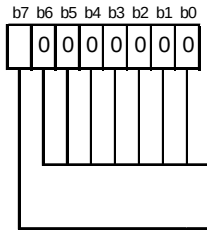
Watchdog Timer Start Register



Symbol	Address	After Reset
WDTS	000Eh	Indeterminate

Function	RW
The watchdog timer starts counting after a write instruction to this register.	WO

Count Source Protection Mode Register



Symbol	Address	After Reset(1)
CSPR	001Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0	RW
CSPRO	Count source protection mode select bit(2)	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

NOTES:
1. When writing 0 to the CSPROINI bit in the OFS register, the value after reset is set to 10000000b.
2. Write 0 before writing 1 to set the CSPRO bit to 1. 0 cannot be set by a program.

Figure 13.3 Registers WDTR, WDTS, and CSPR

13.1 Count Source Protection Mode Disabled

The count source of the watchdog timer is the CPU clock when count source protection mode is disabled. Table 13.2 lists the Watchdog Timer Specifications (with Count Source Protection Mode Disabled).

Table 13.2 Watchdog Timer Specifications (with Count Source Protection Mode Disabled)

Item	Specification
Count Source	CPU clock
Count Operation	Decrement
Period	$\frac{\text{Division ratio of prescaler(n) x count value of watchdog timer(32768)}^{(1)}}{\text{CPU clock}}$ n: 16 or 128 (selected by WDC7 bit in WDC register) e.g.When the CPU clock is 16 MHz and prescaler is divided by 16, the period is approximately 32.8 ms
Count Start Condition	The WDTON bit(2) in the OFS register (0FFFFh) selects the operation of watchdog timer after reset • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after reset and the count starts by writing to the WDTS register • When the WDTON bit is set to 0 (watchdog timer starts automatically after exiting) The watchdog timer and prescaler start counting automatically after reset
Reset Condition of Watchdog Timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow
Count Stop Condition	Stop and wait modes (inherit the count from the held value after exiting modes)
Operation at the Time of Underflow	• When the PM12 bit in the PM1 register is set to 0 Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1 Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

NOTES:
1. The watchdog timer is reset when writing 00h to the WDTR register before writing FFh. The prescaler is reset after the MCU is reset. Some errors occur by the prescaler for the period of the watchdog timer.
2. The WDTON bit cannot be changed by a program. When setting the WDTON bit, write 0 to the bit 0 of the address 0FFFFh using a flash programmer.

13.2 Count Source Protection Mode Enabled

The count source of the watchdog timer is the low-speed on-chip oscillator clock when count source protection mode is enabled. If the CPU clock stops when the program is out of control, the clock can be supplied to the watchdog timer.
Table 13.3 lists the Watchdog Timer Specifications (with Count Source Protection Mode Enabled).

Table 13.3 Watchdog Timer Specifications (with Count Source Protection Mode Enabled)

Item	Specification
Count Source	Low-speed on-chip oscillator clock
Count Operation	Decrement
Period	Count value of watchdog timer (4096) Low-speed on-chip oscillator clock e.g. Period is approximately 32.8 ms when the low-speed on-chip oscillator clock is 125 kHz
Count Start Condition	The WDTON bit(1) in the OFS register (0FFFFh) selects the operation of the watchdog timer after reset. • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after reset and the count starts by writing to the WDTS register • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after reset
Reset Condition of Watchdog Timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow
Count Stop Condition	None (the count does not stop in wait mode after the count starts. The MCU does not enter stop mode)
Operation at the Time of Underflow	Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)
Register, Bit	• When setting the CSPPRO bit in the CSPR register to 1 (count source protection mode is enabled)(2), the following are set automatically - Set 0FFFh to the watchdog timer - Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on) - Set the PM12 bit in the PM1 register to 1 (The watchdog timer is reset when watchdog timer underflows) • The following states are held in count source protection mode - Writing to the CM10 bit in the CM1 register disables (It remains unchanged even if it is set to 1. The MCU does not enter stop mode) - Writing to the CM14 bit in the CM1 register disables (It remains unchanged even if it is set to 1. The low-speed on-chip oscillator does not stop)

NOTES:
1. The WDTON bit cannot be changed by a program. When setting the WDTON bit, write 0 to the bit 0 of the address 0FFFFh using a flash programmer.
2. Even if writing 0 to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. When setting the CSPROINI bit, write 0 to the bit 7 of the address 0FFFFh using a flash programmer.

14. Timers

The MCU contains two 8-bit timers with 8-bit prescaler, two 16-bit timers, and a timer with a 4-bit counter, and an 8-bit counter. The two 8-bit timers with the 8-bit prescaler contain timer RA and timer RB. These timers contain a reload register to memorize the default value of the counter. The 16-bit timer is timer RD which contains the input capture and output compare. The 4 and 8-bit counters are timer RE which contains the output compare. All these timers operate independently.
Table 14.1 lists Functional Comparison of Timers.

Table 14.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RD	Timer RE
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit free-run timer X 2 (with input capture and output compare)	4-bit counter 8-bit counter
Count		Decrement	Decrement	Increment / Decrement	Increment
Count Sources		• f1 • f2 • f8 • fOCO	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • TRDIOA0	• f4 • f8 • f32
Function	Timer mode	provided	provided	provided (input capture function, output compare function)	not provided
	Pulse output mode	provided	not provided	not provided	not provided
	Event counter mode	provided	not provided	not provided	not provided
	Pulse width measurement mode	provided	not provided	not provided	not provided
	Pulse period measurement mode	provided	not provided	not provided	not provided
	Programmable waveform generation mode	not provided	provided	not provided	not provided
	Programmable one-shot generation mode	not provided	provided	not provided	not provided
	Programmable wait one-shot generation mode	not provided	provided	not provided	not provided
	Input capture mode	not provided	not provided	provided	not provided
	Output compare mode	not provided	not provided	provided	provided
	PWM mode	not provided	not provided	provided	not provided
	Reset synchronized PWM mode	not provided	not provided	provided	not provided
	Complementary PWM mode	not provided	not provided	provided	not provided
	PWM3 mode	not provided	not provided	provided	not provided
Input Pin		TRAIO	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRDCLK TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	-
Output Pin		TRAO TRAIO	TRBO	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	TREO
Related Interrupt		Timer RA int INT1 int	Timer RB int INT0 int	Compare match / input capture A0 to D0 int Compare match / input capture A1 to D1 int Overflow int Underflow int(1) INT0 int	Timer RE int
Timer Stop		provided	provided	provided	provided

NOTE:
1. The underflow interrupt can be set to channel 1.

14.1 Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer consist of the reload register and counter. The reload register and counter are allocated at the same address. When accessing the TRAPRE and TRA registers, the reload register and counter can be accessed (refer to **Table 14.2 to 14.6 the Specification of Each Modes**).
The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 14.1 shows the Block Diagram of Timer RA. Figures 14.2 to 14.4 show the registers associated with Timer RA.

Timer RA contains five operation modes listed as follows:

- Timer mode: The timer counts an internal count source.
- Pulse output mode: The timer counts an internal count source and outputs the pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

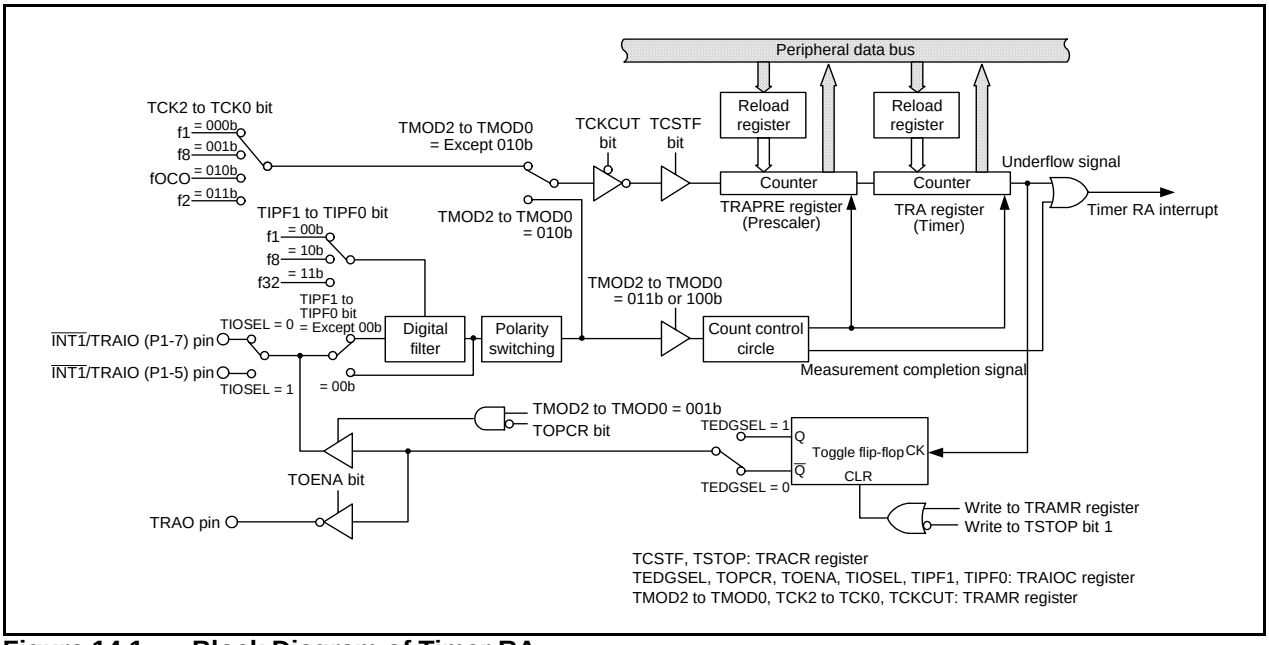
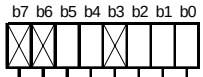


Figure 14.1 Block Diagram of Timer RA

Timer RA Control Register(4)

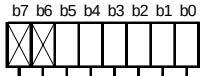


Symbol	Address	After Reset
TRACR	0100h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RA count start bit(1)	0 : Stops counting 1 : Starts counting	RW
TCSTF	Timer RA count status flag(1)	0 : Stops counting 1 : Counting	RO
TSTOP	Timer RA count forcible stop bit(2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TEDGF	Active edge reception flag(3,5)	0 : Active edge not received 1 : Active edge received (end of measurement period)	RW
TUNDF	Timer RA underflow flag(3,5)	0 : No underflow 1 : Underflow	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **14.1.6 Notes on Timer RA**.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.
5. Set to 0 in timer mode, pulse output mode, and event counter mode.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Function varies depending on operation mode	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	INT1/TRAIO select bit		RW
TIPF0	TRAIO input filter select bits		RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.2 Registers TRACR and TRAIOC

Timer RA Mode Register(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRAMR	0102h	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RA operation mode select bits	b2 b1 b0 0 0 0 : Timer mode 0 0 1 : Pulse output mode 0 1 0 : Event counter mode 0 1 1 : Pulse width measurement mode 1 0 0 : Pulse period measurement mode 1 0 1 : } Do not set 1 1 0 : } 1 1 1 : }	RW
TMOD1			RW
TMOD2			RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCK0	Timer RA count source select bits	b6 b5 b4 0 0 0 : f1 0 0 1 : f8 0 1 0 : fOCO 0 1 1 : f2 1 0 0 : } Do not set 1 0 1 : } 1 1 0 : } 1 1 1 : }	RW
TCK1			RW
TCK2			RW
TCKCUT	Timer RA count source cutoff bit	0 : Provides count source 1 : Cuts off count source	RW

NOTE:
1. When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

Timer RA Prescaler Register

b7 b0

Symbol	Address	After Reset
TRAPRE	0103h	FFh(1)

Mode	Function	Setting Range	RW
Timer Mode	Counts an internal count source	00h to FFh	RW
Pulse Output Mode	Counts an internal count source	00h to FFh	RW
Event Counter Mode	Counts an external count source	00h to FFh	RW
Pulse Width Measurement Mode	Counts an internal count source	00h to FFh	RW
Pulse Period Measurement Mode	Counts an internal count source	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.

Figure 14.3 Registers TRAMR and TRAPRE

Timer RA Register

b7 b0

Symbol	Address	After Reset
TRA	0104h	FFh(1)

Mode	Function	Setting Range	RW
All Modes	Counts of an underflow of the TRAPRE register	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.

Figure 14.4 TRA Register

14.1.1 Timer Mode

In this mode, the timer counts an internally generated count source (see **Table 14.2 Timer Mode Specifications**).
Figure 14.5 shows the TRAIOC Register in Timer Mode.

Table 14.2 Timer Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, fOCO
Count Operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is inherited
Divide Ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count Start Condition	Write 1 (count starts) to the TSTART bit in the TRACR register
Count Stop Conditions	• Write 0 (count stops) to the TSTART bit in the TRACR register • Write 1 (count forcibly stops) to the TSTOP bit in the TRACR register
Interrupt Request Generation Timing	When Timer RA underflows [Timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO Pin Function	Programmable I/O port or $\overline{\text{INT1}}$ interrupt input
TRAO Pin Function	Programmable I/O port
Read from Timer	The count value can be read by reading the TRA and TRAPRE registers
Write to Timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).

Timer RA I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	0	0		0	0	0

Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits	Set to 0 in timer mode	RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.5 TRAIOC Register in Timer Mode

14.1.1.1 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed.

Figure 14.6 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

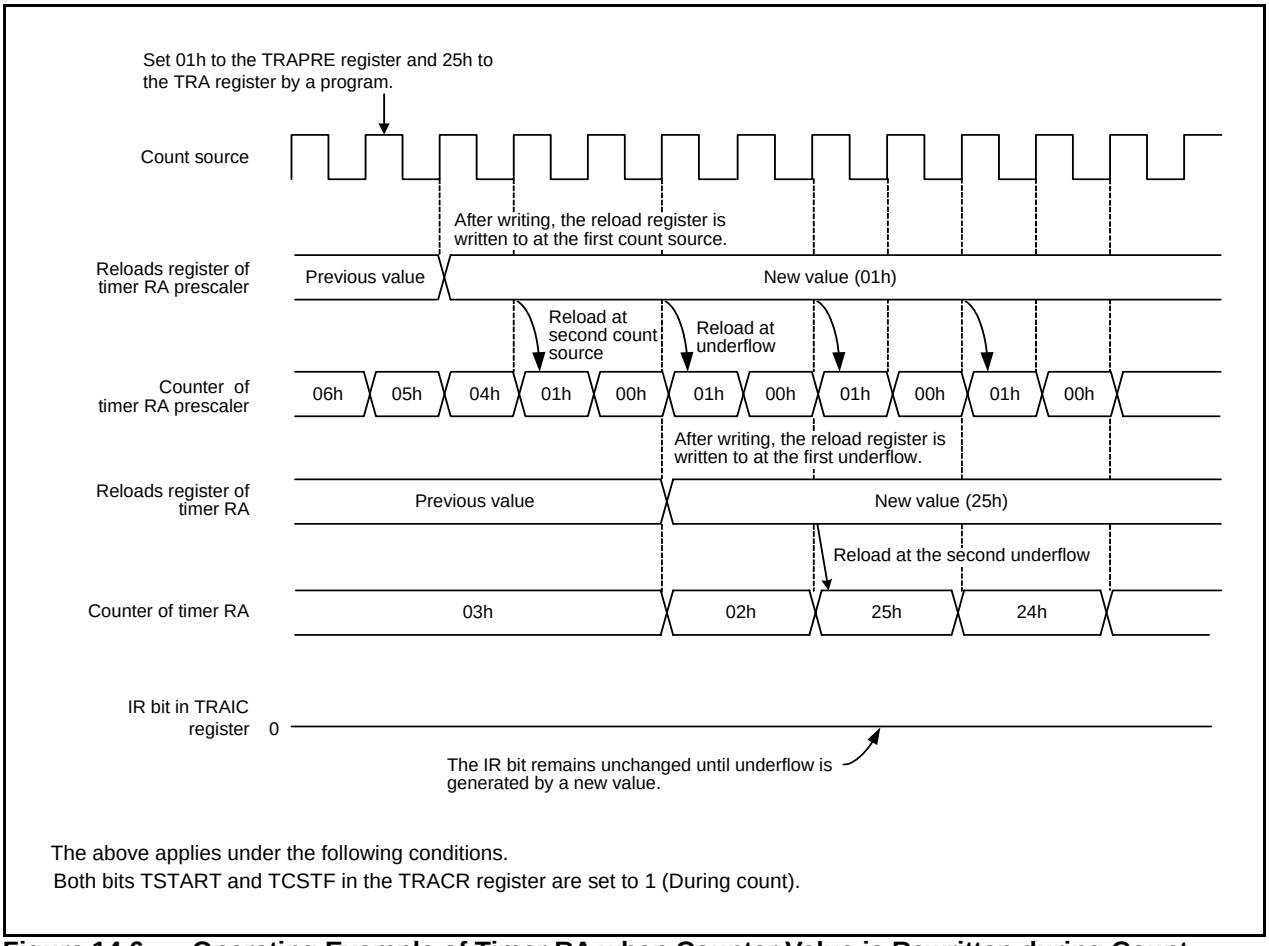


Figure 14.6 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

14.1.2 Pulse Output Mode

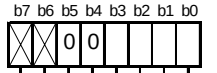
Pulse output mode is mode to count the count source internally generated and outputs the pulse which inverts the polarity from the TRAIO pin each time the timer underflows (see **Table 14.3 Pulse Output Mode Specifications**).
Figure 14.7 shows the TRAIOC Register in Pulse Output Mode.

Table 14.3 Pulse Output Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, fOCO
Count Operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is inherited
Divide Ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count Start Condition	Write 1 (count starts) to the TSTART bit in the TRACR register
Count Stop Conditions	• Write 0 (count stops) to the TSTART bit in the TRACR register • Write 1 (count forcibly stops) to the TSTOP bit in the TRACR register
Interrupt Request Generation Timing	When timer RA underflows [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO Pin Function	Pulse output, programmable output port, or $\overline{\text{INT1}}$ interrupt(1)
TRAO Pin Function	Programmable I/O port or inverted output of TRAIO(1)
Read from Timer	The count value can be read by reading the TRA and TRAPRE registers
Write to Timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select Functions	• TRAIO output polarity switch function The TEDGSEL bit in the TRAIOC register can select the polarity level when the pulse output starts(1) • Inverted pulse output function The pulse which inverts the polarity of the TRAIO output can be output from the TRAO pin (selected by the TOENA bit in the TRAIOC register) • Pulse output stop function The pulse output from the TRAIO pin can be stopped by the TOPCR bit. • INT1/TRAIO pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register.

NOTE:
1. The level of output pulse turn into the level when the pulse output starts by writing the TRAMR register.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : TRAIO output starts at “H” 1 : TRAIO output starts at “L”	RW
TOPCR	TRAIO output control bit	0 : TRAIO output 1 : Port P1_7 or P1_5	RW
TOENA	TRAO output enable bit	0 : Port P3_0 1 : TRAO output (Inverted TRAIO output from P3_0)	RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits	Set to 0 in pulse output mode	RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.7 TRAIOC Register in Pulse Output Mode

14.1.3 Event Counter Mode

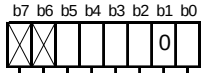
Event counter mode is mode to count an external signal which inputs from the $\overline{\text{INT1}}$/TRAIO pin (see **Table 14.4 Event Counter Mode Specifications**).
Figure 14.8 shows the TRAIOC Register in Event Counter Mode.

Table 14.4 Event Counter Mode Specifications

Item	Specification
Count Source	External signal which is input to TRAIO pin (active edge is selectable by a program)
Count Operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is inherited
Divide Ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count Start Condition	Write 1 (count starts) to the TSTART bit in the TRACR register
Count Stop Conditions	• Write 0 (count stops) to the TSTART bit in the TRACR register • Write 1 (count forcibly stops) to the TSTOP bit in the TRACR register
Interrupt Request Generation Timing	When timer RA underflows [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO Pin Function	Count source input ($\overline{\text{INT1}}$ interrupt input)
TRAO Pin Function	Programmable I/O port(1)
Read from Timer	The count value can be read by reading the TRA and TRAPRE registers
Write to Timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select Functions	• $\overline{\text{INT1}}$ input polarity switch function The TEDGSEL bit in the TRAIOC register can select the active edge of the count source. • Count source input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Pulse output function The pulse which inverts the polarity can be output from the TRAO pin each time the timer underflows. (selected by the TOENA bit in the TRAIOC register)(1) • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTE:
1. The level of output pulse turn into the level when the pulse output starts by writing the TRAMR register.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : Starts counting at rising edge of the TRAIO input or TRAIO starts output at "L" 1 : Starts counting at falling edge of the TRAIO input or TRAIO starts output at "H"	RW
TOPCR	TRAIO output control bit	Set to 0 in event counter mode	RW
TOENA	TRAO output enable bit	0 : Port P3_0 1 : TRAO output	RW
TIOSEL	$\overline{INT1}$/TRAIO select bit	0 : $\overline{INT1}$/TRAIO pin (P1_7) 1 : $\overline{INT1}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 14.8 TRAIOC Register in Event Counter Mode

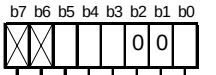
14.1.4 Pulse Width Measurement Mode

Pulse width measurement mode is mode to measure the pulse width of an external signal which inputs from the $\overline{\text{INT1}}$/TRAIO pin (see **Table 14.5 Pulse Width Measurement Mode Specifications**).
Figure 14.9 shows the TRAIOC Register in Pulse Width Measurement Mode and Figure 14.10 shows the Operating Example of Pulse Width Measurement Mode.

Table 14.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, fOCO
Count Operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents in the reload register is reloaded and the count is inherited
Count Start Condition	Write 1 (count starts) to the TSTART bit in the TRACR register
Count Stop Conditions	• Write 0 (count stops) to the TSTART bit in the TRACR register • Write 1 (count forcibly stops) to the TSTOP bit in the TRACR register
Interrupt Request Generation Timing	• When timer RA underflows [timer RA interrupt] • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO Pin Function	Measurement pulse input ($\overline{\text{INT1}}$ interrupt input)
TRAO Pin Function	Programmable I/O port
Read from Timer	The count value can be read by reading the TRA and TRAPRE registers.
Write to Timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select Functions	• Measurement level select The TEDGSEL bit in the TRAIOC register can select during “H” or “L” level • Measurement pulse input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : TRAIO input starts at "L" 1 : TRAIO input starts at "H"	RW
TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode	RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 14.9 TRAIOC Register in Pulse Width Measurement Mode

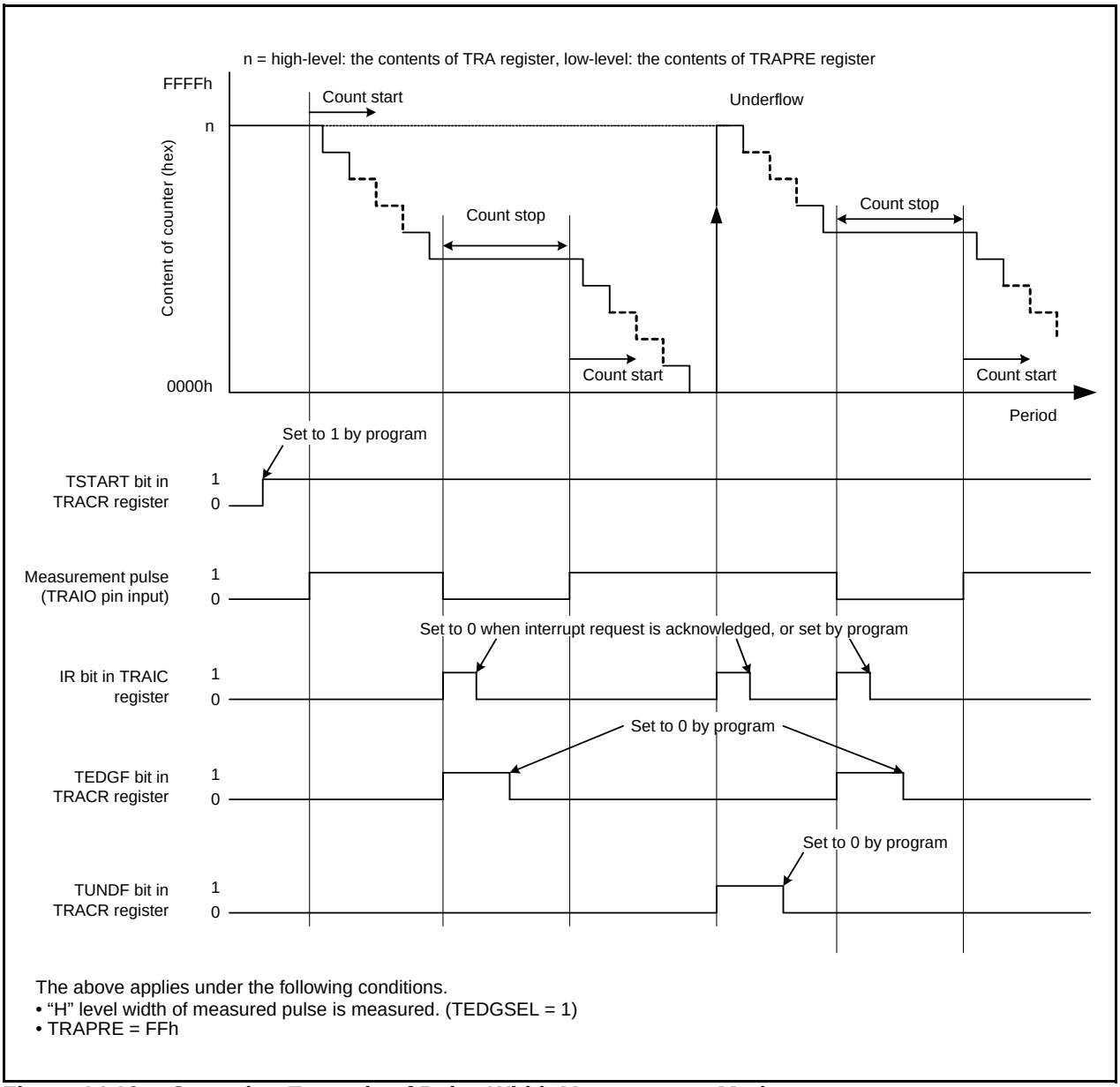


Figure 14.10 Operating Example of Pulse Width Measurement Mode

14.1.5 Pulse Period Measurement Mode

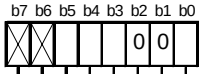
Pulse period measurement mode is mode to measure the pulse period of an external signal which inputs from the $\overline{\text{INT1}}$/TRAIO pin (see **Table 14.6 Pulse Period Measurement Mode Specifications**).
Figure 14.11 shows the TRAIOC Register in Pulse Period Measurement Mode and Figure 14.12 shows the Operating Example of Pulse Period Measurement Mode.

Table 14.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, fOCO
Count Operations	• Decrement • After an active edge of measurement pulse is input, contents for the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count Start Condition	Write 1 (count start) to the TSTART bit in the TRACR register
Count Stop Conditions	• Write 0 (count stop) to TSTART bit in the TRACR register • Write 1 (count forcibly stops) to the TSTOP bit in the TRACR register
Interrupt Request Generation Timing	• When timer RA underflows or reloads [timer RA interrupt] • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO Pin Function	Measurement pulse input(1) ($\overline{\text{INT1}}$ interrupt input)
TRAO Pin Function	Programmable I/O port
Read from Timer	The count value can be read by reading the TRA and TRAPRE registers.
Write to Timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select Functions	• Measurement level select The TEDGSEL bit in the TRAIOC register can select the measurement period of input pulse. • Measurement pulse input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTE:
1. Input the pulse whose period is longer than twice of the timer RA prescaler period. Input the longer pulse for “H” width and “L” width than the timer RA prescaler period. If the shorter pulse than the period is input to the TRAIO pin, the input may be disabled.

Timer RA I/O Control Register

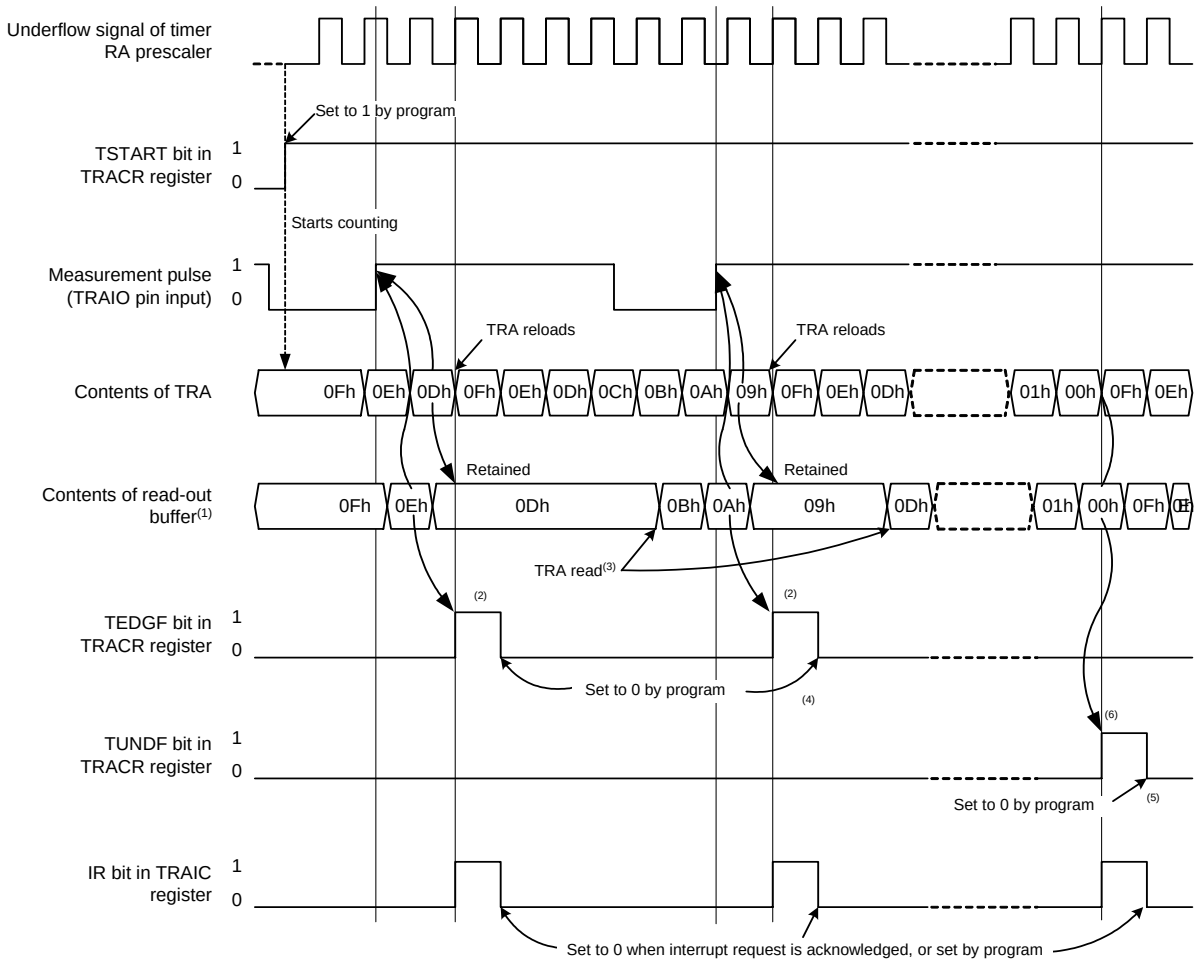


Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : Measures measurement pulse from one rising edge to next rising edge 1 : Measures measurement pulse from one falling edge to next falling edge	RW
TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode	RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 14.11 TRAIOC Register in Pulse Period Measurement Mode



Conditions: A period from one rising edge to the next rising edge of measurement pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

NOTES:
1. The contents of the read-out buffer can be read when the TRA register is read in pulse period measurement mode.
2. After an active edge of measurement pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge found) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge found). The content in the read-out buffer is retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. When set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. When set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. The TUNDF and TEDGF bits are both set to 1 if the timer RA underflows and reloads on an active edge simultaneously.

Figure 14.12 Operating Example of Pulse Period Measurement Mode

14.1.6 Notes on Timer RA

- Timer RA stops counting after reset. Set the value to timer RA and timer RA prescaler before the count starts.
- Even if the prescaler and timer RA is read out in 16-bit units, these registers are read by 1 byte in the MCU. Consequently, the timer value may be updated during the period these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, the TEDGF and TUNDF bits in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged when 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is executed. At the time, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse width measurement mode and pulse period measurement mode from other mode, the contents of the TEDGF and TUNDF bits are indeterminate. Write 0 to the TEDGF and TUNDF bits before the count starts.
- The TEDGF bit may be set to 1 by timer RA prescaler underflow which is generated for the first time since the count starts.
- When using the pulse period measurement mode, leave two periods or more of timer RA prescaler immediately after count starts, and set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count stops.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).
  The TCSTF bit retains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is performing. Timer RA counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, TRA

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

14.2 Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer consist of the reload register and counter. (Refer to **Table 14.7 to 14.10 the Specification of Each Modes**).
Timer RB contains the timer RB primary and timer RB secondary as the reload register.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 14.13 shows the Block Diagram of Timer RB. Figures 14.14 and 14.16 show the registers associated with timer RB.

Timer RB contains four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs delayed one-shot pulse.

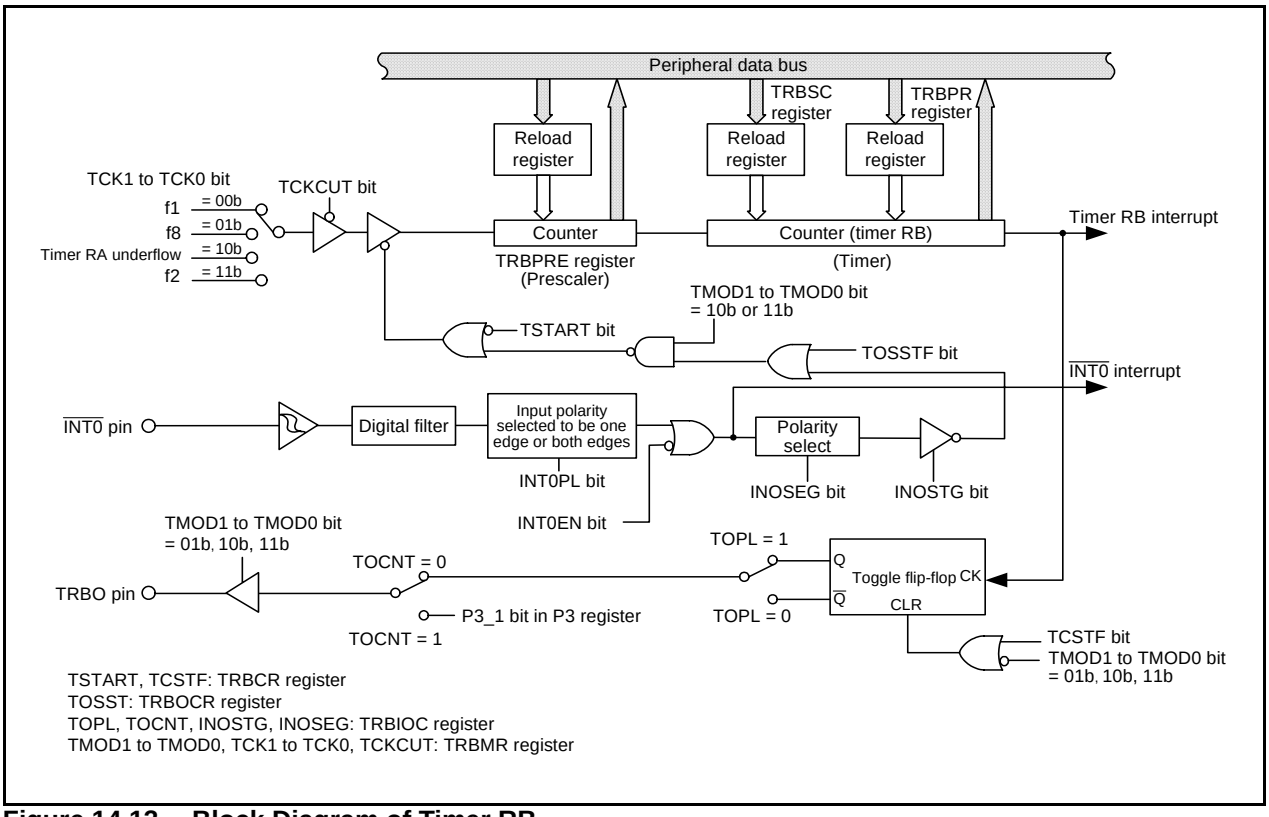
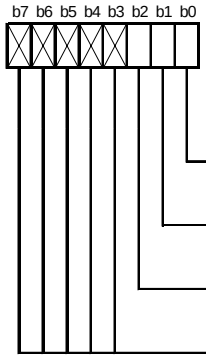


Figure 14.13 Block Diagram of Timer RB

Timer RB Control Register

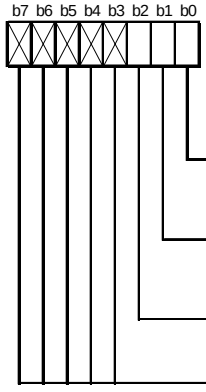


Symbol	Address	After Reset
TRBCR	0108h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RB count start bit(1)	0 : Stops counting 1 : Starts counting	RW
TCSTF	Timer RB count status flag(1)	0 : Stops counting 1 : Counting(3)	RO
TSTOP	Timer RB count forcible stop bit(1,2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **14.2.5 Notes on Timer RB**.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger has been acknowledged.

Timer RB One-Shot Control Register(2)



Symbol	Address	After Reset
TRBOCR	0109h	00h

Bit Symbol	Bit Name	Function	RW
TOSST	Timer RB one-shot start bit	When this bit is set to 1, the one-shot trigger generated. When read, the content is 0.	RW
TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, the one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	RW
TOSSTF	Timer RB one-shot status flag(1)	0 : One-shot stopping 1 : One-shot operating (including wait period)	RO
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.
2. This register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 10b (programmable wait one-shot generation mode).

Figure 14.14 Registers TRBCR and TRBOCR

Timer RB I/O Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	Function varies depending on operating mode	RW
TOCNT	Timer RB output switch bit		RW
INOSTG	One-shot trigger control bit		RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Timer RB Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRBMR	010Bh	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RB operating mode select bits(1)	b1 b0 0 0 : Timer mode 0 1 : Programmable waveform generation mode 1 0 : Programmable one-shot generation mode 1 1 : Programmable wait one-shot generation mode	RW
TMOD1			RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TWRC	Timer RB write control bit(2)	0 : Write to reload register and counter 1 : Write to reload register only	RW
TCK0	Timer RB count source select bits(1)	b5 b4 0 0 : f1 0 1 : f8 1 0 : Timer RA underflow 1 1 : f2	RW
TCK1			RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCKCUT	Timer RB count source cutoff bit(1)	0 : Provides count source 1 : Cuts off count source	RW

NOTES:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).

Figure 14.15 Registers TRBIOC and TRBMR

Timer RB Prescaler Register(1)

b7 b0

Symbol	Address	After Reset
TRBPRE	010Ch	FFh

Mode	Function	Setting Range	RW
Timer mode	Counts an internal count source or a timer RA underflow	00h to FFh	RW
Programmable waveform generation mode		00h to FFh	RW
Programmable one-shot generation mode		00h to FFh	RW
Programmable wait one-shot generation mode		00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

Timer RB Secondary Register(3,4)

b7 b0

Symbol	Address	After Reset
TRBSC	010Dh	FFh

Mode	Function	Setting Range	RW
Timer mode	Disable	00h to FFh	—
Programmable waveform generation mode	Counts a timer RB prescaler underflow (1)	00h to FFh	WO(2)
Programmable one-shot generation mode	Disable	00h to FFh	—
Programmable wait one-shot generation mode	Counts a timer RB prescaler underflow (one-shot width is counted)	00h to FFh	WO(2)

NOTES:
1. Each value in the TRBPR register and TRBSC register is reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.
3. When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
4. To write to the TRBSC register, perform the following steps.
   (1) Write the value to the TRBSC register.
   (2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

Timer RB Primary Register(2)

b7 b0

Symbol	Address	After Reset
TRBPR	010Eh	FFh

Mode	Function	Setting Range	RW
Timer mode	Counts a timer RB prescaler underflow	00h to FFh	RW
Programmable waveform generation mode	Counts a timer RB prescaler underflow (1)	00h to FFh	RW
Programmable one-shot generation mode	Counts a timer RB prescaler underflow (one-shot width is counted)	00h to FFh	RW
Programmable wait one-shot generation mode	Counts a timer RB prescaler underflow (wait period width is counted)	00h to FFh	RW

NOTES:
1. Each value in the TRBPR register and TRBSC register is reloaded to the counter alternately and counted.
2. When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

Figure 14.16 Registers TRBPRE, TRBSC, and TRBPR

14.2.1 Timer Mode

Timer mode is mode to count a count source which is internally generated or timer RA underflow (see **Table 14.7 Timer Mode Specifications**). The TRBOCR and TRBSC registers are unused in timer mode.
Figure 14.17 shows the TRBIOC Register in Timer Mode.

Table 14.7 Timer Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, Timer RA underflow
Count Operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded)
Divide Ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count Start Condition	Write 1 (count starts) to the TSTART bit in the TRBCR register
Count Stop Conditions	• Write 0 (count stops) to the TSTART bit in the TRBCR register • Write 1 (count forcibly stop) to the TSTOP bit in the TRBCR register
Interrupt Request Generation Timing	When timer RB underflows [timer RB interrupt]
TRBO Pin Function	Programmable I/O port
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read out by reading the TRBPR and TRBPRE registers
Write to Timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **14.2.1.1 Timer Write Control during Count Operation**.)

Timer RB I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0	0	0	0

Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	Set to 0 in timer mode	RW
TOCNT	Timer RB output switch bit		RW
INOSTG	One-shot trigger control bit		RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.17 TRBIOC Register in Timer Mode

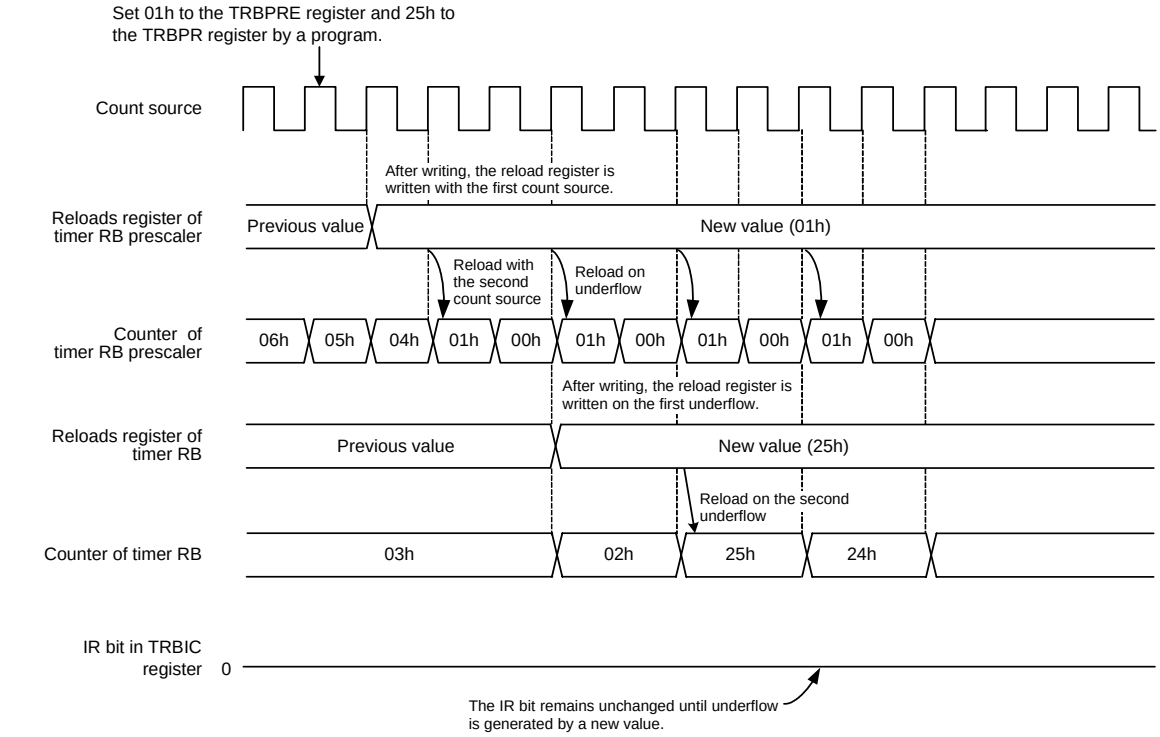
14.2.1.1 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

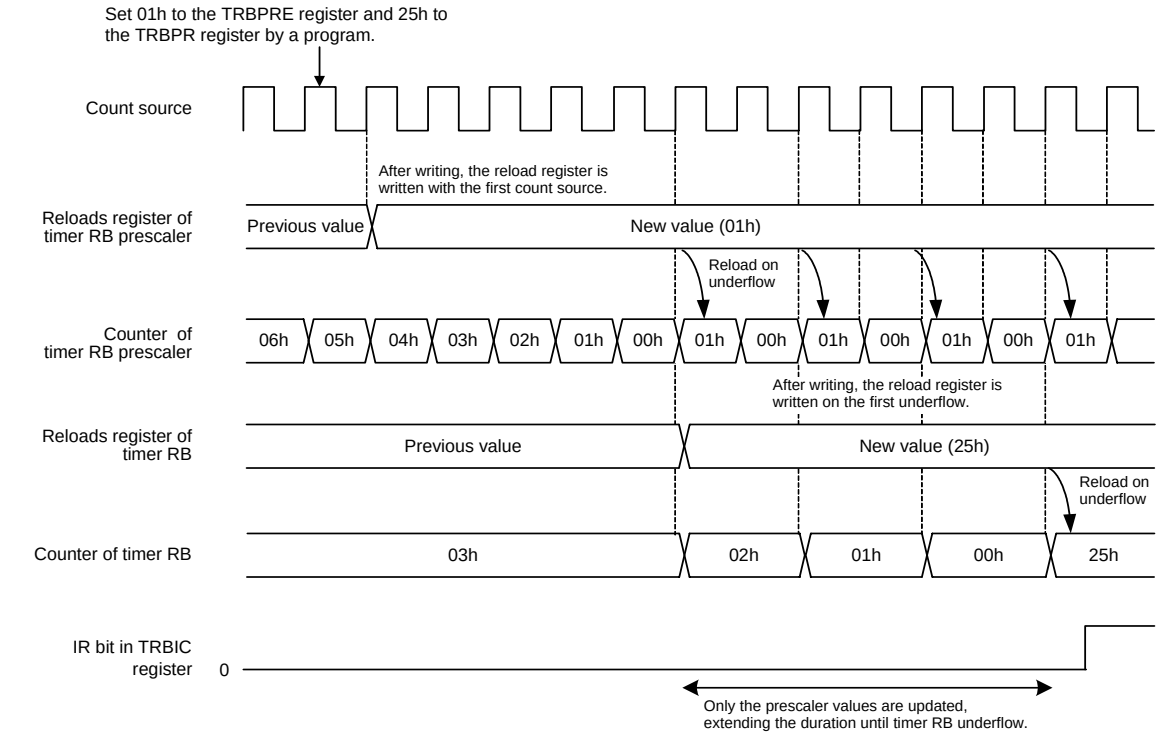
However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes.

Figure 14.18 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

When the TWRC bit is set to 0 (write to reload register and counter)



When the TWRC bit is set to 1 (write to reload register only)



The above applies under the following conditions.
Both bits TSTART and TCSTF in the TRBCR register are set to 1 (During count).

Figure 14.18 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

14.2.2 Programmable Waveform Generation Mode

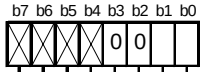
Programmable waveform generation mode is mode to invert the signal output from the TRBO pin each time the counter underflows, while the values in the TRBPR and TRBSC registers are counted alternately (see **Table 14.8 Programmable Waveform Generation Mode Specifications**). A counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 14.19 shows the TRBIOC Register in Programmable Waveform Generation Mode. Figure 14.20 shows the Operation Example of Timer RB in Programmable Waveform Generation Mode.

Table 14.8 Programmable Waveform Generation Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, timer RA underflow
Count Operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and Period of Output Waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Setting value in TRBPRE register m: Setting value in TRBPR register p: Setting value in TRBSC register
Count Start Condition	Write 1 (count start) to the TSTART bit in the TRBCR register
Count Stop Conditions	• Write 0 (count stop) to the TSTART bit in the TRBCR register • Write 1 (count forcibly stop) to the TSTOP bit in the TRBCR register
Interrupt Request Generation Timing	In half of count source, after timer RB underflows during secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO Pin Function	Programmable output port or pulse output
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read out by reading the TRBPR and TRBPRE registers(1)
Write to Timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(2)
Select Functions	• Output level select function The TOPL bit can select the output level during primary and secondary periods. • TRBO pin output switch function Timer RB pulse output or P3_1 latch output is selected by the TOCNT bit in the TRBIOC register.(3)

NOTES:
1. Even when counting the secondary period, read out the TRBPR register.
2. The set values are reflected to the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   - When count starts.
   - When the timer RB interrupt request is generated.
     The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

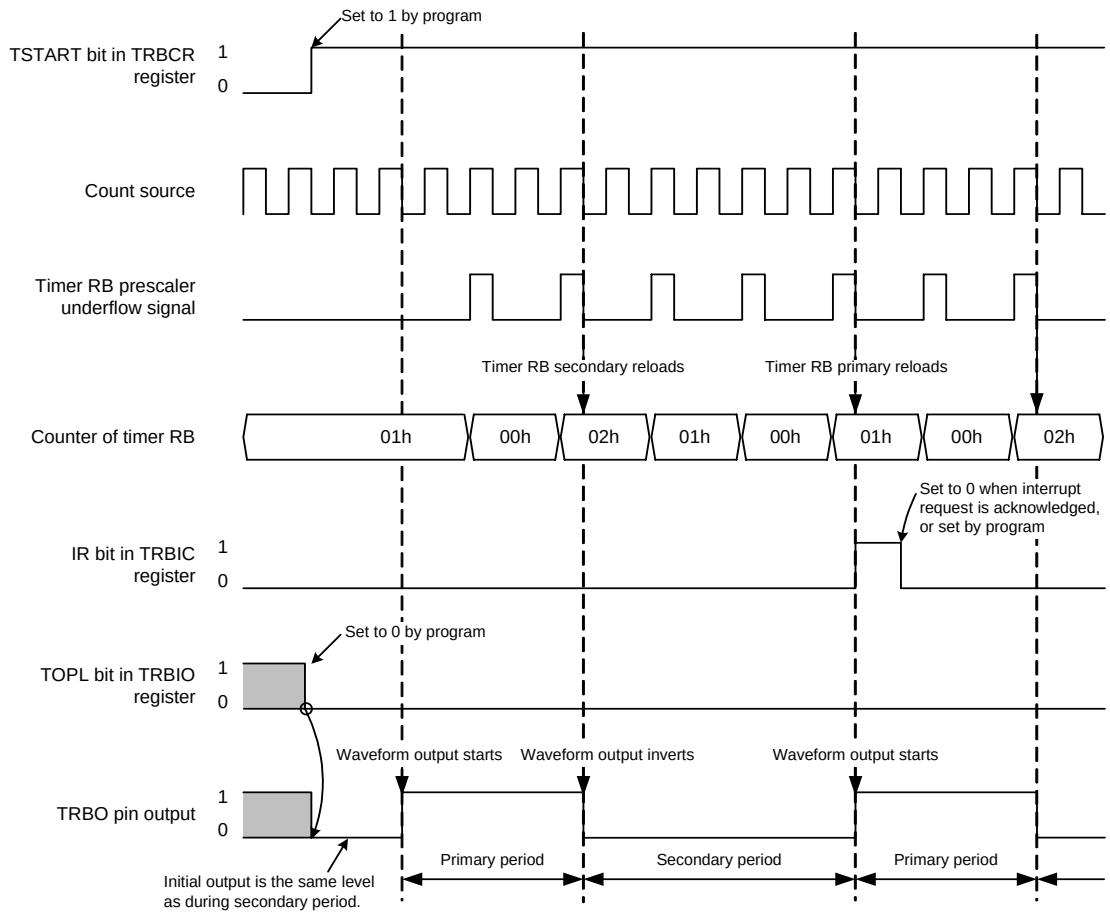
Timer RB I/O Control Register



Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0 : Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1 : Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB output switch bit	0 : Outputs timer RB waveform 1 : Outputs value in P3_1 port latch	RW
INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode	RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.19 TRBIOC Register in Programmable Waveform Generation Mode



The above applies to the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 14.20 Operation Example of Timer RB in Programmable Waveform Generation Mode

14.2.3 Programmable One-shot Generation Mode

Programmable one-shot generation mode is mode to output the one-shot pulse from the TRBO pin by a program or an external trigger input (input to the INT0 pin) (see **Table 14.9 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is unused in this mode.

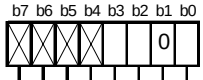
Figure 14.21 shows the TRBIOC Register in Programmable One-Shot Generation Mode. Figure 14.22 shows the Operation Example of Programmable One-Shot Generation Mode.

Table 14.9 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, timer RA underflow
Count Operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When a count stops, the timer reloads the contents of the reload register before it stops.
One-Shot Pulse Output Time	(n+1)(m+1)/fi fi: Count source frequency, n: Setting value in TRBPRE register, m: Setting value in TRBPR register(2)
Count Start Conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the INT0 pin
Count Stop Conditions	• When reloading completes after Timer RB underflows during primary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt Request Generation Timing	In half cycles of count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]
TRBO Pin Function	Pulse output
INT0 Pin Functions	• When the INOSTG bit in the TRBIOC register is set to 0 (INT0 one-shot trigger disabled), programmable I/O port or INT0 interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 (INT0 one-shot trigger enabled), external trigger (INT0 interrupt input)
Read from Timer	The count value can be read out by reading the TRBPR and TRBPRE registers.
Write to Timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload)(1).
Select Functions	• Output level select function The TOPL bit in the TRBIOC register can select the output level of the one-shot pulse waveform. • One-shot trigger select function Refer to **14.2.3.1 One-Shot Trigger Selection**.

NOTES:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.
2. Do not set both the TRBPRE and TRBPR registers to 00h.

Timer RB I/O Control Register

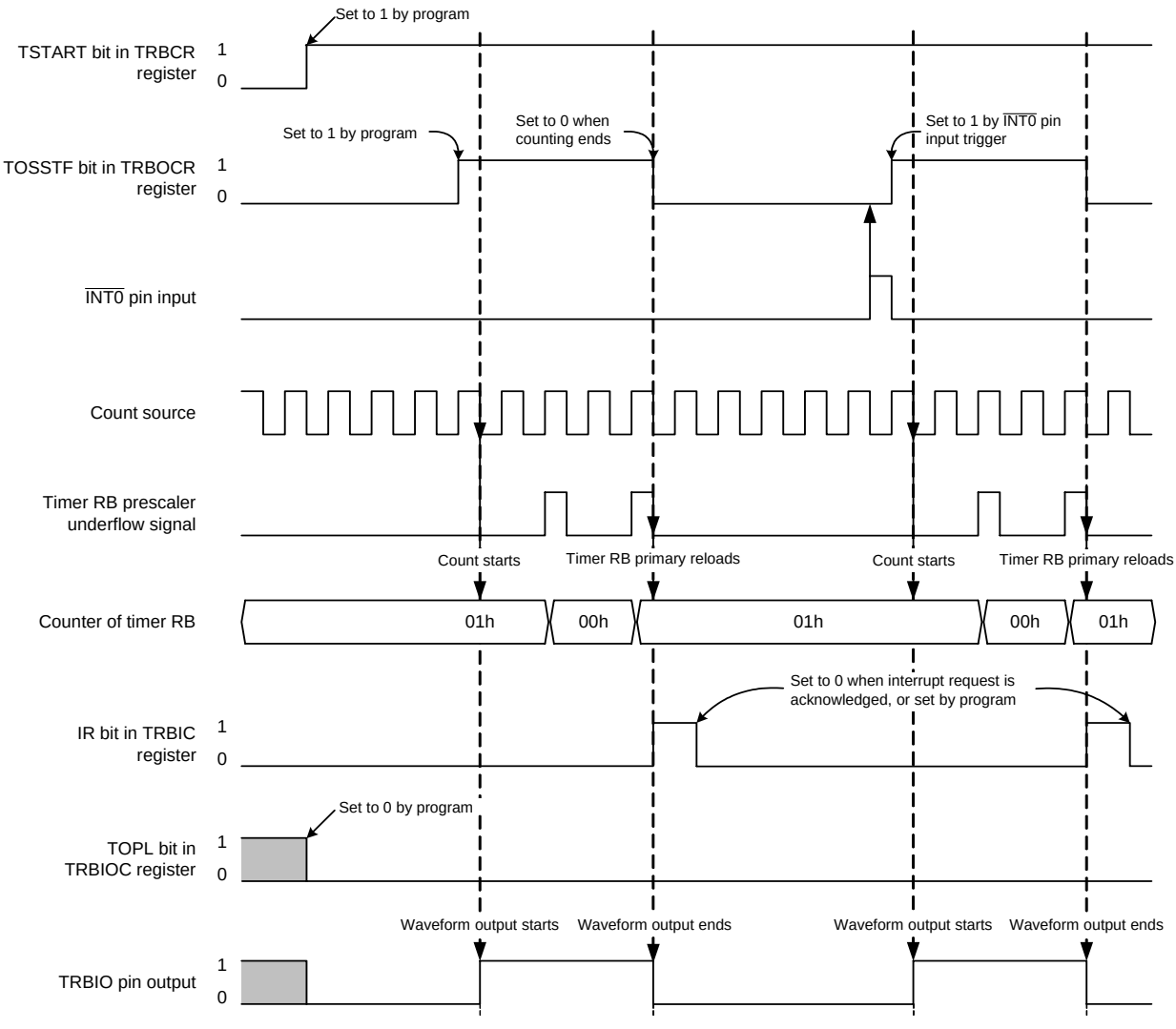


Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0 : Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1 : Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB output switch bit	Set to 0 in programmable one-shot generation mode	RW
INOSTG	One-shot trigger control bit(1)	0 : $\overline{INT0}$ pin one-shot trigger disabled 1 : $\overline{INT0}$ pin one-shot trigger enabled	RW
INOSEG	One-shot trigger polarity select bit(1)	0 : Falling edge trigger 1 : Rising edge trigger	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Refer to **14.2.3.1 One-shot Trigger Selection**.

Figure 14.21 TRBIOC Register in Programmable One-Shot Generation Mode



The above applies to the following conditions.

TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 14.22 Operation Example of Programmable One-Shot Generation Mode

14.2.3.1 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 0 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **12. Interrupts** for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

14.2.4 Programmable Wait One-shot Generation Mode

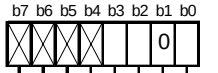
Programmable wait one-shot generation mode is mode to output the one-shot pulse from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (see **Table 14.10 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from this point, the timer starts outputting pulses only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.
Figure 14.23 shows the TRBIOC Register in Programmable Wait One-Shot Generation Mode. Figure 14.24 shows the Operation Example of Programmable Wait One-Shot Generation Mode.

Table 14.10 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count Sources	f1, f2, f8, timer RA underflow
Count Operations	• Decrement the setting value in timer RB primary • When a count of timer RB primary underflows, the timer reloads the contents of the timer RB secondary before the count continues. • When a count of timer RB secondary underflows, the timer reloads the contents of the timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When a count stops, the timer reloads the contents of the reload register before it stops.
Wait Time	(n+1)(m+1)/fi fi: Count source frequency n: Setting value in the TRBPRE register, m: Setting value in the TRBPR register(2)
One-Shot Pulse Output Time	(n+1)(p+1)/fi fi: Count source frequency n: Setting value in the TRBPRE register, p: Setting value in the TRBSC register
Count Start Conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the INT0 pin
Count Stop Conditions	• When reloading completes after timer RB underflows during secondary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (starts counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt Request Generation Timing	In half cycles of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt]
TRBO Pin Function	Pulse output
INT0 Pin Functions	• When the INOSTG bit in the TRBIOC register is set to 0 (INT0 one-shot trigger disabled), programmable I/O port or INT0 interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 (INT0 one-shot trigger enabled), external trigger (INT0 interrupt input)
Read from Timer	The count value can be read out by reading the TRBPR and TRBPRE registers.
Write to Timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(1)
Select Functions	• Output level select function The TOPL bit in the TRBIO register can select the output level of the one-shot pulse waveform. • One-shot trigger select function Refer to **14.2.3.1 One-Shot Trigger Selection**.

NOTES:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.
2. Do not set both the TRBPRE and TRBPR registers to 00h.

Timer RB I/O Control Register

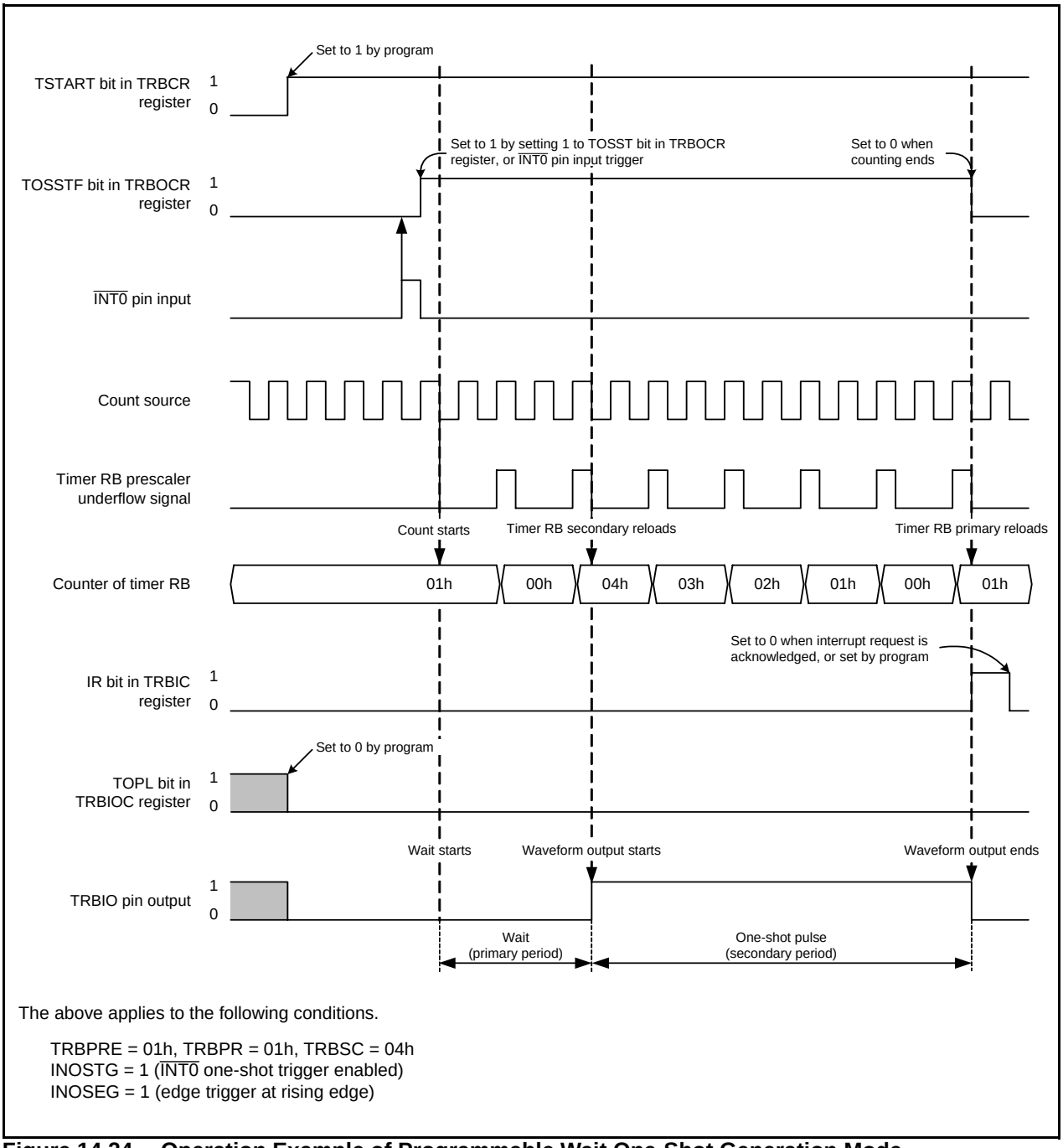


Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0 : Outputs one-shot pulse “H” Outputs “L” when the timer is stopped or during wait 1 : Outputs one-shot pulse “L” Outputs “H” when the timer is stopped or during wait	RW
TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode	RW
INOSTG	One-shot trigger control bit(1)	0 : $\overline{INT0}$ pin one-shot trigger disabled 1 : $\overline{INT0}$ pin one-shot trigger enabled	RW
INOSEG	One-shot trigger polarity select bit(1)	0 : Falling edge trigger 1 : Rising edge trigger	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Refer to **14.2.3.1 One-shot Trigger Selection.**

Figure 14.23 TRBIOC Register in Programmable Wait One-Shot Generation Mode



The above applies to the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 14.24 Operation Example of Programmable Wait One-Shot Generation Mode

14.2.5 Notes on Timer RB

- Timer RB stops counting after reset. Set the value to timer RB and timer RB prescaler before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read by 1 byte in the MCU. Consequently, the timer value may be updated during the period these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0, 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, read the timer count value in programmable one-shot generation mode and programmable wait one-shot generation mode before the timer stops.
- The TCSTF bit retains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count stops.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.
  The TCSTF bit retains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is performing. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, TRBPR

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

14.2.5.1 Timer mode

The following workaround should be performed in timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

14.2.5.2 Programmable waveform generation mode

The following three workarounds should be performed in programmable waveform generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 14.25 and 14.26.

The following shows the detailed workaround examples.

- Workaround example (a):
  As shown in Figure 14.25, write to registers TRBSC and TRBPR in the timer RB interrupt routine. These write operations must be completed by the beginning of period A.

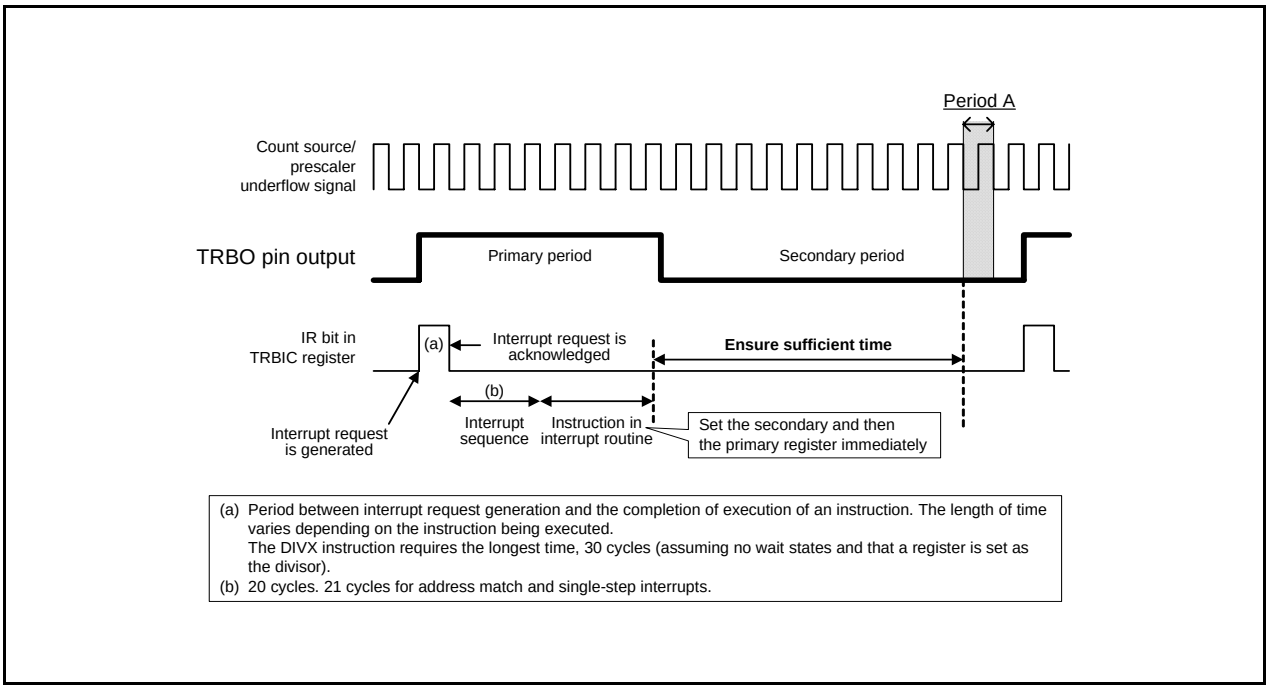


Figure 14.25 Workaround Example (a) When Timer RB Interrupt is Used

• Workaround example (b):
As shown in Figure 14.26 detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. These write operations must be completed by the beginning of period A.
If the port register's bit value is read after the port direction register's bit corresponding to the TRBO pin is set to 0 (input mode), the read value indicates the TRBO pin output value.

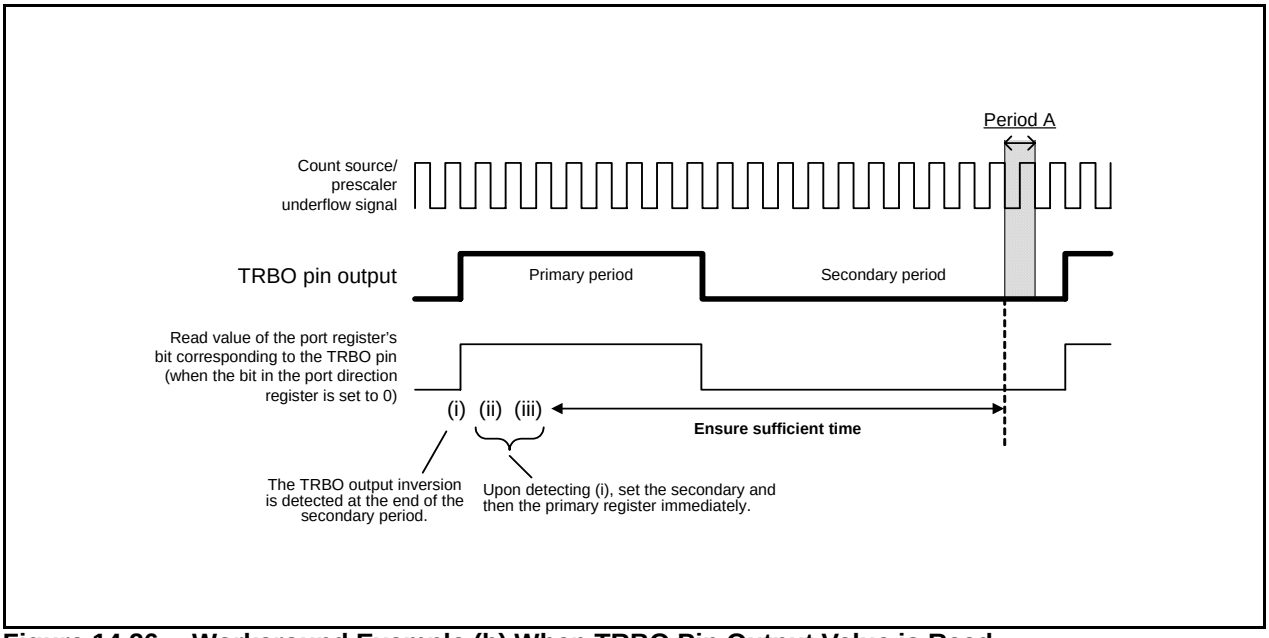


Figure 14.26 Workaround Example (b) When TRBO Pin Output Value is Read

(3) To stop the timer counting in the primary period, use the TSTOP bit in the TRBCR register. In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

14.2.5.3 Programmable one-shot generation mode

The following two workarounds should be performed in programmable one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

• When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

• When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

14.2.5.4 Programmable wait one-shot generation mode

The following three workarounds should be performed in programmable wait one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

(3) Set registers TRBSC and TRBPR using the following procedure.

(a) To use "$\overline{\text{INT0}}$ pin one-shot trigger enabled" as the count start condition
Set the TRBSC register and then the TRBPR register. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before trigger input from the $\overline{\text{INT0}}$ pin.

(b) To use "writing 1 to TOSST bit" as the start condition
Set the TRBSC register, the TRBPR register, and then TOSST bit. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit.

14.3 Timer RD

Timer RD has 2 16-bit timers (channels 0 and 1). Each channel has 4 I/O pins.
The operation clock of Timer RD is f1 or fOCO40M.
Table 14.11 lists the Timer RD Operation Clocks.

Table 14.11 Timer RD Operation Clocks

Condition	Operation Clock of Timer RD
The count source is f1, f2, f4, f8, f32 and TRDCLK input. (The TCK2 to TCK0 bits in the TRDCR0 and TRDCR1 registers are set to 000b to 101b.)	f1
The count source is fOCO40M. (The TCK2 to TCK0 bits in the TRDCR0 and TRDCR1 registers are set to 110b.)	fOCO40M

Figure 14.27 shows the Block Diagram of Timer RD. Timer RD has 5 modes:

- Timer mode
  - Input capture function — Transfer the counter value to a register as a trigger of the external signal
  - Output compare function — Detect the register value match with a counter (Pin output can be changed at detection)

The following 4 modes using the output compare function.

- PWM mode — Output any-wide pulse continuously
- Reset synchronous PWM mode — Output three-phase waveforms (6) without sawtooth wave modulation and dead time
- Complementary PWM mode — Output three-phase waveforms (6) with triangular wave modulation and dead time
- PWM3 mode — Output PWM waveform (2) with same period

In the input capture function, output compare function and PWM mode, Channels 0 and 1 have the equivalent functions, and functions or modes can be selected every pin. Also, a combination of these functions and modes can be used in 1 channel.
In reset synchronous PWM mode, complementary PWM mode and PWM3 mode, a waveform is output with a combination of counters and registers in Channels 0 and 1.

Tables 14.12 to 14.20 lists the Pin Functions of timer RD.

Table 14.12 Pin Functions TRDIOA0/TRDCLK(P2_0)

Register	TRDOER1	TRDFCR			TRDIORA0		Function
Bit	EA0	PWM3	STCLK	CMD1, CMD0	IOA3	IOA2_IOA0	
Setting value	0	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	0	00b	1	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	0	00b	X	1XXb	Timer mode trigger input (input capture function)(1)
		1	1	XXb	X	000b	External clock input (TRDCLK)(1)
	Other than above						I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_0 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function) and external clock input (TRDCLK).

Table 14.13 Pin Functions TRDIOB0(P2_1)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA0	Function
Bit	EB0	PWM3	CMD1, CMD0	PWMB0	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_1 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.14 Pin Functions TRDIOC0(P2_2)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	EC0	PWM3	CMD1, CMD0	PWMC0	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_2 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.15 Pin Functions TRDIOD0(P2_3)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	ED0	PWM3	CMD1, CMD0	PWMD0	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_3 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.16 Pin Functions TRDIOA1(P2_4)

Register	TRDOER1	TRDFCR		TRDIORA1	Function
Bit	EA1	PWM3	CMD1, CMD0	IOA2_IOA0	
Setting value	0	X	1Xb	XXXb	Complementary PWM mode waveform output
	0	X	01b	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above				I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_4 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.17 Pin Functions TRDIOB1(P2_5)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA1	Function
Bit	EB1	PWM3	CMD1, CMD0	PWMB1	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_5 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.18 Pin Functions TRDIOC1(P2_6)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	EC1	PWM3	CMD1, CMD0	PWMC1	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_6 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.19 Pin Functions TRDIOD1(P2_7)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	ED1	PWM3	CMD1, CMD0	PWMD1	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_7 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.20 Pin Functions $\overline{\text{INT0}}$(P4_5)

Register	TRDOER2	INTEN		PD4	Function
Bit	PTO	INT0PL	INT0EN	PD4_5	
Setting value	1	0	1	0	Pulse output forced cutoff signal input
	Other than above				I/O port or $\overline{\text{INT0}}$ interrupt input

X: can be 0 or 1, no change in outcome

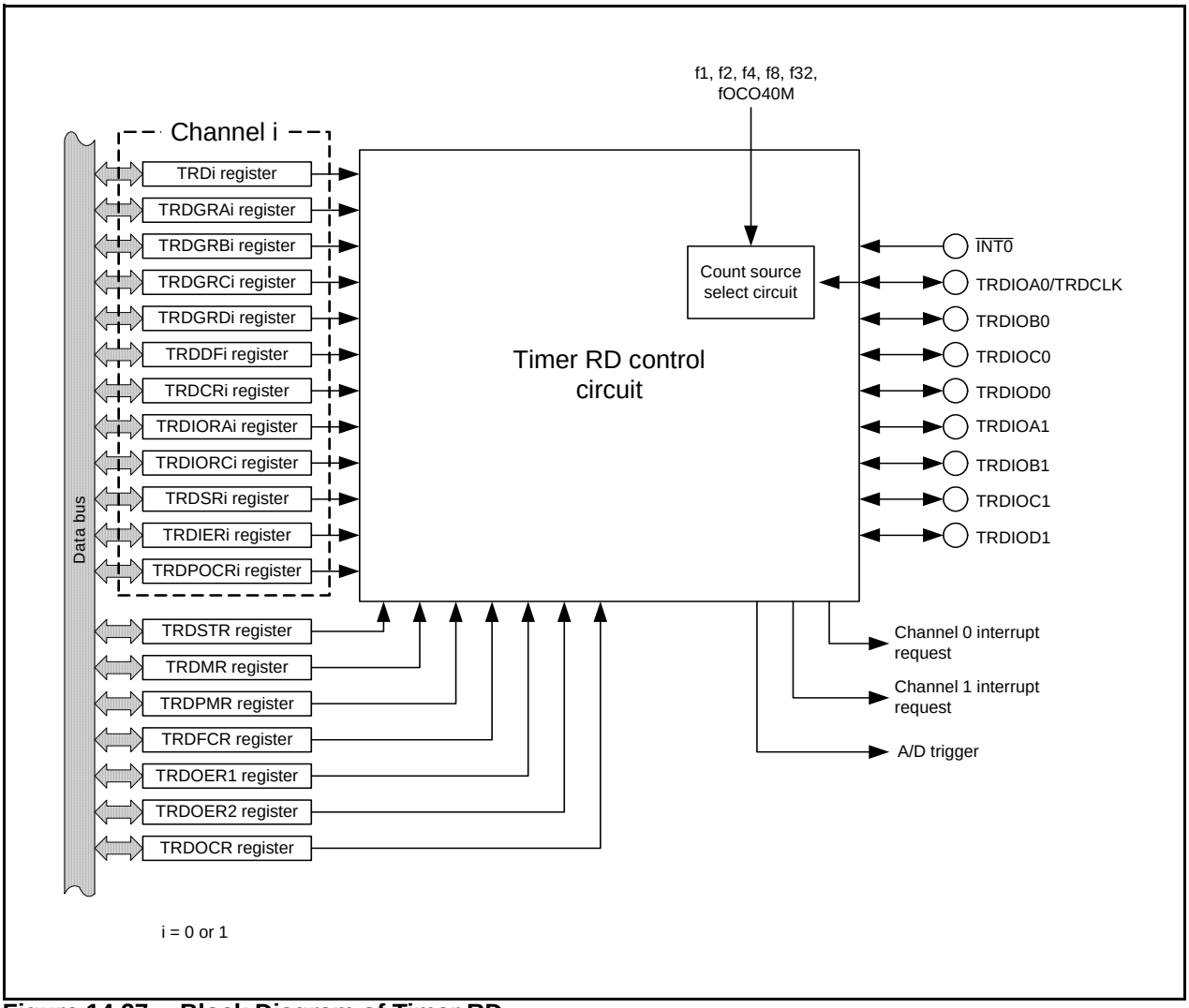


Figure 14.27 Block Diagram of Timer RD

14.3.1 Count Source

The count source selection can be used in all modes. However, in PWM3 mode, the external clock cannot be selected.

Table 14.21 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in the TRDCRi register.
fOCO40M(1)	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator frequency). Bits TCK2 to TCK0 in the TRDCRi register is set to 110b (fOCO40M).
External Signal Input to TRDCLK Pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). The TCK2 to TCK0 bits in the TRDCRi register are set to 101b (count source: external clock). The valid edge selected by the CKEG1 to CKEG0 bits in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

NOTE:

1. The count source fOCO40M can be used with VCC = 3.0 to 5.5 V.

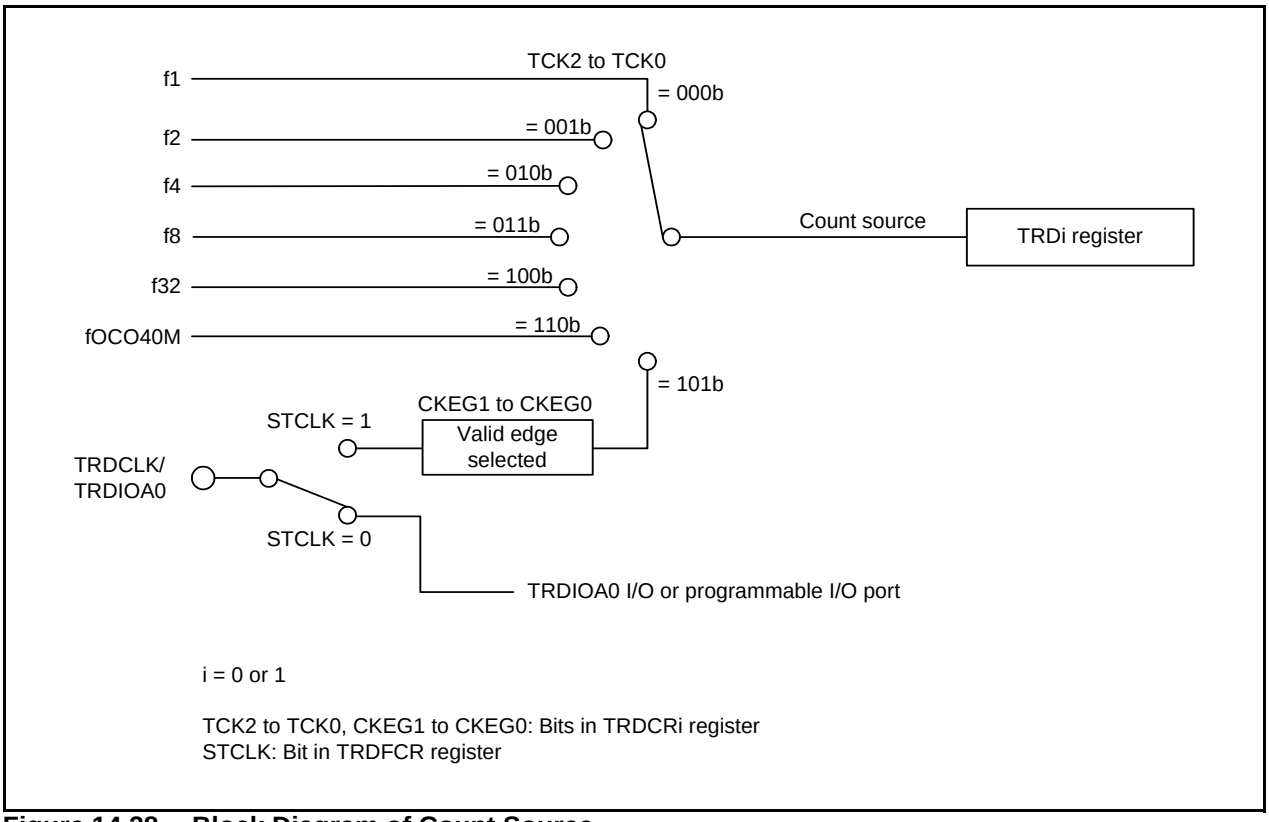


Figure 14.28 Block Diagram of Count Source

Set the pulse width of the external clock which inputs to the TRDCLK pin to 3 cycles or above of the operation clock of Timer RD (refer to **Table 14.11 Timer RD Operation Clocks**).

When selecting fOCO40M for the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting the TCK2 to TCK0 bits in the TRDCRi register (i = 0 or 1) to 110b (fOCO40M).

14.3.2 Buffer Operation

The TRDGRCi register can be used as the buffer register of the TRDGRAi register, and the TRDGRDi register can be used as the buffer register of the TRDGRBi register by the BFCi and BFDi bits in the TRDMR register.

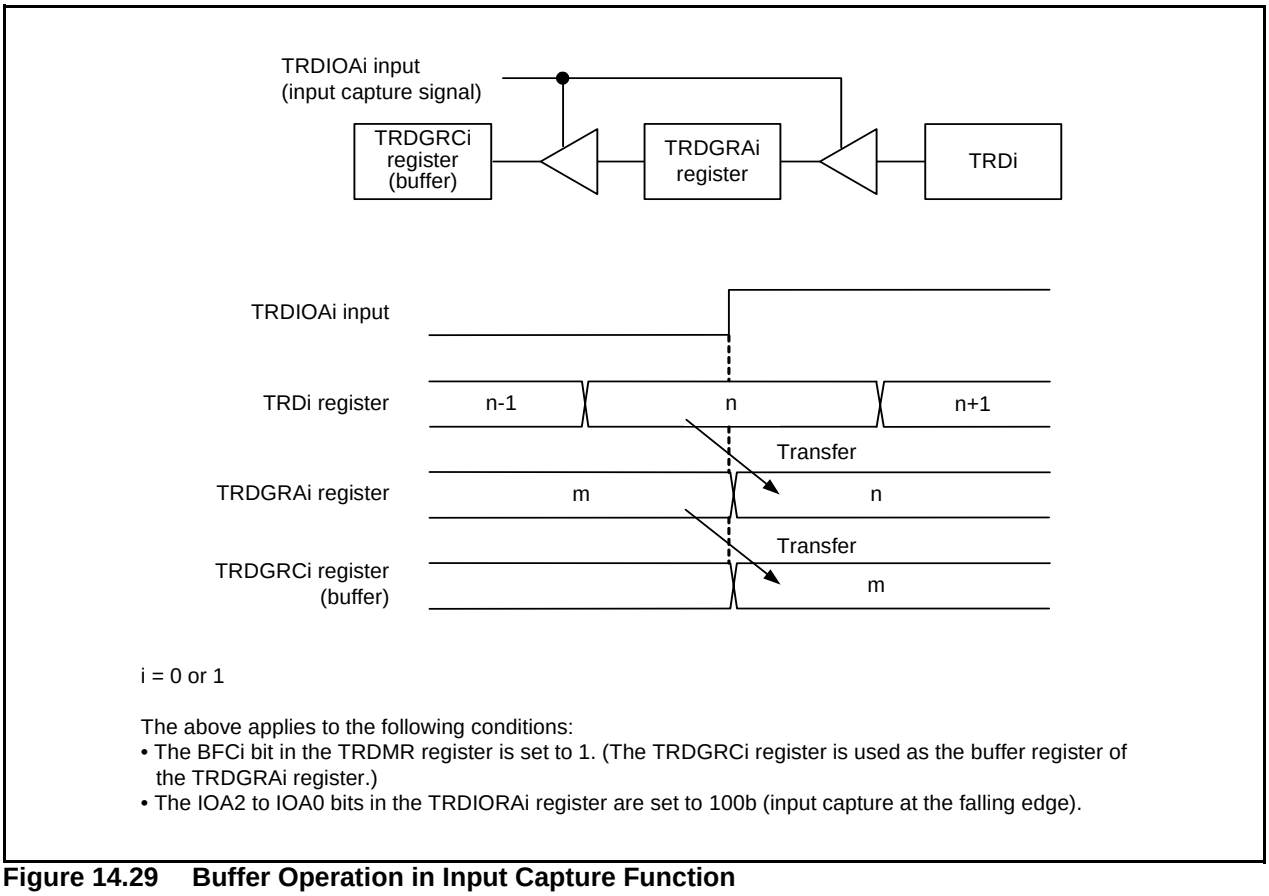
- TRDGRAi buffer register: TRDGRCi register
- TRDGRBi buffer register: TRDGRDi register

Buffer operation depends on modes. Table 14.22 lists the Buffer Operation in Each Mode.
Figure 14.29 shows the Buffer Operation in Input Capture Function, and Figure 14.30 shows the Buffer Operation in Output Compare Function.

Table 14.22 Buffer Operation in Each Mode

Function and Mode	Transfer Timing	Transfer Register
Input Capture Function	Input capture signal input	Transfer content in TRDGRAi (TRDGRBi) register to buffer register
Output Compare Function PWM Mode	Compare match with TRDi register and TRDGRAi (TRDGRBi) register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Reset Synchronous PWM Mode	Compare match withTRD0 register and TRDGRA0 register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Complementary PWM Mode	• Compare match with TRD0 register and TRDGRA0 register • TRD1 register underflow	Transfer content in buffer register to TRDGRB0, TRDGRA1 and TRDGRB1 registers
PWM3 Mode	Compare match with TRD0 register and TRDGRA0 register	Transfer content in buffer register to TRDGRA0, TRDGRB0, TRDGRA1 and TRDGRB1 registers

i = 0 or 1



i = 0 or 1

The above applies to the following conditions:
- The BFCi bit in the TRDMR register is set to 1. (The TRDGRCi register is used as the buffer register of the TRDGRAi register.)
- The IOA2 to IOA0 bits in the TRDIORAi register are set to 100b (input capture at the falling edge).

Figure 14.29 Buffer Operation in Input Capture Function

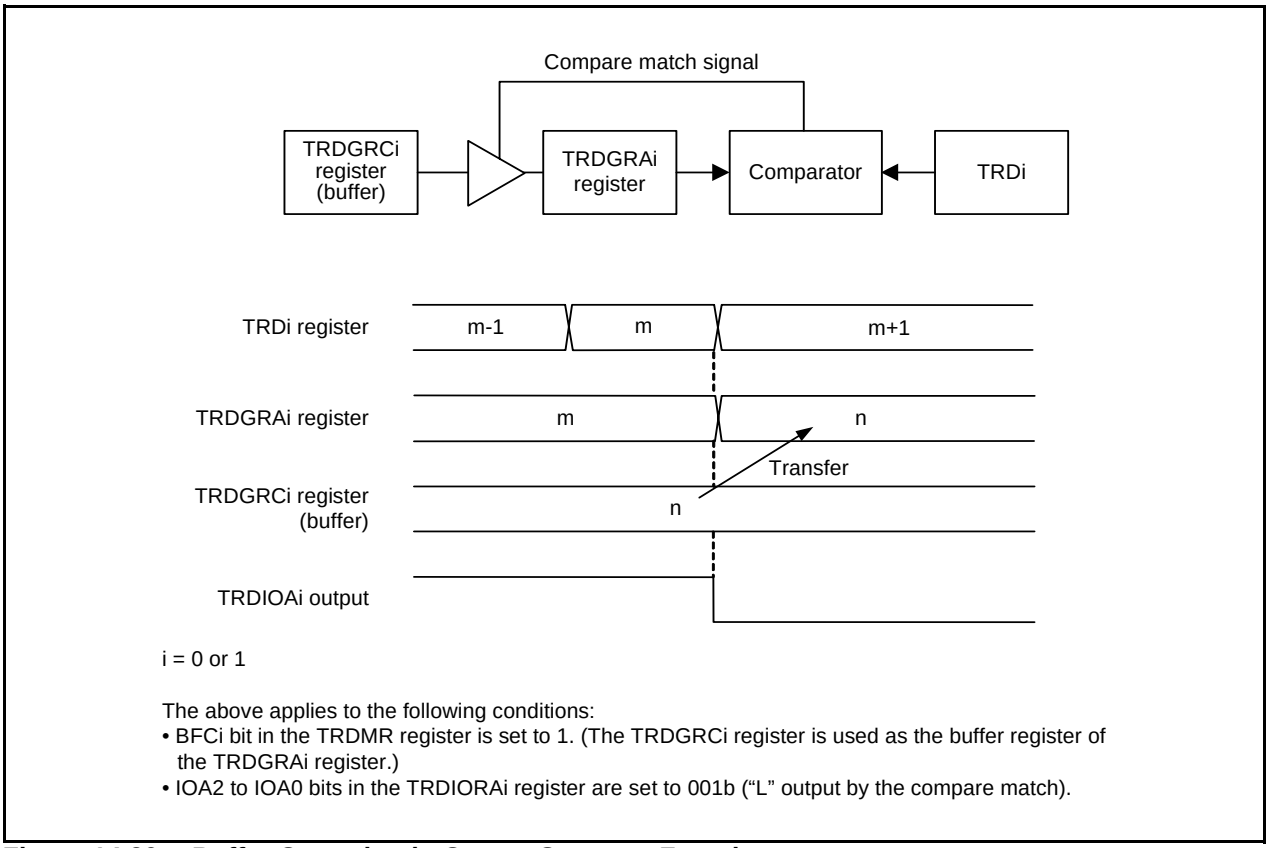


Figure 14.30 Buffer Operation in Output Compare Function

Perform the following for the timer mode (input capture and output compare functions).
When using the TRDGRCi (i = 0 or 1) register as the buffer register of the TRDGRAi register

- Set the IOC3 bit in the TRDIORCi register to 1 (general register or buffer register).
- Set the IOC2 bit in the TRDIORCi register to the same as the IOA2 bit in the TRDIORAi register.

When using the TRDGRDi register as the buffer register of the TRDGRBi register

- Set the IOD3 bit in the TRDIORDi register to 1 (general register or buffer register).
- Set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

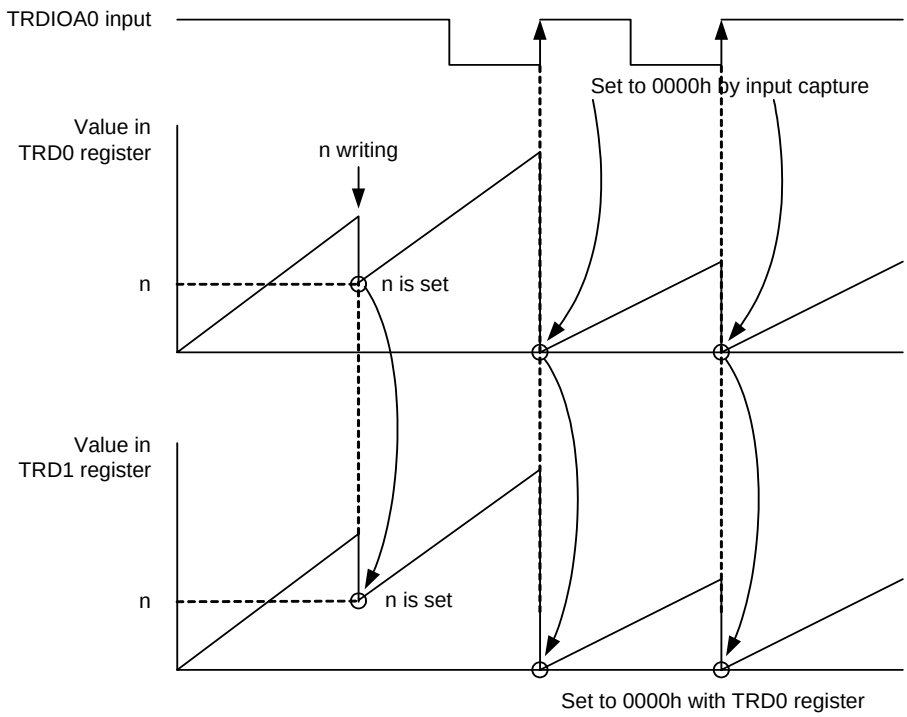
Bits IMFC and IMFD in the TRDSRi register are set to 1 at the input edge of the TRDIOCi pin when also using registers TRDGRCi and TRDGRDi as the buffer register in the input capture function.

When using the TRDGRCi and TRDGRDi registers for the buffer register in output compare function, reset synchronous PWM mode, complementary PWM mode and PWM3 mode, the IMFC and IMFD bits in the TRDSRi register are set to 1 by the compare match with the TRDi register.

14.3.3 Synchronous Operation

The TRD1 register is synchronized with the TRD0 register.

- Synchronous preset
  When the SYNC bit in the TRDMR register is set to 1 (synchronous operation), the data is written to both the TRD0 and TRD1 registers after writing to the TRDi register.
- Synchronous clear
  When the SYNC bit in the TRDMR register is set to 1 and the CCLR2 to CCLR0 bits in the TRDCRi register are set to 011b (synchronous clear), and the TRD0 register is set to 0000h at the same time as the TRD1 register is set to 0000h.
  Also, when the SYNC bit in the TRDMR register is set to 1 and the CCLR2 to CCLR0 bits in the TRDCRi register are set to 011b (synchronous clear), and the TRD1 register is set to 0000h at the same time as the TRD0 register is set to 0000h.



The above applies to the following conditions:

- The SYNC bit in the TRDMR register is set to 1 (synchronous operation).
- The CCLR2 to CCLR0 bits in the TRDCR0 register are set to 001b (set the TRD0 register to 0000h in input capture).
  The CCLR2 to CCLR0 bits in the TRDCR1 register are set to 011b.
  (Set the TRD1 register to 0000h synchronizing with the TRD0 register.)
- The IOA2 to IOA0 bits in the TRDIORA0 register are set to 100b.
- The CMD1 to CMD0 bits in the TRDFCR register are set to 00b.
  The PWM 3 bit in the TRDFCR register is set to 1.

} (Input capture at the rising edge of the TRDIOA0 input)

Figure 14.31 Synchronous Operation

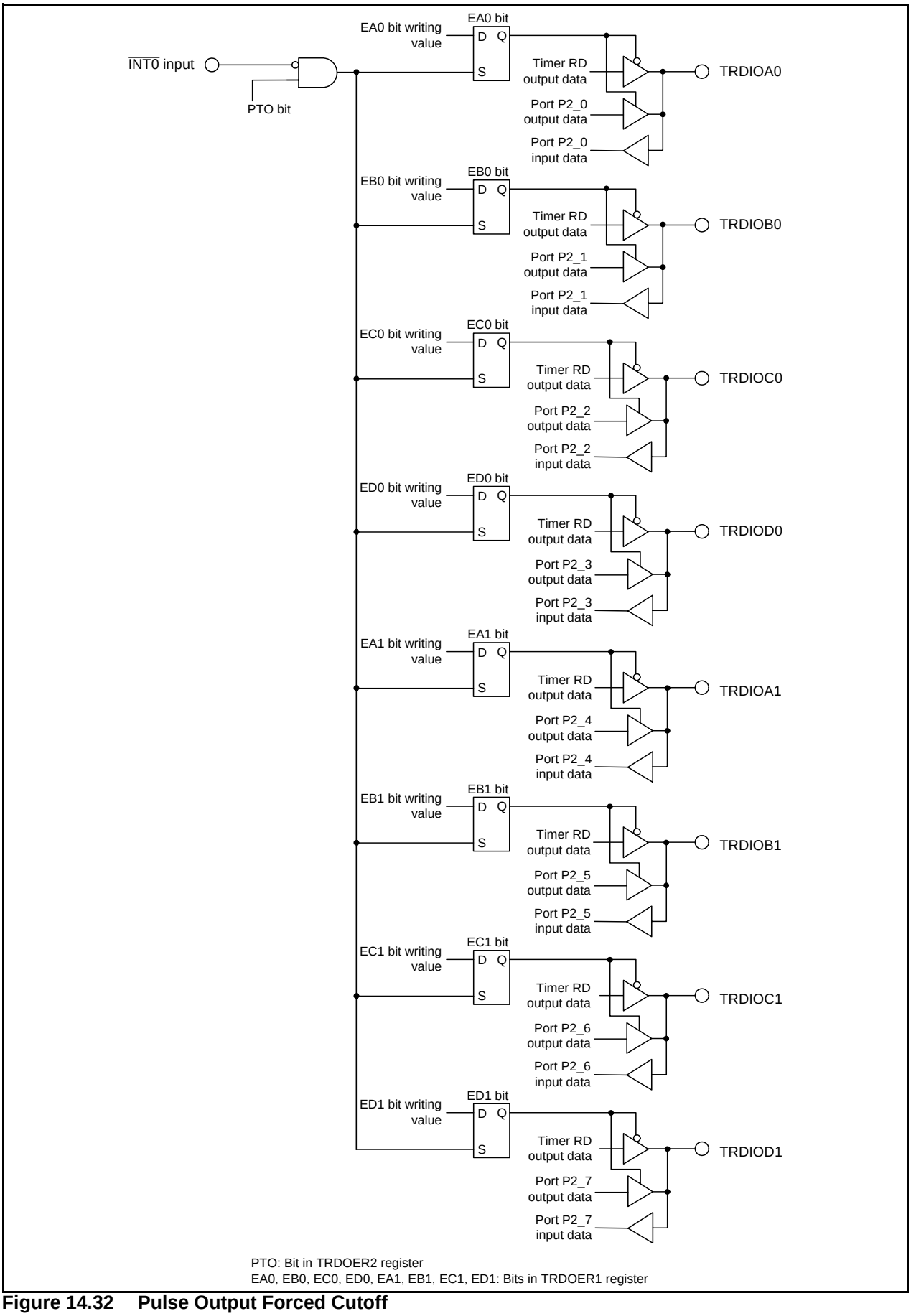
14.3.4 Pulse Output Forced Cutoff

In the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode and PWM3 mode, the TRDIOji output pin can be forcibly set to the programmable I/O port by the $\overline{\text{INT0}}$ pin input, and pulse output can be cut off.
The used pins for the output in these functions or modes can function as the output pin of Timer RD when setting the applicable bit in the TRDOER1 register to 0 (enable Timer RD output). When the PTO bit in the TRDOER2 register to 1 ($\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled), all bits in the TRDOER1 register are set to 1 (disable Timer RD output, the TRDIOji output pin is used as the programmable I/O port) after "L" is applied to the $\overline{\text{INT0}}$ pin. The TRDIOji output pin is set to the programmable I/O port after "L" is applied to the $\overline{\text{INT0}}$ pin and waiting for 1 to 2 cycles of the Timer RD operation clock (refer to **Table 14.11 Timer RD Operation Clocks**).

Set as below when using this function:

- Set the pin status (high impedance, "L" or "H" output) with the pulse output forced cutoff by the P2 and PD2 registers.
- Set the INT0EN bit in the INTEN register to 1 (enable $\overline{\text{INT0}}$ input) and the INT0PL bit to 0 (one edge).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Set the $\overline{\text{INT0}}$ digital filter by the INT0F1 to INT0F0 bits in the INTF register.
- Set the PTO bit in the TRDOER2 register to 1 (enable pulse output forced cutoff signal input $\overline{\text{INT0}}$).

According to the selection of the POL bit in the INT0IC register and change of the $\overline{\text{INT0}}$ pin input, the IR bit in the INT0IC register is set to 1 (interrupt request). Refer to **12. Interrupts** for details of interrupts.

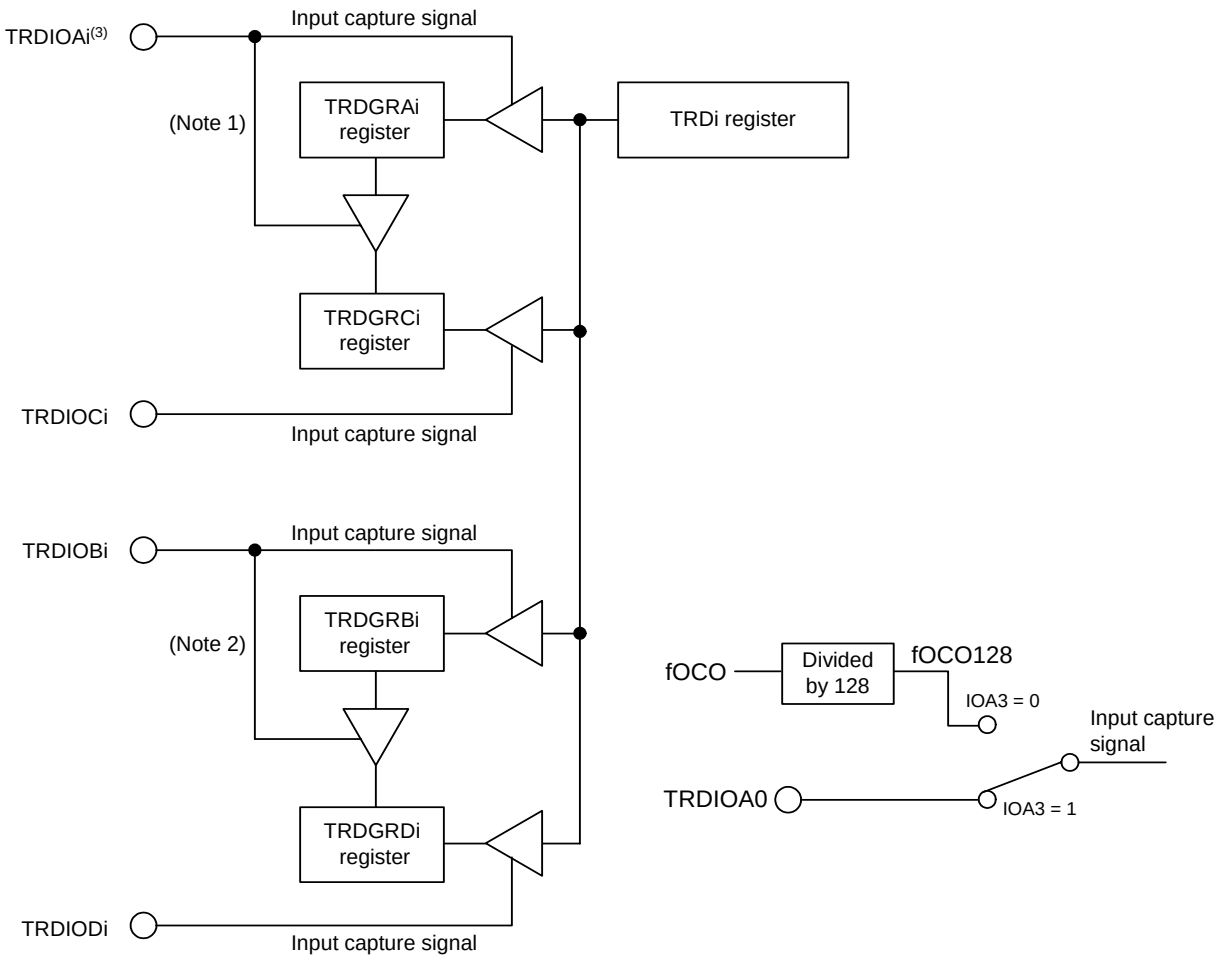


PTO: Bit in TRDOER2 register
EA0, EB0, EC0, ED0, EA1, EB1, EC1, ED1: Bits in TRDOER1 register

Figure 14.32 Pulse Output Forced Cutoff

14.3.5 Input Capture Function

The input capture function is to measure the external signal width and period. The content in the TRDi register (counter) is transferred to the TRDGRji register as a trigger of the TRDIOji (i = 0 or 1, j = either A, B, C or D) pin external signal (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, any of the input capture function, other modes or functions can be selected every pin.
The TRDGRA0 register can also select fOCO128 signal as input-capture trigger input.
Figure 14.33 shows the Block Diagram of Input Capture Function, Table 14.23 lists the Input Capture Function Specifications. Figures 14.34 to 14.44 show the Registers Associated with Input Capture Function and Figure 14.45 shows the Operating Example of Input Capture Function.



i = 0 or 1

NOTES:
1. When the BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).
2. When the BFDi bit in the TRDMR register is set to 1 (the TRDGRDi register is used as the buffer register of the TRDGRBi register).
3. The trigger input of the TRDGRA0 register can select the TRDIOA0 pin input or fOCO128 signal.

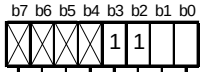
Figure 14.33 Block Diagram of Input Capture Function

Table 14.23 Input Capture Function Specifications

Item	Specification
Count Sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count Operations	Increment
Count Period	When the CCLR2 to CCLR0 bits in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source
Count Start Condition	Write 1 (count starts) to the TSTARTi bit in the TRDSTR register.
Count Stop Condition	Write 0 (count stops) to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt Request Generation Timing	• Input capture (valid edge of TRDIOji input or fOCO128 signal edge) • TRDi register overflows
TRDIOA0 Pin Function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 Pin Functions	Programmable I/O port, or input-capture input (Select every pin)
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read by reading the TRDi register.
Write to Timer	• When the SYNC bit in the TRDMR register is set to 0 (channels 0 and 1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (channels 0 and 1 operate synchronously.) Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selection Functions	• Input-capture input pin selected Either 1 pin or multiple pins of the TRDIOAi, TRDIOBi, TRDIOCi or TRDIODi pin. • Input-capture input valid edge selected The rising edge, falling edge or both the rising and falling edges • The timing when the TRDi register is set to 0000h At overflow or input capture • Buffer operation (refer to **14.3.2 Buffer Operation**) • Synchronous operation (refer to **14.3.3 Synchronous Operation**) • Digital filter The TRDIOji input is sampled, and when the sampled input level match 3 times, its level is assumed as a determination. • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRDGRA0 register.

i = 0 or 1, j = either A, B, C or D

Timer RD Start Register(1)

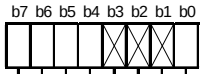


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag	0 : Count stops 1 : Count starts	RW
TSTART1	TRD1 count start flag	0 : Count stops 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	Set to 1 in the input capture function	RW
CSEL1	TRD1 count operation select bit	Set to 1 in the input capture function	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTE:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD.**

Timer RD Mode Register

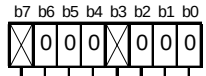


Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0 : TRD0 and TRD1 registers operate independently 1 : TRD0 and TRD1 registers operate synchronously	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function selection bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function selection bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function selection bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function selection bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.34 Registers TRDSTR and TRDMR in Input Capture Function

Timer RD PWM Mode Register



Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 selection bit	Set to 0 (timer mode) in the input capture function.	RW
PWMC0	PWM mode of TRDIOC0 selection bit	Set to 0 (timer mode) in the input capture function.	RW
PWMD0	PWM mode of TRDIOD0 selection bit	Set to 0 (timer mode) in the input capture function.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 selection bit	Set to 0 (timer mode) in the input capture function.	RW
PWMC1	PWM mode of TRDIOC1 selection bit	Set to 0 (timer mode) in the input capture function.	RW
PWMD1	PWM mode of TRDIOD1 selection bit	Set to 0 (timer mode) in the input capture function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.35 TRDPMR Register in Input Capture Function

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

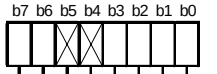
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode selection bit(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the input capture function.	RW
CMD1			RW
OLS0	Normal-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	RW
OLS1	Counter-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in the input capture function.	RW
ADEG	A/D trigger edge selection bit (in complementary PWM mode)	This bit is disabled in the input capture function.	RW
STCLK	External clock input selection bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode selection bit(2)	Set this bit to 1 (other than PWM3 mode) in the input capture function.	RW

NOTES:
1. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.36 TRDFCR Register in Input Capture Function

Timer RD Digital Filter Function Selection Register i (i = 0 or 1)



Symbol	Address	After Reset
TRDDF0	013Eh	00h
TRDDF1	013Fh	00h

Bit Symbol	Bit Name	Function	RW
DFA	TRDIOA pin digital filter function selection bit	0 : Function is not used 1 : Function is used	RW
DFB	TRDIOB pin digital filter function selection bit	0 : Function is not used 1 : Function is used	RW
DFC	TRDIOC pin digital filter function selection bit	0 : Function is not used 1 : Function is used	RW
DFD	TRDIOD pin digital filter function selection bit	0 : Function is not used 1 : Function is used	RW
— (b5 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
DFCK0	Clock selection bit for digital filter function	b7 b6 0 0 : f32 0 1 : f8 1 0 : f1 1 1 : Count source (clock selected by the TCK2 to TCK0 bits in the TRDCRi register)	RW
DFCK1			RW

Figure 14.37 Registers TRDDF0 to TRDDF1 in Input Capture Function

Timer RD Control Register i (i = 0 or 1)

b7 b6 b5 b4 b3 b2 b1 b0

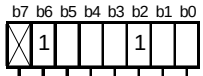
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source selection bit	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge selection bit(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set	RW
CKEG1			RW
CCLR0	TRDi counter clear selection bit	b7 b6 b5 0 0 0 : Disable clear (free-running operation) 0 0 1 : Clear by the input capture in the TRDGRAi register 0 1 0 : Clear by the input capture in the TRDGRBi register 0 1 1 : Synchronous clear (clear simultaneously with other channel counter)(3) 1 0 0 : Do not set 1 0 1 : Clear by the input capture in the TRDGRCi register 1 1 0 : Clear by the input capture in the TRDGRDi register 1 1 1 : Do not set	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This bit is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. This bit is enabled when the TCK2 to TCK0 bits are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This bit is enabled when the SYNC bit in the TRDMR register is set to 1 (TRD0 and TRD1 registers operate synchronously).

Figure 14.38 Registers TRDCR0 to TRDCR1 in Input Capture Function

Timer RD I/O Control Register Ai (i = 0 or 1)



Symbol	Address	After Reset
TRDIORA0	0141h	10001000b
TRDIORA1	0151h	10001000b

Bit Symbol	Bit Name	Function	RW
IOA0	TRDGRA control bit	b1 b0 0 0 : Input capture to the TRDGRAi register at the rising edge 0 1 : Input capture to the TRDGRAi register at the falling edge 1 0 : Input capture to the TRDGRAi register at both edges 1 1 : Do not set	RW
IOA1			RW
IOA2	TRDGRA mode selection bit(1)	Set to 1 (input capture) in the input capture function	RW
IOA3	Input capture input switch bit(3,4)	0 : fOCO128 Signal 1 : TRDIOA0 pin	RW
IOB0	TRDGRB control bit	b5 b4 0 0 : Input capture to the TRDGRBi register at the rising edge 0 1 : Input capture to the TRDGRBi register at the falling edge 1 0 : Input capture to the TRDGRBi register at both edges 1 1 : Do not set	RW
IOB1			RW
IOB2	TRDGRB mode selection bit(2)	Set to 1 (input capture) in the input capture function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. When selecting 1 (The TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. When selecting 1 (The TRDGRDi register is used as a buffer register of TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.
3. The IOA3 bit in the only TRDIORA0 register is enabled. Set to the IOA3 bit in the TRDIORA1 to 1.
4. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

Figure 14.39 Registers TRDIORA0 to TRDIORA1 in Input Capture Function

Timer RD I/O Control Register Ci (i = 0 or 1)

b7	b6	b5	b4	b3	b2	b1	b0
1	1			1	1		

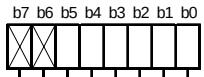
Symbol	Address	After Reset
TRDIORC0	0142h	10001000b
TRDIORC1	0152h	10001000b

Bit Symbol	Bit Name	Function	RW
IOC0	TRDGRC control bit	b1 b0 0 0 : Input capture to the TRDGRCi register at the rising edge 0 1 : Input capture to the TRDGRCi register at the falling edge 1 0 : Input capture to the TRDGRCi register at both edges 1 1 : Do not set	RW
IOC1			RW
IOC2	TRDGRC mode selection bit(1)	Set to 1 (input capture) in the input capture function	RW
IOC3	TRDGRC register function selection bit	Set to 1 (general register or buffer register) in the input capture function	RW
IOD0	TRDGRD control bit	b5 b4 0 0 : Input capture to the TRDGRDi register at the rising edge 0 1 : Input capture to the TRDGRDi register at the falling edge 1 0 : Input capture to the TRDGRDi register at both edges 1 1 : Do not set	RW
IOD1			RW
IOD2	TRDGRD mode selection bit(2)	Set to 1 (input capture) in the input capture function	RW
IOD3	TRDGRD register function selection bit	Set to 1 (general register or buffer register) in the input capture function	RW

NOTES:
1. When selecting 1 (The TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. When selecting 1 (The TRDGRDi register is used as a buffer register of TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

Figure 14.40 Registers TRDIORC0 to TRDIORC1 in Input Capture Function

Timer RD Status Register i (i = 0 or 1)



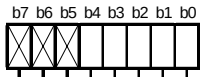
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] TRDSR0 register: fOCO128 signal edge when the IOA3 bit in the TRDIORA0 register is set to 0 (fOCO128 signal) TRDIOA0 pin input edge when the IOA3 bit in the TRDIORA0 register is set to 1 (TRDIOA0 input)(3) TRDSR1 register: Input edge of TRDIOA1 pin.(3)	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] Input edge of TRDIOBi pin.(3)	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] Input edge of TRDIOCi pin.(4)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] Input edge of TRDIODi pin.(4)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the TRDi register overflows	RW
UDF	Underflow flag(1)	This bit is disabled in the input capture function.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to the b5 in the TRDSR0 register. When writing to the b5, write 0. When reading, its content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and writing 0 to the same bit.
   - This bit remains unchanged even if the read result is 0 and writing 0 to the same bit. (This bit remains 1 even if this bit is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged when writing 1.
3. Edge selected by bits IOj1 to IOj0 (j = A or B) in the TRDIORAi register.
4. Edge selected by bits IOk1 to IOk0 (k = C or D) in the TRDIORCi register.
   Including when the BFki bit in the TRDMR register is set to 1 (TRDGRki is used as the buffer register).

Figure 14.41 Registers TRDSR0 to TRDSR1 in Input Capture Function

Timer RD Interrupt Enable Register i (i = 0 or 1)

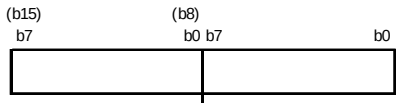


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable an interrupt (IMIA) by the IMFA bit 1 : Enable an interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable an interrupt (IMIB) by the IMFB bit 1 : Enable an interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable an interrupt (IMIC) by the IMFC bit 1 : Enable an interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable an interrupt (IMID) by the IMFD bit 1 : Enable an interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable an interrupt (OVI) by the OVF bit 1 : Enable an interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.42 Registers TRDIER0 to TRDIER1 in Input Capture Function

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 14.43 Registers TRD0 to TRD1 in Input Capture Function

Timer RD General Register Ai, Bi, Ci and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.24 TRDGRji Register Functions in Input Capture Function**	RW

NOTE:
1. Access the TRDGRAi to TRDGRDi registers in 16-bit units. Do not access them in 8-bit units.

Figure 14.44 Registers TRDGRAi, TRDGRBi, TRDGRCi and TRDGRDi in Input Capture Function

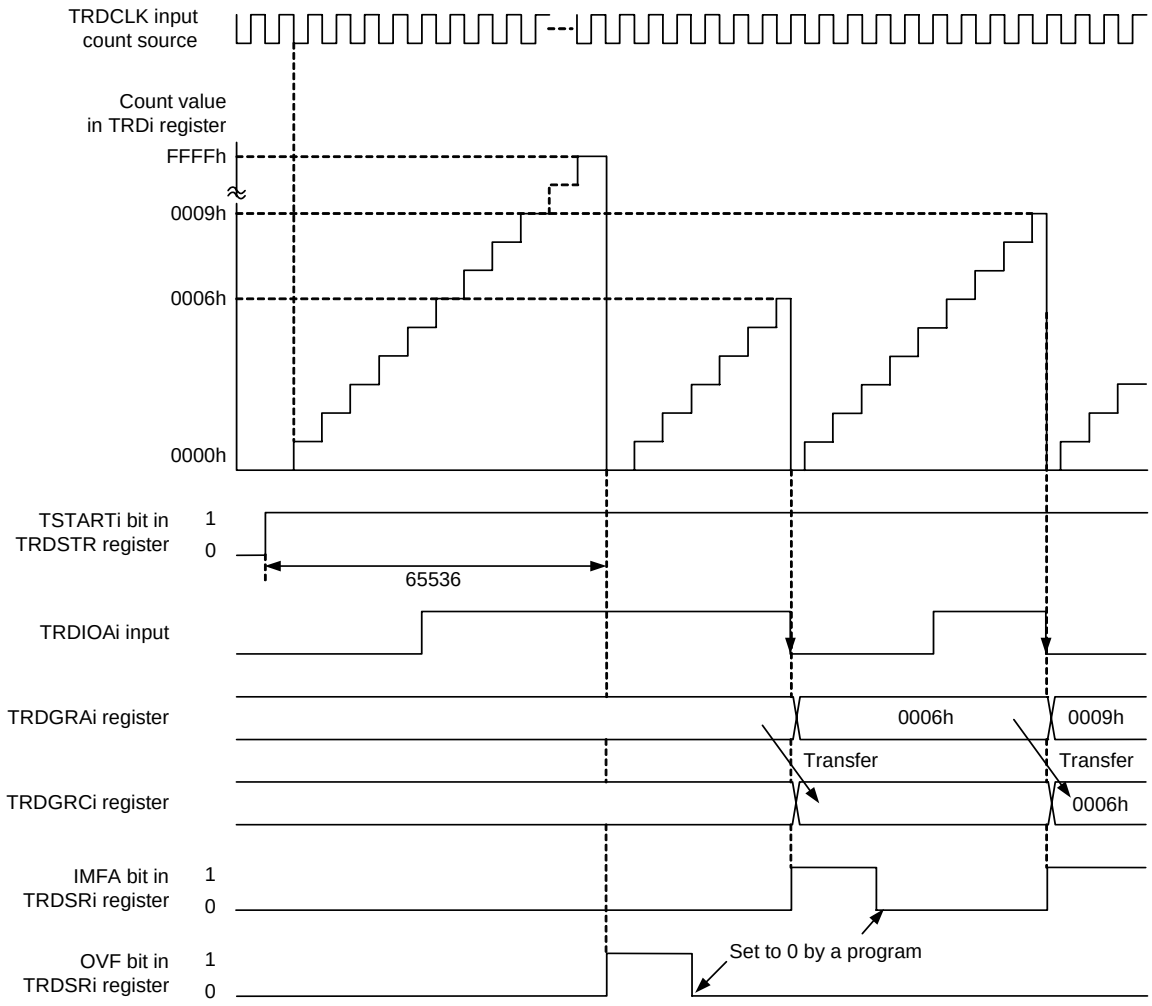
The following registers are disabled in the input capture function:
TRDOER1, TRDOER2, TRDOCR, TRDPOCR0 and TRDPOCR1

Table 14.24 TRDGRji Register Functions in Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRAi	–	General register The value in the TRDi register can be read at the input capture.	TRDIOAi
TRDGRBi			TRDIOBi
TRDGRCi	BFCi = 0	General register The value in the TRDi register can be read at the input capture.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register The value in the TRDi register can be read at the input capture. (Refer to **14.3.2 Buffer Operation**)	TRDIOAi
TRDGRDi	BFDi = 1		TRDIOBi

i = 0 or 1, j = either A, B, C or D
BFCi, BFDi: Bits in TRDMR Register

Set the pulse width of the input capture signal applied to the TRDIOji pin to 3 cycles or more of the Timer RD operation clock (refer to **Table 14.11 Timer RD Operation Clocks**) for “no digital filter” (the DFj bit in the TRDDFi register is set to 0).



i = 0 or 1

The above applies to the following conditions:
The CCLR2 to CCLR0 bits in the TRDCRi register are set to 001b. (Set the TRDi register to 0000h by the TRDGRAi register input capture.)
The TCK2 to TCK0 bits in the TRDCRi register are set to 101b (TRDCLK input for the count source).
The CKEG1 to CKEG0 bits in the TRDCRi register are set to 01b (count at the falling edge for the count source).
The IOA2 to IOA0 bits in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1. (The TRDGRCi register is used as the buffer register of the TRDGRAi register.)

Figure 14.45 Operating Example of Input Capture Function

14.3.5.1 Digital Filter

The TRDIOji input is sampled, and when the sampled input level matches 3 times, its level is assumed as a determination. Select the digital filter function and sampling clock by the TRDDFi register.

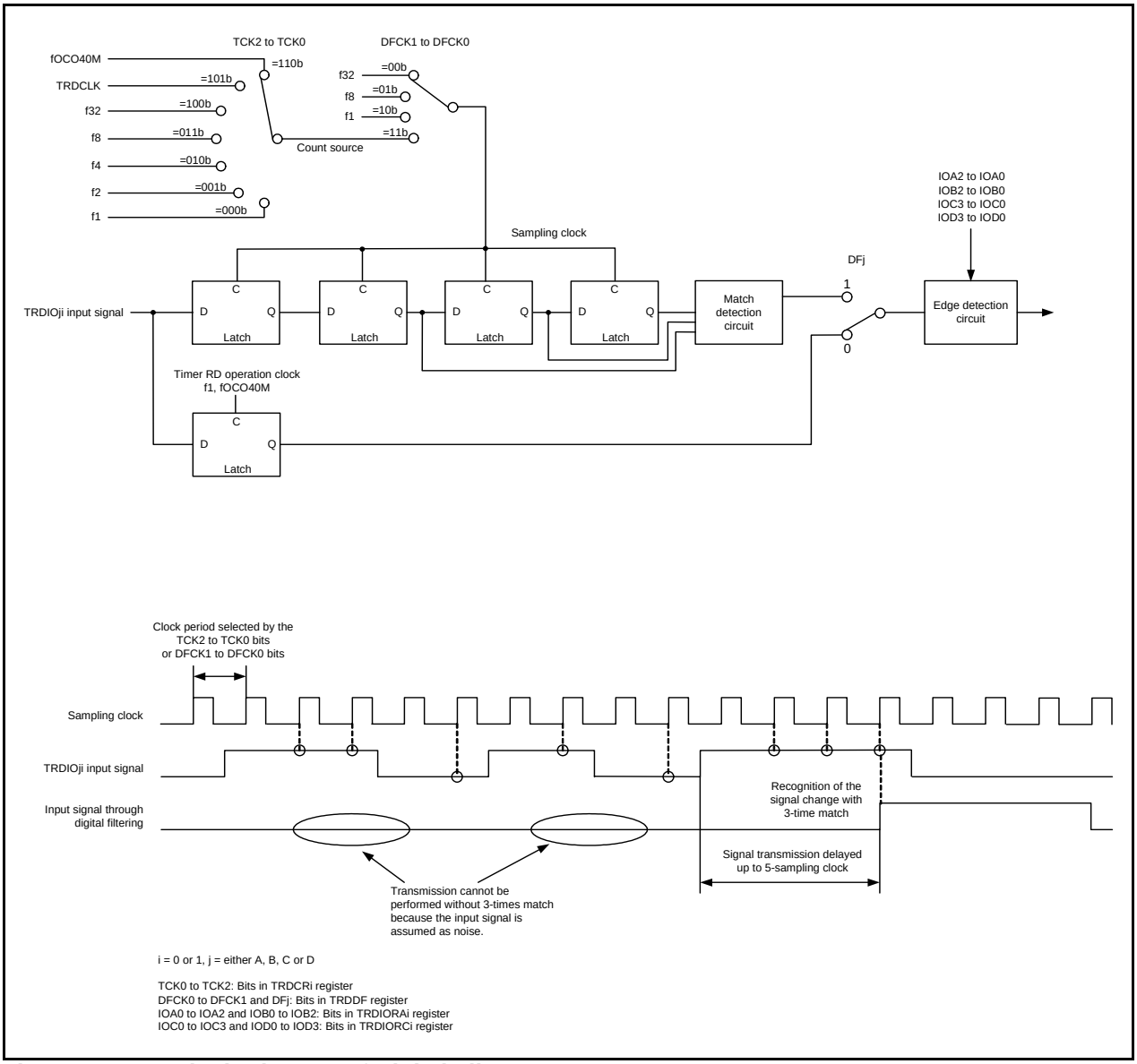


Figure 14.46 Block Diagram of Digital Filter

14.3.6 Output Compare Function

This function is to detect the match (compare match) of the content in the TRDGRji (j = either A, B, C and D) register with the content in the TRDi (i = 0 or 1) register. When the content matches, any level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, any of the output compare function, other modes or functions can be selected every pin.
Figure 14.47 shows the Block Diagram of Output Compare Function, Table 14.25 lists the Output Compare Function Specifications. Figures 14.48 to 14.59 list the Registers Associated with Output Compare Function and Figure 14.60 shows the Operating Example of Output Compare Function.

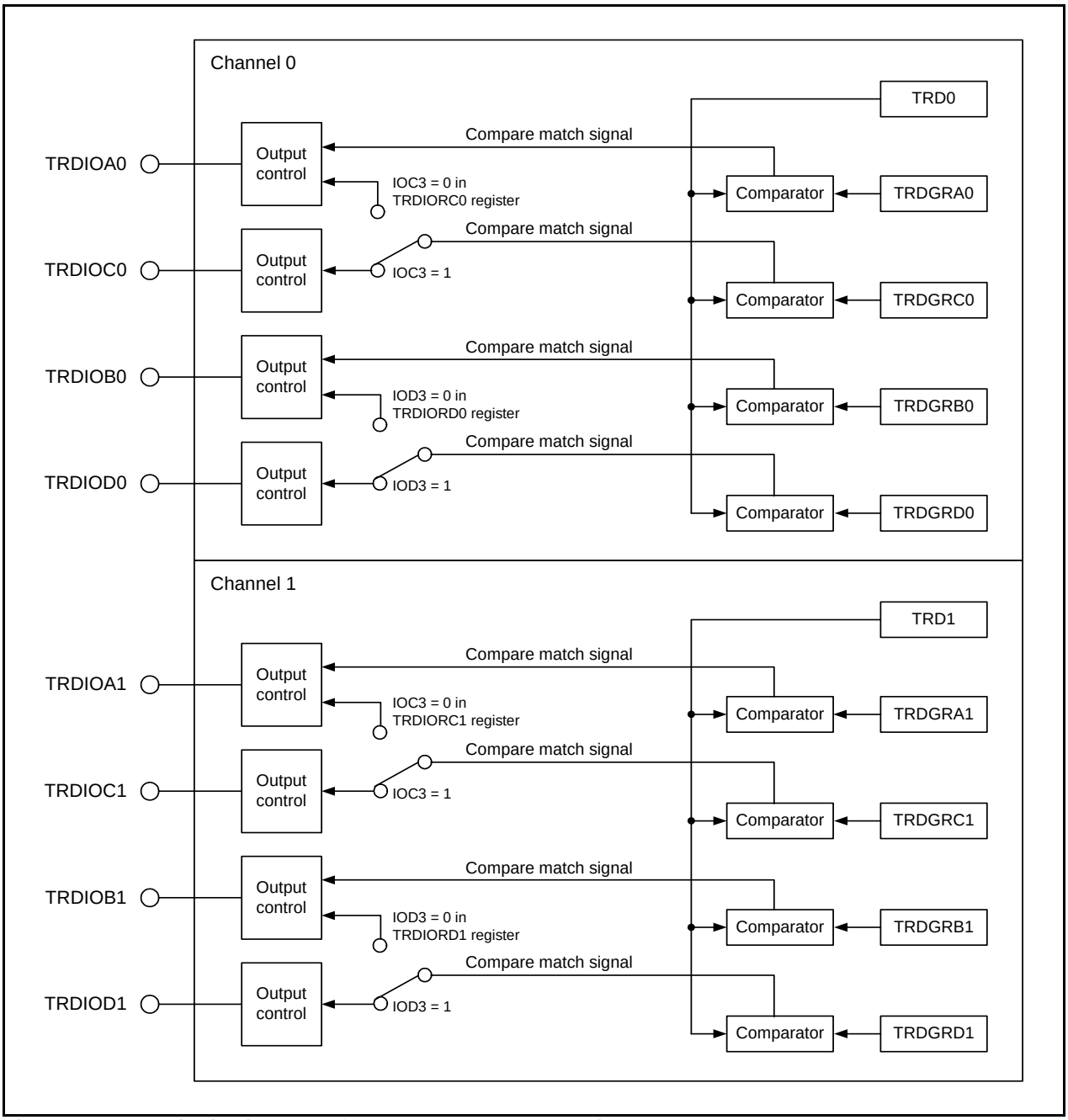


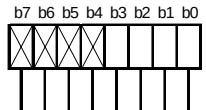
Figure 14.47 Block Diagram of Output Compare Function

Table 14.25 Output Compare Function Specifications

Item	Specification
Count Sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count Operations	Increment
Count Period	• When the CCLR2 to CCLR0 bits in the TRDCRi register are set to 000b (free-running operation) 1/fk × 65536 fk: Frequency of count source • The CCLR1 to CCLR0 bits in the TRDCRi register are set to 01b or 10b (set the TRDi register to 0000h at the compare match in the TRDGRji register.) Frequency of count source x (n + 1) n: Setting value in the TRDGRji register
Waveform Output Timing	Compare match
Count Start Condition	Write 1 (count starts) to the TSTARTi bit in the TRDSTR register.
Count Stop Conditions	• Write 0 (count stops) to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output compare output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The output compare output pin holds level after output change by the compare match.
Interrupt Request Generation Timing	• Compare match (the content in the TRDi register matches with the content in the TRDGRji register.) • TRDi register overflows
TRDIOA0 Pin Function	Programmable I/O port, output-compare output or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 Pin Functions	Programmable I/O port or output-compare output (select every pin)
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read by reading the TRDi register.
Write to Timer	• When the SYNC bit in the TRDMR register is set to 0 (channels 0 and 1 operate independently) Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (channels 0 and 1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selection Functions	• Output-compare output pin selected Either 1 pin or multiple pins of the TRDIOAi, TRDIOBi, TRDIOCi or TRDIODi pin. • Output level at the compare match selected “L” output, “H” output or output level inversed • Initial output level selected Set the level at period from the count start to the compare match. • Timing to set the TRDi register to 0000h Overflow or compare match in the TRDGRAi register • Buffer operation (refer to **14.3.2 Buffer Operation**) • Synchronous operation (refer to **14.3.3 Synchronous Operation**) • Output pin in the TRDGRCi and TRDGRDi registers changed The TRDGRCi register can be used as output control of the TRDIOAi pin and the TRDGRDi register can be used as output control of the TRDIOBi pin. • Pulse output forced cutoff signal input (refer to **14.3.4 Pulse Output Forced Cutoff**) • Timer RD can be used as the internal timer without output.

i = 0 or 1, j = either A, B, C or D

Timer RD Start Register(1)

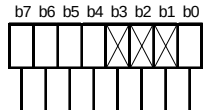


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at the compare match with the TRDGRA0 register after the count clear 1 : Count continues at the compare match with the TRDGRA0 register after the count clear	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at the compare match with the TRDGRA1 register after the count clear 1 : Count continues at the compare match with the TRDGRA1 register after the count clear	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of Notes on Timer RD.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and generating the compare match signal (TRDIOA0), this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and generating the compare match signal (TRDIOA1), this bit is set to 0 (count stops).

Timer RD Mode Register



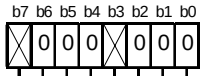
Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0 : TRD0 and TRD1 registers operate independently 1 : TRD0 and TRD1 registers operate synchronously	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function selection bit(1)	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function selection bit(1)	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function selection bit(1)	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function selection bit(1)	0 : General register 1 : Buffer register of TRDGRB1 register	RW

NOTE:
1. When selecting 0 (change the TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi (i = 0 or 1) register, set the BFji bit in the TRDMR register to 0.

Figure 14.48 Registers TRDSTR and TRDMR in Output Compare Function

Timer RD PWM Mode Register



Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 selection bit	Set to 0 (timer mode) in the output compare function	RW
PWMC0	PWM mode of TRDIOC0 selection bit	Set to 0 (timer mode) in the output compare function	RW
PWMD0	PWM mode of TRDIOD0 selection bit	Set to 0 (timer mode) in the output compare function	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 selection bit	Set to 0 (timer mode) in the output compare function	RW
PWMC1	PWM mode of TRDIOC1 selection bit	Set to 0 (timer mode) in the output compare function	RW
PWMD1	PWM mode of TRDIOD1 selection bit	Set to 0 (timer mode) in the output compare function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.49 TRDPMR Register in Output Compare Function

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

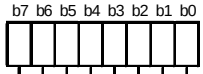
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode selection bit(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the output compare function.	RW
CMD1			RW
OLS0	Normal-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the output compare function.	RW
OLS1	Counter-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the output compare function.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in the output compare function.	RW
ADEG	A/D trigger edge selection bit (in complementary PWM mode)	This bit is disabled in the output compare function.	RW
STCLK	External clock input selection bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode selection bit(2)	Set this bit to 1 (other than PWM3 mode) in the output compare function.	RW

NOTES:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.50 TRDFCR Register in Output Compare Function

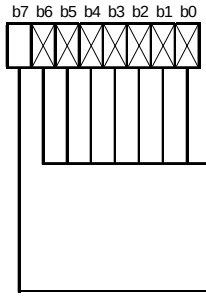
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2



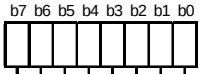
Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6 - b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{INT0}$ pin)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff**.

Figure 14.51 Registers TRDOER1 to TRDOER2 in Output Compare Function

Timer RD Output Control Register(1,2)



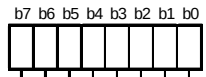
Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level selection bit	0 : Initial output “L” 1 : Initial output “H”	RW
TOB0	TRDIOB0 output level selection bit	0 : Initial output “L” 1 : Initial output “H”	RW
TOC0	TRDIOC0 initial output level selection bit	0 : “L” 1 : “H”	RW
TOD0	TRDIOD0 initial output level selection bit		RW
TOA1	TRDIOA1 initial output level selection bit		RW
TOB1	TRDIOB1 initial output level selection bit		RW
TOC1	TRDIOC1 initial output level selection bit		RW
TOD1	TRDIOD1 initial output level selection bit		RW

NOTES:
1. Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When the pin functions are waveform output (refer to **Table 14.12** to **14.19**) and the TRDOCR register is set, the initial output level is output.

Figure 14.52 TRDOCR Register in Output Compare Function

Timer RD Control Register i (i = 0 or 1)



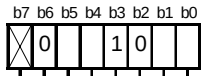
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source selection bit	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge selection bit(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set	RW
CKEG1			RW
CCLR0	TRDi counter clear selection bit	b7 b6 b5 0 0 0 : Disable clear (free-running operation) 0 0 1 : Clear by the compare match in the TRDGRAi register 0 1 0 : Clear by the compare match in the TRDGRBi register 0 1 1 : Synchronous clear (clear simultaneously with other channel counter)(3) 1 0 0 : Do not set 1 0 1 : Clear by the compare match in the TRDGRCi register 1 1 0 : Clear by the compare match in the TRDGRDi register 1 1 1 : Do not set	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This bit is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. This bit is enabled when the TCK2 to TCK0 bits are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This bit is enabled when the SYNC bit in the TRDMR register is set to 1 (TRD0 and TRD1 operate synchronously).

Figure 14.53 Registers TRDCR0 to TRDCR1 in Output Compare Function

Timer RD I/O Control Register Ai (i = 0 or 1)



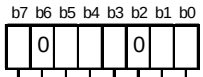
Symbol	Address	After Reset
TRDIORA0	0141h	10001000b
TRDIORA1	0151h	10001000b

Bit Symbol	Bit Name	Function	RW
IOA0	TRDGRA control bit	b1 b0 0 0 : Disable pin output by the compare match (TRDIOAi pin functions as programmable I/O port) 0 1 : "L" output by the compare match in the TRDGRAi register 1 0 : "H" output by the compare match in the TRDGRAi register 1 1 : Toggle output by the compare match in the TRDGRAi register	RW
IOA1			RW
IOA2	TRDGRA mode selection bit(1)	Set to 0 (output compare) in the output compare function	RW
IOA3	Input capture input switch bit	Set to 1	RW
IOB0	TRDGRB control bit	b5 b4 0 0 : Disable pin output by the compare match (TRDIOBi pin functions as programmable I/O port) 0 1 : "L" output by the compare match in the TRDGRBi register 1 0 : "H" output by the compare match in the TRDGRBi 1 1 : Toggle output by the compare match in the TRDGRBi register	RW
IOB1			RW
IOB2	TRDGRB mode selection bit(2)	Set to 0 (output compare) in the output compare function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. When selecting 1 (The TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same as the IOA2 bit in the TRDIORAi register.
2. When selecting 1 (The TRDGRDi register is used as a buffer register of TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same as the IOB2 bit in the TRDIORAi register.

Figure 14.54 Registers TRDIORA0 to TRDIORA1 in Output Compare Function

Timer RD I/O Control Register Ci (i = 0 or 1)



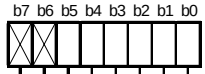
Symbol	Address	After Reset
TRDIORC0	0142h	10001000b
TRDIORC1	0152h	10001000b

Bit Symbol	Bit Name	Function	RW
IOC0	TRDGRC control bit	b1 b0 0 0 : Disable pin output by the compare match 0 1 : "L" output by the compare match in the TRDGRCi register 1 0 : "H" output by the compare match in the TRDGRCi register 1 1 : Toggle output by the compare match in the TRDGRCi register	RW
IOC1			RW
IOC2	TRDGRC mode selection bit(1)	Set to 0 (output compare) in the output compare function	RW
IOC3	TRDGRC register function selection bit(1)	0 : TRDIOA output register (Refer to **14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**) 1 : General register or buffer register	RW
IOD0	TRDGRD control bit	b5 b4 0 0 : Disable pin output by the compare match 0 1 : "L" output by the compare match in the TRDGRDi register 1 0 : "H" output by the compare match in the TRDGRDi register 1 1 : Toggle output by the compare match in the TRDGRDi register	RW
IOD1			RW
IOD2	TRDGRD mode selection bit(2)	Set to 0 (output compare) in the output compare function	RW
IOD3	TRDGRD register function selection bit	0 : TRDIOB output register (Refer to **14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**) 1 : General register or buffer register	RW

NOTES:
1. When selecting 1 (The TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same as the IOA2 bit in the TRDIORAi register.
2. When selecting 1 (The TRDGRDi register is used as a buffer register of TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same as the IOB2 bit in the TRDIORAi register.

Figure 14.55 Registers TRDIORC0 to TRDIORC1 in Output Compare Function

Timer RD Status Register i (i = 0 or 1)



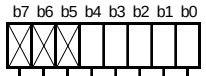
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register.(3)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register.(3)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in the output compare function.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to the b5 in the TRDSR0 register. When writing to the b5, write 0. When reading, its content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and writing 0 to the same bit.
   - This bit remains unchanged even if the read result is 0 and writing 0 to the same bit. (This bit remains 1 even if this bit is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged when writing 1.
3. Including when the BFji bit (j = C or D) in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.56 Registers TRDSR0 to TRDSR1 in Output Compare Function

Timer RD Interrupt Enable Register i (i = 0 or 1)

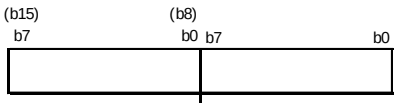


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable an interrupt (IMIA) by the IMFA bit 1 : Enable an interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable an interrupt (IMIB) by the IMFB bit 1 : Enable an interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable an interrupt (IMIC) by the IMFC bit 1 : Enable an interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable an interrupt (IMID) by the IMFD bit 1 : Enable an interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable an interrupt (OVI) by the OVF bit 1 : Enable an interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.57 Registers TRDIER0 to TRDIER1 in Output Compare Function

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 14.58 Registers TRD0 to TRD1 in Output Compare Function

Timer RD General Register Ai, Bi, Ci and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.26 TRDGRji Register Functions in Output Compare Function**	RW

NOTE:
1. Access the TRDGRAi to TRDGRDi registers in 16-bit units. Do not access them in 8-bit units.

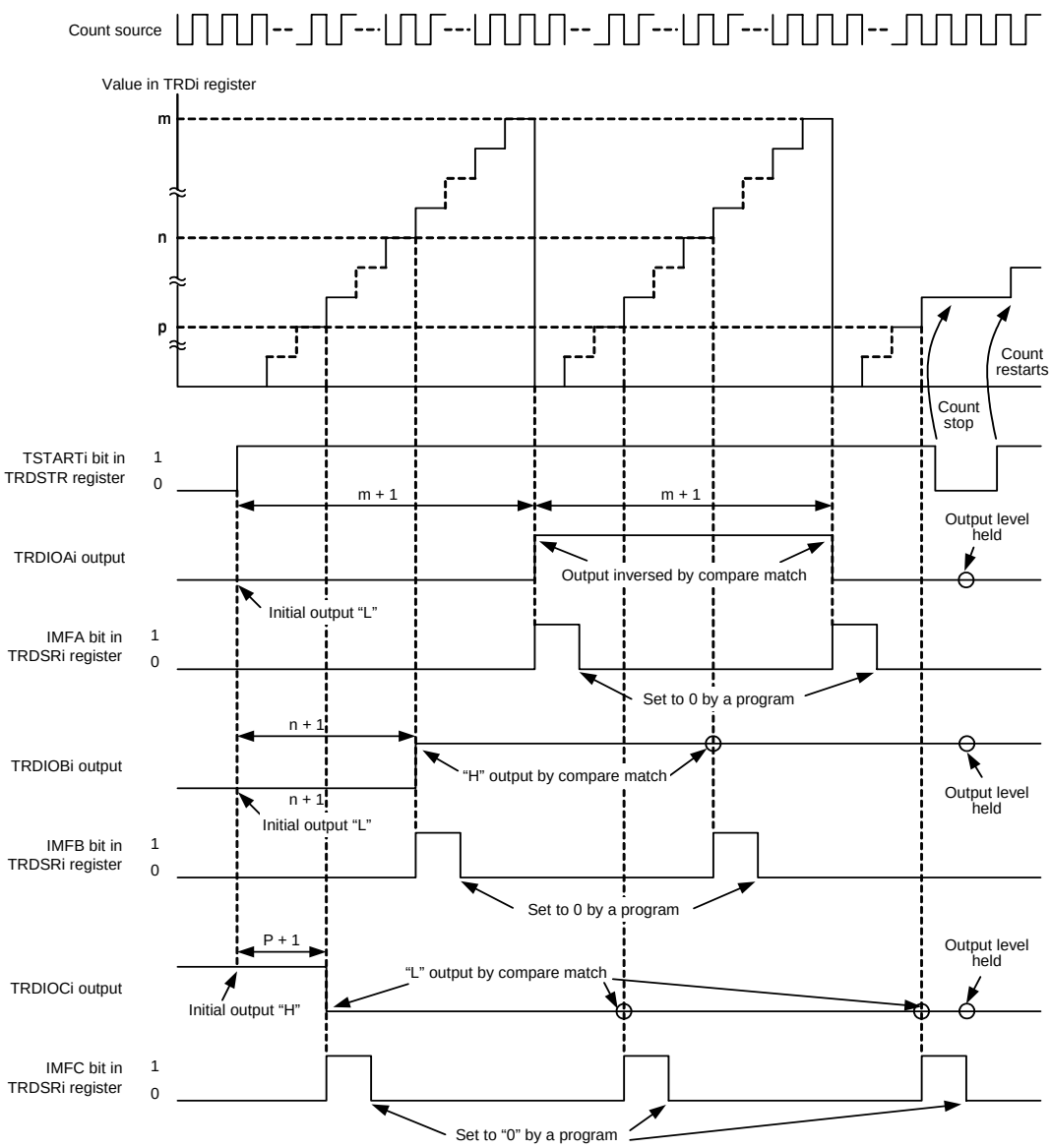
Figure 14.59 Registers TRDGRAi, TRDGRBi, TRDGRCi and TRDGRDi in Output Compare Function

The following registers are disabled in the output compare function:
TRDDF0, TRDDF1, TRDPOCR0 and TRDPOCR1

Table 14.26 TRDGRji Register Functions in Output Compare Function

Register	Setting		Register Function	Output-Compare Output Pin
	BFji	IOj3		
TRDGRAi	–	–	General register. Write the compare value.	TRDIOAi
TRDGRBi				TRDIOBi
TRDGRCi	0	1	General register. Write the compare value.	TRDIOCi
TRDGRDi				TRDIODi
TRDGRCi	1	1	Buffer register. Write the next compare value (refer to **14.3.2 Buffer Operation**.)	TRDIOAi
TRDGRDi				TRDIOBi
TRDGRCi	0	0	TRDIOAi output control (refer to **14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.)	TRDIOAi
TRDGRDi				TRDIOBi

i = 0 or 1, j = either A, B, C or D
BFji: Bit in TRDMR register IOj3: Bit in TRDIORCi register



i = 0 or 1

m: Setting value in TRDGRAi register
n: Setting value in TRDGRBi register
p: Setting value in TRDGRCi register

The above applies to the following conditions:
The CSELi bit in the TRDSTR register is set to 1. (The TRDi register is not stopped by the compare match.)
The BFCi and BFDi bits in the TRDMR register are set to 0. (The TRDGRCi and TRDGRDi registers are not used as the buffer register.)
The EAi, EBi and ECi bits in the TRDOER1 register are set to 0. (Enable the TRDIOAi, TRDIOBi and TRDIOCi pin outputs.)
The CCLR2 to CCLR0 bits in the TRDCRi register are set to 001b. (Set the TRDi register to 000h by the compare match in the TRDGRAi register.)
The TOAi and TOBi bits in the TRDOCR register is set to 0. (initial output "L" to the compare match), the TOCi bit is set to 1. (initial output "H" to the compare match.)
The IOA2 to IOA0 bits in the TRDIORAi register are set to 011b. (TRDIOAi output inversed at the TRDGRAi register compare match.)
The IOB2 to IOB0 bits in the TRDIORAi register are set to 010b. (TRDIOBi "H" output at the TRDGRBi register compare match.)
The IOC3 to IOC0 bits in the TRDIORCi register are set to 1001b. (TRDIOCi "L" output at the TRDGRCi register compare match.)
The IOD3 bit in the TRDIORCi register is set to 1. (TRDGRDi register does not control TRDIOBi pin output.)

Figure 14.60 Operating Example of Output Compare Function

14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi

The TRDGRCi register can be used as output control of the TRDIOAi pin and the TRDGRDi register can be used as output control of the TRDIOBi pin. Therefore, each pin output can be controlled as follows:

- TRDIOAi output is controlled by the values in the TRDGRAi and TRDGRCi registers.
- TRDIOBi output is controlled by the values in the TRDGRBi and TRDGRDi registers.

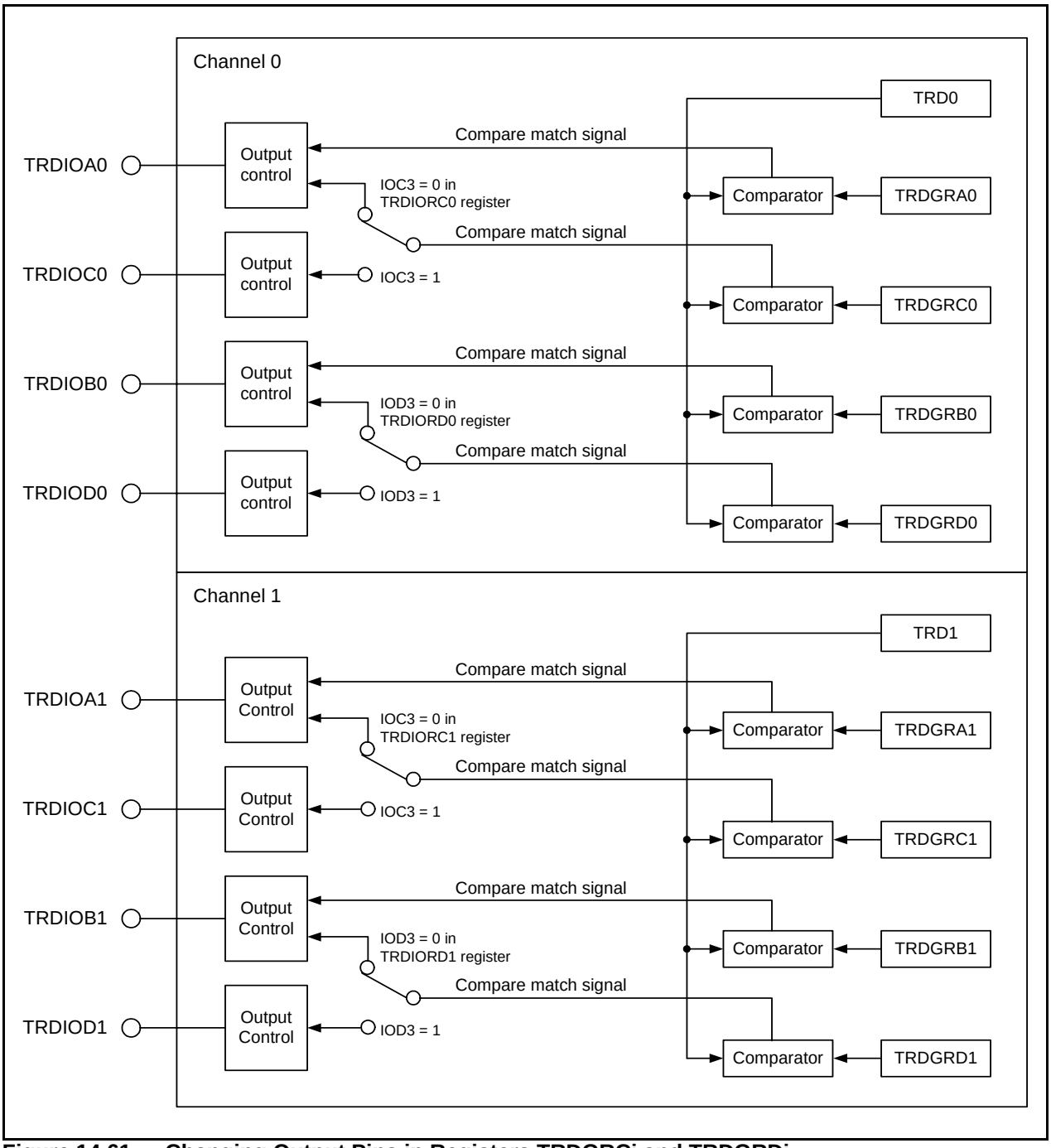
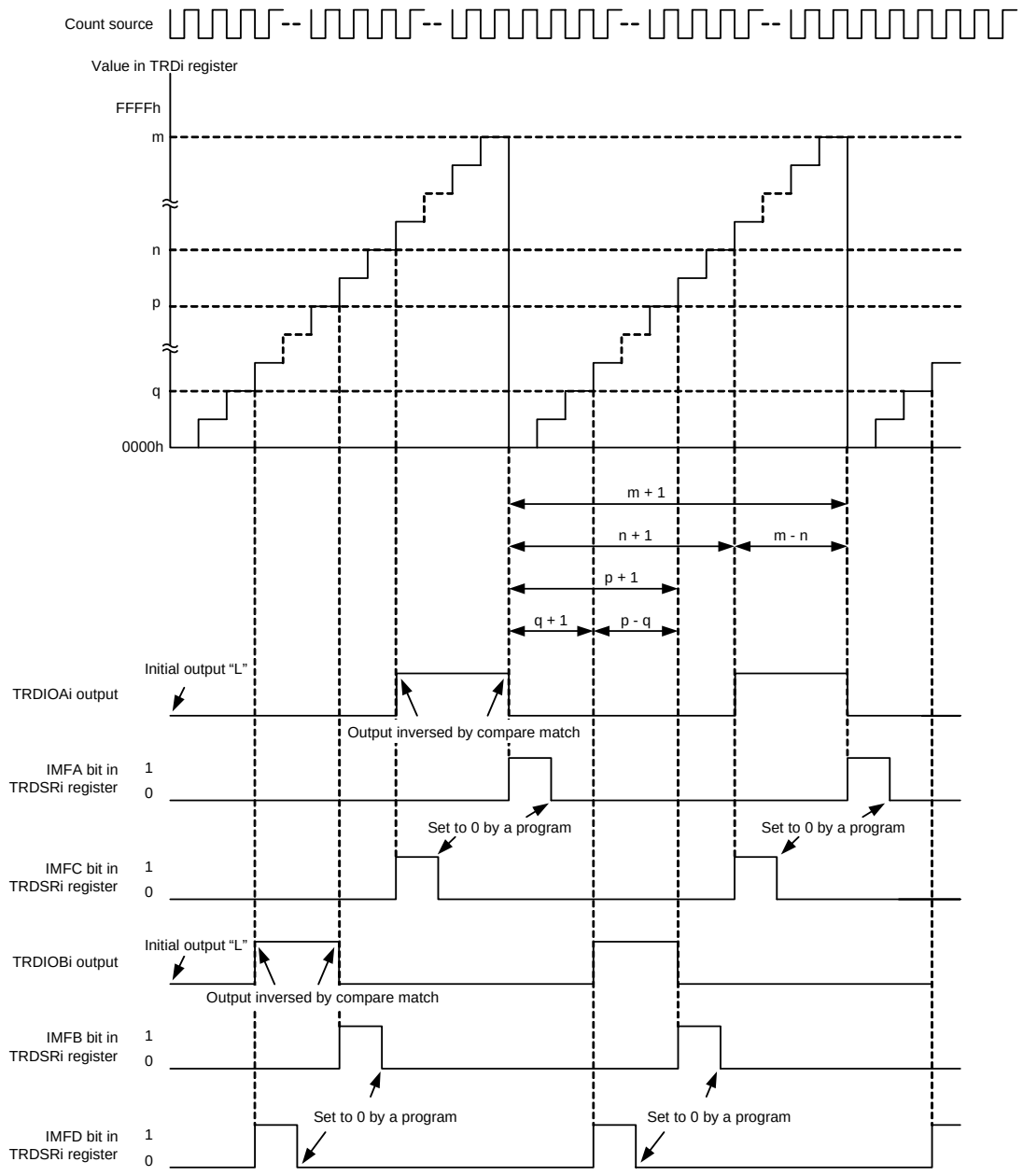


Figure 14.61 Changing Output Pins in Registers TRDGRCi and TRDGRDi

Change output pins in the TRDGRCi and TRDGRDi registers as below:

- Select 0 (change TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi register.
- Set the BFji bit in the TRDMR register to 0 (general register).
- Set the different value in the TRDGRCi register and the TRDGRAi register. Also, set the different value in the TRDGRDi register and the TRDGRBi register.

Figure 14.62 lists the Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin.



m: Setting Value in TRDGRAi register
n: Setting Value in TRDGRCi register
p: Setting Value in TRDGRBi register
q: Setting Value in TRDGRDi register

i = 0 or 1

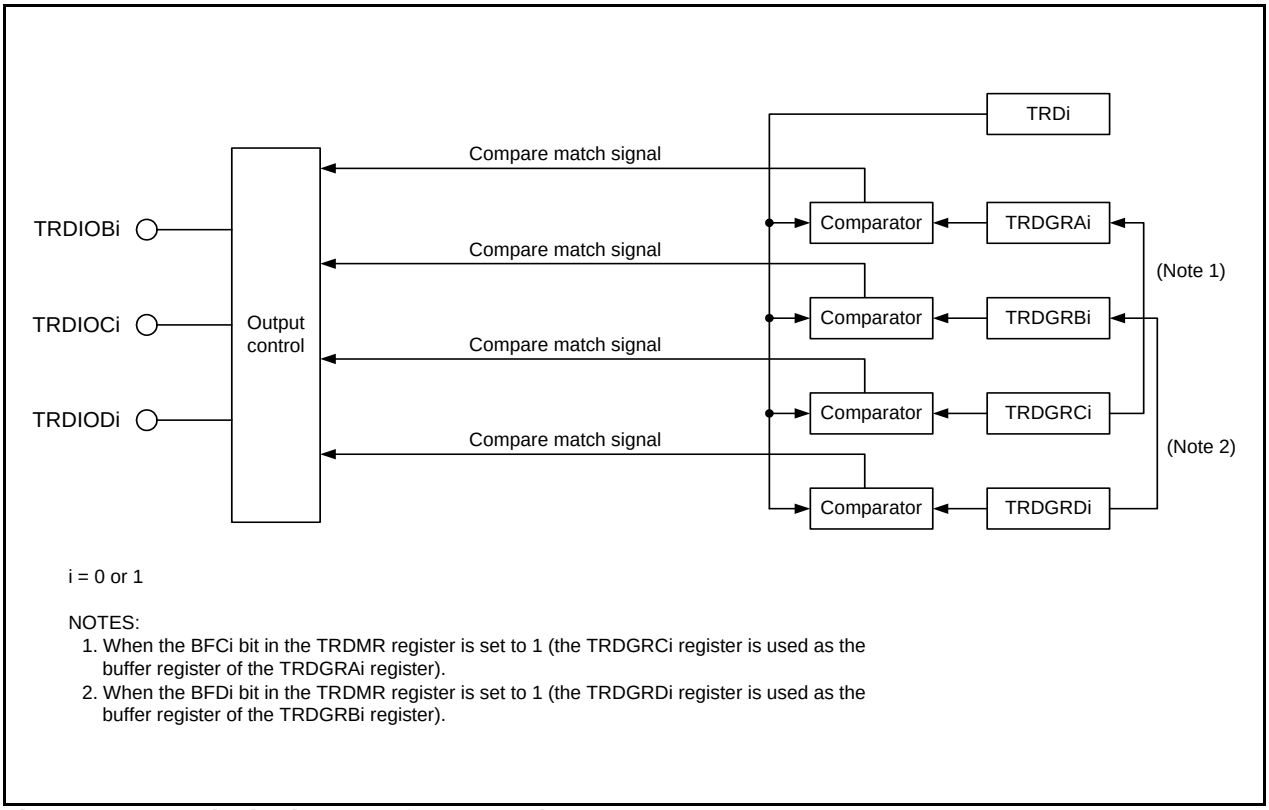
The above applies to the following conditions:
The CSELi bit in the TRDSTR register is set to 1. (The TRDi register is not stopped by the compare match.)
The BFCi and BFDi bits in the TRDMR register are set to 0. (The TRDGRCi and TRDGRDi registers are not used as the buffer register.)
The EAi and EBi bits in the TRDOER1 register are set to 0. (Enable TRDIOAi and TRDIOBi pin outputs.)
The CCLR2 to CCLR0 bits in the TRDCRi register are set to 001b. (Set the TRDi register to 0000h by the compare match in the TRDGRAi register.)
The TOAi and TOBi bits in the TRDOCR register are set to 0. (initial output "L" to the compare match.)
The IOA2 to IOA0 bits in the TRDIORAi register are set to 011b. (TRDIOAi output inversed at the TRDGRAi register compare match.)
The IOB2 to IOB0 bits in the TRDIORAi register are set to 011b. (TRDIOBi output inversed at the TRDGRBi register compare match.)
The IOC3 to IOC0 bits in the TRDIORCi register are set to 0011b. (TRDIOAi output inversed at the TRDGRCi register compare match.)
The IOD3 to IOD0 bits in the TRDIORCi register are set to 0011b. (TRDIOBi output inversed at the TRDGRDi register compare match.)

Figure 14.62 Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin

14.3.7 PWM Mode

PWM mode is to output a PWM waveform. Up to 3 PWM waveforms with the same period can be output by 1 channel. Also, Up to 6 PWM waveforms with the same period can be output by synchronizing Channels 0 and 1. Since this mode functions by a combination of the TRDIOji (i = 0 or 1, j = B, C or D) pin and TRDGRji register, any of PWM mode, other modes or functions can be selected every pin. (However, since the TRDGRAi register is used when using any pin for PWM mode, the TRDGRAi register cannot be used for other modes.)

Figure 14.63 shows the Block Diagram of PWM Mode, Table 14.27 lists the PWM Mode Specifications. Figures 14.64 to 14.73 show the Registers Associated with PWM Mode and Figures 14.74 to 14.75 show the Operations of PWM Mode.

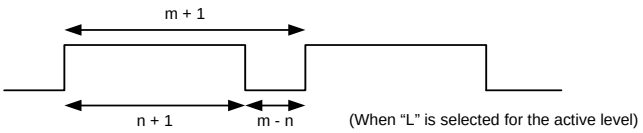


i = 0 or 1

NOTES:
1. When the BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).
2. When the BFDi bit in the TRDMR register is set to 1 (the TRDGRDi register is used as the buffer register of the TRDGRBi register).

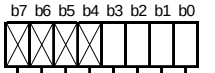
Figure 14.63 Block Diagram of PWM Mode

Table 14.27 PWM Mode Specifications

Item	Specification
Count Sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count Operations	Increment
PWM Waveform	PWM period: 1/fk x (m+1) Active level width: 1/fk x (m-n) Inactive level width: 1/fk x (n+1) fk: Frequency of count source m: Setting value in the TRDGRAi register n: Setting value in the TRDGRji register 
Count Start Condition	Write 1 (count starts) to the TSTARTi bit in the TRDSTR register.
Count Stop Conditions	• Write 0 (count stops) to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The PWM output pin holds level after output change by the compare match.
Interrupt Request Generation Timing	• Compare match (the content in the TRDi register matches with the content in the TRDGRhi register.) • TRDi register overflows
TRDIOA0 Pin Function	Programmable I/O port or TRDCLK (external clock) input
TRDIOA1 Pin Function	Programmable I/O port
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOB1, TRDIOC1, TRDIOD1 Pin Functions	Programmable I/O port or pulse output (select every pin)
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read by reading the TRDi register.
Write to Timer	The value can be written to the TRDi register.
Selection Functions	• 1 to 3 PWM output pins selected per 1 channel Either 1 pin or multiple pins of the TRDIOBi, TRDIOCi or TRDIODi pin. • The active level selected every pin. • Initial output level selected every pin. • Synchronous operation (refer to **14.3.3 Synchronous Operation**.) • Buffer operation (refer to **14.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (refer to **14.3.4 Pulse Output Forced Cutoff**.)

i = 0 or 1, j = either B, C or D,
h = either A, B, C or D

Timer RD Start Register(1)



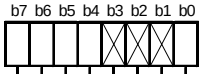
Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at the compare match with the TRDGRA0 register 1 : Count continues at the compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at the compare match with the TRDGRA1 register 1 : Count continues at the compare match with the TRDGRA1 register	RW
— (b7 - b4)	Nothing is assigned. When write, set to 0. When read, its content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of Notes on Timer RD.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and generating the compare match signal (TRDIOA0), this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and generating the compare match signal (TRDIOA1), this bit is set to 0 (count stops).

Figure 14.64 TRDSTR Register in PWM Mode

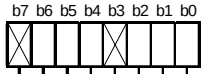
Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0 : TRD0 and TRD1 registers operate independently 1 : TRD0 and TRD1 registers operate synchronously	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function selection bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function selection bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function selection bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function selection bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Timer RD PWM Mode Register



Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 selection bit	0 : Timer mode 1 : PWM mode	RW
PWMC0	PWM mode of TRDIOC0 selection bit	0 : Timer mode 1 : PWM mode	RW
PWMD0	PWM mode of TRDIOD0 selection bit	0 : Timer mode 1 : PWM mode	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 selection bit	0 : Timer mode 1 : PWM mode	RW
PWMC1	PWM mode of TRDIOC1 selection bit	0 : Timer mode 1 : PWM mode	RW
PWMD1	PWM mode of TRDIOD1 selection bit	0 : Timer mode 1 : PWM mode	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.65 Registers TRDMR and TRDPMR in PWM Mode

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

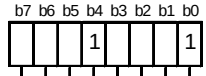
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode selection bit(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM mode.	RW
CMD1			RW
OLS0	Normal-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM mode.	RW
OLS1	Counter-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM mode.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in PWM mode.	RW
ADEG	A/D trigger edge selection bit (in complementary PWM mode)	This bit is disabled in PWM mode.	RW
STCLK	External clock input selection bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode selection bit(2)	Set this bit to 1 (other than PWM3 mode) in PWM mode.	RW

NOTES:
1. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.66 TRDFCR Register in PWM Mode

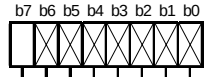
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	Set this bit to 1 (The TRDIOA0 pin is used as a programmable I/O mode) in PWM mode.	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O mode.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O mode.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O mode.)	RW
EA1	TRDIOA1 output disable bit	Set this bit to 1 (The TRDIOA0 pin is used as a programmable I/O mode) in PWM mode.	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O mode.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O mode.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O mode.)	RW

Timer RD Output Master Enable Register 2



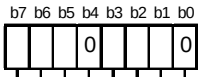
Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6 - b0)	Nothing is assigned. When write, set to 0. When read, its content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{INT0}$ pin)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff**.

Figure 14.67 Registers TRDOER1 to TRDOER2 in PWM Mode

Timer RD Output Control Register(1)

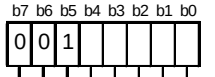


Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level selection bit	Set this bit to 0 (enable output) in PWM mode	RW
TOB0	TRDIOB0 output level selection bit(2)	0 : Initial output is inactive level 1 : Initial output is active level	RW
TOC0	TRDIOC0 initial output level selection bit(2)		RW
TOD0	TRDIOD0 initial output level selection bit(2)		RW
TOA1	TRDIOA1 initial output level selection bit	Set this bit to 0 (enable output) in PWM mode	RW
TOB1	TRDIOB1 initial output level selection bit(2)	0 : Inactive level 1 : Active level	RW
TOC1	TRDIOC1 initial output level selection bit(2)		RW
TOD1	TRDIOD1 initial output level selection bit(2)		RW

NOTES:
1. Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When the pin functions are waveform output (refer to **Table 14.13** to **14.15**; **Table 14.17** to **14.19**) and the TRDOCR register is set, the initial output level is output.

Timer RD Control Register i (i = 0 or 1)



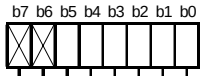
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source selection bit	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge selection bit(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set	RW
CKEG1			RW
CCLR0	TRDi counter clear selection bit	Set to 001b (the TRDi register clear at the compare match with TRDGRAi register) in PWM mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This bit is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. This bit is enabled when the TCK2 to TCK0 bits are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Figure 14.68 Registers TRDOCR and TRDCR0 to TRDCR1 in PWM Mode

Timer RD Status Register i (i = 0 or 1)



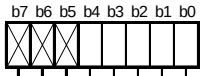
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register.(3)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register.(3)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in PWM mode.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to the bit 5 in the TRDSR0 register. When writing to the bit 5, write 0. When reading, its content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and writing 0 to the same bit.
   - This bit remains unchanged even if the read result is 0 and writing 0 to the same bit. (This bit remains 1 even if this bit is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged when writing 1.
3. Including when the BFji bit (j = C or D) in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.69 Registers TRDSR0 to TRDSR1 in PWM Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)

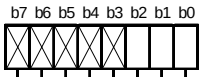


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable an interrupt (IMIA) by the IMFA bit 1 : Enable an interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable an interrupt (IMIB) by the IMFB bit 1 : Enable an interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable an interrupt (IMIC) by the IMFC bit 1 : Enable an interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable an interrupt (IMID) by the IMFD bit 1 : Enable an interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable an interrupt (OVI) by the OVF bit 1 : Enable an interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.70 Registers TRDIER0 to TRDIER1 in PWM Mode

Timer RD PWM Mode Output Level Control Register i (i = 0 or 1)

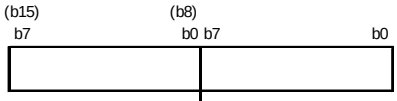


Symbol	Address	After Reset
TRDPOCR0	0145h	11111000b
TRDPOCR1	0155h	11111000b

Bit Symbol	Bit Name	Function	RW
POLB	PWM mode output level control bit B	0 : “L” active of TRDIOBi output level is selected 1 : “H” active of TRDIOBi output level is selected	RW
POLC	PWM mode output level control bit C	0 : “L” active of TRDIOCi output level is selected 1 : “H” active of TRDIOCi output level is selected	RW
POLD	PWM mode output level control bit D	0 : “L” active of TRDIODi output level is selected 1 : “H” active of TRDIODi output level is selected	RW
— (b7 - b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.71 Registers TRDPOCR0 to TRDPOCR1 in PWM Mode

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 14.72 Registers TRD0 to TRD1 in PWM Mode

Timer RD General Register Ai, Bi, Ci and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.28 TRDGRji Register Functions in PWM Mode**	RW

NOTE:
1. Access the TRDGRAi to TRDGRDi registers in 16-bit units. Do not access them in 8-bit units.

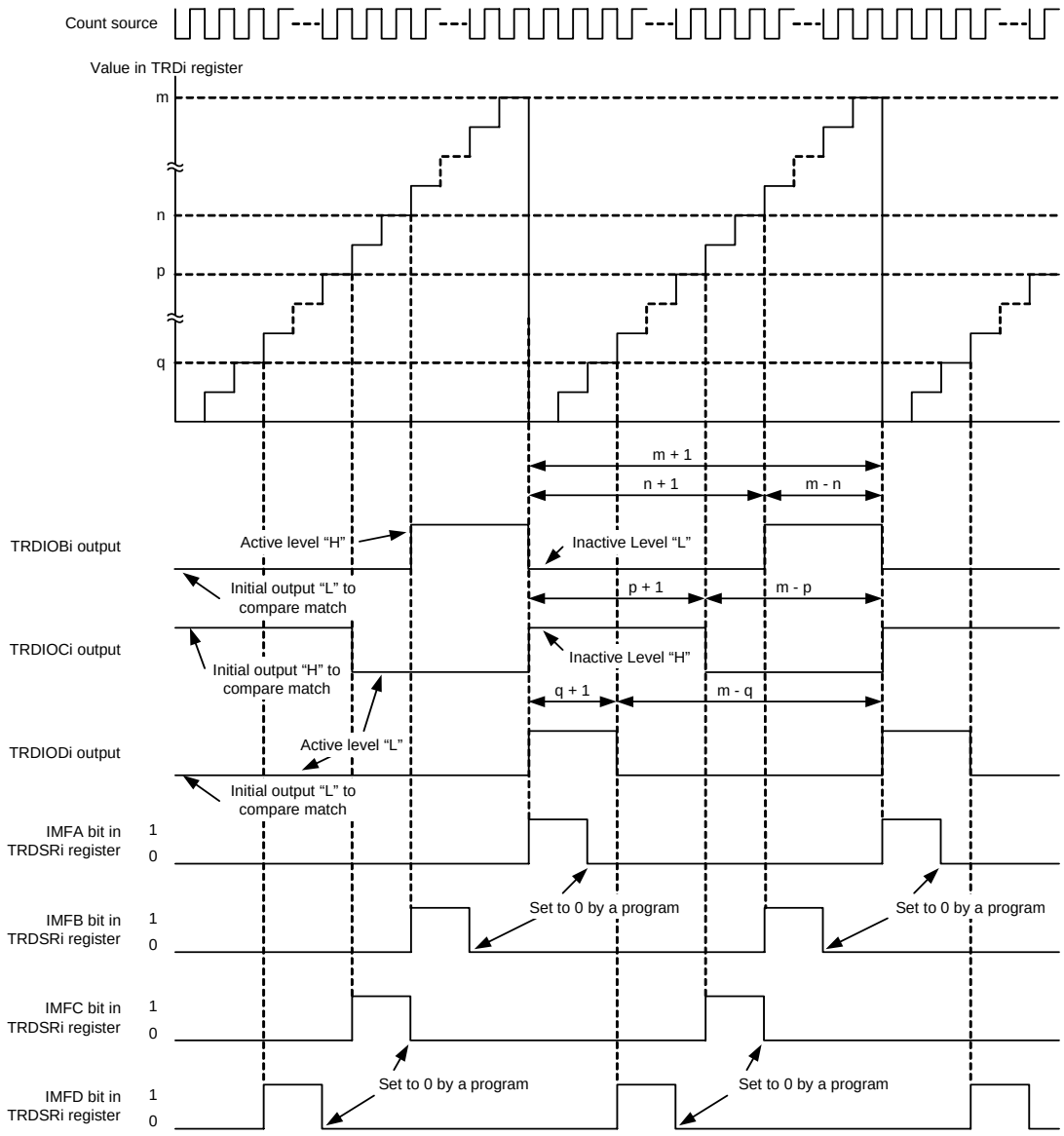
Figure 14.73 Registers TRDGRAi, TRDGRBi, TRDGRCi and TRDGRDi in PWM Mode

The following registers are disabled in the PWM mode:
TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDIORA1 and TRDIORC1

Table 14.28 TRDGRji Register Functions in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRAi	–	General register. Set the PWM period.	–
TRDGRBi	–	General register. Set the changing point of PWM output	TRDIOBi
TRDGRCi	BFCi = 0	General register. Set the changing point of PWM output	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register. Set the next PWM period (refer to **14.3.2 Buffer Operation**.)	–
TRDGRDi	BFDi = 1	Buffer register. Set the changing point of the next PWM output (refer to **14.3.2 Buffer Operation**.)	TRDIOBi

i = 0 or 1
BFCi, BFDi: Bits in TRDMR register

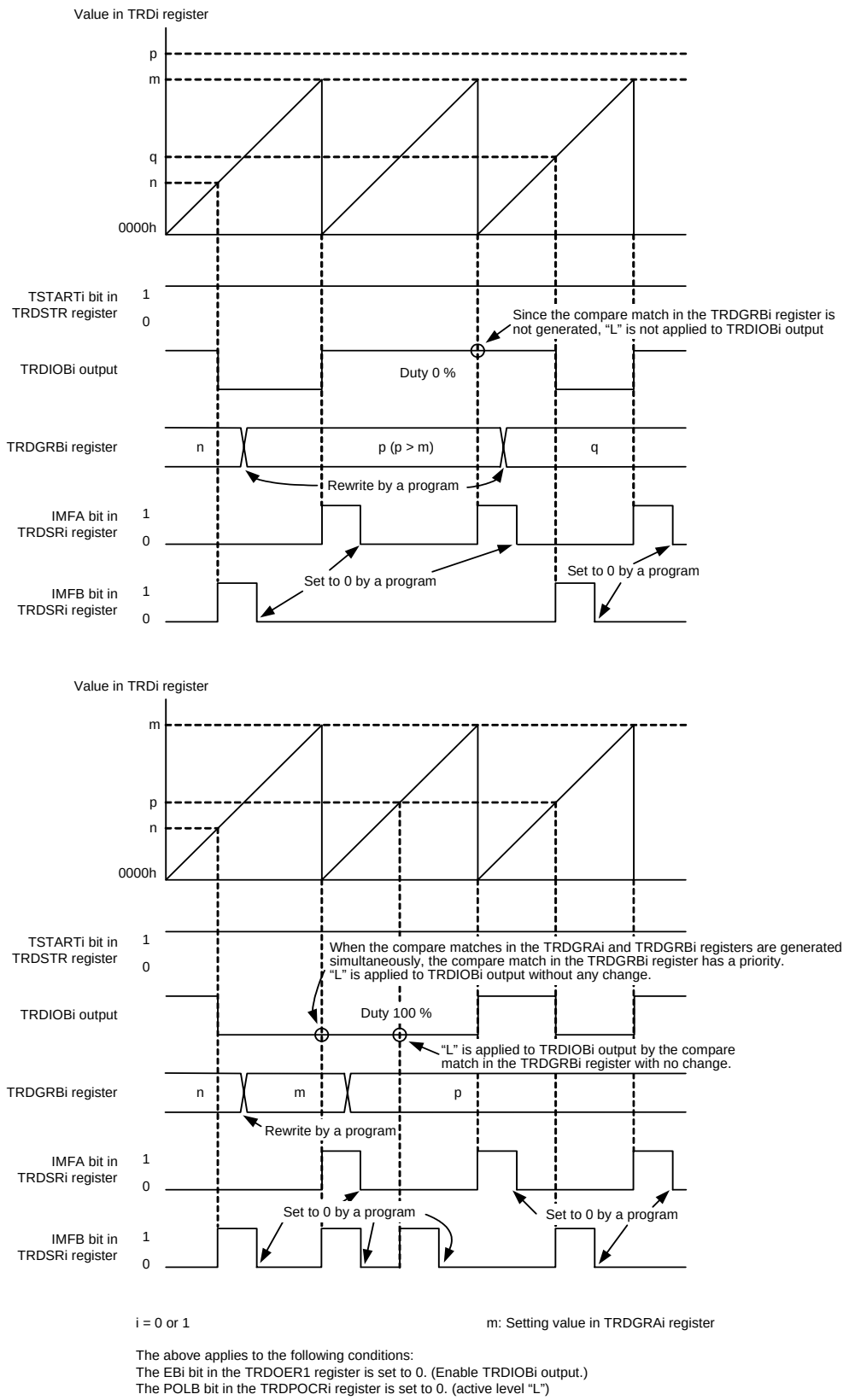


i = 0 or 1

m: Setting value in TRDGRAi register
n: Setting value in TRDGRBi register
p: Setting value in TRDGRCi register
q: Setting value in TRDGRDi register

The above applies to the following conditions:
The BFCi and BFDi bits in the TRDMR register are set to 0. (The TRDGRCi and TRDGRDi registers are not used as the buffer register.)
The EBi, ECi and EDi bits in the TRDOER1 register are set to 0. (Enable TRDIOBi, TRDIOCi and TRDIODi pin outputs.)
The TOBi and TOCi bits in the TRDOCR register are set to 0 (inactive level), the TODi bit is set to 1. (active level)
The POLB bit in the TRDPOCRi register is set to 1 (active level "H"), the POLC and POLD bits are set to 0. (active level "L")

Figure 14.74 Operating Example of PWM Mode



i = 0 or 1

m: Setting value in TRDGRAi register

The above applies to the following conditions:
The EBi bit in the TRDOER1 register is set to 0. (Enable TRDIOBi output.)
The POLB bit in the TRDPOCRi register is set to 0. (active level "L")

Figure 14.75 Operating Example of PWM Mode (Duty 0%, Duty 100%)

14.3.8 Reset Synchronous PWM Mode

Output 3 normal-phases and 3 counter-phases of the PWM waveform with the same period (no three-phase, sawtooth wave modulation and dead time).
Figure 14.76 shows the Block Diagram of Reset Synchronous PWM Mode, Table 14.29 lists the Reset Synchronous PWM Mode Specifications. Figures 14.77 to 14.84 show the Registers Associated with Reset Synchronous PWM Mode and Figure 14.85 shows the Operating Example of Reset Synchronous PWM Mode.
Refer to **Figure 14.75 Operating Example of PWM Mode (Duty 0%, Duty 100%)** for the operation example in PWM Mode of duty 0% and duty 100%.

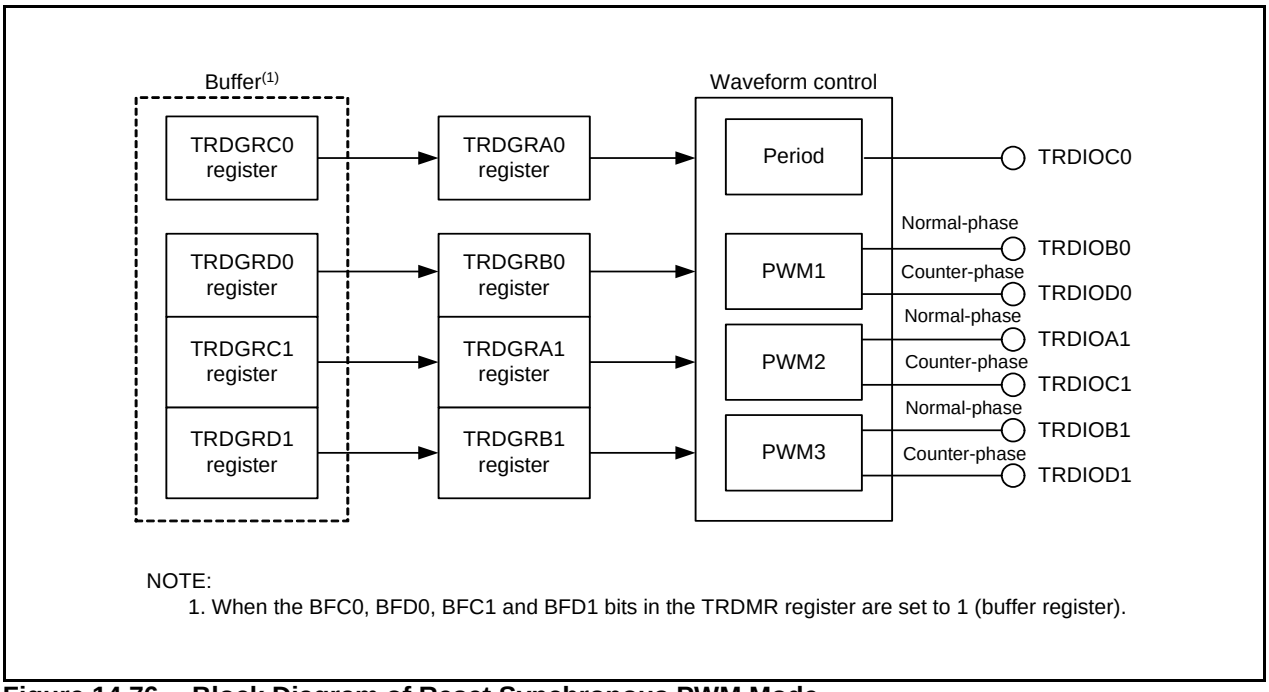
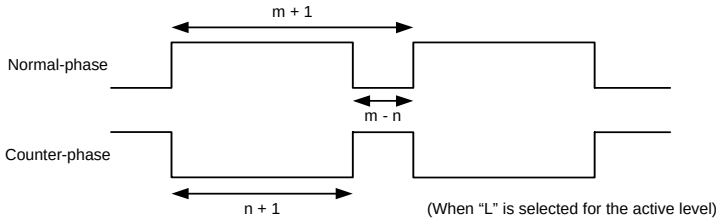


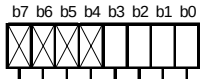
Figure 14.76 Block Diagram of Reset Synchronous PWM Mode

Table 14.29 Reset Synchronous PWM Mode Specifications

Item	Specification
Count Sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count Operations	The TRD0 register is incremented (The TRD1 register is not used.)
PWM Waveform	PWM period: 1/fk × (m + 1) Active level width of normal-phase: 1/fk × (m - n) Active level width of counter-phase: 1/fk × (n + 1) fk: Frequency of count source m: Setting value in the TRDGRA0 register n: Setting value in the TRDGRB0 register (PWM output 1), Setting value in the TRDGRA1 register (PWM output 2), Setting value in the TRDGRB1 register (PWM output 3) 
Count Start Condition	Write 1 (count starts) to the TSTART0 bit in the TRDSTR register.
Count Stop Conditions	• Write 0 (count stops) to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRA0 register. The PWM output pin holds level after output change by the compare match.
Interrupt Request Generation Timing	• Compare match (the content in the TRD0 register matches with the content in the TRDGRj0, TRDGRA1 and TRDGRB1 registers.) • The TRD0 register overflows
TRDIOA0 Pin Function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 Pin Function	PWM output 1 normal-phase output
TRDIOD0 Pin Function	PWM output 1 counter-phase output
TRDIOA1 Pin Function	PWM output 2 normal-phase output
TRDIOC1 Pin Function	PWM output 2 counter-phase output
TRDIOB1 Pin Function	PWM output 3 normal-phase output
TRDIOD1 Pin Function	PWM output 3 counter-phase output
TRDIOC0 Pin Function	Output inverted every period of PWM
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read by reading the TRD0 register.
Write to Timer	The value can be written to the TRD0 register.
Selection Functions	• The active level of normal-phase and counter-phase and initial output level selected individually. • Buffer operation (refer to **14.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (refer to **14.3.4 Pulse Output Forced Cutoff**.)

j = either A, B, C or D

Timer RD Start Register(1)



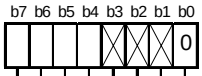
Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5) [This bit is not used in reset synchronous PWM mode]	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at the compare match with the TRDGRA0 register 1 : Count continues at the compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at the compare match with the TRDGRA1 register 1 : Count continues at the compare match with the TRDGRA1 register	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of Notes on Timer RD.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and generating the compare match signal(TRDIOA0), this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and generating the compare match signal(TRDIOA1), this bit is set to 0 (count stops).

Figure 14.77 TRDSTR Register in Reset Synchronous PWM Mode

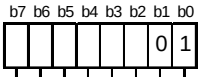
Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	Set this bit to 0 (the TRD0 and TRD1 registers operate independently.) in reset synchronous PWM mode.	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function selection bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function selection bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function selection bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function selection bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Timer RD Function Control Register



Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode selection bit(1,2)	Set to 01b (reset synchronous PWM mode) in reset synchronous PWM mode.	RW
CMD1			RW
OLS0	Normal-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
OLS1	Counter-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in reset synchronous PWM mode.	RW
ADEG	A/D trigger edge selection bit (in complementary PWM mode)	This bit is disabled in reset synchronous PWM mode.	RW
STCLK	External clock input selection bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode selection bit(3)	This bit is disabled in reset synchronous PWM mode.	RW

NOTES:
1. When bits CMD1 to CMD0 are set to 01b, 10b, or 11b, the MCU enters reset synchronous PWM mode or complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
3. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.78 Registers TRDMR and TRDFCR in Reset Synchronous PWM Mode

Timer RD Output Master Enable Register 1

b7	b6	b5	b4	b3	b2	b1	b0
							1

Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in reset synchronous PWM mode.	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (the TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (the TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (the TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (the TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (the TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (the TRDIOC1 pin is used as a programmable I/O port.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (the TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6 - b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (all bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{INT0}$ pin)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff**.

Figure 14.79 Registers TRDOER1 to TRDOER2 in Reset Synchronous PWM Mode

Timer RD Control Register 0(3)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1					

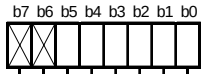
Symbol	Address	After Reset
TRDCR0	0140h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source selection bit	b2 b1b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge selection bit(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set	RW
CKEG1			RW
CCLR0	TRD0 counter clear selection bit	Set to 001b (TRD0 register clear at the compare match with TRDGRA0 register) in reset synchronous PWM mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This bit is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. This bit is enabled when the TCK2 to TCK0 bits are set to “101b” (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. The TRDCR1 register is not used in reset synchronous PWM mode.

Figure 14.80 TRDCR0 Register in Reset Synchronous PWM Mode

Timer RD Status Register i (i = 0 or 1)



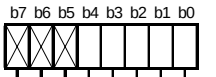
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register.(3)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register.(3)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in reset synchronous PWM mode.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to the b5 in the TRDSR0 register. When writing to the b5, write 0. When reading, its content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and writing 0 to the same bit.
   - This bit remains unchanged even if the read result is 0 and writing 0 to the same bit. (This bit remains 1 even if this bit is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged when writing 1.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.81 Registers TRDSR0 to TRDSR1 in Reset Synchronous PWM Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)

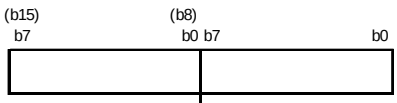


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable an interrupt (IMIA) by the IMFA bit 1 : Enable an interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable an interrupt (IMIB) by the IMFB bit 1 : Enable an interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable an interrupt (IMIC) by the IMFC bit 1 : Enable an interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable an interrupt (IMID) by the IMFD bit 1 : Enable an interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow/underflow interrupt enable bit	0 : Disable an interrupt (OVI) by the OVF bit 1 : Enable an interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.82 Registers TRDIER0 to TRDIER1 in Reset Synchronous PWM Mode

Timer RD Counter 0(1,2)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTES:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
2. The TRD1 register is not used in reset synchronous PWM mode.

Figure 14.83 TRD0 Registrar in Reset Synchronous PWM Mode

Timer RD General Register Ai, Bi, Ci and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.30 TRDGRji Register Functions in Reset Synchronous PWM Mode**	RW

NOTE:
1. Access the TRDGRAi to TRDGRDi registers in 16-bit units. Do not access them in 8-bit units.

Figure 14.84 Registers TRDGRAi, TRDGRBi, TRDGRCi and TRDGRDi in Reset Synchronous PWM Mode

The following registers are disabled in the reset synchronous PWM mode:
TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1 and TRDPOCR1

Table 14.30 TRDGRji Register Functions in Reset Synchronous PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period.	(Output inverted every period of TRDIOC0 and PWM pins)
TRDGRB0	–	General register. Set the changing point of PWM1 output.	TRDIOB0 TRDIOD0
TRDGRC0	BFC0 = 0	(These registers are not used in reset synchronous PWM mode.)	–
TRDGRD0	BFD0 = 0		
TRDGRA1	–	General register. Set the changing point of PWM2 output.	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output.	TRDIOB1 TRDIOD1
TRDGRC1	BFC1 = 0	(These points are not used in reset synchronous PWM mode.)	–
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **14.3.2 Buffer Operation**)	(Output inverted every period of TRDIOC0 and PWM pins)
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of the next PWM1 output. (Refer to **14.3.2 Buffer Operation**)	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of the next PWM2 output. (Refer to **14.3.2 Buffer Operation**)	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of the next PWM3 output. (Refer to **14.3.2 Buffer Operation**)	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR Register

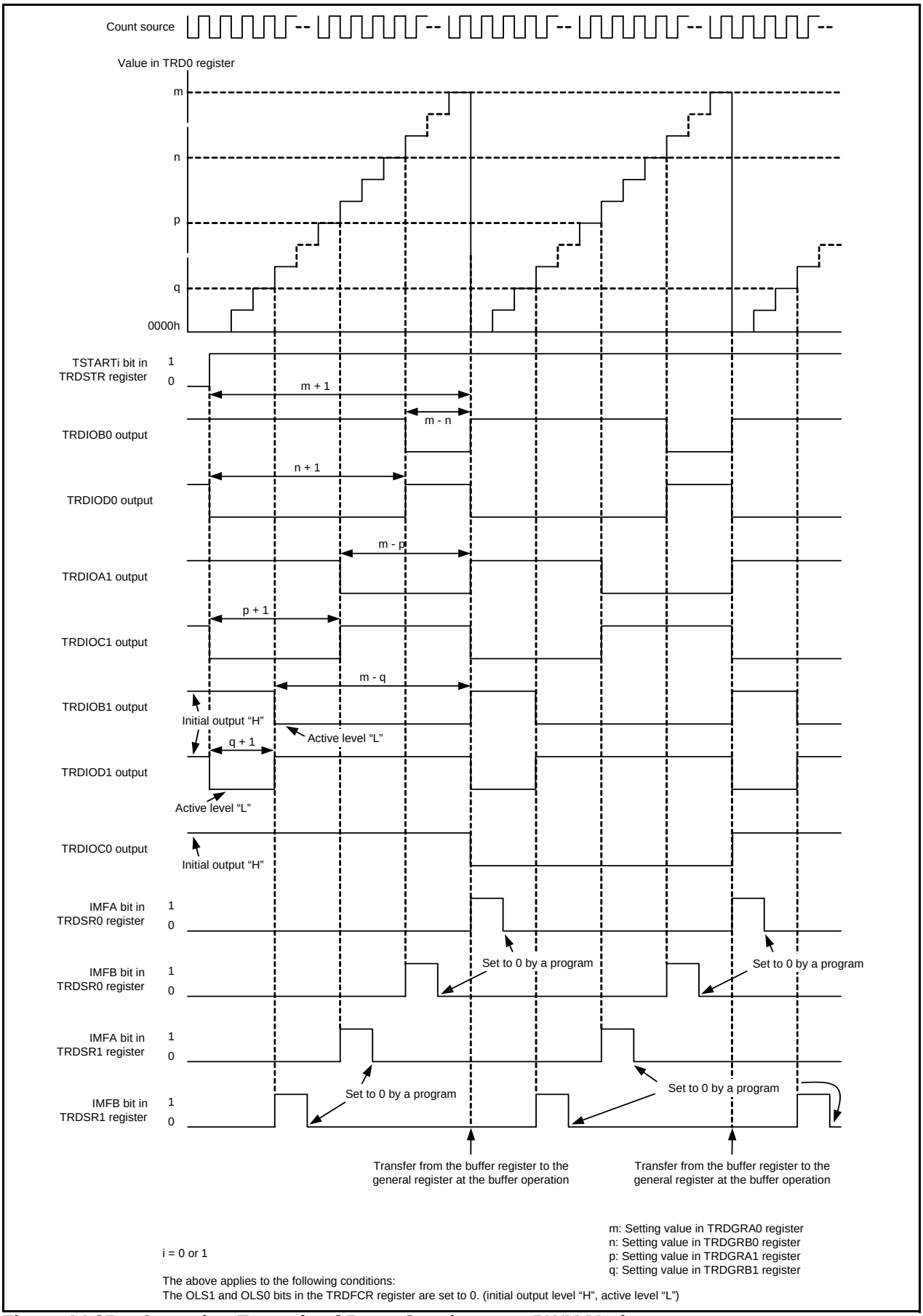


Figure 14.85 Operating Example of Reset Synchronous PWM Mode

14.3.9 Complementary PWM Mode

Output 3 normal-phases and 3 counter-phases of the PWM waveform with the same period (with three-phase, triangular wave modulation and dead time).
Figure 14.86 shows the Block Diagram of Complementary PWM Mode, Table 14.31 lists the Complementary PWM Mode Specifications. Figures 14.87 to 14.95 show the Registers Associated with Complementary PWM Mode, Figure 14.96 shows the Output Model of Complementary PWM Mode and Figure 14.97 shows the Operating Example of Complementary PWM Mode.

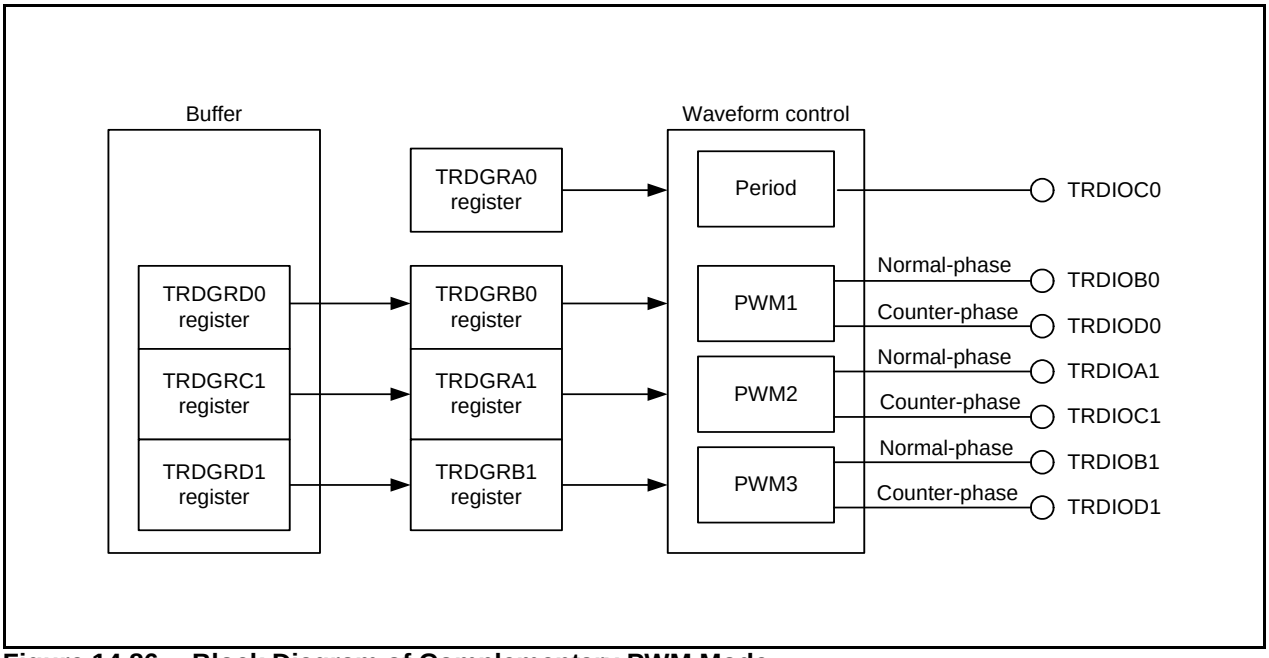
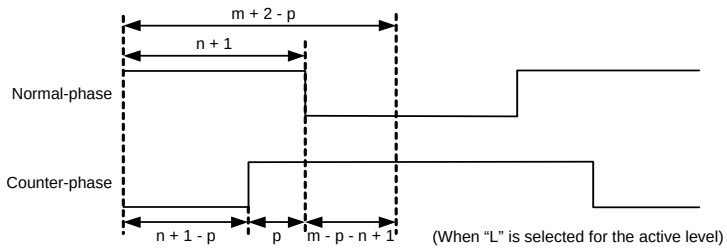


Figure 14.86 Block Diagram of Complementary PWM Mode

Table 14.31 Complementary PWM Mode Specifications

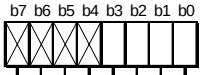
Item	Specification
Count Sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program) Set the TCK2 to TCK0 bits in the TRDCR1 register to the same value (same count source) as the TCK2 to TCK0 bits in the TRDCR0 register.
Count Operations	Increment or decrement The TRD0 and TRD1 registers are decremented with the compare match in the TRD0 and TRDGRA0 registers during increment. The TRD1 register is set from 0000h to FFFFh during decrement, the TRD0 and TRD1 registers are incremented.
PWM Operations	PWM period: 1/fk × (m + 2 - p) × 2(1) Dead time: p Active level width of normal-phase: 1/fk × (m - n - p + 1) × 2 Active level width of counter-phase: 1/fk × (n + 1 - p) × 2 fk: Frequency of count source m: Setting value in the TRDGRA0 register n: Setting value in the TRDGRB0 register (PWM output 1) Setting value in the TRDGRA1 register (PWM output 2) Setting value in the TRDGRB1 register (PWM output 3) p: Setting value in the TRD0 register 
Count Start Condition	Write 1 (count starts) to the TSTART0 and TSTART1 bits in the TRDSTR register.
Count Stop Conditions	Write 0 (count stops) to the TSTART0 and TSTART1 bits in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin holds output level before the count stops.)
Interrupt Request Generation Timing	• Compare match (the content in the TRDi register matches with the content in the TRDGRji register.) • The TRD1 register undeflows
TRDIOA0 Pin Function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 Pin Function	PWM output 1 normal-phase output
TRDIOD0 Pin Function	PWM output 1 counter-phase output
TRDIOA1 PIn Function	PWM output 2 normal-phase output
TRDIOC1 Pin Function	PWM output 2 counter-phase output
TRDIOB1 Pin Function	PWM output 3 normal-phase output
TRDIOD1 Pin Function	PWM output 3 counter-phase output
TRDIOC0 Pin Function	Output inversed every 1/2 period of PWM
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read by reading the TRDi register.
Write to Timer	The value can be written to the TRDi register.
Selection Functions	• Pulse output forced cutoff signal input (refer to **14.3.4 Pulse Output Forced Cutoff**) • The active level of normal-phase and counter-phase and initial output level selected individually. • Transfer timing from the buffer register selected • A/D trigger generated

i = 0 or 1, j = either A, B, C or D

NOTE:

1. After a count starts, the PWM period is stable.

Timer RD Start Register(1)



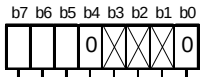
Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at the compare match with the TRDGRA0 register 1 : Count continues at the compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at the compare match with the TRDGRA1 register 1 : Count continues at the compare match with the TRDGRA1 register	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of Notes on Timer RD.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and generating the compare match signal(TRDIOA0), this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and generating the compare match signal(TRDIOA1), this bit is set to 0 (count stops).

Figure 14.87 TRDSTR Register in Complementary PWM Mode

Timer RD Mode Register

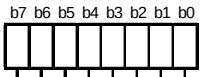


Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	Set this bit to 0 (The TRD0 and TRD1 registers operate independently.) in complementary PWM mode.	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function selection bit	Set this bit to 0 (general register) in complementary PWM mode.	RW
BFD0	TRDGRD0 register function selection bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function selection bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function selection bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.88 TRDMR Register in Complementary PWM Mode

Timer RD Function Control Register



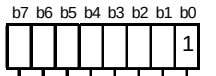
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode selection bit(1,2)	b1 b0 1 0 : Complementary PWM mode (transfer from the buffer register to the general register at the underflow in the TRD1 register.) 1 1 : Complementary PWM mode (transfer from the buffer register to the general register at the compare match with the TRD0 and TRDGRA0 registers.) Other than above : Do not set	RW
CMD1			RW
OLS0	Normal-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
OLS1	Counter-phase output level selection bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	0 : Disable A/D trigger 1 : Enable A/D trigger(3)	RW
ADEG	A/D trigger edge selection bit (in complementary PWM mode)	0 : A/D trigger is generated at the compare match in the TRD0 and TRDGRA0 register 1 : A/D trigger is generated at the underflow in the TRD1 register	RW
STCLK	External clock input selection bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode selection bit(4)	This bit is disabled in complementary PWM mode.	RW

NOTES:
1. When setting bits CMD1 to CMD0 to 10b or 11b, the MCU enters complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
3. Set the ADCAP bit in the ADC0N0 register to 1 (starts by timer RD).
4. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.89 TRDFCR Register in Complementary PWM Mode

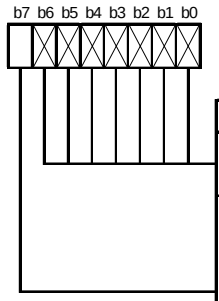
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	Set this bit to 1 (The TRDIOA0 pin is used as a programmable I/O port) in complementary PWM mode.	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2



Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6 - b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{INT0}$ pin)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff**.

Figure 14.90 Registers TRDOER1 to TRDOER2 in Complementary PWM Mode

Timer RD Control Register i (i = 0 or 1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0					

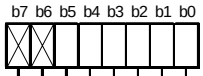
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source selection bit(2)	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge selection bit(2,3)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set	RW
CKEG1			RW
CCLR0	TRDi counter clear selection bit	Set to 000b (disable clear (free-running operation)) in complementary PWM mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This bit is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Set the TCK2 to TCK0 bits and CKEG1 to CKEG0 bits in the TRDCR0 and TRDCR1 registers to the same values.
3. This bit is enabled when the TCK2 to TCK0 bits are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Figure 14.91 Registers TRDCR0 to TRDCR1 in Complementary PWM Mode

Timer RD Status Register i (i = 0 or 1)



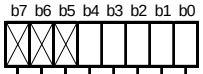
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register.(3)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register.(3)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	[Source for setting this bit to 0] Write 0 after read.(2) [Source for setting this bit to 1] When the TRD1 register underflows.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to the bit 5 in the TRDSR0 register. When writing to the bit 5, write 0. When reading, its content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and writing 0 to the same bit.
   - This bit remains unchanged even if the read result is 0 and writing 0 to the same bit. (This bit remains 1 even if this bit is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged when writing 1.
3. Including when the BFji (j = C or D) bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.92 Registers TRDSR0 to TRDSR1 in Complementary PWM Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)



Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable an interrupt (IMIA) by the IMFA bit 1 : Enable an interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable an interrupt (IMIB) by the IMFB bit 1 : Enable an interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable an interrupt (IMIC) by the IMFC bit 1 : Enable an interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable an interrupt (IMID) by the IMFD bit 1 : Enable an interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable an interrupt (OVI) by the OVF and UDF bits 1 : Enable an interrupt (OVI) by the OVF and UDF bits	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.93 Registers TRDIER0 to TRDIER1 in Complementary PWM Mode

Timer RD Counter 0(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Set the dead time. Count a count source. Count operation is incremented or decremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.

Timer RD Counter 1(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Select 0000h. Count a count source. Count operation is incremented or decremented. When an underflow occurs, the UDF bit in the TRDSR1 register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRD1 register in 16-bit units. Do not access it in 8-bit units.

Figure 14.94 Registers TRD0 to TRD1 in Complementary PWM Mode

Timer RD General Register Ai, Bi, C1 and Di (i = 0 or 1)(1,2)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.32 TRDGRji Register Functions in Complementary PWM Mode**	RW

NOTES:
1. Access the TRDGRAi to TRDGRDi registers in 16-bit units. Do not access them in 8-bit units.
2. The TRDGRC0 register is not used in complementary PWM mode.

Figure 14.95 Registers TRDGRAi, TRDGRBi, TRDGRC1 and TRDGRDi in Complementary PWM Mode

The following registers are disabled in the complementary PWM mode:
TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1 and TRDPOCR1

Table 14.32 TRDGRji Register Functions in Complementary PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period at initialization. Setting range: Setting value or above in TRD0 register FFFFh - TRD0 register setting value or below Do not write when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	(Output inversed every half period of TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB0 TRDIOD0
TRDGRA1	–	General register. Set the changing point of PWM2 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB1 TRDIOD1
TRDGRC0	–	These registers not used in complementary PWM mode.	–
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM1 output. (Refer to **14.3.2 Buffer Operation**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB0 register for the initialization.	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM2 output. (Refer to **14.3.2 Buffer Operation**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRA1 register for the initialization.	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM3 output. (Refer to **14.3.2 Buffer Operation**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB1 register for the initialization.	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Since values cannot be written to the TRDGRB0, TRDGRA1, or TRDGRB1 register directly after count operation starts (prohibited item), use the TRDGRD0, TRDGRC1, or TRDGRD1 register as a buffer register. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).

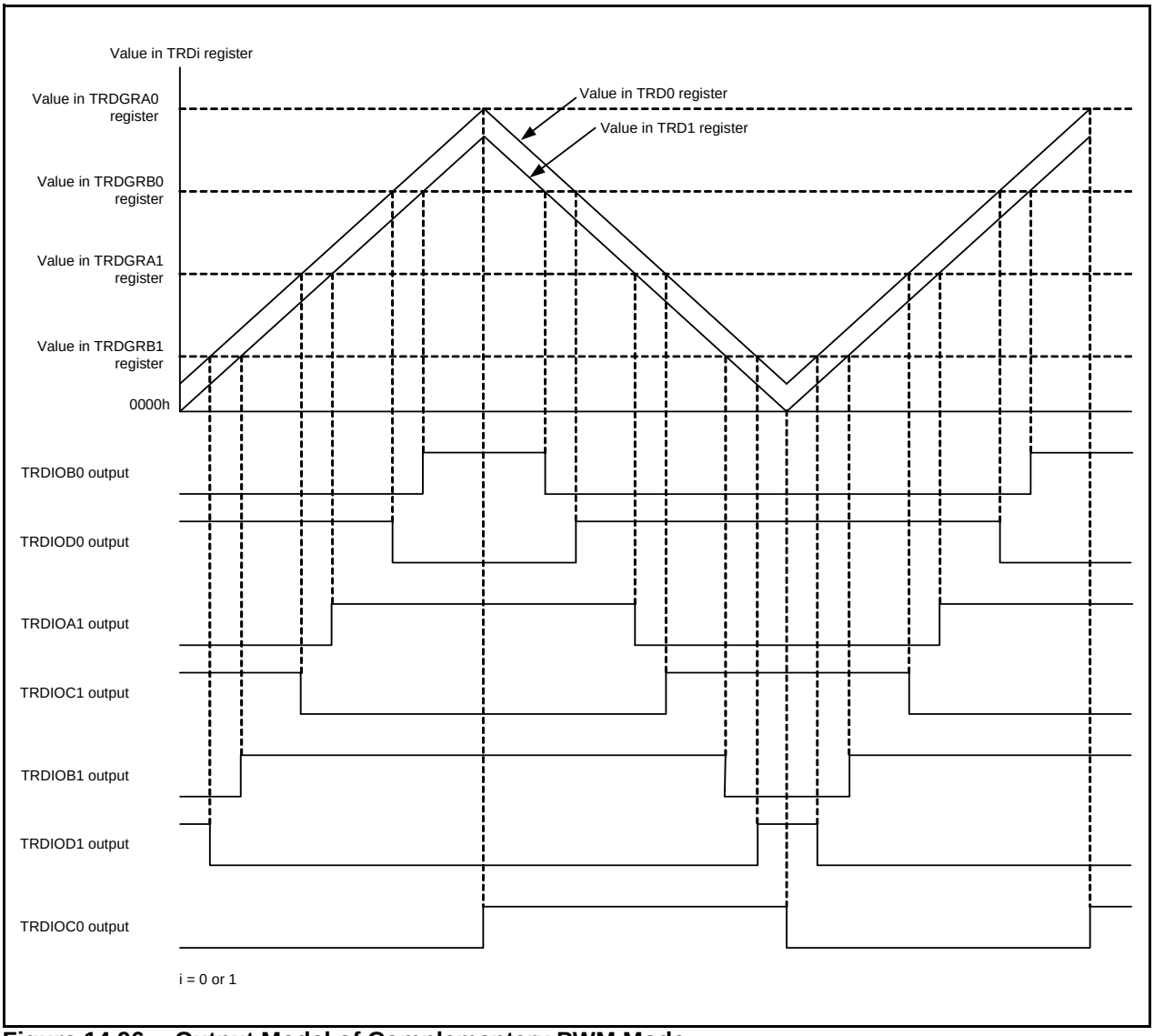
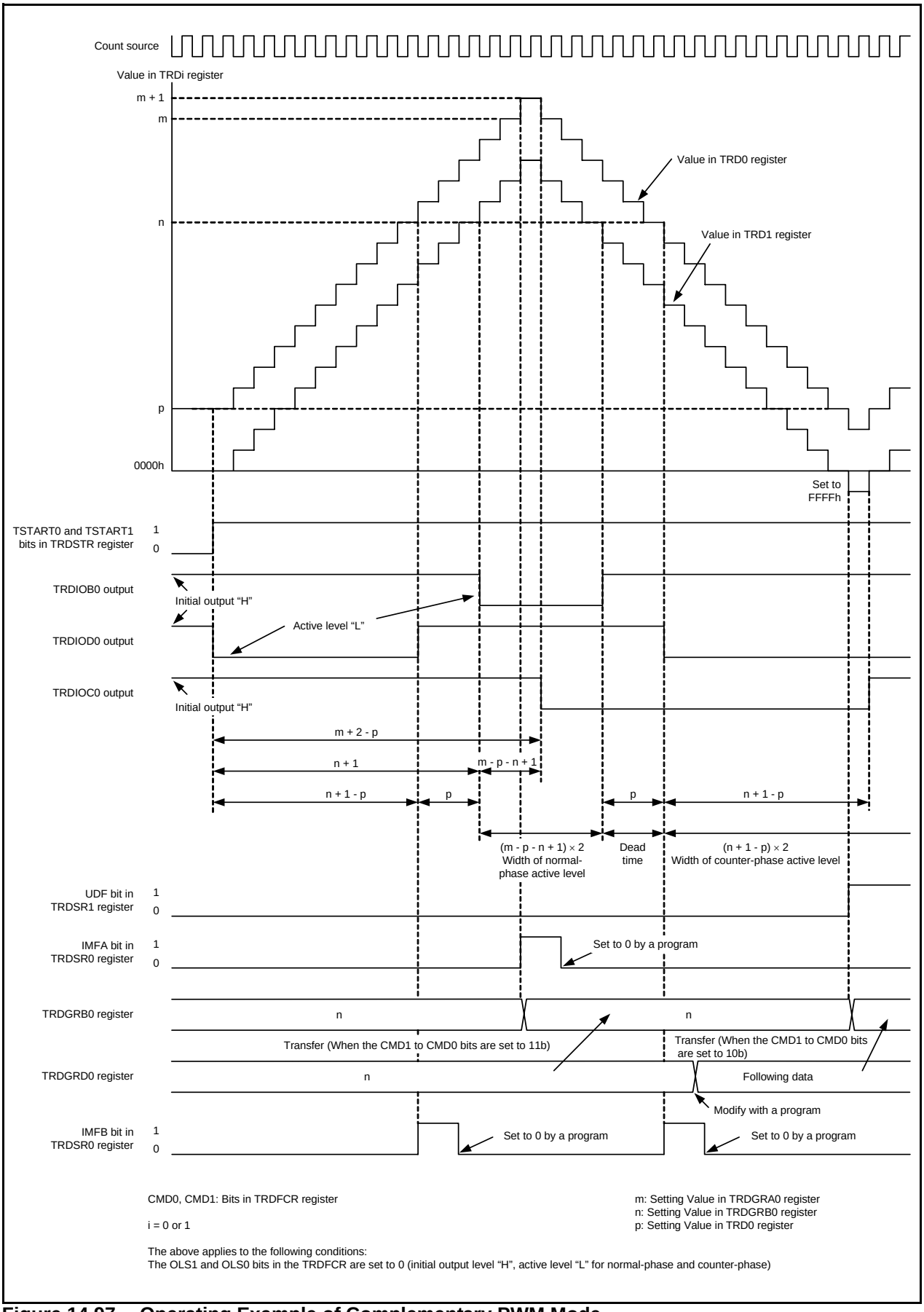


Figure 14.96 Output Model of Complementary PWM Mode



CMD0, CMD1: Bits in TRDFCR register

i = 0 or 1

m: Setting Value in TRDGRA0 register
n: Setting Value in TRDGRB0 register
p: Setting Value in TRD0 register

The above applies to the following conditions:
The OLS1 and OLS0 bits in the TRDFCR are set to 0 (initial output level "H", active level "L" for normal-phase and counter-phase)

Figure 14.97 Operating Example of Complementary PWM Mode

14.3.9.1 Transfer Timing from Buffer Register

- Transfer from the TRDGRD0, TRDGRC1 and TRDGRD1 registers to the TRDGRB0, TRDGRA1 and TRDGRB1 registers
  When the CMD1 to CMD0 bits in the TRDFCR register are set to 10b, the content is transferred when the TRD1 register underflows.
  When the CMD1 to CMD0 bits are set to 11b, the content is transferred at the compare match in the TRD0 and TRDGRA0 registers.

14.3.9.2 A/D Trigger Generation

The compare match in the TRD0 and TRDGRA0 registers and the TRD1 underflow can be used as a conversion start trigger of the A/D converter. It can be selected by the ADEG and ADTRG bits in the TRDFCR register.
Also, set the ADCAP bit in the ADCON0 register to 1 (starts in Timer RD).

14.3.10 PWM3 Mode

Output 2 PWM waveforms with the same period.
Figure 14.98 shows the Block Diagram of PWM3 Mode, Table 14.33 lists the PWM3 Mode Specifications. Figures 14.99 to 14.107 show the Registers Associated with PWM3 Mode and Figure 14.108 shows the Operating Example of PWM3 Mode.

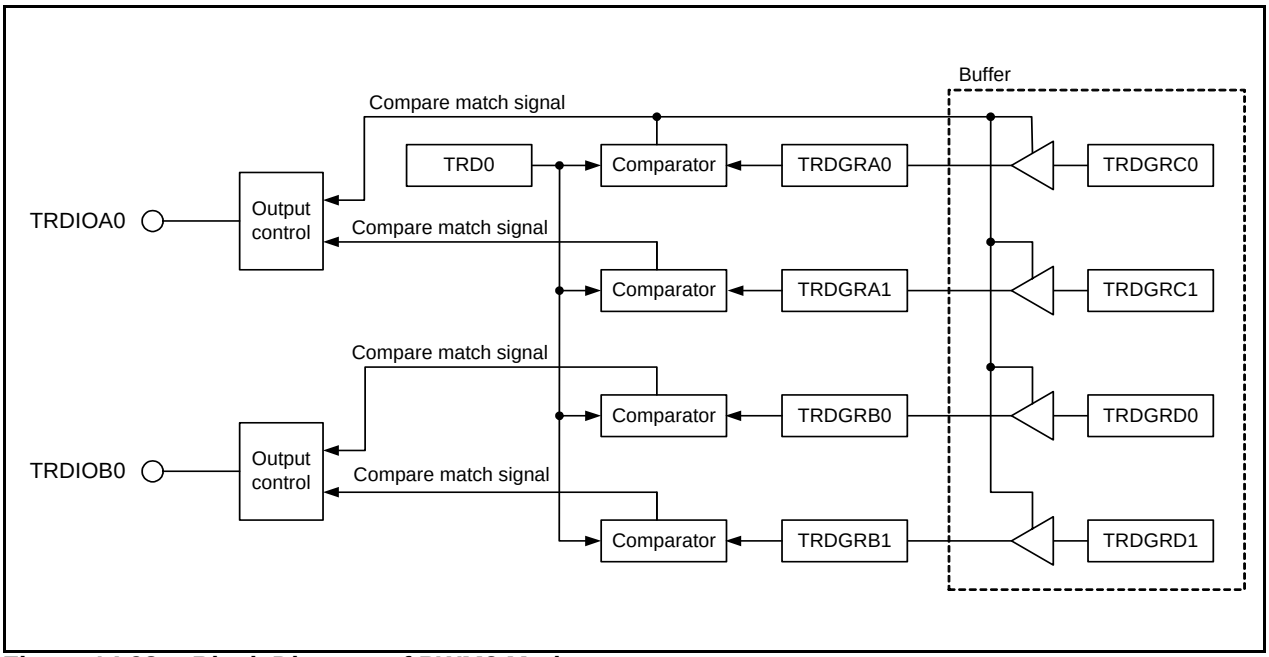
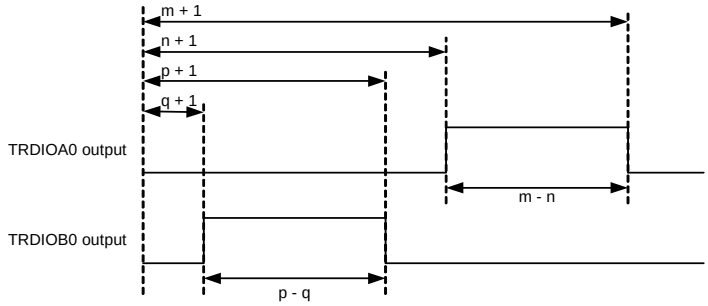


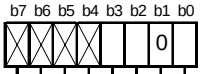
Figure 14.98 Block Diagram of PWM3 Mode

Table 14.33 PWM3 Mode Specifications

Item	Specification
Count Sources	f1, f2, f4, f8, f32, fOCO40M
Count Operations	The TRD0 register is incremented. (The TRD1 is not used.)
PWM Waveform	PWM period: 1/fk × (m + 1) Active level width of TRDIOA0 output: 1/fk × (m - n) Active level width of TRDIOB0 output: 1/fk × (p - q) fk: Frequency of count source m: Setting value in the TRDGRA0 register n: Setting value in the TRDGRA1 register p: Setting value in the TRDGRB0 register q: Setting value in the TRDGRB1 register  (When “H” is selected for the active level)
Count Start Condition	Write 1 (count starts) to the TSTART0 bit in the TRDSTR register.
Count Stop Conditions	• Write 0 (count stops) to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRA0 register. The PWM output pin holds level after output change by the compare match.
Interrupt Request Generation Timing	• Compare match (the content in the TRDi register matches with the content in the TRDGRji register.) • The TRD0 register overflows
TRDIOA0, TRDIOB0 Pin Functions	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 Pin Functions	Programmable I/O port
$\overline{\text{INT0}}$ Pin Function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from Timer	The count value can be read by reading the TRD0 register.
Write to Timer	The value can be written to the TRD0 register.
Selection Functions	• Pulse output forced cutoff signal input (refer to **14.3.4 Pulse Output Forced Cutoff**) • Select the active level every pin. • Buffer operation (refer to **14.3.2 Buffer Operation**)

i = 0 or 1, j = either A, B, C or D

Timer RD Start Register(1)



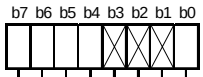
Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	Set this bit to 0 (count stops) in PWM3 mode(3)	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at the compare match with the TRDGRA0 register 1 : Count continues at the compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at the compare match with the TRDGRA1 register 1 : Count continues at the compare match with the TRDGRA1 register	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of Notes on Timer RD.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and generating the compare match signal(TRDIOA0), this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and generating the compare match signal(TRDIOA1), this bit is set to 0 (count stops).

Figure 14.99 TRDSTR Register in PWM3 Mode

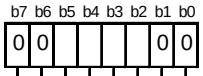
Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	This bit is disabled in PWM3 mode.	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function selection bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function selection bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function selection bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function selection bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Timer RD Function Control Register



Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode selection bit(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM3 mode.	RW
CMD1			RW
OLS0	Normal-phase output level selection bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
OLS1	Counter-phase output level selection bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
ADTRG	A/D trigger enable bit (enabled in complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
ADEG	A/D trigger edge selection bit (enabled in complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
STCLK	External clock input selection bit	Set this bit to 0 (external clock input disabled) in PWM3 mode.	RW
PWM3	PWM3 mode selection bit(2)	Set this bit to 0 (PWM3 mode) in PWM3 mode.	RW

NOTES:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.100 Registers TRDMR and TRDFCR in PWM3 Mode

Timer RD Output Master Enable Register 1

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1	1		

Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	Set these bits to 1 (programmable I/O port) in PWM3 mode.	RW
ED0	TRDIOD0 output disable bit		RW
EA1	TRDIOA1 output disable bit		RW
EB1	TRDIOB1 output disable bit		RW
EC1	TRDIOC1 output disable bit		RW
ED1	TRDIOD1 output disable bit		RW

Timer RD Output Master Enable Register 2

b7	b6	b5	b4	b3	b2	b1	b0

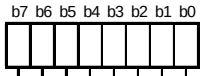
Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6 - b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{INT0}$ pin)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff**.

Figure 14.101 Registers TRDOER1 to TRDOER2 in PWM3 Mode

Timer RD Output Control Register(1)



Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level selection bit(2)	0 : Active level “H”, initial output “L”, output “H” by the compare match in the TRDGRA1register, output “L” by the compare match in the TRDGRA0 register 1 : Active level “L”, initial output “H”, output “L” by the compare match in the TRDGRA1register, output “H” by the compare match in the TRDGRA0 register	RW
TOB0	TRDIOB0 output level selection bit(2)	0 : Active level “H”, initial output “L”, output “H” by the compare match in the TRDGRB1register, output “L” by the compare match in the TRDGRB0 register 1 : Active level “L”, initial output “H”, output “L” by the compare match in the TRDGRB1register, output “H” by the compare match in the TRDGRB0 register	RW
TOC0	TRDIOC0 initial output level selection bit	This bit is disabled in PWM3 mode.	RW
TOD0	TRDIOD0 initial output level selection bit		RW
TOA1	TRDIOA1 initial output level selection bit		RW
TOB1	TRDIOB1 initial output level selection bit		RW
TOC1	TRDIOC1 initial output level selection bit		RW
TOD1	TRDIOD1 initial output level selection bit		RW

NOTES:
1. Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When the pin functions are waveform output (refer to **Table 14.12** and **14.13**) and the TRDOCR register is set, the initial output level is output.

Figure 14.102 TRDOCR Register in PWM3 Mode

Timer RD Control Register i (i = 0 or 1)(2)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1					

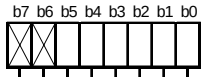
Symbol	Address	After Reset
TRDCR0	0140h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source selection bit	b2 b1b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : Do not set 1 1 0 : fOCO40M 1 1 1 : Do not set	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge selection bit(1)	This bit is disabled in PWM3 mode.	RW
CKEG1			RW
CCLR0	TRD0 counter clear selection bit	Set to 001b (the TRD0 register clear at the compare match with TRDGRA0 register) in PWM3 mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This bit is enabled when the TCK2 to TCK0 bits are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. The TRDCR1 register is not used in PWM3 mode.

Figure 14.103 TRDCR0 Register in PWM3 Mode

Timer RD Status Register i (i = 0 or 1)



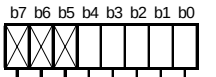
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.(1) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read.(1) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read.(1) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register.(2)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read.(1) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register.(2)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read.(1) [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in PWM3 mode.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and writing 0 to the same bit.
   - This bit remains unchanged even if the read result is 0 and writing 0 to the same bit. (This bit remains 1 even if this bit is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged when writing 1.
2. Including when the BFji bit (j = C or D) in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.104 Registers TRDSR0 and TRDSR1 in PWM3 Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)

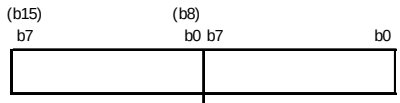


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable an interrupt (IMIA) by the IMFA bit 1 : Enable an interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable an interrupt (IMIB) by the IMFB bit 1 : Enable an interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable an interrupt (IMIC) by the IMFC bit 1 : Enable an interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable an interrupt (IMID) by the IMFD bit 1 : Enable an interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow/underflow interrupt enable bit	0 : Disable an interrupt (OVI) by the OVF bit 1 : Enable an interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.105 Registers TRDIER0 and TRDIER1 in PWM3 Mode

Timer RD Counter 0(1,2)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTES:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
2. The TRD1 register is not used in PWM3 mode.

Figure 14.106 TRD0 Register in PWM3 Mode

Timer RD General Register Ai, Bi, Ci and Di (i = 0 or 1)(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.34 TRDGRji Register Functions in PWM3 Mode**	RW

NOTE:
1. Access the TRDGRAi to TRDGRDi registers in 16-bit units. Do not access them in 8-bit units.

Figure 14.107 Registers TRDGRAi, TRDGRBi, TRDGRCi and TRDGRDi in PWM3 Mode

The following registers are disabled in PWM3 mode:
TRDPMR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1 and TRDPOCR1

Table 14.34 TRDGRji Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period. Setting range: Value set in TRDGRA1 register or above	TRDIOA0
TRDGRA1		General register. Set the changing point (the active level timing) of PWM output. Setting range: Value set in TRDGRA0 register or below	
TRDGRB0		General register. Set the changing point (the timing that returns to initial output level) of PWM output. Setting range: Value set in TRDGRB1 register or above Value set in TRDGRA0 register or below	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output. Setting range: Value set in TRDGRB0 register or below	
TRDGRC0	BFC0 = 0	(These registers are not used in PWM3 mode)	–
TRDGRC1	BFC1 = 0		
TRDGRD0	BFD0 = 0		
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRC1 register or above	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRC0 register or below	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRD1 register or above, setting value or below in TRDGRC0 register.	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRD0 register or below	

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR Register

Registers TRDGRC0, TRDGRC1, TRDGRD0, and TRDGRD1 are not used in PWM3 mode. To use them as buffer registers, set bits BFC0, BFC1, BFD0, and BFD1 to 0 (general register) and write a value to the TRDGRC0, TRDGRC1, TRDGRD0, or TRDGRD1 register. After this, bits BFC0, BFC1, BFD0, and BFD1 may be set to 1 (buffer register).

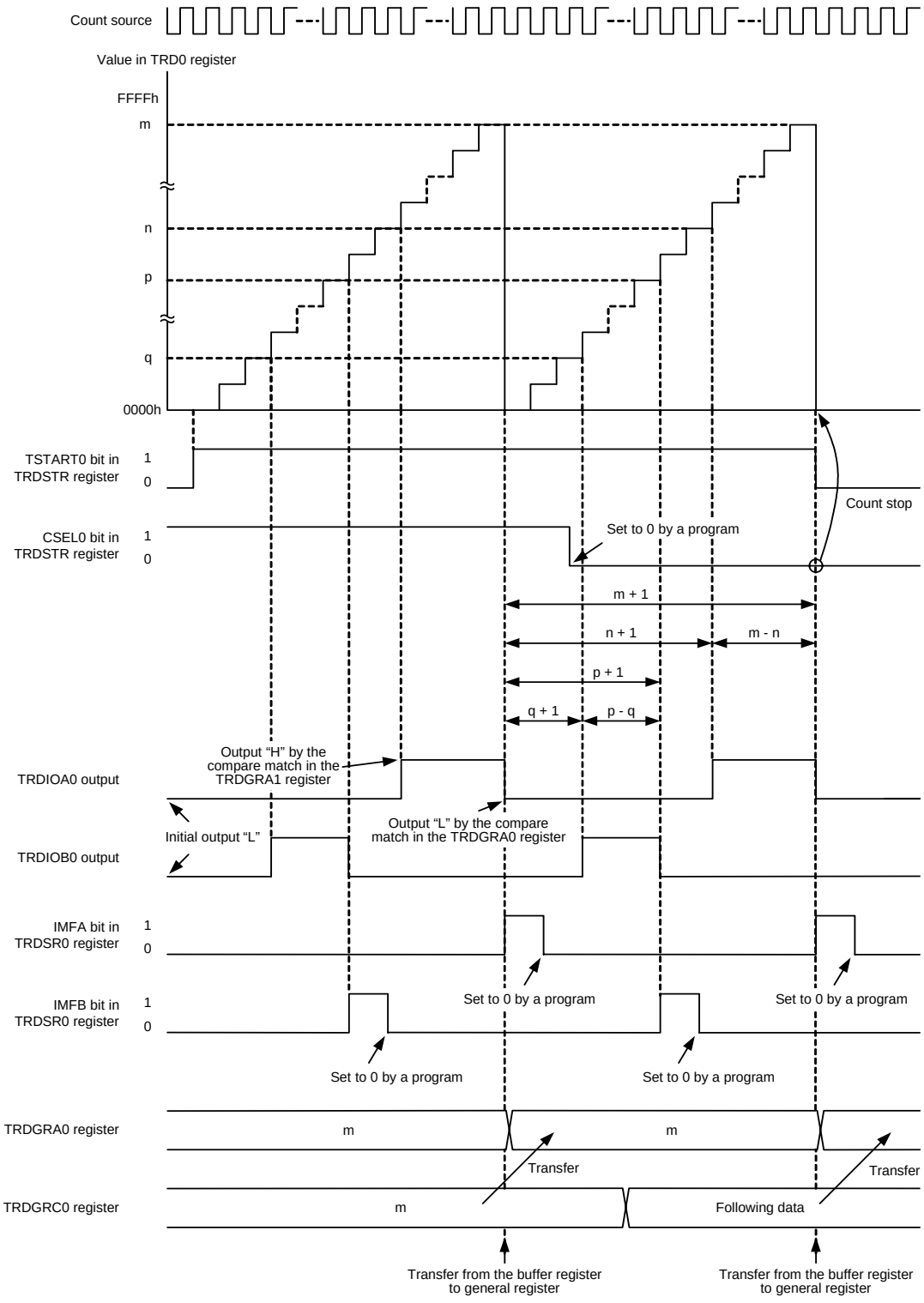


Figure 14.108 Operating Example of PWM3 Mode

14.3.11 Timer RD Interrupt

Timer RD generates the Timer RD interrupt request based on 6 sources every channel. The Timer RD interrupt has 1 TRDiIC register (IR bit, ILVL0 to ILVL2 bits) every channel, and 1 vector.
Table 14.35 lists the Registers Associated with Timer RD Interrupt and Figure 14.109 shows the Block Diagram of Timer RD Interrupt.

Table 14.35 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Channel 0	TRDSR0	TRDIER0	TRD0IC
Channel 1	TRDSR1	TRDIER1	TRD1IC

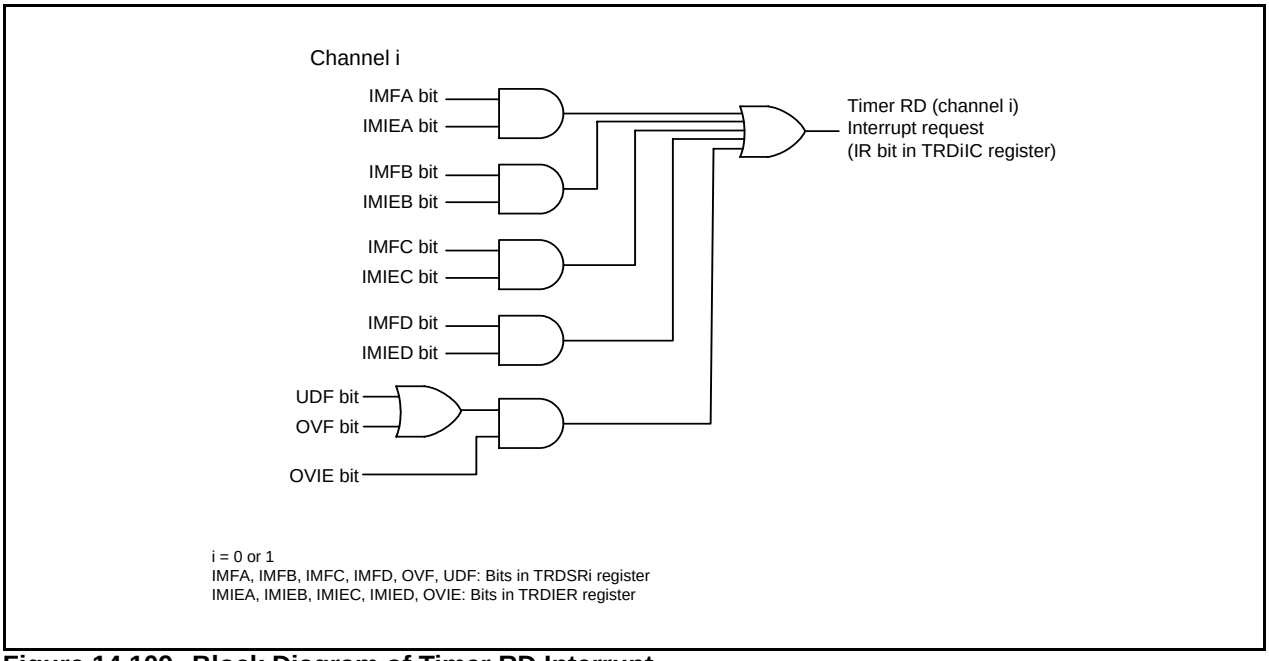


Figure 14.109 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (enable interrupt), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both of them, are set to 0, the IR bit is set to 0 (interrupt not requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained.
- When the conditions of other request sources are met, the IR bit remains 1.
- When multiple bits in the TRDIERi register are set to 1, which request source causes an interrupt is determined by the TRDSRi register.
- Since each bit in the TRDSRi register is not automatically set to 0 even if the interrupt is acknowledged, set each bit to 0 in the interrupt routine. For information on how to set these bits to 0, refer to the descriptions of the registers used in the different modes (**Figures 14.41, 14.56, 14.69, 14.81, 14.92 and 14.104**).

Refer to **Registers TRDSR0 to TRDSR1 in each mode (Figures 14.41, 14.56, 14.69, 14.81, 14.92 and 14.104)** for the TRDSRi register. Refer to **Registers TRDIER0 to TRDIER1 in each mode (Figures 14.42, 14.57, 14.70, 14.82, 14.93** and **14.105)** for the TRDIERi register.
Refer to **12.1.6 Interrupt Control** for the TRDiIC register and **12.1.5.2 Relocatable Vector Tables** for the interrupt vector.

14.3.12 Notes on Timer RD

14.3.12.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.
- When the CSELi (i = 0 or 1) is set to 0 (the count stops at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is set to 0.
  To stop counting by a program, set the TSTARTi bit to 0 after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with 1 instruction), the count cannot be stopped.
- Table 14.36 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji pin with the timer RD output.

Table 14.36 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	Hold the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	Hold the output level after output changes by compare match.

14.3.12.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid to overlap with the timing to set the TRDi register to 0000h, and then write. When the timing to set the TRDi register to 0000h overlaps with the timing to write the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by the CCLR2 to CCLR0 bits in the TRDCRi register.
  - 001b (clear by the TRDi register at the compare match with the TRDGRAi register)
  - 010b (clear by the TRDi register at the compare match with the TRDGRBi register.)
  - 011b (synchronous clear)
  - 101b (clear by the TRDi register at the compare match with the TRDGRCi register.)
  - 110b (clear by the TRDi register at the compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program Example     MOV.W   #XXXXh, TRD0    ;Writing
                    JMP.B   L1              ;JMP.B
                L1: MOV.W   TRD0,DATA       ;Reading
```

14.3.12.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program Example     MOV.B   #XXh, TRDSR0    ;Writing
                    JMP.B   L1              ;JMP.B
                L1: MOV.B   TRDSR0,DATA     ;Reading
```

14.3.12.4 Count Source Switch

- When switching the count source, switch it after the count stops.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change the TCK2 to TCK0 bits in the TRDCRi register.

- When changing the count source from fOCO40M to the other and stopping fOCO40M, wait 2 cycles or more of f1 after setting the clock switch, and then stop fOCO40M.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change the TCK2 to TCK0 bits in the TRDCRi register.
(3) Wait 2 cycles or more of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator stops).

14.3.12.5 Input Capture Function

- Set the pulse width of input capture signal to 3 cycles or more of the Timer RD operation clock. (Refer to **Table 14.11 Timer RD Operation Clocks**.)
- The value in the TRDi register is transferred to the TRDGRji register after 2 to 3 cycles of the Timer RD operation clock since the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C or D) (no digital filter).

14.3.12.6 Reset Synchronous PWM Mode

- When reset synchronous PWM mode is used for motor control, use it with OLS0 = OLS1.
- Set to reset synchronous PWM mode in the following procedure:

Change procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set the CMD1 to CMD0 bits in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set the CMD1 to CMD0 bits to 01b (reset synchronous PWM mode).
(4) Set the registers associated with other Timer RD again.

14.3.12.7 Complementary PWM Mode

- When complementary PWM mode is used for motor control, use it with OLS0 = OLS1.
- Change the CMD1 to CMD0 bits in the TRDFCR register in the following procedure.

Change procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set the CMD1 to CMD0 bits in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode)
(3) Set the DMD1 to CMD0 bits to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other Timer RD again.

Change procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and CSEL1 bits in the TRDSTR register to 0 (count stops).
(2) Set the CMD1 to CMD bits to 00b (other than reset synchronous PWM mode, complementary PWM mode)

- Do not write to the TRDGRA0, TRDGRB0, TRDGRA1 and TRDGRB1 registers during operation. When changing the PWM waveform, transfer the value written to the TRDGRD0, TRDGRC1 and TRDGRD1 registers to the TRDGRB0, TRDGRA1 and TRDGRB1 registers using the buffer operation. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register). The PWM period cannot be changed.

- When the value in the TRDGRA0 register is assumed as m, the TRD0 register counts order of m - 1, m, m + 1, m, m - 1 when changing from increment to decrement.
  When changing from m to m + 1, the IMFA bit is set to 1. Also, the CMD1 to CMD0 bits in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred by the compare match in the TRD0 and TRDGRA0 registers), the content in the buffer register (TRDGRD0, TRDGRC1, TRDGRD1) is transferred to the general register (TRDGRB0, TRDGRA1, TRDGRB1).
  For the order of m + 1, m, m - 1 operation, the IMFA bit remains unchanged and data are not transferred to the register such as the TRDGRA0 register.

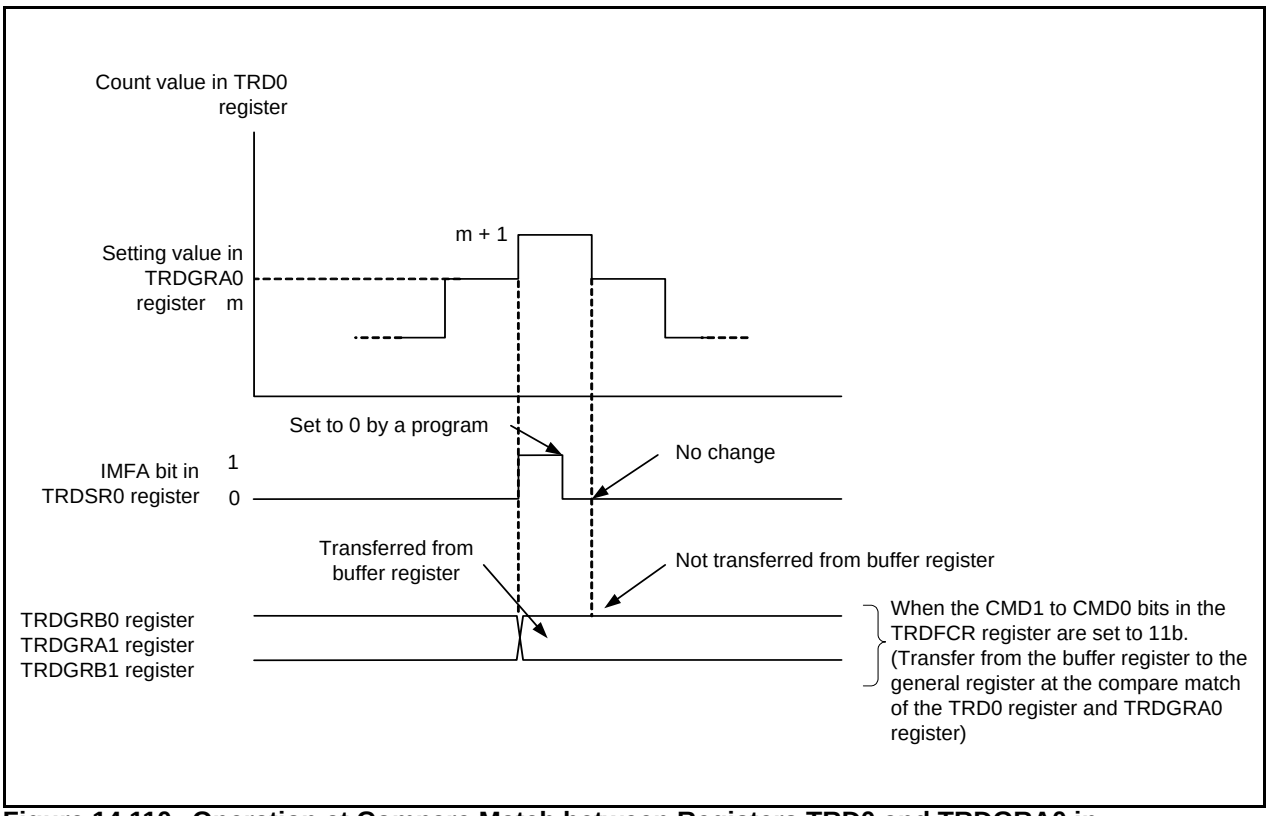


Figure 14.110 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts the order of 1, 0, FFFFh, 0, 1 when changing from decrement to increment. The UDF bit is set to 1 by the order of 1, 0, FFFFh operation. Also, when the CMD1 to CMD0 bits in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred by the underflow in the TRD1 register), the content in the buffer register (TRDGRD0, TRDGRC1, TRDGRD1) is transferred to the general register (TRDGRB0, TRDGRA1, TRDGRB1). For the order of FFFFh, 0, 1 operation, data are not transferred to the register such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

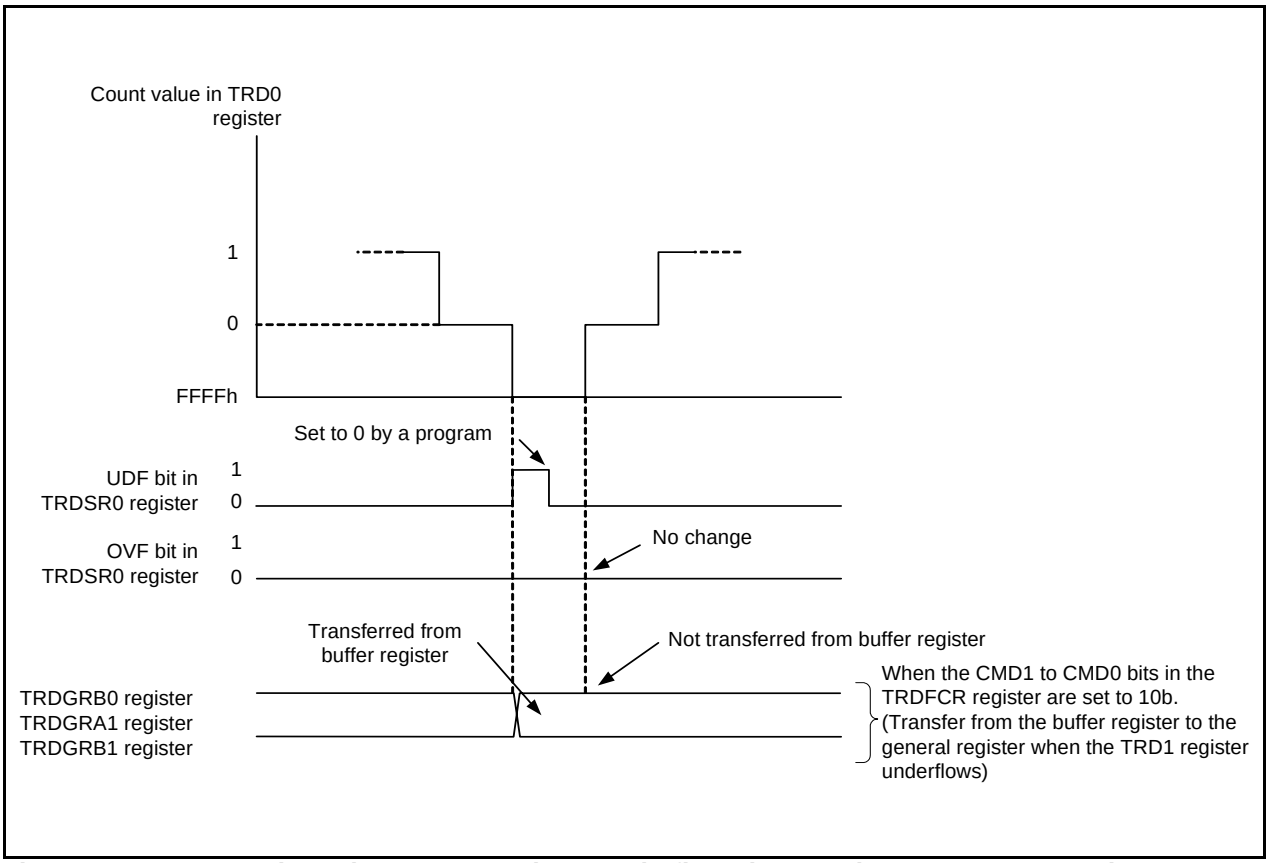
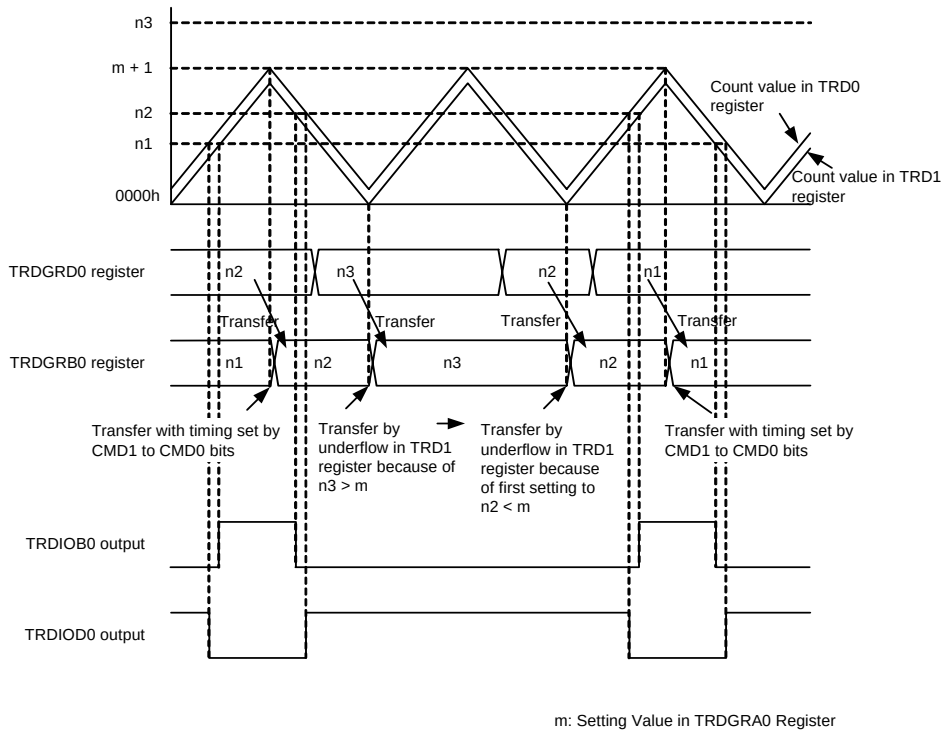


Figure 14.111 Operation When TRD1 Register Underflows in Complementary PWM Mode

- Select with the CMD1 to CMD0 bits for the data transfer timing from the buffer register to the general register. However, transfer with the following timing in spite of the value of the CMD1 to CMD0 bits for the following cases:

  Value in buffer register ≥ Value in TRDGRA0 register:
  Transfer at the underflow in the TRD1 register.
  And then, when setting the buffer register to 0001h or above and the smaller value than the one in the TRDGRA0 register, and the TRD1 register underflows in the fist time after setting, the value is transferred to the general register. After that, transfer the value with the timing selected by the CMD1 to CMD0 bits.



The above applies to the following conditions:
- The CMD1 to CMD0 bits in the TRDFCR register are set to 11b.
  (Data in the buffer register is transferred at the compare match in the TRD0 and TRDGRA0 registers in complementary PWM mode.)
- Both the OSL0 and OLS1 bits in the TRDFCR are set to 1. (active 'H" for normal-phase and counter-phase)

Figure 14.112 Operation When Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode

When the value in the buffer register is set to 0000h:
Transfer by the compare match in the TRD0 and TRDGRA0 registers.
And then, when setting the buffer register to 0001h or above and the smaller value than the one in the TRDGRA0 register, and the compare match in the TRD0 and TRDGRA0 registers in the fist time after setting, the value is transferred to the general register. After that, transfer the value with the timing selected by the CMD1 to CMD0 bits.

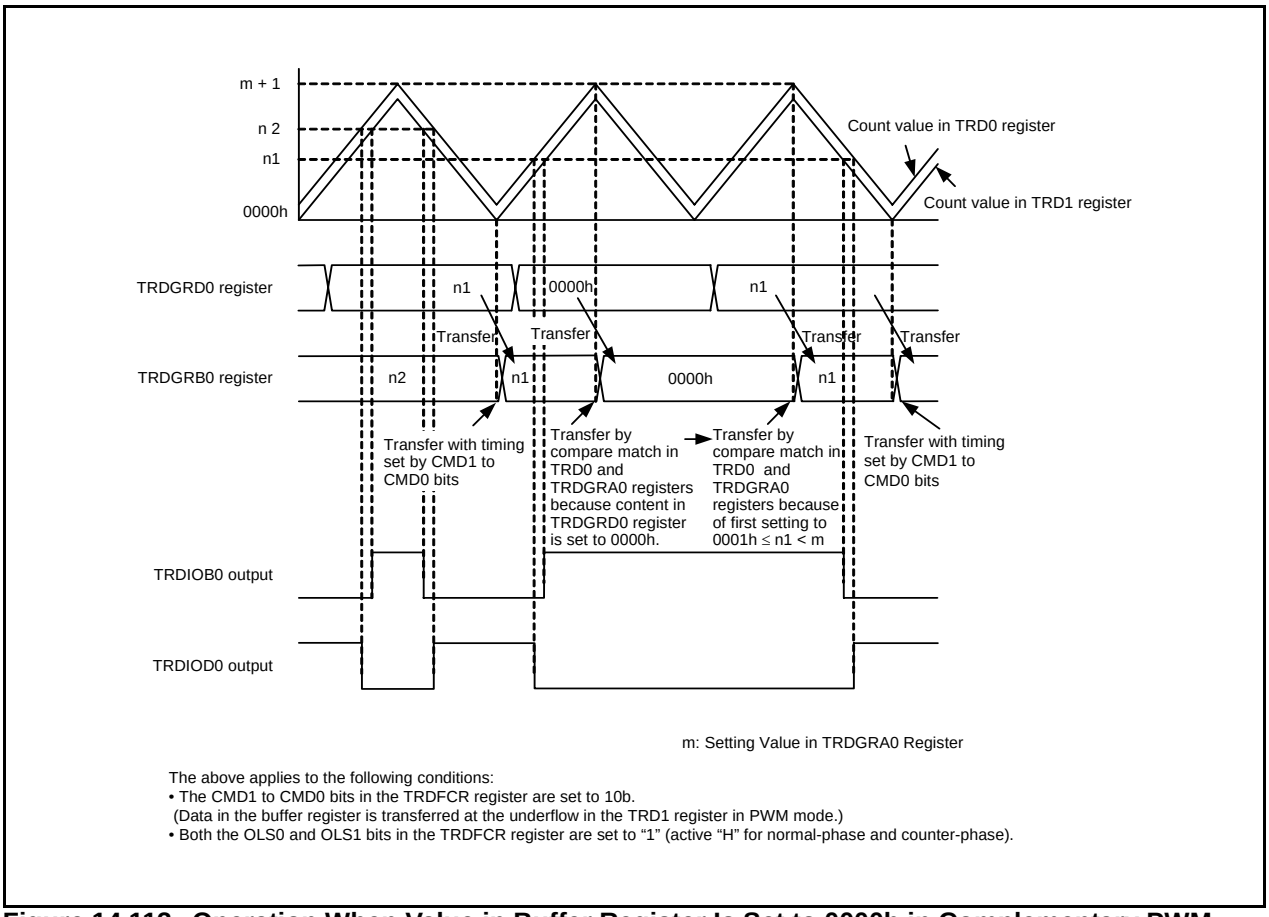


Figure 14.113 Operation When Value in Buffer Register Is Set to 0000h in Complementary PWM Mode

14.3.12.8 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 3.0 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (select fOCO40M as the count source).

14.4 Timer RE

Timer RE has the 4-bit counter and 8-bit counter. Timer RE has the following mode:

- Output compare mode Count a count source and detect the compare match

The count source for timer RE is the operating clock that regulates the timing of timer operations.

14.4.1 Output Compare Mode

The output compare mode is to count the internal count source divided-by-2 using the 4-bit or 8-bit counter and detect the compare value match with the 8-bit counter.
Figure 14.114 shows the Block Diagram of Output Compare Mode and Table 14.37 lists the Output Compare Mode Specifications. Figures 14.115 to 14.119 show the Registers Associated with Output Compare Mode and Figure 14.120 shows the Operation in Output Compare Mode.

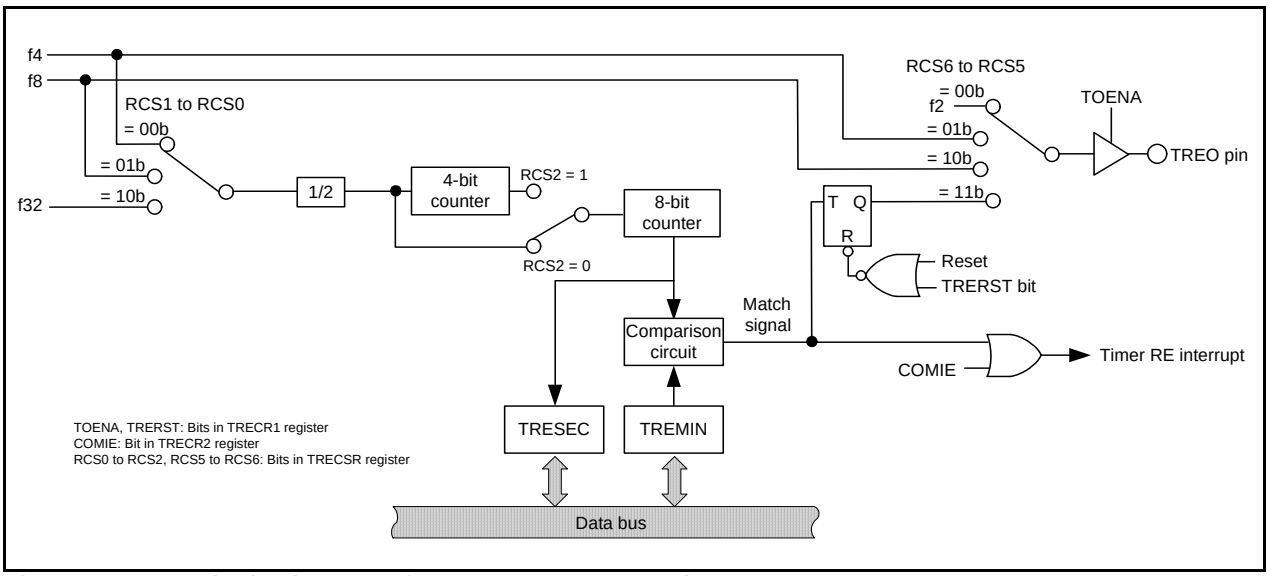
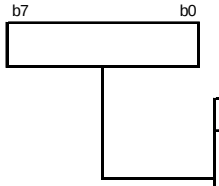


Figure 14.114 Block Diagram of Output Compare Mode

Table 14.37 Output Compare Mode Specifications

Item	Specification
Count Source	f4, f8, f32
Count Operation	• Increment • When the 8-bit counter content matches with the TREMIN register content, the value returns to 00h and count continues. The count value is held while count stops.
Count Period	• When RCS2 = 0 (4-bit counter is not used) 1/fi x 2 x (n + 1) • When RCS2 = 1 (4-bit counter is used) 1/fi x 32 x (n + 1) fi: Frequency of count source n: Setting value of TREMIN register
Count Start Condition	Write 1 (count starts) to the TSTART bit in the TRECR1 register
Count Stop Condition	Write 0 (count stops) to the TSTART bit in the TRECR1 register
Interrupt Request Generation Timing	When the 8-bit counter content matches with the TREMIN register content
TREO Pin Function	Select any one of the followings: • Programmable I/O ports • Output any one of f2, f4 and f8 • Compare output
Read from Timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to Timer	Writing to the TRESEC register is disabled. When the TSTART and TCSTF bits in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Select Functions	• Select use of 4-bit counter • Compare output function Every time the 8-bit counter value matches with the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs “L” after reset is deasserted and the Timer RE reset by the TRERST bit in the TRECR1 register. Output level is held by setting the TSTART bit to 0 (count stops).

Timer RE Counter Data Register

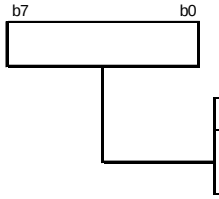


Symbol	Address	After Reset
TRESEC	0118h	00h

Function	RW
8-bit counter data can be read. Although Timer RE stops counting, the count value is held. The TRESEC register is set to 00h with the compare match.	RO

Figure 14.115 TRESEC Register in Output Compare Mode

Timer RE Compare Data Register

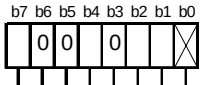


Symbol	Address	After Reset
TREMIN	0119h	00h

Function	RW
8-bit compare data is stored.	RW

Figure 14.116 TREMIN Register in Output Compare Mode

Timer RE Control Register 1

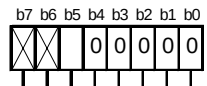


Symbol	Address	After Reset
TRECR1	011Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCSTF	Timer RE count status flag	0 : During count stop 1 : In count	RO
TOENA	TREO pin output enable bit	0 : Disable clock output 1 : Enable clock output	RW
INT	Interrupt request timing bit	Set to 0 in output compare mode	RW
TRERST	Timer RE reset bit	When setting this bit to 0 after setting it to 1, the followings will occur. • The TRESEC, TREMIN, and TRECR2 registers are set to 00h. • The TCSTF, INT, and TSTART bits in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	RW
— (b6-b5)	Reserved bit	Set to 0	RW
TSTART	Timer RE count start bit	0 : Count stops 1 : Count starts	RW

Figure 14.117 TRECR1 Register in Output Compare Mode

Timer RE Control Register 2

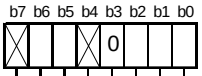


Symbol	Address	After Reset
TRECR2	011Dh	00h

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	Reserved bit	Set to 0	RW
COMIE	Compare match interrupt enable bit	0 : Disable compare match interrupt 1 : Enable compare match interrupt	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.118 TRECR2 Register in Output Compare Mode

Timer RE Count Source Select Register



Symbol	Address	After Reset
TRECSR	011Eh	08h

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bit	b1 b0 0 0 : f4 0 1 : f8 1 0 : f32 1 1 : Do not set	RW
RCS1			RW
RCS2	4-bit counter select bit	0 : Not used 1 : Used	RW
— (b3)	Reserved bit	Set to 0	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RCS5	Clock output select bit(1)	b6 b5 0 0 : f2 0 1 : f4 1 0 : f8 1 1 : Compare output	RW
RCS6			RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Write to the RCS5 to RCS6 bits when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

Figure 14.119 TRECSR Register in Output Compare Mode

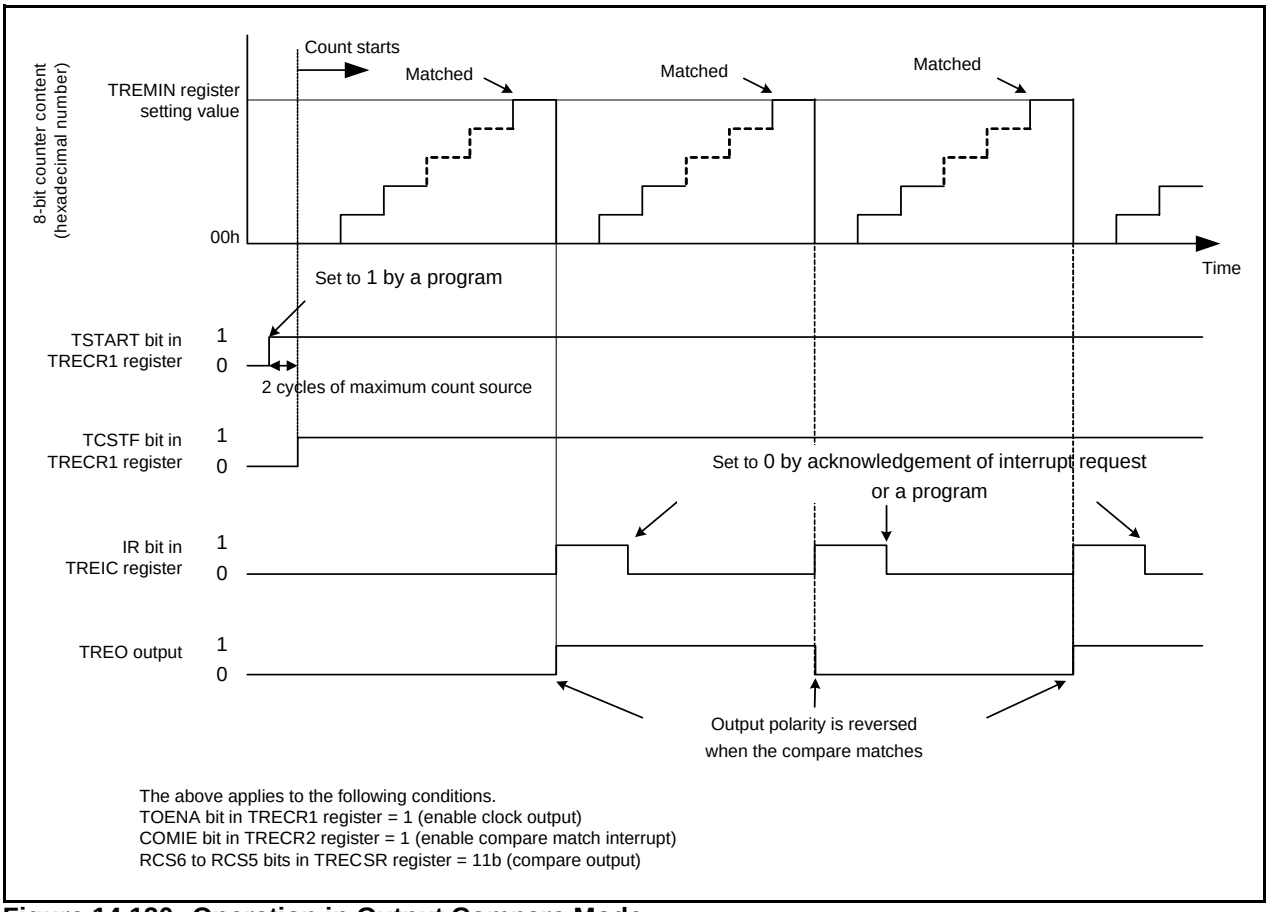


Figure 14.120 Operation in Output Compare Mode

14.4.2 Notes on Timer RE

14.4.2.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing count start or stop, and the TCSTF bit which indicates count start or stop. The TSTART and TCSTF bits are in the TRECR1 register.
Timer RE starts counting when setting the TSTART bit to 1 (count starts) and the TCSTF bit is set to 1 (count starts). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with Timer RE(1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with Timer RE: TRESEC, TREMIN, TRECR1, TRECR2, TRECSR

14.4.2.2 Register Setting

Write to the following registers or bits while timer RE stops.

- TRESEC and TRECR2 registers
- The INT bit in TRECR1 register
- RCS0 to RCS2 bits in TRECSR register

The state while Timer RE stops is indicated as the state where the TSTART and TCSTF bits in the TRECR1 register are set to 0 (timer RE stops).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.

15. Serial Interface

Serial Interface is configured with two channels: UART0 and UART1. Each UART0 and Uart1 has an exclusive timer to generate a transfer clock and they operate independently.
Figure 15.1 shows the UARTi (i = 0 or 1) Block Diagram. Figure 15.2 shows the UARTi (i = 0 or 1) Transmit/Receive Unit.
UART0 has two modes: clock synchronous serial I/O mode, and clock asynchronous serial I/O mode (UART mode).
UART1 has only one mode: clock asynchronous serial interface mode (UART mode).
Figures 15.3 to 15.6 show the Registers Associated with UARTi.

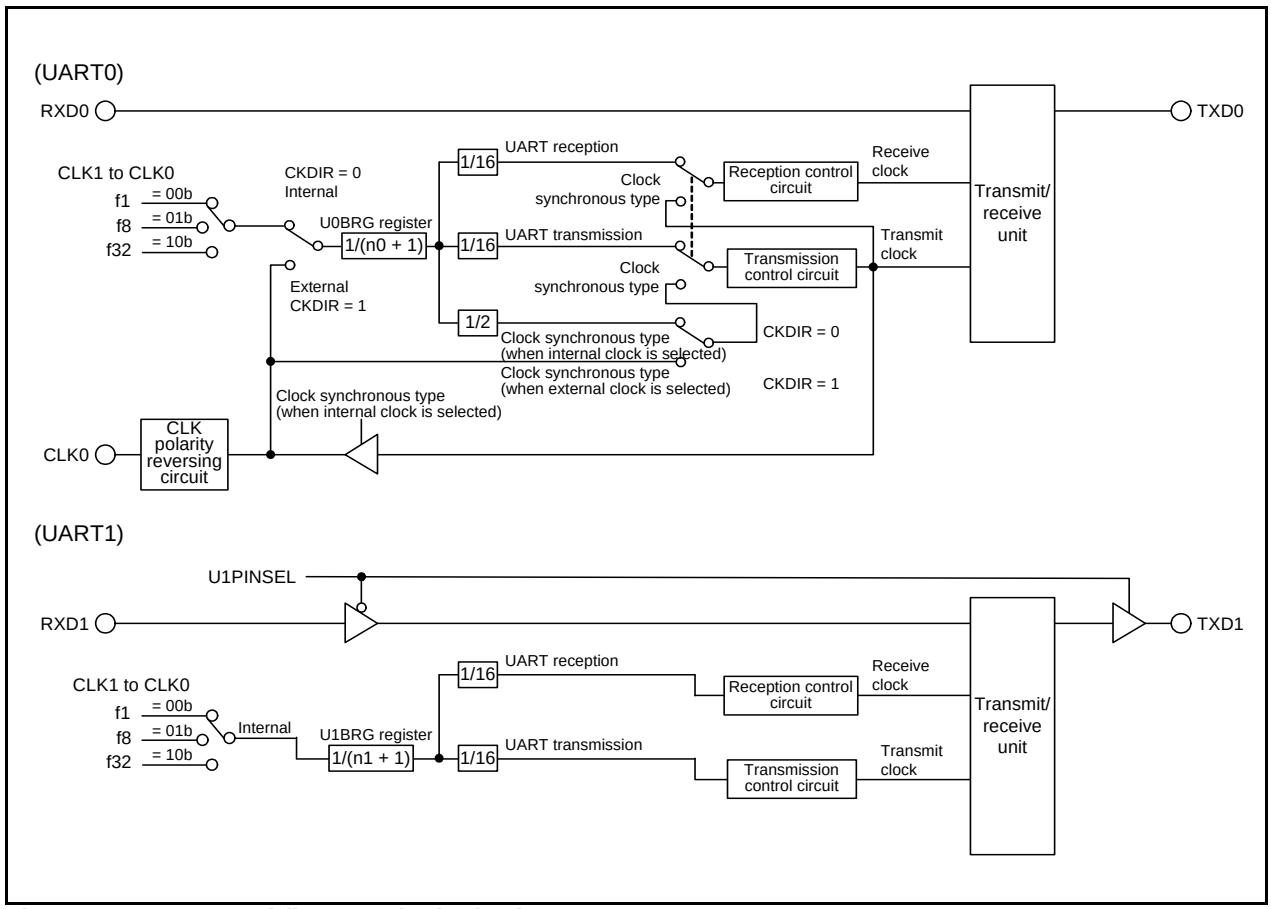


Figure 15.1 UARTi (i = 0 or 1) Block Diagram

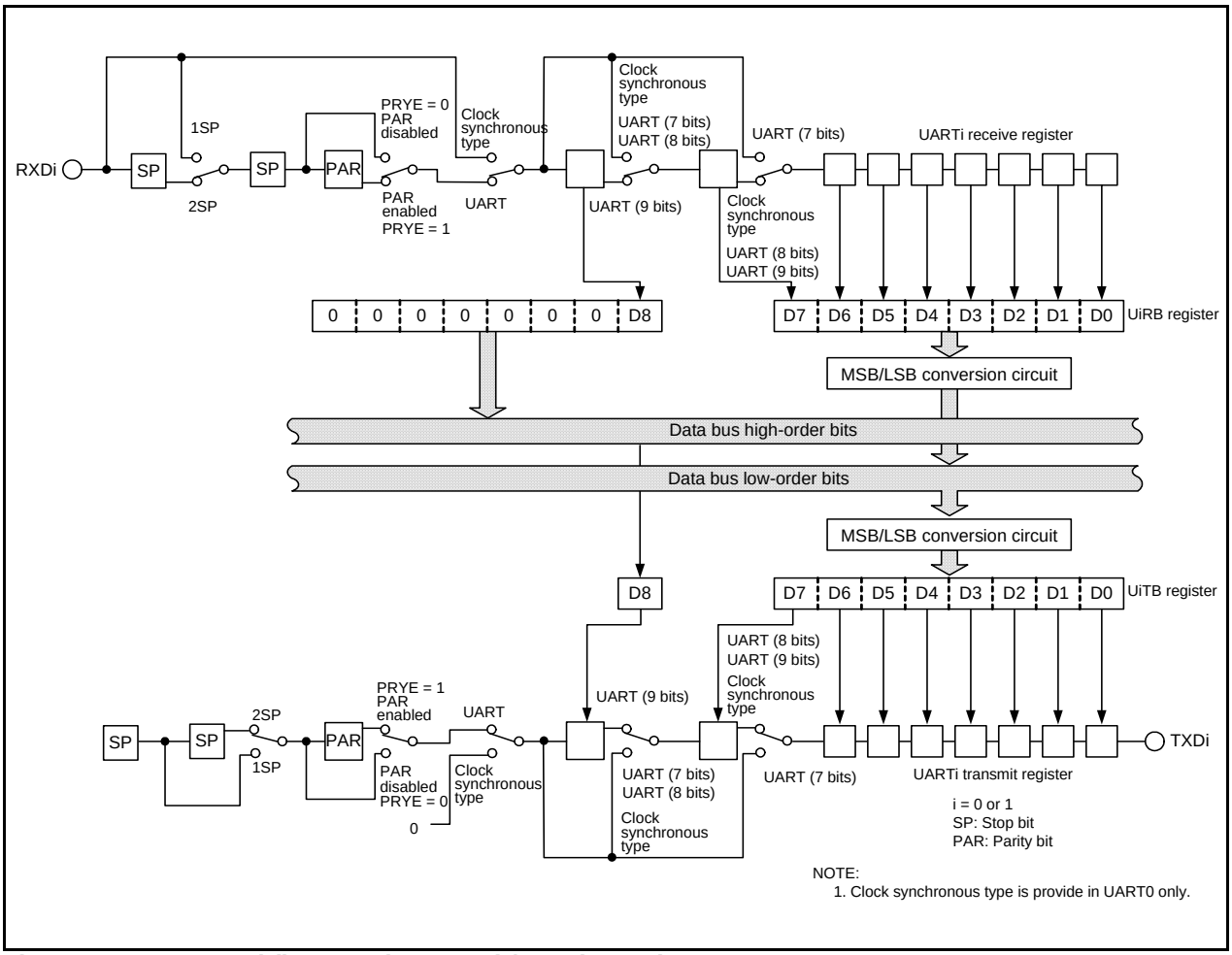
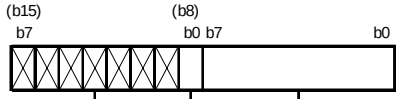


Figure 15.2 UARTi (i = 0 or 1) Transmit/Receive Unit

UARTi Transmit Buffer Register (i = 0 or 1)(1,2)

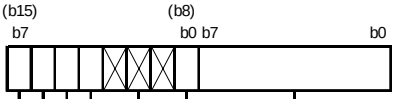


Symbol	Address	After Reset
U0TB	00A3h-00A2h	Indeterminate
U1TB	00ABh-00AAh	Indeterminate

Bit Symbol	Function	RW
— (b8-b0)	Transmit data	WO
— (b15-b9)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.	—

NOTES:
1. When the transfer data length is 9-bit long, write to high-byte data first then low-byte data.
2. Use the MOV instruction to write to this register.

UARTi Receive Buffer Register (i = 0 or 1)(1)

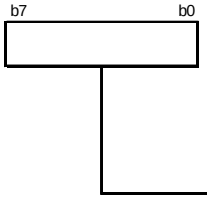


Symbol	Address	After Reset
U0RB	00A7h-00A6h	Indeterminate
U1RB	00AFh-00AEh	Indeterminate

Bit Symbol	Bit Name	Function	RW
— (b7-b0)	—	Receive data (D7 to D0)	RO
— (b8)	—	Receive data (D8)	RO
— (b11-b9)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.		—
OER	Overrun error flag(2)	0 : No overrun error 1 : Overrun error	RO
FER	Framing error flag(2)	0 : No framing error 1 : Framing error	RO
PER	Parity error flag(2)	0 : No parity error 1 : Parity error	RO
SUM	Error sum flag(2)	0 : No error 1 : Error	RO

NOTES:
1. Read out the UiRB register in 16-bit unit.
2. The SUM, PER, FER and OER bits are set to 0 (no error) when the SMD2 to SMD0 bits in the UiMR register are set to 000b (serial interface disabled) or the RE bit in the U0C1 register is set to 0 (receive disable). The SUM bit is set to 0 (no error) when the PER, FER and OER bits are set to 0 (no error). Also, the PER and FER bits are set to 0 when the higher byte of the UiRB register is read out.

UARTi Bit Rate Register (i = 0 or 1)(1,2,3)



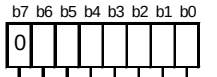
Symbol	Address	After Reset
U0BRG	00A1h	Indeterminate
U1BRG	00A9h	Indeterminate

Function	Setting Range	RW
Assuming that set value is n, UiBRG divides the count source by n+1	00h to FFh	WO

NOTES:
1. Write to this register while the serial interface is neither transmitting nor receiving.
2. Use the MOV instruction to write to this register.
3. After setting the CLK0 to CLK1 bits in the UiC0 register, write to the UiBRG register.

Figure 15.3 Registers UiTB, UiRB, and UiBRG (i = 0 or 1)

UARTi Transmit/Receive Mode Register (i = 0 or 1)



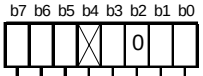
Symbol	Address	After Reset
U0MR	00A0h	00h
U1MR	00A8h	00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit(2,4)	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Other than above : Do not set	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit(3)	0 : Internal clock 1 : External clock(1)	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Enables when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
— (b7)	Reserved bit	Set to 0	RW

NOTES:
1. Set the PD1_6 bit in the PD1 register to 0 (input).
2. Do not set bits SMD2 to SMD0 in the U1MR register to any values other than 000b, 100b, 101b and 110b.
3. Set the CKDIR bit to 0 (internal clock) in UART1.
4. The SMD2 to SMD1 bits can not select clock synchronous serial I/O mode in UART1.

Figure 15.4 UiMR Register (i = 0 or 1)

UARTi Transmit/Receive Control Register 0 (i = 0 or 1)

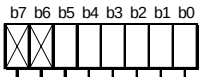


Symbol	Address	After Reset
U0C0	00A4h	00001000b
U1C0	00ACh	00001000b

Bit Symbol	Bit Name	Function	RW
CLK0	BRG count source select bit(1)	b1 b0 0 0 : Selects f1 0 1 : Selects f8 1 0 : Selects f32 1 1 : Do not set	RW
CLK1			RW
— (b2)	Reserved bit	Set to 0	RW
TXEPT	Transmit register empty flag	0 : Data in transmit register (during transmit) 1 : No data in transmit register (transmit completed)	RO
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
NCH	Data output select bit	0 : TXDi pin is a pin of CMOS output 1 : TXDi pin is a pin of N-channel open drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	RW

NOTE:
1. If the BRG count source is switched, set the UiBRG register again.

UARTi Transmit/Receive Control Register 1 (i = 0 or 1)



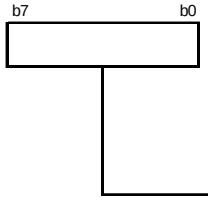
Symbol	Address	After Reset
U0C1	00A5h	00000010b
U1C1	00ADh	00000010b

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Disables transmit 1 : Enables transmit	RW
TI	Transmit buffer empty flag	0 : Data in UiTB register 1 : No data in UiTB register	RO
RE	Receive enable bit	0 : Disables receive 1 : Enables receive	RW
RI	Receive complete flag(1)	0 : No data in UiRB register 1 : Data in UiRB register	RO
UiIRS	UARTi transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmit completed (TXEPT = 1)	RW
UiRRM	UARTi continuous receive mode enable bit(2)	0 : Disables continuous receive mode 1 : Enables continuous receive mode	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The RI bit is set to 0 when the higher byte of the UiRB register is read out.
2. Set the UiRRM bit to 0 (disables continuous receive mode) in UART mode.

Figure 15.5 Registers UiC0 and UiC1 (i = 0 or 1)

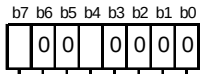
UART1 Function Select Register



Symbol	Address	After Reset
U1SR	00F5h	Indeterminate

Function	RW
Set to 03h when using UART1. As a result, UART1 can be used as the clock asynchronous serial I/O. Do not set values other than 03h. When read, its content is indeterminate.	WO

Port Mode Register



Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0	—
U1PINSEL	Port TXD1/RXD1 switch bit	0 : I/O port P6_6, P6_7 1 : TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0	—
IICSEL	SSU/I²C bus switch bit	0 : SSU function selects 1 : I²C bus function selects	RW

Figure 15.6 Registers U1SR and PMR

15.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode is mode to transmit and receive data using a transfer clock. This mode is selected in UART0 only.
Table 15.1 lists the Clock Synchronous Serial I/O Mode Specifications. Table 15.2 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode(1).

Table 15.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer Data Format	• Transfer data length: 8 bits
Transfer Clocks	• CKDIR bit in U0MR register is set to 0 (internal clock): fi/(2(n + 1)) fi = f1, f8, f32 n = setting value in U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): input from CLK0 pin
Transmit Start Conditions	• Before transmit starts, the following requirements are required(1) - The TE bit in the U0C1 register is set to 1 (transmit enabled) - The TI bit in the U0C1 register is set to 0 (data in the U0TB register)
Receive Start Conditions	• Before receive starts, the following requirements are required(1) - The RE bit in the U0C1 register is set to 1 (receive enabled) - The TE bit in the U0C1 register is set to 1 (transmit enabled) - The TI bit in the U0C1 register is set to 0 (data in the U0TB register)
Interrupt Request Generation Timing	• When transmit, one of the following conditions can be selected - The U0IRS bit is set to 0 (transmit buffer empty): when transferring data from the U0TB register to UART0 transmit register (when transmit starts) - The U0IRS bit is set to 1 (transmit completes): when completing transmit data from UARTi transmit register • When receive When transferring data from the UART0 receive register to the U0RB register (when receive completes)
Error Detection	• Overrun error(2) This error occurs if serial interface starts receiving the following data before reading the U0RB register and receives the 7th bit of the following data
Select Functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock • LSB first, MSB first selection Whether transmitting or receiving data beginning with the bit 0 or beginning with the bit 7 can be selected • Continuous receive mode selection Receive is enabled immediately by reading the U0RB register

NOTES:
1. When an external clock is selected, meet the conditions while the CKPOL bit in the U0C0 register is set to 0 (transmit data output at the falling edge and the receive data input at the rising edge of the transfer clock), the external clock is held “H”; if the CKPOL bit in the U0C0 register is set to 1 (transmit data output at the rising edge and the receive data input at the falling edge of the transfer clock), the external clock is held “L”.
2. If an overrun error occurs, the receive data (b0 to b8) of the U0RB register will be undefined. The IR bit in the S0RIC register remains unchanged.

Table 15.2 Registers Used and Settings in Clock Synchronous Serial I/O Mode(1)

Register	Bit	Function
U0TB	0 to 7	Set transmit data
U0RB	0 to 7	Receive data can be read
	OER	Overrun error flag
U0BRG	0 to 7	Set bit rate
U0MR	SMD2 to SMD0	Set to 001b
	CKDIR	Select the internal clock or external clock
U0C0	CLK1 to CLK0	Select the count source in the U0BRG register
	TXEPT	Transmit register empty flag
	NCH	Select TXD0 pin output mode
	CKPOL	Select the transfer clock polarity
	UFORM	Select the LSB first or MSB first
U0C1	TE	Set this bit to 1 to enable transmit/receive
	TI	Transmit buffer empty flag
	RE	Set this bit to 1 to enable reception
	RI	Reception complete flag
	U0IRS	Select the UART0 transmit interrupt source
	U0RRM	Set this bit to 1 to use continuous receive mode

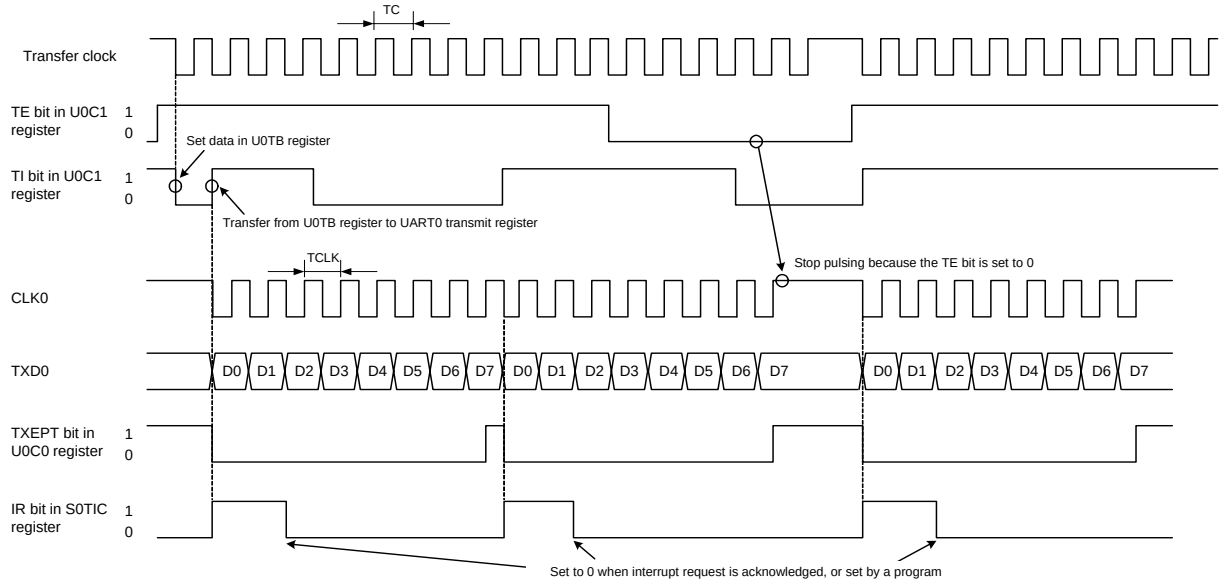
NOTE:
1. Set bits which are not in this table to 0 when writing to the registers in clock synchronous serial I/O mode.

Table 15.3 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode. The TXD0 pin outputs “H” level between the operating mode selection of UART0 and transfer start, an “H” (If the NCH bit is set to 1 (the N-channel open-drain output), this pin is in a high-impedance state.)

Table 15.3 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0(P1_4)	Output serial data	(Outputs dummy data when performing receive only)
RXD0(P1_5)	Input serial data	The PD1_5 bit in the PD1 register = 0 (P1_5 can be used as an input port when performing transmit only)
CLK0(P1_6)	Output transfer clock	The CKDIR bit in the U0MR register = 0
	Input transfer clock	The CKDIR bit in the U0MR register = 1 PD1_6 bit in PD1 register = 0

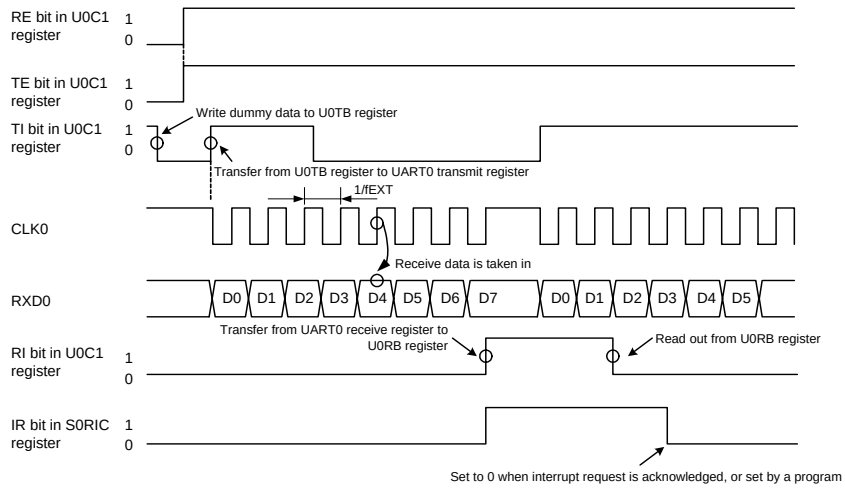
• Example of transmit timing (when internal clock is selected)



TC = TCLK = 2(n+1)/fi
fi: Frequency of UiBRG count source (f1, f8, f32)
n: Setting value to UiBRG register

The above applies under the following settings:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0 (output transmit data at the falling edge and input receive data at the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0 (an interrupt request is generated when the transmit buffer is empty)

• Example of receive timing (when external clock is selected)



The above applies under the following settings:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0 (output transmit data at the falling edge and input receive data at the rising edge of the transfer clock)

The following conditions are met when “H” is applied to the CLK0 pin before receiving data:
- TE bit in U0C1 register = 1 (enables transmit)
- RE bit in U0C1 register = 1 (enables receive)
- Write dummy data to the U0TB register

fEXT: Frequency of external clock

Figure 15.7 Transmit and Receive Timing Example in Clock Synchronous Serial I/O Mode

15.1.1 Polarity Select Function

Figure 15.8 shows the Transfer Clock Polarity. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.

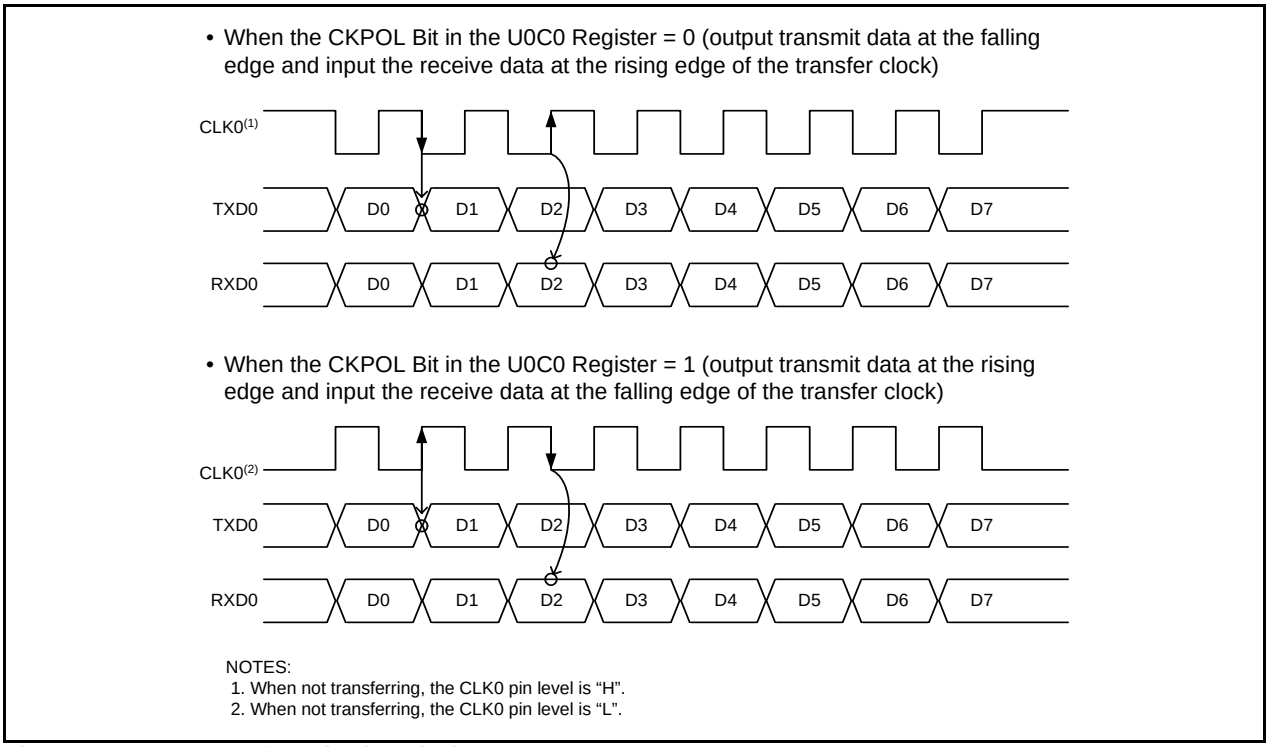


Figure 15.8 Transfer Clock Polarity

15.1.2 LSB First/MSB First Select Function

Figure 15.9 shows the Transfer Format. Use the UFORM bit in the U0C0 register to select the transfer format.

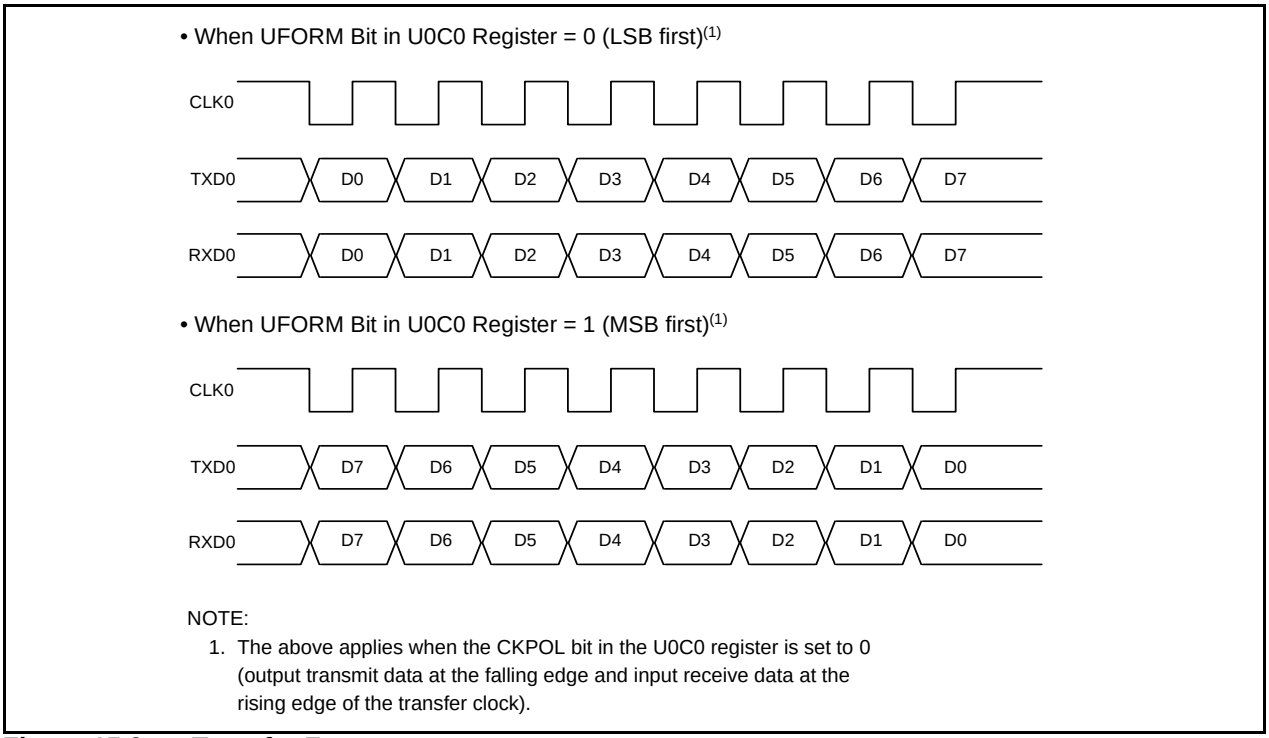


Figure 15.9 Transfer Format

15.1.3 Continuous Receive Mode

Continuous receive mode is held by setting the U0RRM bit in the U0C1 register to 1 (enables continuous receive mode). In this mode, reading U0RB register sets the TI bit in the U0C1 register to 0 (data in the U0TB register). When the U0RRM bit is set to 1, do not write dummy data to the U0TB register in a program.

15.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows transmit and receive data after setting the desired bit rate and transfer data format. Table 15.4 lists the UART Mode Specifications. Table 15.5 lists the Registers Used and Settings for UART Mode.

Table 15.4 UART Mode Specifications

Item	Specification
Transfer Data Formats	• Character bit (transfer data): selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: selectable from odd, even, or none • Stop bit: selectable from 1 or 2 bits
Transfer Clocks	• CKDIR bit in UiMR register is set to 0 (internal clock): fj/(16(n + 1)) fj = f1, f8, f32 n = setting value in U0BRG register: 00h to FFh • CKDIR bit is set to 1 (external clock): fEXT/(16(n + 1)) fEXT: Input from CLK0 pin n = setting value in UiBRG register: 00h to FFh
Transmit Start Conditions	• Before transmit starts, the following are required - TE bit in UiC1 register is set to 1 (transmit enabled) - TI bit in UiC1 register is set to 0 (data in UiTB register)
Receive Start Conditions	• Before receive starts, the following are required - RE bit in UiC1 register is set to 1 (receive enabled) - Detects start bit
Interrupt Request Generation Timing	• When transmitting, one of the following conditions can be selected - UiIRS bit is set to 0 (transmit buffer empty): when transferring data from the UiTB register to UARTi transmit register (when transmit starts) - UiIRS bit is set to 1 (transfer ends): when serial interface completes transmitting data from the UARTi transmit register • When receiving When transferring data from the UARTi receive register to UiRB register (when receive ends)
Error Detection	• Overrun error(1) This error occurs if serial interface starts receiving the following data before reading the UiRB register and receiving the bit one before the last stop bit of the following data • Framing error This error occurs when the number of stop bits set are not detected • Parity error This error occurs when parity is enabled, the number of 1's in parity and character bits do not match the number of 1's set • Error sum flag This flag is set is set to 1 when any of the overrun, framing, and parity errors is generated

i = 0 or 1

NOTE:

1. If an overrun error occurs, the receive data (b0 to b8) of the U0RB register will be undefined. The IR bit in the S0RIC register remains unchanged.

Table 15.5 Registers Used and Settings for UART Mode

Register	Bit	Function
UiTB	0 to 8	Set transmit data(1)
UiRB	0 to 8	Receive data can be read(1, 2)
	OER,FER,PER,SUM	Error flag
UiBRG	0 to 7	Set a bit rate
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7-bit long Set to 101b when transfer data is 8-bit long Set to 110b when transfer data is 9-bit long
	CKDIR	Select the internal clock or external clock(3)
	STPS	Select the stop bit
	PRY, PRYE	Select whether parity is included and odd or even
UiC0	CLK0, CLK1	Select the count source for the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode
	CKPOL	Set to 0
	UFORM	LSB first or MSB first can be selected when transfer data is 8-bit long. Set to 0 when transfer data is 7- or 9-bit long.
UiC1	TE	Set to 1 to enable transmit
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable receive
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source
	UiRRM	Set to 0

i = 0 or 1

NOTES:

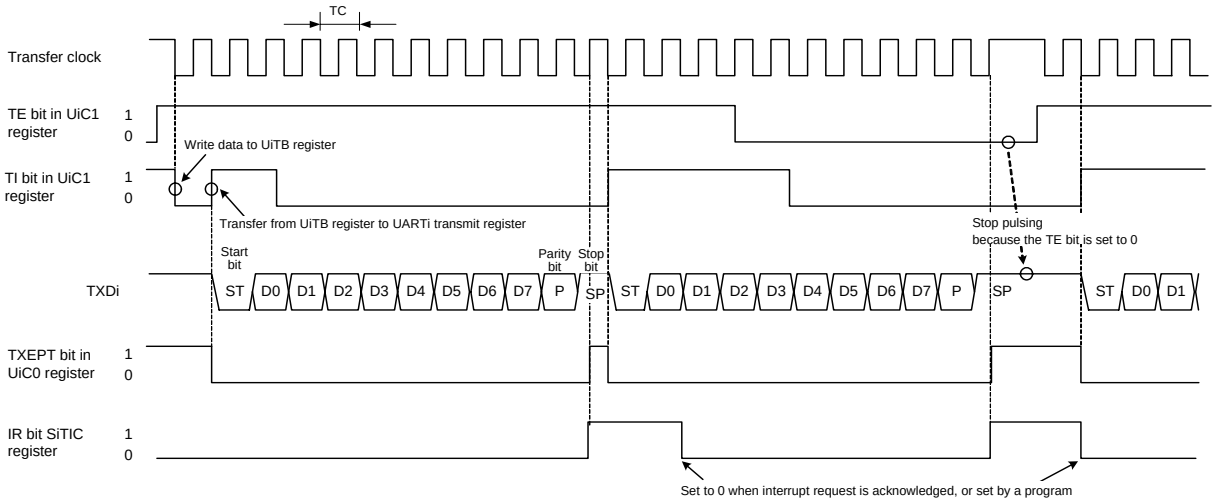
1. The bits used for transmit/receive data are as follows: Bits 0 to 6 when transfer data is 7-bit long; bits 0 to 7 when transfer data is 8-bit long; bits 0 to 8 when transfer data is 9-bit long.
2. The following bits are undefined: Bits 7 and 8 when transfer data is 7 bits long; bit 8 when transfer data is 8 bits long.
3. External clock can be selected in UART0 only.

Table 15.6 lists the I/O Pin Functions in UART Mode. After the UARTi (i = 0 or 1) operating mode is selected, the TXDi pin outputs “H” level (if the NCH bit is set to 1 (N-channel open-drain outputs), this pin is in a high-impedance state) until transfer starts.

Table 15.6 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0(P1_4)	Output serial data	(Cannot be used as a port when performing receive only)
RXD0(P1_5)	Input serial data	The PD1_5 bit in the PD1 register = 0 (P1_5 can be used as an input port when performing transmit only)
CLK0(P1_6)	Programmable I/O port	The CKDIR bit in the U0MR register = 0
	Input transfer clock	The CKDIR bit in the U0MR register = 1 The PD1_6 bit in the PD1 register = 0
TXD1(P6_6)	Output serial data	U1PINSEL bit in PMR register = 1 (Cannot be used as a port when performing receive only)
RXD1(P6_7)	Input serial data	U1PINSEL bit in PMR register = 1 The PD6_7bit in the PD6 register = 0 (P6_7 can be used as an input port when performing transmit only)

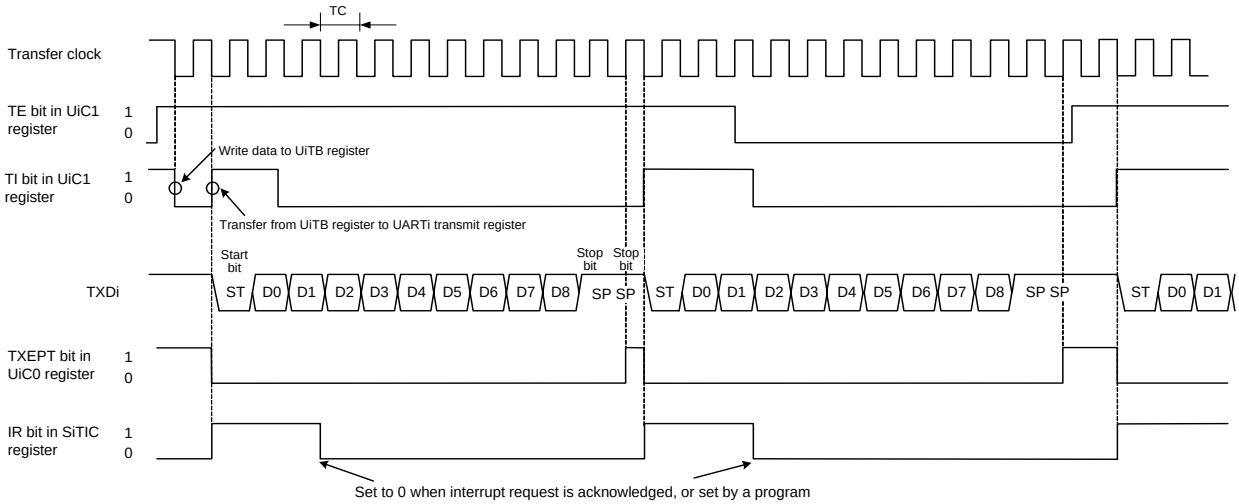
• Transmit timing when transfer data is 8 bits long (parity enabled, 1 stop bit)



The above timing diagram applies under the following conditions:
- PRYE bit in UiMR register = 1 (parity enabled)
- STPS bit in UiMR register = 0 (1 stop bit)
- UiIRS bit in UiC1 register = 1 (an interrupt request is generated when transmit completes)

TC=16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value to UiBRG register
i = 0 or 1

• Transmit timing when transfer data is 9 bits long (parity disabled, 2 stop bits)



The above timing diagram applies under the following conditions:
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 1 (2 stop bits)
- UiIRS bit in UiC1 register = 0 (an interrupt request is generated when transmit buffer is empty)

TC=16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value to UiBRG register
i = 0 or 1

Figure 15.10 Transmit Timing in UART Mode

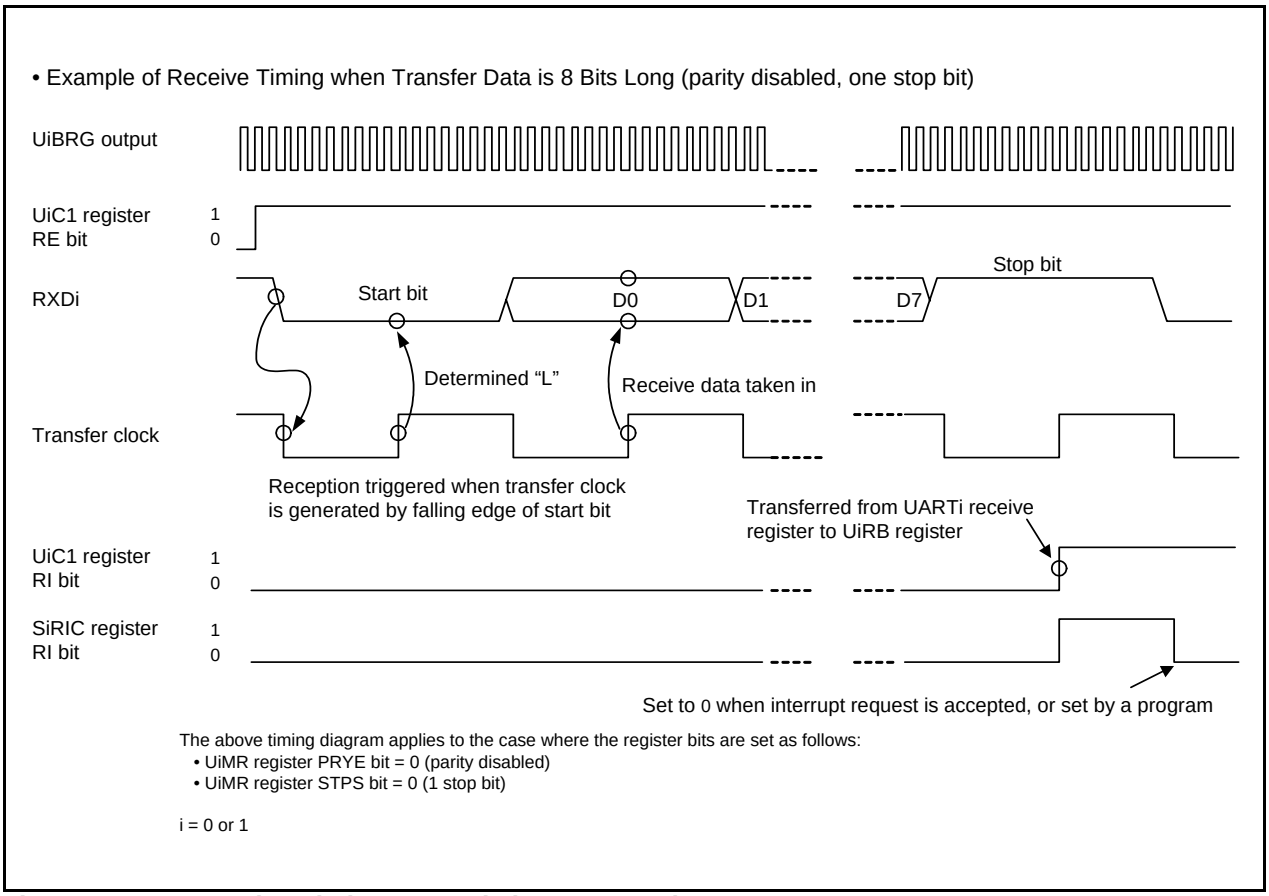


Figure 15.11 Receive Timing Example in UART Mode

15.2.1 Bit Rate

Divided-by-16 of frequency by the UiBRG (i = 0 or 1) register in UART mode is a bit rate.

<UART Mode>

• When selecting internal clock

$$\text{Setting value to the UiBRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj: Count source frequency of the UiBRG register (f1, f8 and f32)

• When selecting external clock

$$\text{Setting value to the UiBRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of the UiBRG register (external clock)
i = 0 or 1

Figure 15.12 Calculation Formula of UiBRG (i = 0 or 1) Register Setting Value

Table 15.7 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	UiBRG Count Source	System Clock = 20 MHz			System Clock = 8 MHz		
		UiBRG Setting Value	Actual Time (bps)	Setting Error(%)	UiBRG Setting Value	Actual Time (bps)	Setting Error(%)
1200	f8	129 (81h)	1201.92	0.16	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	16 (10h)	29411.76	2.12
31250	f1	39 (27h)	31250.00	0.00	15 (0Fh)	31250.00	0.00
38400	f1	32 (20h)	37878.79	-1.36	12 (0Ch)	38461.54	0.16
51200	f1	23 (17h)	52083.33	1.73	9 (09h)	50000.00	-2.34

i = 0 or 1

15.3 Notes on Serial Interface

- When reading data from the UiRB (i = 0 or 1) register even in the clock asynchronous serial I/O mode or in the clock synchronous serial I/O mode. Ensure to read data in 16-bit unit. When the high-order byte of the UiRB register is read, the PER and FER bits in the UiRB register and the RI bit in the UiC1 register are set to 0. To check receive errors, read the UiRB register and then use the read data.

Example (when reading receive buffer register):

```
MOV.W   00A6H,R0        ; Read the U0RB register
```

- When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, write data high-order byte first, then low-order byte in 8-bit units.

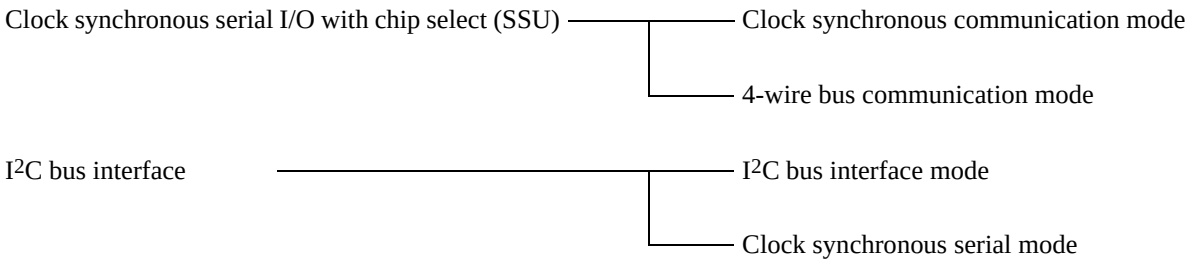
Example (when reading transmit buffer register):

```
MOV.B   #XXH,00A3H  ; Write the high-order byte of U0TB register
MOV.B   #XXH,00A2H  ; Write the low-order byte of U0TB register
```

16. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock Synchronous Serial Interface



The clock synchronous serial interface uses the registers of addresses 00B8h to 00BFh. Registers, bits, symbols and functions vary even in the same addresses depending on the modes. Refer to registers of each function for details. Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format and data output format.

16.1 Mode Selection

The clock synchronous serial interface contains 4 modes.
Table 16.1 lists the Mode Selections. Refer to **16.2 Clock Synchronous Serial I/O with Chip Select (SSU)** or after for details of each mode.

Table 16.1 Mode Selections

IICSEL Bit in PMR Register	Bit 7 in 00B8h (ICE Bit in ICCR1 Register)	Bit 0 in 00BDh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Clock synchronous serial I/O with chip select	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

16.2 Clock Synchronous Serial I/O with Chip Select (SSU)

The serial data of the clock synchronous can communicate for the clock synchronous serial I/O with chip select. Table 16.2 lists the Clock Synchronous Serial I/O with Chip Select Specifications and Figure 16.1 shows a Block Diagram of Clock Synchronous Serial I/O with Chip Select.
Figures 16.2 to 16.9 show Clock Synchronous Serial I/O with Chip Select Associated Registers.

Table 16.2 Clock Synchronous Serial I/O with Chip Select Specifications

Item	Specification
Transfer Data Format	• Transfer-data length 8 bits Continuous transmit and receive of serial data are enabled since both transmitter and receiver have buffer structure.
Operating Mode	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master / Slave Device	Selectable
I/O Pin	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin $\overline{\text{SSO}}$ (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip-select I/O pin
Transfer Clock	• When the MSS bit in the SSCRH register is set to 0 (operates as slave device), external clock can be selected. • When the MSS bit in the SSCRH register is set to 1 (operates as master device), internal clock (selects from f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4 and outputs from SSCK pin) can be selected. • Clock polarity and phase of SSCK can be selected.
Receive Error Detection	• Overrun error Overrun error occurs during receive and completes by error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and completing the next serial data receive, the ORER bit is set to 1.
Multimaster Error Detection	• Conflict error While the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if “L” applies to the $\overline{\text{SCS}}$ pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{\text{SCS}}$ pin input changes state from “L” to “H”, the CE bit in the SSSR register is set to 1.
Interrupt Request	5 interrupt requests (transmit-end, transmit-data-empty, receive-data-full, overrun error and conflict error).(1)
Select Function	• Data transfer direction Selects MSB-first or LSB-first • SSCK clock polarity Selects “L” or “H” level when clock stops • SSCK clock phase Selects edge of data change and data download

NOTE:
1. The interrupt vector table is one of the clock synchronous serial I/O with chip select specification.

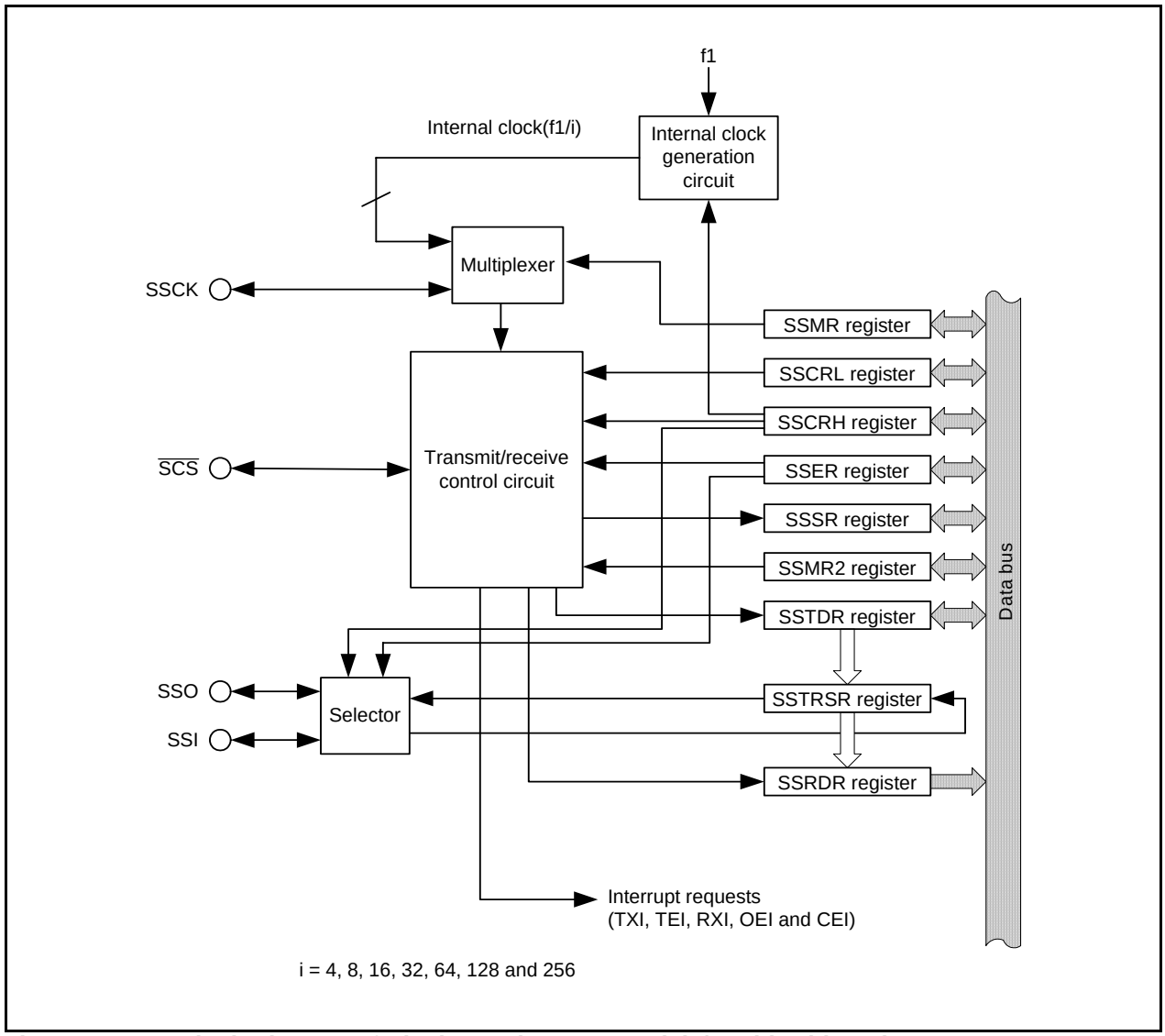
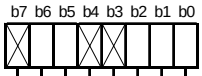


Figure 16.1 Block Diagram of Clock Synchronous Serial I/O with Chip Select

SS Control Register H



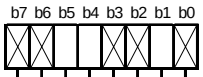
Symbol	Address	After Reset
SSCRH	00B8h	00h

Bit Symbol	Bit Name	Function	RW
CKS0	Transfer clock rate select bit(1)	b2 b1 b0 0 0 0 : f1/256 0 0 1 : f1/128 0 1 0 : f1/64 0 1 1 : f1/32 1 0 0 : f1/16 1 0 1 : f1/8 1 1 0 : f1/4 1 1 1 : Do not set	RW
CKS1			RW
CKS2			RW
— (b4-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
MSS	Master/slave device select bit(2)	0 : Operates as slave device 1 : Operates as master device	RW
RSSTP	Receive single stop bit(3)	0 : Maintains receive operation after receiving 1-byte data 1 : Completes receive operation after receiving 1-byte data	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The set clock is used when the internal clock is selected.
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operates as master device). The MSS bit is set to 0 (operates as slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operates as slave device).

Figure 16.2 SSCRH Register

SS Control Register L



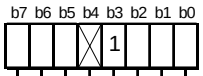
Symbol	Address	After Reset
SSCRL	00B9h	01111101b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
SRES	Clock synchronous serial I/O with chip select control part reset bit	When this bit is set to 1, the clock synchronous serial I/O with chip select control part and SSTRSR register are reset. The values of the registers(1) in the clock synchronous serial I/O with chip select register are maintained.	RW
— (b3-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
SOLP	SOL write protect bit(2)	The output level can be changed by the SOL bit when this bit is set to 0. The SOLP bit remains unchanged even if 1 is written to it. When read, its content is 1.	RW
SOL	Serial data output value setting bit	When read, 0 : The last bit of the serial data output is set to “L” 1 : The last bit of the serial data output is set to “H” When write,(2,3) 0 : The data outputs “L” after the serial data output 1 : The data outputs “H” after the serial data output	RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR and SSRDR registers.
2. The data output after the serial data is output can be changed when writing to the SOL bit before or after transfer. When writing to the SOL bit, set the SOLP bit to 0 and then write to bits SOLP and SOL by the MOV instruction.
3. Do not write to the SOL bit during the data transfer.

Figure 16.3 SSCRL Register

SS Mode Register



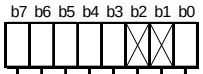
Symbol	Address	After Reset
SSMR	00BAh	00011000b

Bit Symbol	Bit Name	Function	RW
BC0	Bit counter 2 to 0	b2 b1 b0 0 0 0 : 8-bit left 0 0 1 : 1-bit left 0 1 0 : 2-bit left 0 1 1 : 3-bit left 1 0 0 : 4-bit left 1 0 1 : 5-bit left 1 1 0 : 6-bit left 1 1 1 : 7-bit left	RO
BC1			RO
BC2			RO
— (b3)	Reserved bit	Set to 1. When read, its content is 1.	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
CPHS	SSCK clock phase select bit(1)	0 : Change data at odd edge (downloads data at even edge) 1 : Change data at even edge (downloads data at odd edge)	RW
CPOS	SSCK clock polarity select bit(1)	0 : “H” when clock stops 1 : “L” when clock stops	RW
MLS	MSB first/LSB first select bit	0 : Transfers data at MSB first 1 : Transfers data at LSB first	RW

NOTE:
1. Refer to **16.2.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the setting of the CPHS and CPOS bits.

Figure 16.4 SSMR Register

SS Enable Register

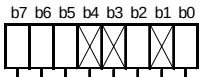


Symbol	Address	After Reset
SSER	00BBh	00h

Bit Symbol	Bit Name	Function	RW
CEIE	Conflict error interrupt enable bit	0 : Disables conflict error interrupt request 1 : Enables conflict error interrupt request	RW
— (b2-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RE	Receive enable bit	0 : Disables receive 1 : Enables receive	RW
TE	Transmit enable bit	0 : Disables transmit 1 : Enables transmit	RW
RIE	Receive interrupt enable bit	0 : Disables receive data full and overrun error interrupt request 1 : Enables receive data full and overrun error interrupt request	RW
TEIE	Transmit end interrupt enable bit	0 : Disables transmit end interrupt request 1 : Enables transmit end interrupt request	RW
TIE	Transmit interrupt enable bit	0 : Disables transmit data empty interrupt request 1 : Enables transmit data empty interrupt request	RW

Figure 16.5 SSER Register

SS Status Register(7)



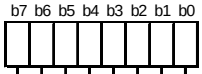
Symbol	Address	After Reset
SSSR	00BCh	00h

Bit Symbol	Bit Name	Function	RW
CE	Conflict error flag(1)	0 : No conflict error occurs 1 : Conflict error occurs(2)	RW
— (b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
ORER	Overrun error flag(1)	0 : No overrun error occurs 1 : Overrun error occurs(3)	RW
— (b4-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RDRF	Receive data register full (1,4)	0 : No data in SSRDR register 1 : Data in SSRDR register	RW
TEND	Transmit end(1,5)	0 : The TDRE bit is set to 0 when transmitting the end of the bit in transmit data 1 : The TDRE bit is set to 1 when transmitting the end of the bit in transmit data	RW
TDRE	Transmit data empty(1,5,6)	0 : Data is not transferred from the SSTDR to SSTRSR registers 1 : Data is transferred from the SSTDR to SSTRSR registers	RW

NOTES:
1. When reading 1 and writing 0, the CE, ORER, RDRF, TEND and TDRE bits are set to 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device), the CE bit is set to 1 if "L" is applied to the $\overline{SCS}$ pin input. Refer to **16.2.7 $\overline{SCS}$ Pin Control and Arbitration** for more information. When the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) is set to 0 (operates as slave device) and the $\overline{SCS}$ pin input changes the level from "L" to "H" during transfer, the CE bit is set to 1.
3. Indicates overrun error occurs and receive completes by error when receive. When the next serial data receive is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1. After the ORER bit is set to 1 (overrun error occurs), do not transmit or receive while the ORER bit is set to 1.
4. The RDRF bit is set to 0 when reading out the data from the SSRDR register.
5. The TEND and TDRE bits are set to "0" when writing the data to the SSTDR register.
6. The TDRE bit is set to 1 when setting the TE bit in the SSER register to 0 (disables transmit).
7. When accessing the SSSR register continuously, insert one or more NOP instructions between the instructions to access it.

Figure 16.6 SSSR Register

SS Mode Register 2



Symbol	Address	After Reset
SSMR2	00BDh	00h

Bit Symbol	Bit Name	Function	RW
SSUMS	Clock synchronous serial I/O with chip select mode select bit(1)	0 : Clock synchronous communication mode 1 : Four-wire bus communication mode	RW
CSOS	$\overline{SCS}$ pin open drain output select	0 : CMOS output 1 : N-channel open drain output	RW
SOOS	SSO pin open drain output select bit(1)	0 : CMOS output(5) 1 : N-channel open drain output	RW
SCKOS	SSCK pin open drain output select bit	0 : CMOS output 1 : N-channel open drain output	RW
CSS0	$\overline{SCS}$ pin select bit(2)	b5 b4 0 0 : Functions as port 0 1 : Function as $\overline{SCS}$ input pin 1 0 : Function as $\overline{SCS}$ output pin(3) 1 1 : Functions as $\overline{SCS}$ output pin(3)	RW
CSS1			RW
SCKS	SSCK pin select bit	0 : Functions as port 1 : Functions as serial clock pin	RW
BIDE	Bidirectional mode enable bit(1,4)	0 : Standard mode (communicates using 2 pins of data input and data output) 1 : Bidirectional mode (communicates using 1 pin of data input and data output)	RW

NOTES:
1. Refer to **16.2.2.1 Association between Data I/O Pins and SS Shift Register** for the combination of the data I/O pin.
2. The $\overline{SCS}$ pin functions as a port, regardless of the contents of the CSS0 and CSS1 bits when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. The SSI pin and SSO pin corresponding port direction bits are set to 0 (input mode) when the SOOS bit is set to 0 (CMOS output).

Figure 16.7 SSMR2 Register

SS Transmit Data Register

b7 b0

Symbol	Address	After Reset
SSTDR	00BEh	FFh

Function	RW
Store the transmit data. The stored transmit data is transferred to the SSTRSR register and the transmit is started when detecting the SSTRSR register is empty. When the next transmit data is written to the SSTDR register during the data transmit from the SSTRSR register, the data can be transmitted continuously. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB-first), the data in which MSB and LSB are reversed can be read, after writing to the SSTDR register.	RW

SS Receive Data Register

b7 b0

Symbol	Address	After Reset
SSRDR	00BFh	FFh

Function	RW
Store the receive data.(1) The receive data is transferred to the SSRDR register and the receive operation is completed when receiving 1-byte data to the SSTRSR register. At this time, the following receive is possible. The continuous receive is possible by the SSTRSR and SSRDR registers.	RO

NOTE:
1. The SSRDR register maintains the receive data before the overrun error occurs when the ORER bit in the SSSR register is set to 1 (overrun error occurs). When an overrun error occurs, the receive data may contain errors and therefore, should be discarded.

Figure 16.8 Registers SSTDR and SSRDR

Port Mode Register

b7 b6 b5 b4 b3 b2 b1 b0
— 0 0 — 0 0 0 0

Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0	—
U1PINSEL	Port TXD1/RXD1 switch bit	0 : I/O port P6_6, P6_7 1 : TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0	—
IICSEL	SSU/I²C bus switch bit	0 : SSU function selects 1 : I²C bus function selects	RW

Figure 16.9 PMR Register

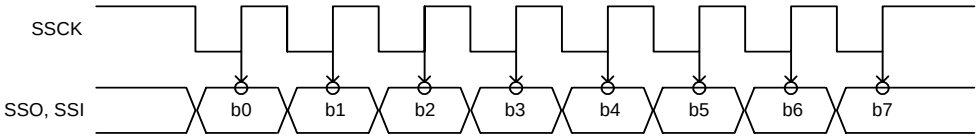
16.2.1 Transfer Clock

A transfer clock can be selected from 7 internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4) and an external clock.
When using the clock synchronous serial I/O with chip select, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.
When the MSS bit in the SSCRH register is set to 1 (operates as master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs clocks of the transfer rate selected in the CKS0 to CKS2 bits in the SSCRH register.
When the MSS bit in the SSCRH register is set to 0 (operates as slave device), an external clock can be selected and the SSCK pin functions as input.

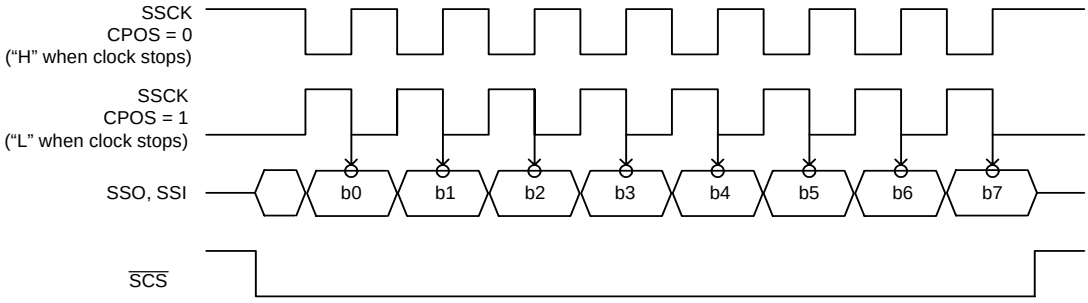
16.2.1.1 Association between Transfer Clock Polarity, Phase, and Data

Association between transfer clock polarity, phase and data changes according to a combination of the SSUMS bit in the SSMR2 register and the CPHS and CPOS bits in the SSMR register.
Figure 16.10 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.
Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB to MSB. When the MLS bit is set to 0, transfer is started from the MSB to LSB.

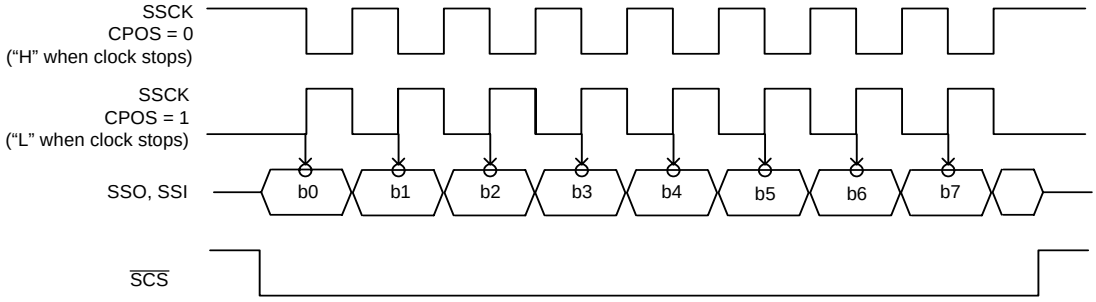
- When SSUMS bit = 0 (clock synchronous communication mode), CPHS bit = 0 (data change at odd edge) and CPOS bit = 0 (“H” when clock stops)



- When SSUMS bit = 1 (4-wire bus communication mode) and CPHS bit = 0 (data change at odd edge)



- When SSUMS bit = 1 (4-wire bus communication mode), CPHS bit = 1 (data download at odd edge)



CPHS and CPOS: bits in SSMR register, SSUMS: Bits in SSMR2 register

Figure 16.10 Association between Transfer Clock Polarity, Phase, and Transfer Data

16.2.2 SS Shift Register (SSTRSR)

The SSTRSR register is the shift register to transmit and receive the serial data.
When the transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB-first), the bit 0 in the SSTDR register is transferred to the bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB-first), the bit 7 in the SSTDR register is transferred to the bit 0 in the SSTRSR register.

16.2.2.1 Association between Data I/O Pins and SS Shift Register

Connecting association between the data I/O pin and SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. Also, connecting association changes according to the BIDE bit in the SSMR2 register.
Figure 16.11 shows an Association between Data I/O Pins and SSTRSR Register.

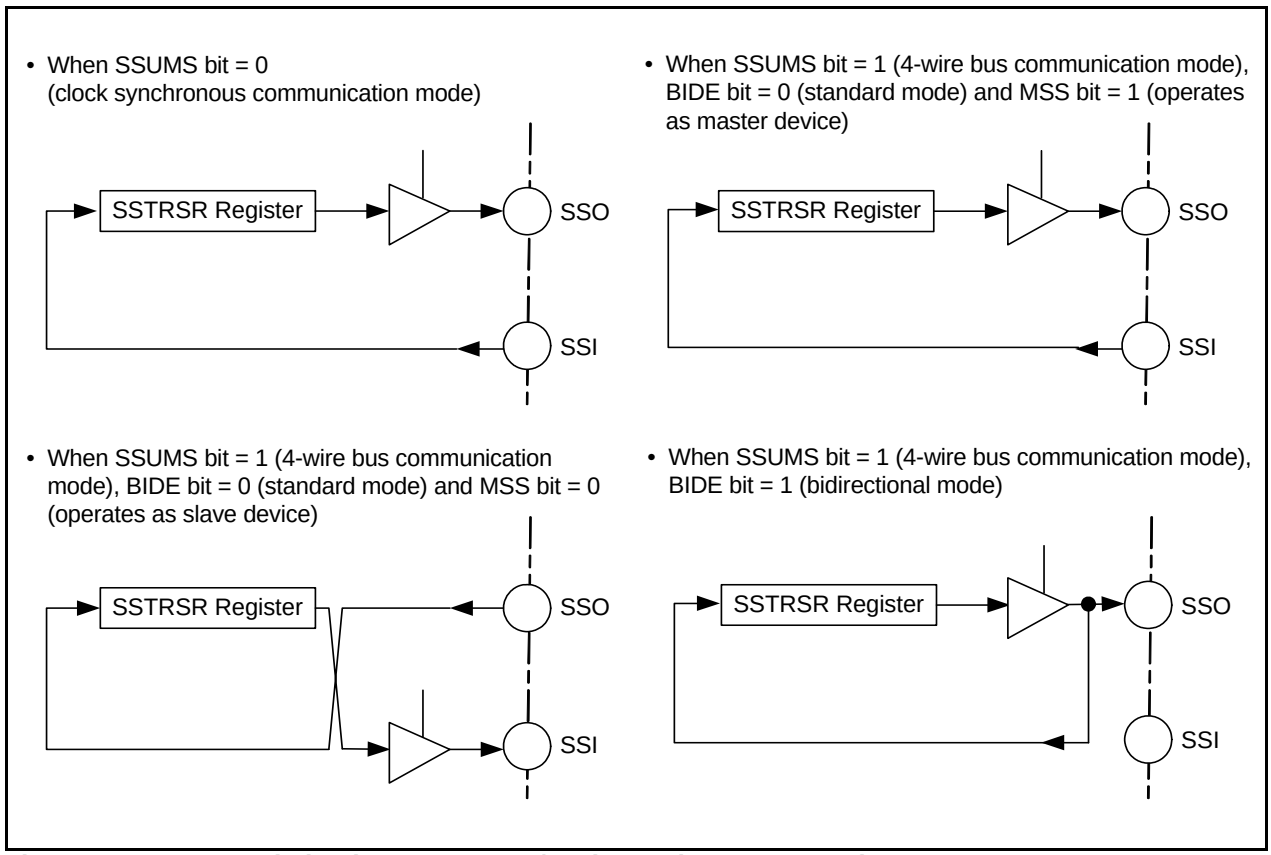


Figure 16.11 Association between Data I/O Pins and SSTRSR Register

16.2.3 Interrupt Requests

Clock synchronous serial I/O with chip select has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error and conflict error. Since these interrupt requests are assigned to the clock synchronous serial I/O with chip select interrupt vector table, determining interrupt sources by flags is required. Table 16.3 shows the Clock Synchronous Serial I/O with Chip Select Interrupt Requests.

Table 16.3 Clock Synchronous Serial I/O with Chip Select Interrupt Requests

Interrupt Request	Abbreviation	Generation Condition
Transmit Data Empty	TXI	TIE = 1, TDRE = 1
Transmit End	TEI	TEIE = 1, TEND = 1
Receive Data Full	RXI	RIE = 1, RDRF = 1
Overrun Error	OEI	RIE = 1, ORER = 1
Conflict Error	CEI	CEIE = 1, CE = 1

CEIE, RIE, TEIE and TIE: Bits in SSER register
ORER, RDRF, TEND and TDRE: Bits in SSSR register

Generation conditions of Table 16.3 are met, a clock synchronous serial I/O with chip select interrupt request is generated. Set the each interrupt source to 0 by a clock synchronous serial I/O with chip select interrupt routine.

However, the TDRE and TEND bits are automatically set to 0 by writing the transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. When writing the transmit data to the SSTDR register, at the same time the TDRE bit is set to 1 (data is transmitted from the SSTDR to SSTRSR registers) again and when setting the TDRE bit to 0 (data is not transmitted from the SSTDR to SSTRSR registers), additional 1-byte data may be transmitted.

16.2.4 Communication Modes and Pin Functions

Clock synchronous serial I/O with chip select switches functions of the I/O pin in each communication mode according to the setting of the MSS bit in the SSCRH register and the RE and TE bits in the SSER register. Table 16.4 shows the Association between Communication Modes and I/O Pins.

Table 16.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock Synchronous Communication Mode	0	Disabled	0	0	1	Input	–(1)	Input
				1	0	–(1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	–(1)	Output
				1	0	–(1)	Output	Output
					1	Input	Output	Output
4-Wire Bus Communication Mode	1	0	0	0	1	–(1)	Input	Input
				1	0	Output	–(1)	Input
					1	Output	Input	Input
			1	0	1	Input	–(1)	Output
				1	0	–(1)	Output	Output
					1	Input	Output	Output
4-Wire Bus (Bidirectional) Communication Mode(2)	1	1	0	0	1	–(1)	Input	Input
				1	0	–(1)	Output	Input
			1	0	1	–(1)	Input	Output
				1	0	–(1)	Output	Output

NOTES:
1. This pin can be used as programmable I/O port.
2. Do not set both the TE and RE bits to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS and BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE and RE: Bits in SSER register

16.2.5 Clock Synchronous Communication Mode

16.2.5.1 Initialization in Clock Synchronous Communication Mode

Figure 16.12 shows an Initialization in Clock Synchronous Communication Mode. Set the TE bit in the SSER register to 0 (disables transmit) and the RE bit to 0 (disables receive) before data transmit / receive as an initialization.

When communication mode and format are changed, set the TE bit to 0 and the RE bit to 0 before changing. Setting the RE bit to 0 does not change the contents of the RDRF and ORER flags, and the contents of the SSRDR register.

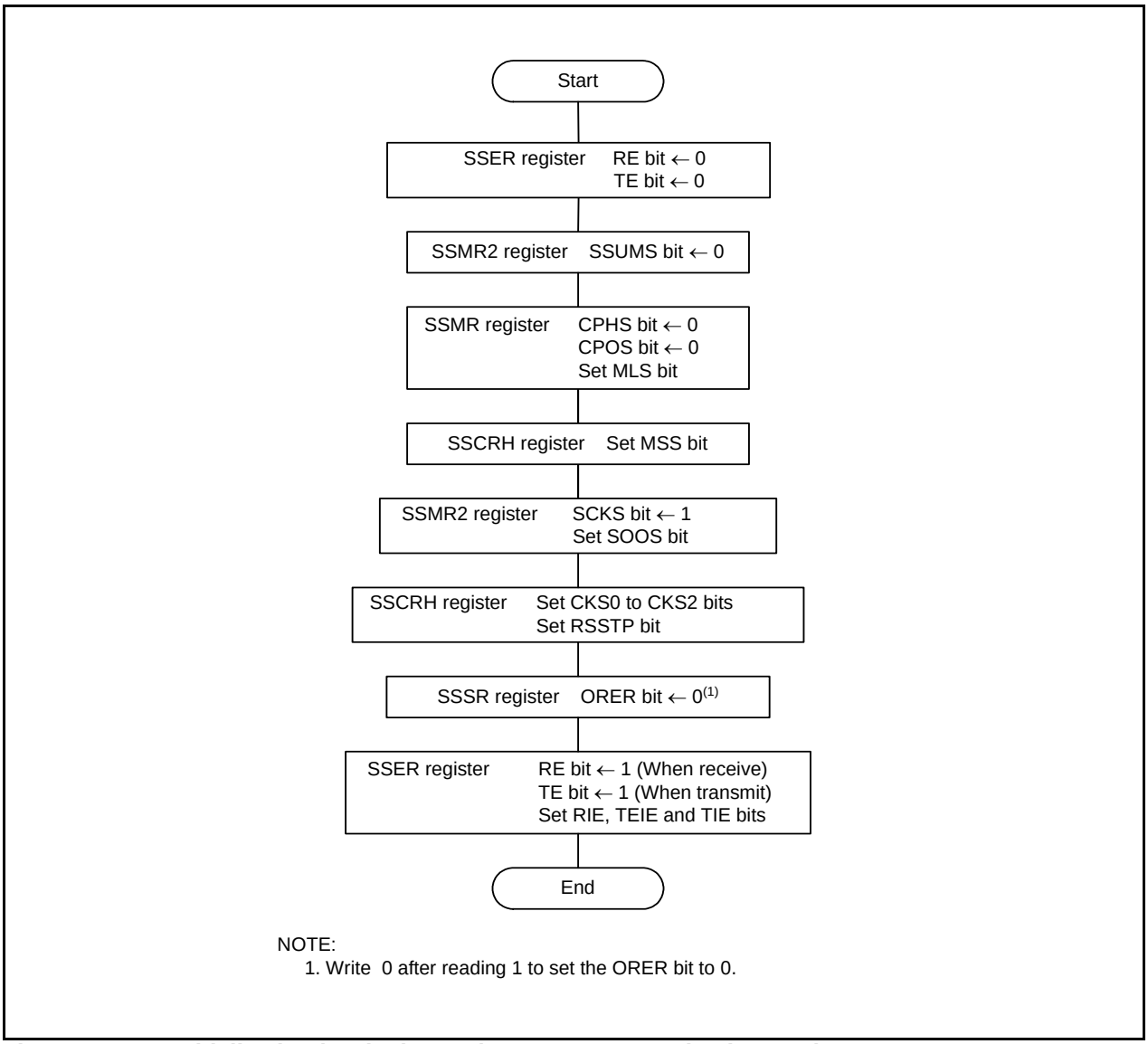


Figure 16.12 Initialization in Clock Synchronous Communication Mode

16.2.5.2 Data Transmission

Figure 16.13 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Transmission (Clock Synchronous Communication Mode). During the data transmit, the clock synchronous serial I/O with chip select operates as described below.

When the clock synchronous serial I/O with chip select is set as a master device, it outputs a synchronous clock and data.

When the clock synchronous serial I/O with chip select is set as a slave device, it outputs data synchronized with the input clock. When setting the TE bit to 1 (enables transmit) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data is not transferred from the SSTDR to SSTRSR registers) and the data is transferred from the SSTDR to SSTRSR registers.

After the TDRE bit is set to 1 (data is transferred from the SSTDR to SSTRSR registers), a transmit is started. When the TIE bit in the SSER register is set to 1, the TXI interrupt request is generated. When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from the SSTDR to SSTRSR registers and a transmit of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (the TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. The TEI interrupt request is generated when the TEIE bit in the SSER register is set to 1 (enables transmit-end interrupt request). The SSCK pin is retained “H” after transmit-end.

Transmit can not be performed while the ORER bit in the SSSR register is set to 1 (overrun error occurs). Confirm that the ORER bit is set to 0 before transmit.

Figure 16.14 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

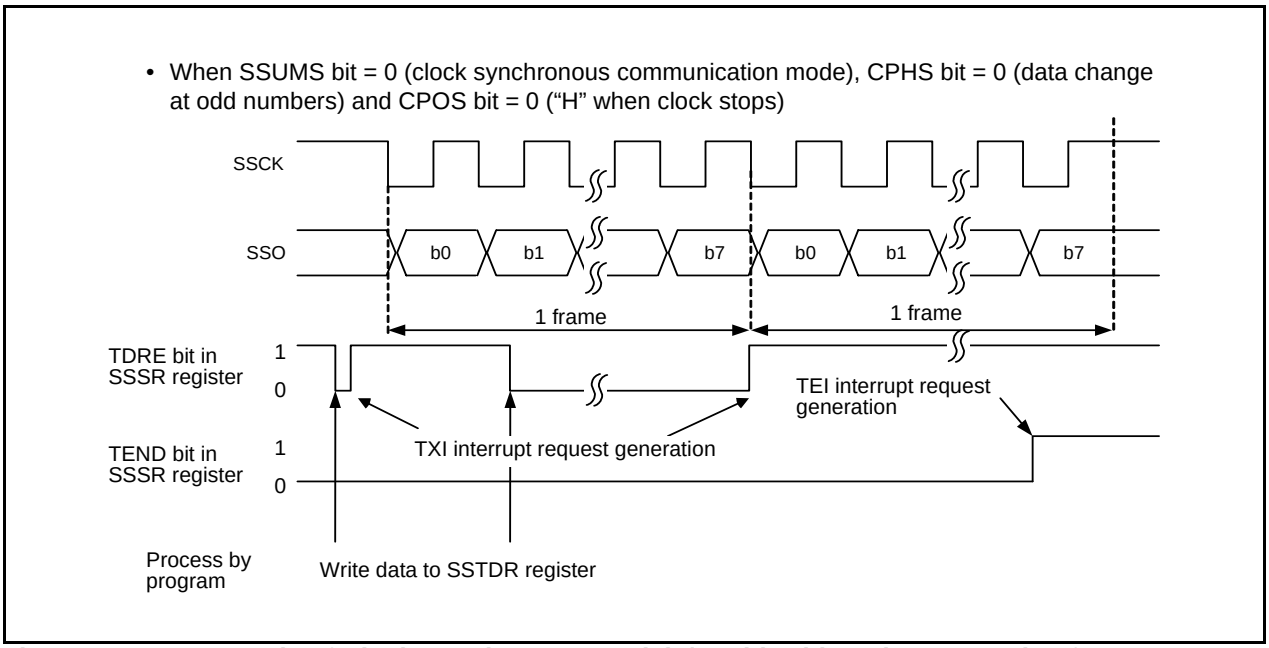


Figure 16.13 Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Transmission (Clock Synchronous Communication Mode)

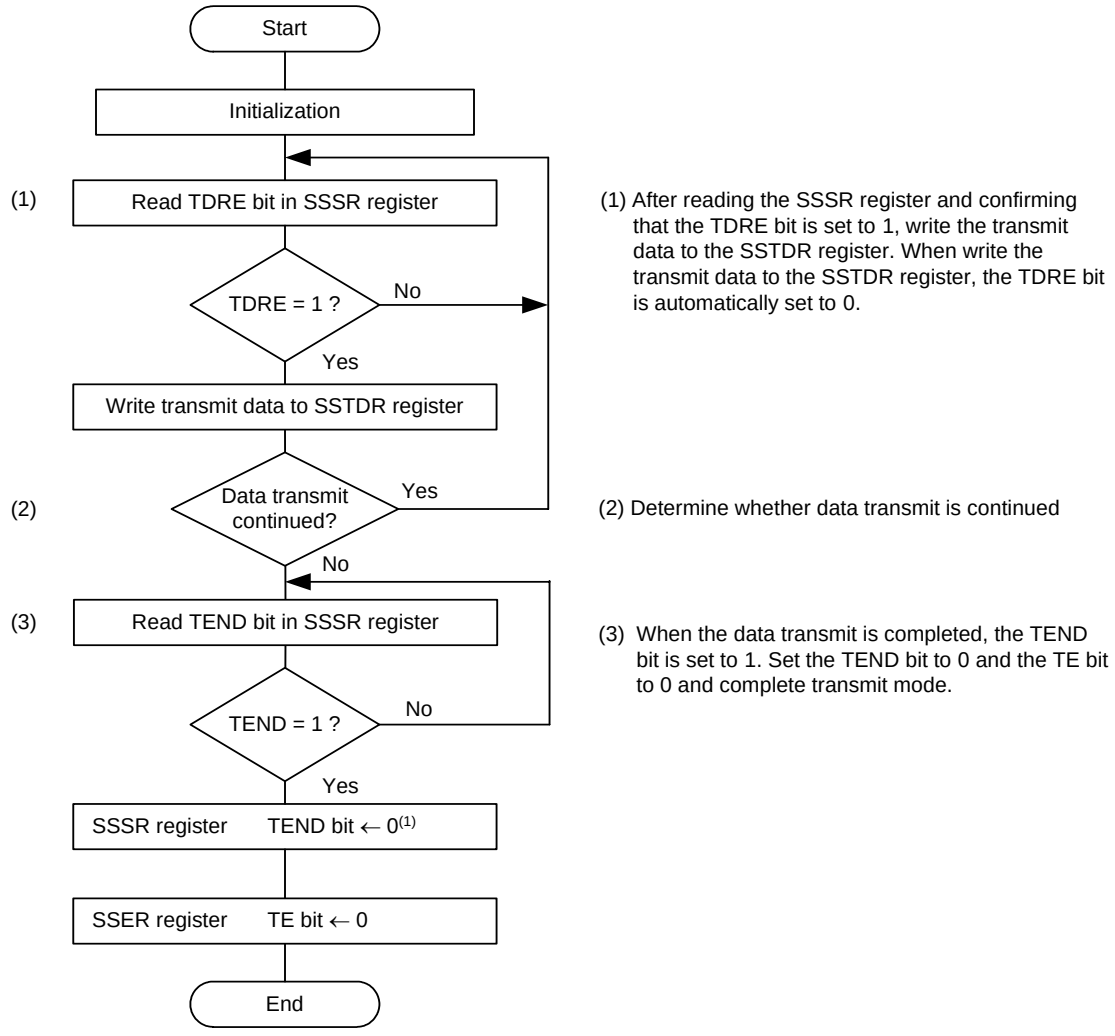


Figure 16.14 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

16.2.5.3 Data Reception

Figure 16.15 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Reception (Clock Synchronous Communication Mode).

During the data receive, the clock synchronous serial I/O with chip select operates as described below. When the clock synchronous serial I/O with chip select is set as a master device, it outputs a synchronous clock and inputs data.

When the clock synchronous serial I/O with chip select is set as a salve device, it outputs data synchronized with the input clock. When the clock synchronous serial I/O with chip select is set as a master device, it outputs a receive clock and starts receiving by performing dummy read on the SSRDR register.

After the 8-bit data is received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (enables RXI and OEI interrupt request), the RXI interrupt request is generated. If the SSDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1-byte data, the receive operation is completed). The clock synchronous serial I/O with chip select outputs a clock for receiving 8-bit data and stops. After that, set the RE bit in the SSER register to 0 (disables receive) and the RSSTP bit to 0 (receive operation is continued after receiving the 1-byte data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (enables receive), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error occurs: OEI) and the operation is stopped. When the ORER bit is set to 1, receive can not be performed. Confirm that the ORER bit is set to 0 before restarting receive.

Figure 16.16 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

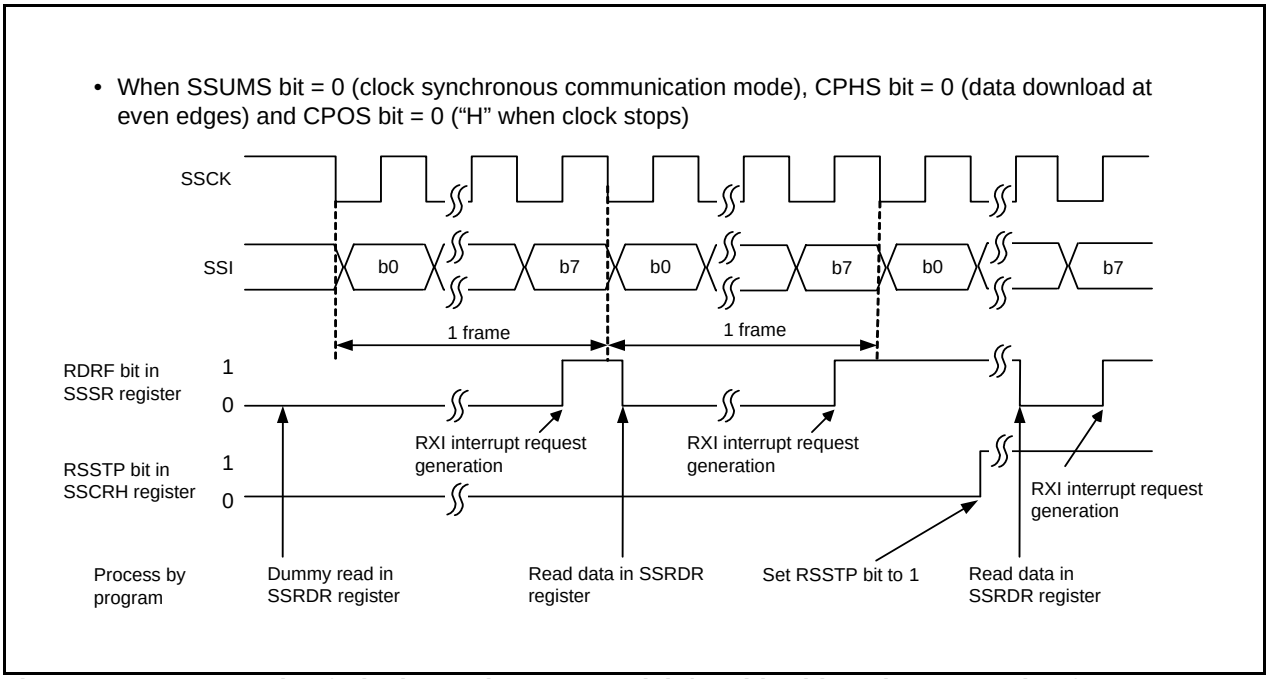


Figure 16.15 Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Reception (Clock Synchronous Communication Mode)

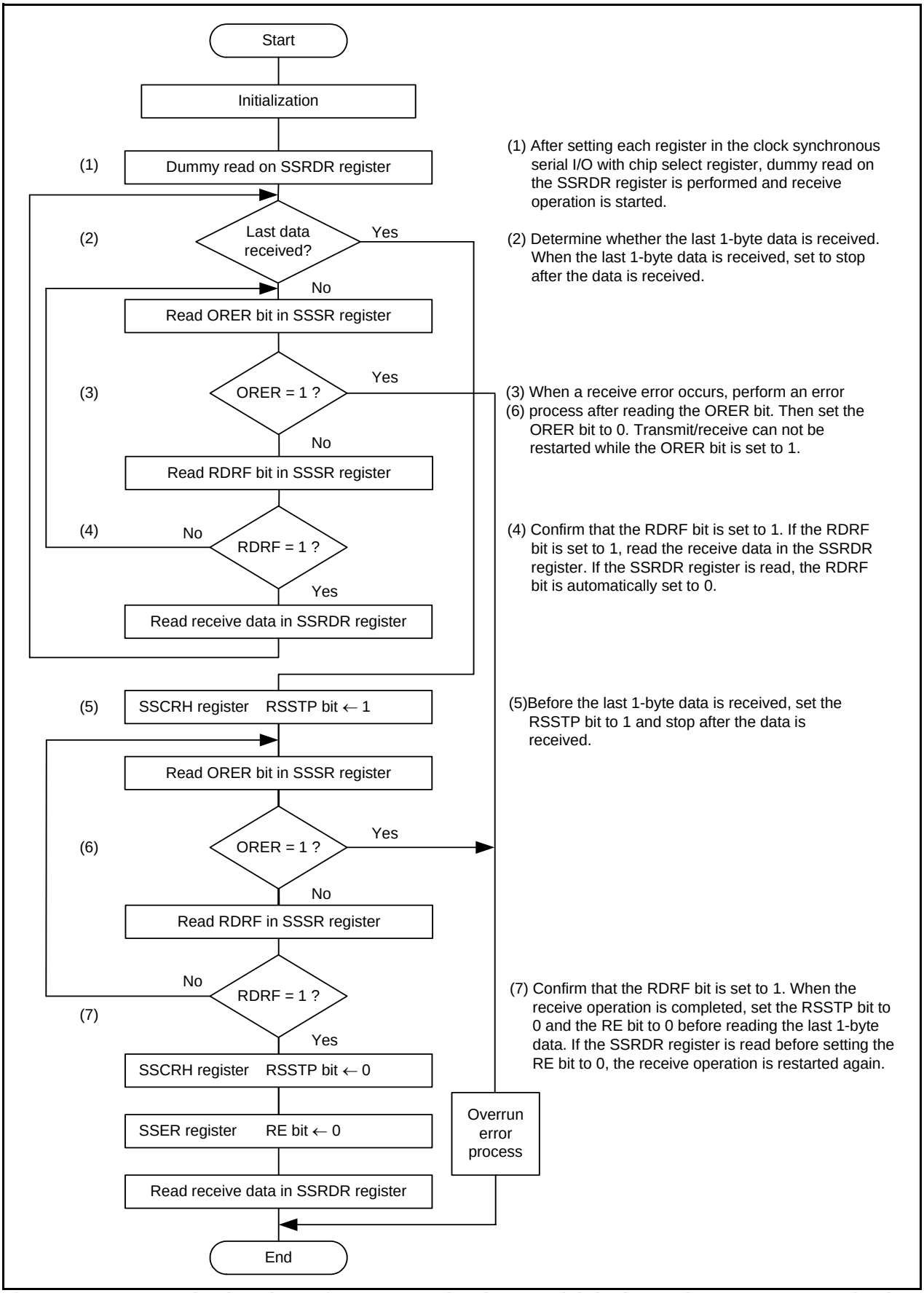


Figure 16.16 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

16.2.5.4 Data Transmission/Reception

Data transmit/receive is a combined operation of data transmit and receive which are described before. Transmit/receive is started by writing data in the SSTDR register.
When the 8th clock rises or the ORER bit is set to 1 (overrun error occurs) while the TDRE bit is set to 1 (data is transferred from the SSTDR to SSTRSR registers), the transmit/receive operation is stopped.
When switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (Te = RE =1), set the TE bit to 0 and RE bit to 0 before switching. After confirming that the TEND bit is set to 0 (the TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RERF bit is set to 0 (no data in the SSRDR register) and the ORER bit is set to 0 (no overrun error), set the TE and RE bits to 1.
Figure 16.17 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).

When exiting transmit/receive mode after this mode is used (TE = RE = 1), a clock may be output if transmit/receive mode is exited after reading the SSRDR register. To avoid any clock outputs, perform either of the following:

- First set the RE bit to 0, and then set the TE bit to 0.
- Set bits TE and RE at the same time.

When subsequently switching to receive mode (TE = 0 and RE = 1), first set the SRES bit to 1, and set this bit to 0 to reset the clock synchronous serial interface control unit and the SSTRSR register. Then, set the RE bit to 1.

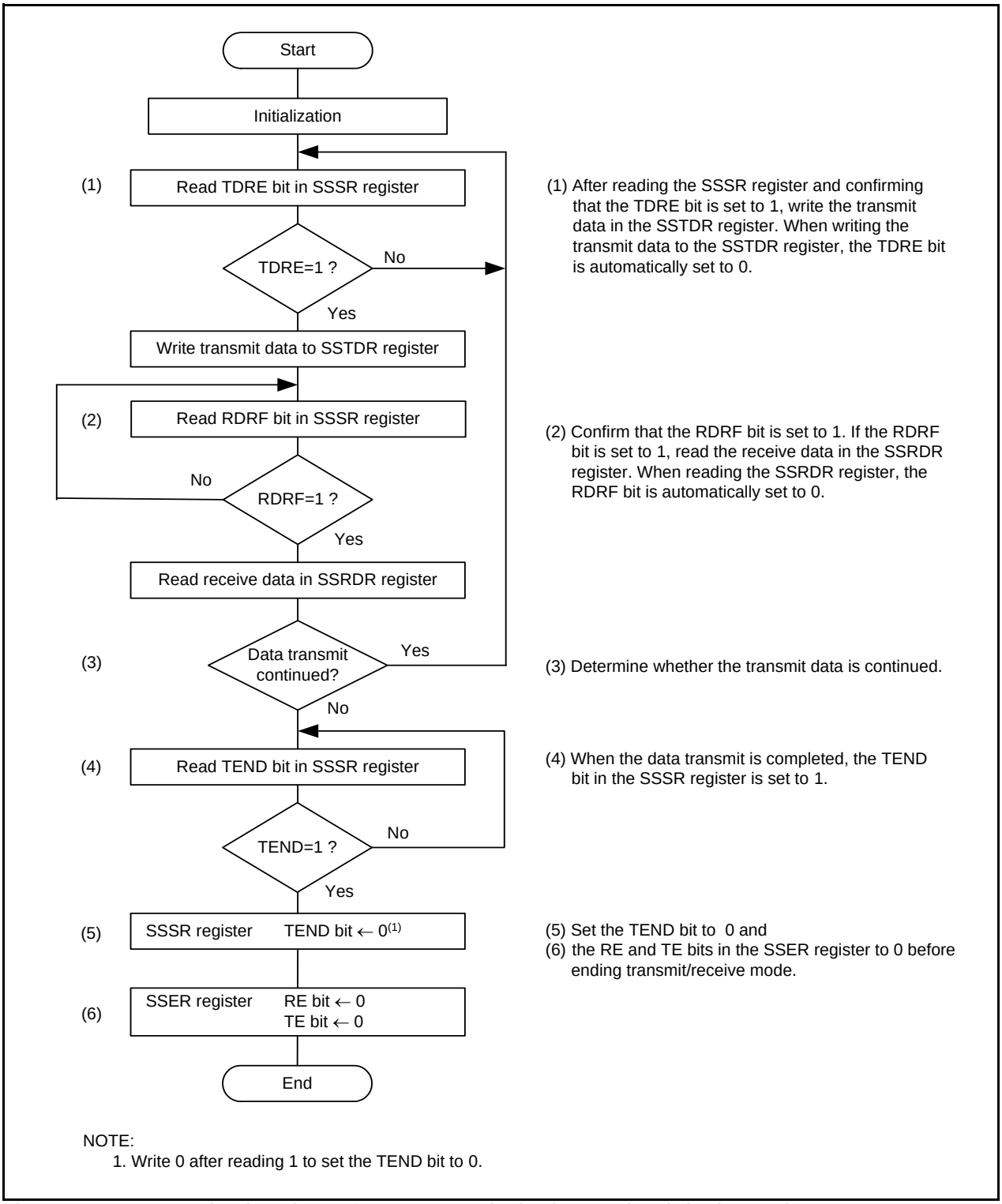


Figure 16.17 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

16.2.6 Operation in 4-Wire Bus Communication Mode

4-wire bus communication mode is a mode which communicates with the 4-wire bus; a clock line, data input line, data output line and chip select line. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line are changed according to the setting of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **16.2.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, association between the clock polarity, phase and data can be set by the CPOS and CPHS bits in the SSMR register. For details, refer to **16.2.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When the clock synchronous serial I/O with chip select is set as a master device, the chip select line controls output. When the clock synchronous serial I/O with chip select is set as a slave device, the chip select line controls input. When the clock synchronous serial I/O with chip select is set as master device, the chip select line controls output of the $\overline{SCS}$ pin or controls output of a general port by setting the CSS1 bit in the SSMR2 register. When the clock synchronous serial I/O with chip select is set as a slave device, the chip select line set the $\overline{SCS}$ pin as an input pin by setting the CSS1 and CSS0 bits in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed using the MSB-first.

16.2.6.1 Initialization in 4-Wire Bus Communication Mode

Figure 16.18 shows an Initialization in 4-Wire Bus Communication Mode. Before the data transit/receive, set the TE bit in the SSER register to 0 (disables transmit) and the RE bit in the SSER register to 0 (disables receive) and initialize the clock synchronous serial I/O with chip select.

When communication mode and format are changed, set the TE bit to 0 and the RE bit to 0 before changing.

Setting the RE bit to 0 does not change the contents of the RDRF and ORER flags, and the contents of the SSRDR register.

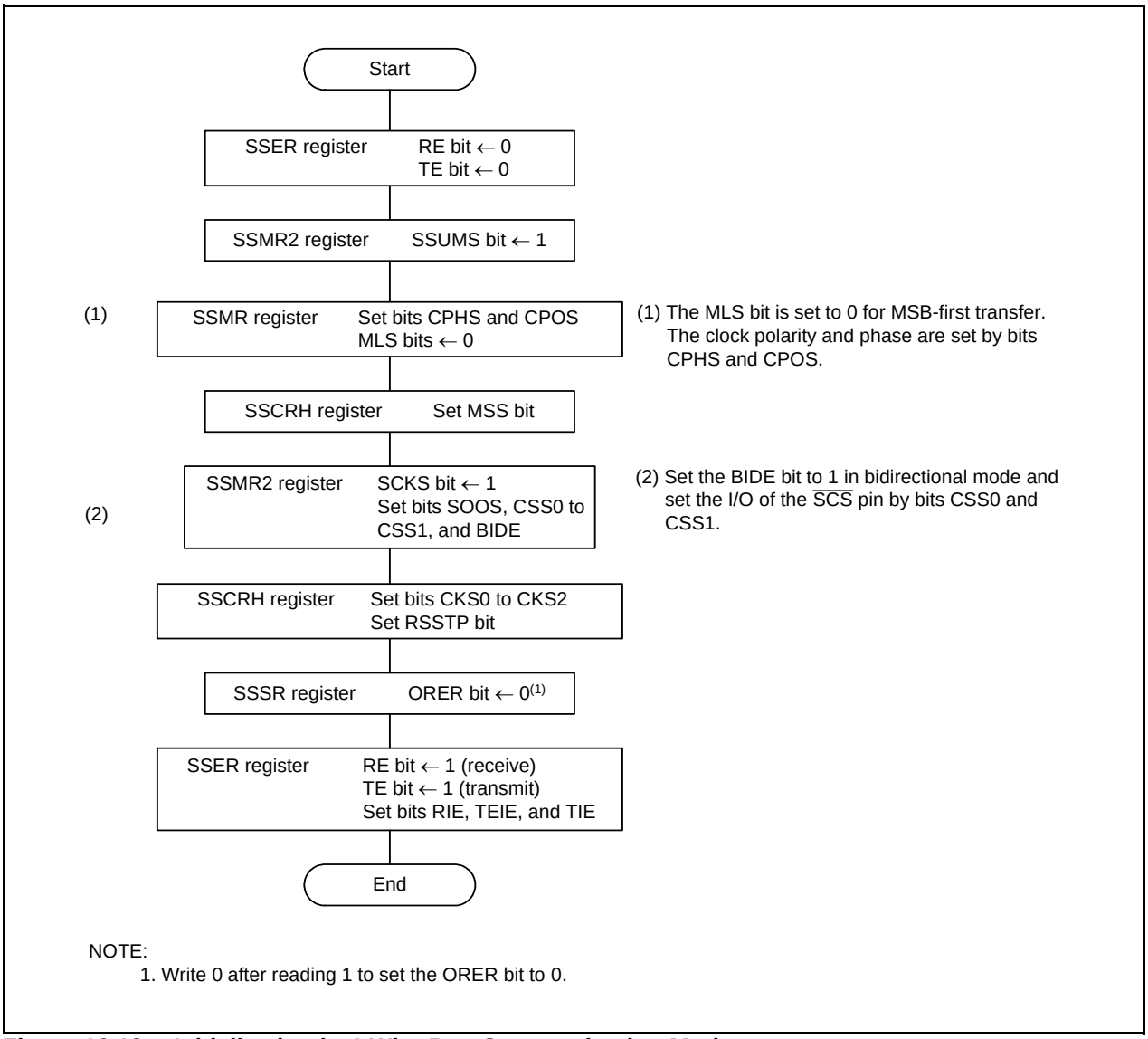


Figure 16.18 Initialization in 4-Wire Bus Communication Mode

16.2.6.2 Data Transmission

Figure 16.19 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Transmission (4-Wire Bus Communication Mode). During the data transmit, the clock synchronous serial I/O with chip select operates as described below.

When the clock synchronous serial I/O with chip select is set as a master device, it outputs a synchronous clock and data. When the UUSA is set as a slave device, it outputs data in synchronized with the input clock while "L" applies to the $\overline{SCS}$ pin.

When writing the transmit data to the SSTDR register after setting the TE bit to 1 (enables transmit), the TDRE bit is automatically set to 0 (data is not transferred from the SSTDR to SSTRSR registers) and the data is transferred from the SSTDR to SSTRSR registers. After the TDRE bit is set to 1 (data is transferred from the SSTDR to SSTRSR registers), a transmit is started. When the TIE bit in the SSER register is set to 1, the TXI interrupt request is generated.

When the 1-frame data is transferred while the TDRE bit is set to 0, the data is transferred from the SSTDR to SSTRSR registers and the next frame transmit is started. If the 8th bit is transmitted while the TDRE is set to 1, the TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. If the TEIE bit in the SSER register is set to 1 (enables transmit-end interrupt request), the TEI interrupt request is generated. The SSCK pin is retained "H" after transmit-end and the $\overline{SCS}$ pin is held "H". When the $\overline{SCS}$ pin is transmitted When transmitting continuously while the $\overline{SCS}$ pin is held "L", write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmit can not be performed while the ORER bit in the SSSR register is set to 1 (overrun error occurs). Confirm that the ORER bit is set to 0 before transmit.

The difference from the clock synchronous communication mode is that the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as a master device and the SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in "H" input state when operating as a slave device.

A sample flowchart is the same as the clock synchronous communication mode (refer to **Figure 16.14 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

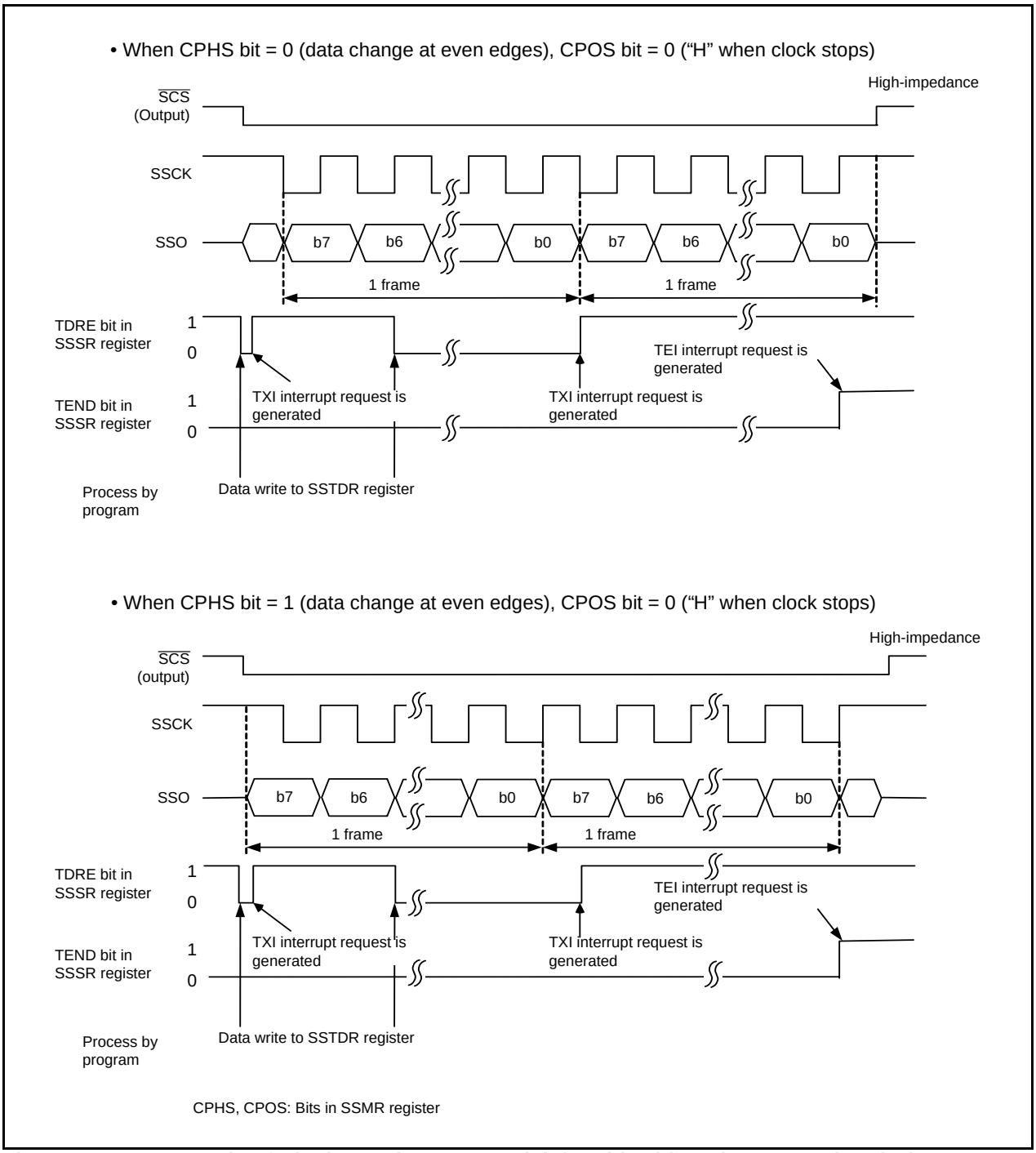


Figure 16.19 Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Transmission (4-Wire Bus Communication Mode)

16.2.6.3 Data Reception

Figure 16.20 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Reception (4-Wire Bus Communication Mode). During the data receive, the clock synchronous serial I/O with chip select operates as described below.

When the clock synchronous serial I/O with chip select is set as a master device, it outputs a synchronous clock and inputs data. When the clock synchronous serial I/O with chip select is set as a salve device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin is held “L” input. When the clock synchronous serial I/O with chip select is set as a master device, it outputs a receive clock and starts receiving by performing dummy read on the SSRDR register.

After the 8-bit data is received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (enables RXI and OEI interrupt request), the RXI interrupt request is generated. If the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1-byte data, the receive operation is completed). The clock synchronous serial I/O with chip select outputs a clock for receiving 8-bit data and stops. After that, set the RE bit in the SSER register to 0 (disables receive) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (enables receive), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error occurs: OEI) and the operation is stopped. When the ORER bit is set to 1, receive can not be performed. Confirm that the ORER bit is set to 0 before restarting receive.

When the RDRF and ORER bits are set to 1, it varies depending on setting the CPHS bit in the SSMR register. Figure 16.20 shows when the RDRF and ORER bits are set to 1.

When the CPHS bit is set to 1 (data download at the odd edges), the RDRF and ORER bits are set to 1 at one point of a frame.

A sample flowchart is the same as the clock synchronous communication mode (refer to **Figure 16.16 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

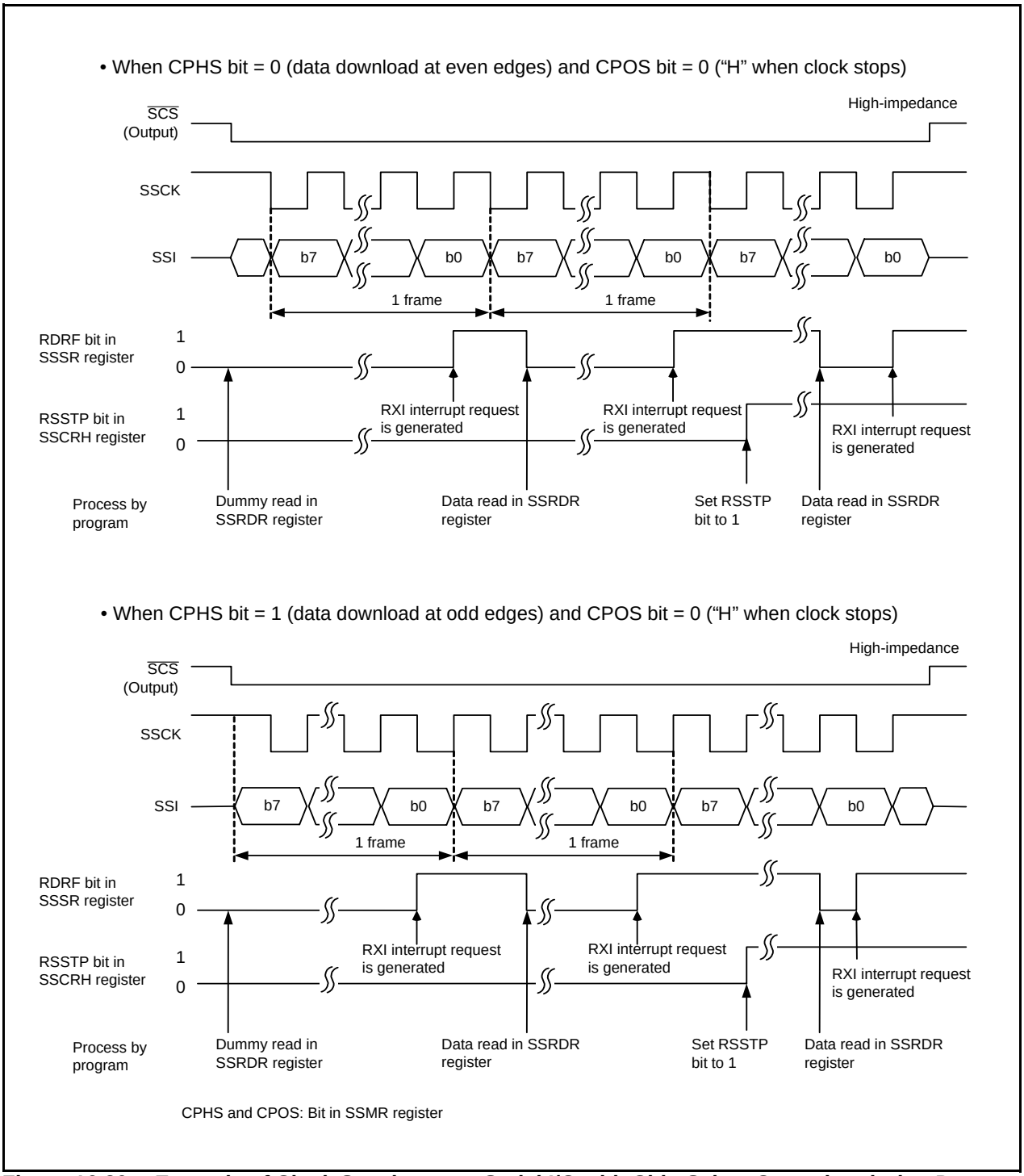


Figure 16.20 Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Reception (4-Wire Bus Communication Mode)

16.2.7 $\overline{\text{SCS}}$ Pin Control and Arbitration

When setting the SSUMS bit in the SSMR2 register to 1 (4-wire bus communication mode), and the CSS1 bit in the SSMR2 register to 1 (functions as $\overline{\text{SCS}}$ output pin), Set the MSS bit in the SSCRH register to 1 (operates as a master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If the clock synchronous serial I/O with chip select detects that the synchronized internal $\overline{\text{SCS}}$ signal is held "L" in this period, the CE bit in the SSSR register to 1 (a conflict error occurs) and the MSS bit is automatically set to 0 (operates as a slave device).
Figure 16.21 shows an Arbitration Check Timing.

A future transmit operation is not performed while the CE bit is set to 1. Set the CE bit to 0 (a conflict error does not occur) before a transmit is started.

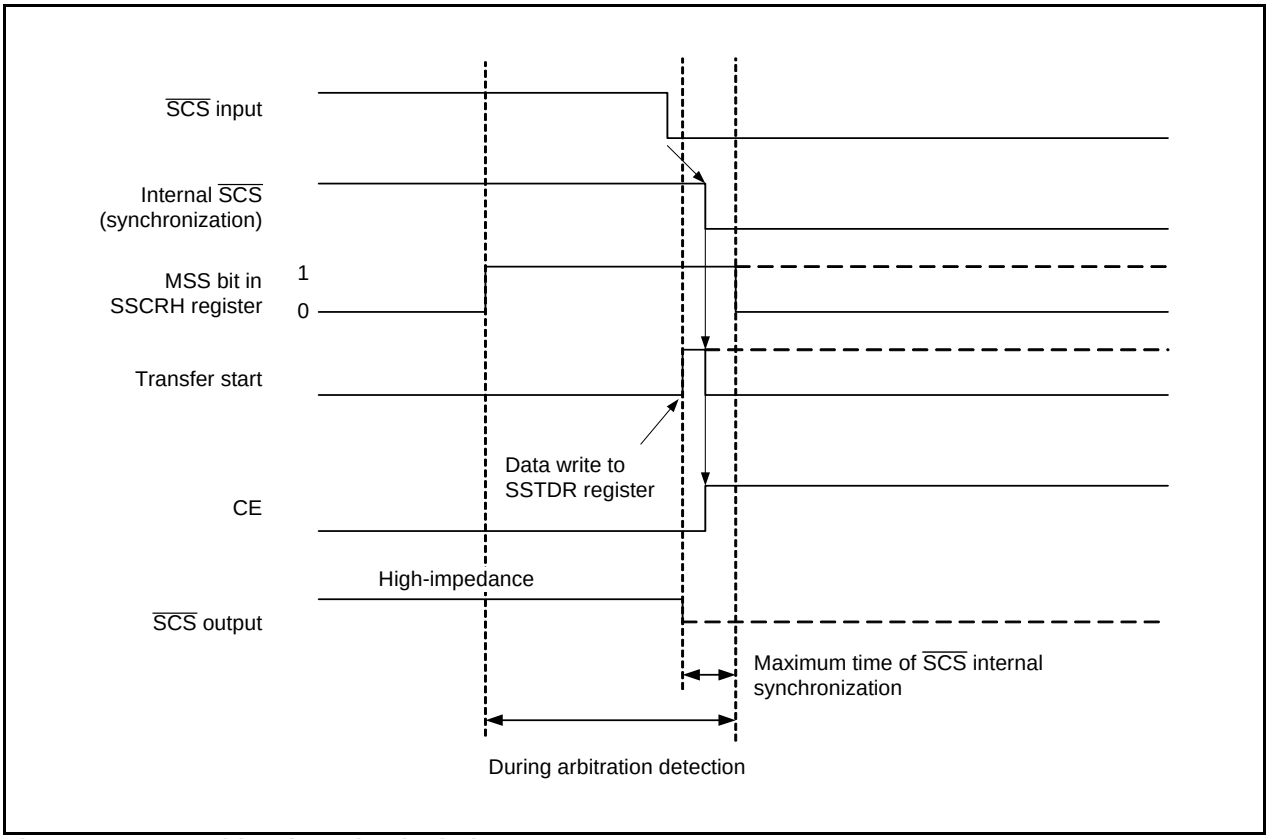


Figure 16.21 Arbitration Check Timing

16.2.8 Notes on Clock Synchronous Serial I/O with Chip Select

Set the IICSEL bit in the PMR register to 0 (select clock synchronous serial I/O with chip select function) to use the clock synchronous serial I/O with chip select.

16.3 I²C Bus Interface

The I²C bus interface is the circuit which is used for a serial communication based on the data transfer format of the Philips I²C bus.
Table 16.5 lists a I²C Bus Interface Specifications, Figure 16.22 shows a Block Diagram of I²C bus Interface and Figure 16.23 shows the External Circuit Connection Example of Pins SCL and SDA. Figures 16.24 to 16.31 show the registers associated with the I²C bus interface.

* I²C bus is a trademark of Koninklijke Philips Electronics N. V.

Table 16.5 I²C Bus Interface Specifications

Item	Specification
Communication Formats	• I²C bus format - Selectable for master / slave device - Continuous transmit / receive (since the shift register, transmit data register and receive data register are independent) - Start / stop conditions are automatically generated in master mode - Automatic loading of acknowledge bit when transmit - Bit synchronization / wait function (in master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, stand by to set the SCL signal to “L”. - Direct drive of the SCL and SDA pins (N-channel open drain output) is enabled • Clock synchronous serial format - Continuous transmit / receive (since the shift register, transmit data register and receive data register are independent)
I/O Pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer Clocks	• When the MST bit in the ICCR1 register is set to 0 The external clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1 The internal clock selected by the CKS0 to CKS3 bits in the ICCR1 register (output from the SCL pin)
Receive Error Detection	• Detects overrun error (clock synchronous serial format) An overrun error occurs during receive. When the last bit of the following data is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt Sources	• I²C bus format ..... 6 types(1) Transmit data empty (including when slave address matches), transmit ends, receive data full (including when slave address matches), arbitration lost, NACK detection and stop condition detection. • Clock synchronous serial format ..... 4 types(1) Transmit data empty, transmit ends, receive data full and overrun error
Select Functions	• I²C bus format - Selectable for the output level of the acknowledge signal when receive • Clock synchronous serial format - Selectable for the MSB-first or LSB-first to the data transfer direction

NOTE:
1. The interrupt sources can use the only I²C bus interface interrupt vector table.

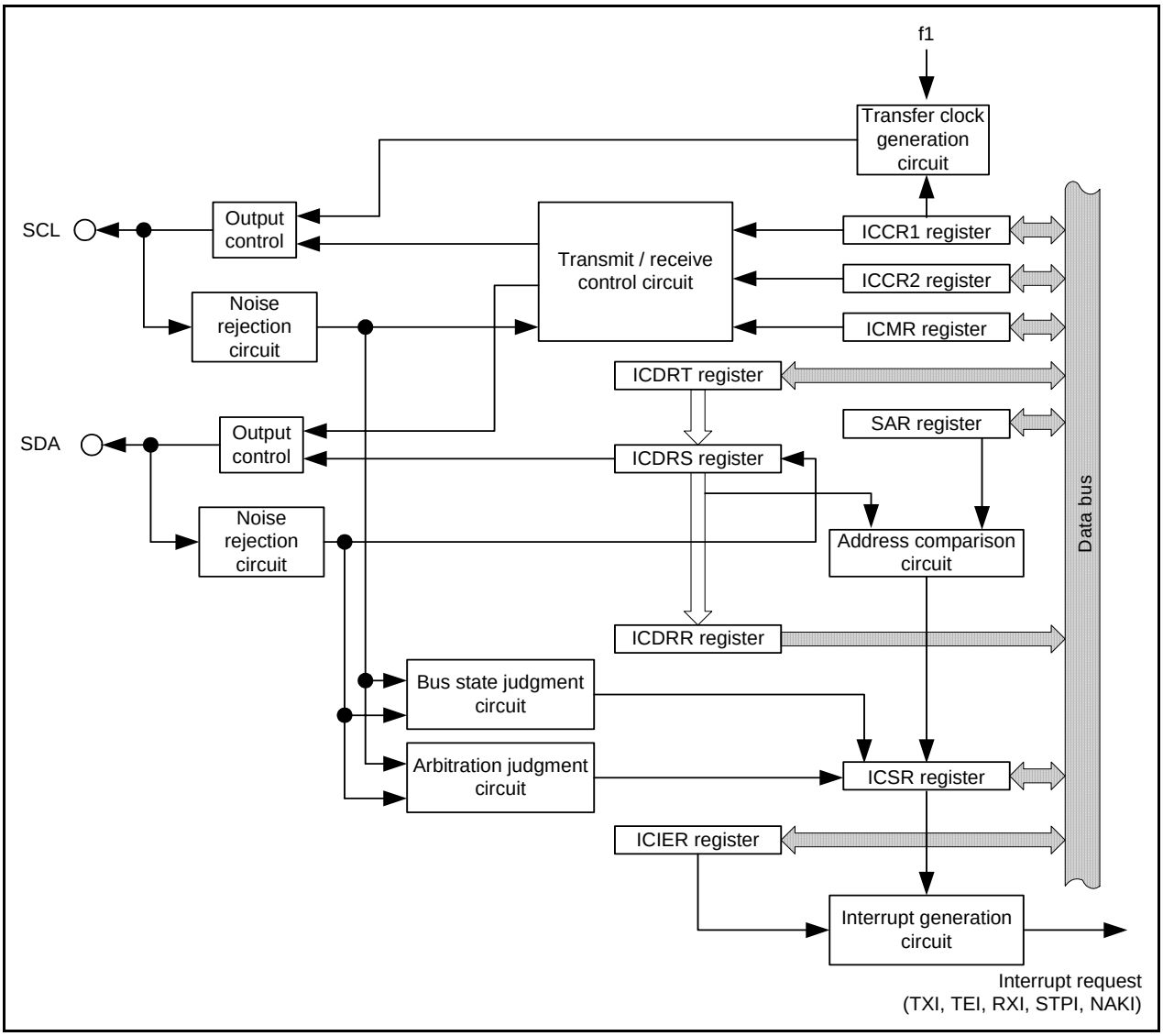


Figure 16.22 Block Diagram of I²C Bus Interface

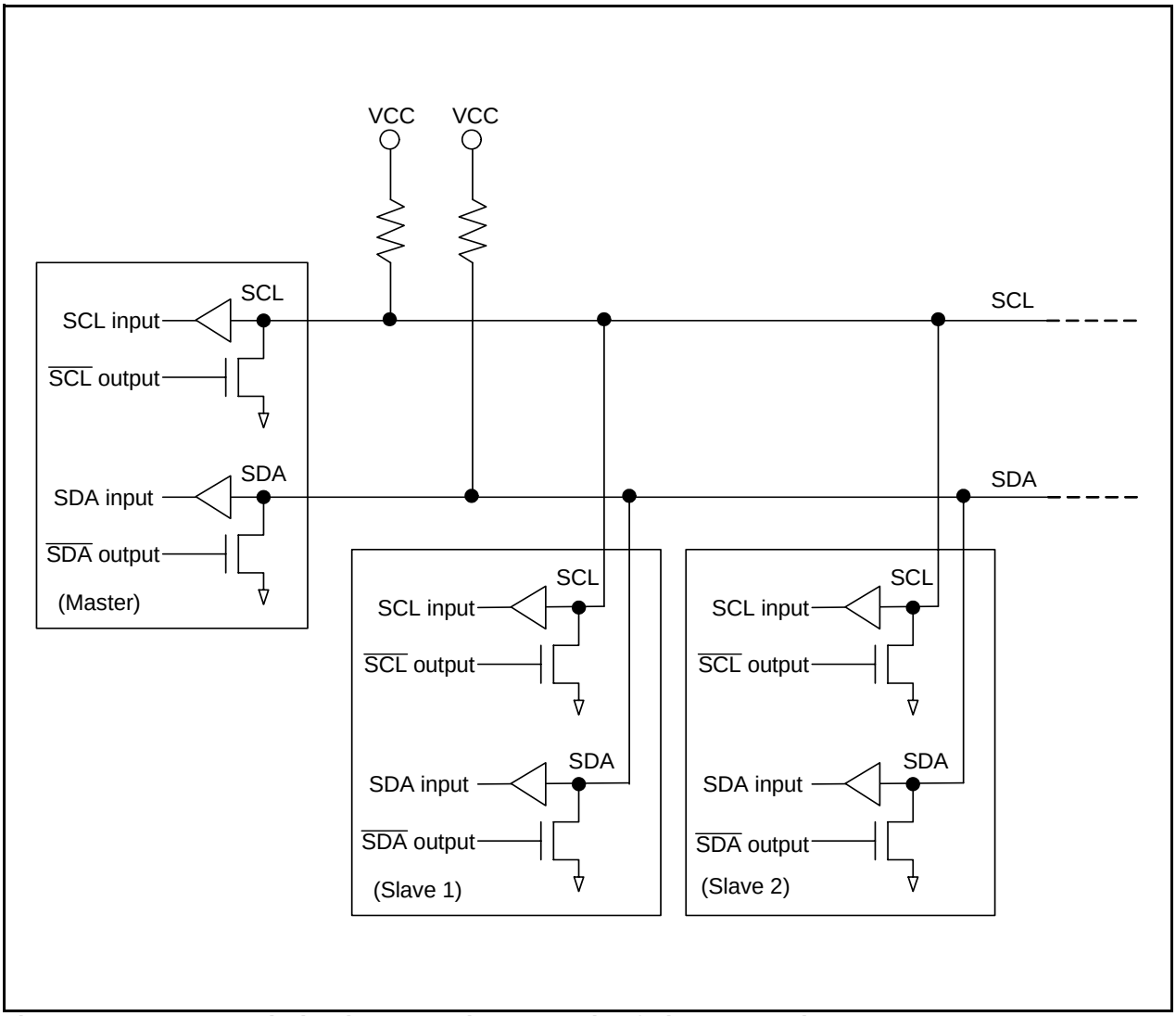
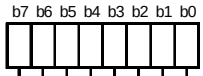


Figure 16.23 External Circuit Connection Example of Pins SCL and SDA

IIC Bus Control Register 1



Symbol	Address	After Reset
ICCR1	00B8h	00h

Bit Symbol	Bit Name	Function	RW
CKS0	Transmit clock select bit 3 to 0(1)	b3 b2 b1 b0 0 0 0 0 : f1/28 0 0 0 1 : f1/40 0 0 1 0 : f1/48 0 0 1 1 : f1/64 0 1 0 0 : f1/80 0 1 0 1 : f1/100 0 1 1 0 : f1/112 0 1 1 1 : f1/128 1 0 0 0 : f1/56 1 0 0 1 : f1/80 1 0 1 0 : f1/96 1 0 1 1 : f1/128 1 1 0 0 : f1/160 1 1 0 1 : f1/200 1 1 1 0 : f1/224 1 1 1 1 : f1/256	RW
CKS1			RW
CKS2			RW
CKS3			RW
TRS	Transfer / receive select bit(2,3,6)	b5 b4 0 0 : Slave receive mode(4) 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	RW
MST	Master / slave select bit(5,6)		RW
RCVD	Receive disable bit	After reading the ICDRR register while the TRS bit is set to 0 0 : Maintains the following receive operation 1 : Disables the following receive operation	RW
ICE	I²C bus interface enable bit	0 : This module is halted (SCL and SDA pins are set to port function) 1 : This module is enabled for transfer operations (SCL and SDA pins are bus drive state)	RW

NOTES:
1. Set according to the necessary transfer rate in master mode. Refer to **Table 16.6 Transfer Rate Examples** for the transfer rate. This bit is used for maintaining of the setup time in transmit mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between the transfer frame.
3. When the first 7 bits, after the start condition in slave receive mode, match with the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1.
4. In master mode with the I²C bus format, when arbitration is lost, the MST and TRS bits are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode of the clock synchronous serial format, the MST bit is set to 0 and the IIC enters slave receive mode.
6. In multimaster operation use the MOV instruction to set bits TRS and MST.

Figure 16.24 ICCR1 Register

IIC Bus Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
ICCR2	00B9h	01111101b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
IICRST	IIC control part reset bit	When hang-up occurs due to communication failure during I²C bus interface operation and write 1, reset control part of I²C bus interface without setting port and initializing register.	RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
SCLO	SCL monitor flag	0 : SCL pin is set to "L" 1 : SCL pin is set to "H"	RO
SDAOP	SDAO write protect bit	When rewrite to SDAO bit, write 0 simultaneously.(1) When read, its content is 1.	RW
SDAO	SDA output value control bit	When read 0 : SDA pin output is held "L" 1 : SDA pin output is held "H" When write(1,2) 0 : SDA pin output is changed to "L" 1 : SDA pin output is changed to high-impedance ("H" output is external pull-up resistor)	RW
SCP	Start / stop condition generation disable bit	When write to BBSY bit, write 0 simultaneously.(3) When read, its content is 1. Writing 1 is disabled.	RW
BBSY	Bus busy bit(4)	When read 0 : Bus is in released state (SDA signal changes from "L" to "H" while SCL signal is in "H" state) 1 : Bus is in occupied state (SDA signal changes from "H" to "L" while SCL signal is in "H" state) When write(3) 0 : Generates stop condition 1 : Generates start condition	RW

NOTES:
1. When writing to the SDAO bit, write 0 to the SDAOP bit using the MOV instruction simultaneously.
2. Do not write during transfer operation.
3. This bit is enabled in master mode. When write to the BBSY bit, write 0 to the SCP bit using the MOV instruction simultaneously. Execute the same way when the start condition is regenerating.
4. This bit is disabled when the clock synchronous serial format is used.

Figure 16.25 ICCR2 Register

IIC Bus Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

0

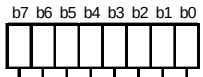
Symbol	Address	After Reset
ICMR	00BAh	00011000b

Bit Symbol	Bit Name	Function	RW
BC0	Bit counter 2 to 0	I²C bus format (remaining transfer bit numbers when read out and data bit numbers of transfer to the next when write)(1,2) b2 b1 b0 0 0 0 : 9 bits(3) 0 0 1 : 2 bits 0 1 0 : 3 bits 0 1 1 : 4 bits 1 0 0 : 5 bits 1 0 1 : 6 bits 1 1 0 : 7 bits 1 1 1 : 8 bits Clock synchronous serial format (when read, read the remaining transfer bit numbers and when write, write 000b.) b2 b1 b0 0 0 0 : 8 bits 0 0 1 : 1 bit 0 1 0 : 2 bits 0 1 1 : 3 bits 1 0 0 : 4 bits 1 0 1 : 5 bits 1 1 0 : 6 bits 1 1 1 : 7 bits	RW
BC1			RW
BC2			RW
BCWP	BC write protect bit	When rewrite to the BC0 to BC2 bits, write 0 simultaneously.(2,4) When read, its content is 1.	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
— (b5)	Reserved bit	Set to 0	RW
WAIT	Wait insertion bit(5)	0 : No wait (Transfer data and acknowledge bit consecutively) 1 : Wait (After the falling of the clock for the final data bit, “L” period is extended for two transfer clocks)	RW
MLS	MSB-first / LSB-first select	0 : Data transfer by MSB-first(6) 1 : Data transfer by LSB-first	RW

NOTES:
1. Rewrite between transfer frames. When write values other than 000b, write when the SCL signal is “L”.
2. When write to the BC0 to BC2 bits, write 0 to the BCWP bit using the MOV instruction.
3. After data including the acknowledge bit is transferred, bits b2 to b0 are automatically set to 000b. When the start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is enabled in master mode of the I²C bus format. It is disabled in slave mode of the I²C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I²C bus format is used.

Figure 16.26 ICMR Register

IIC Bus Interrupt Enable Register



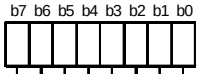
Symbol	Address	After Reset
ICIER	00BBh	00h

Bit Symbol	Bit Name	Function	RW
ACKBT	Transmit acknowledge select bit	0 : 0 is transmitted as acknowledge bit in receive mode 1 : 1 is transmitted as acknowledge bit in receive mode	RW
ACKBR	Receive acknowledge bit	0 : Acknowledge bit which is received from receive device in transmit mode is set to 0 1 : Acknowledge bit which is received from receive device in transmit mode is set to 1	RO
ACKE	Acknowledge bit judgment select bit	0 : Value of receive acknowledge bit is ignored and continuous transfer is performed 1 : When receive acknowledge bit is set to 1, continuous transfer is halted	RW
STIE	Stop condition detection interrupt enable bit	0 : Disables stop condition detection interrupt request 1 : Enables stop condition detection interrupt request(2)	RW
NAKIE	NACK receive interrupt enable bit	0 : Disables NACK receive interrupt request and arbitration lost / overrun error interrupt request 1 : Enables NACK receive interrupt request and arbitration lost / overrun error interrupt request(1)	RW
RIE	Receive interrupt enable bit	0 : Disables receive data full and overrun error interrupt request 1 : Enables receive data full and overrun error interrupt request(1)	RW
TEIE	Transmit end interrupt enable bit	0 : Disables transmit end interrupt request 1 : Enables transmit end interrupt request	RW
TIE	Transmit interrupt enable bit	0 : Disables transmit data empty interrupt request 1 : Enables transmit data empty interrupt request	RW

NOTES:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (enable stop condition detection interrupt request) when the STOP bit in the ICSR register is set to 0.

Figure 16.27 ICIER Register

IIC Bus Status Register(7)



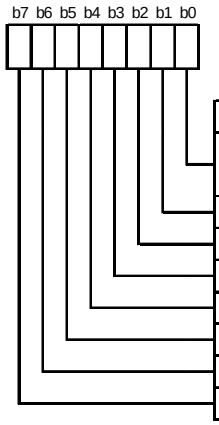
Symbol	Address	After Reset
ICSR	00BCh	0000X000b

Bit Symbol	Bit Name	Function	RW
ADZ	General call address recognition flag(1,2)	When detecting the general call address, this flag is set to 1.	RW
AAS	Slave address recognition flag(1)	This flag is set to 1 when the first frame following start condition matches the SVA0 to SVA6 bits in the SAR register in slave receive mode. (Detect the slave address and generate call address)	RW
AL	Arbitration lost flag / overrun error flag(1)	When the I²C bus format is used, this flag indicates that arbitration is lost in master mode. In the following case, this flag is set to 1.(3) • When the internal SDA signal and SDA pin level do not match at the rise of the SCL signal in master transmit mode • When the start condition is detected and the SDA pin is held "H" in master transmit / receive mode This flag indicates that an overrun error occurs when the clock synchronous format is used In the following case, this flag is set to 1. • When the last bit of the following data is received while the RDRF bit is set to 1	RW
STOP	Stop condition detection flag(1)	When the stop condition is detected after the frame is transferred, this flag is set to 1	RW
NACKF	No acknowledge detection flag(1,4)	When no acknowledge is detected from receive device when transmit, this flag is set to 1	RW
RDRF	Receive data register full(1,5)	When receive data is transferred from ICDRS to ICDRR registers, this flag is set to 1	RW
TEND	Transmit end(1,6)	When the 9th clock of the SCL signal with the I²C bus format while the TDRE bit is set to 1, this flag is set to 1 This flag is set to 1 when the final bit of the transmit frame is transmitted with the clock synchronous format	RW
TDRE	Transmit data empty(1,6)	In the following cases, this flag is set to 1 • Data is transferred from ICDRT to ICDRS registers and ICDRT register is empty • When setting the TRS bit in the ICCR1 register to 1 (transmit mode) • When generating the start condition (including retransmit) • When changing from slave receive mode to slave transmit mode	RW

NOTES:
1. Each bit is set to 0 when reading 1 before writing 0.
2. This flag is enabled in slave receive mode of the I²C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I²C bus Interface monitors the SDA pin and the data which the IIC transmits is different, the AL flag is set to 1 and the bus is occupied by the other masters.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted)
5. The RDRF bit is set to 0 when reading data from the ICDRR register.
6. The TEND and TDRE bits are set to 0 when writing data to the ICDRT register.
7. When accessing the ICSR register continuously, insert one or more NOP instructions between the instructions to access it.

Figure 16.28 ICSR Register

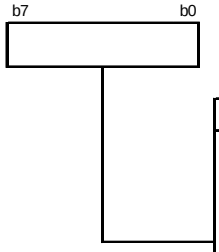
Slave Address Register



Symbol	Address	After Reset
SAR	00BDh	00h

Bit Symbol	Bit Name	Function	RW
FS	Format select bit	0 : I²C bus format 1 : Clock synchronous serial format	RW
SVA0	Slave address 6 to 0	Set the different address from the other slave devices which are connected to the I²C bus. When the 7 high-order bits of the first frame transmitted after the starting condition match the SVA0 to SVA6 bits in slave mode of the I²C bus format, the MCU operates as a slave device.	RW
SVA1			RW
SVA2			RW
SVA3			RW
SVA4			RW
SVA5			RW
SVA6			RW

IIC Bus Transmit Data Register

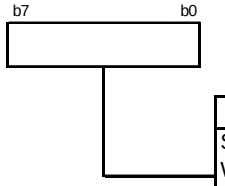


Symbol	Address	After Reset
ICDRT	00BEh	FFh

Function	RW
Store transmit data When detecting that the ICDRS register is empty, the stored transmit data is transferred to the ICDRS register and the starts transmit data. When the next transmit data is written to the ICDRT register during transmitting the data of the ICDRS register, continuous transmit is enabled. When the MLS bit in the ICMR register is set to 1 (data transferred by LSB-first) and after the data is written to the ICDRT register, the MSB and LSB inverted data is read.	RW

Figure 16.29 Registers SAR and ICDRT

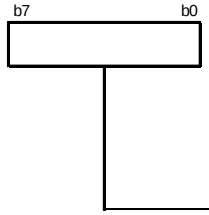
IIC Bus Receive Data Register



Symbol	Address	After Reset
ICDRR	00BFh	FFh

Function	RW
Store receive data When the ICDRS register receives 1-byte data, the receive data is transferred to the ICDRR register and the next receive is enabled.	RO

IIC Bus Shift Register

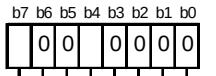


Symbol
ICDRS

Function	RW
This register is a register that is used to transmit and receive data. The transmit data is transferred from the ICDRT to ICDRS registers and data is transmitted from the SDA pin when transmitting. When 1-byte data is received, data is transferred from the ICDRS to ICDRR registers when receiving.	—

Figure 16.30 Registers ICDRR and ICDRS

Port Mode Register



Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0	—
U1PINSEL	Port TXD1/RXD1 switch bit	0 : I/O port P6_6, P6_7 1 : TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0	—
IICSEL	SSU/I²C bus switch bit	0 : SSU function selects 1 : I²C bus function selects	RW

Figure 16.31 PMR Register

16.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0, the transfer clock is the external clock input from the SCL pin. When the MST bit in the ICCR1 register is set to 1, the transfer clock is the internal clock selected by the CKS0 to CKS3 bits in the ICCR1 register and the transfer clock is output from the SCL pin.
Table 16.6 lists the Transfer Rate Examples.

Table 16.6 Transfer Rate Examples

ICCR1 Register				Transfer Clock	Transfer Rate				
CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
			1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
		1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
			1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
	1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
			1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
		1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
			1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
			1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
		1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
			1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
	1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
			1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
		1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
			1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

16.3.2 Interrupt Requests

The interrupt request of the I²C bus interface contains 6 types when the I²C bus format is used and 4 types when the clock synchronous serial format is used.

Table 16.7 lists the Interrupt Requests of I²C Bus Interface.

Since these interrupt requests are allocated at the I²C bus interface interrupt vector table, determining the source by each bit is necessary.

Table 16.7 Interrupt Requests of I²C Bus Interface

Interrupt Request		Generation Condition	Format	
			I²C bus	Clock Synchronous Serial
Transmit Data Empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit Ends	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive Data Full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop Condition Detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK Detection	NAKI	NAKIE = 1 and AL = 1 (or NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration Lost / Overrun Error			Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register
AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When the generation conditions on the Table 16.7 are met, the I²C bus interface interrupt request is generated. Set the interrupt generation conditions to 0 by the I²C bus interface interrupt routine. However, the TDRE and TEND bits are automatically set to 0 by writing transmit data to the ICDRT register and the RDRF bit is automatically set to 0 by reading the ICDRR register. When writing transmit data to the ICDRT register, the TDRE bit is set to 0. When data is transferred from the ICDRT to ICDRS registers, the TDRE bit is set to 1 and when further setting the TDRE bit to 0, extra 1 byte may be transmitted.

Also, set the STIE bit to 1 (enable stop condition detection interrupt request) when the STOP bit is set to 0.

16.3.3 I²C Bus Interface Mode

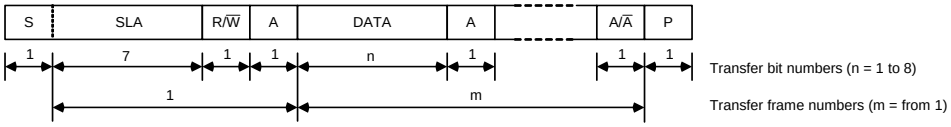
16.3.3.1 I²C Bus Format

Setting the FS bit in the SAR register to 0 communicates in I²C bus format.

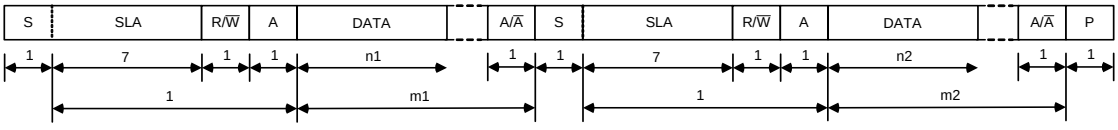
Figure 16.32 shows the I²C Bus Format and Bus Timing. The 1st frame following start condition consists of 8 bits.

(1) I²C bus Format

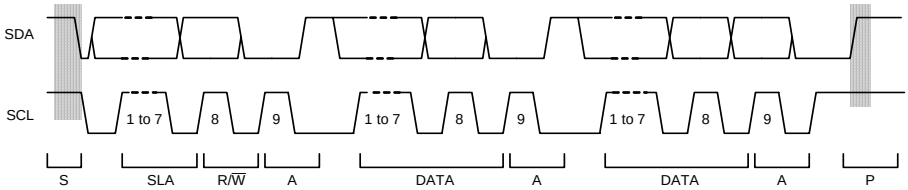
(a) I²C bus format (FS = 0)



(b) I²C bus format (when start condition is retransmitted, FS = 0)



(2) I²C bus timing



Explanation of symbols
S : Start condition
The master device changes the SDA signal from “H” to “L” while the SCL signal is held “H”.
SLA : Slave address
R/W : Indicates the direction of data transmit/receive
Data is transmitted from the slave device to the master device when R/W value is 1 and from the master device to the slave device when R/W value is 0.
A : Acknowledge
The receive device sets the SDA signal to “L”.
DATA : Transmit / receive data
P : Stop condition
The master device changes the SDA signal from “L” to “H” while the SCL signal is held “H”.

Figure 16.32 I²C Bus Format and Bus Timing

16.3.3.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal.

Figure 16.33 and Figure 16.34 show the Operation Timing in Master Transmit Mode (I^2C Bus Interface Mode).

The transmit procedure and operation in master transmit mode are shown below.

(1) Set the STOP bit in the ICSR register to 0 to reset it. And then set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set the WAIT and MLS bits in the ICMR register and set the CKS0 to CKS3 bits in the ICCR1 register (initial setting).

(2) Read the BBSY bit in the ICCR2 register to confirm that the bus is free. Set the TRS and MST bits in the ICCR1 register to master transmit mode. The start condition is generated by writing 1 to the BBSY bit and 0 to the SCP bit by the MOV instruction.

(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from the ICDRT to ICDRS registers), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are shown at the 1st byte). At this time, the TDRE bit is automatically set to 0 and data is transferred from the ICDRT to ICDRS registers, the TDRE bit is set to 1 again.

(4) When the transmit of 1-byte data is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rise of the 9th transmit clock pulse. Read the ACKBR bit in the ICIER register, and confirm that the slave is selected. Write the 2nd-byte data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate the stop condition. The stop condition is generated by the writing 0 to the BBSY bit and 0 to the SCP bit by the MOV instruction. The SCL signal is held “L” until data is available and the stop condition is generated.

(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.

(6) When writing the number of bytes to be transmitted to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (the NACKF bit in the ICSR register is set to 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). And generate the stop condition before setting the TEND and NACKF bits to 0.

(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

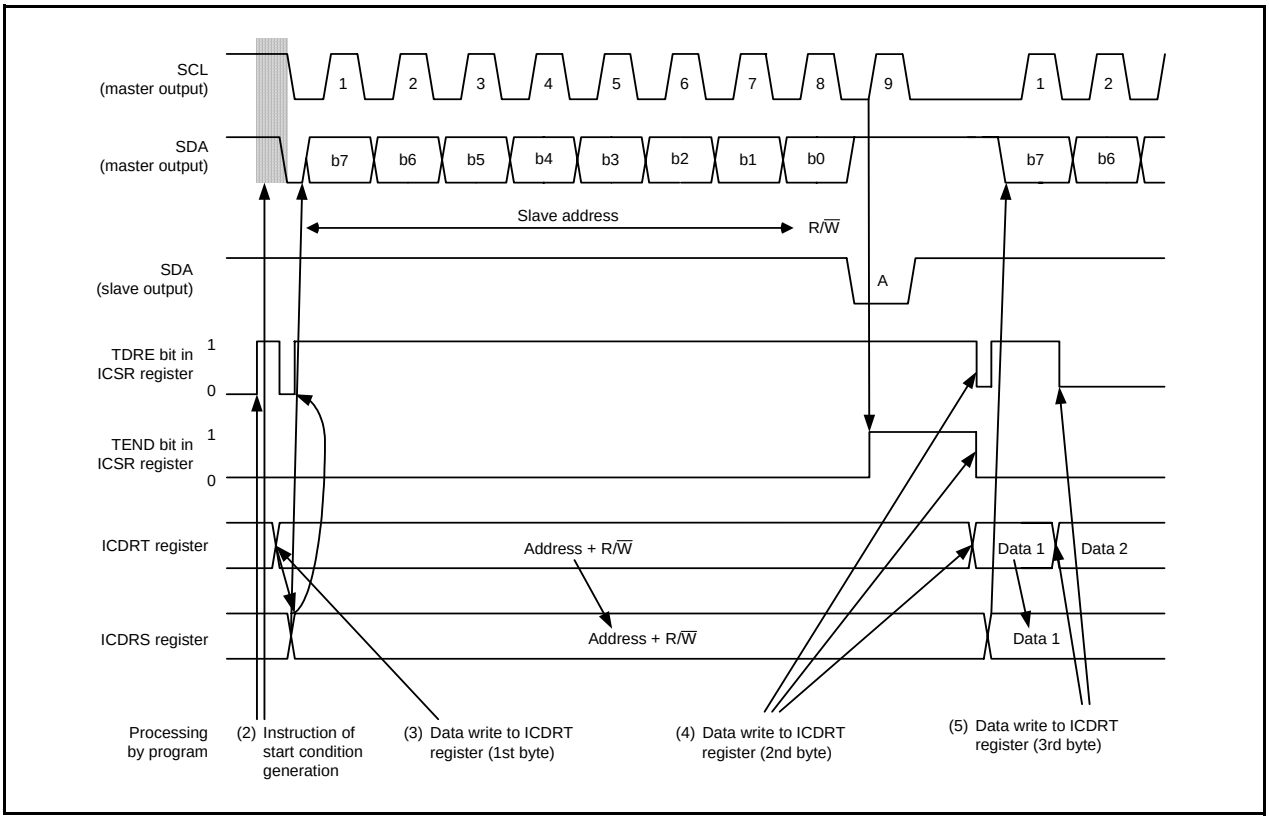


Figure 16.33 Operating Timing in Master Transmit Mode (I^2C Bus Interface Mode) (1)

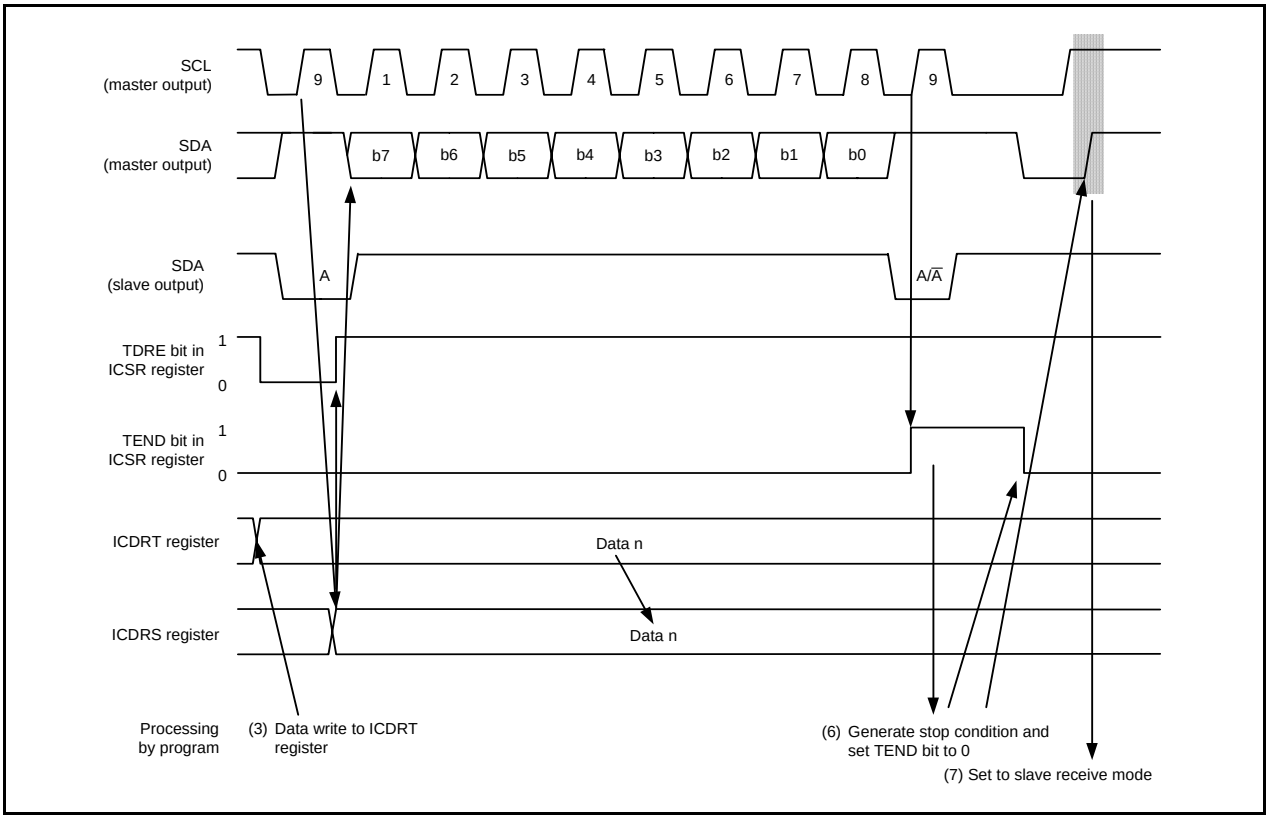


Figure 16.34 Operating Timing in Master Transmit Mode (I^2C Bus Interface Mode) (2)

16.3.3.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal.

Figure 16.35 and Figure 16.36 show the Operation Timing in Master Receive Mode (I^2C Bus Interface Mode).

The receive procedure and operation in master receive mode are shown below.

(1) After setting the TEND bit in the ICSR register to 0, switch from master transmit mode to master receive mode by setting the TRS bit in the ICCR1 register. And set the TDRE bit in the ICSR register to 0.

(2) When performing the dummy-read of the ICDRR register and starting receive, output the receive clock synchronizing with the internal clock and receive data. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the 9th clock of the receive clock.

(3) The 1-frame data receive is completed and the RDRF bit in the ICSR register is set to 1 at the rise of the 9th clock. At this time, when reading the ICDRR register, the received data can be read and the RDRF bit is set to 0 simultaneously.

(4) The continuous receive is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock falls after reading the ICDRR register by the other processes while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read.

(5) If the following frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (disables the next receive operation) before reading the ICDRR register, the stop condition generation is enabled after the following receive.

(6) When the RDRF bit is set to 1 at the rise of the 9th clock of the receive clock, generate the stop condition.

(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register. And set the RCVD bit to 0 (maintain the following receive operation).

(8) Return to slave receive mode.

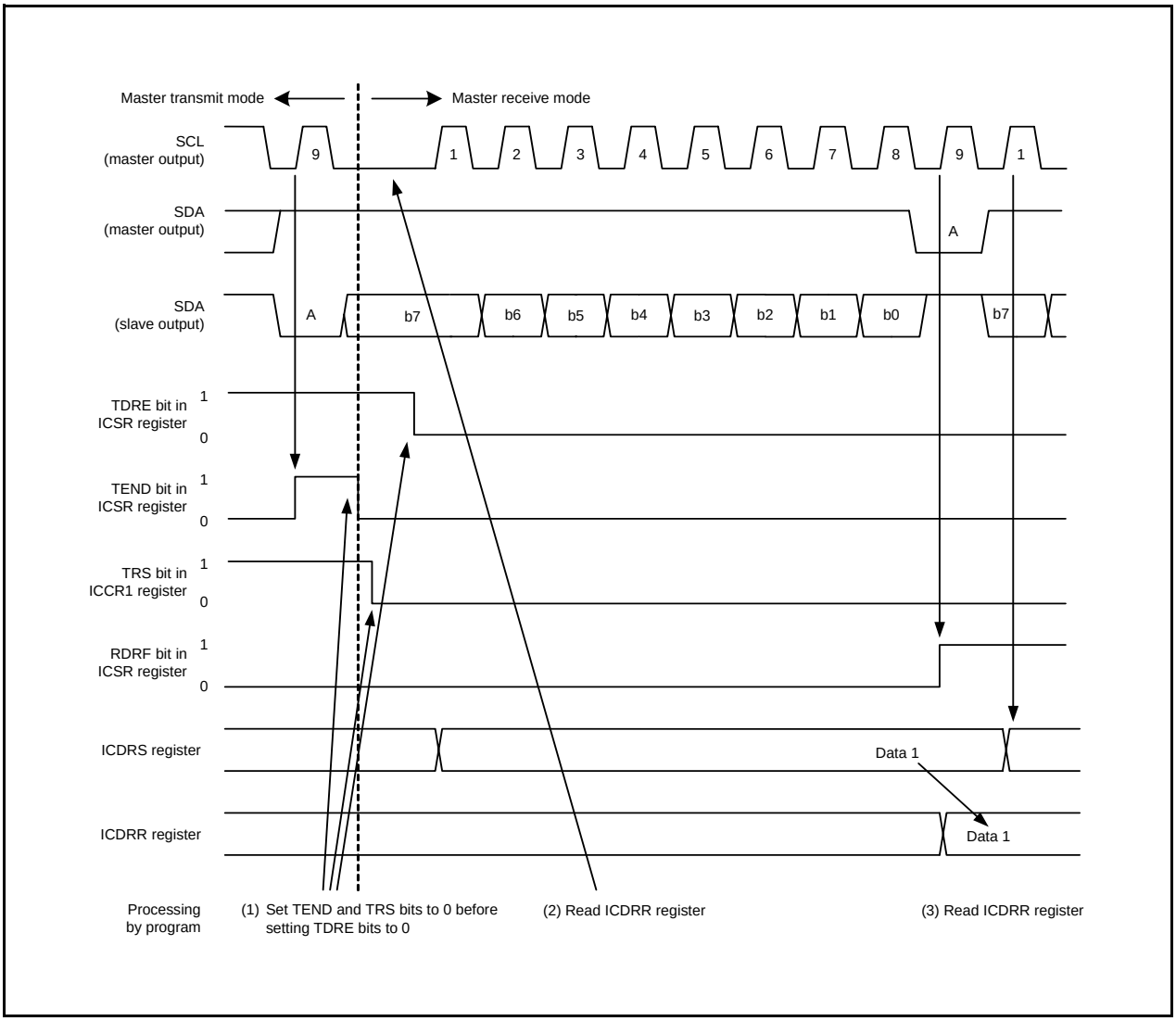


Figure 16.35 Operating Timing in Master Receive Mode (I^2C Bus Interface Mode) (1)

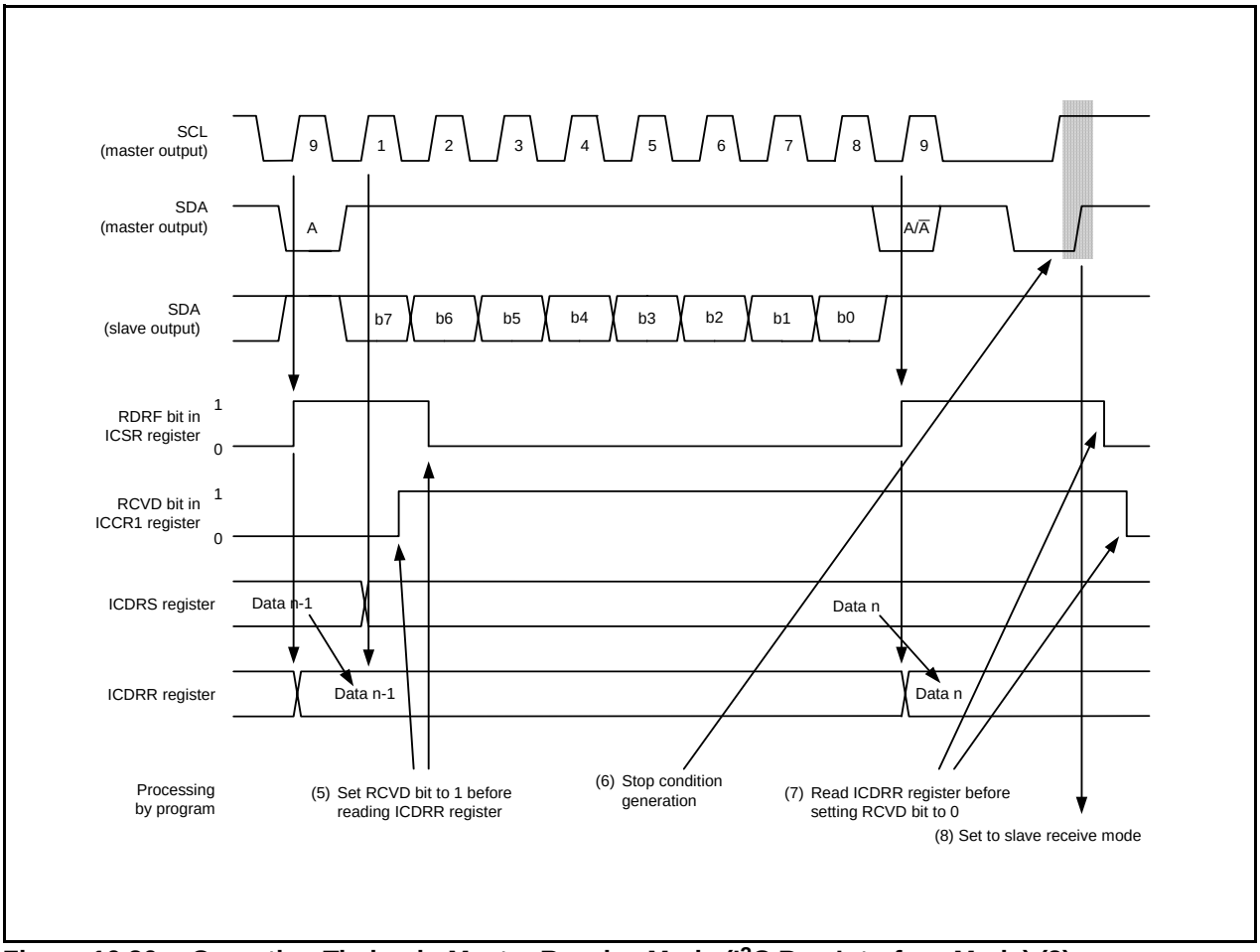


Figure 16.36 Operating Timing in Master Receive Mode (I^2C Bus Interface Mode) (2)

16.3.3.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal.

Figure 16.37 and Figure 16.38 show the Operation Timing in Slave Transmit Mode (I^2C Bus Interface Mode).

The transmit procedure and operation in slave transmit mode are shown below.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set the WAIT and MLS bits in the ICMR register and CKS0 to CKS3 bits in the ICCR1 register (initial setting). Set the TRS and MST bits in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the 1st frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rise of the 9th clock. At this time, if the 8-bit data (R/$\overline{W}$) is set to 1, the TRS and TDRE bit in the ICSR register are set to 1, the mode is switched to slave transmit mode automatically. When writing transmit data to the ICDRT register every time the TDRE bit is set to 1, the continuous transmit is enabled.

(3) When the TDRE bit in the ICDRT register is set to 1 after writing the last transmit data to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) The SCL signal is released by setting the TRS bit to 0 and performing the dummy-read of the ICDRR register for the end process.

(5) Set the TDRE bit to 0.

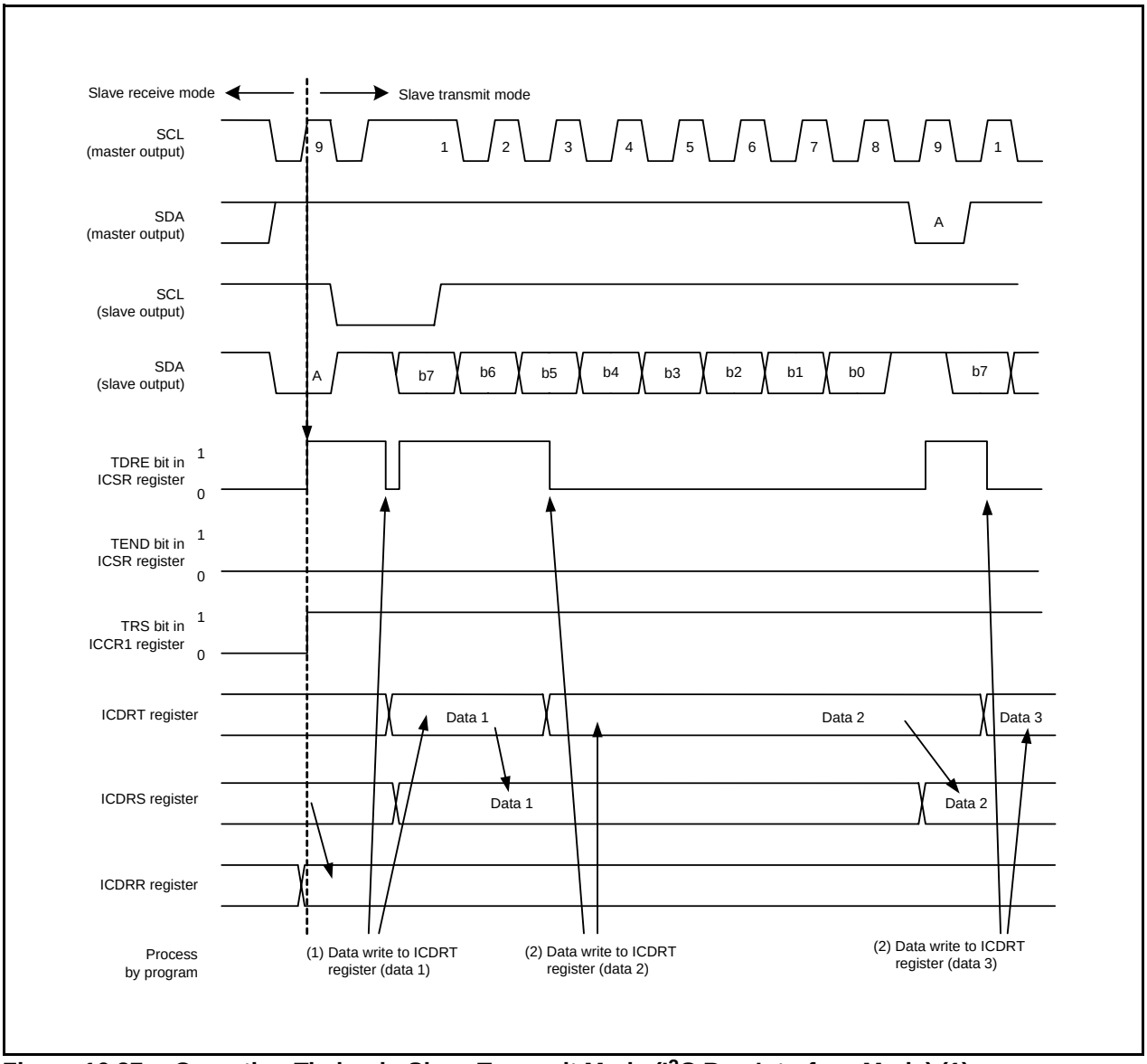


Figure 16.37 Operating Timing in Slave Transmit Mode (I^2C Bus Interface Mode) (1)

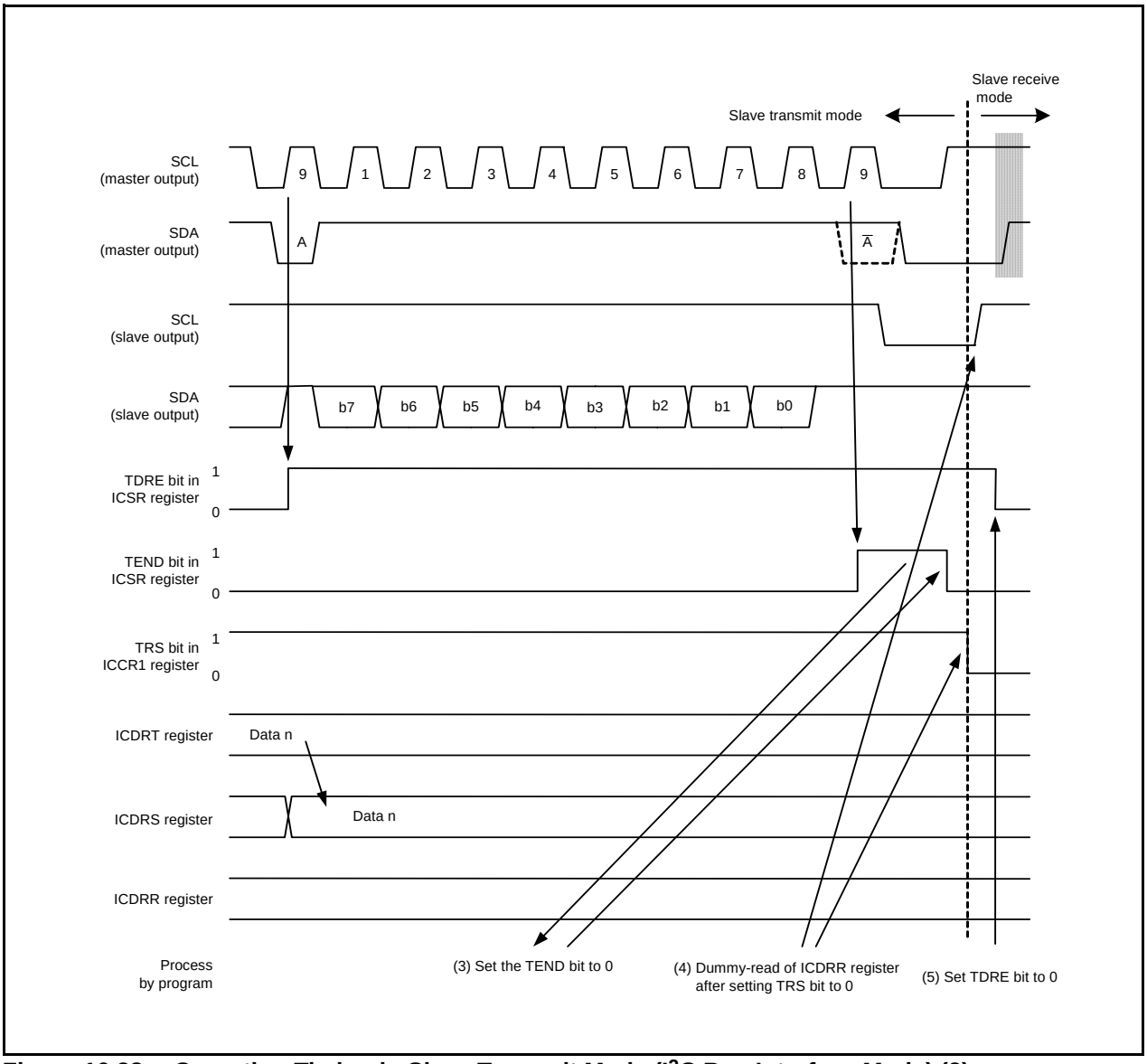


Figure 16.38 Operating Timing in Slave Transmit Mode (I^2C Bus Interface Mode) (2)

16.3.3.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal.

Figure 16.39 and Figure 16.40 show the Operation Timing in Slave Receive Mode (I^2C Bus Interface Mode).

The receive procedure and operation in slave receive mode are shown below.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set the WAIT and MLS bits in the ICMR register and CKS0 to CKS3 bits in the ICCR1 register (initial setting). Set the TRS and MST bits in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the 1st frame after detecting the start condition, the slave device outputs the level set in the ACKBT bit in the ICIER register to the SDA pin at the rise of the 9th clock. Since the RDRF bit in the ICSR register is set to 1 simultaneously, perform the dummy-read (the read data is unnecessary because of showing slave address and R/$\overline{W}$).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock falls while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read. The setting change of the acknowledge signal which returns to master device before reading the ICDRR register reflects the following transfer frame.

(4) Reading the last byte is performed by reading the ICDRR register as well.

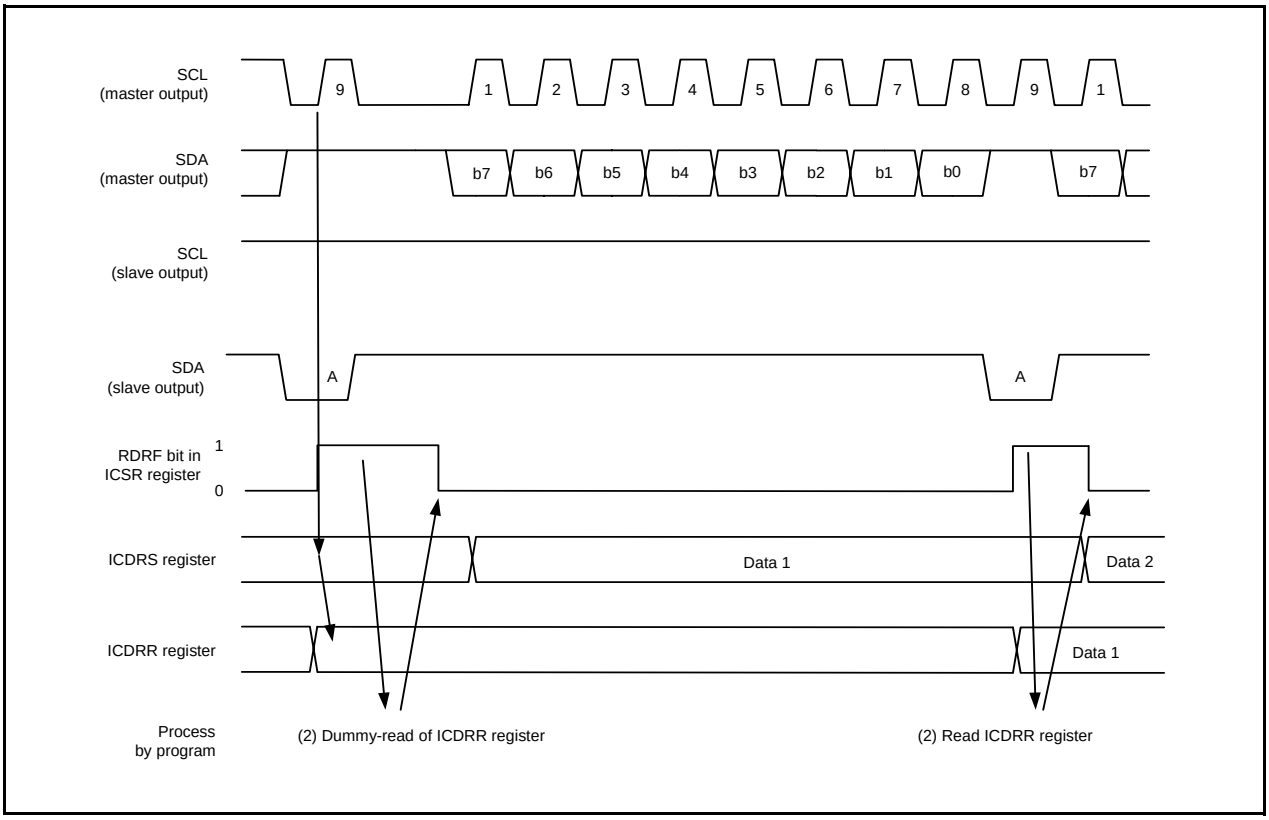


Figure 16.39 Operating Timing in Slave Receive Mode (I^2C Bus Interface Mode) (1)

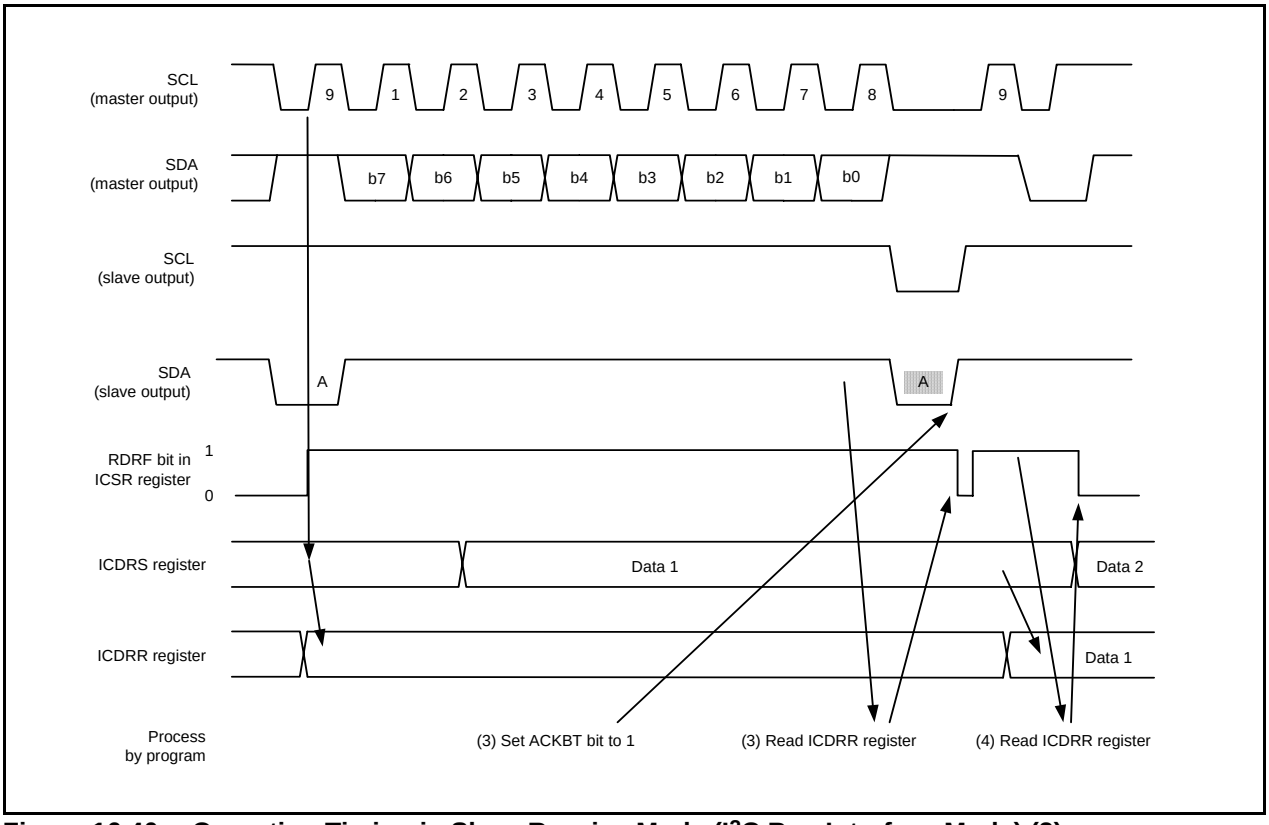


Figure 16.40 Operating Timing in Slave Receive Mode (I^2C Bus Interface Mode) (2)

16.3.4 Clock Synchronous Serial Mode

16.3.4.1 Clock Synchronous Serial Format

When setting the FS bit in the SAR register to 1, the clock synchronous serial format is used to communicate. Figure 16.41 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is output from the SCL pin and when the MST bit is set to 0, the external clock is input.

The transfer data is output between the fall and the following fall of the SCL clock, and data is determined by the rise of the SCL clock. The MSB-first or LSB-first can be selected for the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during the transfer standby.

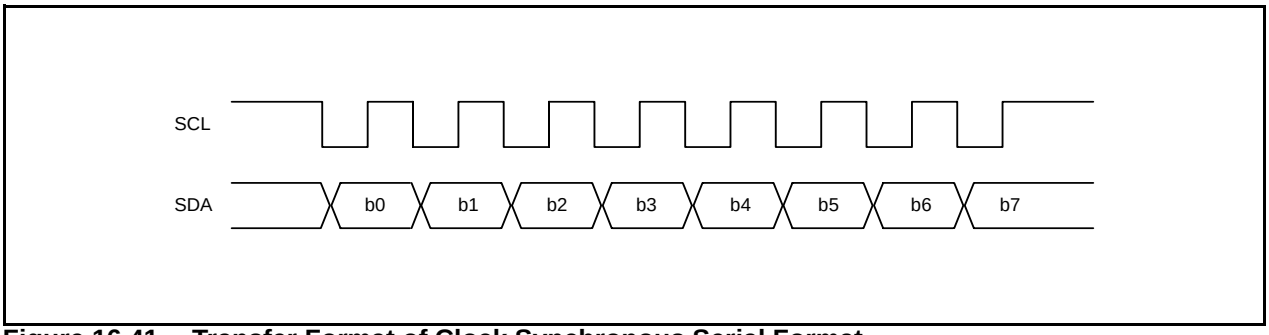


Figure 16.41 Transfer Format of Clock Synchronous Serial Format

16.3.4.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin synchronizing with the fall of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 16.42 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are shown below.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set the CKS0 to CKS3 bits in the ICCR1 register and set the MST bit (initial setting).
(2) The TDRE bit in the ICSR register is set to 1 by selecting transmit mode after setting the TRS bit in the ICCR1 register to 1.
(3) Data is transferred from the ICDRT to ICDRS registers and the TDRE bit is automatically set to 1 by writing transmit data to the ICDRT register after confirming that the TDRE bit is set to 1. When writing data to the ICDRT register every time the TDRE bit is set to 1, the continuous transmit is enabled. When switching from transmit to receive modes, set the TRS bit to 0 while the TDRE bit is set to 1.

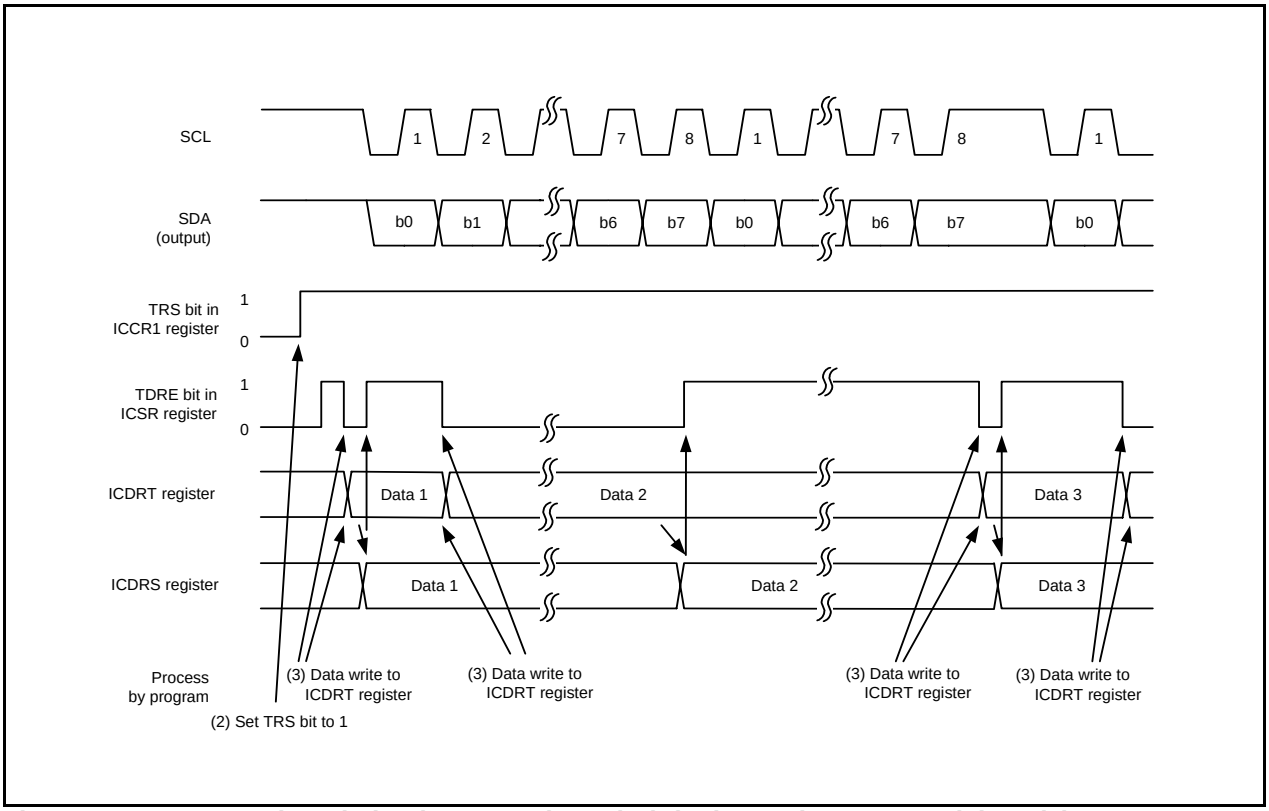


Figure 16.42 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

16.3.4.3 Receive Operation

In receive mode, data is latched at the rise of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 16.43 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are shown below.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set the CKS0 to CKS3 bits in the ICCR1 register and set the MST bit (initial setting).
(2) The output of the receive clock stars by setting the MST bit to 1 when the transfer clock is output.
(3) Data is transferred from the ICDRS to ICDRR registers and the RDRF bit in the ICSR register is set to 1, when the receive is completed. Since the following-byte data is enabled to receive when the MST bit is set to 1, the continuous clock is output. The continuous receive is enabled by reading the ICDRR register every time the RDRF bit is set to 1. An overrun is detected at the rise of the 8th clock while the RDRF bit is set to 1, the AL bit in the ICSR register is set to 1. At this time, the former receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (disables the following receive operation) and read the ICDRR register. The SCL signal is fixed “H” after the receive of the following-byte data is completed.

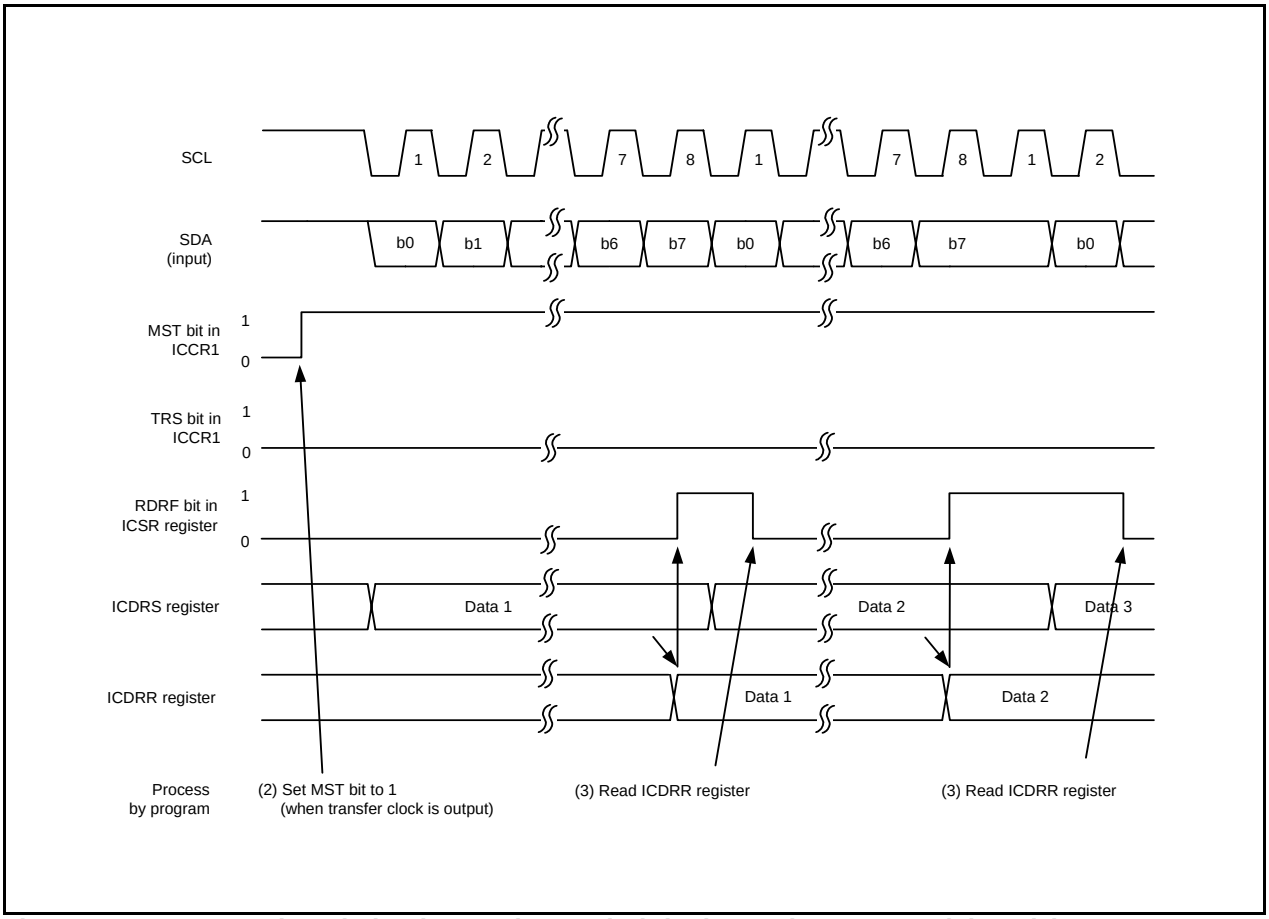


Figure 16.43 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

16.3.5 Noise Canceller

The state of the SCL and SDA pins are routed through the noise rejection circuit before being latched internally. Figure 16.44 shows the Block Diagram of Noise Canceller.

The noise rejection circuit consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and 2 latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

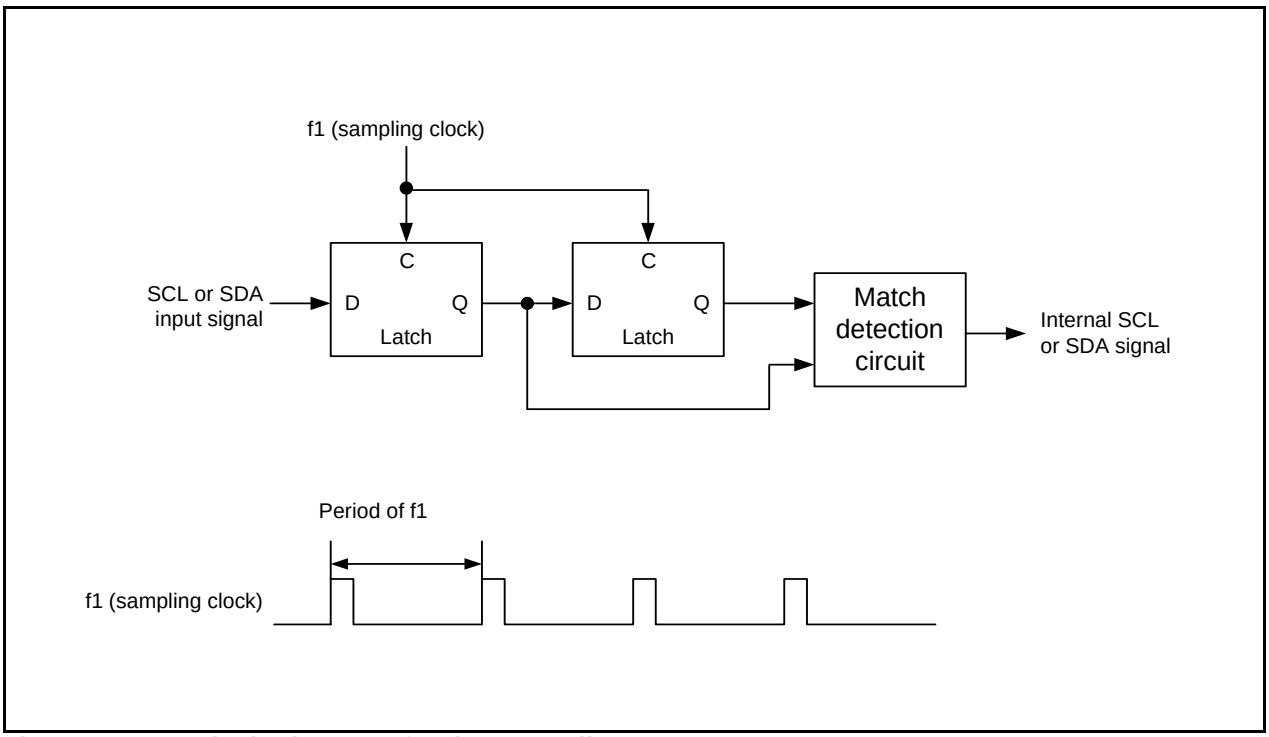


Figure 16.44 Block Diagram of Noise Canceller

16.3.6 Bit Synchronization Circuit

When setting the I^2C bus interface in master mode.

- When the SCL signal is driven to “L” by the slave device.
- Since the “H” period may become shorter while the SCL signal is driven to “L” by the slave device and the rising speed of the SCL signal is lowered by the load (load capacity and pull-up resistor) of the SCL line, the SCL signal is monitored and the communication synchronizes per bit.

Figure 16.45 shows the Timing of Bit Synchronous Circuit and Table 16.8 lists the Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring of SCL Signal.

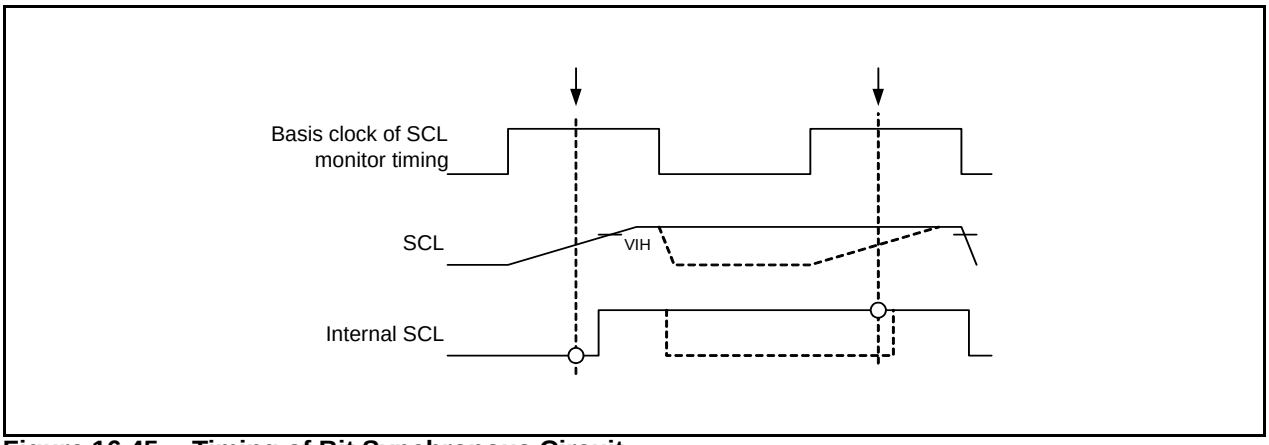


Figure 16.45 Timing of Bit Synchronous Circuit

Table 16.8 Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring of SCL Signal

ICCR1 Register		Time for Monitoring SCL
CKS3	CKS2	
0	0	7.5 Tcyc
	1	19.5 Tcyc
1	0	17.5 Tcyc
	1	41.5 Tcyc

1 Tcyc = 1/f1(s)

16.3.7 Examples of Register Setting

Figure 16.46 to Figure 16.49 show the Examples of Register Setting When Using I2C Bus Interface.

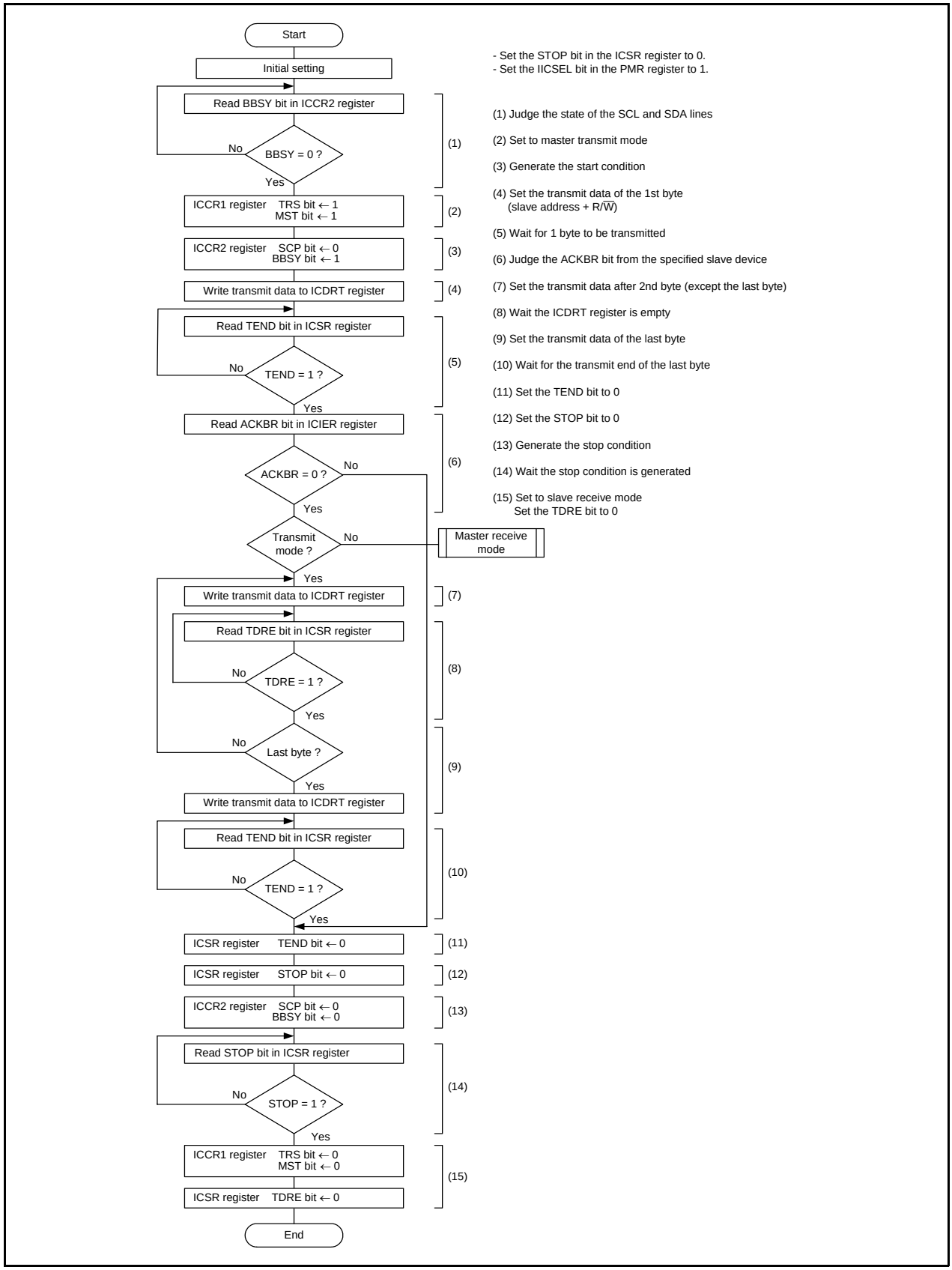
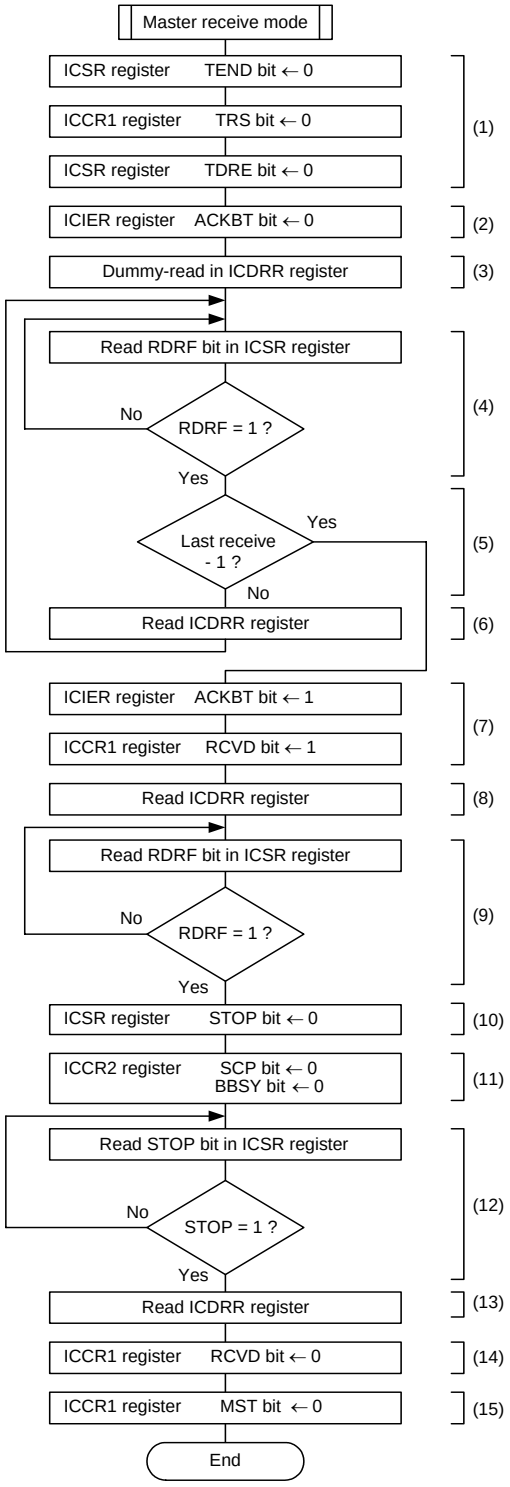


Figure 16.46 Example of Register Setting in Master Transmit Mode (I2C Bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0(1,2)

(2) Set the ACKBT bit to the transmit device(1)

(3) Dummy-read to the ICDRR register(1)

(4) Wait for 1 byte to be received

(5) Judge (last receive - 1)

(6) Read the receive data

(7) Set the ACKBT bit of the last byte and set to disable the continuous receive (RCVD = 1)(2)

(8) Read the receive data of (last byte - 1)

(9) Wait the last byte is received

(10) Set the STOP bit to 0

(11) Generate the stop condition

(12) Wait the stop condition is generated

(13) Read the receive data of the last byte

(14) Set the RCVD bit to 0

(15) Set to slave receive mode

NOTES:
1. Do not generate the interrupt during the process of step (1) to (3).
2. When receiving 1 byte, skip step (2) to (6) after (1) and jump to process of step (7). Process of step (8) is dummy-read in the ICDRR register.

Figure 16.47 Example of Register Setting in Master Receive Mode (I^2C Bus Interface Mode)

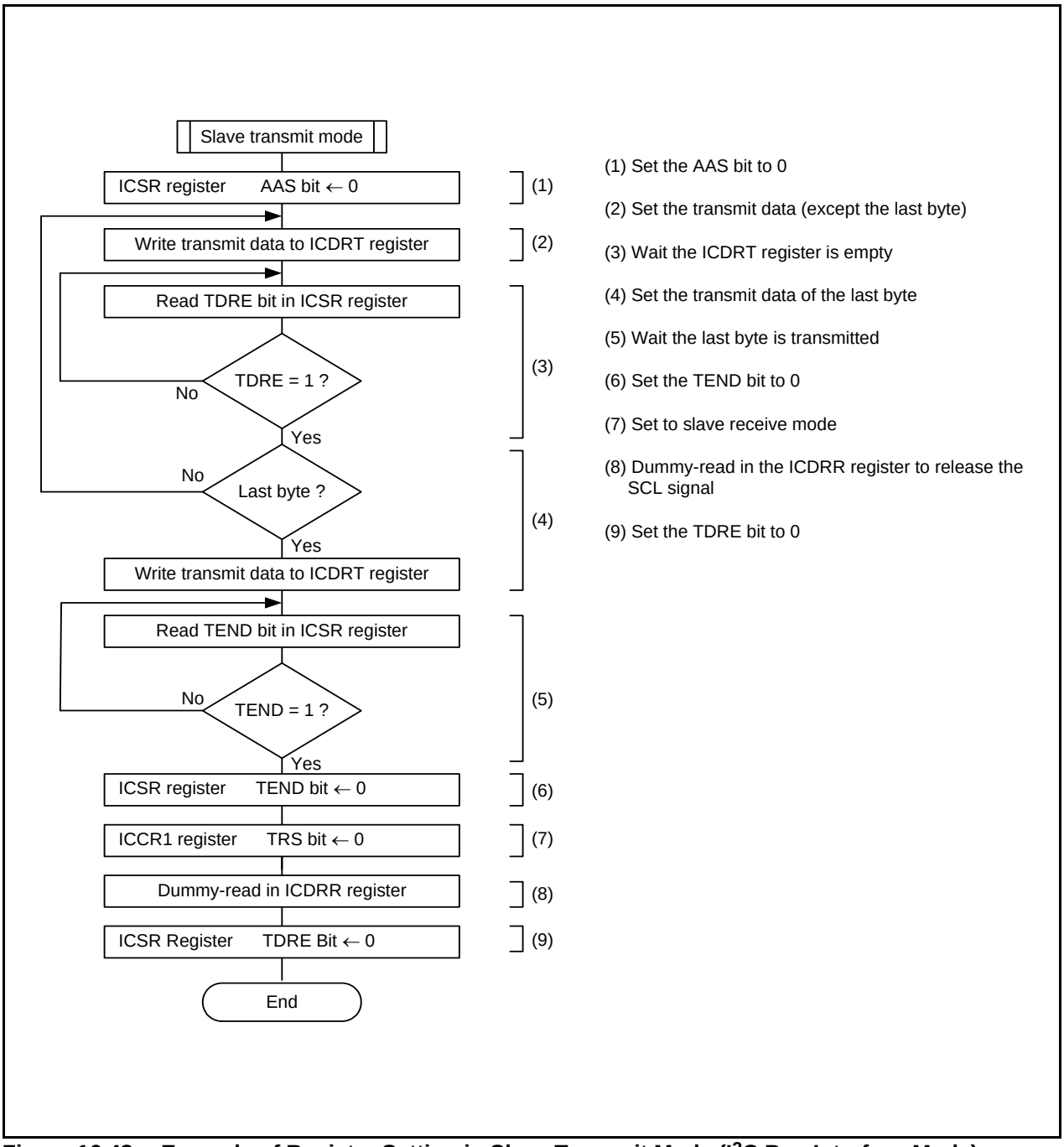
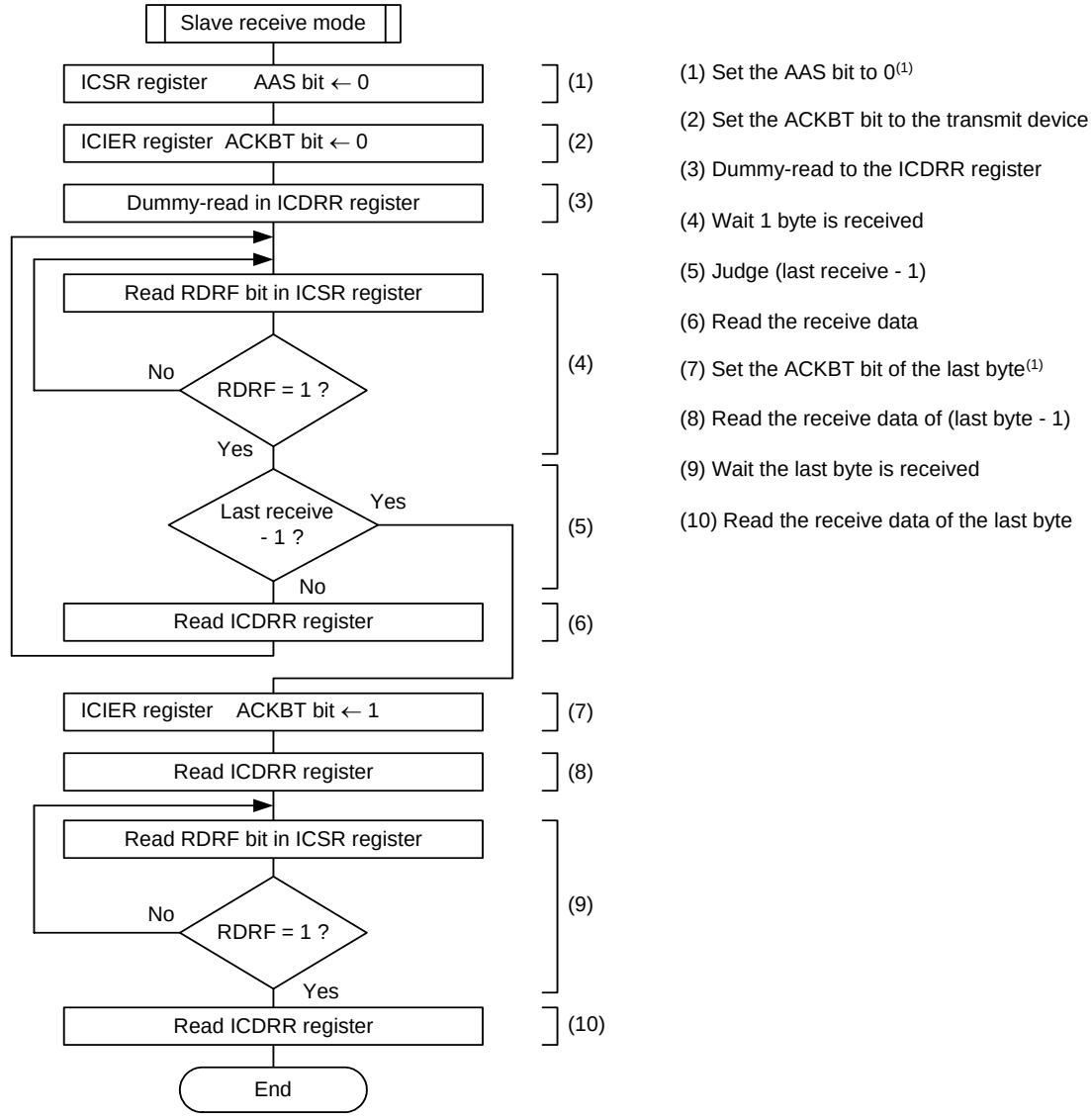


Figure 16.48 Example of Register Setting in Slave Transmit Mode (I^2C Bus Interface Mode)



NOTE:
1. When receiving 1 byte, skip steps (2) to (6) after (1) and jump to process of step (7). Process of step (8) is dummy-read in the ICDRR register.

Figure 16.49 Example of Register Setting in Slave Receive Mode (I^2C Bus Interface Mode)

16.3.8 Notes on I²C Bus Interface

Set the IICSEL bit in the PMR register to 1 (select I²C bus interface function) to use I²C bus interface.

16.3.8.1 Multimaster Operation

The following actions must be performed to use the I²C bus interface in multimaster operation.

- Transfer rate
  Set the transfer rate by 1/1.8 or faster than the fastest rate of the other masters. For example, if the fastest transfer rate of the other masters is set to 400 kbps, the I²C-bus transfer rate in this MCU should be set to 223 kbps (= 400/1.18) or more.

- Bits MST and TRS in the ICCR1 register setting

(a) Use the MOV instruction to set bits MST and TRS.
(b) When arbitration is lost, confirm the contents of bits MST and TRS. If the contents are other than the MST bit set to 0 and the TRS bit set to 0 (slave receive mode), set the MST bit to 0 and the TRS bit to 0 again.

16.3.8.2 Master Receive Mode

Either of the following actions must be performed to use the I²C bus interface in master receive mode.

(a) In master receive mode while the RDRF bit in the ICSR register is set to 1, read the ICDRR register before the rising edge of the 8th clock.
(b) In master receive mode, set the RCVD bit in the ICCR1 register to 1 (disables the next receive operation) to perform 1-byte communications.

17. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RA and UART0.

17.1 Features

The hardware LIN has the following features.
Figure 17.1 shows a Block Diagram of Hardware LIN.

[Master mode]

- Generates Synch Break
- Detects bus collision

[Slave mode]

- Detects Synch Break
- Measures Synch Field
- Controls Synch Break and Synch Field signal inputs to UART0
- Detects bus collision

NOTE:
1. The WakeUp function is detected by INT1.

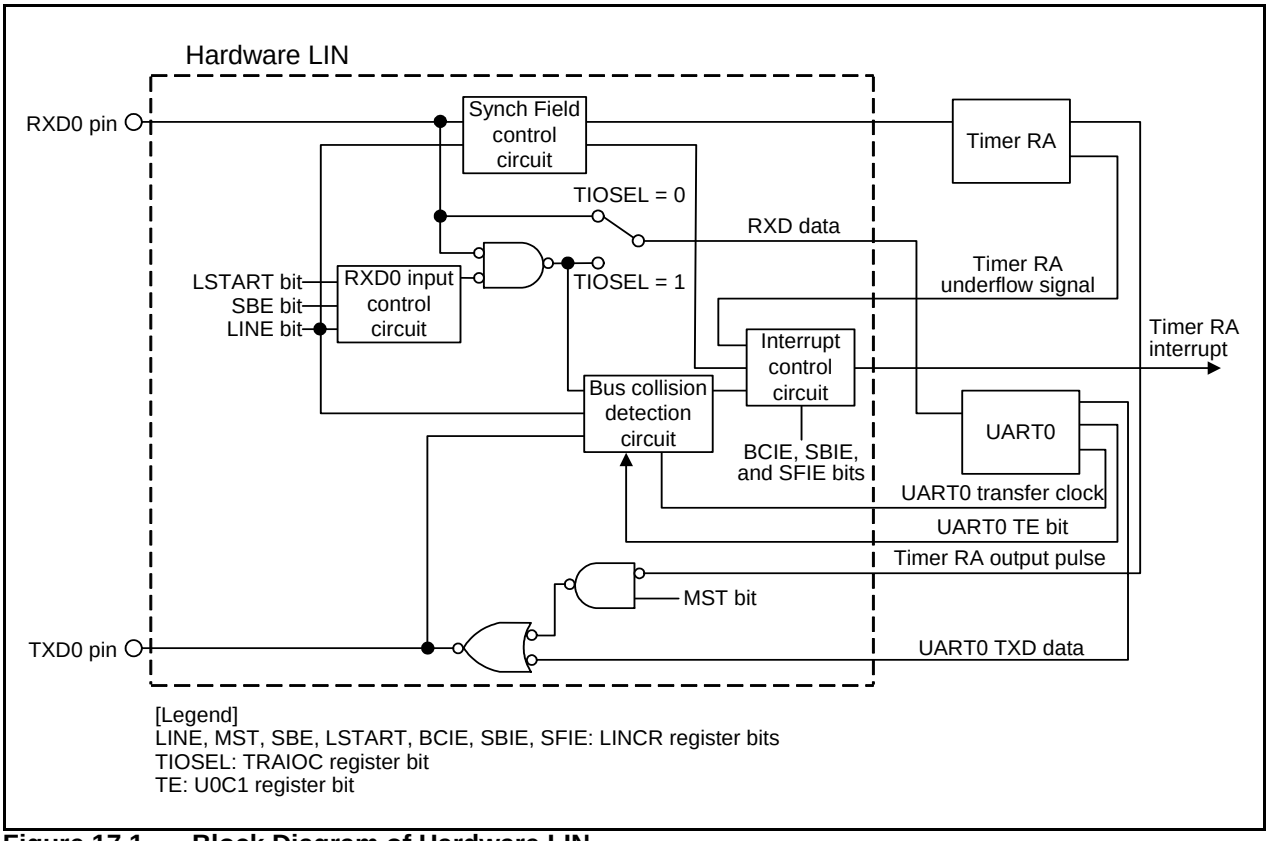


Figure 17.1 Block Diagram of Hardware LIN

17.2 Input/Output Pins

Table 17.1 lists the Pin Configuration of the hardware LIN.

Table 17.1 Pin Configuration

Name	Abbreviation	Input/Output	Function
Receive Data Input	RXD0	Input	Receive data input pin of the hardware LIN
Transmit Data Output	TXD0	Output	Transmit data output pin of the hardware LIN

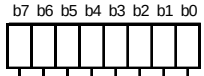
17.3 Register Configuration

The hardware LIN contains the following registers.

- LIN Control Register (LINCR)
- LIN Status Register (LINST)

Figure 17.2 and Figure 17.3 show the LINCR and LINST Registers.

LIN Control Register



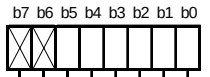
Symbol	Address	After Reset
LINCR	0106h	00h

Bit Symbol	Bit Name	Function	RW
SFIE	Synch Field measurement-completed interrupt enable bit	0 : Disables Synch Field measurement-completed interrupt 1 : Enables Synch Field measurement-completed interrupt	RW
SBIE	Synch Break detection interrupt enable bit	0 : Disables Synch Break detection interrupt 1 : Enables Synch Break detection interrupt	RW
BCIE	Bus collision detection interrupt enable bit	0 : Disables bus collision detection interrupt 1 : Enables bus collision detection interrupt	RW
RXDSF	RxD0 input status flag	0 : RXD0 input enabled 1 : RXD0 input disabled	RO
LSTART	Synch Break detection start bit(1)	When this bit is set to 1, Timer RA input is enabled and RXD0 input is disabled. When read, its content is 0.	WO
SBE	RxD0 input unmasking timing select bit (effective in only slave mode)	0 : Unmasked after Synch Break is detected 1 : Unmasked after Synch Field measurement is completed	RW
MST	LIN operation mode setting bit(2)	0 : Slave mode (Synch Break detection circuit actuated) 1 : Master mode (timer RA output OR'ed with TxD0)	RW
LINE	LIN operation start bit	0 : Causes LIN to stop 1 : Causes LIN to start operating(3)	RW

NOTES:
1. After setting the LSTART bit, confirm that the RXDSF flag is set to 1 before Synch Break input starts.
2. Before changing LIN operation modes, temporarily stop the LIN operation (LINE bit = 0).
3. Input to timer RA and UART0 are prohibited immediately after the LINE bit is set to 1(Causes LIN to start operating). Refer to **Figure 17.5 Example of Header Field Transmission Flowchart (1)** and **Figure 17.9 Example of Header Field Reception Flowchart (2)**.

Figure 17.2 LINCR Register

LIN Status Register



Symbol	Address	After Reset
LINST	0107h	00h

Bit Symbol	Bit Name	Function	RW
SFDCT	Synch Field measurement-completed flag	1 shows Synch Field measurement completed.	RO
SBDCT	Synch Break detection flag	1 shows Synch Break detected or Synch Break generation completed	RO
BCDCT	Bus collision detection flag	1 shows Bus collision detected	RO
B0CLR	SFDCT flag clear bit	When this bit is set to 1, SFDCT bit is set to 0. When read, its content is 0.	WO
B1CLR	SBDCT flag clear bit	When this bit is set to 1, SBDCT bit is set to 0. When read, its content is 0.	WO
B2CLR	BCDCT flag clear bit	When this bit is set to 1, BCDCT bit is set to0. When read, its content is 0.	WO
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.3 LINST Register

17.4 Functional Description

17.4.1 Master Mode

Figure 17.4 shows a Typical Operation when Sending a Header Field. Figure 17.5 and Figure 17.6 show an Example of Header Field Transmission Flowchart.
When transmitting a header field, the hardware LIN operates as described below.

(1) When the TSTART bit in the TRACR register for timer RA is set by writing 1 in a program, the hardware LIN outputs a low-level signal from the TXD0 pin for the period that is set in the TRAPRE and TRA registers for timer RA.
(2) When timer RA underflows upon reaching the terminal count, the hardware LIN reverses the output of the TXD0 pin and sets the SBDCT flag in the LINST register to 1. Furthermore, if the SBIE bit in the LINCR register is set to 1, it generates a timer RA interrupt.
(3) The hardware LIN transmits 55h via UART0.
(4) The hardware LIN transmits an ID field via UART0 after it finished sending 55h.
(5) The hardware LIN performs communication for a response field after it finished sending the ID field.

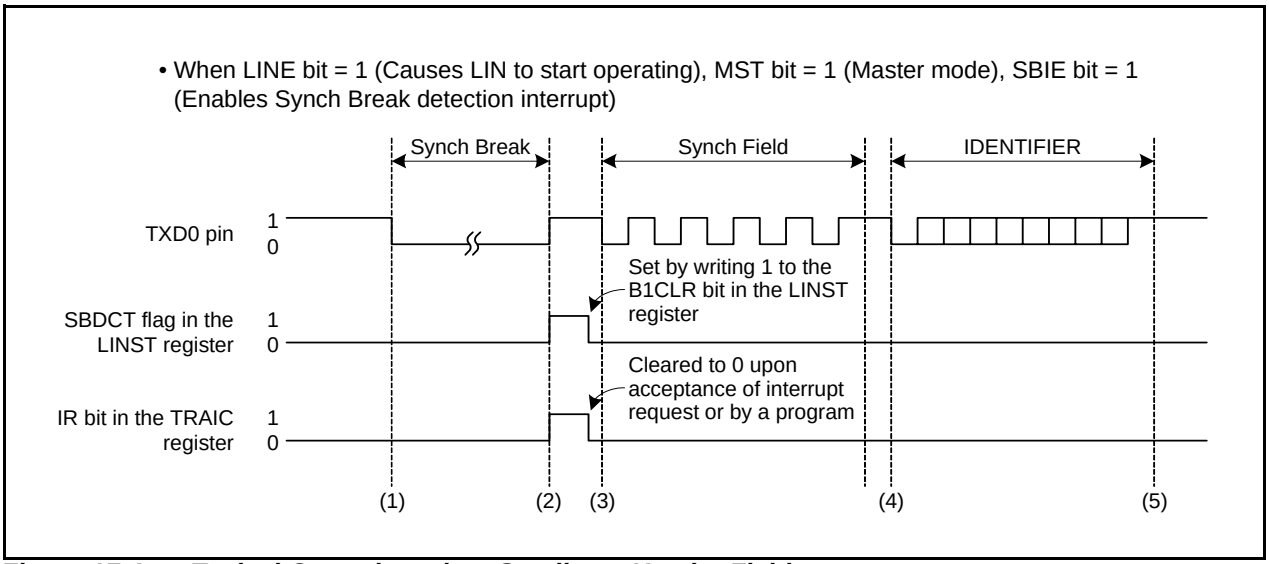


Figure 17.4 Typical Operation when Sending a Header Field

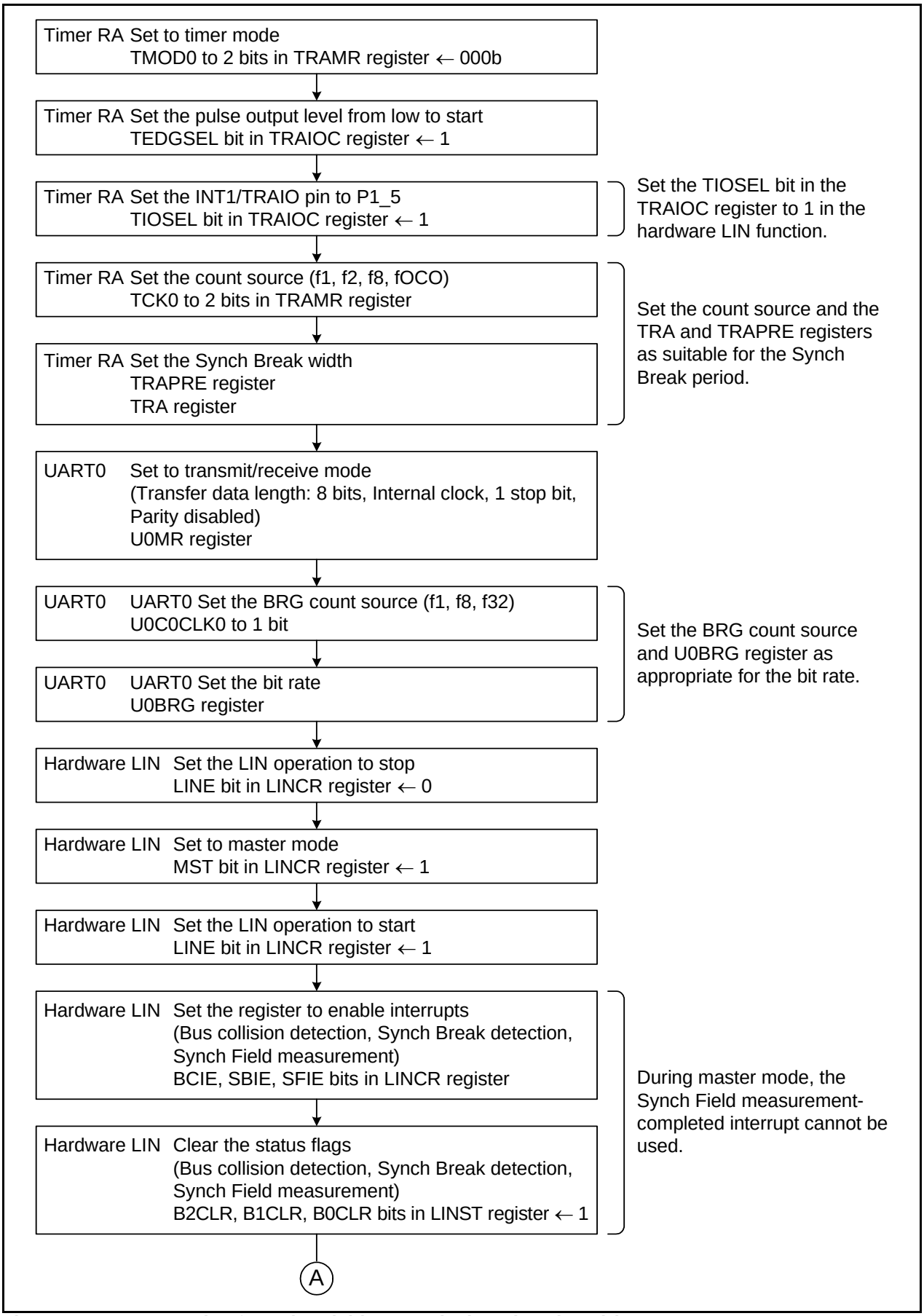


Figure 17.5 Example of Header Field Transmission Flowchart (1)

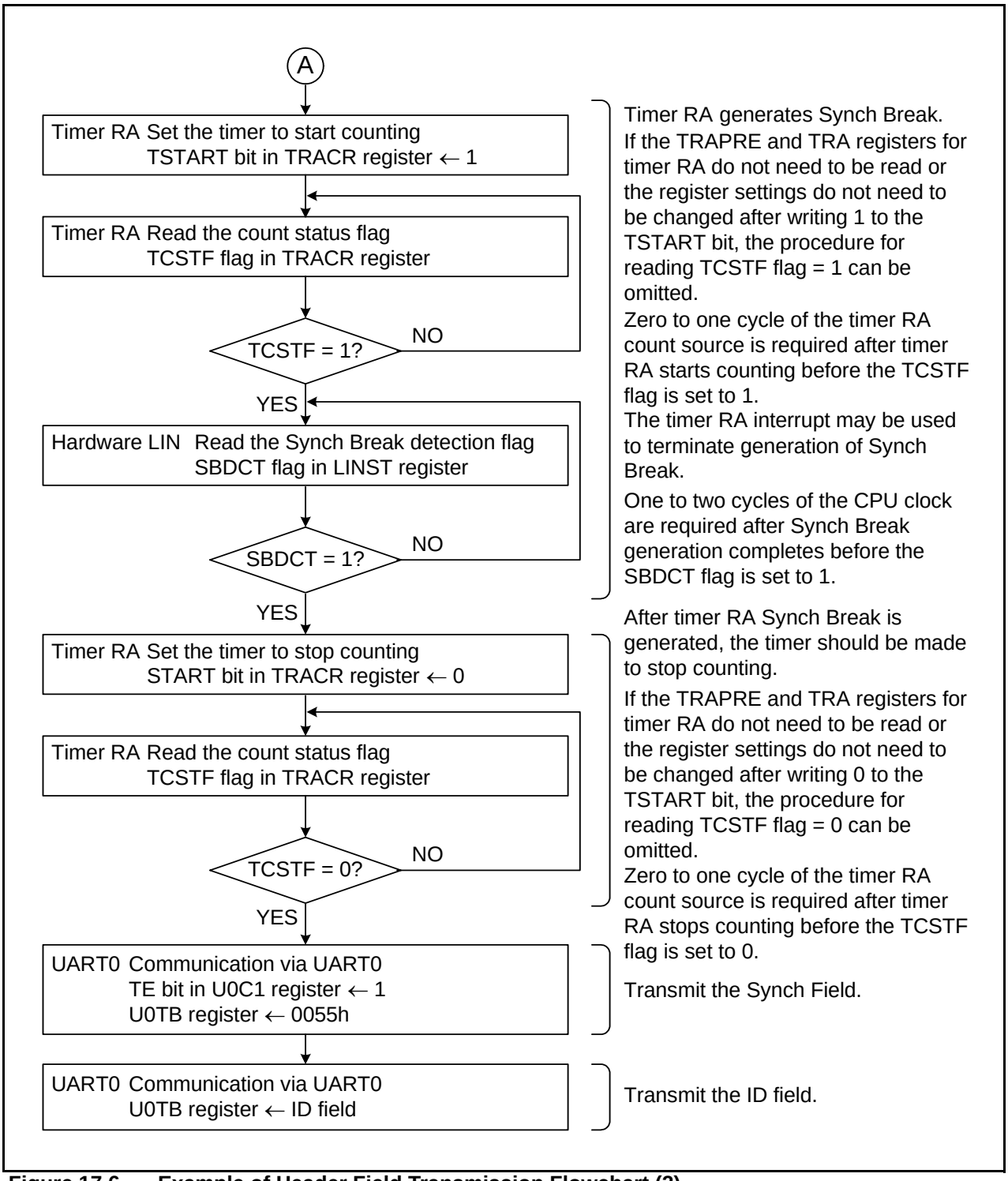


Figure 17.6 Example of Header Field Transmission Flowchart (2)

17.4.2 Slave Mode

Figure 17.7 shows a Typical Operation when Receiving a Header Field. Figure 17.8 through Figure 17.10 show an Example of Header Field Reception Flowchart.
When receiving a header field, the hardware LIN operates as described below.

(1) Synch Break detection is enabled by writing 1 to the LSTART bit in the LINCR register of the hardware LIN.
(2) When a low-level signal is input for a duration equal to or greater than the period set in timer RA, the hardware LIN detects it as Synch Break. At this time, the SBDCT flag in the LINST register is set to 1. Furthermore, if the SBIE bit in the LINCR register is set to 1, the hardware LIN generates a timer RA interrupt. Then it goes to Synch Field measurement.
(3) The hardware LIN receives a Synch Field (55h). At this time, it measures the period of the start bit and bits 0 to 6 by using timer RA. In this case, it is possible to select whether to input the Synch Field signal to RxD0 of UART0 by setting the SBE bit in the LINCR register accordingly.
(4) The hardware LIN sets the SFDCT flag in the LINST register to 1 when it finished measuring the Synch Field. Furthermore, if the SFIE bit in the LINCR register is set to 1, it generates a timer RA interrupt.
(5) After it finished measuring the Synch Field, the hardware LIN calculates a transfer rate from the count value of timer RA and sets the result in UART0 and sets the TRAPRE and TRA registers of the timer RA back again. Then it receives an ID field via UART0.
(6) The hardware LIN performs communication for a response field after it finished receiving the ID field.

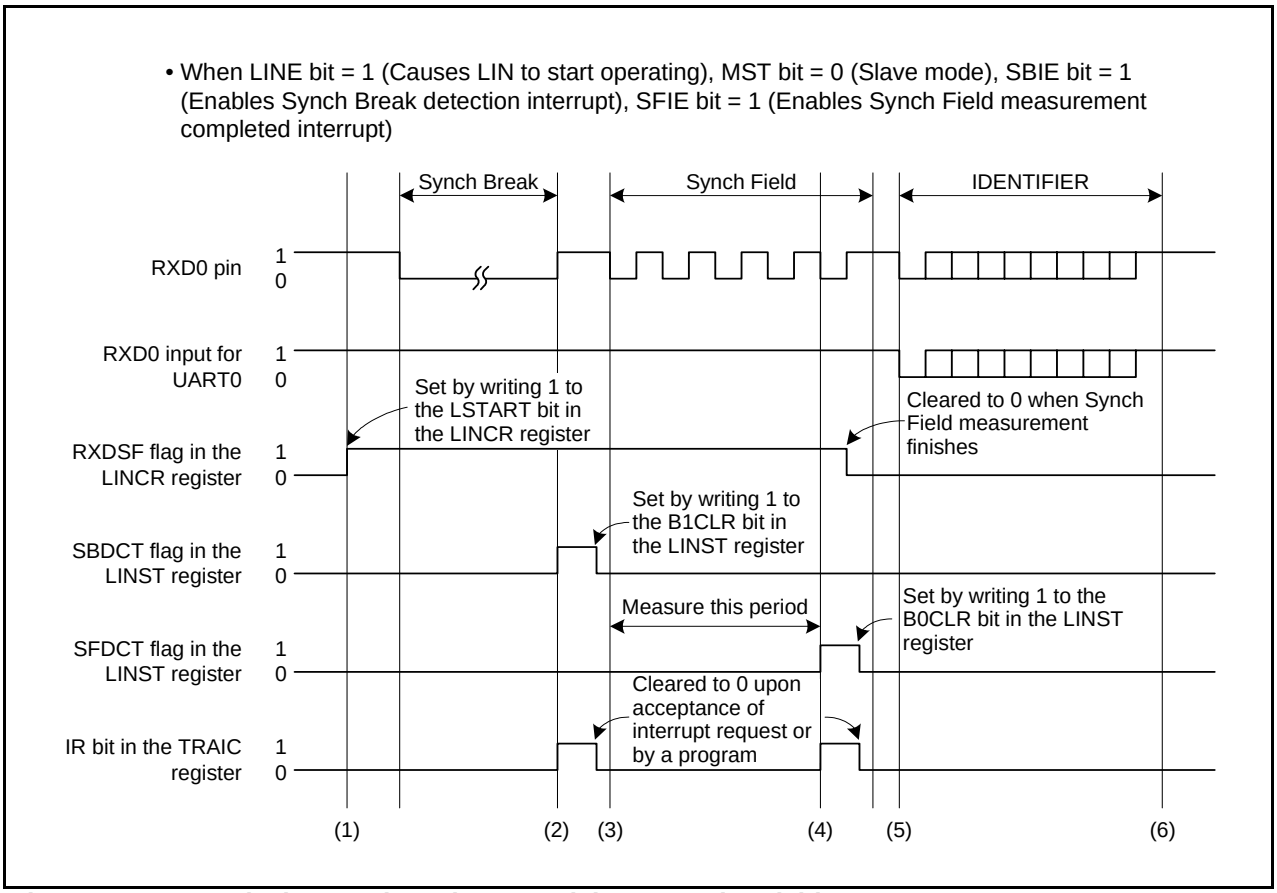


Figure 17.7 Typical Operation when Receiving a Header Field

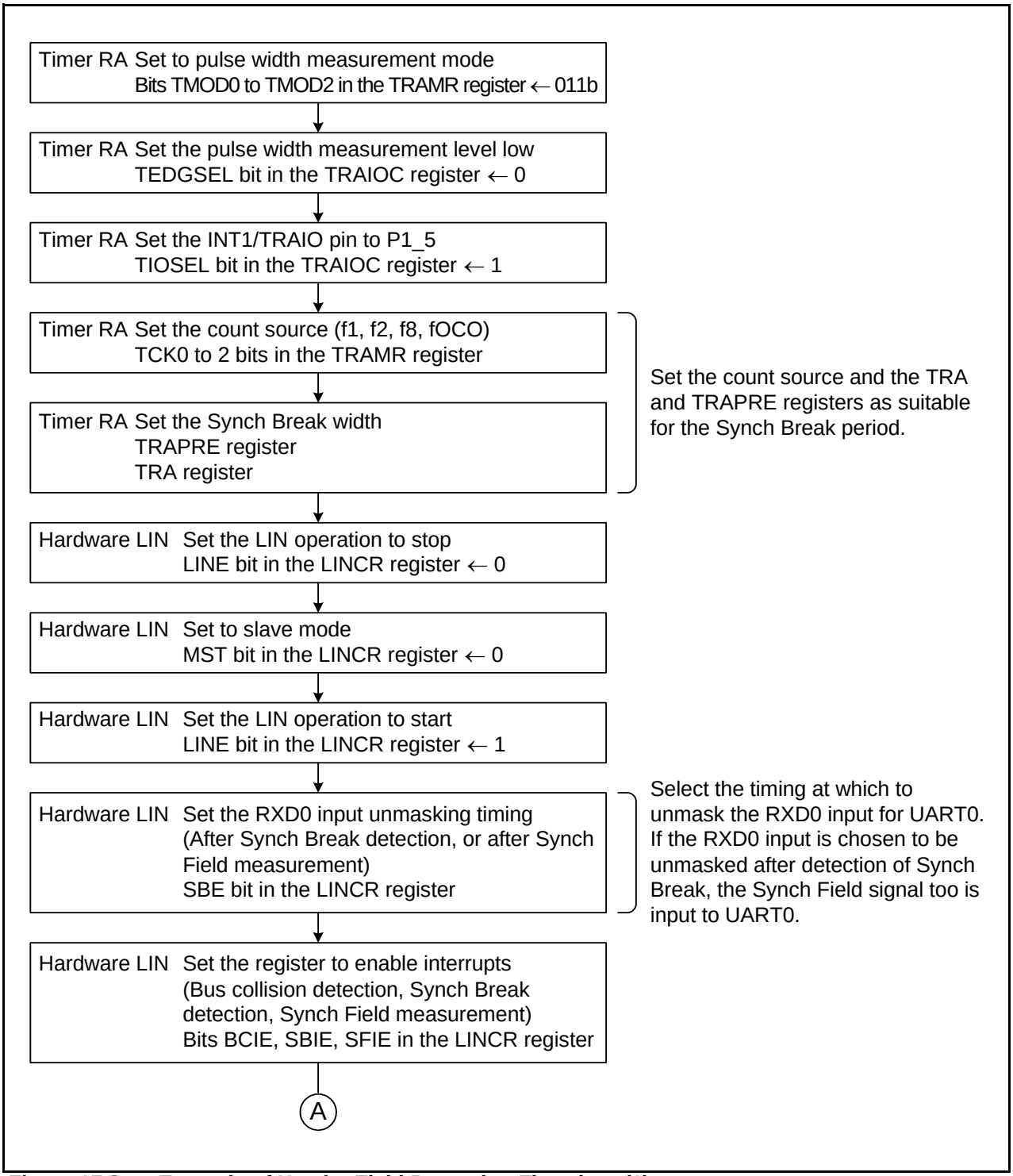


Figure 17.8 Example of Header Field Reception Flowchart (1)

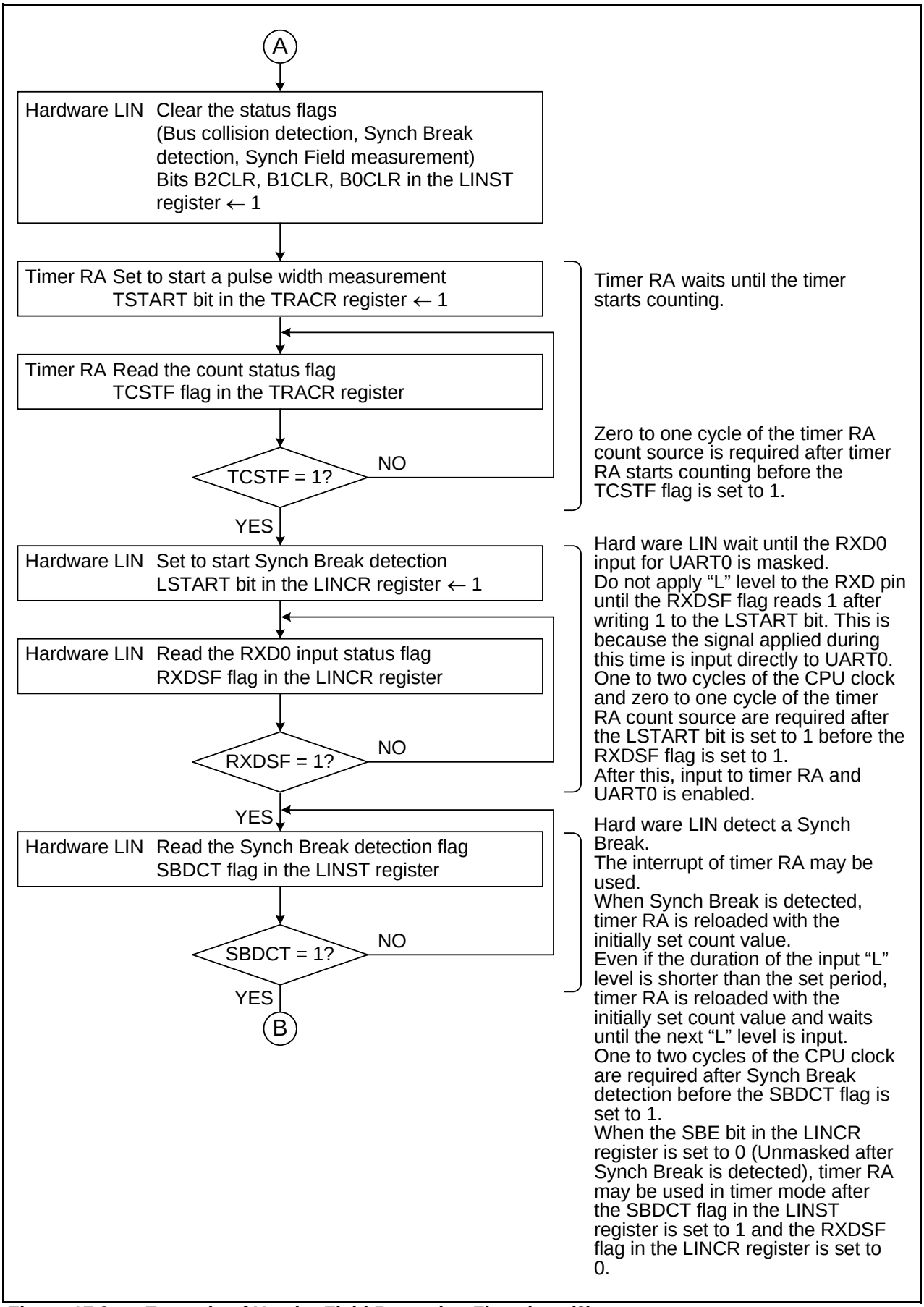


Figure 17.9 Example of Header Field Reception Flowchart (2)

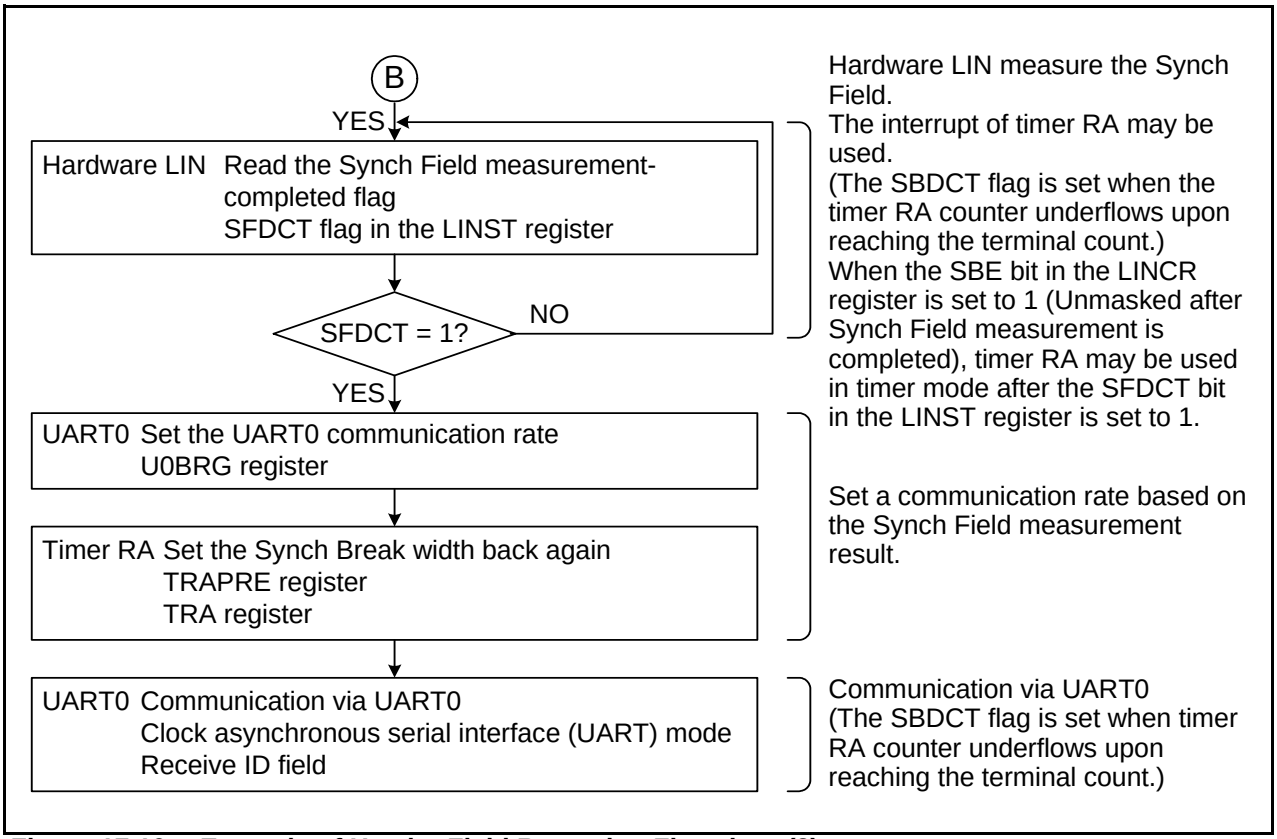


Figure 17.10 Example of Header Field Reception Flowchart (3)

17.4.3 Bus Collision Detection Function

The bus collision detection function can be used when UART0 is enabled for transmission (TE bit in the U0C1 register = 1).
Figure 17.11 shows a Typical Operation when a Bus Collision is Detected.

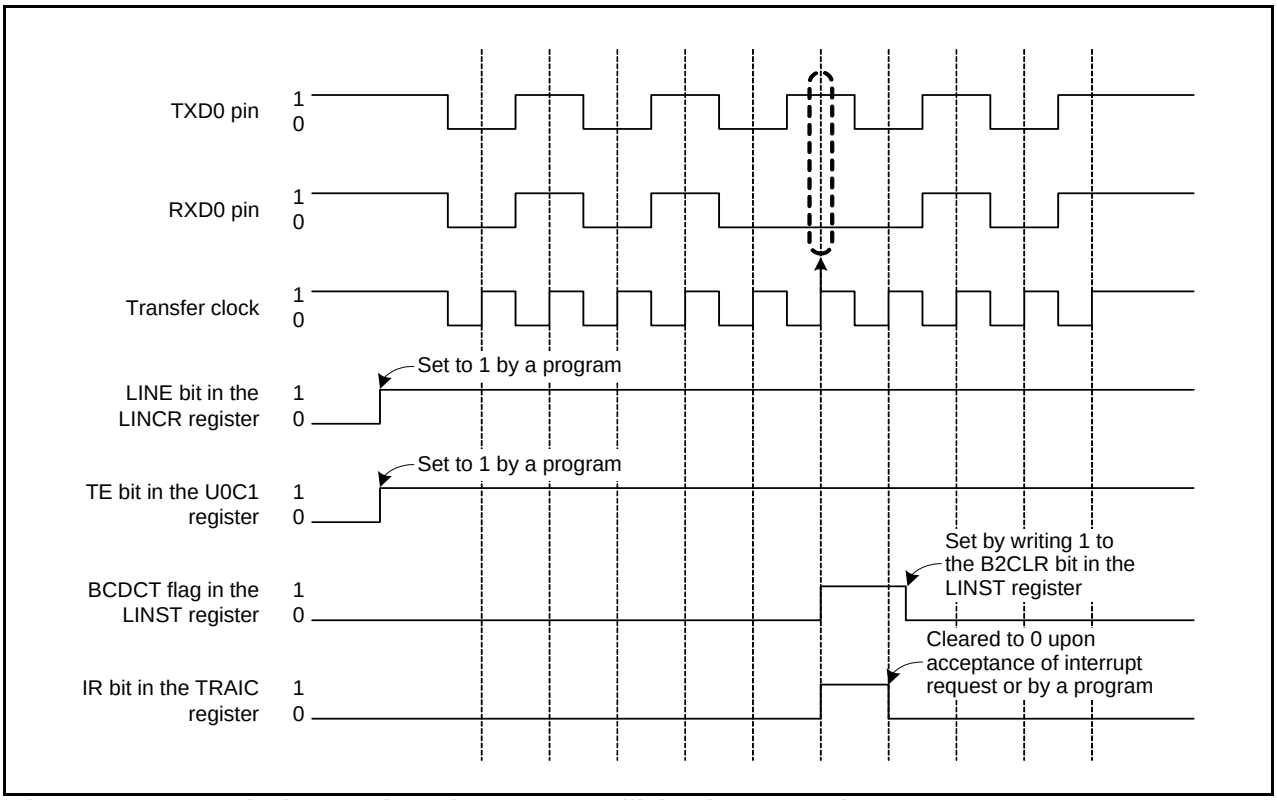


Figure 17.11 Typical Operation when a Bus Collision is Detected

17.4.4 Hardware LIN End Processing

Figure 17.12 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN end processing:

- If the hardware bus collision detection function is used
  Perform hardware LIN end processing after checksum transmission completes.
- If the bus collision detection function is not used
  Perform hardware LIN end processing after header field transmission and reception complete.

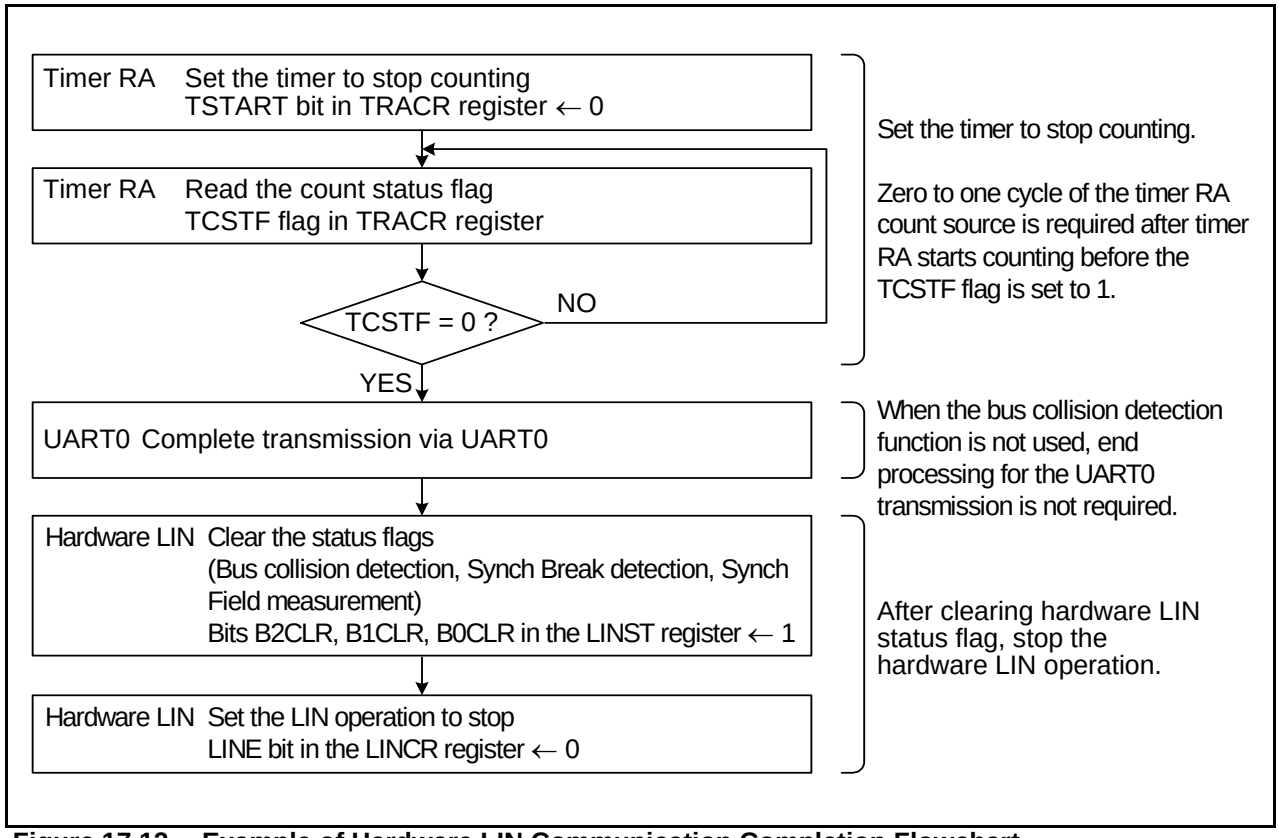


Figure 17.12 Example of Hardware LIN Communication Completion Flowchart

17.5 Interrupt Requests

There are four interrupt requests that are generated by the hardware LIN: Synch Break detection, Synch Break generation completed, Synch Field measurement, and bus collision detection. These interrupts are shared with the timer RA interrupt.
Table 17.2 lists the Interrupt Requests of Hardware LIN.

Table 17.2 Interrupt Requests of Hardware LIN

Interrupt Request	Status Flag	Cause of Interrupt
Synch Break Detection	SBDCT	Generated when timer RA has underflowed after measuring the low level duration of RXD0 input, or when a low-level signal is input for a duration longer than the Synch Break period during communication.
Synch Break Generation Completed		Generated when timer RA has completed outputting a low-level signal to TXD0 for set period.
Synch Field Measurement	SFDCT	Generated when measurement for 8 bits of the Synch Field by timer RA is completed.
Bus Collision Detection	BCDCT	Generated when the RXD0 input and TXD0 output values differed at data latch timing while UART0 is enabled for transmission.

17.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with respect to a Synch Break detection interrupt as the starting point.

18. CAN Module

The CAN (Controller Area Network) module for the R8C/22 Group, R8C/23 Group of MCUs is a communication controller implementing the CAN 2.0B protocol. The R8C/22 Group, R8C/23 Group contains one Full CAN module which can transmit and receive messages in both standard (11-bit) ID and extended (29-bit) ID formats.
Figure 18.1 shows a Block Diagram of CAN Module.
External CAN bus driver and receiver are required.

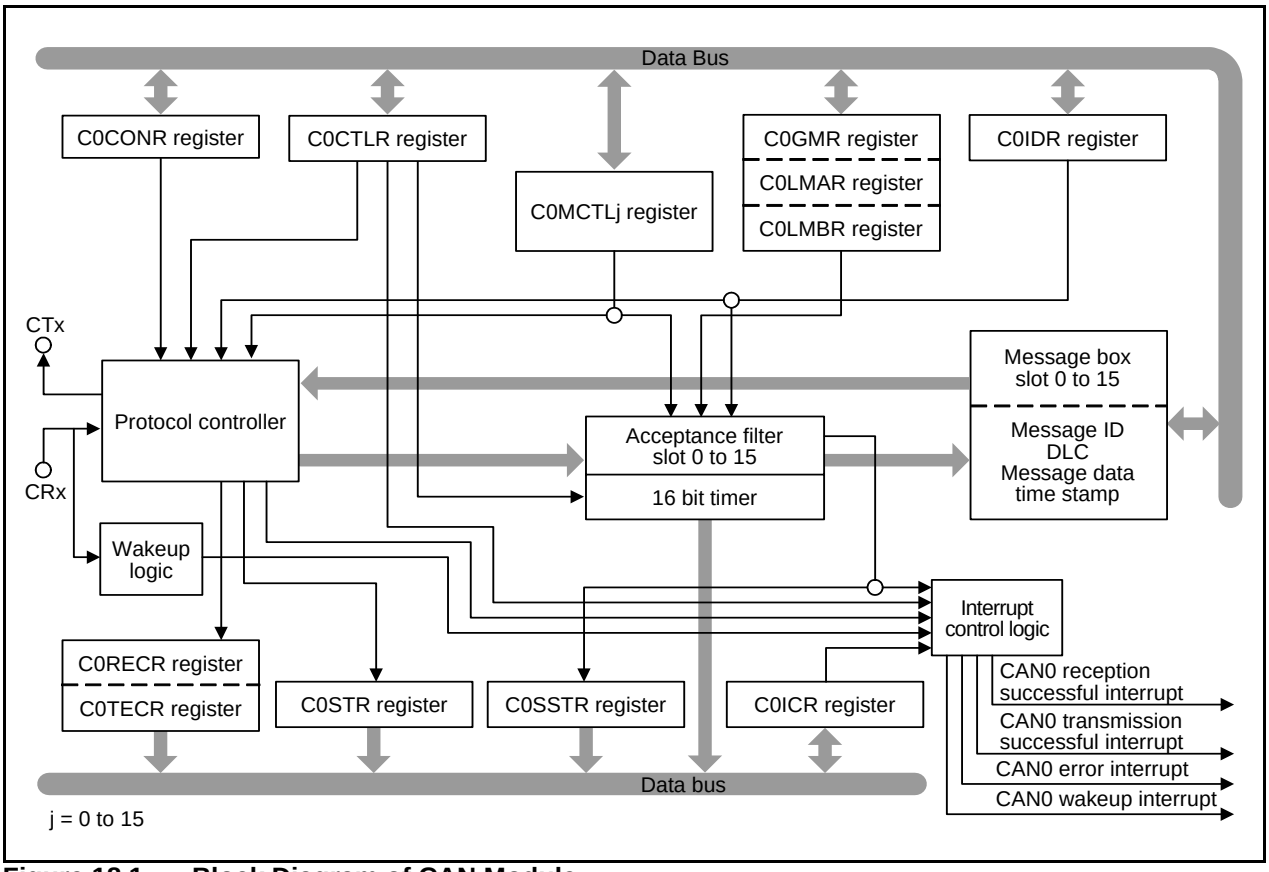


Figure 18.1 Block Diagram of CAN Module

CTx/CRx	:	CAN I/O pins.
Protocol controller	:	This controller handles the bus arbitration and the CAN protocol services, i.e. bit timing, stuffing, error status etc.
Message box	:	This memory block consists of 16 slots that can be configured either as transmitter or receiver. Each slot contains an individual ID, data length code, a data field (8 bytes) and a time stamp.
Acceptance filter	:	This block performs filtering operation for received messages. For the filtering operation, the C0GMR register, the C0LMAR register, or the C0LMBR register is used.
16 bit timer	:	Used for the time stamp function. When the received message is stored in the message memory, the timer value is stored as a time stamp.
Wake up function	:	CAN0 wake up interrupt is generated by a message from the CAN bus.
Interrupt generation function	:	The interrupt events are provided by the CAN module. CAN0 successful reception interrupt, CAN0 successful transmission interrupt, CAN0 error interrupt, and CAN0 wake up interrupt.

18.1 CAN Module-Related Registers

The CAN0 module has the following registers.

(1) CAN Message Box

A CAN module is equipped with 16 slots (16 bytes or 8 words each). Slots 14 and 15 can be used as Basic CAN.

- Priority of the slots: The smaller the number of the slot, the higher the priority, in both transmission and reception.
- A program can define whether a slot is defined as transmitter or receiver.

(2) Acceptance Mask Registers

A CAN module is equipped with 3 masks for the acceptance filter.

- CAN0 global mask register (C0GMR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slots 0 to 13
- CAN0 local mask A register (C0LMAR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slot 14
- CAN0 local mask B register (C0LMBR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slot 15

(3) CAN SFR Registers

- CAN0 message control register i (C0MCTLi register: 8 bits x 16) (i = 0 to 15)
  Control of transmission and reception of a corresponding slot
- CAN0 control register (C0CTLR register: 16 bits)
  Control of the CAN protocol
- CAN0 status register (C0STR register: 16 bits)
  Indication of the protocol status
- CAN0 slot status register (C0SSTR register: 16 bits)
  Indication of the status of contents of each slot
- CAN0 interrupt control register (C0ICR register: 16 bits)
  Selection of interrupt enabled or disabled for each slot
- CAN0 extended ID register (C0IDR register: 16 bits)
  Selection of ID format (standard or extended) for each slot
- CAN0 configuration register (C0CONR register: 16 bits)
  Configuration of the bus timing
- CAN0 receive error count register (C0RECR register: 8 bits)
  Indication of the error status of the CAN module in reception: the counter value is incremented or decremented according to the error occurrence.
- CAN0 transmit error count register (C0TECR register: 8 bits)
  Indication of the error status of the CAN module in transmission: the counter value is incremented or decremented according to the error occurrence.
- CAN0 acceptance filter support register (C0AFS register: 16 bits)
  Decoding the received ID for use by the acceptance filter support unit

Explanation of each register is given below.

18.2 CAN0 Message Box

Table 18.1 shows the Memory Mapping of CAN0 Message Box.
It is possible to access to the message box in byte or word.
Mapping of the message contents differs from byte access to word access. Byte access or word access can be selected by the MsgOrder bit of the C0CTLR register.

Table 18.1 Memory Mapping of CAN0 Message Box

Address	Message Content (Memory Mapping)	
CAN0	Byte access (8 bits)	Word access (16 bits)
1360h + n • 16 + 0	SID10 to SID6	SID5 to SID0
1360h + n • 16 + 1	SID5 to SID0	SID10 to SID6
1360h + n • 16 +2	EID17 to EID14	EID13 to EID6
1360h + n • 16 + 3	EID13 to EID6	EID17 to EID14
1360h + n • 16 + 4	EID5 to EID0	Data Length Code (DLC)
1360h + n • 16 + 5	Data Length Code (DLC)	EID5 to EID0
1360h + n • 16 + 6	Data byte 0	Data byte 1
1360h + n • 16 + 7 ⋮ 1360h + n • 16 + 13	Data byte 1 ⋮ Data byte 7	Data byte 0 ⋮ Data byte 6
1360h + n • 16 + 14	Time stamp high-order byte	Time stamp low-order byte
1360h + n • 16 + 15	Time stamp low-order byte	Time stamp high-order byte

n: Slot number, n = 0 to 15

Figure 18.2 shows the Bit Mapping in Byte Access and Figure 18.3 shows the Bit Mapping in Word Access. The content of each slot remains unchanged unless transmission or reception of a new message is performed.

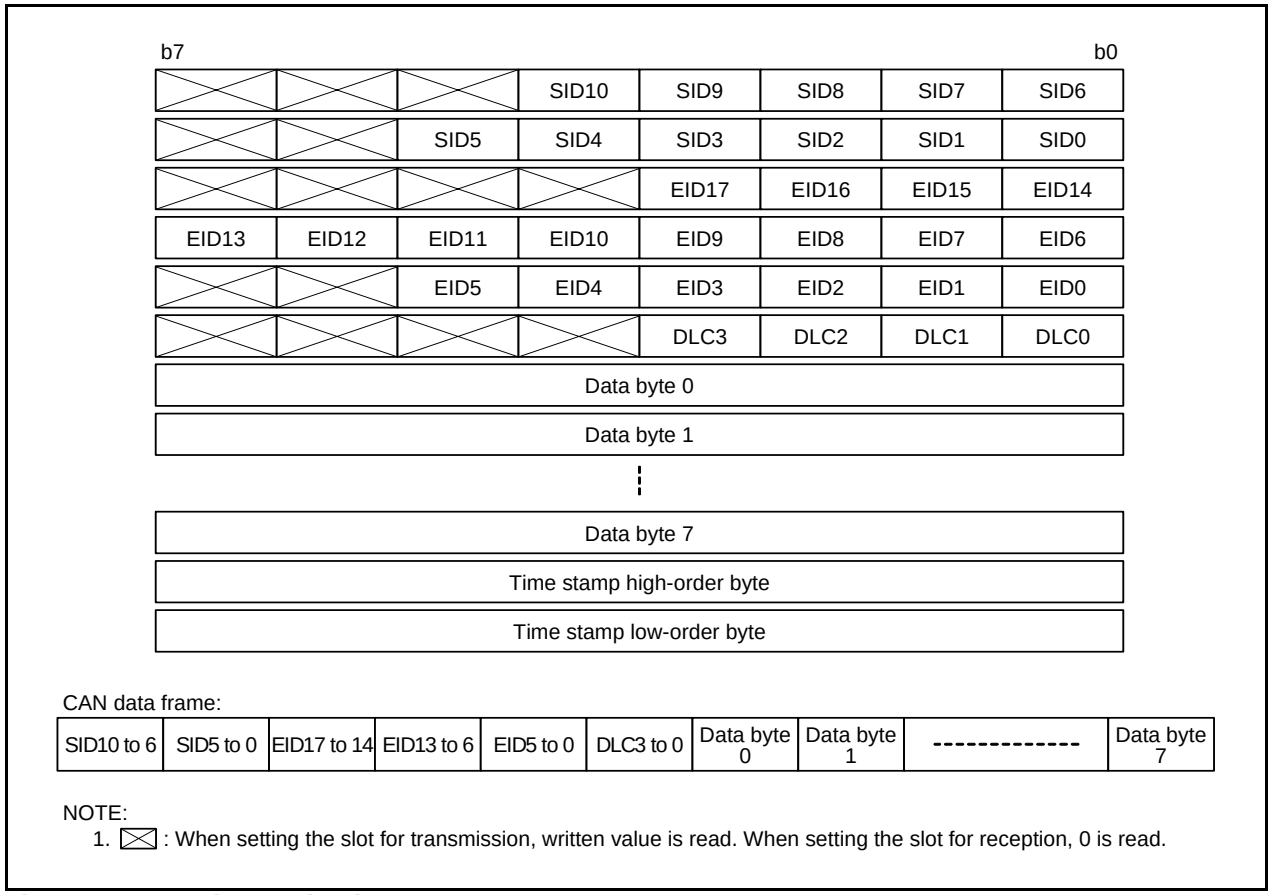


Figure 18.2 Bit Mapping in Byte Access

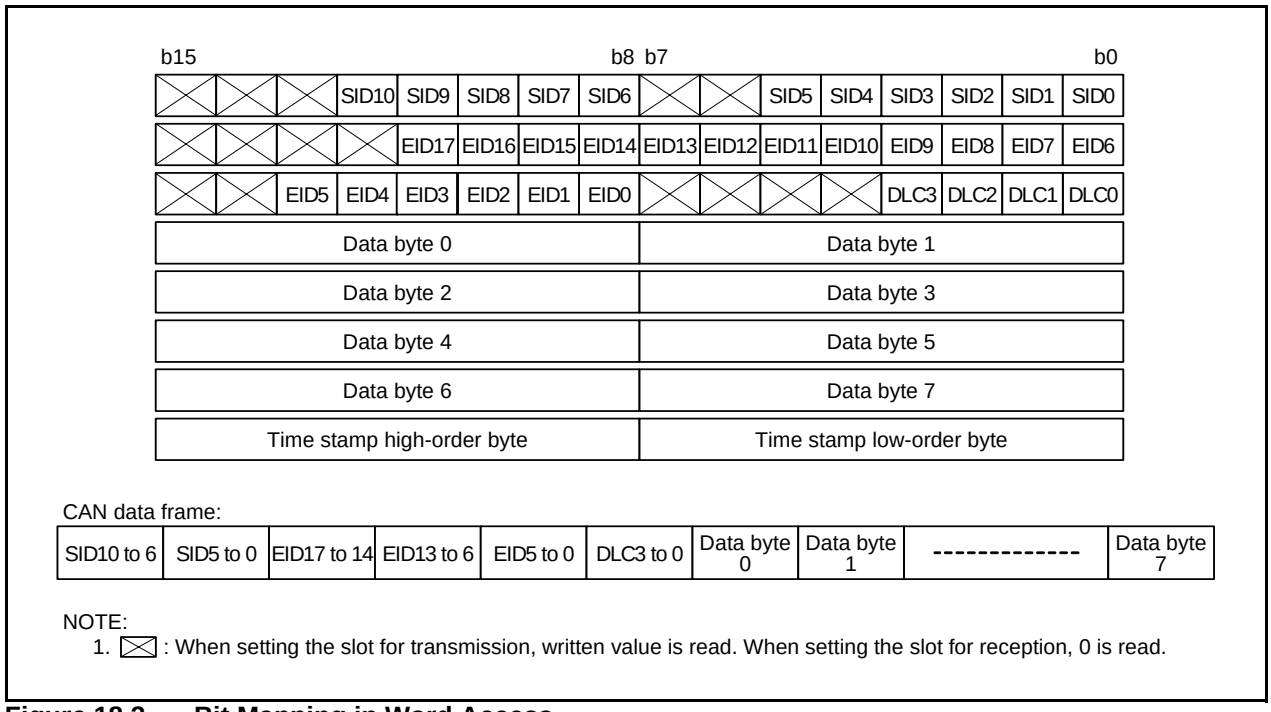


Figure 18.3 Bit Mapping in Word Access

18.3 Acceptance Mask Registers

Figure 18.4 and Figure 18.5 show the C0GMR register, the C0LMAR register, and the C0LMBR register, in which bit mapping in byte access and word access are shown.

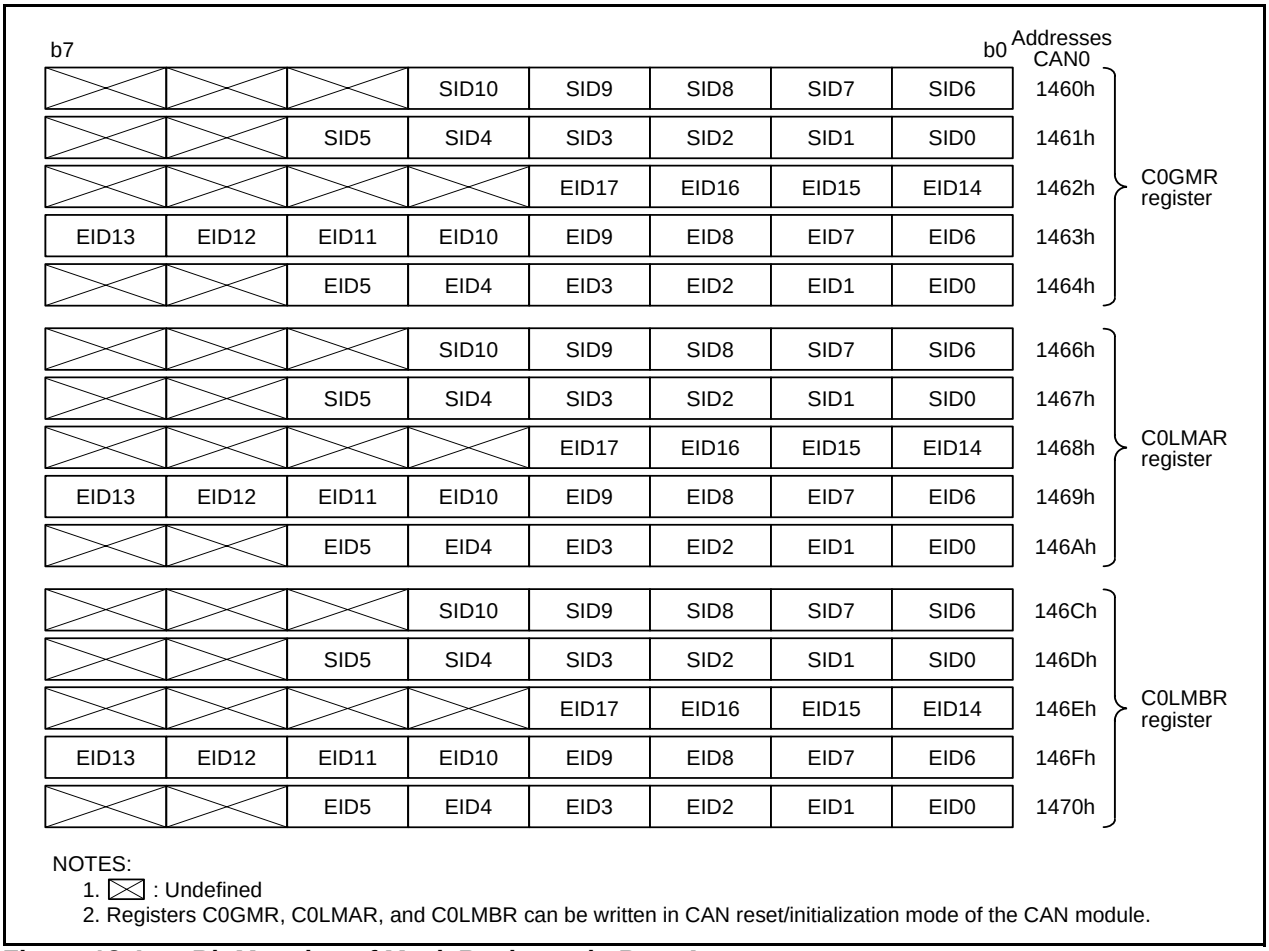


Figure 18.4 Bit Mapping of Mask Registers in Byte Access

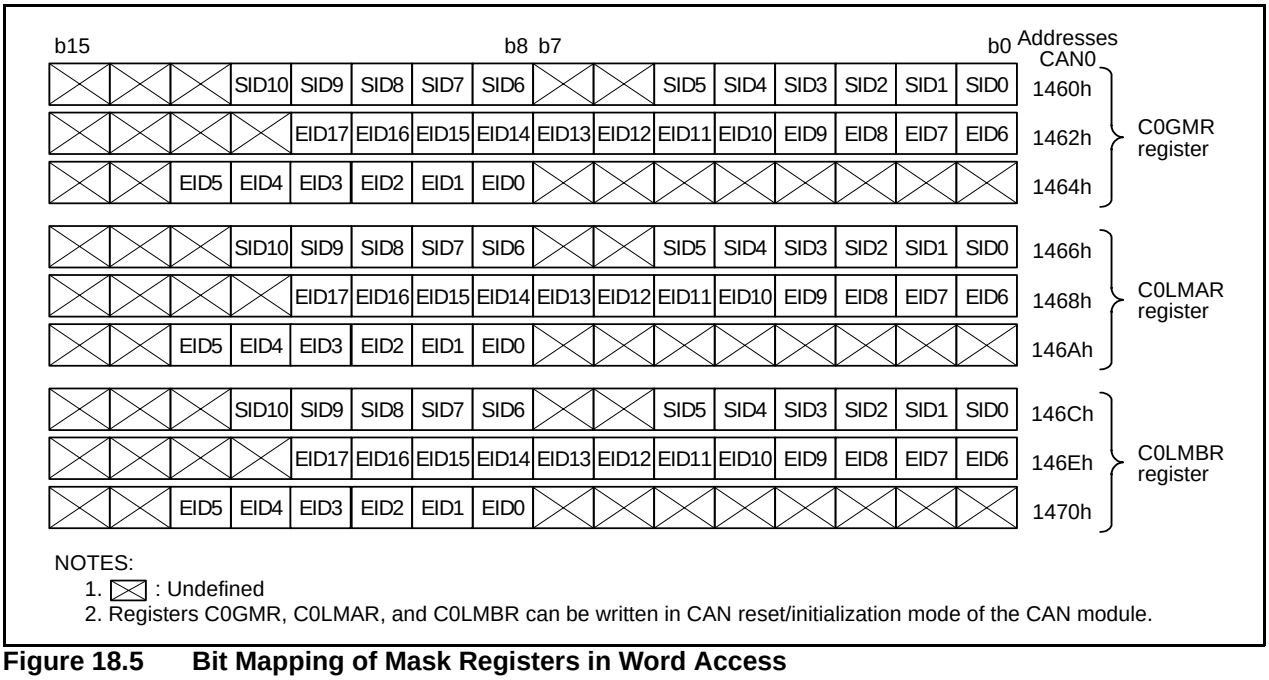


Figure 18.5 Bit Mapping of Mask Registers in Word Access

18.4 CAN SFR Registers

18.4.1 C0MCTLi Register (i = 0 to 15)

Figure 18.6 shows the C0MCTLi Register.

CAN0 Message Control Register i (i = 0 to 15)(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0MCTL0 to C0MCTL15	1300h to 130Fh	00h

Bit Symbol	Bit Name	Function	RW
New Data	Successful reception flag	When set to reception slot 0 : The content of the slot is read or still under processing by the CPU 1 : The CAN module has stored new data in the slot	RO(2)
SentData	Successful transmission flag	When set to transmission slot 0 : Transmission is not started or completed yet 1 : Transmission is successfully completed	RO(2)
InvalData	Under reception flag	When set to reception slot 0 : The message is valid 1 : The message is invalid (The message is being updated)	RO
TrmActive	Under transmission flag	When set to transmission slot 0 : Waiting for bus idle or completion of arbitration 1 : Transmitting	RO
MsgLost	Overwrite flag	When set to reception slot 0 : No message is overwritten 1 : New message is overwritten	RO(2)
RemActive	Remote frame transmission/reception status flag(3)	0 : Data frame transmission/reception status 1 : Remote frame transmission/reception status	RO
RspLock	Auto response lock mode select bit	When set to reception remote frame slot 0 : After a remote frame is received, it will be answered automatically 1 : After a remote frame is received, no transmission will be started as long as this bit is set to 1 (Not responding)	RW
Remote	Remote frame corresponding slot select bit	0 : Slot not corresponding to remote frame 1 : Slot corresponding to remote frame	RW
RecReq	Reception slot request bit(4)	0 : Not reception slot 1 : Reception slot	RW
TrmReq	Transmission slot request bit(4)	0 : Not transmission slot 1 : Transmission slot	RW

NOTES:
1. Set the C0MCTLi register only when the CAN module is in CAN operation mode.
2. When write, set to 0. Each bit is set when the CAN module enters the respective state.
3. In Basic CAN mode, the RemActive bit serves as data format identification flag. When receiving a date frame, the RemActive bit is set to 0 and when receiving a remote frame, the RemActive bit is set to 1.
4. One slot can not be defined as reception slot and transmission slot at the same time.

Figure 18.6 C0MCTLi Register

18.4.2 C0CTLR Register

Figure 18.7 shows the C0CTLR Register.

CAN0 Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0CTLR	1310h	X0000001b

Bit Symbol	Bit Name	Function	RW
Reset	CAN module reset bit(1)	0 : Operation mode 1 : Reset/initialization mode	RW
LoopBack	Loop back mode select bit(2)	0 : Loop back mode disabled 1 : Loop back mode enabled	RW
MsgOrder	Message order select bit(2)	0 : Word access 1 : Byte access	RW
BasicCAN	Basic CAN mode select bit(2)	0 : Basic CAN mode disabled 1 : Basic CAN mode enabled	RW
BusErrEn	Bus error interrupt enable bit(2)	0 : Bus error interrupt disabled 1 : Bus error interrupt enabled	RW
Sleep	Sleep mode select bit(2,3)	0 : Sleep mode disabled 1 : Sleep mode enabled; clock supply stopped	RW
PortEn	CAN port enable bit(2,3)	0 : I/O port function 1 : CTx/CRx function(4)	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.		—

NOTES:
1. When set the Reset bit to 1 (CAN reset/initialization mode), check that the State_Reset bit in the C0STR register is set to 1 (reset mode).
2. Set bits LoopBack, MsgOrder, BasicCAN, BusErrEn, Sleep, and PortEn only when the CAN module is in CAN reset/initialization mode.
3. To use CAN0 wake up interrupt, set bits Sleep and PorEn to 1.
4. Irrespective of setting the PD6 register, P6_1 and P6_2 function as CAN I/O pins.

(b15) (b8)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0CTLR	1311h	XX0X0000b

Bit Symbol	Bit Name	Function	RW
TSPreScale	Time stamp prescaler(1)	b1 b0 0 0 : 1 Period of 1 bit time 0 1 : 1 Period of 1/2 bit time 1 0 : 1 Period of 1/4 bit time 1 1 : 1 Period of 1/8 bit time	RW
TSReset	Time stamp counter reset bit(2)	0 : Nothing is occurred 1 : Forcible reset of time stamp counter	RW
RetBusOff	Return from bus off command bit(3)	0 : Nothing is occurred 1 : Forcible return from bus off	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.		—
RXOnly	Listen-only mode select bit(1)	0 : Listen-only mode disabled 1 : Listen-only mode enabled(4)	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.		—

NOTES:
1. Set bits TSPreScale and RXOnly only when the CAN module is in CAN operation mode.
2. When set the TSReset bit to 1 (forcible reset of time stamp counter), TSReset bit is automatically set to 0 (normal operation mode) after the C0TSR register is set to 0000h.
3. When set the RetBusOff bit to 1 (Fforcible return from bus off), the RetBusOff bit is automatically set to 0 (normal operation mode) after registers C0RECR and C0TECR are set to 0000h.
4. When listen-only mode is selected, do not request a transmission.

Figure 18.7 C0CTLR Register

18.4.3 C0STR Register

Figure 18.8 shows the C0STR Register.

CAN0 Status Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0STR	1312h	00h

Bit Symbol	Bit Name	Function	RW
Mbox	Active slot bits(1)	b3 b2 b1 b0 0 0 0 0 : Slot 0 0 0 0 1 : Slot 1 0 0 1 0 : Slot 2 • • • • 1 1 1 0 : Slot 14 1 1 1 1 : Slot 15	RO
TrmSucc	Successful transmission flag(1)	0 : No [successful] transmission 1 : Transmission successful	RO
RecSucc	Successful reception flag(1)	0 : No [successful] reception 1 : Reception successful	RO
TrmState	Transmission flag (Transmitter)	0 : Idle or receiving 1 : During transmission	RO
RecState	Reception flag (Receiver)	0 : Idle or transmitting 1 : During reception	RO

NOTE:
1. Bits TrmSucc and RecSucc change when the slot enabled the interrupt in the COICR register completed transmitting or receiving.

(b15) (b8)
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0STR	1313h	X0000001b

Bit Symbol	Bit Name	Function	RW
State_Reset	Reset state flag	0 : Operation mode 1 : Reset mode	RO
State_LoopBack	Loop back state flag	0 : No loop back mode 1 : Loop back mode	RO
State_MsgOrder	Message order state flag	0 : Word access 1 : Byte access	RO
State_BasicCAN	Basic CAN mode state flag	0 : No Basic CAN mode 1 : Basic CAN mode	RO
State_BusError	Bus error state flag	0 : No error occurred 1 : CAN bus error occurred	RO
State_ErrPas	Error passive state flag	0 : No error passive state 1 : Error passive state	RO
State_BusOff	Error bus off state flag	0 : No bus off state 1 : Bus off state	RO
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is indeterminate.		—

Figure 18.8 C0STR Register

18.4.4 C0SSTR Register

Figure 18.9 shows the C0SSTR Register.

CAN0 Slot Status Register

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
C0SSTR	1315h, 1314h	0000h

Function	Setting values	RW
Slot status bits Each bit corresponds to the slot with the same number.	0 : Reception slot The message is read Transmission slot Transmission is not completed 1 : Reception slot The message is not read Transmission slot Transmission is completed	RO

Figure 18.9 C0SSTR Register

18.4.5 C0ICR Register

Figure 18.10 shows the C0ICR Register.

CAN0 Interrupt Control Register(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
C0ICR	1317h, 1316h	0000h

Function	Setting values	RW
Interrupt enable bits: Each bit corresponds to the slot of the same number as the bit number. Enabled/disabled successful transmission or reception interrupt can be selected.	0 : Interrupt disabled 1 : Interrupt enabled	RW

NOTE:
1. Set the C0ICR register only when the CAN module is in CAN operation mode.

Figure 18.10 C0ICR Register

18.4.6 C0IDR Register

Figure 18.11 shows the C0IDR Register.

CAN0 Extended ID Register(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
C0IDR	1319h, 1318h	0000h

Function	Setting values	RW
Extended ID bits: Each bit corresponds to the slot of the same number as the bit number. ID format which each slot handles can be selected.	0 : Standard ID 1 : Extended ID	RW

NOTE:
1. Set the C0IDR register only when the CAN module is in CAN operation mode.

Figure 18.11 C0IDR Register

18.4.7 C0CONR Register

Figure 18.12 shows the C0CONR Register.

CAN0 Configuration Register(2)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0CONR	131Ah	Indeterminate

Bit Symbol	Bit Name	Function	RW
BRP	Prescaler division ratio select bits	b3 b2 b1 b0 0 0 0 0 : fCAN divide-by-1(1) 0 0 0 1 : fCAN divide-by-2 0 0 1 0 : fCAN divide-by-3 • • • • 1 1 1 0 : fCAN divide-by-15 1 1 1 1 : fCAN divide-by-16	RW
SAM	Sampling control bit	0 : One time sampling 1 : Three times sampling	RW
PTS	Propagation time segment control bits	b7 b6 b5 0 0 0 : 1Tq 0 0 1 : 2Tq 0 1 0 : 3Tq • • • 1 1 0 : 7Tq 1 1 1 : 8Tq	RW

NOTES:
1. The clock fCAN is used for CAN module. The period is decided by setting the CCLKi bits (i = 0 to 2) in the CCLKR register.
2. Set the C0CONR register only when the CAN module is in CAN operation mode.

(b15) (b8)
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
C0CONR	131Bh	Indeterminate

Bit Symbol	Bit Name	Function	RW
PBS1	Phase buffer segment 1 control bits	b2 b1 b0 0 0 0 : Do not set 0 0 1 : 2Tq 0 1 0 : 3Tq • • • 1 1 0 : 7Tq 1 1 1 : 8Tq	RW
PBS2	Phase buffer segment 2 control bits	b5 b4 b3 0 0 0 : Do not set 0 0 1 : 2Tq 0 1 0 : 3Tq • • • 1 1 0 : 7Tq 1 1 1 : 8Tq	RW
SJW	Re synchronization jump width control bits	b7 b6 0 0 : 1Tq 0 1 : 2Tq 1 0 : 3Tq 1 1 : 4Tq	RW

Figure 18.12 C0CONR Register

18.4.8 C0RECR Register

Figure 18.13 shows the C0RECR Register.

CAN0 Receive Error Count Register

b7 b0

Symbol	Address	After Reset
C0RECR	131Ch	00h

Function	Setting Range	RW
Reception error counting function The value is incremented or decremented according to the CAN module's error status.	00h to FFh(1)	RO

NOTE:
1. The value is indeterminate in bus off state.

Figure 18.13 C0RECR Register

18.4.9 C0TECR Register

Figure 18.14 shows the C0TECR Register.

CAN0 Transmit Error Count Register

b7 b0

Symbol	Address	After Reset
C0TECR	131Dh	00h

Function	Setting Range	RW
Transmission error counting function The value is incremented or decremented according to the CAN module's error status.	00h to FFh(1)	RO

NOTE:
1. The value is indeterminate in bus off state.

Figure 18.14 C0TECR Register

18.4.10 C0AFS Register

Figure 18.15 shows the C0AFS Register.

CAN0 Acceptance Filter Support Register

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After reset
C0AFS	1343h, 1342h	Indeterminate

Function	Setting values	RW
When write, set the standard ID of received message. When read, its content is the converted value of the standard ID.	Standard ID	RW

Figure 18.15 C0AFS Register

18.5 Operational Modes

The CAN module contains the following four operational modes.

- CAN Reset/Initialization Mode
- CAN Sleep Mode
- CAN Operation Mode
- CAN Interface Sleep Mode

Figure 18.16 shows Transition between Operational Modes.

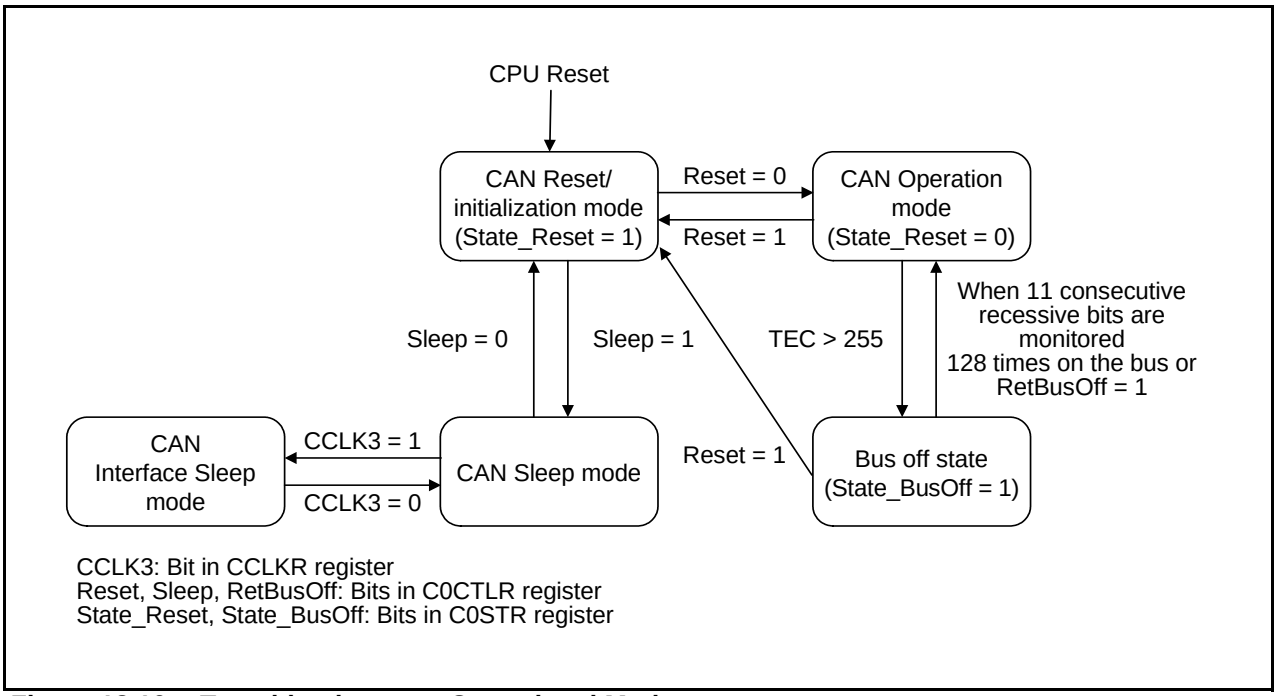


Figure 18.16 Transition between Operational Modes

18.5.1 CAN Reset/Initialization Mode

The CAN module can enter CAN reset/initialization mode by CPU reset or setting the Reset bit in the C0CTLR register. When setting the Reset bit to 1, check that the State_Reset bit in the C0STR register is set to 1 during CAN reset/initialization mode. The CAN module performs the following functions:

- CAN communication is impossible.
- If the CAN module is set to CAN reset/initialization mode during transmitting a message, it is held CAN operation mode until the transmission is completed, it loses in arbitration or an error in it is detected and it enters CAN reset/initialization mode after the State_Reset bit in the C0STR register is set to 0.
- The C0IDR, C0MCTLi (i = 0 to 15), C0ICR, C0STR, C0RECR and C0TECR registers are initialized. All these registers are locked to prevent CPU modification.
- The C0CTLR, C0CONR, C0GMR, C0LMAR and C0LMBR registers and the CAN0 message box retain their contents and are available for CPU access.

18.5.2 CAN Operation Mode

The CAN module can enter CAN operation mode when the Reset bit in the C0CTLR register is set to 0. When set the Reset bit to 0, check that the State_Reset bit in the C0STR register is set to 0. The CAN module performs the following functions after 11 consecutive bits are detected in CAN operation mode.

- The module can transmit and receive a message.
- The module controls the error status by counting transmission and reception errors. CAN communication depends on the error status.

The module is placed in one of three sub modes in CAN operation mode.

- Idle mode: Every nodes do nothing.
- Receive mode: The node can receive a message transmitted by another node.
- Transmit mode: The node can transmit a message. The node can receive own transmitting message simultaneously when the LoopBack bit in the C0CTLR register is set to 1 (Loop back mode).

Figure 18.17 shows Sub Modes in CAN Operation Mode.

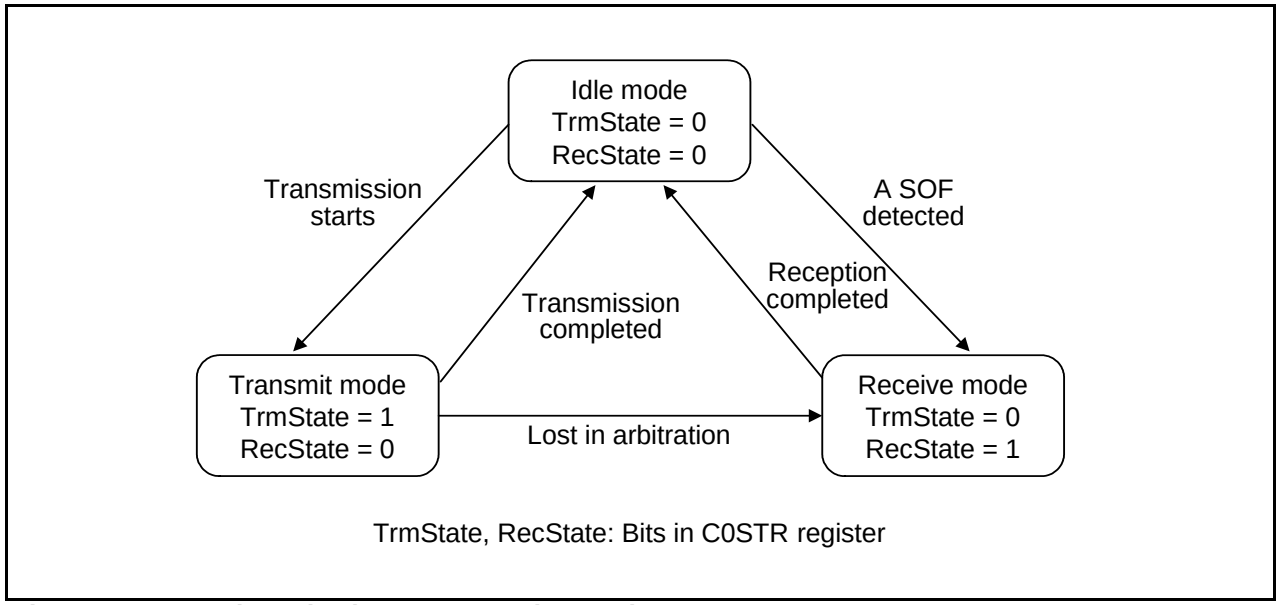


Figure 18.17 Sub Modes in CAN Operation Mode

18.5.3 CAN Sleep Mode

The CAN module can enter CAN sleep mode when the Sleep bit in the C0CTLR register is set to 1. Enter CAN sleep mode via CAN reset/initialization mode.

The power consumption can be reduced because the clock is not provided to the CAN module in CAN sleep mode.

18.5.4 CAN Interface Sleep Mode

The CAN module can enter CAN interface sleep mode when the CCLKR3 bit in the CCLKR register is set to 1. Enter CAN interface sleep mode via CAN sleep mode.

The power consumption can be reduced because the clock is not provided to CPU interface in the CAN module when entering CAN interface sleep mode.

18.5.5 Bus-Off State

When repeating communication error, the CAN module enters a bus-off state according to the fault confinement rule of CAN specification and cannot perform CAN communication. The CAN module can return to CAN operation mode from a bus-off state in the following conditions. At this time, the value of all CAN-associated registers except the C0STR, C0RECR and C0TECR registers are not changed.

(1) When 11 consecutive recessive bits are monitored 128 times
The module enters instantly in an error-active state and performs CAN communication.

(2) When the RetBus Off bit in the C0CTLR register = 1 (forcible return form bus off)
The module enters instantly in an error-active state and performs CAN communication again after 11 consecutive recessive bits are detected.

18.6 Configuration of the CAN Module System Clock

The R8C/22 Group, R8C/23 Group contain a CAN module system clock selectable circuit. The CAN module system clock can be selected by setting the CCLKR register and the BRP bit in the C0CINR register.
For the CCLKR register, refer to **10. Clock Generation Circuit**.
Figure 18.18 shows a Block Diagram of CAN Module System Clock Generation Circuit.

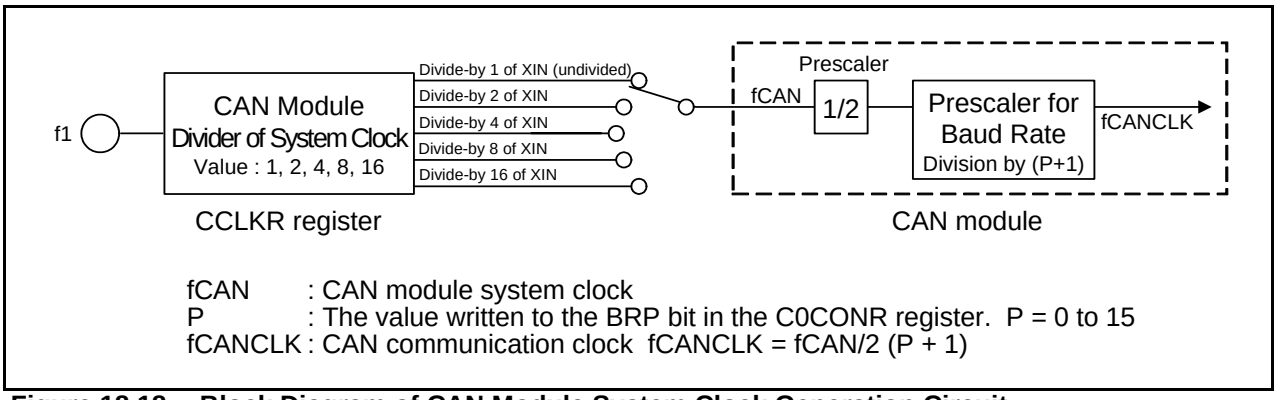


Figure 18.18 Block Diagram of CAN Module System Clock Generation Circuit

18.6.1 Bit Timing Configuration

The bit time consists of the following four segments:

- Synchronization segment (SS)
  This serves for monitoring a falling edge for synchronization.
- Propagation time segment (PTS)
  This segment absorbs physical delay on the CAN network which amounts to double the total sum of delay on the CAN bus, the input comparator delay, and the output driver delay.
- Phase buffer segment 1 (PBS1)
  This serves for compensating the phase error. When the falling edge of the bit falls later than expected, the segment can become longer by the maximum of the value defined in SJW.
- Phase buffer segment 2 (PBS2)
  This segment has the same function as the phase buffer segment 1. When the falling edge of the bit falls earlier than expected, the segment can become shorter by the maximum of the value defined in SJW.

Figure 18.19 shows the Bit Timing.

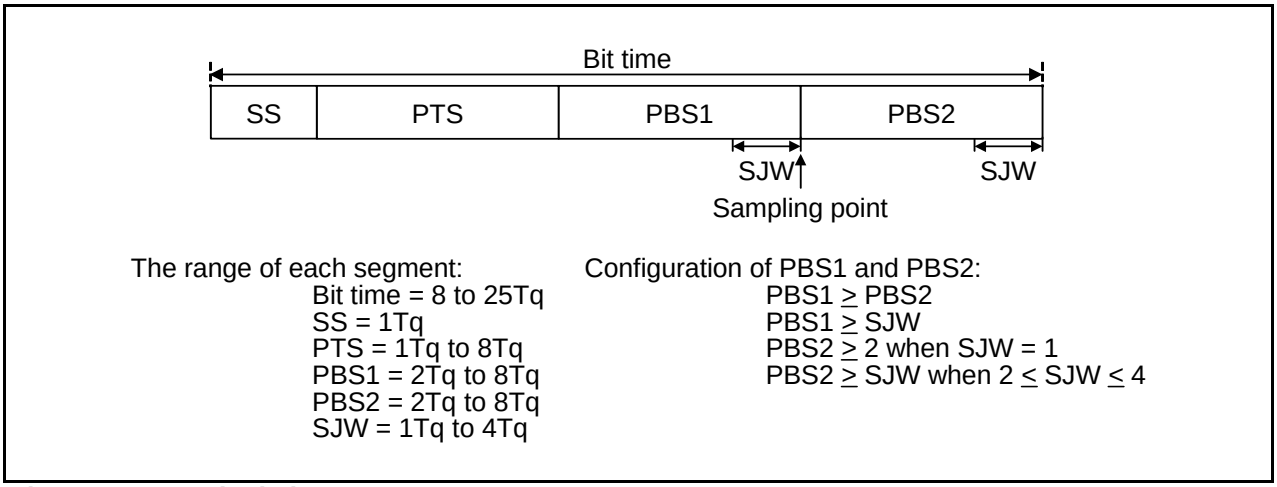


Figure 18.19 Bit Timing

18.6.2 Baud Rate

Baud rate depends on system clock, the division value of the CAN module system clock, the division value of the baud rate prescaler, and the number of Tq's in one bit.
Table 18.2 shows the Examples of Baud Rate.

Table 18.2 Examples of Baud Rate

Baud Rate	20 MHz	16 MHz	10 MHz	8 MHz
1 Mbps	10Tq (1)	8Tq (1)	–	–
500 kbps	10Tq (2) 20Tq (1)	8Tq (2) 16Tq (1)	10Tq (1) –	8Tq (1) –
125 kbps	8Tq (10) 10Tq (8) 16Tq (5) 20Tq (4)	8Tq (8) 16Tq (4) –	8Tq (5) 10Tq (4) 20Tq (2) –	8Tq (4) 16Tq (2) –
83.3 kbps	8Tq (15) 10Tq (12) 20Tq (6)	8Tq (12) 16Tq (6) –	10Tq (6) 20Tq (3) –	8Tq (6) 16Tq (3) –
33.3 kbps	10Tq (30) 20Tq (15) –	8Tq (30) 10Tq (24) 16Tq (15) 20Tq (12)	10Tq (15) –	8Tq (15) 10Tq (12) 20Tq (6) –

NOTE:
1. The number in ( ) indicates a value of fCAN division value multiplied by division value of the baud rate prescaler.

Calculation of Baud Rate

$$\frac{\text{XIN}}{2 \times \text{fCAN division value}^{(1)} \times \text{division value of baud rate prescaler}^{(2)} \times \text{number of Tq's in one bit}}$$

NOTES:
1. fCAN division value = 1, 2, 4, 8, 16
   fCAN division value: a value selected in the CCLKR register
2. Division value of prescaler for baud rate = P + 1 (P: 0 to 15)
   P: a value selected by the BRP bit in the C0CONR register

18.7 Acceptance Filtering Function and Masking Function

These functions serve the users to select and receive a facultative message. The C0GMR, C0LMAR, and C0LMBR registers can perform masking to the standard or extended ID. The C0GMR register corresponds to slots 0 to 13, the C0LMAR register corresponds to slot 14, and the C0LMBR register corresponds to slot 15. When acceptance filtering, the masking function is valid to a received 11 or 29 bit ID by the value set to the slot in the C0IDR register. This function is used for receiving a certain range of IDs.
Figure 18.20 shows Correspondence of Mask Registers to Slots and Figure 18.21 shows the Acceptance Function.

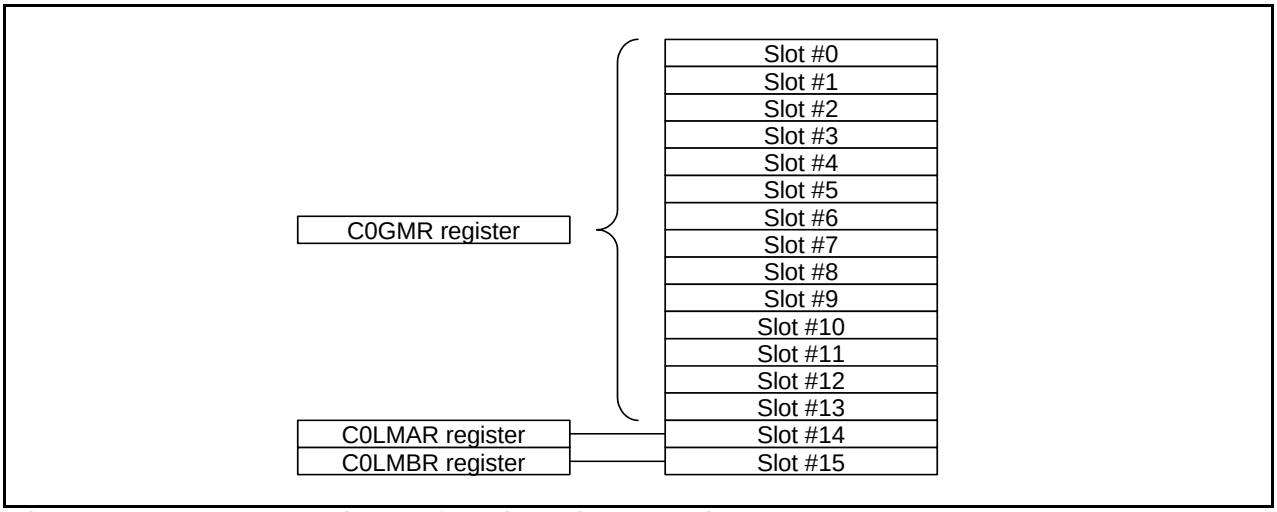


Figure 18.20 Correspondence of Mask Registers to Slots

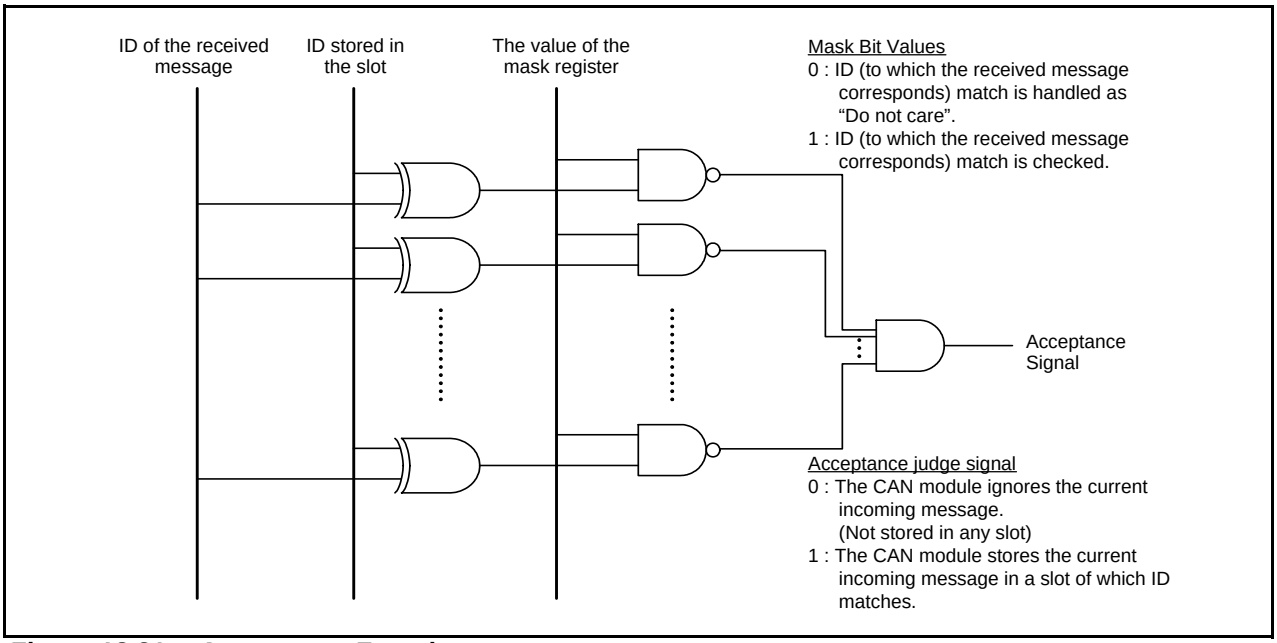


Figure 18.21 Acceptance Function

When using the acceptance function, note the following points.

(1) If two or more slots are set the same ID and received a same message, the smallest slot number is valid.
(2) If slots 14 and 15 are set to receive all IDs in Basic mode, slots 14 and 15 can receive IDs which are not received by slots 0 to 13.

18.8 Acceptance Filter Support Unit (ASU)

The ASU is a function to determine whether the receive ID is valid or not by means of a table search. To use this function, first register the ID to receive in the data table. Next, store the received ID in the C0AFS register, read out the decoded received ID from the C0AFS register and check it by searching the table. The ASU can only be used for the IDs of standard frames.

The ASU will prove effective in the following cases.

- When the IDs to receive cannot be masked by the acceptance filter.
  (Example) IDs to receive: 078h, 087h, 111h
- When there are too many IDs to receive and filtering in software requires an excessive amount of time.

Figure 18.22 shows the Content of C0AFS Register When Written to and Read out (For Word Access).

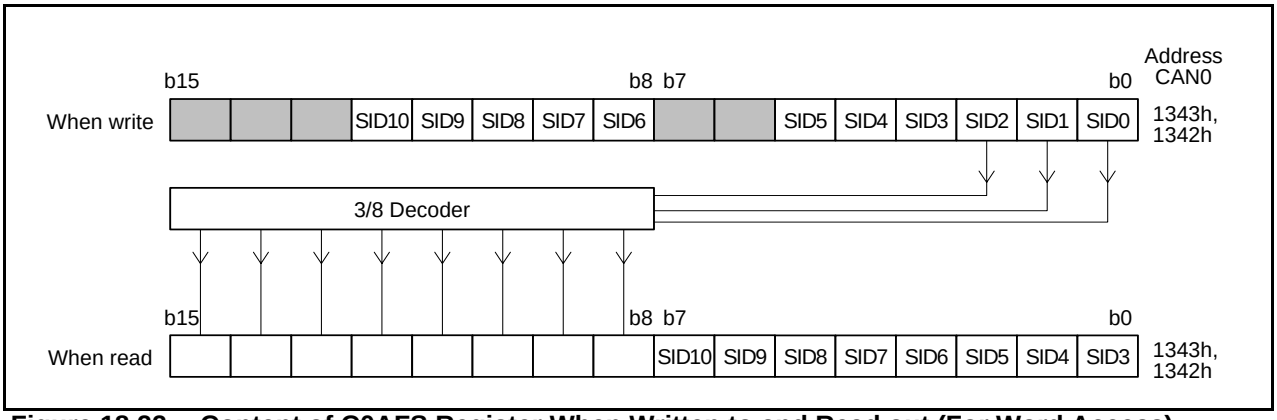


Figure 18.22 Content of C0AFS Register When Written to and Read out (For Word Access)

18.9 Basic CAN Mode

When the BasicCAN bit in the C0CTLR register is set to 1, (Basic CAN mode) slots 14 and 15 correspond to Basic CAN mode. In normal operation mode, each slot can handle only one type message at a time, either a data frame or a remote frame by setting the C0MCTLi register (i = 0 to 15). However, in Basic CAN mode, slots 14 and 15 can receive both types of message at the same time.
When slots 14 and 15 are defined as reception slots in Basic CAN mode, received messages are stored in slots 14 and 15 alternately.
Which type of message has been received can be checked by the RemActive bit in the C0MCTLi register.
Figure 18.23 shows the Operation of Slots 14 and 15 in Basic CAN Mode.

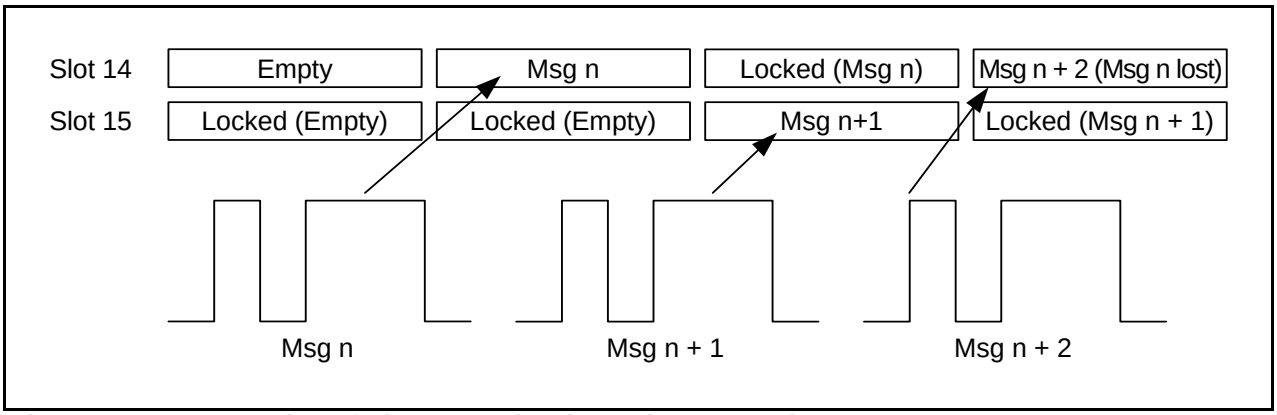


Figure 18.23 Operation of Slots 14 and 15 in Basic CAN Mode

When using Basic CAN mode, note the following points.

(1) Basic CAN mode can only be set in CAN reset/initialization mode.
(2) Slots 14 and 15 must be set the same ID. Also, the C0LMAR and C0LMBR registers for slots 14 and 15 must be set in the same way.
(3) Slots 14 and 15 must be set as reception slot.
(4) No protection against overwritten message. If any slot receives a new message while it is receiving another message, the slot may be overwritten by the new message received.
(5) Slots 0 to 13 operate in normal operation mode.

18.10 Return from Bus off Function

The CAN module can forcibly return from bus off state by setting the RetBusOff bit in the C0CTLR register to 1 (Forcible return from bus off). At the time, an error state in the CAN module transits from a bus-off state to an error-active state. When return from bus-off is executed, the C0TECR and C0RECR registers are initialized and the State_BusOff bit in the C0STR register is set to 0 (No bus off state). However, CAN related registers such as the C0CONR register and contents of slots are not initialized.

18.11 Listen-Only Mode

When the RXOnly bit in the C0CTLR register is set to 1, the CAN module enters listen-only mode.
Listen-only mode is not allowed to transmit any frames such as error and overload frames and acknowledge. When setting the CAN module to Listen-only mode, do not request a transmission.

18.12 Reception and Transmission

Configuration of CAN Reception and Transmission Mode
Table 18.3 shows Configuration of CAN Reception and Transmission Mode.

Table 18.3 Configuration of CAN Reception and Transmission Mode

TrmReq	RecReq	Remote	RspLock	Communication Mode of the Slot
0	0	—	—	Communication environment configuration mode: configure the communication mode of the slot.
0	1	0	0	Configured as a reception slot for a data frame.
1	0	1	0	Configured as a transmission slot for a remote frame. (At this time the RemActive bit is 1.) After completion of transmission, this functions as a reception slot for a data frame. (At this time the RemActive bit is 0.) However, when an ID that matches on the CAN bus is detected before remote frame transmission, this immediately functions as a reception slot for a data frame.
1	0	0	0	Configured as a transmission slot for a data frame.
0	1	1	1/0	Configured as a reception slot for a remote frame. (At this time the RemActive bit is 1.) After completion of reception, this functions as a transmission slot for a data frame. (At this time the RemActive bit is 0.) However, transmission does not start as long as RspLock bit remains 1; thus no automatic remote frame response. Response (transmission) starts when RspLock bit is set to 0.

TrmReq, RecReq, Remote, RspLock, RemActive, RspLock: C0MCTLi register's (i = 0 to 15) bit

When configuring a slot as a reception slot, note the following points.

(1) Before configuring a slot as a reception slot, be sure to set the C0MCTLi registers (i = 0 to 15) to 00h.
(2) A received message is stored in a slot that matches the condition first according to the result of reception mode configuration and acceptance filtering operation. Upon deciding in which slot to store, the smaller the number of the slot is, the higher priority it has.
(3) In normal CAN operation mode, when a CAN module transmits a message of which ID matches, the CAN module never receives the transmitted data. In loop back mode, however, the CAN module receives back the transmitted data. In this case, the module does not return an ACK.

When configuring a slot as a transmission slot, note the following points.

(1) Before configuring a slot as a transmission slot, be sure to set the C0MCTLi registers to 00h.
(2) Set the TrmReq bit to 0 (not transmission slot) before rewriting a transmission slot.
(3) A transmission slot should not be rewritten when the TrmActive bit is 1 (transmitting). If it is rewritten, an indeterminate data will be transmitted.

18.12.1 Reception

Figure 18.24 shows the Timing of Receive Data Frame Sequence. This is an operation example when consecutive messages are received.

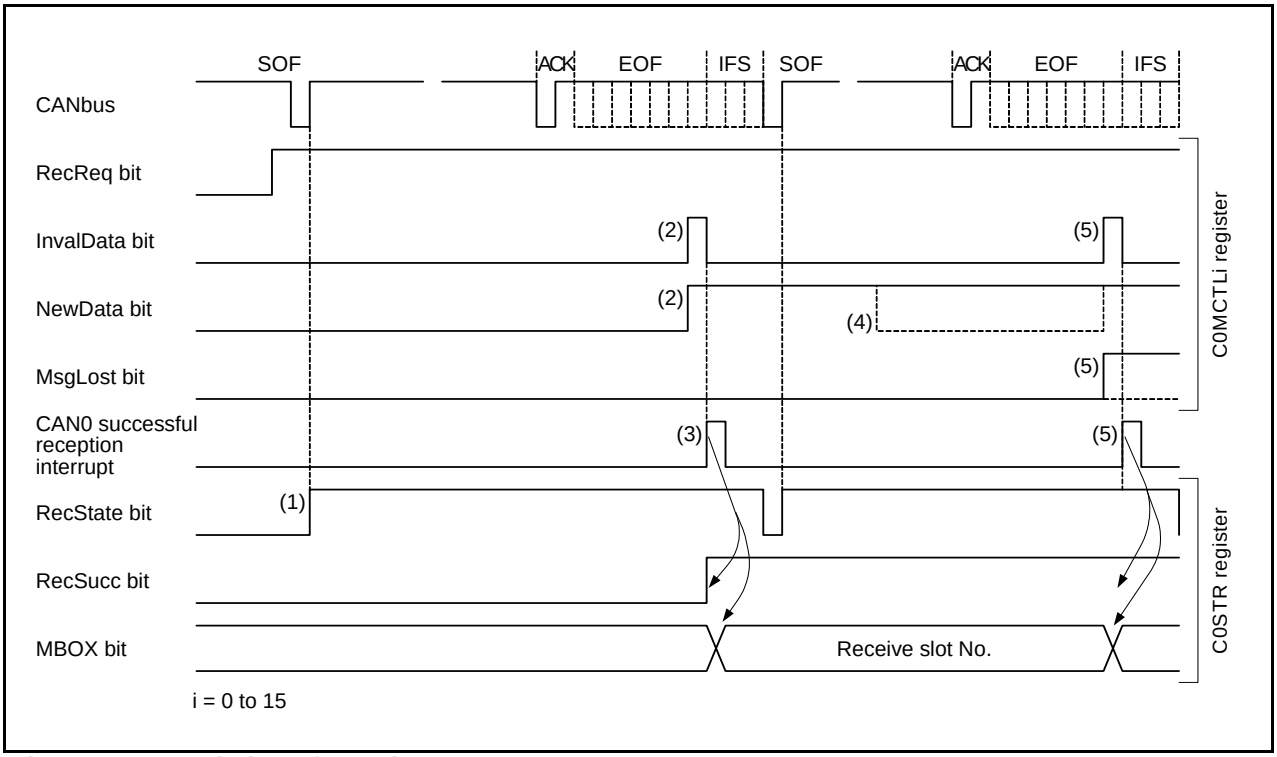


Figure 18.24 Timing of Receive Data Frame Sequence

(1) If a SOF is detected on the CAN bus, the RecState bit in the C0STR register is set to 1 (During reception) immediately and the slot starts receiving a message.

(2) The message successfully is received and the NewData bit in the C0MCTLi register of the reception slot is set to 1 (stored new data in slot). The InvalData bit in the C0MCTLi register is set to 1 (the message is being updated) at the same time and set to 0 (the message is valid) after the message completely is stored to the slot.

(3) If the interrupt enable bit in the C0ICR register of the slot is set to 1 (interrupt enabled), the CAN0 successful reception interrupt request is generated and the MBOX and RecSucc bits in the C0STR register change.

(4) Set the NewData bit to 0 (the content of the slot is read out or still under processing by the CPU) by a program and read the message from the slot.

(5) When next CAN message is received before the NewData bit is set to 0 by a program or a receive request to a slot is canceled, the MsgLost bit in the C0MCTLj register is set to 1 (this slot already contained a message) and new message is stored in a slot. CAN0 successful reception interrupt and the C0STR register change the same as (3).

18.12.2 Transmission

Figure 18.25 shows the Timing of Transmit Sequence.

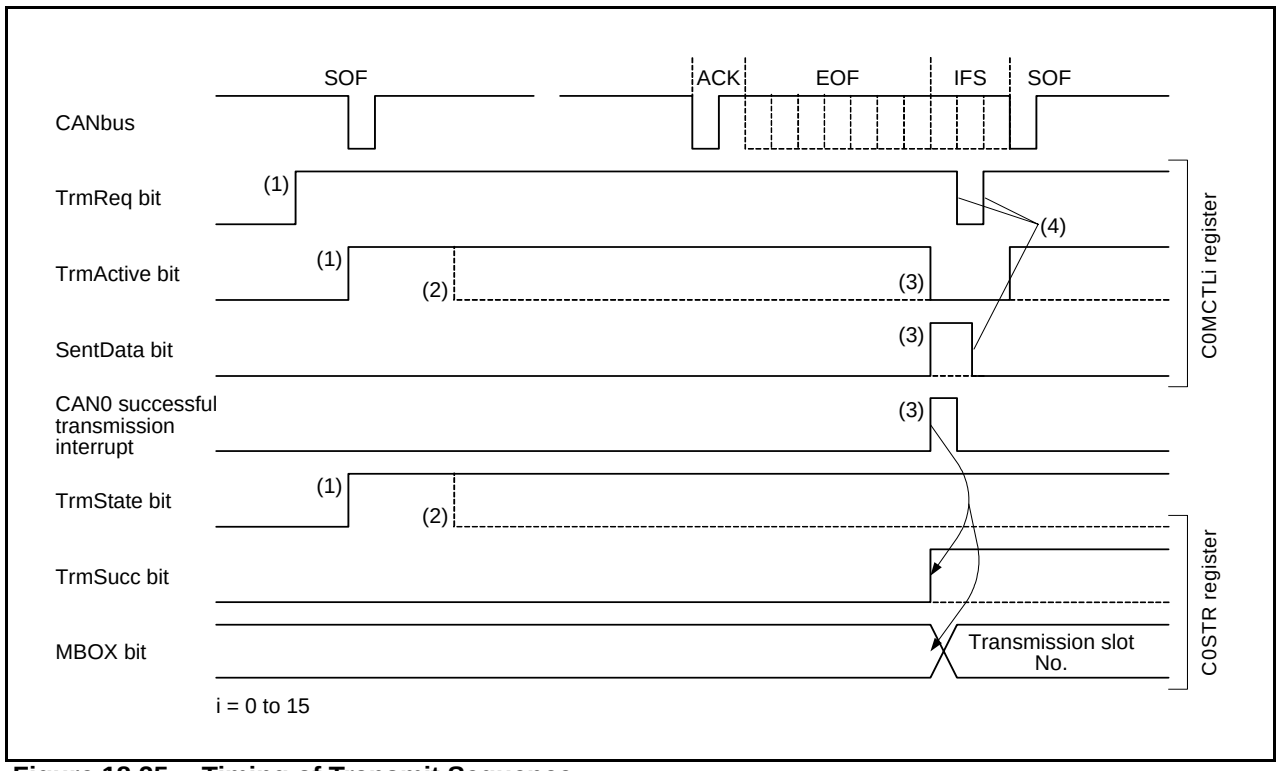


Figure 18.25 Timing of Transmit Sequence

(1) If the TrmReq bit in the C0MCTLi register (i = 0 to 15) is set to 1 (Transmission slot) in bus idle state, the TrmActive bit in the C0MCTLi register and the TrmState bit in the C0STR register are set to 1 (During transmission), and the CAN module starts transmitting a message.

(2) If the arbitration is lost after starting transmitting, the TrmActive and TrmState bits are set to 0.

(3) If the transmission is successful without lost arbitration, the SentData bit in the C0MCTLi register is set to 1 (Transmission is successfully completed) and TrmActive bit in the C0MCTLi register is set to 0 (Waiting for bus idle or completion of arbitration). When the interrupt enable bits in the C0ICR register are set to 1 (Interrupt enabled), CAN0 successful transmission interrupt request is generated and the MBOX and TrmSucc bits in the C0STR register change.

(4) When next transmission is performed, set the SentData and TrmReq bits to 0 and check that they are set to 0. Then, set the TrmReq bit to 1 by a program.

18.13 CAN Interrupts

The CAN module provides the following CAN interrupts.

- CAN0 Successful Reception Interrupt
- CAN0 Successful Transmission Interrupt
- CAN0 Error Interrupt
  - Error Passive State
  - Error BusOff State
  - Bus Error (this feature can be disabled separately)
- CAN0 Wake Up Interrupt

When the CPU detects a successful reception/transmission interrupt, the C0STR register must be read to determine which slot has issued the interrupt.

18.14 Notes on CAN Module

18.14.1 Reading C0STR Register

The CAN module updates the status of the C0STR register in a certain period. When the CPU and the CAN module access to the C0STR register at the same time, the CPU has the access priority; the access from the CAN module is disabled. Consequently, when the updating period of the CAN module matches the access period from the CPU, the status of the CAN module cannot be updated. (See Figure 18.26)
Accordingly, be careful about the following points so that the access period from the CPU should not match the updating period of the CAN module:

- There should be a wait time of 3fCAN or longer (see Table 18.4) before the CPU reads the C0STR register. (See Figure 18.27)
- When the CPU polls the C0STR register, the polling period must be 3fCAN or longer. (See Figure 18.28)

Table 18.4 CAN Module Status Updating Period

3 fCAN Period = 3 x XIN (Original Oscillation Period) x Division Value of CAN Clock (CCLK)	
(Example 1) Condition XIN 16 MHz CCLK: Divided by 1	3 fCAN period = 3 x 62.5 ns x 1 = 187.5 ns
(Example 2) Condition XIN 16 MHz CCLK: Divided by 2	3 fCAN period = 3 x 62.5 ns x 2 = 375 ns
(Example 3) Condition XIN 16 MHz CCLK: Divided by 4	3 fCAN period = 3 x 62.5 ns x 4 = 750 ns
(Example 4) Condition XIN 16 MHz CCLK: Divided by 8	3 fCAN period = 3 x 62.5 ns x 8 = 1.5 μs
(Example 5) Condition XIN 16 MHz CCLK: Divided by 16	3 fCAN period = 3 x 62.5 ns x 16 = 3 μs

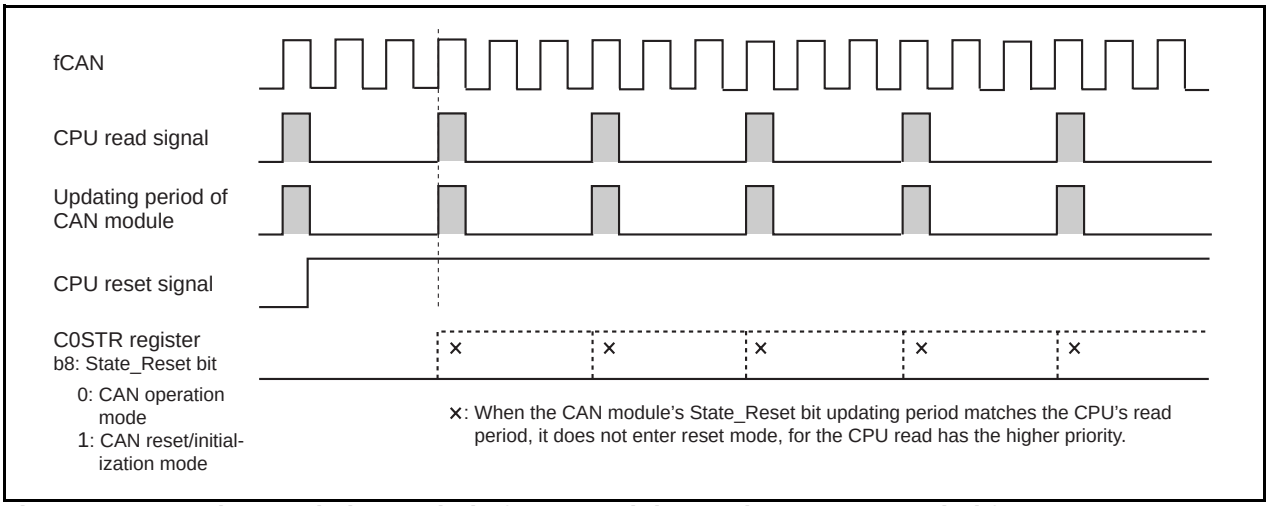


Figure 18.26 When Updating Period of CAN Module Matches Access Period from CPU

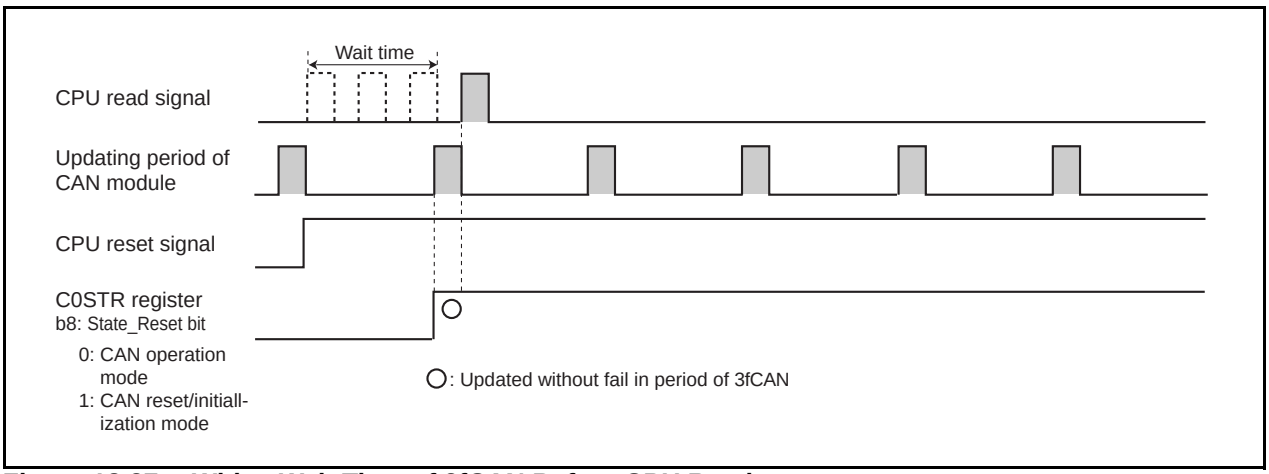


Figure 18.27 With a Wait Time of 3fCAN Before CPU Read

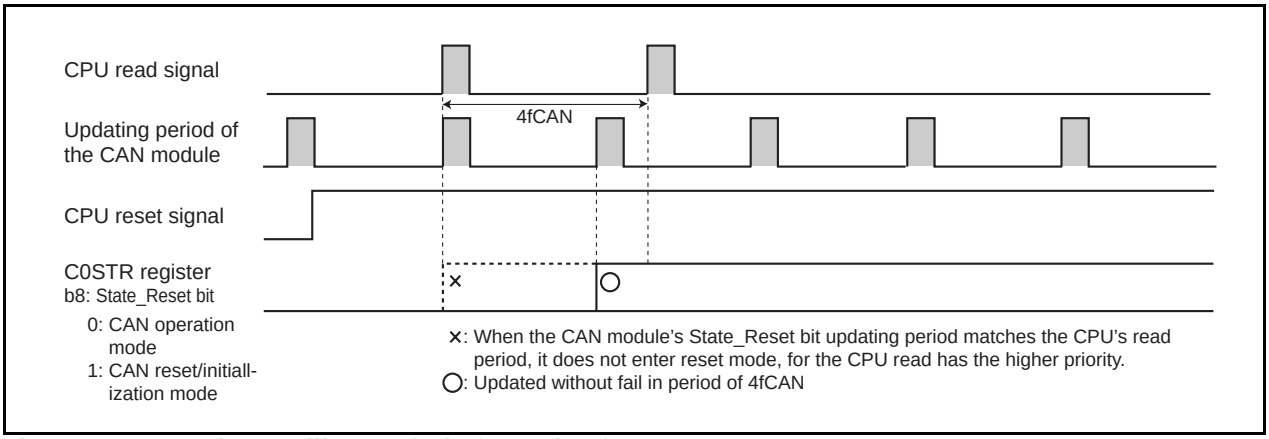


Figure 18.28 When Polling Period of CPU is 3fCAN or Longer

18.14.2 Performing CAN Configuration

If the Reset bit in the C0CTLR register is changed from 0 (operation mode) to 1 (reset/initialization mode) in order to place the CAN module from CAN operation mode into CAN reset/initialization mode, always be sure to check that the State_Reset bit in the C0STR register is set to 1 (reset mode).
Similarly, if the Reset bit is changed from 1 to 0 in order to place the CAN module from CAN reset/initialization mode into CAN operation mode, always be sure to check that the State_Reset bit is set to 0 (operation mode).
The procedure is described below.

To place CAN Module from CAN Operation Mode into CAN Reset/Initialization Mode

- Change the Reset bit from 0 to 1.
- Check that the State_Reset bit is set to 1.

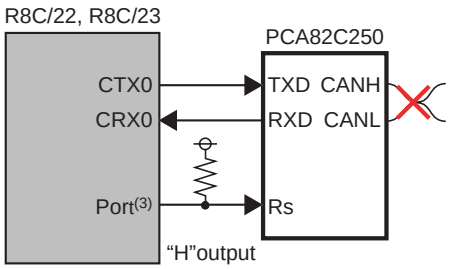
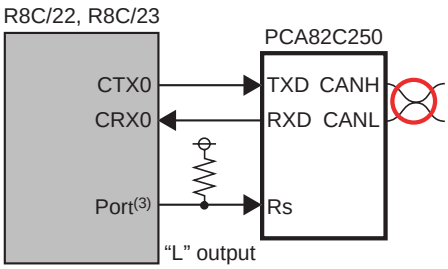
To place CAN Module from CAN Reset/Initialization Mode into CAN Operation Mode

- Change the Reset bit from 1 to 0.
- Check that the State_Reset bit is set to 0.

18.14.3 Suggestions to Reduce Power Consumption

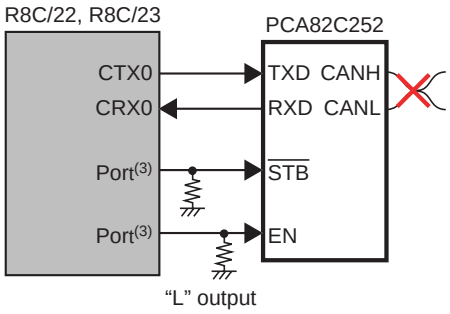
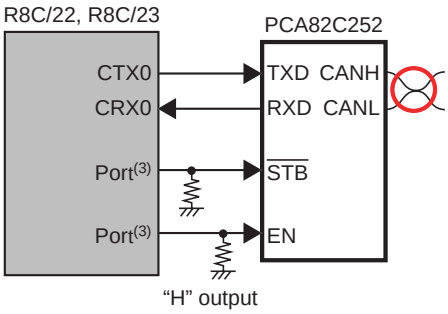
When not performing CAN communication, the operation mode of CAN transceiver should be set to “standby mode” or “sleep mode”.
When performing CAN communication, the power consumption in CAN transceiver in not performing CAN communication can be substantially reduced by controlling the operation mode pins of CAN transceiver.
Table 18.5 and Table 18.6 show Recommended Pin Connections.

Table 18.5 Recommended Pin Connections (In Case of PCA82C250: Philips Product)

	Standby Mode	High-speed Mode
Rs Pin(1)	“H”	“L”
Power Consumption in CAN Transceiver(2)	less than 170 μA	less than 70 mA
CAN Communication	impossible	possible
Connection		

NOTES:
1. The pin which controls the operation mode of CAN transceiver.
2. In case of Topr = 25°C
3. Connect to enabled port to control CAN transceiver.

Table 18.6 Recommended Pin Connections (In Case of PCA82C252: Philips Product)

	Sleep Mode	Normal Operation Mode
$\overline{\text{STB}}$ Pin(1)	“L”	“H”
EN Pin(1)	“L”	“H”
Power Consumption in CAN Transceiver(2)	less than 50 μA	less than 35 mA
CAN Communication	impossible	possible
Connection		

NOTES:
1. The pin which controls the operation mode of CAN transceiver.
2. In case of Topr = 25°C
3. Connect to enabled port to control CAN transceiver.

19. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares the pins with P0_0 to P0_7, P1_0 to P1_3. Therefore, when using these pins, ensure the corresponding port direction bits are set to 0 (input mode).
When not using the A/D converter, set the VCUT bit in the ADCON1 register to 0 (Vref unconnected), so that no current will flow from the VREF pin into the resistor ladder, helping to reduce the power consumption of the chip.
The result of A/D conversion is stored in the AD register.
Table 19.1 lists the Performance of A/D Converter. Figure 19.1 shows the Block Diagram of A/D Converter. Figure 19.2 and Figure 19.3 show the A/D converter-related registers.

Table 19.1 Performance of A/D Converter

Item	Performance
A/D Conversion Method	Successive approximation (with capacitive coupling amplifier)
Analog Input Voltage(1)	0 V to AVCC
Operating Clock ϕAD(2)	4.2 V ≤ AVCC ≤ 5.5 V f1, f2, f4, fOCO-F 2.7 V ≤ AVCC < 4.2 V f2, f4, fOCO-F
Resolution	8 bit or 10 bit is selectable
Absolute Accuracy	AVCC = Vref = 5 V, ϕAD = 10MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.3 V, ϕAD = 10MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating Mode	One-shot and repeat modes(3)
Analog Input Pin	12 pins (AN0 to AN11)
A/D Conversion Start Condition	• Software trigger Set the ADST bit in the ADCON0 register to 1 (A/D conversion starts) • Capture Timer RD interrupt request is generated while the ADST bit is set to 1
Conversion Rate Per Pin	• Without sample and hold function 8-bit resolution: 49ϕAD cycles, 10-bit resolution: 59ϕAD cycles • With sample and hold function 8-bit resolution: 28ϕAD cycles, 10-bit resolution: 33ϕAD cycles

NOTES:
1. Analog input voltage does not depend on use of sample and hold function.
   When analog input voltage exceeds reference voltage, A/D conversion result is 3FFh in 10-bit mode, FFh in 8-bit mode.
2. The frequency of ϕAD must be 10 MHz or below.
   Without sample and hold function, the ϕAD frequency should be 250 kHz or above.
   With the sample and hold function, the ϕAD frequency should be 1 MHz or above.
3. In repeat mode, only 8-bit mode can be used.

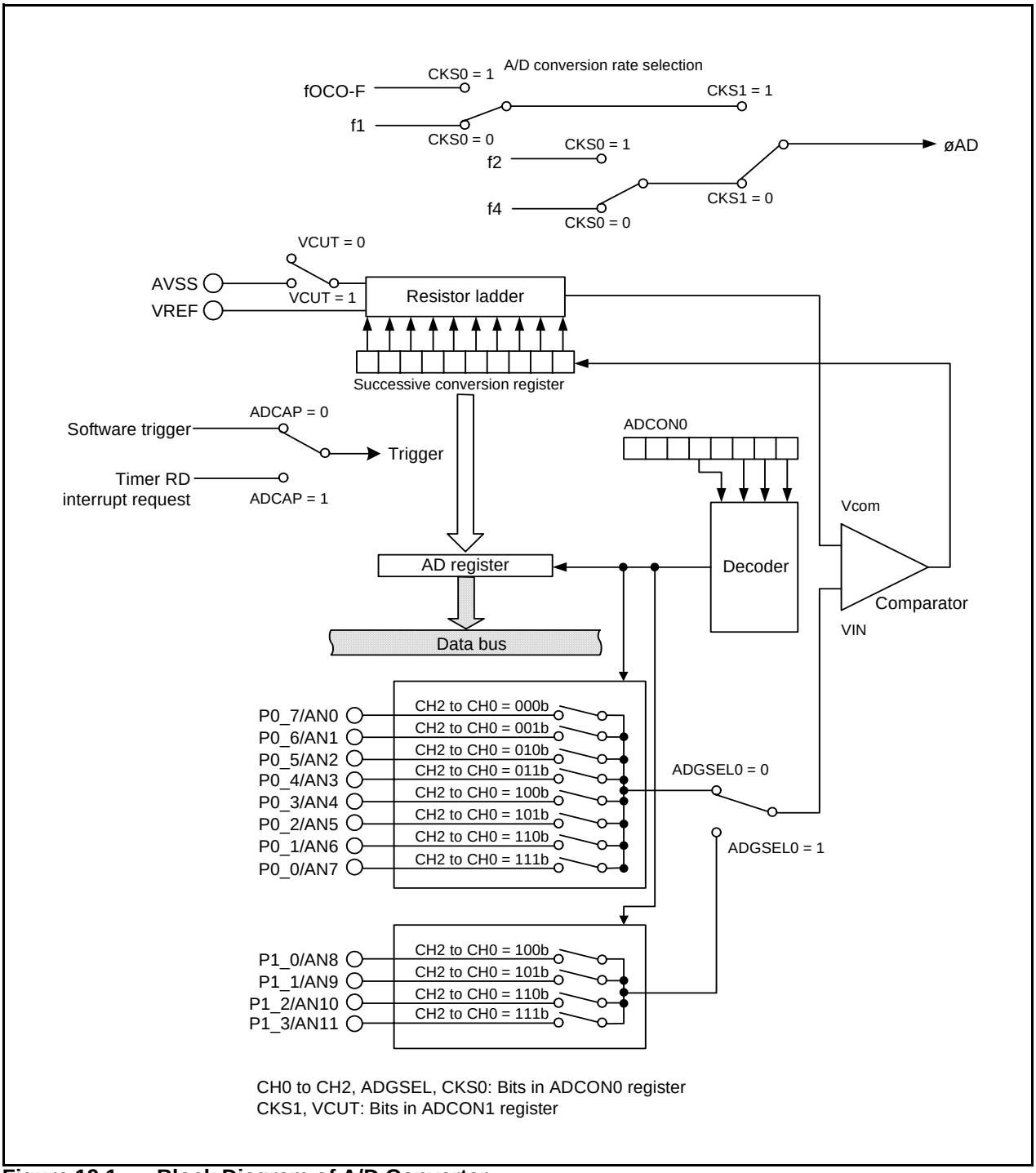
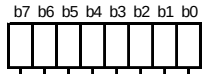


Figure 19.1 Block Diagram of A/D Converter

A/D Control Register 0(1)



Symbol	Address	After Reset
ADCON0	00D6h	00h

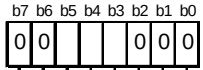
Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Refer to (4)	RW
CH1			RW
CH2			RW
MD	A/D operation mode select bit(2)	0 : On-shot mode 1 : Repeat mode	RW
ADGSEL0	A/D input group select bit(4)	0 : Selects port P0 group (AN0 to AN7) 1 : Selects port P1 group (AN8 to AN11)	RW
ADCAP	A/D conversion automatic start bit	0 : Starts in softw are trigger (ADST bit) 1 : Starts in timer RD (complementary PWM mode)	RW
ADST	A/D conversion start flag	0 : Disables A/D conversion 1 : Starts A/D conversion	RW
CKS0	Frequency select bit 0	[When CKS1 in ADCON1 register = 0] 0 : Select f4 1 : Select f2 [When CKS1 in ADCON1 register = 1] 0 : Select f1(3) 1 : Select fOCO-F	RW

NOTES:
1. If the ADCON0 register is rew ritten during A/D conversion, the conversion result is indeterminate.
2. When changing A/D operation mode, set the analog input pin again.
3. Set øAD frequency to 10 MHz or below .
4. The analog input pin can be select according to a combination of the CH0 to CH2 bits and the ADGSEL0 bit.

CH2 to CH0	ADGSEL0 = 0	ADGSEL0 = 1
000b	AN0	Do not set
001b	AN1	
010b	AN2	
011b	AN3	
100b	AN4	AN8
101b	AN5	AN9
110b	AN6	AN10
111b	AN7	AN11

Figure 19.2 ADCON0 Register

A/D Control Register 1(1)



Symbol	Address	After Reset
ADCON1	00D7h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bit	Set to 0	RW
BITS	8/10-bit mode select bit(2)	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1	Refer to a description of the CKS0 bit in the ADCON0 register function	RW
VCUT	Vref connect bit(3)	0 : Vref not connected 1 : Vref connected	RW
— (b7-b6)	Reserved Bit	Set to 0	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. Set the BITS bit to 0 (8-bit mode) in repeat mode.
3. When the VCUT bit is set to 1 (connected) from 0 (not connected), wait for 1 µs or more before starting A/D conversion.

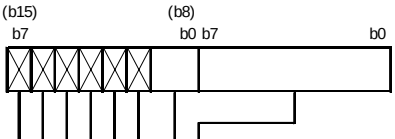
A/D Control Register 2(1)

Symbol	Address	After Reset
ADCON2	00D4h	00h

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0 : Without sample and hold 1 : With sample and hold	RW
— (b3-b1)	Reserved bit	Set to 0	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result is indeterminate.

A/D Register



Symbol	Address	After Reset
AD	00C1h-00C0h	Indeterminate

Function		RW
When BITS bit in ADCON1 register is set to 1 (10-bit mode)	When BITS bit in ADCON1 register is set to 0 (8-bit mode)	RW
8 low-order bits in A/D conversion result	A/D conversion result	RO
2 high-order bits in A/D conversion result	When read, its content is indeterminate	RO
Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 19.3 Registers ADCON1, ADCON2, and AD

19.1 One-Shot Mode

In one-shot mode, the input voltage on one selected pin is A/D converted once.
Table 19.2 lists the One-Shot Mode Specifications. Figure 19.4 shows the ADCON0 Register in One-Shot Mode and Figure 19.5 shows the ADCON1 Register in One-Shot Mode.

Table 19.2 One-Shot Mode Specifications

Item	Specification
Function	The input voltage on one selected pin by bits CH2 to CH0 and ADGSEL0 is A/D converted once
Start Condition	• When the ADCAP bit is set to 0 (software trigger), Set the ADST bit to 1 (A/D conversion starts) • When the ADCAP bit is set to 1 (starts in timer RD (complementary PWM mode)), The compare match in the TRD0 and TRDGRA0 registers or the TRD1 underflow is generated while the ADST bit is set to 1
Stop Condition	• A/D conversion completes (When the ADCAP bit is set to 0 (software trigger), the ADST bit is set to 0) • Set the ADST bit to 0
Interrupt Request Generation Timing	A/D conversion completes
Input Pin	Select one of AN0 to AN11
Reading of A/D Conversion Result	Read the AD register

A/D Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
				0			

Symbol	Address	After Reset
ADCON0	00D6h	00h

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Refer to (4)	RW
CH1			RW
CH2			RW
MD	A/D operation mode select bit(2)	0 : One-shot mode	RW
ADGSEL0	A/D input group select bit(4)	0 : Selects port P0 group (AN0 to AN7) 1 : Selects port P1 group (AN8 to AN11)	RW
ADCAP	A/D conversion automatic start bit	0 : Starts in software trigger (ADST bit) 1 : Starts in timer RD (complementary PWM mode)	RW
ADST	A/D conversion start flag	0 : Disables A/D conversion 1 : Starts A/D conversion	RW
CKS0	Frequency select bit 0	[When CKS1 in ADCON1 register = 0] 0 : Select f4 1 : Select f2 [When CKS1 in ADCON1 register = 1] 0 : Select f1(3) 1 : Select fOCO-F	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. When changing A/D operation mode, set the analog input pin again.
3. Set øAD frequency to 10 MHz or below.
4. The analog input pin can be select according to a combination of the CH0 to CH2 bits and the ADGSEL0 bit.

CH2 to CH0	ADGSEL0 = 0	ADGSEL0 = 1
000b	AN0	Do not set
001b	AN1	
010b	AN2	
011b	AN3	
100b	AN4	AN8
101b	AN5	AN9
110b	AN6	AN10
111b	AN7	AN11

Figure 19.4 ADCON0 Register in One-Shot Mode

A/D Control Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1			0	0	0

Symbol	Address	After Reset
ADCON1	00D7h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bit	Set to 0	RW
BITS	8/10-bit mode select bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1	Refer to a description of the CKS0 bit in the ADCON0 register function	RW
VCUT	Vref connect bit(2)	1 : Vref connected	RW
— (b7-b6)	Reserved bit	Set to 0	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. When the VCUT bit is set to 1 (connected) from 0 (not connected), wait for 1 µs or more before starting A/D conversion.

Figure 19.5 ADCON1 Register in One-Shot Mode

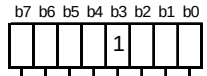
19.2 Repeat Mode

In repeat mode, the input voltage on one selected pin is A/D converted repeatedly.
Table 19.3 lists the Repeat Mode Specifications. Figure 19.6 shows the ADCON0 Register in Repeat Mode and Figure 19.7 shows the ADCON1 Register in Repeat Mode.

Table 19.3 Repeat Mode Specifications

Item	Specification
Function	The Input voltage on one pin selected by CH2 to CH0 and ADGSEL0 bits is A/D converted repeatedly
Start Condition	• When the ADCAP bit is set to 0 (software trigger) Set the ADST bit to 1 (A/D conversion starts) • When the ADCAP bit is set to 1 (starts in timer RD (complementary PWM mode)), The compare match in the TRD0 and TRDGRA0 registers or the TRD1 underflow is generated while the ADST bit is set to 1
Stop Condition	Set the ADST bit to 0
Interrupt Request Generation Timing	Not generated
Input Pin	Select one of AN0 to AN11
Reading of Result of A/D Converter	Read the AD register

A/D Control Register 0(1)



Symbol	Address	After Reset
ADCON0	00D6h	00h

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Refer to (4)	RW
CH1			RW
CH2			RW
MD	A/D operating mode select bit(2)	1 : Repeat mode	RW
ADGSEL0	A/D input group select bit(4)	0 : Selects port P0 group (AN0 to AN7) 1 : Selects port P1 group (AN8 to AN11)	RW
ADCAP	A/D conversion automatic start bit	0 : Starts in software trigger (ADST bit) 1 : Starts in timer RD (complementary PWM mode)	RW
ADST	A/D conversion start flag	0 : Disables A/D conversion 1 : Starts A/D conversion	RW
CKS0	Frequency select bit 0	[When CKS1 in ADCON1 register = 0] 0 : Select f4 1 : Select f2 [When CKS1 in ADCON1 register = 1] 0 : Select f1(3) 1 : Do not set	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. When changing A/D operation mode, set the analog input pin again.
3. Set øAD frequency to 10 MHz or below.
4. The analog input pin can be select according to a combination of the CH0 to CH2 bits and the ADGSEL0 bit.

CH2 to CH0	ADGSEL0 = 0	ADGSEL0 = 1
000b	AN0	Do not set
001b	AN1	
010b	AN2	
011b	AN3	
100b	AN4	AN8
101b	AN5	AN9
110b	AN6	AN10
111b	AN7	AN11

Figure 19.6 ADCON0 Register in Repeat Mode

A/D Control Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1		0	0	0	0

Symbol	Address	After Reset
ADCON1	00D7h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bit	Set to 0	RW
BITS	8/10-bit mode select bit(2)	0 : 8-bit mode	RW
CKS1	Frequency select bit 1	Refer to a description of the CKS0 bit in the ADCON0 register function	RW
VCUT	Vref connect bit(3)	1 : Vref connected	RW
— (b7-b6)	Reserved bit	Set to 0	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. Set the BITS bit to 0 (8-bit mode) in repeat mode.
3. When the VCUT bit is set to 1 (connected) from 0 (not connected), wait for 1 µs or more before starting A/D conversion.

Figure 19.7 ADCON1 Register in Repeat Mode

19.3 Sample and Hold

When the SMP bit in the ADCON2 register is set to 1 (with sample and hold function), A/D conversion rate per pin increases. The sample and hold function is available in all operating modes. Start the A/D conversion after selecting whether the sample and hold circuit is to be used or not.
Figure 19.8 shows the Timing Diagram of A/D Conversion.

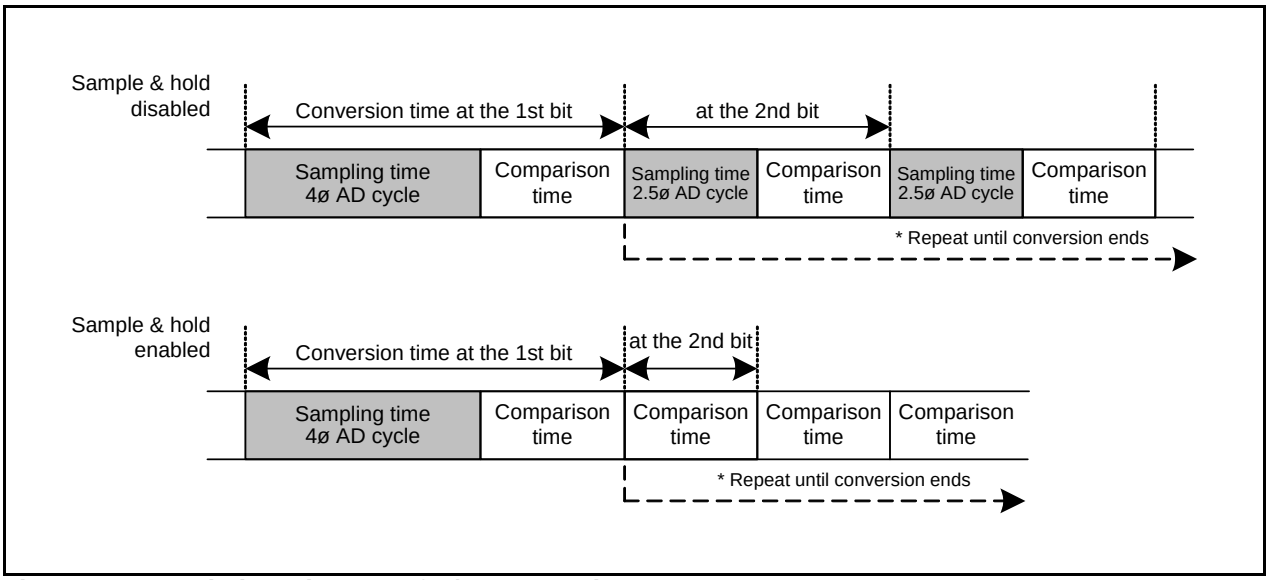
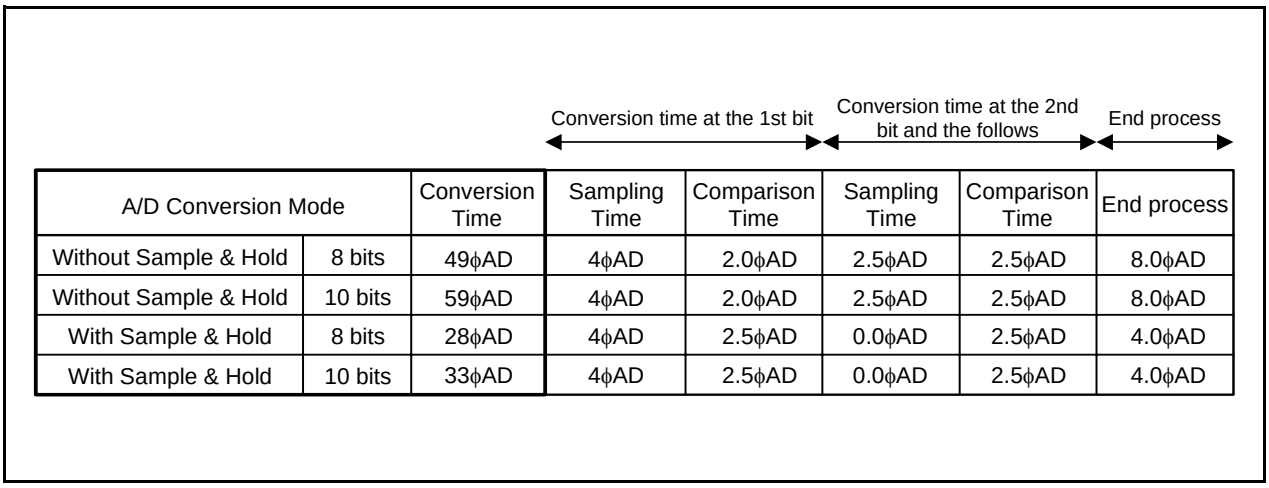


Figure 19.8 Timing Diagram of A/D Conversion

19.4 A/D Conversion Cycles

Figure 19.9 shows the A/D Conversion Cycles.

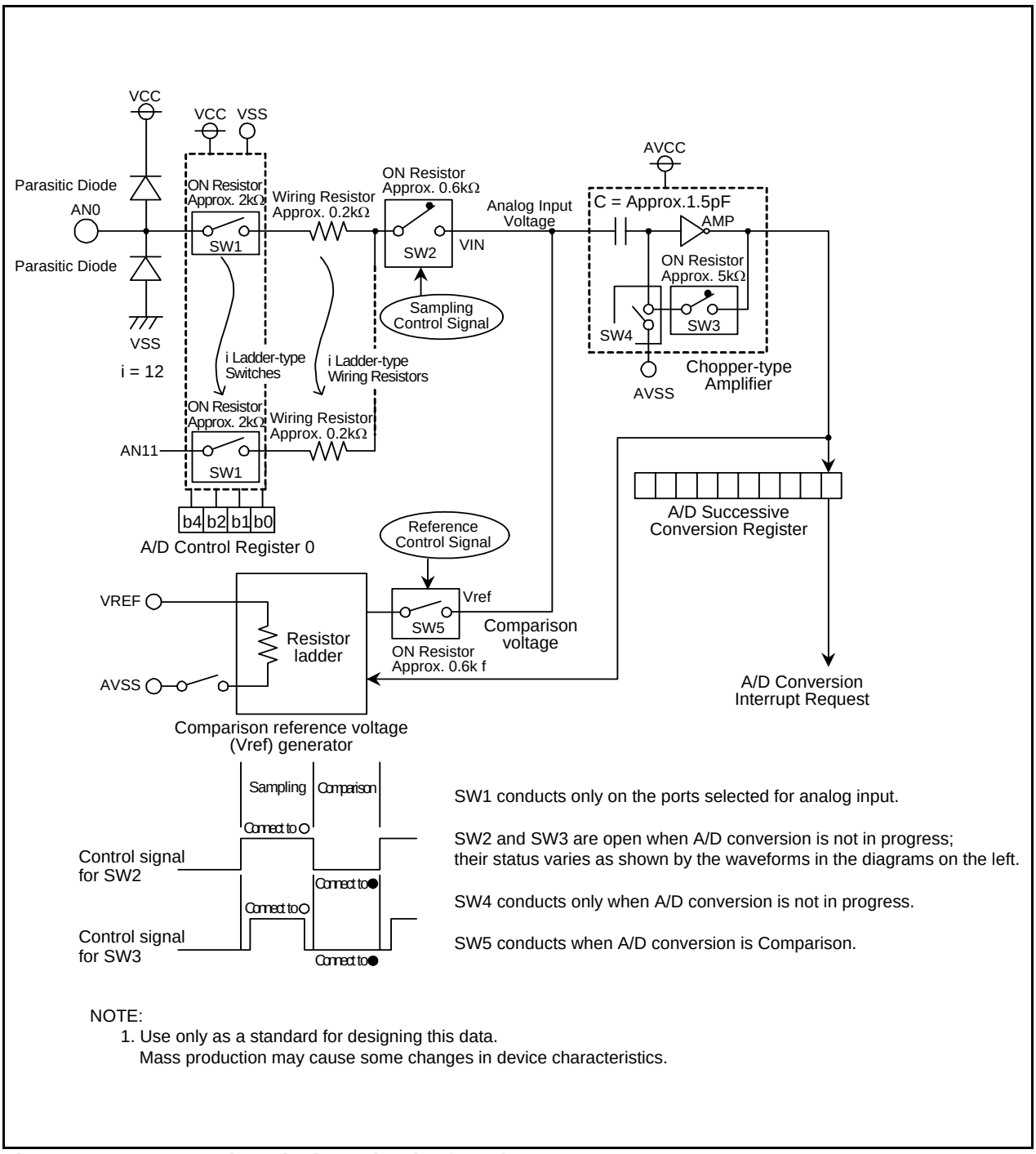


A/D Conversion Mode		Conversion Time	Sampling Time	Comparison Time	Sampling Time	Comparison Time	End process
Without Sample & Hold	8 bits	49ϕAD	4ϕAD	2.0ϕAD	2.5ϕAD	2.5ϕAD	8.0ϕAD
Without Sample & Hold	10 bits	59ϕAD	4ϕAD	2.0ϕAD	2.5ϕAD	2.5ϕAD	8.0ϕAD
With Sample & Hold	8 bits	28ϕAD	4ϕAD	2.5ϕAD	0.0ϕAD	2.5ϕAD	4.0ϕAD
With Sample & Hold	10 bits	33ϕAD	4ϕAD	2.5ϕAD	0.0ϕAD	2.5ϕAD	4.0ϕAD

Figure 19.9 A/D Conversion Cycles

19.5 Internal Equivalent Circuit of Analog Input

Figure 19.10 shows the Internal Equivalent Circuit of Analog Input.



NOTE:
1. Use only as a standard for designing this data.
   Mass production may cause some changes in device characteristics.

Figure 19.10 Internal Equivalent Circuit of Analog Input

19.6 Output Impedance of Sensor Under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 19.11 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

$$\text{VC is generally} \quad VC = VIN\left\{1 - e^{-\frac{1}{C(R0 + R)}t}\right\}$$

$$\text{And when } t = T, \quad VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0 + R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0 + R)}T = 1n\frac{X}{Y}$$

$$\text{Hence,} \quad R0 = -\frac{T}{C \bullet 1n\frac{X}{Y}} - R$$

Figure 19.11 shows Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN (0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.
When f(XIN) = 10 MHz, T = 0.25 µs in the A/D conversion mode without sample & hold. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.25 µs, R = 2.8 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.25 \times 10^{-6}}{6.0 \times 10^{-12} \bullet 1n\frac{0.1}{1024}} - 2.8 \times 10^{3} \approx 1.7 \times 10^{3}$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 1.7 kΩ maximum.

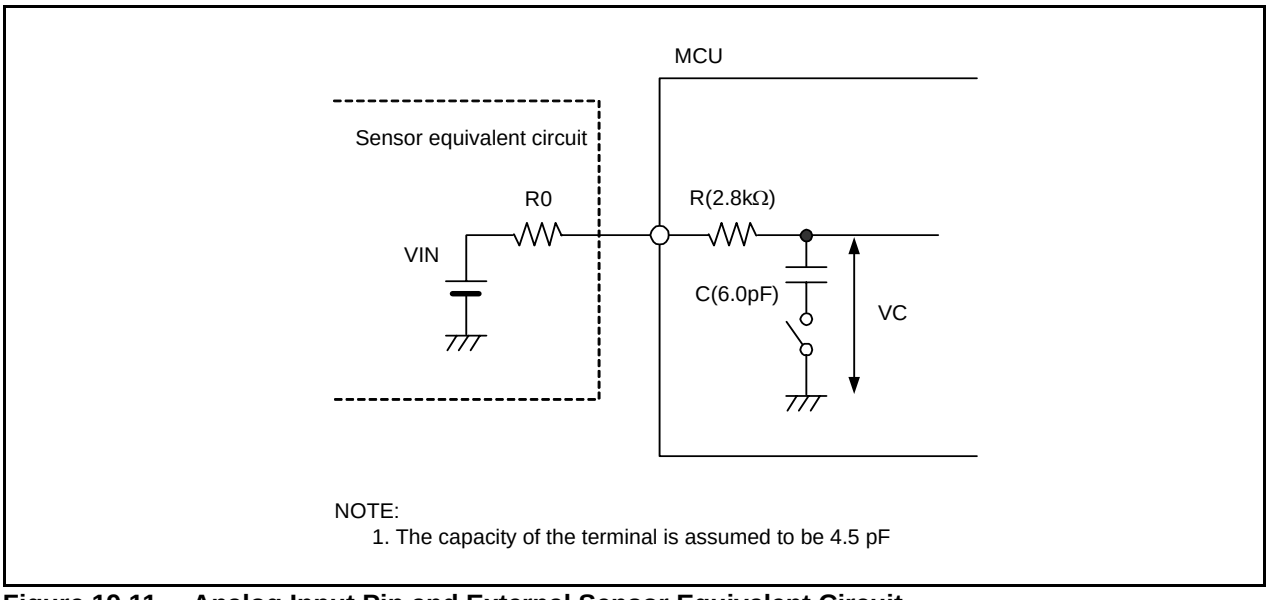


Figure 19.11 Analog Input Pin and External Sensor Equivalent Circuit

19.7 Notes on A/D Converter

- Write to each bit (other than bit 6) in the ADCON0 register, each bit in the ADCON1 register, or the SMP bit in the ADCON2 register when the A/D conversion stops (before a trigger occurs).
  When the VCUT bit in the ADCON1 register is changed from 0 (VREF not connected) to 1 (VREF connected), wait for at least 1 μs or longer before the A/D conversion starts.
- When changing A/D operating mode, select an analog input pin again.
- When using in one-shot mode. Ensure that the A/D conversion is completed and read the AD register. The IR bit in the ADIC register or the ADST bit in the ADCON0 register can determine whether the A/D conversion is completed.
- When using the repeat mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select the fOCO-F for the ϕAD.
- If setting the ADST bit in the ADCON0 register to 0 (A/D conversion stops) by a program and the A/D conversion is forcibly terminated during the A/D conversion operation, the conversion result of the A/D converter will be indeterminate. If the ADST bit is set to 0 by a program, do not use the value of AD register.
- Connect 0.1 μF capacitor between the P4_2/VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode when the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode) during A/D conversion.

20. Flash Memory

20.1 Overview

In the flash memory version, rewrite operations to the flash memory can be performed in three modes; CPU rewrite, standard serial I/O, parallel I/O modes.
Table 20.1 lists the Flash Memory Performance (see **Table 1.1** and **Table 1.2 Performance** for the items not listed on Table 20.1).

Table 20.1 Flash Memory Performance

Item		Specification
Flash Memory Operating Mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O mode)
Division of Erase Block		See **Figure 20.1** and **Figure 20.2**
Program Method		Byte unit
Erase Method		Block erase
Program, Erase Control Method		Program and erase control by software command
Rewrite Control Method		Rewrite control for blocks 0 and 1 by FMR02 bit in FMR0 register
		Rewrite control for block 0 by FMR16 bit and block 1 by FMR16 bit
Number of Commands		5 commands
Programming and erase endurance(1)	Blocks 0 and 1 (Program ROM)	R8C/22 Group: 100 times; R8C/23 Group: 1,000 times
	Blocks A and B (Data Flash)(2)	10,000 times
ID Code Check Function		Standard serial I/O mode supported
ROM Code Protect		For parallel I/O mode supported

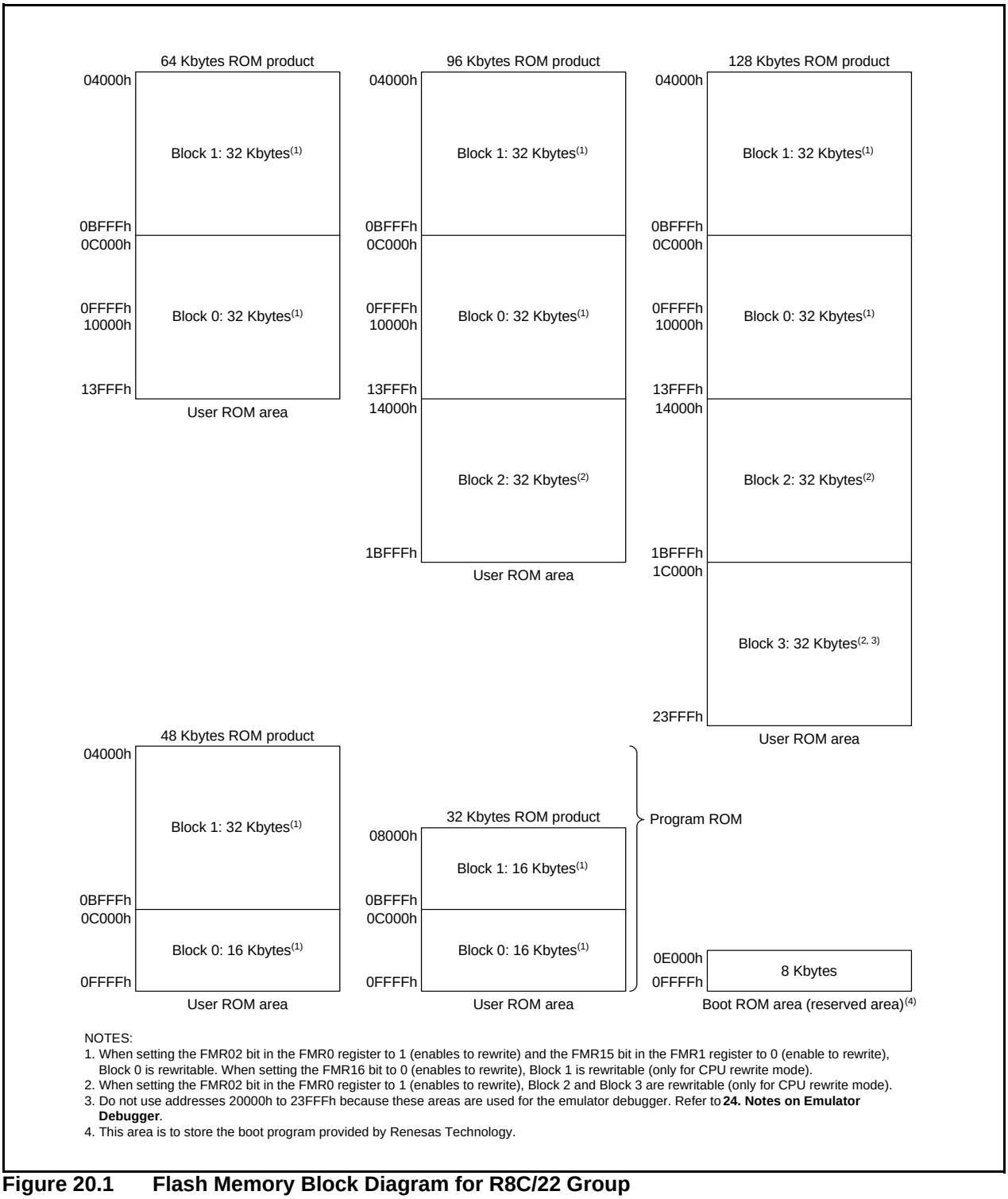
NOTES:
1. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erasure endurance can be reduced by executing programming operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
2. Blocks A and B are embedded only in the R8C/23 Group.

Table 20.2 Flash Memory Rewrite Modes

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU. EW0 mode: Rewritable in the RAM EW1 mode: Rewritable in flash memory	User ROM area is rewritten by using a dedicated serial programmer.	User ROM area is rewritten by using a dedicated parallel programmer.
Areas which can be rewritten	User ROM area	User ROM area	User ROM area
Operating mode	Single chip mode	Boot mode	Parallel I/O mode
ROM programmer	None	Serial programmer	Parallel programmer

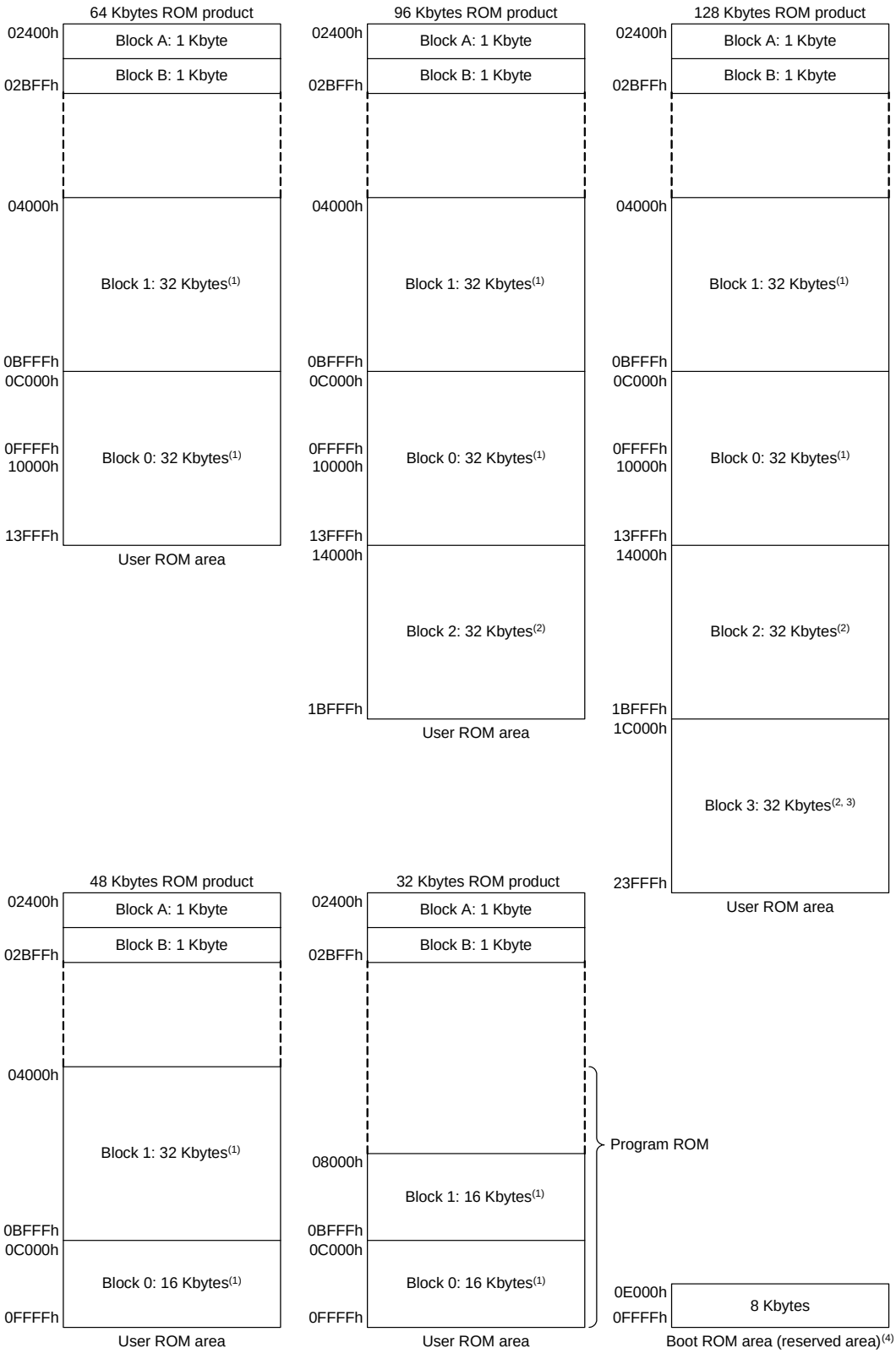
20.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 20.1 shows the Flash Memory Block Diagram for R8C/22 Group. Figure 20.2 shows the Flash Memory Block Diagram for R8C/23 Group.
The user ROM area of R8C/23 Group contains an area which stores a MCU operating program (program ROM) and the 1-Kbyte block A and B (data flash).
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite and standard serial I/O and parallel I/O modes.
When rewriting the block 0 and block 1 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to 1 (rewrite enables), and when setting the FMR15 bit in the FMR1 register to 0 (rewrite enables), block 0 is rewritable. When setting the FMR16 bit to 0 (rewrite enables), block 1 is rewritable.
When rewriting the block 2 and block 3 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to 1 (rewrite enables).
The rewrite control program for standard serial I/O mode is stored in boot ROM area before shipment. The boot ROM area and the user ROM area share the same address, but have an another memory.



NOTES:
1. When setting the FMR02 bit in the FMR0 register to 1 (enables to rewrite) and the FMR15 bit in the FMR1 register to 0 (enable to rewrite), Block 0 is rewritable. When setting the FMR16 bit to 0 (enables to rewrite), Block 1 is rewritable (only for CPU rewrite mode).
2. When setting the FMR02 bit in the FMR0 register to 1 (enables to rewrite), Block 2 and Block 3 are rewritable (only for CPU rewrite mode).
3. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.
4. This area is to store the boot program provided by Renesas Technology.

Figure 20.1 Flash Memory Block Diagram for R8C/22 Group



NOTES:
1. When setting the FMR02 bit in the FMR0 register to 1 (enables to rewrite) and the FMR15 bit in the FMR1 register to 0 (enables to rewrite), Block 0 is rewritable. When setting the FMR16 bit to 0 (enables to rewrite), Block 1 is rewritable (only for CPU rewrite mode).
2. When setting the FMR02 bit in the FMR0 register to 1 (enables to rewrite), Block 2 and Block 3 are rewritable (only for CPU rewrite mode).
3. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.
4. This area is to store the boot program provided by Renesas Technology.

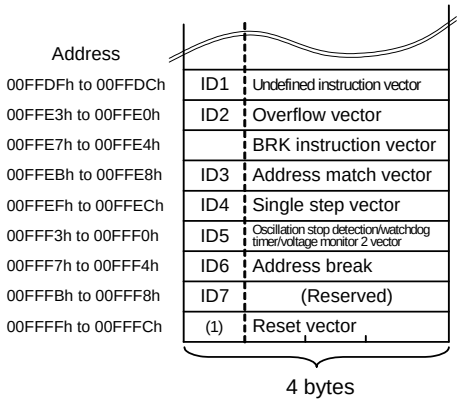
Figure 20.2 Flash Memory Block Diagram for R8C/23 Group

20.3 Functions to Prevent Rewriting of Flash Memory

Standard serial I/O mode contains an ID code check function, and the parallel I/O mode contains a ROM code protect function to prevent the flash memory from reading or rewriting easily.

20.3.1 ID Code Check Function

Use this function in standard serial I/O mode. Unless the flash memory is blank, the ID codes sent from the programmer and the ID codes written in the flash memory are determined whether they match. If the ID codes do not match, the commands sent from the programmer are not acknowledged. The ID code consists of 8-bit data, the areas of which, beginning with the first byte, are 00FFDFh, 00FFE3h, 00FFEBh, 00FFEFh, 00FFF3h, 00FFF7h, and 00FFFBh. Write a program in which the ID codes are set at these addresses and write them in the flash memory.



NOTE:
1. The OFS register is assigned to 00FFFFh. Refer to **Figure 20.4 OFS Register** for the OFS register details.

Figure 20.3 Address for Stored ID Code

20.3.2 ROM Code Protect Function

The ROM code protect function disables to read and change the internal flash memory by the OFS register in parallel I/O mode.
Figure 20.4 shows the OFS Register.
The ROM code protect function is enabled by writing 0 to the ROMCP1 bit and 1 to the ROMCR bit and disables to read and change the internal flash memory.
Once the ROM code protect is enabled, the content in the internal flash memory cannot be rewritten in parallel I/O mode. When the ROM code protect is disabled, erase the block including the OFS register with CPU rewrite mode or standard serial I/O mode.

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
		1	1			1	

Symbol	Address	Before Shipment
OFS	0FFFFh	FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b5-b4)	Reserved bits	Set to 1	RW
LVD1ON	Voltage detection circuit start bit(2)	0 : Voltage monitor 1 reset enabled after reset 1 : Voltage monitor 1 reset disabled after reset	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. To use the power-on reset, set the LVD1ON bit to 0 (voltage monitor 1 reset enabled after reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 20.4 OFS Register

20.4 CPU Rewrite Mode

In CPU rewrite mode, user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using such as a ROM programmer. Execute the program and block erase commands only to each block in user ROM area.
When an interrupt request is generated during an erase operation in CPU rewrite mode, the flash module contains an erase-suspend function which performs the interrupt process after the erase operation is halted temporarily. During the erase-suspend, user ROM area can be read by a program.
When an interrupt request is generated during the auto-program operation in CPU rewrite mode, the flash module contains a program-suspend function which performs the interrupt process after the auto-program operation suspends. During the program-suspend, user ROM area can be read by a program.
CPU rewrite mode contains erase write 0 mode (EW0 mode) and erase write 1 mode (EW1 mode).
Table 20.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 20.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating Mode	Single chip mode	Single chip mode
Areas in which a Rewrite Control Program Can be Located	User ROM area	User ROM area
Areas in which a Rewrite Control Program can be Executed	Necessary to transfer to any areas other than the flash memory (e.g., RAM) before executing	Executing directly in user ROM or RAM area possible
Areas which can be Rewritten	User ROM area	User ROM area However, other than the blocks which contain a rewrite control program(1)
Software Command Restriction	None	• Program and block erase commands Cannot be run on any block which contains a rewrite control program • Read status register command Cannot be executed
Modes After Program or Erase	Read status register mode	Read array mode
Modes After Read Status Register	Read status register mode	Do not execute this command
CPU Status During Auto-write and Auto-erase	Operating	Hold state (I/O ports hold state before the command is executed)
Flash Memory Status Detection	• Read the FMR00, FMR06, and FMR07 bits in the FMR0 register by a program • Execute the read status register command and read the SR7, SR5, and SR4 bits in the status register.	Read the FMR00, FMR06, and FMR07 bits in the FMR0 register by a program
Conditions for Transition to Erase-suspend	Set the FMR40 and FMR41 bits in the FMR4 register to 1 by a program.	The FMR40 bit in the FMR4 register is set to 1 and the interrupt request of the enabled maskable interrupt is generated
Conditions for Transitions to Program-suspend	Set the FMR40 and FMR42 bits in the FMR4 register to 1 by a program.	The FMR40 bit in the FMR4 register is set to 1 and the interrupt request of the enabled maskable interrupt is generated
CPU Clock	5 MHz or below	No restriction to the following (clock frequency to be used)

NOTE:
1. When setting the FMR02 bit in the FMR0 register to 1 (rewrite enables) and rewriting block 0 is enabled by setting the FMR15 bit in the FMR1 register to 0 (rewrite enables). Rewriting block 1 is enabled by setting the FMR16 bit to 0 (rewrite enables).

20.4.1 EW0 Mode

The MCU enters CPU rewrite mode and software commands can be acknowledged by setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled). In this case, since the FMR11 bit in the FMR1 register is set to 0, EW0 mode is selected.

Use software commands to control a program and erase operations. The FMR0 register or the status register can determine status when program and erase operation complete.

When entering an erase-suspend, set the FMR40 bit to 1 (enables suspend) and the FMR41 bit to 1 (requests erase-suspend). Wait for td(SR-SUS) and ensure that the FMR46 bit is set to 1 (enables reading) before accessing the user ROM area. The auto-erase operation restarts by setting the FMR41 bit to 0 (erase restarts).

When entering a program-suspend during the auto-program, set the FMR40 bit to 1 (enables suspend) and the FMR42 bit to 1 (requests program-suspend). Wait for td(SR-SUS) and ensure that the FMR46 bit is set to 1 (enables reading) before accessing the user ROM area. The auto-program operation restarts by setting the FMR42 bit to 0 (program restarts).

20.4.2 EW1 Mode

The MCU enters EW1 mode by setting the FMR11 bit to 1 (EW1 mode) after setting the FMR01 bit to 1 (CPU rewrite mode enabled).

The FMR0 register can determine status when program and erase operation complete. Do not execute commands of the read status register in EW1 mode.

To enable the erase-suspend function during the auto-erase, execute the block erase command after setting the FMR40 bit to 1 (enables suspend). The interrupt to enter an erase-suspend should be in interrupt enabled status. After passing td(SR-SUS) since the block erase command is executed, an interrupt request is acknowledged.

When an interrupt request is generated, the FMR41 bit is automatically set to 1 (requests erase-suspend) and the auto-erase operation is halted. If the auto-erase operation does not complete (FMR00 bit is 0) when the interrupt process completes, the auto-erase operation restarts by setting the FMR41 bit to 0 (erase restarts)

To enable the program-suspend function during the auto-program, execute the program command after setting the FMR40 bit to 1 (enables suspend). The interrupt to enter a program-suspend should be in interrupt enabled status. After waiting for td(SR-SUS) since the program command is executed, an interrupt request is acknowledged.

When an interrupt request is generated, the FMR42 bit is automatically set to 1 (requests program-suspend) and the auto-program operation suspends. When the auto-program operation does not complete (FMR00 bit is 0) after the interrupt process completes, the auto-program operation restarts by setting the FMR42 bit to 0 (program restarts).

Figure 20.5 shows the FMR0 Register, Figure 20.6 shows the FMR1 Register and Figure 20.7 shows the FMR4 Register.

20.4.2.1 FMR00 Bit

This bit indicates the operating status of the flash memory. The bit is 0 during programming, erasing (including suspend periods), or erase-suspend mode; otherwise, the bit is 1.

20.4.2.2 FMR01 Bit

The MCU is made ready to accept commands by setting the FMR01 bit to 1 (CPU rewrite mode).

20.4.2.3 FMR02 Bit

The block0, block1, block2 and block3 do not accept the program and block erase commands if the FMR02 bit is set to 0 (rewrite disabled).
The block0 and block1 are controlled rewriting in the FMR15 and FMR16 bits if the FMR02 bit is set to 1 (rewrite enabled).

20.4.2.4 FMSTP Bit

This bit is provided for initializing the flash memory control circuits, as well as for reducing the amount of current consumed in the flash memory. The flash memory is disabled against access by setting the FMSTP bit to 1. Therefore, the FMSTP bit must be written to by a program transferred to the RAM.
In the following cases, set the FMSTP bit to 1:

- When flash memory access resulted in an error while erasing or programming in EW0 mode (FMR00 bit not reset to 1 (ready))
- When entering high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stop)

Figure 20.11 shows a Process to Reduce Power Consumption in High-Speed On-Chip Oscillator Mode, Low-Speed On-Chip Oscillator Mode (XIN Clock Stops) and Low-Speed Clock Mode (XIN Clock Stops). Note that when going to stop or wait mode while the CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on again after returning from stop or wait mode.

20.4.2.5 FMR06 Bit

This is a read-only bit indicating the status of auto program operation. The bit is set to 1 when a program error occurs; otherwise, it is cleared to 0. For details, refer to the description of the **20.4.5 Full Status Check**.

20.4.2.6 FMR07 Bit

This is a read-only bit indicating the status of auto erase operation. The bit is set to 1 when an erase error occurs; otherwise, it is set to 0. Refer to **20.4.5 Full Status Check** for the details.

20.4.2.7 FMR11 Bit

Setting this bit to 1 (EW1 mode) places the MCU in EW1 mode.

20.4.2.8 FMR15 Bit

When the FMR02 bit is set to 1 (rewrite enabled) and the FMR15 bit is set to 0 (rewrite enabled), the block0 accepts the program command and block erase command.

20.4.2.9 FMR16 Bit

When the FMR02 bit is set to 1 (rewrite enabled) and the FMR16 bit is set to 0 (rewrite enabled), the block1 accepts the program command and block erase command.

20.4.2.10 FMR40 Bit

The suspend function is enabled by setting the FMR40 bit to 1 (enable).

20.4.2.11 FMR41 Bit

In EW0 mode, the MCU enters erase-suspend mode when setting the FMR41 bit to 1 by a program. The FMR41 bit is automatically set to 1 (requests erase-suspend) when an interrupt request of an enabled interrupt is generated in EW1 mode, and then the MCU enters erase-suspend mode.
Set the FMR41 bit to 0 (erase restart) when the auto-erase operation restarts.

20.4.2.12 FMR42 Bit

In EW0 mode, the MCU enters program-suspend mode when setting the FMR42 bit to 1 by a program. The FMR42 bit is automatically set to 1 (requests program-suspend) when an interrupt request of an enabled interrupt is generated in EW1 mode, and then the MCU enters program-suspend mode.
Set the FMR42 bit to 0 (program restarts) when the auto-program operation restarts.

20.4.2.13 FMR43 Bit

When the auto-erase operation starts, the FMR43 bit is set to 1 (during erase execution). The FMR43 bit remains 1 (during erase execution) during erase-suspend operation.
When the auto-erase operation ends, the FMR43 bit is set to 0 (erase not executed).

20.4.2.14 FMR44 Bit

When the auto-program starts, the FMR44 bit is set to 1 (during program execution). The FMR44 bit remains 1 (during program execution) during program-suspend operation.
When the auto-program operation ends, the FMR44 bit is set to 0 (program not executed).

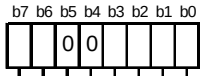
20.4.2.15 FMR46 Bit

The FMR46 bit is set to 0 (reading disabled) during auto-program or auto-erase execution and set to 1 (reading enabled) in suspend mode. Do not access the flash memory while this bit is set to 0.

20.4.2.16 FMR47 Bit

Power consumption when reading the flash memory can be reduced by setting the FMR47 bit to 1 (enabled) in low-speed on-chip oscillator mode (XIN clock stops).

Flash Memory Control Register 0



Symbol	Address	After Reset
FMR0	01B7h	00000001b

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0 : Busy (During writing or erasing) 1 : Ready	RO
FMR01	CPU rewrite mode select bit(1)	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Block 0, 1, 2, 3 rewrite enable bit(2,6)	0 : Disables rewrite 1 : Enables rewrite	RW
FMSTP	Flash memory stop bit(3,5)	0 : Enables flash memory operation 1 : Stops flash memory (Enters low-power consumption state and flash memory is reset)	RW
— (b5-b4)	Reserved bit	Set to 0	RW
FMR06	Program status flag(4)	0 : Completed successfully 1 : Terminated by error	RO
FMR07	Erase status flag(4)	0 : Completed successfully 1 : Terminated by error	RO

NOTES:
1. When setting this bit to 1, set to 1 immediately after setting it first to 0. Do not generate an interrupt between setting the bit to 0 and setting it to 1. Enter read array mode and set this bit to 0.
2. Set this bit to 1 immediately after setting this bit first to 0 while the FMR01 bit is set to 1. Do not generate an interrupt between setting the bit to 0 and setting it to 1.
3. Set this bit by a program transferred to the RAM.
4. This bit is set to 0 by executing the clear status command.
5. This bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). When the FMR01 bit is set to 0 and writing 1 to the FMSTP bit, the FMSTP bit is set to 1. The flash memory does not enter low-power consumption stat
6. When setting the FMR01 bit to 0 (CPU rewrite mode disabled), the FMR02 bit is set to 0 (disables rewrite).

Figure 20.5 FMR0 Register

Flash Memory Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
1			0	0	0		

Symbol	Address	After Reset
FMR1	01B5h	1000000Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	When read, its content is indeterminate.	RO
FMR11	EW1 mode select bit(1,2)	0 : EW0 mode 1 : EW1 mode	RW
— (b4-b2)	Reserved bit	Set to 0	RW
FMR15	Block 0 rewrite disable bit(2,3)	0 : Enables rewrite 1 : Disables rewrite	RW
FMR16	Block 1 rewrite disable bit(2,3)	0 : Enables rewrite 1 : Disables rewrite	RW
— (b7)	Reserved bit	Set to 1	RW

NOTES:

1. When setting this bit to 1, set to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1 (CPU rewrite mode enable) . Do not generate an interrupt between setting the bit to 0 and setting it to 1.
2. This bit is set to 0 by setting the FMR01 bit to 0 (CPU rewrite mode disabled).
3. When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the FMR15 and FMR16 bits can be written.
   When setting this bit to 0, set to 0 immediately after setting it first to 1.
   When setting this bit to 1, set it to 1.

Figure 20.6 FMR1 Register

Flash Memory Control Register 4

b7	b6	b5	b4	b3	b2	b1	b0
		0					

Symbol	Address	After Reset
FMR4	01B3h	01000000b

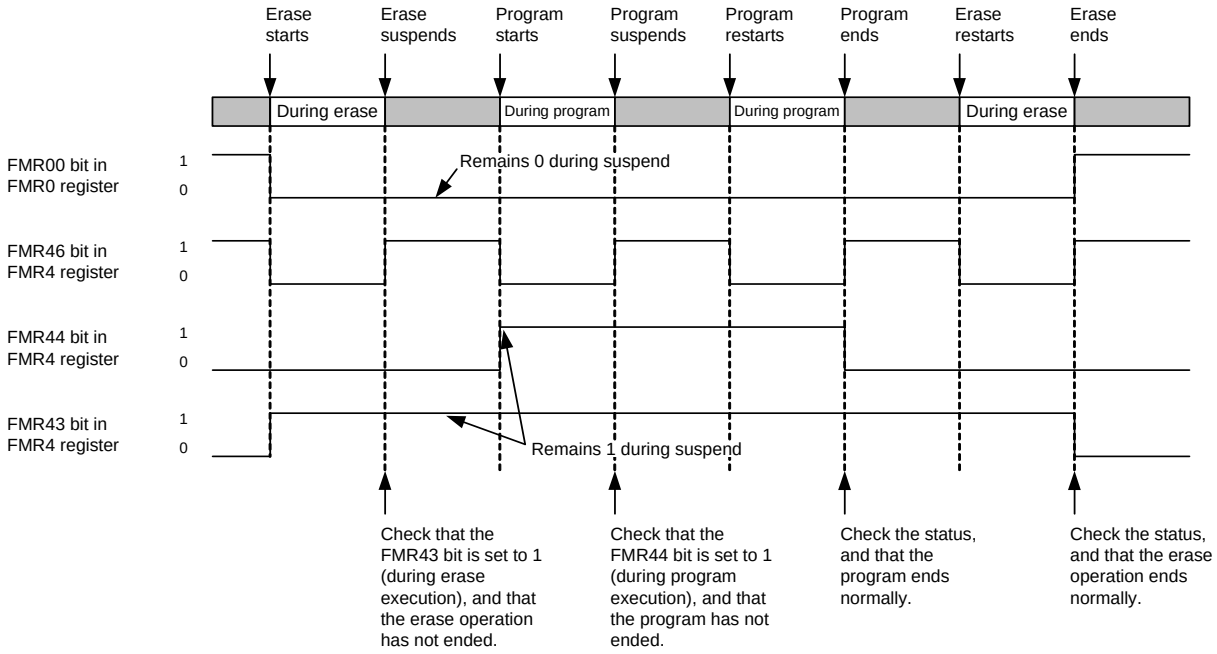
Bit Symbol	Bit Name	Function	RW
FMR40	Erase-suspend function enable bit(1)	0 : Disable 1 : Enable	RW
FMR41	Erase-suspend request bit(2)	0 : Erase restart 1 : Erase-suspend request	RW
FMR42	Program-suspend request bit(3)	0 : Program restart 1 : Program-suspend request	RW
FMR43	Erase command flag	0 : Erase not executed 1 : During erase execution	RO
FMR44	Program command flag	0 : Program not executed 1 : During program execution	RO
— (b5-b2)	Reserved bit	Set to 0	RO
FMR46	Read status flag	0 : Disables reading 1 : Enables reading	RO
FMR47	Low-power consumption read mode enable bit (1,4)	0 : Disable 1 : Enable	RW

NOTES:

1. When setting this bit to 1, set to 1 immediately after setting it first to 0. Do not generate an interrupt between setting the bit to 0 and setting it to 1.
2. This bit is enabled when the FMR40 bit is set to 1 (enable) and this bit can be written during the period between issuing an erase command and completing an erase (This bit is set to 0 during the periods other than above.)
   In EW0 mode, this can be set to 0 or 1 by a program.
   In EW1 mode, this bit is automatically set to 1 if a maskable interrupt is generated during an erase operation while the FMR40 bit is set to 1. Do not set this bit to 1 by a program (0 can be written).
3. The FMR42 bit is enabled only when the FMR40 bit is set to 1 (enable) and programming to the FMR42 bit is enabled until the auto-program ends since the program command is generated. (This bit is set to 0 during periods other than above.)
   In EW0 mode, 0 or 1 can be programmed to the FMR42 bit by a program.
   In EW1 mode, the FMR42 bit is automatically set to 1 by generating a maskable interrupt during the auto-program when the FMR40 bit is set to 1. 1 cannot be programmed to the FMR42 bit by a program.
4. In high-speed clock mode and high-speed on-chip oscillator mode, set the FMR47 bit to 0 (disabled).
5. Set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) in low-power-consumption read mode.

Figure 20.7 FMR4 Register

Figure 20.8 shows the Timing of Suspend Operation.



The above figure shows an example of the use of program-suspend during programming following erase-suspend.

NOTE:
1. If program-suspend is entered during erase-suspend, always restart programming.

Figure 20.8 Timing of Suspend Operation

Figure 20.9 shows the How to Set and Exit EW0 Mode. Figure 20.10 shows the How to Set and Exit EW1 Mode.

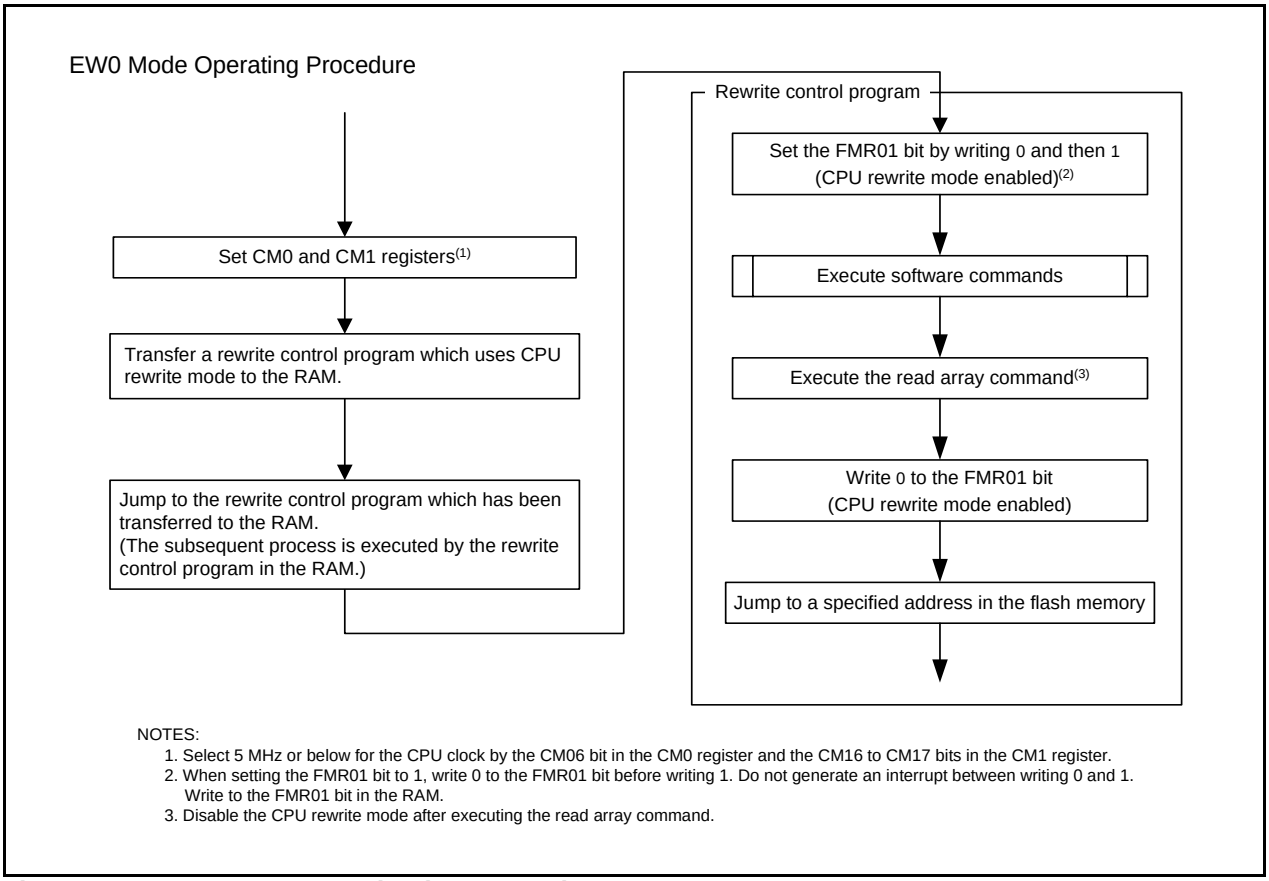


Figure 20.9 How to Set and Exit EW0 Mode

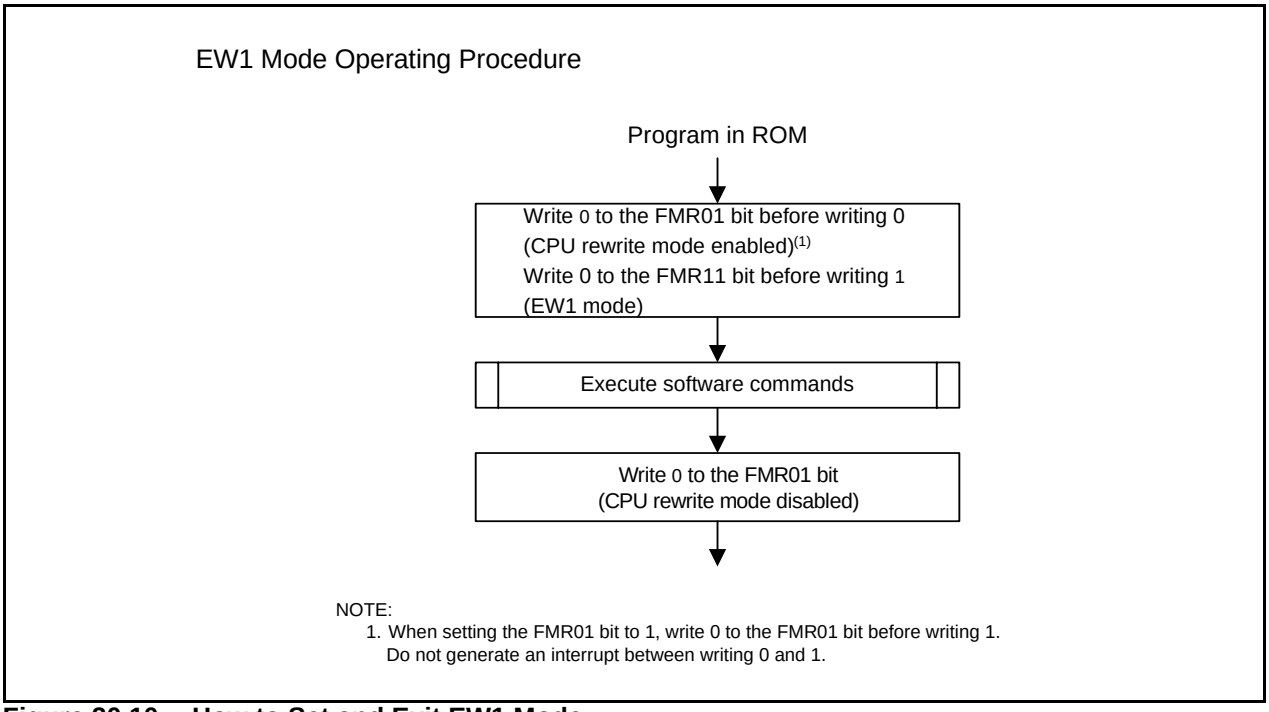
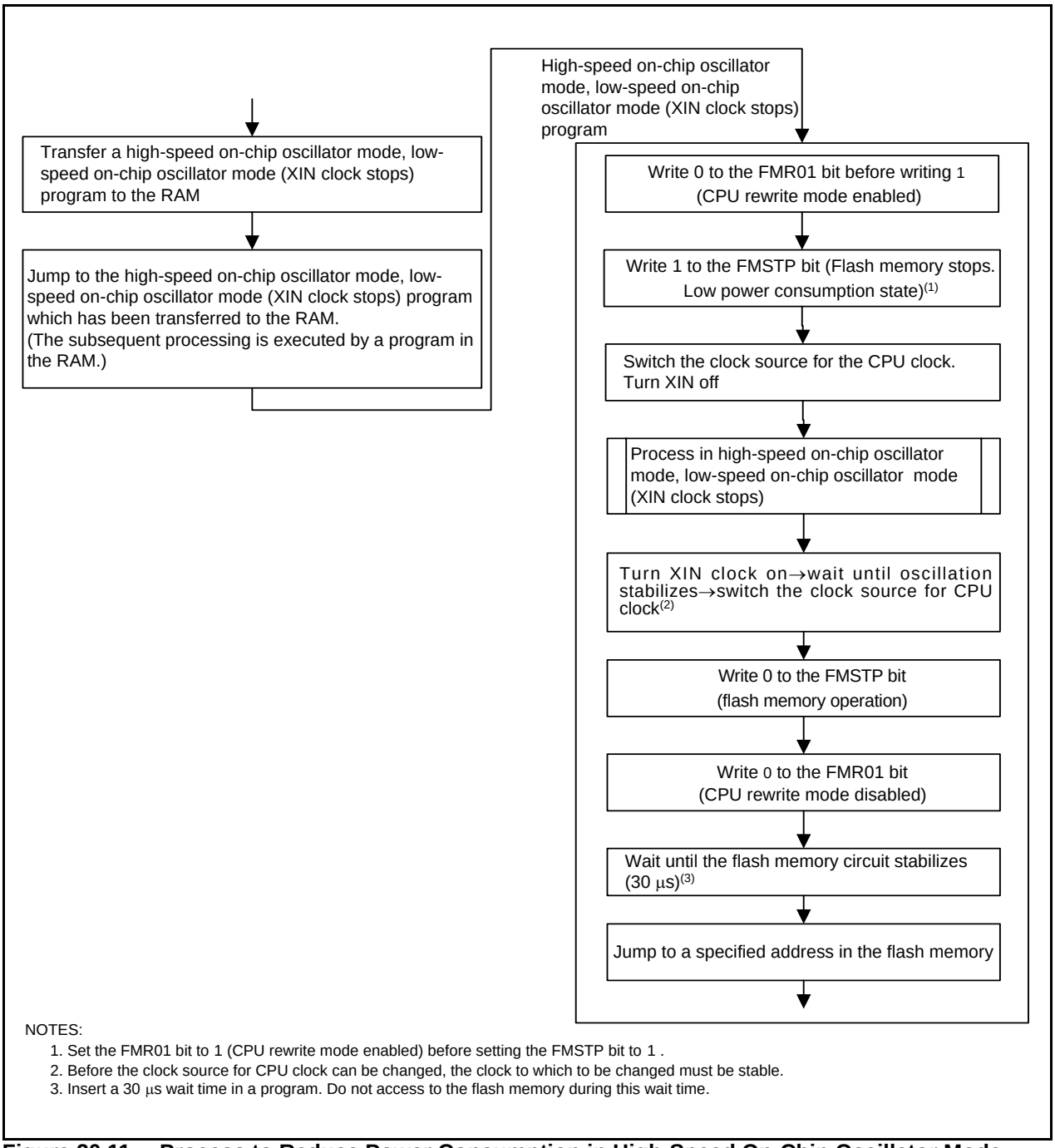


Figure 20.10 How to Set and Exit EW1 Mode



NOTES:
1. Set the FMR01 bit to 1 (CPU rewrite mode enabled) before setting the FMSTP bit to 1 .
2. Before the clock source for CPU clock can be changed, the clock to which to be changed must be stable.
3. Insert a 30 μs wait time in a program. Do not access to the flash memory during this wait time.

Figure 20.11 Process to Reduce Power Consumption in High-Speed On-Chip Oscillator Mode, Low-Speed On-Chip Oscillator Mode (XIN Clock Stops) and Low-Speed Clock Mode (XIN Clock Stops)

20.4.3 Software Commands

Software commands are described below. Read or write commands and data from or to in 8-bit units.

Table 20.4 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data (D7 to D0)	Mode	Address	Data (D7 to D0)
Read Array	Write	×	FFh			
Read Status Register	Write	×	70h	Read	×	SRD
Clear Status Register	Write	×	50h			
Program	Write	WA	40h	Write	WA	WD
Block Erase	Write	×	20h	Write	BA	D0h

SRD: Status register data (D7 to D0)
WA: Write address (Ensure the address specified in the first bus cycle is the same address as the write address specified in the second bus cycle.)
WD: Write data (8 bits)
BA: Given block address
×: Any specified address in the user ROM area

20.4.3.1 Read Array Command

The read array command reads the flash memory.
The MCU enters read array mode by writing FFh in the first bus cycle. If entering the read address after the following bus cycles, the content of the specified address can be read in 8-bit units.
Since the MCU remains in read array mode until another command is written, the contents of multiple addresses can be read continuously.
In addition, the MCU enters read array mode after a reset.

20.4.3.2 Read Status Register Command

The read status register command reads the status register.
If writing 70h in the first bus cycle, the status register can be read in the second bus cycle. (Refer to **20.4.4 Status Registers**) When reading the status register, specify an address in the user ROM area.
Do not execute this command in EW1 mode.
The MCU remains in read status register mode until the next read array command is written.

20.4.3.3 Clear Status Register Command

The clear status register command sets the status register to 0.
If writing 50h in the first bus cycle, the FMR06 to FMR07 bits in the FMR0 register and SR4 to SR5 in the status register will be set to 0.

20.4.3.4 Program Command

The program command writes data to the flash memory in 1-byte units.
By writing 40h in the first bus cycle and data in the second bus cycle to the write address, and an auto program operation (data program and verify) will start. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FMR00 bit in the FMR0 register can determine whether auto programming has completed.
When suspend function disabled, the FMR00 bit is set to 0 during auto-programming and set to 1 when auto-programming completes.
When suspend function enabled, the FMR44 bit is set to 1 during auto-programming and set to 0 when auto-programming completes.
The FMR06 bit in the FMR0 register can determine the result of auto programming after it has been finished. (Refer to **20.4.5 Full Status Check**)
When the FMR02 bit in the FMR0 register is set to 0 (disable rewriting), program commands targeting block 0 to 3 are not acknowledged. When the FMR02 bit is set to 1 (rewrite enables) and the FMR15 bit in the FMR1 register is set to 1 (disable rewriting), program commands targeting block 0 are not acknowledged. When the FMR16 bit is set to 1 (disable rewriting), program commands targeting block 1 are not acknowledged.
Figure 20.12 shows the Program Command (When Suspend Function Disabled). Figure 20.13 shows the Program Command (When Suspend Function Enabled).
In EW1 mode, do not execute this command on any address at which the rewrite control program is allocated.
In EW0 mode, the MCU enters read status register mode at the same time auto programming starts and the status register can be read. The status register bit 7 (SR7) is set to 0 at the same time auto programming starts and set back to 1 when auto programming completes. In this case, the MCU remains in read status register mode until a read array command is written next. Reading the status register can determine the result of auto programming after auto programming has completed.

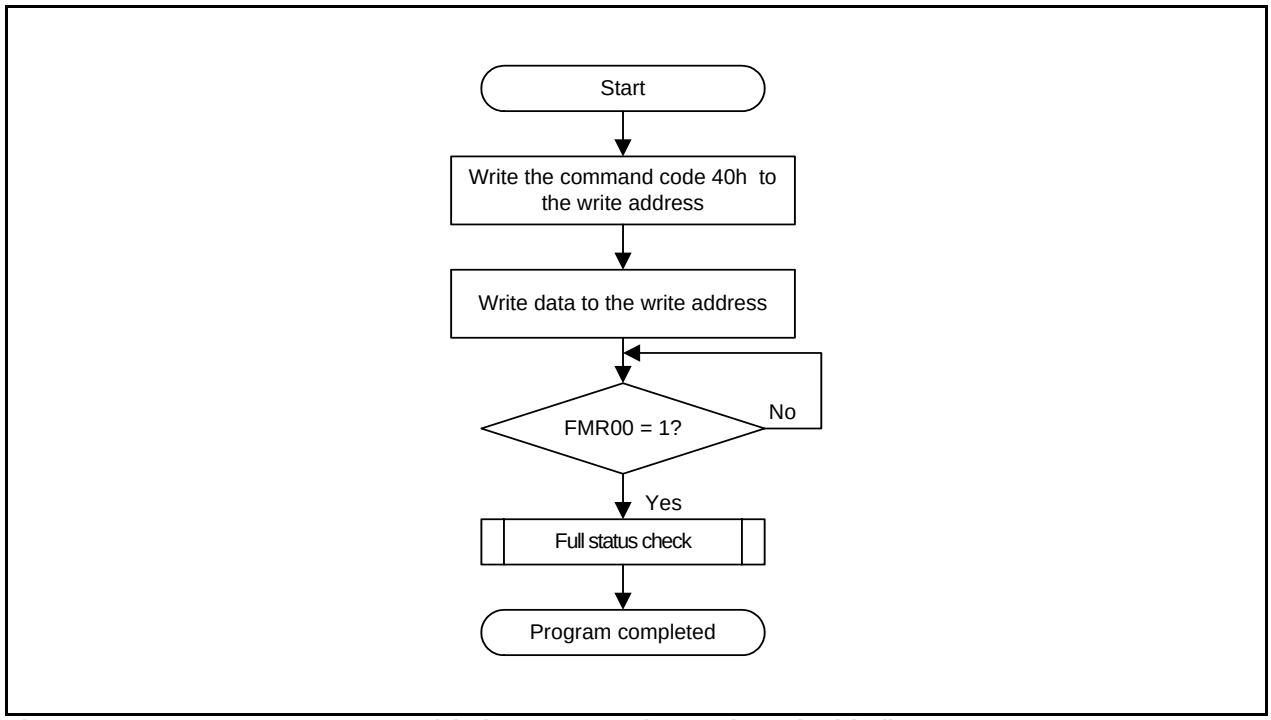
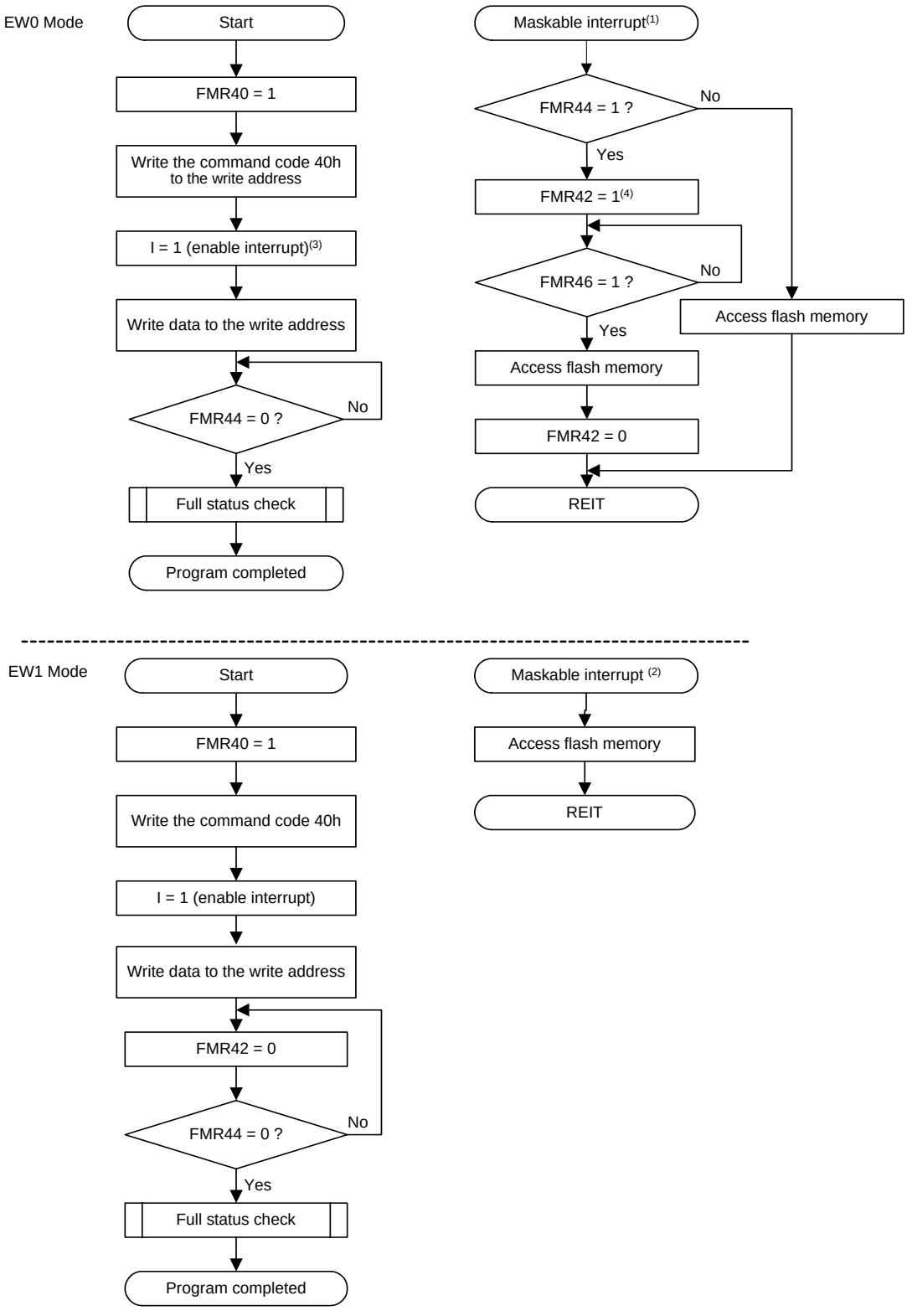


Figure 20.12 Program Command (When Suspend Function Disabled)



NOTES:
1. In EW0 mode, the interrupt vector table and interrupt routine for interrupts to be used should be allocated to the RAM area.
2. td(SR-SUS) is needed until the interrupt request is acknowledged after it is generated. The interrupt to enter suspend should be in interrupt enabled status.
3. When no interrupt is used, the instruction to enable interrupts is not needed.
4. td(SR-SUS) is needed until program is suspended after the FMR42 bit in the FMR4 register is set to 1.

Figure 20.13 Program Command (When Suspend Function Enabled)

20.4.3.5 Block Erase

If writing 20h in the first bus cycle and D0h to the given address of a block in the second bus cycle, and an auto erase operation (erase and verify) will start.
The FMR00 bit in the FMR0 register can determine whether auto erasing has completed.
The FMR00 bit is set to 0 during auto erasing and set to 1 when auto erasing completes.
The FMR07 bit in the FMR0 register can determine the result of auto erasing after auto erasing has completed. (Refer to **20.4.5 Full Status Check**)
When the FMR02 bit in the FMR0 register is set to 0 (disable rewriting) or the FMR02 bit is set to 1 (rewrite enables) and the FMR15 bit in the FMR1 register is set to 1 (disable rewriting), the block erase command on block 0 is not acknowledged. When the FMR16 bit is set to 1 (disable rewriting), the block erase command on block 1 is not acknowledged.
Do not use the block erase command during program-suspend.
Figure 20.14 shows the Block Erase Command (When Erase-Suspend Function Disabled). Figure 20.15 shows the Block Erase Command (When Erase-Suspend Function Enabled).
In EW1 mode, do not execute this command on any address at which the rewrite control program is allocated.
In EW0 mode, the MCU enters read status register mode at the same time auto erasing starts and the status register can be read. The status register bit 7 (SR7) is set to 0 at the same time auto erasing starts and set back to 1 when auto erasing completes. In this case, the MCU remains in read status register mode until the read array command is written next.

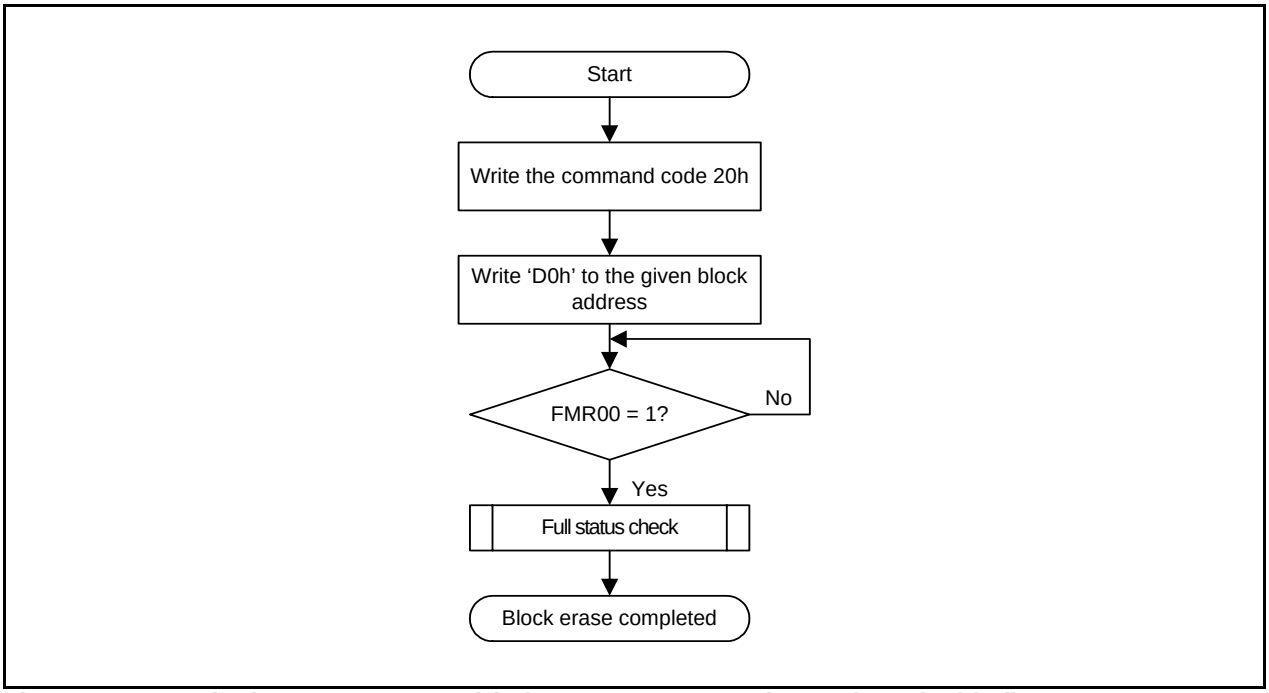
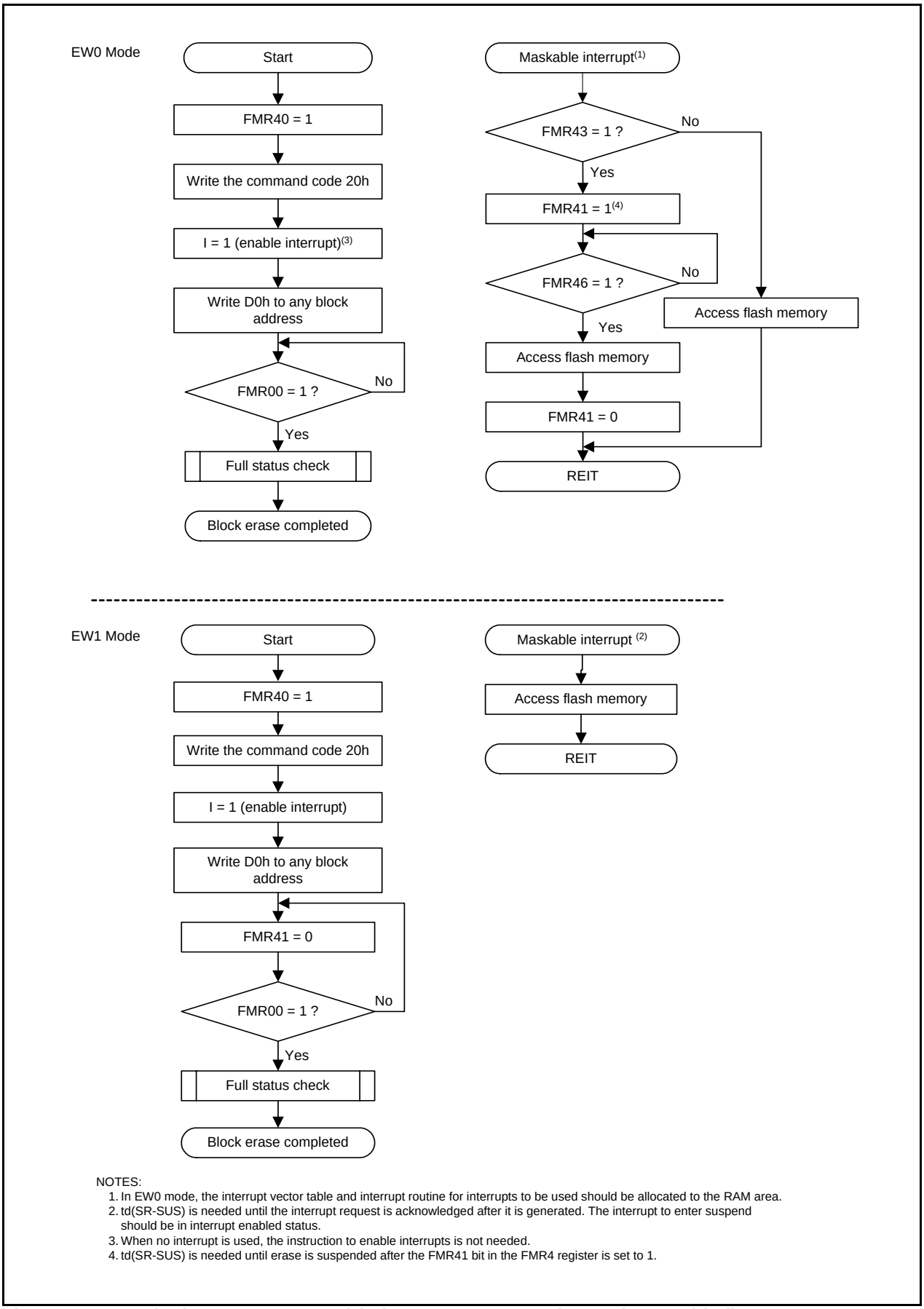


Figure 20.14 Block Erase Command (When Erase-Suspend Function Disabled)



NOTES:
1. In EW0 mode, the interrupt vector table and interrupt routine for interrupts to be used should be allocated to the RAM area.
2. td(SR-SUS) is needed until the interrupt request is acknowledged after it is generated. The interrupt to enter suspend should be in interrupt enabled status.
3. When no interrupt is used, the instruction to enable interrupts is not needed.
4. td(SR-SUS) is needed until erase is suspended after the FMR41 bit in the FMR4 register is set to 1.

Figure 20.15 Block Erase Command (When Erase-Suspend Function Enabled)

20.4.4 Status Registers

The status register indicates the operating status of the flash memory and whether an erasing or programming operation completes normally or in error. Status of the status register can be read by the FMR00, FMR06, and FMR07 bits in the FMR0 register.
Table 20.5 lists the Status Register Bits.
In EW0 mode, the status register can be read in the following cases:

- When a given address in the user ROM area is read after writing the read status register command
- When a given address in the user ROM area is read after executing the program or block erase command but before executing the read array command.

20.4.4.1 Sequencer Status (Bits SR7 and FMR00)

The sequencer status indicates operating status of the flash memory. SR7 = 0 (busy) during auto programming and auto erasing, and is set to 1 (ready) at the same time the operation completes.

20.4.4.2 Erase Status (Bits SR5 and FMR07)

Refer to **20.4.5 Full Status Check**.

20.4.4.3 Program Status (Bits SR4 and FMR06)

Refer to **20.4.5 Full Status Check**.

Table 20.5 Status Register Bits

Status Register Bit	FMR0 Register Bit	Status Name	Description		Value after Reset
			0	1	
SR0 (D0)	–	Reserved	–	–	–
SR1 (D1)	–	Reserved	–	–	–
SR2 (D2)	–	Reserved	–	–	–
SR3 (D3)	–	Reserved	–	–	–
SR4 (D4)	FMR06	Program status	Completed normally	Error	0
SR5 (D5)	FMR07	Erase status	Completed normally	Error	0
SR6 (D6)	–	Reserved	–	–	–
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1

- D0 to D7: Indicates the data bus which is read when the read status register command is executed.
- The FMR07 (SR5) to FMR06 bits (SR4) are set to 0 by executing the clear status register command.
- When the FMR07 bit (SR5) or FMR06 bit (SR4) is set to 1, the program and block erase command cannot be accepted.

20.4.5 Full Status Check

When an error occurs, the FMR06 to FMR07 bits in the FMR0 register are set to 1, indicating occurrence of each specific error. Therefore, checking these status bits (full status check) can determine the executed result. Table 20.6 lists the Errors and FMR0 Register Status. Figure 20.16 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 20.6 Errors and FMR0 Register Status

FMR0 Register (Status Register) Status		Error	Error Occurrence Condition
FMR07(SR5)	FMR06(SR4)		
1	1	Command sequence error	• When any command is not written correctly • When invalid data other than those that can be written in the second bus cycle of the block erase command is written (i.e., other than D0h or FFh)(1) • When executing the program command or block erase command while rewriting is disabled using the FMR02 bit in the FMR0 register, the FMR15 or FMR16 bit in the FMR1 register. • When inputting and erasing the address in which the Flash memory is not allocated during the erase command input • When executing to erase the block which disables rewriting during the erase command input. • When inputting and writing the address in which the Flash memory is not allocated during the write command input. • When executing to write the block which disables rewriting during the write command input.
1	0	Erase error	• When the block erase command is executed but not automatically erased correctly
0	1	Program error	• When the program command is executed but not automatically programmed correctly.

NOTE:
1. The MCU enters read array mode by writing FFh in the second bus cycle of these commands, at the same time the command code written in the first bus cycle will disabled.

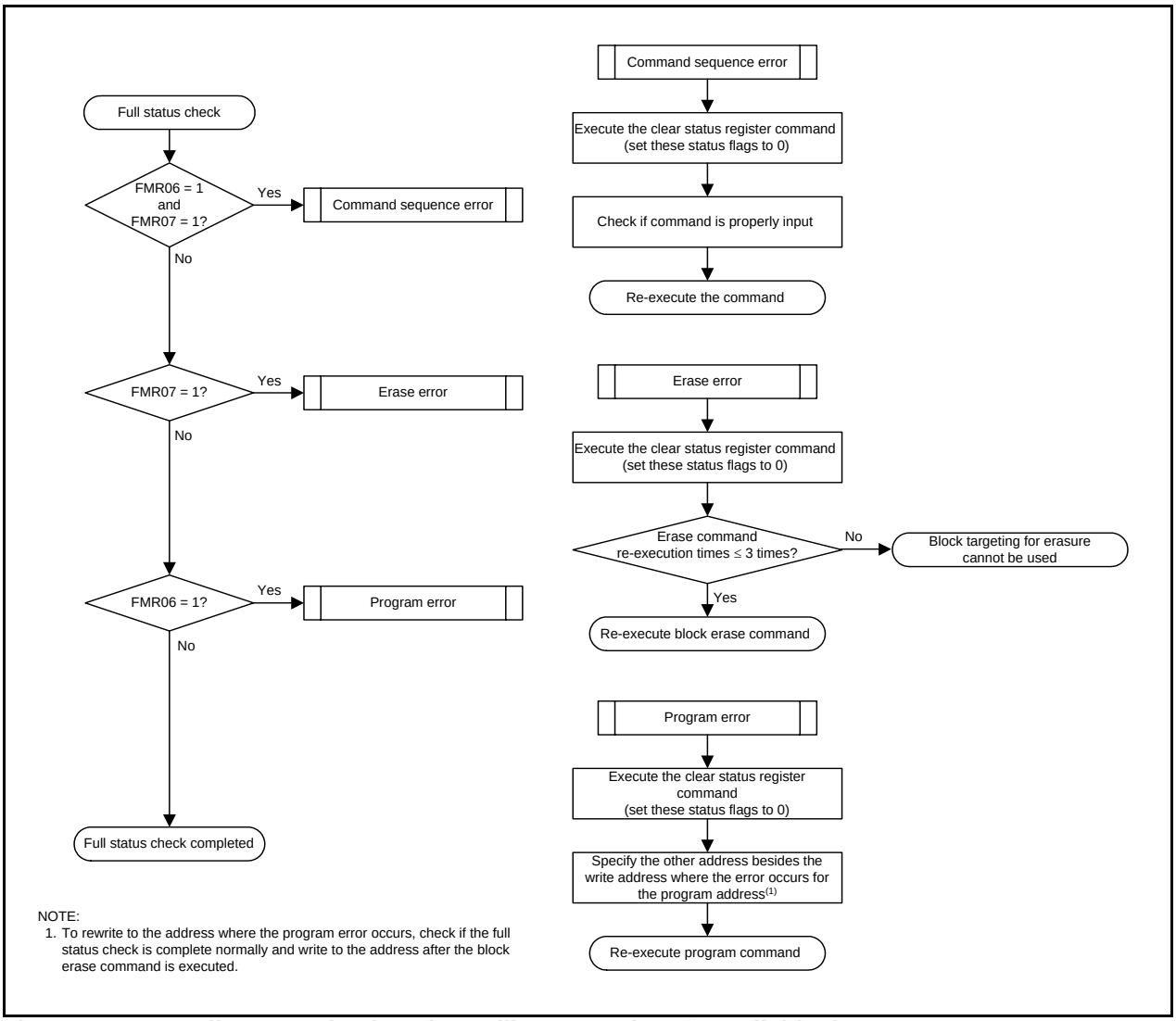


Figure 20.16 Full Status Check and Handling Procedure for Individual Errors

20.5 Standard Serial I/O Mode

In standard serial I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a serial programmer which is applicable for the MCU.

There are three types of Standard serial I/O modes:

- Standard serial I/O mode 1 . . . . Clock synchronous serial I/O used to connect with a serial programmer
- Standard serial I/O mode 2 . . . . Clock asynchronous serial I/O used to connect with a serial programmer
- Standard serial I/O mode 3 . . . . Special clock asynchronous serial I/O used to connect with a serial programmer

This MCU uses Standard serial I/O mode 2 and Standard serial I/O mode 3.

Refer to **Appendix 2. Connection Examples between Serial Writer and On-Chip Debugging Emulator**. Contact the manufacturer of your serial programmer for serial programmer. Refer to the user's manual of your serial programmer for details on how to use it.

Table 20.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2), Table 20.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3), Figure 20.17 shows Pin Connections for Standard Serial I/O Mode 3. After processing the pins shown in Table 20.8 and rewriting a flash memory using a writer, apply "H" to the MODE pin and reset a hardware if a program is operated on the flash memory in single-chip mode.

20.5.1 ID Code Check Function

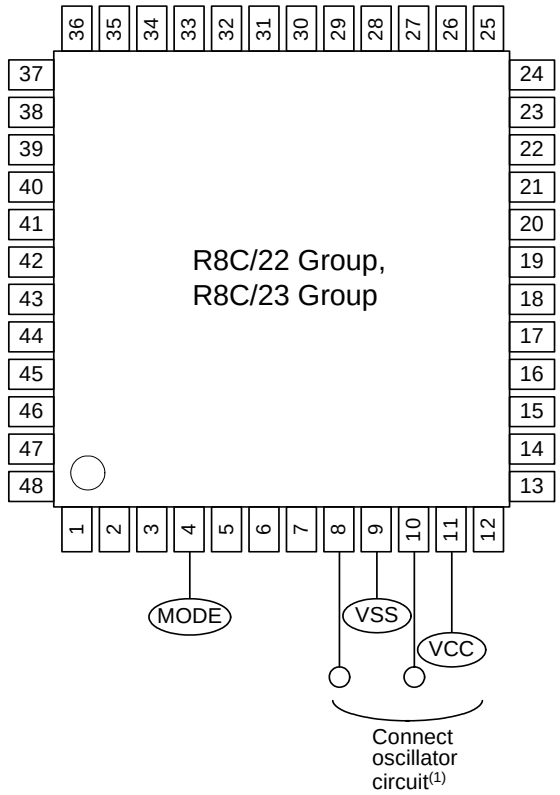
The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match (refer to **20.3 Functions to Prevent Rewriting of Flash Memory**).

Table 20.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC,VSS	Power input		Apply the voltage guaranteed for programming and erasure to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	Connect a ceramic resonator or crystal oscillator between the XIN and XOUT pins.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_7	Input port P0	I	Input "H" or "L" level signal or leave the pin open.
P1_0 to P1_7	Input port P1	I	Input "H" or "L" level signal or leave the pin open.
P2_0 to P2_7	Input port P2	I	Input "H" or "L" level signal or leave the pin open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input "H" or "L" level signal or leave the pin open.
P4_2, P4_5	Input port P4	I	Input "H" or "L" level signal or leave the pin open.
P6_0 to P6_5	Input port P6	I	Input "H" or "L" level signal or leave the pin open.
MODE	MODE	I	Input "L".
P6_6	TXD output	O	Serial data input pin.
P6_7	RXD input	I	Serial data output pin.

Table 20.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC,VSS	Power input		Apply the voltage guaranteed for programming and erasure to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	Connect ceramic resonator or crystal oscillator between XIN and XOUT pins when connecting external oscillator. Apply “H” and “L” or leave the pin open when using as input port
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_7	Input port P0	I	Input “H” or “L” level signal or leave the pin open.
P1_0 to P1_7	Input port P1	I	Input “H” or “L” level signal or leave the pin open.
P2_0 to P2_7	Input port P2	I	Input “H” or “L” level signal or leave the pin open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input “H” or “L” level signal or leave the pin open.
P4_2 to P4_5	Input port P4	I	Input “H” or “L” level signal or leave the pin open.
P6_0 to P6_7	Input port P6	I	Input “H” or “L” level signal or leave the pin open.
MODE	MODE	I/O	Serial data I/O pin. connect to the flash programmer.



Package: PLQP0048KB-A

NOTE:
1. No need to connect an oscillating circuit when operating with on-chip oscillator clock.

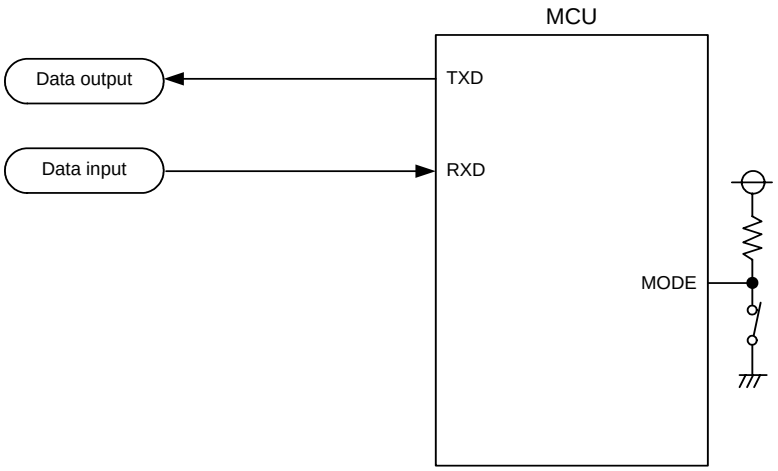
Mode setting

Signal	Value
MODE	Voltage from programmer
$\overline{\text{RESET}}$	VSS → VCC

Figure 20.17 Pin Connections for Standard Serial I/O Mode 3

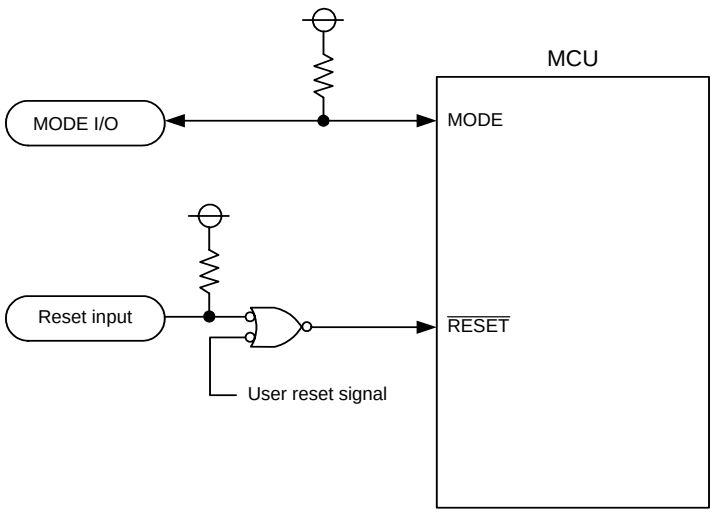
20.5.1.1 Example of Circuit Application in the Standard Serial I/O Mode

Figure 20.18 shows an example of Pin Processing in Standard Serial I/O Mode 2 and Figure 20.19 shows an example of Pin Processing in Standard Serial I/O Mode 3. Since the controlled pins vary depending on the programmer, refer to the manual of your serial programmer.



NOTES:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. Connecting the oscillation is necessary. Set the main clock frequency 1 MHz to 20 MHz. Refer to **Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)**.

Figure 20.18 Pin Processing in Standard Serial I/O Mode 2



NOTES:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with on-chip oscillator clock, connecting the oscillating circuit is not necessary.

Figure 20.19 Pin Processing in Standard Serial I/O Mode 3

20.6 Parallel I/O Mode

Parallel I/O mode is used to input and output the required software command, address and data parallel to controls (read, program and erase) for internal flash memory. Use a parallel programmer which supports this MCU. Contact the manufacturer of your parallel programmer about the parallel programmer and refer to the user's manual of your parallel programmer for details on how to use it.

User ROM area can be rewritten shown in Figure 20.1 and Figure 20.2 in parallel I/O mode.

20.6.1 ROM Code Protect Function

The ROM code protect function disables to read and rewrite the flash memory. (Refer to **20.3 Functions to Prevent Rewriting of Flash Memory**.)

20.7 Notes on Flash Memory

20.7.1 CPU Rewrite Mode

20.7.1.1 Operating Speed

Before entering CPU rewrite mode (EW0 mode), select 5 MHz or below for the CPU clock using the CM06 bit in the CM0 register and the CM16 to CM17 bits in the CM1 register. This usage note is not needed for EW1 mode.

20.7.1.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because the flash memory internal data is referenced: UND, INTO, and BRK instructions.

20.7.1.3 Interrupts

Table 20.9 lists the EW0 Mode Interrupts and Table 20.10 lists the EW1 Mode Interrupts.

Table 20.9 EW0 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection and Voltage Monitor 2 Interrupt Request are Acknowledged
EW0	During automatic erasing	Any interrupt can be used by allocating a vector to RAM	Once an interrupt request is acknowledged, the auto-programming or auto-erasing is forcibly stopped immediately and resets the flash memory. An interrupt process starts after the fixed period and the flash memory restarts. Since the block during the auto-erasing or the address during the auto-programming is forcibly stopped, the normal value may not be read. Execute the auto-erasing again and ensure the auto-erasing is completed normally. Since the watchdog timer does not stop during the command operation, the interrupt request may be generated. Reset the watchdog timer regularly.
	Automatic writing		

NOTES:
1. Do not use the address match interrupt while the command is executed because the vector of the address match interrupt is allocated on ROM.
2. Do not use the non-maskable interrupt while block 0 is automatically erased because the fixed vector is allocated block 0.

Table 20.10 EW1 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection and Voltage Monitor 2 Interrupt Request are Acknowledged
EW1	During automatic erasing (erase-suspend function is enabled)	The auto-erasing is suspended after td(SR-SUS) and the interrupt process is executed. The auto-erasing can be restarted by setting the FMR41 bit in the FMR4 register to 0 (erase restart) after the interrupt process completes.	Once an interrupt request is acknowledged, the auto-programming or auto-erasing is forcibly stopped immediately and resets the flash memory. An interrupt process starts after the fixed period and the flash memory restarts. Since the block during the auto-erasing or the address during the auto-programming is forcibly stopped, the normal value may not be read. Execute the auto-erasing again and ensure the auto-erasing is completed normally. Since the watchdog timer does not stop during the command operation, the interrupt request may be generated. Reset the watchdog timer regularly using the erase-suspend function.
	During automatic erasing (erase-suspend function is disabled)	The auto-erasing has a priority and the interrupt request acknowledgement is waited. The interrupt process is executed after the auto-erasing completes.	
	During automatic programming (program suspend function enabled)	The auto-programming is suspended after td(SR-SUS) and the interrupt process is executed. The auto-programming can be restarted by setting the FMR42 bit in the FMR4 register to 0 (program restart) after the interrupt process completes.	
	Auto programming (program suspend function disabled)	The auto-programming has a priority and the interrupt request acknowledgement is waited. The interrupt process is executed after the auto-programming completes.	

NOTES:
1. Do not use the address match interrupt while the command is executed because the vector of the address match interrupt is allocated on ROM.
2. Do not use the non-maskable interrupt while block 0 is automatically erased because the fixed vector is allocated block 0.

20.7.1.4 How to Access

Write 0 to the corresponding bits before writing 1 when setting the FMR01, FMR02, or FMR11 bit to 1. Do not generate an interrupt between writing 0 and 1.

20.7.1.5 Rewriting User ROM Area

In EW0 mode, if the power supply voltage drops while rewriting any block in which the rewrite control program is stored, the flash memory may not be able to be rewritten because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

20.7.1.6 Program

Do not write additions to the already programmed address.

20.7.1.7 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

21. Electrical Characteristics

Table 21.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (D, J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 21.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 21.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AVCC	–	–	10	Bits
–	Absolute Accuracy	10-bit mode	ϕAD = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕAD = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕAD = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕAD = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AVCC	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕAD = 10 MHz, V_{ref} = AVCC = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕAD = 10 MHz, V_{ref} = AVCC = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	AVCC	V
V_{IA}	Analog input voltage(2)			0	–	AVCC	V
–	A/D operating clock frequency	Without sample & hold		0.25	–	10	MHz
		With sample & hold		1	–	10	MHz

NOTES:
1. VCC = AVCC = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. When analog input voltage exceeds reference voltage, A/D conversion result is 3FFh in 10-bit mode, FFh in 8-bit mode.

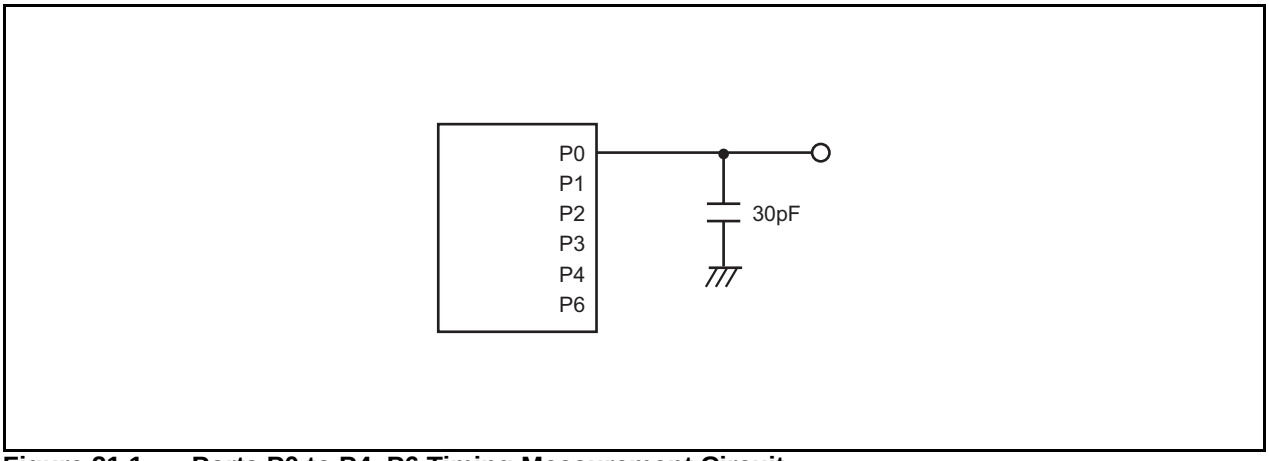


Figure 21.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 21.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/22 Group	100(3)	–	–	times
		R8C/23 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 21.5 Flash Memory (Data Flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Minimum endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

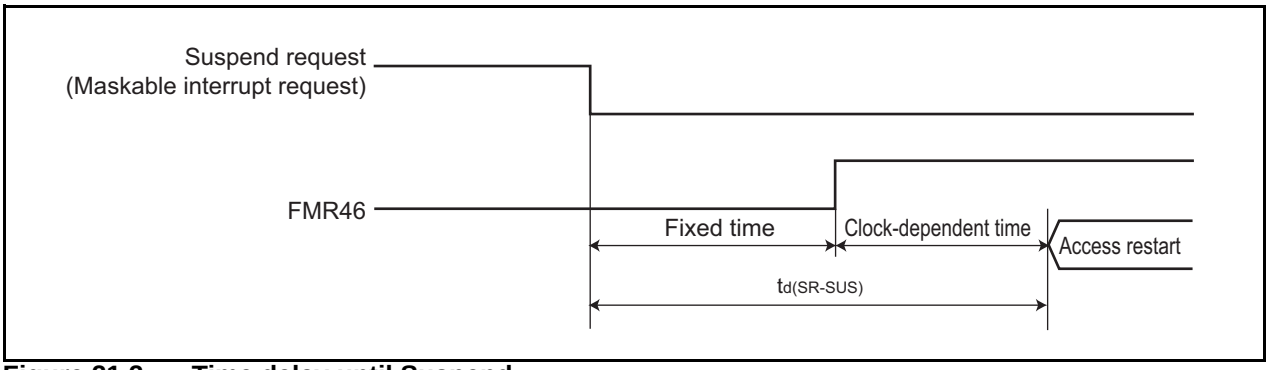


Figure 21.2 Time delay until Suspend

Table 21.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3, 4)		2.70	2.85	3.00	V
$t_{d(Vdet1-A)}$	Voltage monitor 1 reset generation time(5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold $V_{det2} > V_{det1}$.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 21.7 Voltage Detection 2 Circuit Electrical Characteristics

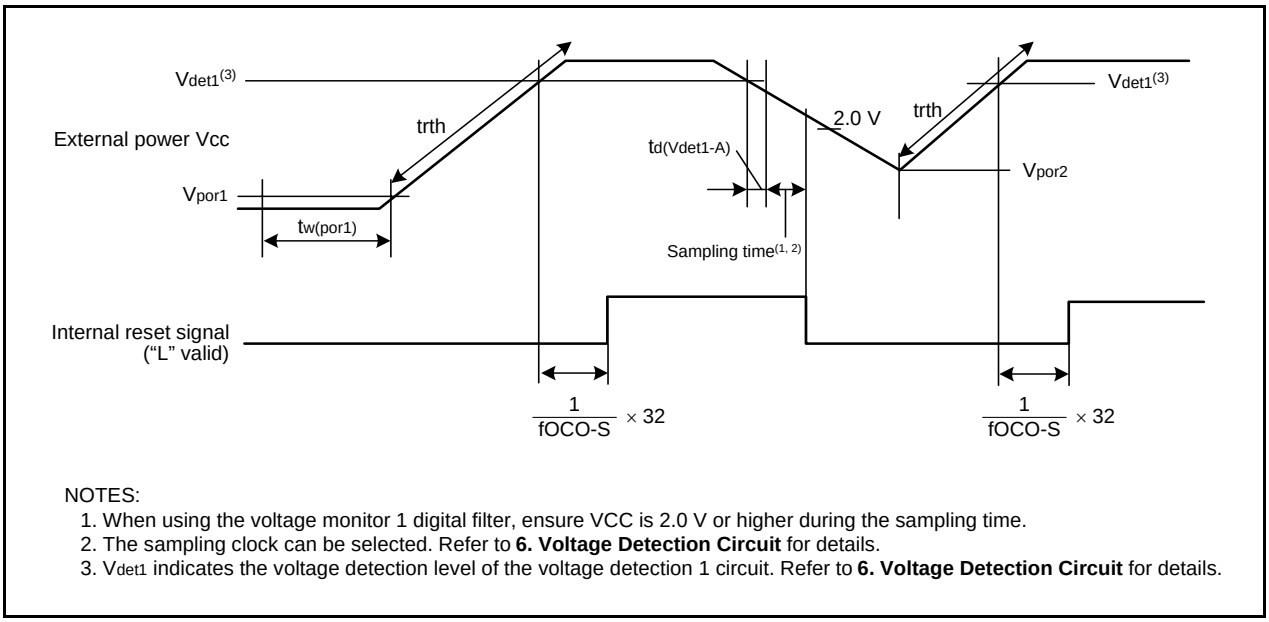
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.3	3.6	3.9	V
$t_{d(Vdet2-A)}$	Voltage monitor 2 reset/interrupt request generation time(2, 5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold $V_{det2} > V_{det1}$.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 21.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	Vdet1	V
trth	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20(2)	–	–	mV/msec
		$V_{CC} > 3.6$ V	20(2)	–	2,000	mV/msec

NOTES:
1. Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30s or more if -20°C ≤ Topr ≤ 125°C, maintain $t_{w(por1)}$ for 3,000s or more if -40°C ≤ Topr < -20°C.



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** for details.

Figure 21.3 Power-on Reset Circuit Electrical Characteristics

Table 21.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V, 0°C ≤ Topr ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 3.0 V to 5.25 V, -20°C ≤ Topr ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 125°C(2)	38.0	40	42.0	MHz
		V_{CC} = 2.7 V to 5.5 V, -40°C ≤ Topr ≤ 125°C(2)	37.6	40	42.4	MHz
–	The value of the FRA1 register when the reset is deasserted		08h	40	F7h	–
–	High-speed on-chip oscillator adjustment range	Adjust the FRA1 register to -1 bit (the value when the reset is deasserted)	–	+ 0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption when high-speed on-chip oscillator oscillating	V_{CC} = 5.0 V, Topr = 25°C	–	600	–	µA

NOTES:
1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. The standard value shows when the reset is deasserted for the FRA1 register.

Table 21.10 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption when low-speed on-chip oscillator oscillating	V_{CC} = 5.0 V, Topr = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.

Table 21.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 21.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1t_{CYC} + 100	ns
t_{OR}	SSI slave out open time			–	–	1t_{CYC} + 100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

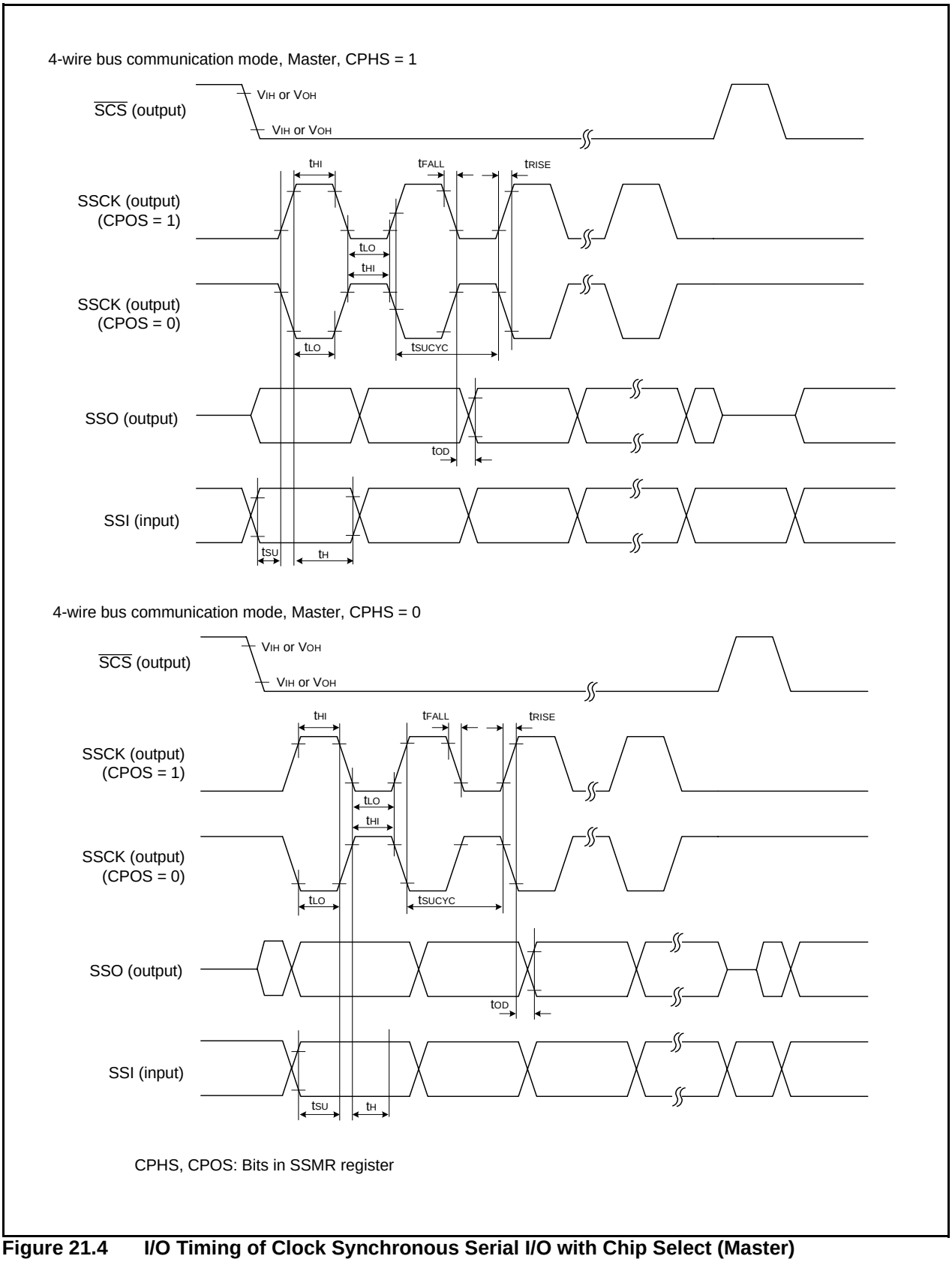


Figure 21.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

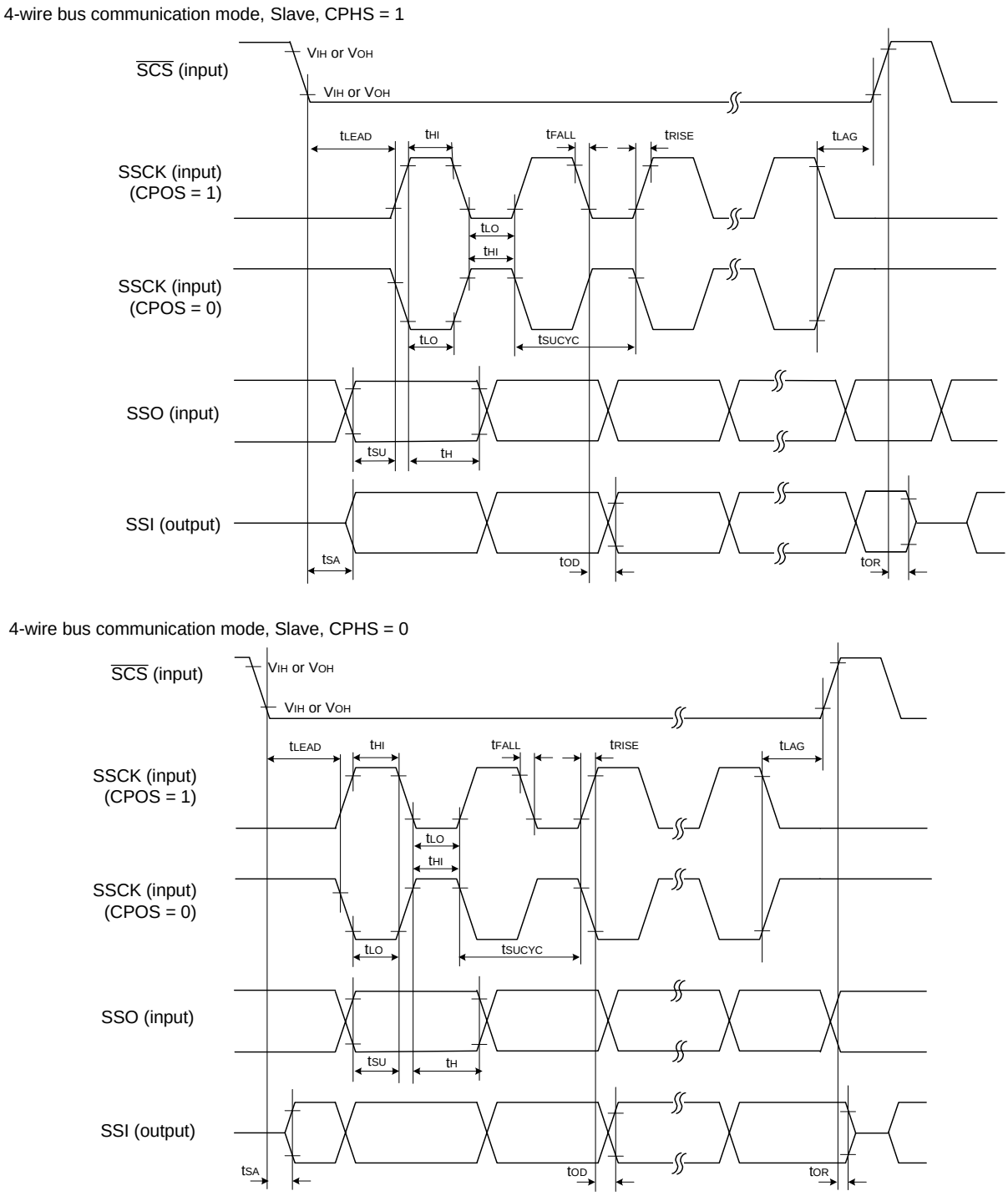


Figure 21.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

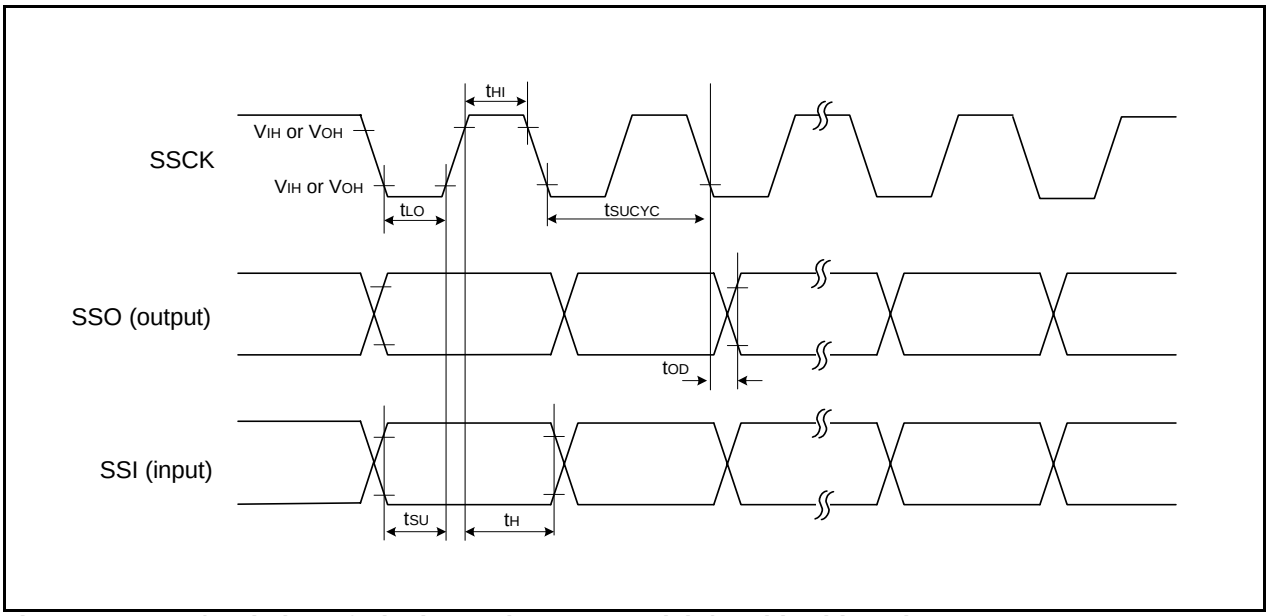
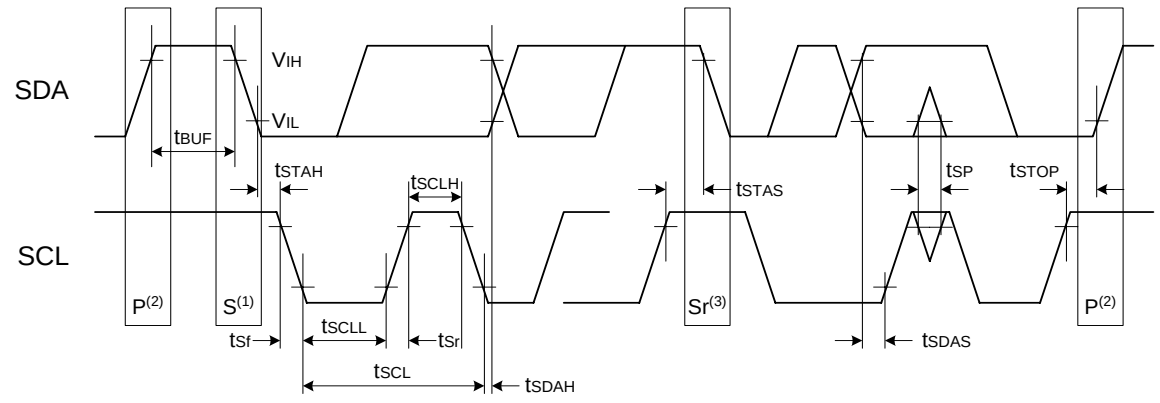


Figure 21.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 21.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 500(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 21.7 I/O Timing of I²C Bus Interface

Table 21.14 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except XOUT	I_{OH} = -5 mA		Vcc – 2.0	–	Vcc	V
			I_{OH} = -200 µA		Vcc – 0.3	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	Vcc – 2.0	–	Vcc	V
			Drive capacity LOW	I_{OH} = -500 µA	Vcc – 2.0	–	Vcc	V
V_{OL}	Output “L” Voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 µA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5 V		–	–	-5.0	µA
R_{PULLUP}	Pull-Up Resistance		VI = 0 V, Vcc = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 21.15 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	12.5	25.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10.0	20.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	6.5	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	13.0	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	150	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	60	120	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	µA

Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 21.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

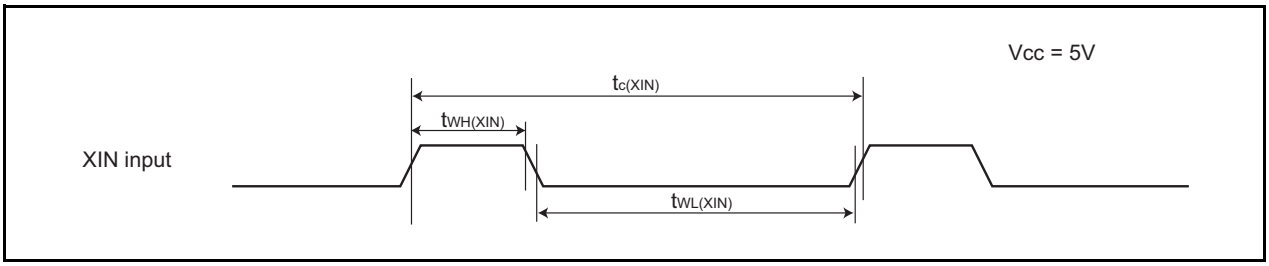


Figure 21.8 XIN Input Timing Diagram when Vcc = 5 V

Table 21.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

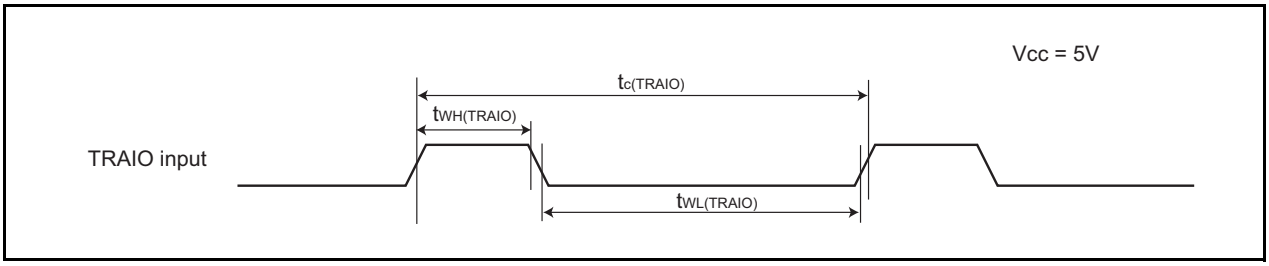


Figure 21.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 21.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

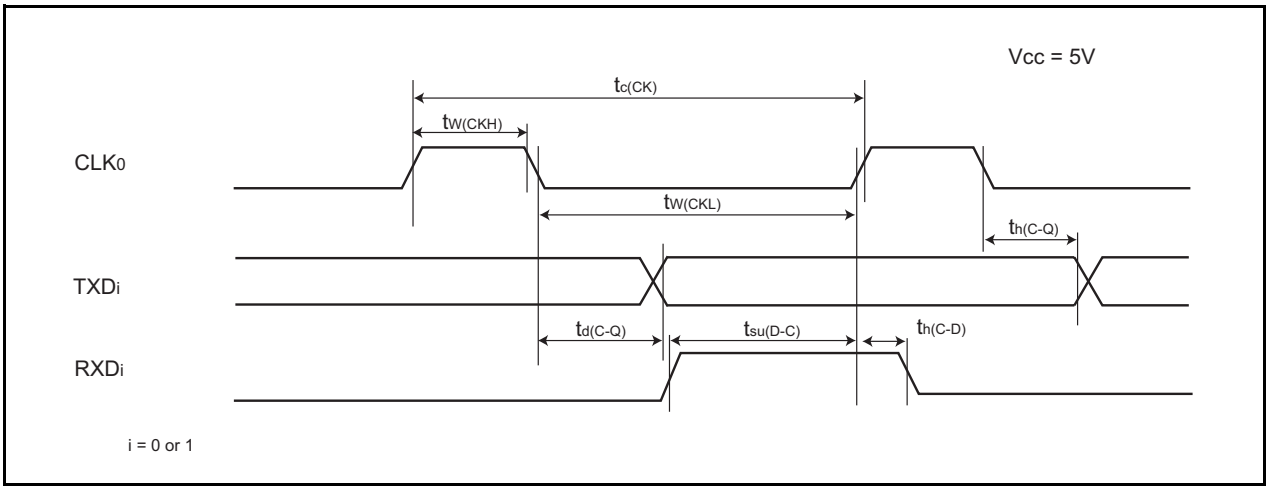


Figure 21.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 21.19 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

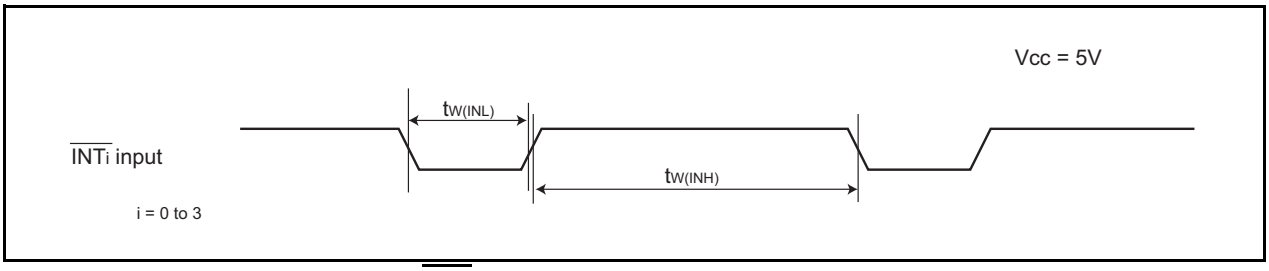


Figure 21.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V (i = 0 to 3)

Table 21.20 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except XOUT	I_{OH} = -1 mA		V_{CC} – 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except XOUT	I_{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, Vcc = 3 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 3 V		–	–	-4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 3 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 2.7 to 3.3 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

Table 21.21 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	11.5	23.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9.5	19.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.0	12.0	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	6.3	12.6	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	145	290	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	56	112	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	35	70	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.7	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.1	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	3.8	–	µA

Timing Requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0V at Topr = 25°C) [Vcc = 3 V]

Table 21.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

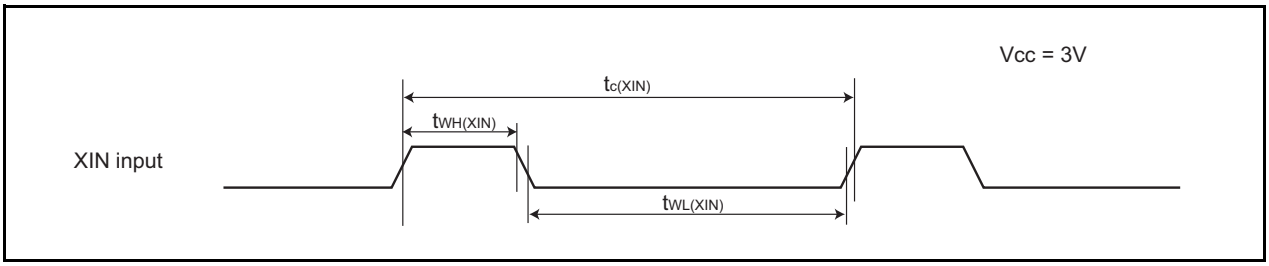


Figure 21.12 XIN Input Timing Diagram when Vcc = 3 V

Table 21.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input Cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

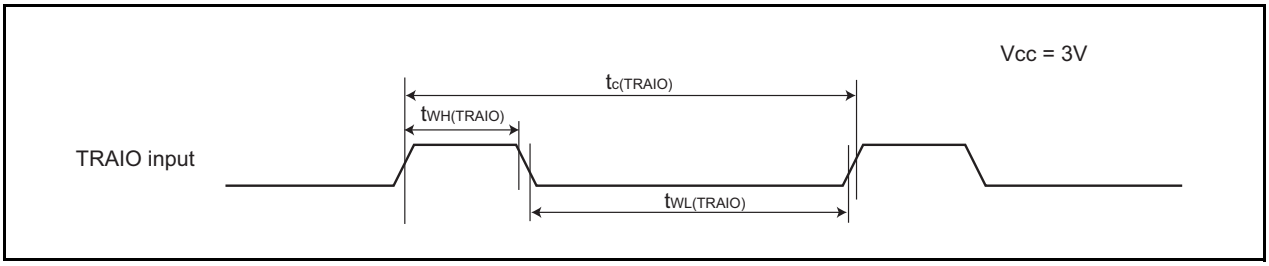


Figure 21.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 21.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

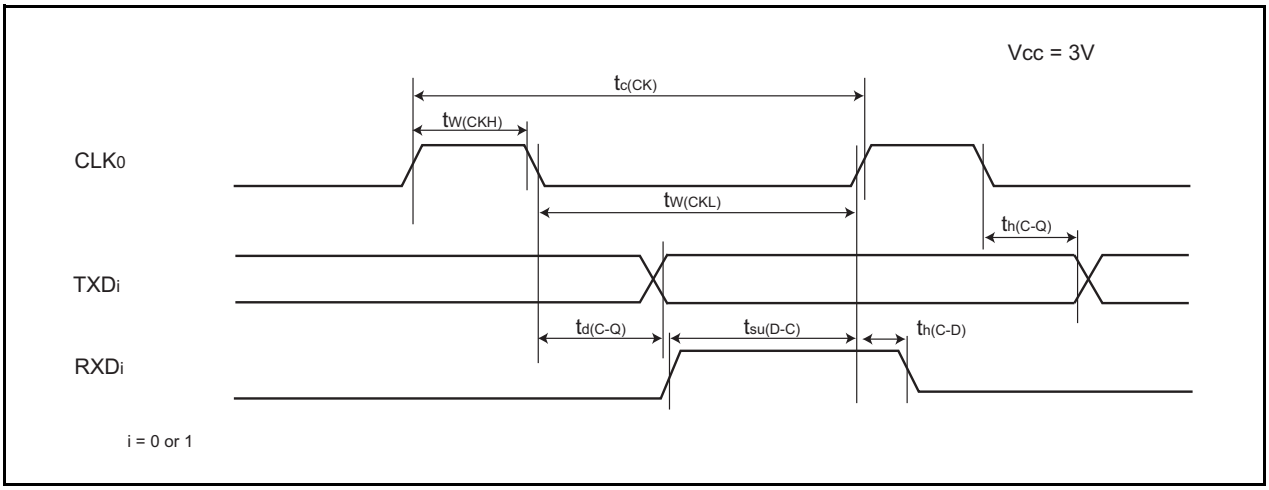


Figure 21.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 21.25 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

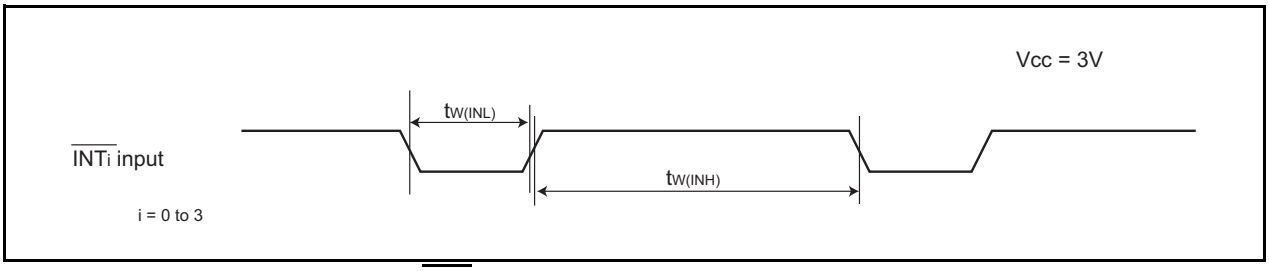


Figure 21.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)

22. Usage Notes

22.1 Notes on Clock Generation Circuit

22.1.1 Stop Mode

When entering stop mode, set the FMR01 bit to “0” (CPU rewrite mode disabled) and the CM10 bit to “1” (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit in the CM1 register to “1” (stop mode) and the program stops. Insert at least 4 NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to “1”.

• Example to enter stop mode

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        BSET    0,PRCR          ; Protect disabled
        FSET    I               ; Enable interrupt
        BSET    0,CM1           ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

22.1.2 Wait Mode

When entering wait mode, set the FMR01 bit to “0” (CPU rewrite mode disabled) and execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

• Example to execute the WAIT instruction

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

22.1.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is less than 2 MHz, set the OCD1 to OCD0 bits to 00b.

22.1.4 Oscillation Circuit Constants

Ask the maker of the oscillator to specify the beat oscillation circuit constants on your system.

22.2 Notes on Interrupts

22.2.1 Reading Address 00000h

Do not read the address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to 0.
If the address 00000h is read in a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause a problem that the interrupt is canceled, or an unexpected interrupt is generated.

22.2.2 SP Setting

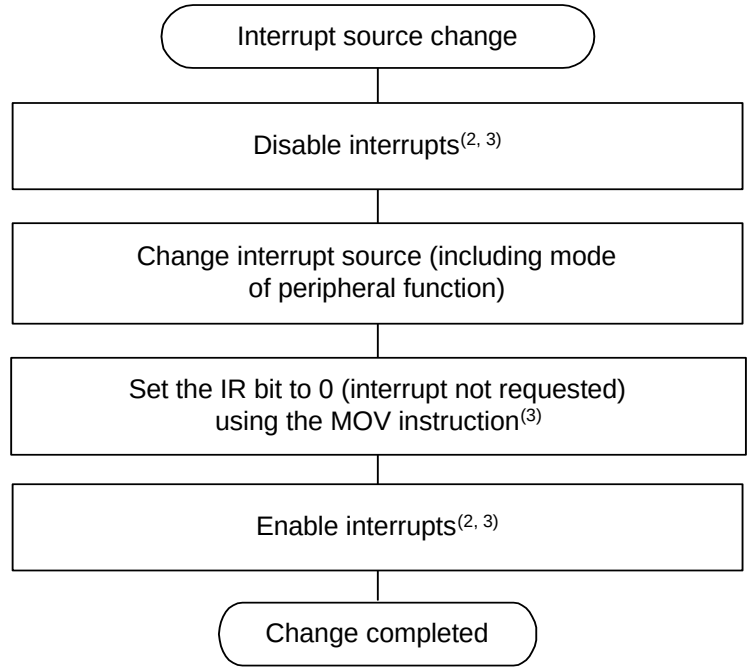
Set any value in the SP before an interrupt is acknowledged. The SP is set to 0000h after reset. Therefore, if an interrupt is acknowledged before setting any value in the SP, the program may run out of control.

22.2.3 External Interrupt and Key Input Interrupt

Either an “L” level or an “H” level of width shown in the Electrical Characteristics is necessary for the signal input to the $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ pins and $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ pins regardless of the CPU clocks. For details, refer to **Table 21.19 External Interrupt INTi (i = 0 to 3) Input**, **Table 21.25 External Interrupt INTi (i = 0 to 3) Input**.

22.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. When using an interrupt, set the IR bit to 0 (no interrupt requested) after changing the interrupt source. In addition, the changes of interrupt sources include all sources that change the interrupt sources assigned to individual software interrupt numbers, polarities, and timing. Therefore, when a mode change of the peripheral functions involves interrupt sources, edge polarities, and timing, Set the IR bit to 0 (no interrupt requested) after the change. Refer to each peripheral function for the interrupts caused by the peripheral functions.
Figure 22.1 shows an Example of Procedure for Changing Interrupt Sources.



IR bit: The interrupt control register bit of an interrupt whose source is changed.

NOTES:
1. Execute the above settings individually. Do not execute two or more settings at once (by one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled. If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 of the interrupt whose source is changed.
3. Refer to **12.6.5 Changing Interrupt Control Register Contents** for the instructions to be used and usage notes.

Figure 22.1 Example of Procedure for Changing Interrupt Sources

22.2.5 Changing Interrupt Control Register Contents

(a) Each interrupt control register can only be changed while interrupt requests corresponding to that register are not generated. If interrupt requests may be generated, disable the interrupts before changing the interrupt control register.

(b) When changing any interrupt control register after disabling interrupts, be careful with the instructions to be used.
When changing any bit other than IR bit
If an interrupt request corresponding to that register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register.
Instructions to use: AND, OR, BCLR, BSET
When changing IR bit
If the IR bit is set to 0 (interrupt not requested), it may not be set to 0 depending on the instruction to be used. Therefore, use the MOV instruction to set the IR bit to 0.

(c) When disabling interrupts using the I flag, set the I flag according to the following sample programs. Refer to (b) for the change of interrupt control registers in the sample programs.

Sample programs 1 to 3 are preventing the I flag from being set to 1 (interrupt enables) before changing the interrupt control register for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag being set to 1 before interrupt control register is changed

```
INT_SWITCH1:
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set TRAIC register to 00h
    NOP                 ;
    NOP
    FSET    I           ; Enable interrupts
```

Example 2: Use dummy read to have FSET instruction wait

```
INT_SWITCH2:
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set TRAIC register to 00h
    MOV.W   MEM,R0      ; Dummy read
    FSET    I           ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set TRAIC register to 00h
    POPC    FLG         ; Enable interrupts
```

22.3 Notes on Timers

22.3.1 Notes on Timer RA

- Timer RA stops counting after reset. Set the value to timer RA and timer RA prescaler before the count starts.
- Even if the prescaler and timer RA is read out in 16-bit units, these registers are read by 1 byte in the MCU. Consequently, the timer value may be updated during the period these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, the TEDGF and TUNDF bits in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged when 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is executed. At the time, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse width measurement mode and pulse period measurement mode from other mode, the contents of the TEDGF and TUNDF bits are indeterminate. Write 0 to the TEDGF and TUNDF bits before the count starts.
- The TEDGF bit may be set to 1 by timer RA prescaler underflow which is generated for the first time since the count starts.
- When using the pulse period measurement mode, leave two periods or more of timer RA prescaler immediately after count starts, and set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count stops.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).
  The TCSTF bit retains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is performing. Timer RA counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, TRA

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

22.3.2 Notes on Timer RB

- Timer RB stops counting after reset. Set the value to timer RB and timer RB prescaler before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read by 1 byte in the MCU. Consequently, the timer value may be updated during the period these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0, 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, read the timer count value in programmable one-shot generation mode and programmable wait one-shot generation mode before the timer stops.
- The TCSTF bit retains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count stops.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.
  The TCSTF bit retains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is performing. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, TRBPR

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

22.3.2.1 Timer mode

The following workaround should be performed in timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

22.3.2.2 Programmable waveform generation mode

The following three workarounds should be performed in programmable waveform generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 22.2 and 22.3.

The following shows the detailed workaround examples.

- Workaround example (a):
  As shown in Figure 22.2, write to registers TRBSC and TRBPR in the timer RB interrupt routine. These write operations must be completed by the beginning of period A.

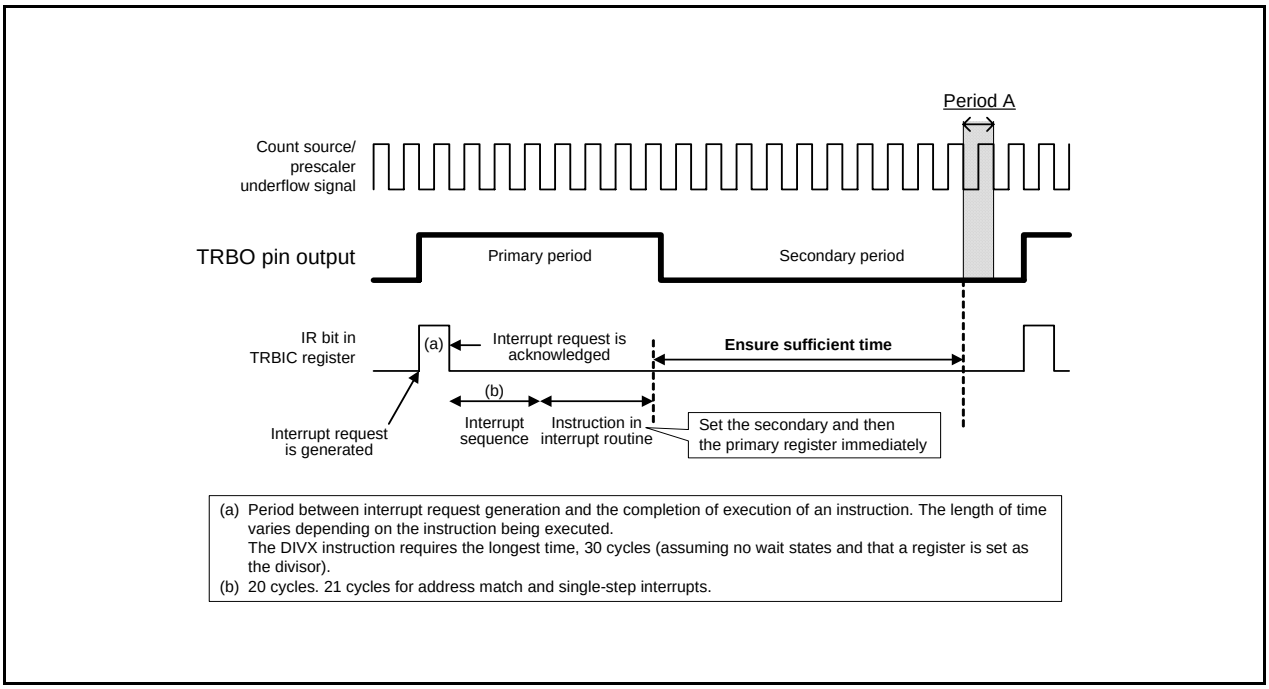


Figure 22.2 Workaround Example (a) When Timer RB Interrupt is Used

• Workaround example (b):
As shown in Figure 22.3 detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. These write operations must be completed by the beginning of period A.
If the port register's bit value is read after the port direction register's bit corresponding to the TRBO pin is set to 0 (input mode), the read value indicates the TRBO pin output value.

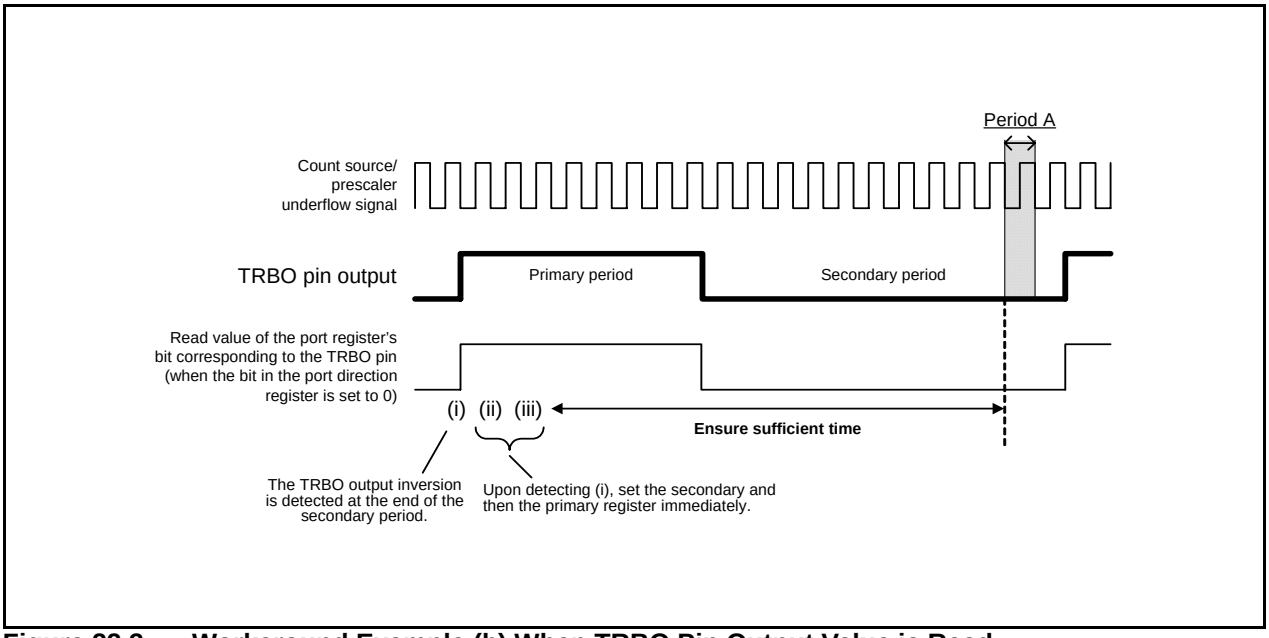


Figure 22.3 Workaround Example (b) When TRBO Pin Output Value is Read

(3) To stop the timer counting in the primary period, use the TSTOP bit in the TRBCR register. In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

22.3.2.3 Programmable one-shot generation mode

The following two workarounds should be performed in programmable one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

• When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

• When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

22.3.2.4 Programmable wait one-shot generation mode

The following three workarounds should be performed in programmable wait one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

(3) Set registers TRBSC and TRBPR using the following procedure.

(a) To use "$\overline{\text{INT0}}$ pin one-shot trigger enabled" as the count start condition
Set the TRBSC register and then the TRBPR register. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before trigger input from the $\overline{\text{INT0}}$ pin.

(b) To use "writing 1 to TOSST bit" as the start condition
Set the TRBSC register, the TRBPR register, and then TOSST bit. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit.

22.3.3 Notes on Timer RD

22.3.3.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.
- When the CSELi (i = 0 or 1) is set to 0 (the count stops at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is set to 0.
  To stop counting by a program, set the TSTARTi bit to 0 after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with 1 instruction), the count cannot be stopped.
- Table 22.1 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji pin with the timer RD output.

Table 22.1 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	Hold the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	Hold the output level after output changes by compare match.

22.3.3.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid to overlap with the timing to set the TRDi register to 0000h, and then write. When the timing to set the TRDi register to 0000h overlaps with the timing to write the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by the CCLR2 to CCLR0 bits in the TRDCRi register.
  - 001b (clear by the TRDi register at the compare match with the TRDGRAi register)
  - 010b (clear by the TRDi register at the compare match with the TRDGRBi register.)
  - 011b (synchronous clear)
  - 101b (clear by the TRDi register at the compare match with the TRDGRCi register.)
  - 110b (clear by the TRDi register at the compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program Example     MOV.W   #XXXXh, TRD0    ;Writing
                    JMP.B   L1              ;JMP.B
                L1: MOV.W   TRD0,DATA       ;Reading
```

22.3.3.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program Example     MOV.B   #XXh, TRDSR0    ;Writing
                    JMP.B   L1              ;JMP.B
                L1: MOV.B   TRDSR0,DATA     ;Reading
```

22.3.3.4 Count Source Switch

- When switching the count source, switch it after the count stops.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change the TCK2 to TCK0 bits in the TRDCRi register.

- When changing the count source from fOCO40M to the other and stopping fOCO40M, wait 2 cycles or more of f1 after setting the clock switch, and then stop fOCO40M.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change the TCK2 to TCK0 bits in the TRDCRi register.
(3) Wait 2 cycles or more of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator stops).

22.3.3.5 Input Capture Function

- Set the pulse width of input capture signal to 3 cycles or more of the Timer RD operation clock. (Refer to **Table 14.11 Timer RD Operation Clocks**.)
- The value in the TRDi register is transferred to the TRDGRji register after 2 to 3 cycles of the Timer RD operation clock since the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C or D) (no digital filter).

22.3.3.6 Reset Synchronous PWM Mode

- When reset synchronous PWM mode is used for motor control, use it with OLS0 = OLS1.
- Set to reset synchronous PWM mode in the following procedure:

Change procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set the CMD1 to CMD0 bits in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set the CMD1 to CMD0 bits to 01b (reset synchronous PWM mode).
(4) Set the registers associated with other Timer RD again.

22.3.3.7 Complementary PWM Mode

- When complementary PWM mode is used for motor control, use it with OLS0 = OLS1.
- Change the CMD1 to CMD0 bits in the TRDFCR register in the following procedure.

Change procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set the CMD1 to CMD0 bits in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode)
(3) Set the DMD1 to CMD0 bits to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other Timer RD again.

Change procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and CSEL1 bits in the TRDSTR register to 0 (count stops).
(2) Set the CMD1 to CMD bits to 00b (other than reset synchronous PWM mode, complementary PWM mode)

- Do not write to the TRDGRA0, TRDGRB0, TRDGRA1 and TRDGRB1 registers during operation. When changing the PWM waveform, transfer the value written to the TRDGRD0, TRDGRC1 and TRDGRD1 registers to the TRDGRB0, TRDGRA1 and TRDGRB1 registers using the buffer operation. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register). The PWM period cannot be changed.

- When the value in the TRDGRA0 register is assumed as m, the TRD0 register counts order of m - 1, m, m + 1, m, m - 1 when changing from increment to decrement.
  When changing from m to m + 1, the IMFA bit is set to 1. Also, the CMD1 to CMD0 bits in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred by the compare match in the TRD0 and TRDGRA0 registers), the content in the buffer register (TRDGRD0, TRDGRC1, TRDGRD1) is transferred to the general register (TRDGRB0, TRDGRA1, TRDGRB1).
  For the order of m + 1, m, m - 1 operation, the IMFA bit remains unchanged and data are not transferred to the register such as the TRDGRA0 register.

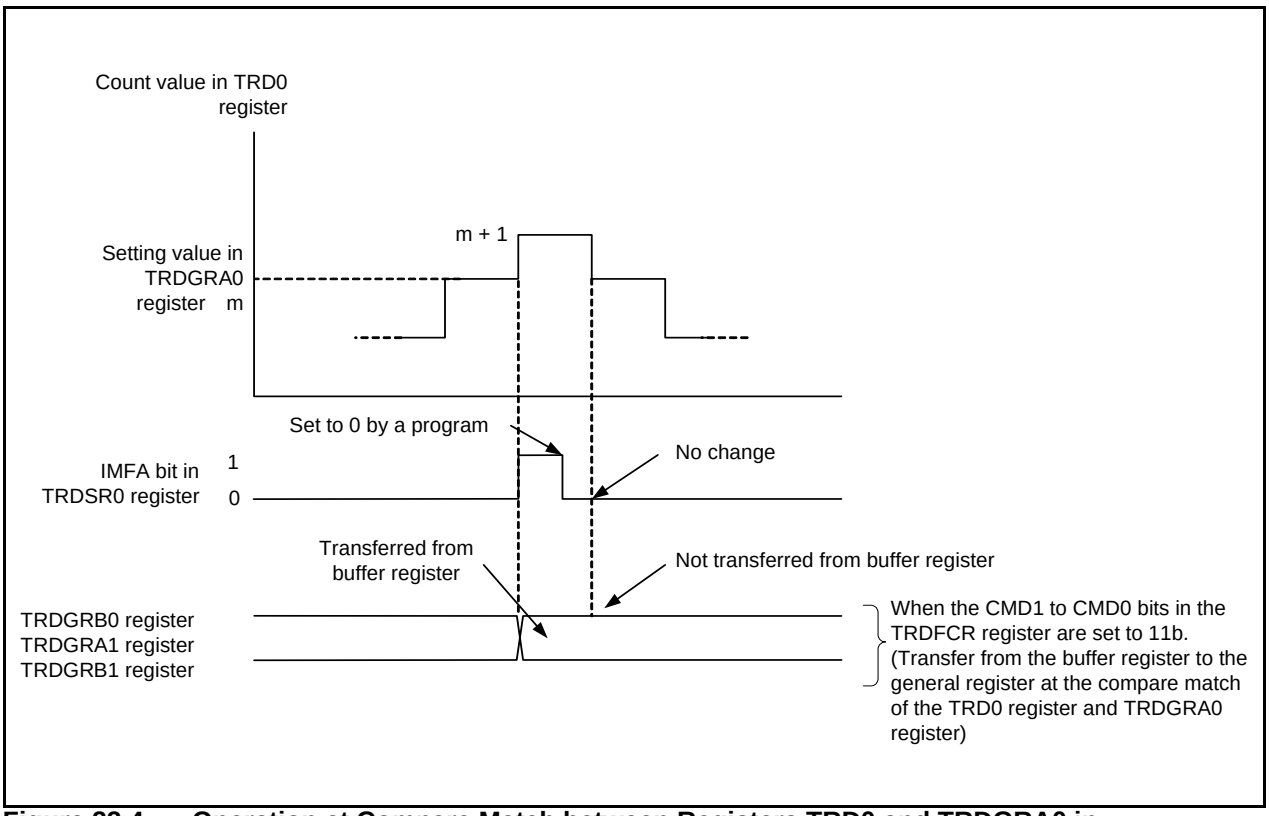


Figure 22.4 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts the order of 1, 0, FFFFh, 0, 1 when changing from decrement to increment. The UDF bit is set to 1 by the order of 1, 0, FFFFh operation. Also, when the CMD1 to CMD0 bits in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred by the underflow in the TRD1 register), the content in the buffer register (TRDGRD0, TRDGRC1, TRDGRD1) is transferred to the general register (TRDGRB0, TRDGRA1, TRDGRB1). For the order of FFFFh, 0, 1 operation, data are not transferred to the register such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

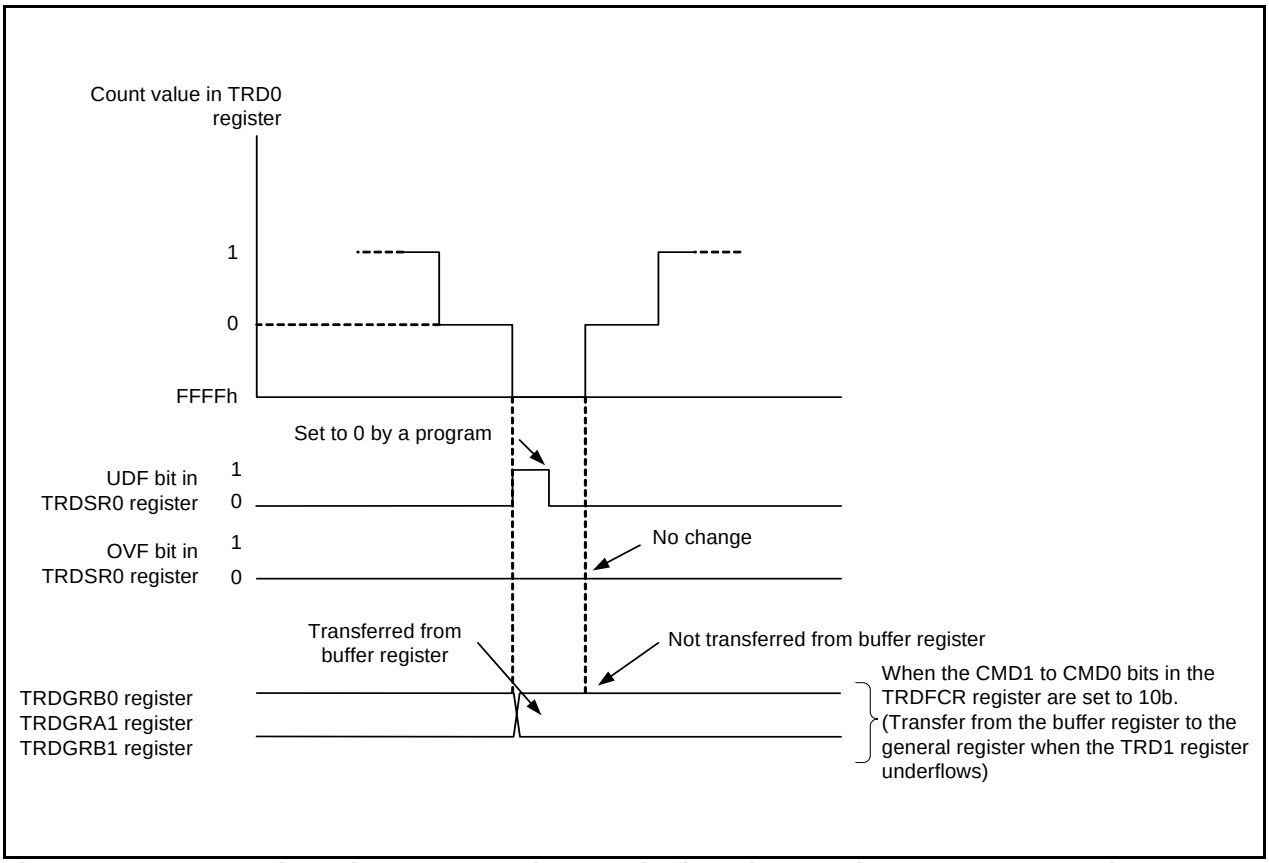
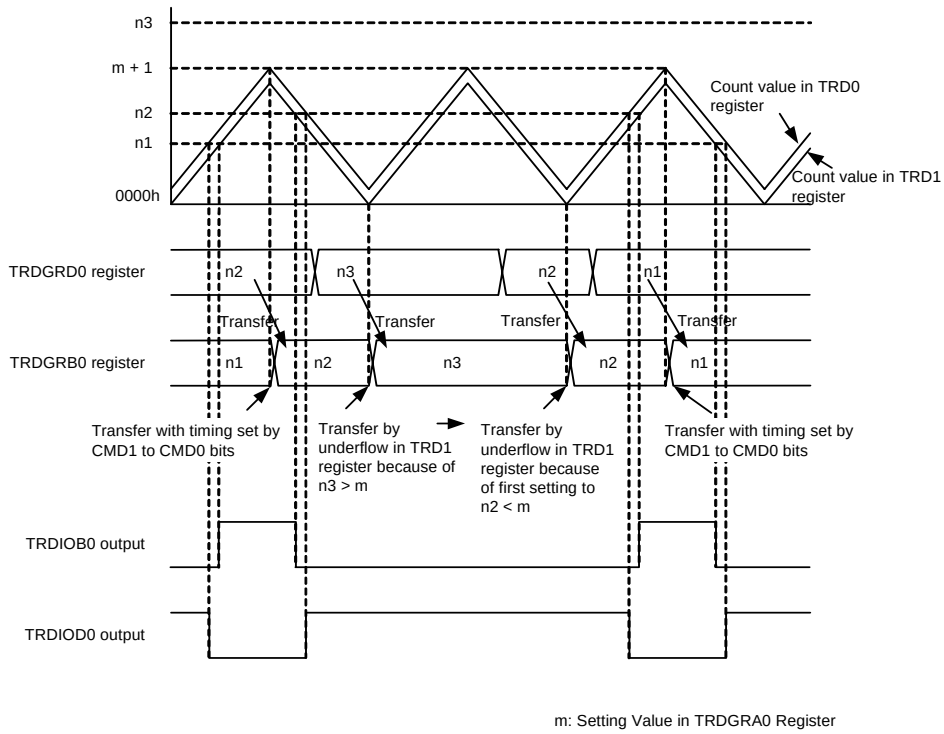


Figure 22.5 Operation When TRD1 Register Underflows in Complementary PWM Mode

- Select with the CMD1 to CMD0 bits for the data transfer timing from the buffer register to the general register. However, transfer with the following timing in spite of the value of the CMD1 to CMD0 bits for the following cases:

  Value in buffer register ≥ Value in TRDGRA0 register:
  Transfer at the underflow in the TRD1 register.
  And then, when setting the buffer register to 0001h or above and the smaller value than the one in the TRDGRA0 register, and the TRD1 register underflows in the fist time after setting, the value is transferred to the general register. After that, transfer the value with the timing selected by the CMD1 to CMD0 bits.



The above applies to the following conditions:
- The CMD1 to CMD0 bits in the TRDFCR register are set to 11b.
  (Data in the buffer register is transferred at the compare match in the TRD0 and TRDGRA0 registers in complementary PWM mode.)
- Both the OSL0 and OLS1 bits in the TRDFCR are set to 1. (active 'H" for normal-phase and counter-phase)

Figure 22.6 Operation When Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode

When the value in the buffer register is set to 0000h:
Transfer by the compare match in the TRD0 and TRDGRA0 registers.
And then, when setting the buffer register to 0001h or above and the smaller value than the one in the TRDGRA0 register, and the compare match in the TRD0 and TRDGRA0 registers in the fist time after setting, the value is transferred to the general register. After that, transfer the value with the timing selected by the CMD1 to CMD0 bits.

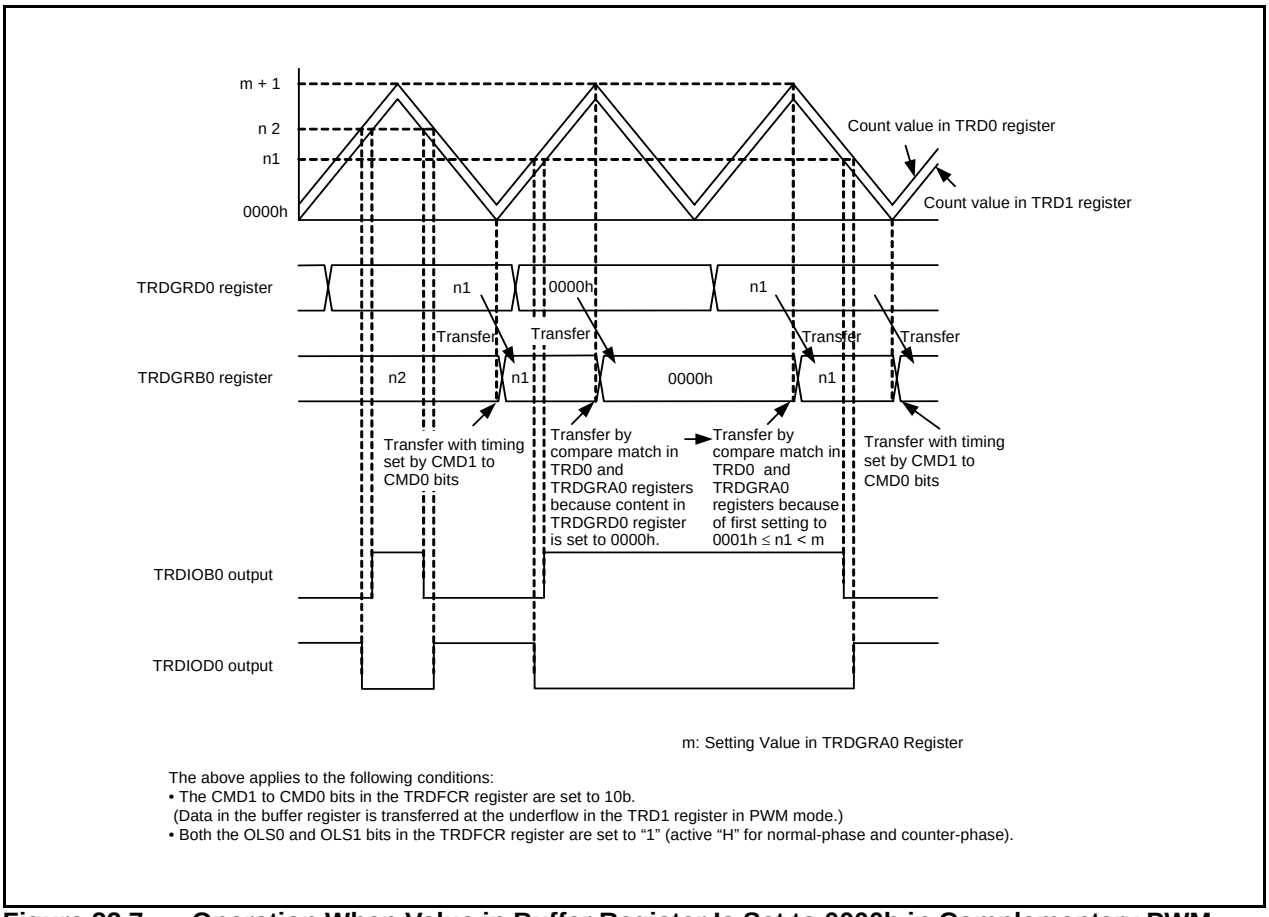


Figure 22.7 Operation When Value in Buffer Register Is Set to 0000h in Complementary PWM Mode

22.3.3.8 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 3.0 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (select fOCO40M as the count source).

22.3.4 Notes on Timer RE

22.3.4.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing count start or stop, and the TCSTF bit which indicates count start or stop. The TSTART and TCSTF bits are in the TRECR1 register.
Timer RE starts counting when setting the TSTART bit to 1 (count starts) and the TCSTF bit is set to 1 (count starts). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with Timer RE(1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with Timer RE: TRESEC, TREMIN, TRECR1, TRECR2, TRECSR

22.3.4.2 Register Setting

Write to the following registers or bits while timer RE stops.

- TRESEC and TRECR2 registers
- The INT bit in TRECR1 register
- RCS0 to RCS2 bits in TRECSR register

The state while Timer RE stops is indicated as the state where the TSTART and TCSTF bits in the TRECR1 register are set to 0 (timer RE stops).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.

22.4 Notes on Serial Interface

- When reading data from the UiRB (i = 0 or 1) register even in the clock asynchronous serial I/O mode or in the clock synchronous serial I/O mode. Ensure to read data in 16-bit unit. When the high-order byte of the UiRB register is read, the PER and FER bits in the UiRB register and the RI bit in the UiC1 register are set to 0. To check receive errors, read the UiRB register and then use the read data.

Example (when reading receive buffer register):

```
MOV.W   00A6H,R0        ; Read the U0RB register
```

- When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, write data high-order byte first, then low-order byte in 8-bit units.

Example (when reading transmit buffer register):

```
MOV.B   #XXH,00A3H  ; Write the high-order byte of U0TB register
MOV.B   #XXH,00A2H  ; Write the low-order byte of U0TB register
```

22.5 Clock Synchronous Serial Interface

22.5.1 Notes on Clock Synchronous Serial I/O with Chip Select

Set the IICSEL bit in the PMR register to 0 (select clock synchronous serial I/O with chip select function) to use the clock synchronous serial I/O with chip select.

22.5.2 Notes on I²C Bus Interface

Set the IICSEL bit in the PMR register to 1 (select I²C bus interface function) to use I²C bus interface.

22.5.2.1 Multimaster Operation

The following actions must be performed to use the I²C bus interface in multimaster operation.

- Transfer rate
  Set the transfer rate by 1/1.8 or faster than the fastest rate of the other masters. For example, if the fastest transfer rate of the other masters is set to 400 kbps, the I²C-bus transfer rate in this MCU should be set to 223 kbps (= 400/1.18) or more.

- Bits MST and TRS in the ICCR1 register setting

(a) Use the MOV instruction to set bits MST and TRS.
(b) When arbitration is lost, confirm the contents of bits MST and TRS. If the contents are other than the MST bit set to 0 and the TRS bit set to 0 (slave receive mode), set the MST bit to 0 and the TRS bit to 0 again.

22.5.2.2 Master Receive Mode

Either of the following actions must be performed to use the I²C bus interface in master receive mode.

(a) In master receive mode while the RDRF bit in the ICSR register is set to 1, read the ICDRR register before the rising edge of the 8th clock.
(b) In master receive mode, set the RCVD bit in the ICCR1 register to 1 (disables the next receive operation) to perform 1-byte communications.

22.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with respect to a Synch Break detection interrupt as the starting point.

22.7 Notes on CAN Module

22.7.1 Reading C0STR Register

The CAN module updates the status of the C0STR register in a certain period. When the CPU and the CAN module access to the C0STR register at the same time, the CPU has the access priority; the access from the CAN module is disabled. Consequently, when the updating period of the CAN module matches the access period from the CPU, the status of the CAN module cannot be updated. (See Figure 22.8)
Accordingly, be careful about the following points so that the access period from the CPU should not match the updating period of the CAN module:

- There should be a wait time of 3fCAN or longer (see Table 22.2) before the CPU reads the C0STR register. (See Figure 22.9)
- When the CPU polls the C0STR register, the polling period must be 3fCAN or longer. (See Figure 22.10)

Table 22.2 CAN Module Status Updating Period

3 fCAN Period = 3 x XIN (Original Oscillation Period) x Division Value of CAN Clock (CCLK)	
(Example 1) Condition XIN 16 MHz CCLK: Divided by 1	3 fCAN period = 3 x 62.5 ns x 1 = 187.5 ns
(Example 2) Condition XIN 16 MHz CCLK: Divided by 2	3 fCAN period = 3 x 62.5 ns x 2 = 375 ns
(Example 3) Condition XIN 16 MHz CCLK: Divided by 4	3 fCAN period = 3 x 62.5 ns x 4 = 750 ns
(Example 4) Condition XIN 16 MHz CCLK: Divided by 8	3 fCAN period = 3 x 62.5 ns x 8 = 1.5 μs
(Example 5) Condition XIN 16 MHz CCLK: Divided by 16	3 fCAN period = 3 x 62.5 ns x 16 = 3 μs

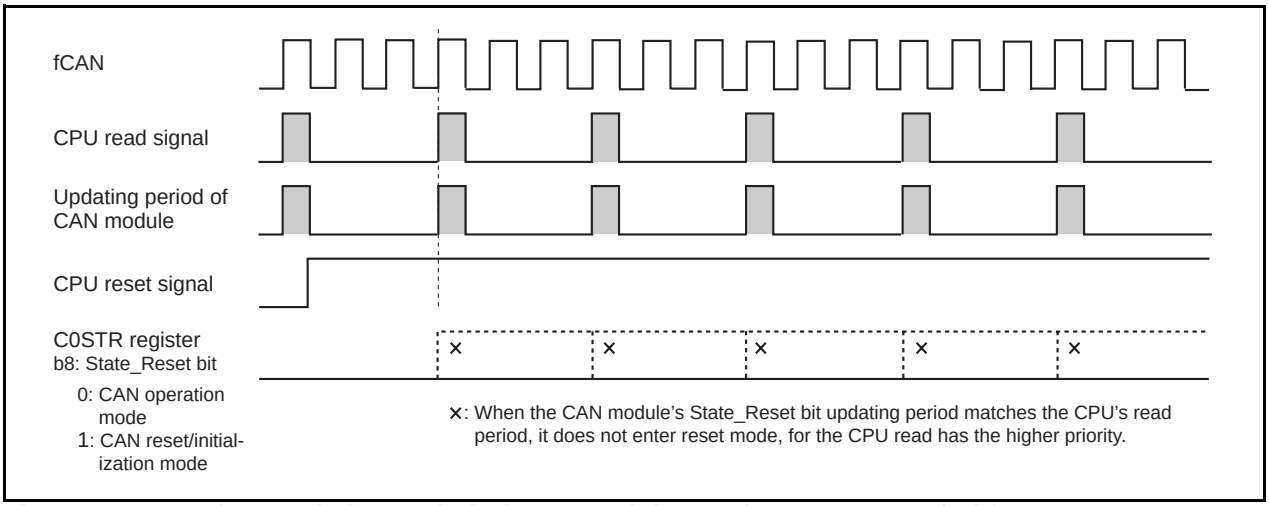


Figure 22.8 When Updating Period of CAN Module Matches Access Period from CPU

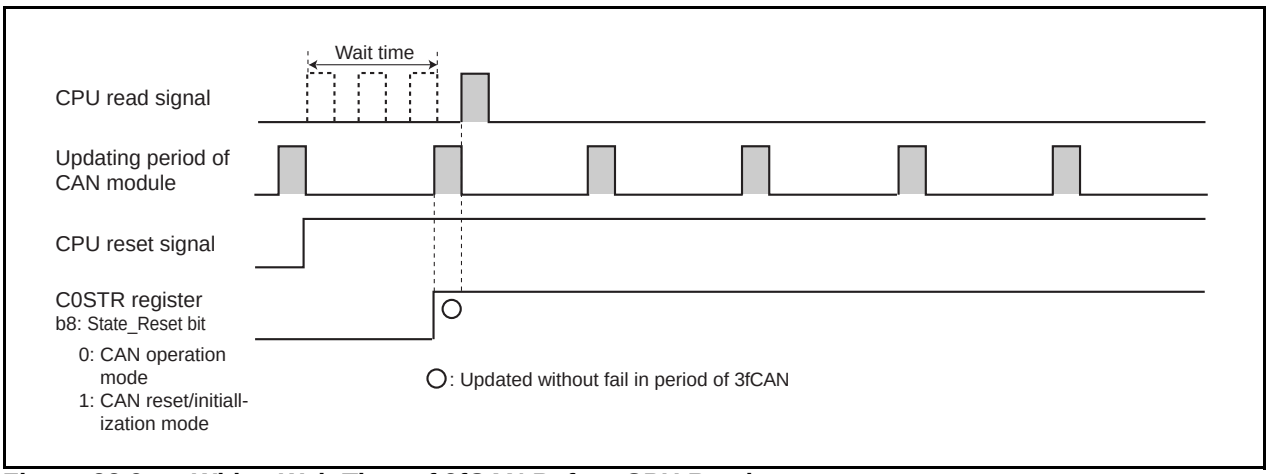


Figure 22.9 With a Wait Time of 3fCAN Before CPU Read

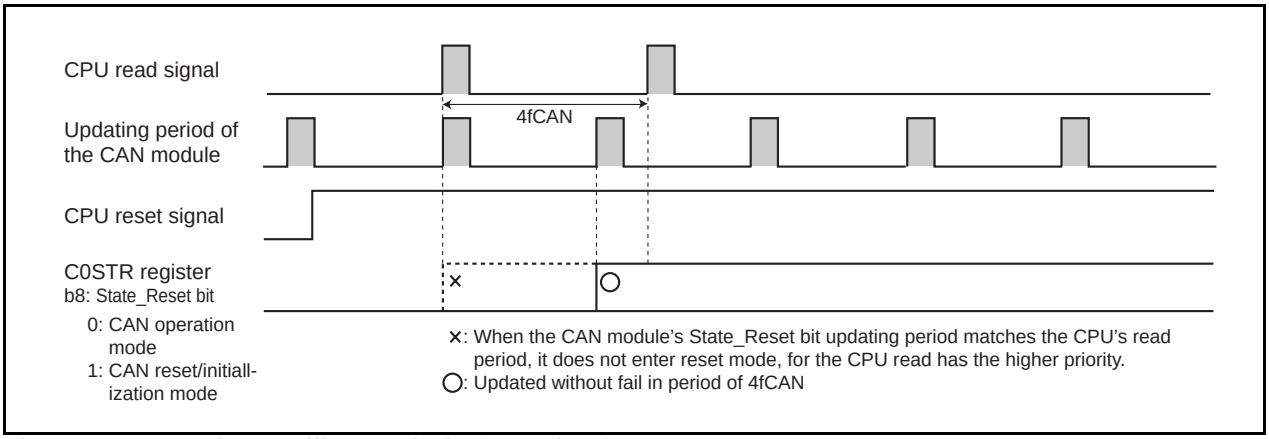


Figure 22.10 When Polling Period of CPU is 3fCAN or Longer

22.7.2 Performing CAN Configuration

If the Reset bit in the C0CTLR register is changed from 0 (operation mode) to 1 (reset/initialization mode) in order to place the CAN module from CAN operation mode into CAN reset/initialization mode, always be sure to check that the State_Reset bit in the C0STR register is set to 1 (reset mode).
Similarly, if the Reset bit is changed from 1 to 0 in order to place the CAN module from CAN reset/initialization mode into CAN operation mode, always be sure to check that the State_Reset bit is set to 0 (operation mode).
The procedure is described below.

To place CAN Module from CAN Operation Mode into CAN Reset/Initialization Mode

- Change the Reset bit from 0 to 1.
- Check that the State_Reset bit is set to 1.

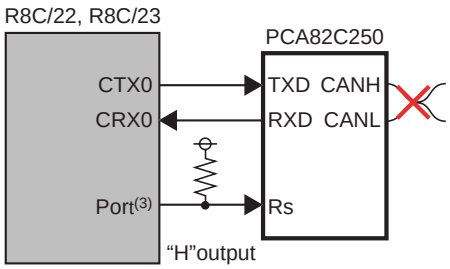
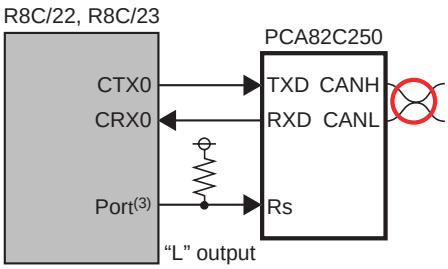
To place CAN Module from CAN Reset/Initialization Mode into CAN Operation Mode

- Change the Reset bit from 1 to 0.
- Check that the State_Reset bit is set to 0.

22.7.3 Suggestions to Reduce Power Consumption

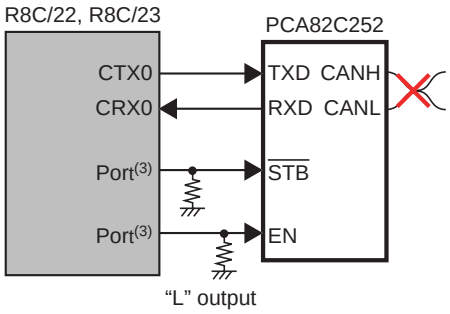
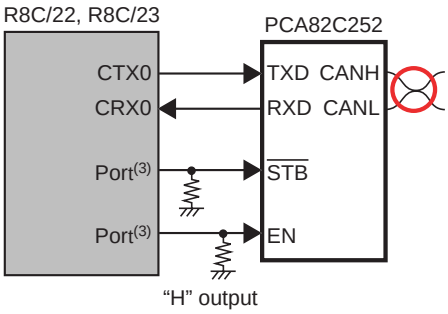
When not performing CAN communication, the operation mode of CAN transceiver should be set to “standby mode” or “sleep mode”.
When performing CAN communication, the power consumption in CAN transceiver in not performing CAN communication can be substantially reduced by controlling the operation mode pins of CAN transceiver.
Table 22.3 and Table 22.4 show Recommended Pin Connections.

Table 22.3 Recommended Pin Connections (In Case of PCA82C250: Philips Product)

	Standby Mode	High-speed Mode
Rs Pin(1)	“H”	“L”
Power Consumption in CAN Transceiver(2)	less than 170 μA	less than 70 mA
CAN Communication	impossible	possible
Connection		

NOTES:
1. The pin which controls the operation mode of CAN transceiver.
2. In case of Topr = 25°C
3. Connect to enabled port to control CAN transceiver.

Table 22.4 Recommended Pin Connections (In Case of PCA82C252: Philips Product)

	Sleep Mode	Normal Operation Mode
$\overline{\text{STB}}$ Pin(1)	“L”	“H”
EN Pin(1)	“L”	“H”
Power Consumption in CAN Transceiver(2)	less than 50 μA	less than 35 mA
CAN Communication	impossible	possible
Connection		

NOTES:
1. The pin which controls the operation mode of CAN transceiver.
2. In case of Topr = 25°C
3. Connect to enabled port to control CAN transceiver.

22.8 Notes on A/D Converter

- Write to each bit (other than bit 6) in the ADCON0 register, each bit in the ADCON1 register, or the SMP bit in the ADCON2 register when the A/D conversion stops (before a trigger occurs).
  When the VCUT bit in the ADCON1 register is changed from 0 (VREF not connected) to 1 (VREF connected), wait for at least 1 μs or longer before the A/D conversion starts.
- When changing A/D operating mode, select an analog input pin again.
- When using in one-shot mode. Ensure that the A/D conversion is completed and read the AD register. The IR bit in the ADIC register or the ADST bit in the ADCON0 register can determine whether the A/D conversion is completed.
- When using the repeat mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select the fOCO-F for the ϕAD.
- If setting the ADST bit in the ADCON0 register to 0 (A/D conversion stops) by a program and the A/D conversion is forcibly terminated during the A/D conversion operation, the conversion result of the A/D converter will be indeterminate. If the ADST bit is set to 0 by a program, do not use the value of AD register.
- Connect 0.1 μF capacitor between the P4_2/VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode when the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode) during A/D conversion.

22.9 Notes on Flash Memory

22.9.1 CPU Rewrite Mode

22.9.1.1 Operating Speed

Before entering CPU rewrite mode (EW0 mode), select 5 MHz or below for the CPU clock using the CM06 bit in the CM0 register and the CM16 to CM17 bits in the CM1 register. This usage note is not needed for EW1 mode.

22.9.1.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because the flash memory internal data is referenced: UND, INTO, and BRK instructions.

22.9.1.3 Interrupts

Table 22.5 lists the EW0 Mode Interrupts and Table 22.6 lists the EW1 Mode Interrupts.

Table 22.5 EW0 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection and Voltage Monitor 2 Interrupt Request are Acknowledged
EW0	During automatic erasing	Any interrupt can be used by allocating a vector to RAM	Once an interrupt request is acknowledged, the auto-programming or auto-erasing is forcibly stopped immediately and resets the flash memory. An interrupt process starts after the fixed period and the flash memory restarts. Since the block during the auto-erasing or the address during the auto-programming is forcibly stopped, the normal value may not be read. Execute the auto-erasing again and ensure the auto-erasing is completed normally. Since the watchdog timer does not stop during the command operation, the interrupt request may be generated. Reset the watchdog timer regularly.
	Automatic writing		

NOTES:
1. Do not use the address match interrupt while the command is executed because the vector of the address match interrupt is allocated on ROM.
2. Do not use the non-maskable interrupt while block 0 is automatically erased because the fixed vector is allocated block 0.

Table 22.6 EW1 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection and Voltage Monitor 2 Interrupt Request are Acknowledged
EW1	During automatic erasing (erase-suspend function is enabled)	The auto-erasing is suspended after td(SR-SUS) and the interrupt process is executed. The auto-erasing can be restarted by setting the FMR41 bit in the FMR4 register to 0 (erase restart) after the interrupt process completes.	Once an interrupt request is acknowledged, the auto-programming or auto-erasing is forcibly stopped immediately and resets the flash memory. An interrupt process starts after the fixed period and the flash memory restarts. Since the block during the auto-erasing or the address during the auto-programming is forcibly stopped, the normal value may not be read. Execute the auto-erasing again and ensure the auto-erasing is completed normally. Since the watchdog timer does not stop during the command operation, the interrupt request may be generated. Reset the watchdog timer regularly using the erase-suspend function.
	During automatic erasing (erase-suspend function is disabled)	The auto-erasing has a priority and the interrupt request acknowledgement is waited. The interrupt process is executed after the auto-erasing completes.	
	During automatic programming (program suspend function enabled)	The auto-programming is suspended after td(SR-SUS) and the interrupt process is executed. The auto-programming can be restarted by setting the FMR42 bit in the FMR4 register to 0 (program restart) after the interrupt process completes.	
	Auto programming (program suspend function disabled)	The auto-programming has a priority and the interrupt request acknowledgement is waited. The interrupt process is executed after the auto-programming completes.	

NOTES:
1. Do not use the address match interrupt while the command is executed because the vector of the address match interrupt is allocated on ROM.
2. Do not use the non-maskable interrupt while block 0 is automatically erased because the fixed vector is allocated block 0.

22.9.1.4 How to Access

Write 0 to the corresponding bits before writing 1 when setting the FMR01, FMR02, or FMR11 bit to 1. Do not generate an interrupt between writing 0 and 1.

22.9.1.5 Rewriting User ROM Area

In EW0 mode, if the power supply voltage drops while rewriting any block in which the rewrite control program is stored, the flash memory may not be able to be rewritten because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

22.9.1.6 Program

Do not write additions to the already programmed address.

22.9.1.7 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

22.10 Notes on Noise

22.10.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect the bypass capacitor (at least 0.1 μF) using the shortest and thickest as possible.

22.10.2 Countermeasures against Noise Error of Port Control Registers

During severe noise testing, mainly power supply system noise, and introduction of external noise, the data of port related registers may be changed.
As a firmware countermeasure, it is recommended to periodically reset the port registers, port direction registers and pull-up control registers. However, examine fully before introducing the reset routine as conflicts may be created between this reset routine and interrupt routines.

23. Notes on On-Chip Debugger

When using the on-chip debugger to develop the R8C/22 and R8C/23 Groups program and debug, pay the following attention.

(1) Do not access the registers associated with UART1.
(2) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(3) Do not set the address match interrupt (registers AIER, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(4) Do not use the BRK instruction in a user system.

Connecting and using the on-chip debugger has some peculiar restrictions. Refer to each on-chip debugger manual for on-chip debugger details.

24. Notes on Emulator Debugger

When using the emulator debugger to develop the R8C/22 and R8C/23 Groups program and debug, pay the following attention.

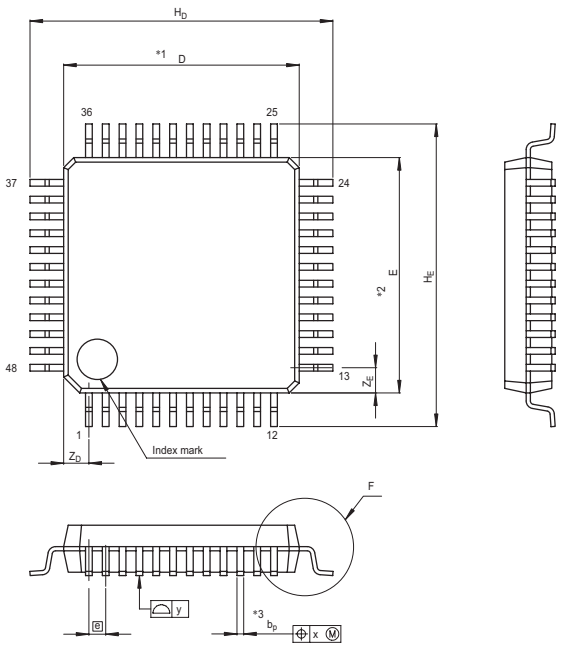
(1) Do not use the following flash memory areas because these areas are used for the emulator debugger.
When debugging of these areas, intensive evaluation on the real chip is required.
ROM 128 KB Product (R5F2122CJFP, R5F2122CKFP, R5F2123CJFP, R5F2123CKFP) addresses 20000h to 23FFFh

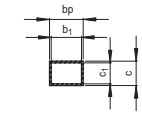
Connecting and using the emulator debugger has some peculiar restrictions. Refer to each emulator debugger manual for emulator debugger details.

Appendix 1. Package Dimensions

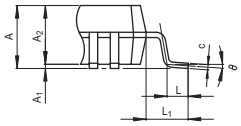
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



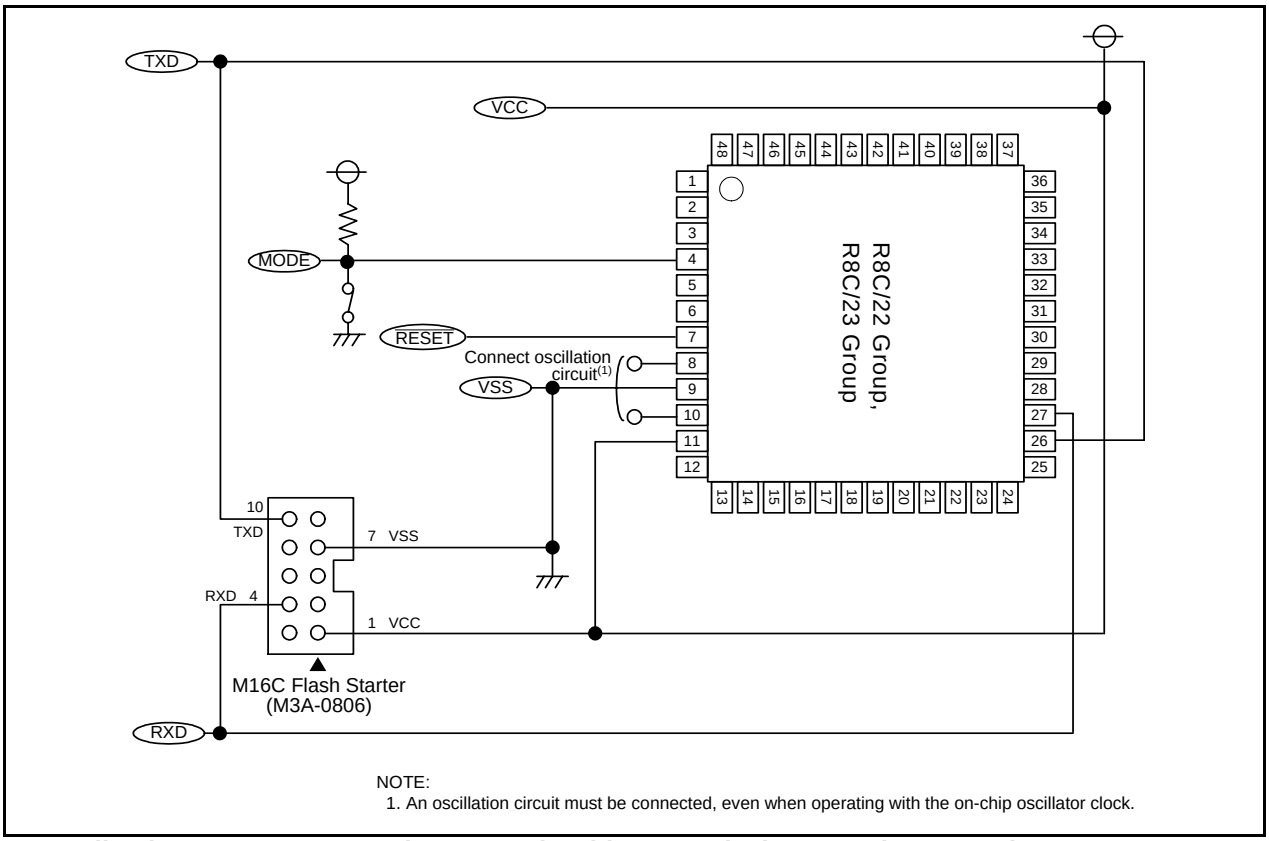
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

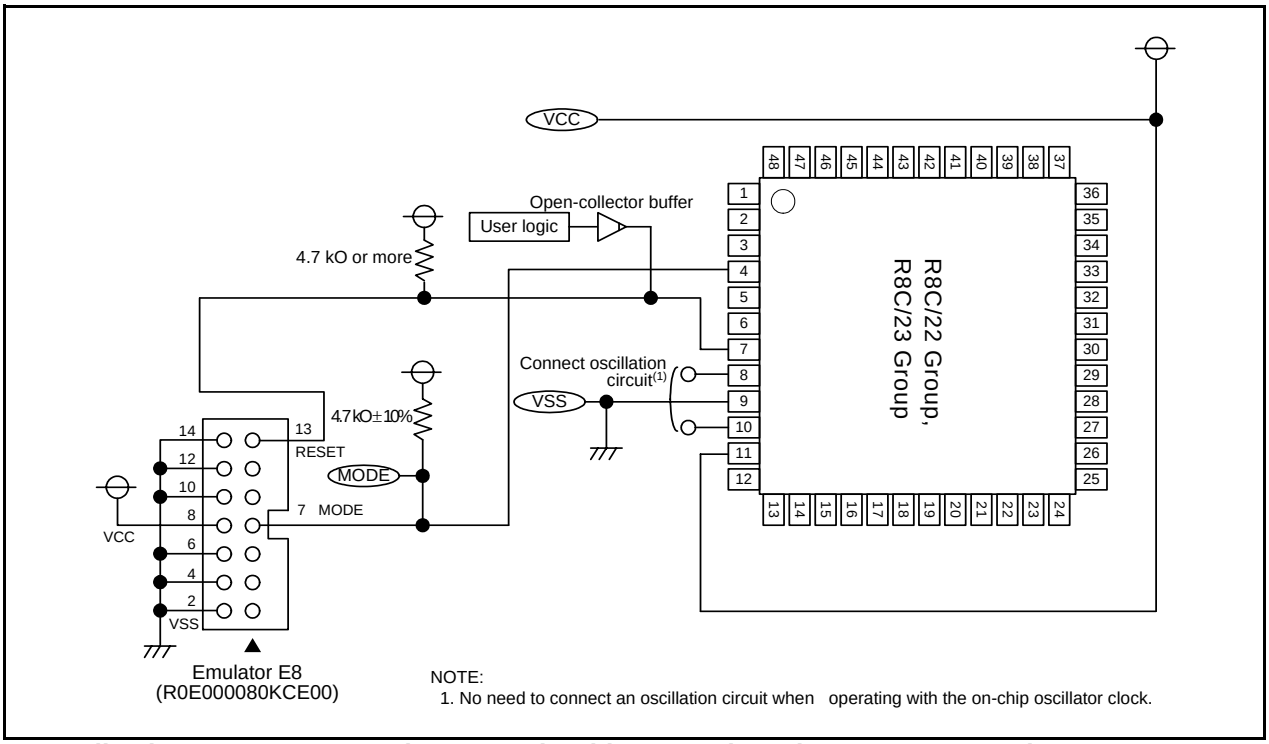
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Appendix 2. Connection Examples between Serial Writer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows the Connection Example with M16C Flash Starter (M3A-0806) and Appendix Figure 2.2 shows the Connection Example with E8 Emulator (R0E000080KCE00).



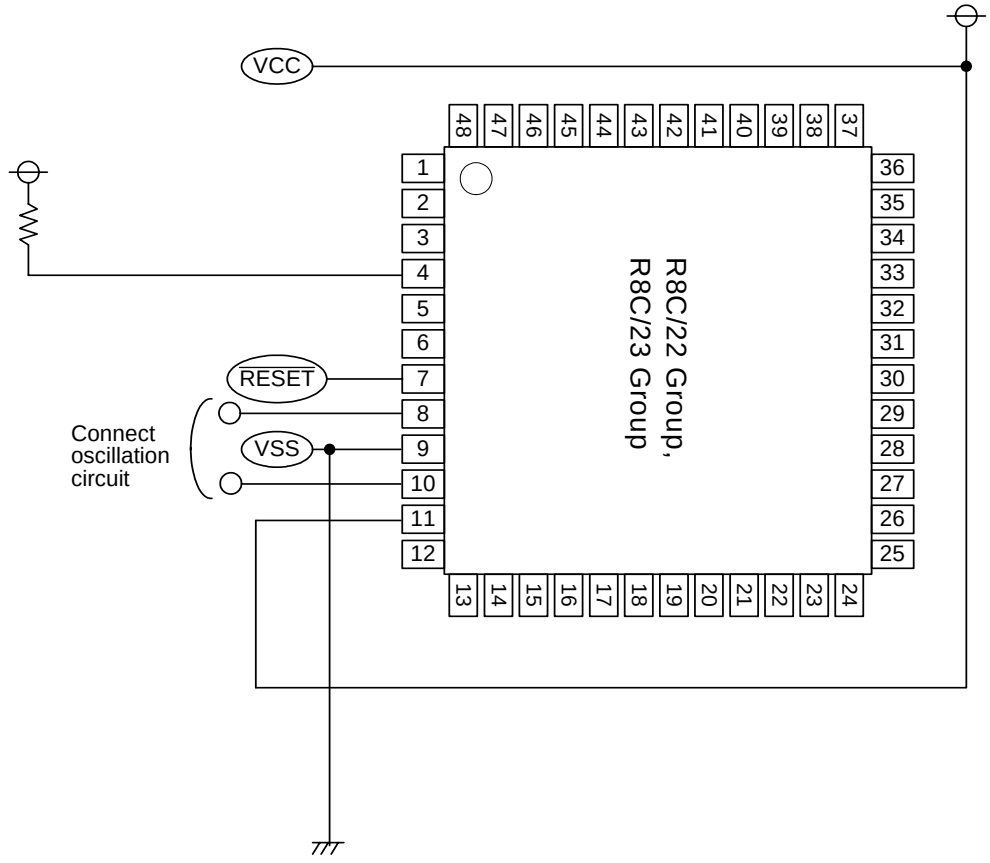
Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)



Appendix Figure 2.2 Connection Example with E8 Emulator (R0E000080KCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows the Example of Oscillation Evaluation Circuit.



NOTE:
1. After reset, the XIN clock stops. Write a program to oscillate the XIN clock.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

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Rev.	Date	Description	
		Page	Summary
0.10	Sep 29, 2005	–	First Edition issued
0.20	Jun 28, 2006	All pages	• Symbol name revised. "SSUAIC" → "SSUIC", "IIC2AIC" → "IICIC", "TRDMDR" → "TRDMR" • Bit Symbol name revised. "TSTOP0" → "CSEL0" in the TRDSTR register "TSTOP1" → "CSEL1" in the TRDSTR register "TPSC0" → "TCK0" in the TRDCRi register (i=0 or 1) "TPSC1" → "TCK1" in the TRDCRi register (i=0 or 1) "TPSC2" → "TCK2" in the TRDCRi register (i=0 or 1) • Pin name revised. "TCLK" → "TRDCLK" • Register name revised. "Timer RE Comparison Reigster" → "Timer RE Compare Data Register"
		1	1. Overview, on the 5th and 6th lines; "data flash" added.
		2	Table 1.1 Functions and Specifications for R8C/22 Group revised
		3	Table 1.2 Functions and Specifications for R8C/23 Group revised
		4	Figure 1.1 Block Diagram; "System Clock Generation" → "System clock generation circuit" revised
		5	Table 1.3 Product Information of R8C/22 Group revised. Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group revised.
		6	Table 1.4 Product Information of R8C/23 Group revised Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group revised.
		7	Figure 1.4 Pin Assignments (Top View); "TCLK" → "TRDCLK" revised
		8	Table 1.5 Pin Functions; "Analog Power Supply Input" revised
		9	Table 1.6 Pin Name Information by Pin Number revised. NOTE added.
		11	2.8.1 Carry Flag (C) "2.8.1 Carry Flag (C Flag)" → "2.8.1 Carry Flag (C)" revised. 2.8.2 Debug Flag (D) "2.8.2 Debug Flag (D Flag)" → "2.8.2 Debug Flag (D)" revised. 2.8.3 Zero Flag (Z) "2.8.3 Zero Flag (Z Flag)" → "2.8.3 Zero Flag (Z)" revised. 2.8.4 Sign Flag (S) "2.8.4 Sign Flag (S Flag)" → "2.8.4 Sign Flag (S)" revised. 2.8.5 Register Bank Select Flag (B) "2.8.5 Rgister Bank Select Flag (B Flag)" → "2.8.5 Register Bank Select Flag (B)" revised. 2.8.6 Overflow Flag (O) "2.8.6 Overflow Flag (O Flag)" → "2.8.6 Overflow Flag (O)" revised.

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		Page	Summary
0.20	Jun 28, 2006	12	2.8.7 Interrupt Enable Flag (I) "2.8.7 Interrupt Enable Flag (I Flag)" → "2.8.7 Interrupt Enable Flag (I)" revised. 2.8.8 Stack Pointer Select Flag (U) "2.8.8 Stack Pointer Select Flag (U Flag)" → "2.8.8 Stack Pointer Select Flag (U)" revised. 2.8.10 Reserved Bit "2.8.10 Reserved Area" → "2.8.10 Reserved Bit" revised.
		13	Figure 3.1 Memory Map of R8C/22 Group; "Internal ROM" → "Internal ROM (program ROM)" revised Address "1ZZZZh" added. NOTE revised. Part Number revised.
		14	Figure 3.2 Memory Map of R8C/23 Group; "Internal ROM" → "Internal ROM (program ROM)" revised. "Data area" → "Data flash" "program area" → "program ROM" revised Address "1ZZZZh" added. NOTE2 added. Part Number revised.
		15	Table 4.1 SFR Information (1); 001Ch: 00h → 00h, 1000000b 0024h: TBD → Value when shipping NOTES revised.
		30	Figure 5.4 OFS Register, Function of the LVD1ON bit; "~ after Hardware reset" → "~ after reset" revised. NOTES revised.
		31	5.1.1 When Power Supply is Stable (2) revised. 5.1.2 Power On (4) revised.
		32	Figure 5.5 Example of Hardware Reset Circuit and Operation and Figure 5.6 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation revised.
		33	5.2 Power-On Reset Function, on the 2nd line; "When a capacitor is ~ or more." added. Figure 5.7 Example of Power-On Reset Circuit and Operation revised. NOTES revised.
		34	5.3 Voltage Monitor 1 Reset(1); on the 8th line; The LVD1ON bit in the OFS register can select to~ "after a reset" added.
		35 to 68	"6. Programmable I/O Ports" → "6. Voltage Detection Circuit" and "7. Voltage Detection Circuit" → "7. Programmable I/O Ports" revised.
		38	Figure 6.4 Registers VCA1 and VCA2; VCA2 register revised.
		39	Figure 6.5 VW1C Register revised.

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0.20	Jun 28, 2006	41	6.1 VCC Input Voltage; "6.1 Monitoring VCC Input Voltage" → "6.1 VCC Input Voltage" revised.
		48	Figure 7.2 Configuration of Programmable I/O Ports (2) revised.
		49	Figure 7.3 Configuration of Programmable I/O Ports (3) revised.
		51	Figure 7.5 Configuration of Programmable I/O Ports (5) revised.
		53	Figure 7.7 Configuration of Programmable I/O Ports (7) revised.
		55	Figure 7.9 PDi (i = 0 to 4 and 6) Registers; NOTE3 added. Figure 7.10 Pi (i = 0 to 4 and 6) Registers; P6 Address "00EEh" → "00ECh" corrected.
		57 to 67	7.4 Port Settings added.
		69	8.1 Processor Modes "8.1 Type of Processor Mode" → "8.1 Processor Modes" revised.
		70	9. Bus revised; Table 9.2 Bus Cycles by Access Space of the R8C/23 Group added. Table 9.3 Access Unit and Bus Operations; "SFR" → "SFR, data flash" "ROM/RAM" → "ROM (program ROM), RAM" below the Table.9.3 "However, only following ~ at a time." added.
		73	Figure 10.2 CM0 Register; NOTE6 deleted.
		75	Figure 10.4 OCD Register; "System clock select bet(3)" → "System clock select bet(4)" "1:Selects on-chip oscillator clock(4)" → "1:Selects on-chip oscillator clock(3)" corrected.
		76	Figure 10.5 Registers FRA0 and FRA1; NOTE2 in the FRA0 register revised.
		77	Figure 10.7 VCA2 Register added.
		79	Figure 10.9 Examples of XIN Clock Connection Circuit; NOTE revised.
		80	10.2.2 High-Speed On-Chip Oscillator Clock, on the 3rd and 8th lines; "To use the high-speed ~ (divide-by-4 mode or more)." added. "Since the difference ~ each bit" → "Since there are ~ individual bits." revised.
		81	10.3.5 fOCO40M; "fOCO40M can be used with supply voltage VCC = 3.0 to 5.5V." added.
		83	Table 10.2 Settings and Modes of Clock Associated Bits; "-: can be 0 or 1, no change in outcome." added.

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0.20	Jun 28, 2006	84	10.4.1.3 Low-Speed On-Chip Oscillator Mode, on the 8th line; "In this mode, ~ consumption operation." added. 10.4.2.2 Entering Wait Mode revised. 10.4.2.3 Pin Status in Wait Mode revised.
		85	10.4.2.4 Exiting Wait Mode revised. Table 10.3 Interrupts to Exit Wait Mode and Usage Conditions; CM02 = 1 of Timer RA Interrupt revised. CM02 = 1 of Timer RD Interrupt revised.
		86	Figure 10.10 Time from Wait Mode to Interrupt Routine Execution added.
		90	Figure 10.12 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock revised.
		91	Figure 10.13 Example of Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt revised.
		92	10.6 Notes on Clock Generation Circuit revised.
		94	Figure 12.1 Interrupts; Address break (2) added.
		98	Table 12.2 Relocatable Vector Tables; "A0RIC" → "S0RIC" corrected.
		104	Table 12.5 IPL Value When Software or Special Interrupt Is Acknowledged; "Address break" added.
		106	Figure 12.10 Priority Levels of Hardware Interrupts; "Address break" added.
		118	12.7 Notes on Interrupts; "12.7 Precautions on Interrupts" → "12.7 Notes on Interrupts" revised.
		121	Figure 13.1 Block Diagram of Watchdog Timer; "("L") active", "PM12: Bit in PM1 register" added.
		122	Figure 13.2 Registers OFS and WDC revised.
		126	14. Timers; "The count source for ~ counting and reloading" deleted.
		127	Table 14.1 Functional Comparison of Timers; Count source of Timer RD, "TRCIOA0" → "TRDIOA0" corrected.
		128	14.1 Timer RA, the 5th line; "The count source for ~ counting and reloading" added. Figure 14.1 Block Diagram of Timer RA revised.
		129	Figure 14.2 Registers TRACR and TRAIOC; The TRAIOC register revised.
		148	14.1.6 Notes on Timer RA; "14.1.6 Precautions on Timer RA" → "14.1.6 Notes on Timer RA" revised.

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0.20	Jun 28, 2006	149	14.2 Timer RB, on the 5th line; "The count source for timer RB ~ counting and reloading" added. Figure 14.17 Block Diagram of Timer RB revised.
		155	Table 14.8 Programmable Waveform Generation Mode Specifications, "Write to Timer" in the item; "TRAPRE" → "TRBPRE" corrected.
		158	Table 14.9 Programmable One-Shot Generation Mode Specifications, "Write to Timer" in the item; "TRAPRE" → "TRBPRE" corrected.
		162	Table 14.10 Programmable Wait One-Shot Generation Mode Specifications, "Write to Timer" in the item; "TRAPRE" → "TRBPRE" corrected.
		166	Table 14.11 Timer RD Operation Clocks; "TPSC2" → "TCK2" and "TRSC0" → "TCK0" revised. On the 5th line below the Table 14.11; "(Pin output ~ detection)" added.
		167 to 169	Table 14.12 Pin Functions TRDIOA0/TRDCLK(P2_0) Table 14.13 Pin Functions TRDIOB0(P2_1) Table 14.14 Pin Functions TRDIOC0(P2_2) Table 14.15 Pin Functions TRDIOD0(P2_3) Table 14.16 Pin Functions TRDIOA1(P2_4) Table 14.17 Pin Functions TRDIOB1(P2_5) Table 14.18 Pin Functions TRDIOC1(P2_6) Table 14.19 Pin Functions TRDIOD1(P2_7) Table 14.20 Pin Functions INT0(P4_5) added.
		171	14.3.1 Mode Selection deleted Table 14.21 Count Source Selection; Selection of f1, f2, f4, f8, f32, and fOCO40M revised. Figure 14.29 Block Diagram of Count Source; "TPSC2 to TPSC0" → "TCK2 to TCK0" revised.
		172	Figure 14.30 Buffer Operation in Input Capture Function revised.
		173	Figure 14.31 Buffer Operation in Output Compare Function revised. On the 4th line below the Figure 14.31; "IOC2 to IOC0 bits" → "IOC2 bit" and "IOA2 to IOA0 bits" → "IOA2 bit" revised. On the 7th line below the Figure 14.31; "IOD2 to IOD0 bits" → "IOD2 bit" and "IOB2 to IOB0 bits" → "IOB2 bit" revised. On the 8th line below the Figure 14.31; "Bits IMFC ~ capture function" added.
		174	Below the Figure 14.32 Synchronous Operation; "For the synchronous ~ register=110b)" deleted.

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0.20	Jun 28, 2006	175	14.3.4 Pulse Output Forced Cutoff, on the 13th line; "P2D" → "PD2" corrected. On the 15th line; "P4_5 bit in the P4D register" → "PD4_5 bit in the PD4 register" corrected. On the 2nd line from the bottom; "According to ~ of interrupts" added.
		177	14.3.5 Input Capture Function, on the 5th line; "The TRDGRA0 register ~ trigger input." added. Figure 14.34 Block Diagram of Input Capture Function; NOTES revised.
		178	Table 14.23 Input Capture Function Specifications revised.
		179	Figure 14.35 Registers TRDSTR and TRDMR in Input Capture Function; The TRDSTR register revised.
		180	Figure 14.36 TRDPMR Register in Input Capture Function revised.
		181	Figure 14.37 TRDFCR Register in Input Capture Function revised.
		183	Figure 14.39 Registers TRDCR0 to TRDCR1 in Input Capture Function revised.
		184	Figure 14.40 Registers TRDIORA0 to TRDIORA1 in Input Capture Function revised.
		185	Figure 14.41 Registers TRDIORC0 to TRDIORC1 in Input Capture Function revised.
		186	Figure 14.42 Registers TRDSR0 to TRDSR1 in Input Capture Function revised.
		192	Table 14.25 Output Compare Function Specifications, on the 5 to 6th lines from the bottom; "TRCIOAi" → "TRDIOAi" and "TRCIOBi" → "TRDIOBi" corrected.
		193	Figure 14.49 Registers TRDSTR and TRDMR in Output Compare Function revised.
		194	Figure 14.50 TRDPMR Register in Output Compare Function revised.
		195	Figure 14.51 TRDFCR Register in Output Compare Function revised.
		196	Figure 14.52 Registers TRDOER1 to TRDOER2 in Output Compare Function; NOTE in the TRDOER2 register added.
		198	Figure 14.54 Registers TRDCR0 to TRDCR1 in Output Compare Function revised.
		199	Figure 14.55 Registers TRDIORA0 to TRDIORA1 in Output Compare Function revised.
		200	Figure 14.56 Registers TRDIORC0 to TRDIORC1 in Output Compare Function revised.
		201	Figure 14.57 Registers TRDSR0 to TRDSR1 in Output Compare Function revised.
		209	Figure 14.65 TRDSTR Register in PWM Mode revised

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0.20	Jun 28, 2006	210	Figure 14.66 Registers TRDMR and TRDPMR in PWM Mode revised
		211	Figure 14.67 TRDFCR Register in PWM Mode revised
		212	Figure 14.68 Registers TRDOER1 to TRDOER2 in PWM Mode; NOTE in the TRDOER2 register added.
		213	Figure 14.69 Registers TRDOCR and TRDCR0 to TRDCR1 in PWM Mode revised.
		214	Figure 14.70 Registers TRDSR0 to TRDSR1 in PWM Mode revised.
		221	Table 14.29 Reset Synchronous PWM Mode Specifications revised.
		222	Figure 14.78 TRDSTR Register in Reset Synchronous PWM Mode revised.
		223	Figure 14.79 Registers TRDMR and TRDFCR in Reset Synchronous PWM Mode revised.
		224	Figure 14.80 Registers TRDOER1 to TRDOER2 in Reset Synchronous PWM Mode; NOTE in the TRDOER2 register added.
		225	Figure 14.81 TRDCR0 Register in Reset Synchronous PWM Mode revised.
		226	Figure 14.82 Registers TRDSR0 to TRDSR1 in Reset Synchronous PWM Mode revised.
		232	Figure 14.88 TRDSTR Register in Complementary PWM Mode revised.
		233	Figure 14.89 TRDMR Register in Complementary PWM Mode revised.
		234	Figure 14.90 TRDFCR Register in Complementary PWM Mode revised.
		235	Figure 14.91 Registers TRDOER1 to TRDOER2 in Complementary PWM Mode; NOTE in the TRDOER2 register added.
		236	Figure 14.92 Registers TRDCR0 to TRDCR1 in Complementary PWM Mode revised.
		237	Figure 14.93 Registers TRDSR0 to TRDSR1 in Complementary PWM Mode revised.
		240	Below the Table 14.32; “Since values ~ (buffer register).” added.
		244	Figure 14.99 Block Diagram of PWM3 Mode; “Buffer” added.
		245	Table 14.33 PWM3 Mode Specifications revised.
		246	Figure 14.100 TRDSTR Register in PWM3 Mode revised.
		247	Figure 14.101 Registers TRDMR and TRDFCR in PWM3 Mode revised.
		248	Figure 14.102 Registers TRDOER1 to TRDOER2 in PWM3 Mode; NOTE in the TRDOER2 register added.
		250	Figure 14.104 TRDCR0 Register in PWM3 Mode revised.
		251	Figure 14.105 Registers TRDSR0 and TRDSR1 in PWM3 Mode added.
		252	Figure 14.106 Registers TRDIER0 and TRDIER1 in PWM3 Mode revised.

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0.20	Jun 28, 2006	254	Table 14.34 TRDGRji Register Functions in PWM3 Mode revised. On the 4th line from the bottom; "Registers TRDGRC0, ~ (buffer register)." added.
		255	Figure 14.109 Operating Example of PWM3 Mode revised.
		258	14.3.12 Notes on Timer RD; "14.3.13 Precautions on Timer RD" → "14.3.12 Notes on Timer RD" revised. 14.3.12.1 TRDSTR Register (i = 0 or 1) added.
		259	14.3.12.6 Reset Synchronous PWM Mode revised. 14.3.12.7 Complementary PWM Mode revised.
		263	14.3.13.7 PWM3 mode deleted. 14.3.12.8 Count Source fOCO40M added.
		264	14.4 Timer RE, on the 3rd line; "The count source ~ timer operations." added.
		271	14.4.2 Notes on Timer RE; "14.4.2 Precautions on Timer RE" → "14.4.2 Notes on Timer RE" revised.
		276	Figure 15.5 Registers UiC0 and UiC1 (i = 0 or 1); The UiC0 register (i=0 or 1) revised.
		284	Table 15.5 Registers Used and Settings for UART Mode revised. Table 15.6 I/O Pin Functions in UART Mode revised.
		285	Figure 15.10 Transmit Timing in UART Mode revised.
		286	Figure 15.11 Receive Timing Example in UART Mode revised.
		288	15.3 Notes on Serial Interface; "15.3 Precautions on Serial Interface" → "15.3 Notes on Serial Interface" revised.
		289	16. Clock Synchronous Serial Interface, on the 3rd line; "(SSU)" added.
		290	16.2 Clock Synchronous Serial I/O with Chip Select (SSU); "(SSU)" added. Table 16.2 Clock Synchronous Serial I/O with Chip Select Specifications; NOTE2 deleted.
		294	Figure 16.4 SSMR Register revised.
		297	Figure 16.7 SSMR2 Register revised.
		298	Figure 16.8 Registers SSTDR and SSRDR; NOTE in the SSTDR register revised.
		299	16.2.1 Transfer Clock; "ϕ" → "f1" revised.
		305	16.2.5.2 Data Transmission; "16.2.5.2 Data Transmit" → "16.2.5.2 Data Transmission" revised. 16.2.5.2 Data Transmission, on the 4th line from the bottom; "When setting the ~ transmit is enabled." deleted.

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0.20	Jun 28, 2006	306	Figure 16.14 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode); NOTE revised.
		307	16.2.5.3 Data Reception; "16.2.5.3 Data Receive" → "16.2.5.3 Data Reception" revised.
		309	16.2.5.4 Data Transmission/Reception; "16.2.5.4 Data Transmit/Receive" → "16.2.5.4 Data Transmission/ Reception" revised. 16.2.5.4 Data Transmission/Reception, on the 5th line from the bottom; "When setting the ~ transmit is enabled." deleted.
		310	Figure 16.17 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode) revised.
		313	16.2.6.2 Data Transmission; "16.2.6.2 Data Transmit" → "16.2.6.2 Data Transmission" revised. 16.2.6.2 Data Transmission, on the 9th line from the bottom; "When setting the ~ transmit is enabled." deleted.
		315	16.2.6.3 Data Reception; "16.2.6.3 Data Receive" → "16.2.6.3 Data Reception" revised.
		318	16.2.8 Notes on Clock Synchronous Serial I/O with Chip Select; "16.2.8 Precautions on Clock Synchronous Serial I/O with Chip Select" → "16.2.8 Notes on Clock Synchronous Serial I/O with Chip Select" revised.
		347	Figure 16.46 Example of Register Setting in Master Transmit Mode (I^2C Bus Interface Mode); "Figure 16.46 Example of Register Setting in Master Transmit Mode (Clock Synchronous Serial)" → "Figure 16.46 Example of Register Setting in Master Transmit Mode (I^2C Bus Interface Mode)" revised.
		348	Figure 16.47 Example of Register Setting in Master Receive Mode (I^2C Bus Interface Mode); "Figure 16.47 Example of Register Setting in Master Receive Mode (Clock Synchronous Serial)" → "Figure 16.47 Example of Register Setting in Master Receive Mode (I^2C Bus Interface Mode)" revised.
		349	Figure 16.48 Example of Register Setting in Slave Transmit Mode (I^2C Bus Interface Mode); "Figure 16.48 Example of Register Setting in Slave Transmit Mode (Clock Synchronous Serial)" → "Figure 16.48 Example of Register Setting in Slave Transmit Mode (I^2C Bus Interface Mode)" revised.
		350	Figure 16.49 Example of Register Setting in Slave Receive Mode (I^2C Bus Interface Mode); "Figure 16.49 Example of Register Setting in Slave Receive Mode (Clock Synchronous Serial)" → "Figure 16.49 Example of Register Setting in Slave Receive Mode (I^2C Bus Interface Mode)" revised.
		351	16.3.8 Notes on I^2O Bus Interface; "16.3.8 Precautions on I^2O Bus Interface" → "16.3.8 Notes on I^2O Bus Interface" revised.

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0.20	Jun 28, 2006	352 to 385	17. Hardware LIN; "Sync" → "Synch" revised.
		354	Figure 17.2 LINCR Register revised.
		355	Figure 17.3 LINST Register revised.
		356	Figure 17.4 Typical Operation when Sending a Header Field; "RAIC" → "TRAIC" corrected.
		357	Figure 17.5 Example of Header Field Transmission Flowchart (1) revised.
		358	Figure 17.6 Example of Header Field Transmission Flowchart (2) revised.
		359	Figure 17.7 Typical Operation when Receiving a Header Field; "RAIC" → "TRAIC" corrected.
		360	Figure 17.8 Example of Header Field Reception Flowchart (1) revised.
		361	Figure 17.9 Example of Header Field Reception Flowchart (2) revised.
		362	Figure 17.10 Example of Header Field Reception Flowchart (3) revised.
		363	Figure 17.11 Typical Operation when a Bus Collision is Detected; "RAIC" → "TRAIC" corrected.
		364	17.5 Interrupt Requests, on the 2nd line; "Synch Break generation competed" added.
		374	Figure 18.9 C0SSTR Register, Setting values; "1: Reception slot, The message is read" → "1: Reception slot, The message is not read" corrected.
		379	Figure 18.16 Transition between Operational Modes revised.
		380	18.5.3 CAN Sleep Mode, on the 1st line; "and the Reset bit is set to 0" deleted.
		383	Table 18.2 Examples of Baud Rate revised.
		391	18.14 Notes on CAN Module; "18.14 Precautions on CAN Module" → "18.14 Notes on CAN Module" revised.
		394	Table 18.5 Recommended Pin Connections (In Case of PCA82C250: Philips Product) and Table 18.6 Recommended Pin Connections (In Case of PCA82C252: Philips Product); NOTES; "Ta" → "Topr" revised.
		395	Table 19.1 Performance of A/D converter revised.
		396	Figure 19.1 Block Diagram of A/D Converter; "ADGSEL" → "ADGSEL0" corrected.
		399	Table 19.2 One-Shot Mode Specifications, Input pin; "AN8" → "AN0" corrected.
		405	19.3 Sample and Hold, on the 2nd and 5th lines; "to 28 ϕ AD cycles ~ 10-bit resolution." deleted. "When performing ~ the microcomputer." deleted.
		406	19.4 A/D Conversion Cycles added.
		407	19.5 Internal Equivalent Circuit of Analog Input added.
		408	19.6 Output Impedance of Sensor Under A/D Conversion added.

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0.20	Jun 28, 2006	409	19.7 Notes on A/D Converter; "19.7 Precautions on A/D Converter" → "19.7 Notes on A/D Converter" revised.
		410	20. Flash Memory; "20. Flash Memory Version" → "20. Flash Memory" revised. Table 20.1 Flash Memory Performance, Program and Erase Endurance; "Program Area" → "Program ROM" "Data Area" → "Data ROM" revised.
		412	20.2 Memory Map, on the 4th and 5th lines; "(program ROM)" and "(data flash)" added. Figure 20.1 Flash Memory Block Diagram for R8C/22 Group revised.
		413	Figure 20.2 Flash Memory Block Diagram for R8C/23 Group revised.
		414	20.3 Functions to Prevent Rewriting of Flash Memory; "20.3 Functions to prevent Flash Memory from Rewriting" → "20.3 Functions to Prevent Rewriting of Flash Memory" revised. 20.3.2 ROM Code Protect Function, on the 5th and 7th lines; "The ROM code ~ flash memory." deleted. "write 0 to the ROMCR bit" → "erase the block including the OFS register" revised.
		415	Figure 20.4 OFS Register revised.
		417	20.4.2 EW1 Mode, on the 3rd line; "Do not execute software command ~" → "Do not execute command ~" revised.
		418	20.4.2.1 FMR00 Bit, on the 1st line; "(including suspend periods)" added.
		419	20.4.2.16 FMR47 Bit revised.
		420	Figure 20.5 FMR0 Register; NOTE6 added.
		422	Figure 20.7 FMR4 Register; NOTES revised.
		423	Figure 20.8 Timing of Suspend Operation revised.
		427	20.4.3.4 Program Command, on the 5th line; "The FMR00 bit is ~ completes." → "When suspend function ~ auto-programming completes." revised.
		428	Figure 20.13 Program Command (When Suspend Function Enabled) added.
		429	20.4.3.5 Block Erase, on the 11th line; "The block erase ~ program suspend." → "Do not use ~ program-suspend" revised.
		430	Figure 20.15 Block Erase Command (When Erase-Suspend Function Enabled) revised.
		431	Table 20.5 Status Register Bits, Value after Reset of SR7 (D7) "0" → "1" corrected.

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0.20	Jun 28, 2006	434	20.5 Standard Serial I/O Mode, on the 3rd line; "Standard serial I/O ~ interface" → "There are three ~ serial I/O mode 3." revised. Table 20.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2) revised.
		436	Figure 20.17 Pin Connections for Standard Serial I/O Mode 3; "Figure 20.17 Pin Connections for Standard Serial I/O Mode" → "Figure 20.17 Pin Connections for Standard Serial I/O Mode 3" revised.
		437	Figure 20.18 Pin Processing in Standard Serial I/O Mode 2 added. Figure 20.19 Pin Processing in Standard Serial I/O Mode 3; "Figure 20.19 Pin Processing in Standard Serial I/O Mode" → "Figure 20.19 Pin Processing in Standard Serial I/O Mode 3" revised.
		439	20.7 Notes on Flash Memory; "20.7 Precautions on Flash Memory Version" → "20.7 Notes on Flash Memory" revised.
		442 to 461	21. Electrical Characteristics revised.
		462	22. Usage Notes; "22. Precautions" → "22. Usage Notes" revised. 22.1.1 Stop Mode and Wait Mode revised. 22.1.3 Oscillation Circuit Constants revised.
		468	22.3.3.1 TRDSTR Register (i = 0 or 1) added.
		469	22.3.3.6 Reset Synchronous PWM Mode; (2) revised. 22.3.3.7 Complementary PWM Mode; (2) revised. On the 3rd line from the bottom; "However, to write data ~ to 1 (buffer register)." added.
		473	22.3.3.7 PWM3 Mode deleted. 22.3.3.8 Count Source fOCO40M added.
		487	23. Notes on On-Chip Debugger; "23. Precaution for On-chip Debugger" → "23. Notes on On-Chip Debugger" revised. (2) and (3) added.
		488	Appendix 1. Package Dimensions; "Diagrams shows ~ website." added.
		489	Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806); NOTES revised.
		490	Appendix Figure 3.1 Example of Oscillation Evaluation Circuit revised.
1.00	Oct 27, 2006	All pages	"Preliminary" and "Under development" deleted
		2	Table 1.1 Functions and Specifications for R8C/22 Group revised. NOTE1 deleted.
		3	Table 1.2 Functions and Specifications for R8C/23 Group revised. NOTE1 deleted.

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1.00	Oct 27, 2006	5	Table 1.3 Product Information for R8C/22 Group; "R5F2122AJFP (D)", "R5F2122CJFP (D)", "R5F2122AKFP (D)", "R5F2122CKFP (D)", and NOTE added. Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group; "A: 96 KB" and "C: 128 KB" added.
		6	Table 1.4 Product Information for R8C/23 Group; "R5F2123AJFP (D)", "R5F2123CJFP (D)", "R5F2123AKFP (D)", "R5F2123CKFP (D)", and NOTE added. Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group; "A: 96 KB" and "C: 128 KB" added.
		13	Figure 3.1 Memory Map of R8C/22 Group revised.
		14	Figure 3.2 Memory Map of R8C/23 Group revised.
		15	Table 4.1 SFR Information (1)(1); NOTE8; "The CSPROINI bit in the OFS register is set to 0." → "The CSPROINI bit in the OFS register is 0." revised.
		29	Table 5.2 Title of Table revised
		30	Figure 5.4 OFS Register; NOTE2; "LVD0ON" → "LVD1ON" revised.
		33	5.2 Power-On Reset Function(1); NOTE1 deleted. NOTE2 revised. Figure 5.7 Example of Power-On Reset Circuit and Operation revised.
		34	5.3 Voltage Monitor 1 Reset, on the 9th line; "To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, bits VW1C0 and VW1C6 in the VW1C register to 1, the VCA bit in the VCA2 register to 1." added. NOTE1 deleted. 5.4 Voltage Monitor 2 Reset; NOTE1 deleted.
		35	6. Voltage Detection Circuit; NOTE1 deleted.
		38	Figure 6.4 Registers VCA1 and VCA2; Voltage Detection Register 2(1) revised. NOTE5 added.
		47 to 53	Figure 7.1 to Figure 7.3 Configuration of Programmable I/O Ports; NOTE1 added
		55	Figure 7.9 PDi (i = 0 to 4 and 6) Registers; Bit Names revised. Figure 7.10 Pi (i = 0 to 4 and 6) Registers; Bit Names revised.
		66	Table 7.42 Port P6_2/CRX0; "CRX0 output" → "CRX0 input" revised.
		71	Table 10.1 Specifications of Clock Generation Circuit; NOTE3; "10 MHz" → "20 MHz" revised.

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1.00	Oct 27, 2006	75	Figure 10.4 OCD Register; NOTE7; "Figure 10.12" → "Figure 10.14"corrected.
		76	Figure 10.5 Registers FRA0 and FRA1; High-Speed On-Chip Oscillator Control Register 0(1); NOTE2 revised. High-Speed On-Chip Oscillator Control Register 1(1); NOTE revised.
		77	Figure 10.6 FRA2 Register; High-Speed On-Chip Oscillator Control Register 2(1) revised. NOTE3 added. Figure 10.7 VCA2 Register; Voltage Detection Register 2(1) revised. NOTE5 added.
		79	Figure 10.9 Examples of XIN Clock Connection Circuit; Ceramic resonator external circuit revised.
		80	10.2.2 High-Speed On-Chip Oscillator Clock; On the 4th line revised. On the2nd line from the bottom; "Adjust the amount of high-speed on-chip oscillator frequency to 40 MHz and below by setting the FRA1 register." added.
		84	10.4.1.3 Low-Speed On-Chip Oscillator Mode; On the 2nd line from the bottom; "To enter wait mode from low-speed clock mode, setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled) enables lower consumption current in wait mode." added.
		85	10.4.2.4 Exiting Wait Mode; On the 13th line from the bottom; Figure 10.10 shows the Time from Wait Mode to Interrupt Routine Execution. added.
		86	Figure 10.10 Time from Wait Mode to Interrupt Routine Execution revised.
		87	10.4.2.5 Reducing Internal Power Consumption and Figure 10.11 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit added
		88	10.4.3.3 Exiting Stop Mode, on the 4th line; "Figure 10.12 shows the Time from Stop Mode to Interrupt Routine Execution." added.
		89	Figure 10.12 Time from Stop Mode to Interrupt Routine Execution added.
		90	"Figure 10.11 State Transitions in Power Control Mode" → "Figure 10.13 State Transitions in Power Control Mode" corrected.
		91	10.5.1 How to Use Oscillation Stop Detection Function, on the 6th line; "Figure 10.13" → "Figure 10.15" corrected. On the 10th line; "Figure 10.12" → "Figure 10.14" corrected.
		92	"Figure 10.12 ~" → "Figure 10.14 ~" corrected.
		93	"Figure 10.13 ~" → "Figure 10.15 ~" corrected.
		94	"10.6. Notes on Clock Generation Circuit" revised.
		103	Figure 12.5 Registers INT0IC to INT3IC; NOTE3; "INTOPL" → "INTiPL" corrected.
		111	Figure 12.13 INTF Register revised

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1.00	Oct 27, 2006	124	Figure 13.2 Registers OFS and WDC; Option Function Select Register(1); NOTE2 revised. Watchdog Timer Control Register revised.
		127	Table 13.3 Watchdog Timer Specifications (with Count Source Protection Mode Enabled); NOTE2; "CSPRO" → "CSPROINI" corrected.
		130	Figure 14.1 Block Diagram of Timer RA revised.
		131	Figure 14.2 Registers TRACR and TRAIOC revised.
		132	Figure 14.3 Registers TRAMR and TRAPRE Timer RA Mode Register(1); NOTE added. Timer RA Prescaler Register; NOTE1 revised.
		133	Figure 14.4 TRA Register; NOTE1 revised.
		134	Table 14.2 Timer Mode Specifications; "Write to Timer" revised. Figure 14.5 TRAIOC Register in Timer Mode; NOTES deleted.
		135	Figure 14.6 Registers TRAIOC and TRAMR in Timer Mode deleted. 14.1.1.1 Timer Write Control during Count Operation and Figure 14.6 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation added.
		136	Table 14.3 Pulse Output Mode Specifications revised.
		137	Figure 14.7 Register TRACR and TRAIOC in Pulse Output Mode → Figure 14.7 TRAIOC Register in Pulse Output Mode replaced. Timer RA Control Register deleted.
		138	Figure 14.8 TRAMR Register in Pulse Output Mode deleted. Table 14.4 Event Counter Mode Specifications revised.
		139	Figure 14.9 Registers TRACR and TRAIOC in Event Counter Mode → Figure 14.8 TRAIOC Register in Event Counter Mode replaced. Timer RA Control Register deleted. Figure 14.10 TRAMR Register in Event Counter Mode deleted.
		140	14.1.4 Pulse Width Measurement Mode, on the 3rd line; Table 14.5 Pulse Width Measurement Mode Specifications revised.
		141	Figure 14.11 Registers TRACR and TRAIOC in Pulse Width Measurement Mode → Figure 14.9 TRAIOC Register in Pulse Width Measurement Mode replaced. Timer RA Control Register (4) deleted. Figure 14.12 TRAMR Register in Pulse Width Measurement Mode deleted.
		142	Figure 14.10 Operating Example of Pulse Width Measurement Mode revised.
		143	Table 14.6 Pulse Period Measurement Mode Specifications revised.
		144	Figure 14.14 Registers TRACR and TRAIOC in Pulse Period Measurement Mode → Figure 14.11 TRAIOC Register in Pulse Period Measurement Mode replaced. Timer RA Control Register (4) deleted. Figure 14.15 TRAMR Register in Pulse Period Measurement Mode deleted.

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1.00	Oct 27, 2006	145	Figure 14.16 Operating Example of Pulse Period Measurement Mode → Figure 14.12 Operating Example of Pulse Period Measurement Mode replaced. NOTE6 revised.
		148	Figure 14.18 Registers TRBCR and TRBOCR → Figure 14.14 Registers TRBCR and TRBOCR replaced. Timer RB Control Register; NOTES revised. Timer RB One-Shot Control Register; Function and NOTES revised. NOTE deleted.
		149	Figure 14.19 Registers TRBIOC and TRBMR → Figure 14.15 Registers TRBIOC and TRBMR replaced. Timer RB Mode Register; TWRC bit and NOTES revised.
		150	Figure 14.20 Registers TRBPRE, TRBSC, and TRBPR → Figure 14.16 Registers TRBPRE, TRBSC, and TRBPR replaced. NOTES revised.
		151	Table 14.7 Timer Mode Specifications; “Write to Timer” revised. Figure 14.21 Regsiters TRBIOC and TRBMR in Timer Mode → Figure 14.17 TRBIOC Register in Timer Mode replaced. Timer RB Mode Register deleted.
		152	14.2.1.1 Timer Write Control during Count Operation added.
		153	Figure 14.18 TRBIOC Register in Timer Mode added.
		154	Table 14.8 Programmable Waveform Generation Mode Specifications revised. NOTE2 and NOTE3 revised.
		155	Figure 14.22 Registers TRBIOC and TRBMR in Programmable Waveform Generation Mode → Figure 14.19 TRBIOC Register in Programmable Waveform Generation Mode replaced. TOCNT bit revised. NOTE deleted. Timer RB Mode Register deleted.
		156	Figure 14.23 Operation Example of Timer RB in Programmable Waveform Generation Mode → Figure 14.20 Operation Example of Timer RB in Programmable Waveform Generation Mode replaced. Figure 14.20 revised.
		157	Table 14.9 Programmable One-Shot Generation Mode Specifications revised. NOTE added.
		158	Figure 14.24 Registers TRBIOC and TRBMR in Programmable One-Shot Generation Mode → Figure 14.21 TRBIOC Register in Programmable One-Shot Generation Mode replaced. NOTE revised. Timer RB Mode Register deleted.
		160	14.2.3.1 One-Shot Trigger Selection added.
		162	Table 14.10 Programmable Wait One-Shot Generation Mode Specifications revised. NOTE1 revised.

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1.00	Oct 27, 2006	163	Figure 14.26 Registers TRBIOC and TRBMR in Programmable Wait One-Shot Generation Mode → Figure 14.23 TRBIOC Register in Programmable Wait One-Shot Generation Mode replaced. TOPL bit and NOTE revised. Timer RB Mode Register deleted.
		164	Figure 14.27 Operation Example of Programmable Wait One-Shot Generation Mode → Figure 14.24 Operation Example of Programmable Wait One-Shot Generation Mode replaced. Figure 14.24 revised.
		165	14.2.5 Notes on Timer RB revised.
		171	Table 14.21 Count Source Selection; NOTE1 added.
		179	Figure 14.35 Registers TRDSTR and TRDMR in Input Capture Function → FIgure 14.32 Registers TRDSTR and TRDMR in Input Capture Function replaced. Timer RD Start Register(1); "TRD0 count start bit" → "TRD0 count start flag" revised. "TRD1 count start bit" → "TRD1 count start flag" revised.
		193	Figure 14.49 Registers TRDSTR and TRDMR in Output Compare Function → Figure 14.46 Registers TRDSTR and TRDMR in Output Compare Function replaced. Timer RD Start Register(1); "TRD0 count start bit(4)" → "TRD0 count start flag(4)" revised. "TRD1 count start bit(5)" → "TRD1 count start flag(5)" revised.
		196	Figure 14.52 Registers TRDOER1 to TRDOER2 in Output Compare Function → Figure 14.49 Registers TRDOER1 to TRDOER2 in Output Compare Function replaced. Timer RD Output Master Enable Register 1 revised.
		197	Figure 14.50 TRDOCR Register in Output Compare Function → Figure 14.50 TRDOCR Register in Output Compare Function replaced. NOTE2 added.
		206	On the first line; "Figure 14.63 ~" → "Figure 14.60 lists ~" corrected.
		209	Figure 14.65 TRDSTR Register in PWM Mode → Figure 14.62 TRDSTR Register in PWM Mode replaced. Timer RD Star Register(1); "TRD0 count start bit(4)" → "TRD0 count start flag(4)" corrected. "TRD1 count start bit(5)" → "TRD1 count start flag(5)" corrected.
		212	Figure 14.68 Registers TRDOER1 to TRDOER2 in PWM Mode → Figure 14.65 Registers TRDOER1 to TRDOER2 in PWM Mode replaced.
		213	Figure 14.69 Registers TRDOCR and TRDCR0 to TRDCR1 in PWM Mode → Figure 14.66 Registers TRDOCR and TRDCR0 to TRDCR1 in PWM Mode replaced. Timer RD Output Control Register(1); NOTE2 added.

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1.00	Oct 27, 2006	218	Figure 14.75 Operating Example of PWM Mode → Figure 14.72 Operating Example of PWM Mode replaced. Figure 14.72 revised.
		222	Figure 14.78 TRDSTR Register in Reset Synchronous PWM Mode → Figure 14.75 TRDSTR Register in Reset Synchronous PWM Mode replaced. Timer RD Start Register(1); "TRD0 count start bit(4)" → "TRD0 count start flag(4)" corrected. "TRDi count start bit(5)" → "TRD1 count start flag(5)" corrected.
		228	Table 14.30 TRDGRji Register Functions in Reset Synchronous PWM Mode; TRDGRA0 register; "(Output inversed every half period of TRDIOC0 pin)" → "(Output inversed every period of TRDIOC0 and PWM pins)", TRDGRC0 register; "(Output inversed every half period of TRDIOC0 pin)" → "(Output inversed every period of TRDIOC0 and PWM pins)" revised.
		231	Table 14.31 Complementary PWM Mode Specifications, on the 3rd line from the bottom; "i = 0 to 2, j = either A, B, C or D" → "i = 0 or 1, j = either A, B, C or D" corrected.
		232	Figure 14.85 TRDSTR Register in Complementary PWM Mode → Figure 14.85 TRDSTR Register in Complementary PWM Mode replaced. Timer RD Start Register(1); TRD0 count start bit(4) → "TRD0 count start flag(4)" corrected. "TRD1 count start bit(5)" → "TRD1 count start flag(5)" corrected.
		242	Figure 14.98 Operating Example of Complementary PWM Mode → Figure 14.95 Operating Example of Complementary PWM Mode replaced.
		245	Table 14.33 PWM3 Mode Specifications, on the bottom line; "j = either A, B, C or D" → "i = 0 or 1, j = either A, B, C or D" corrected.
		246	Figure 14.100 TRDSTR Register in PWM3 Mode → Figure 14.97 TRDSTR Register in PWM3 Mode replaced. Timer RD Start Register(1); "TRD0 count start bit(4)" → "TRD0 count start flag(4)" corrected. "TRD1 count start bit(5)" → "TRD1 count start flag(5)" corrected.
		249	Figure 14.103 TRDOCR Register in PWM3 Mode → Figure 14.100 TRDOCR Register in PWM3 Mode replaced. NOTE2 added.
		259	14.3.12.4 Count Source Switch; "count clock source" → "count source" corrected. 14.3.12.7 Complementary PWM Mode, on the bottom line; "Do not use the TRDGRC0 register in complementary PWM mode." deleted.
		275	Figure 15.4 UiMR Register (i = 0 or 1); "Serial Interface mode select bit(2,4)" → "Serial I/O mode select bit(2,4)" corrected.
		276	Figure 15.5 Registers UiC0 and UiC1 (i = 0 or 1); UARTi Transmit/Receive Control Register 1 (i = 0 or 1) revised. NOTE2 added.
		289	Table 16.1 Mode Selections revised.

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1.00	Oct 27, 2006	293	Figure 16.3 SSCRL Register; NOTE2 revised
		321	Figure 16.23 External Circuit Connection Example of Pins SCL and SDA revised.
		348	Figure 16.47 Example of Register Setting in Master Receive Mode (I^2C Bus Interface Mode); (1) "Set the ~ master receive mode ~"→ "Set the ~ master transmit mode ~" corrected.
		357	Figure 17.5 Example of Header Field Transmission Flowchart (1); Hard ware LIN Clear the status flags; "~ in LINST register" → "~ in LINST register: 0" corrected.
		361	Figure 17.9 Example of Header Field Reception Flowchart (2); "When the SBE bit in the LINCR register is 0(Unmasked after Synch Break is detected), timer RA is usable in timer mode after the SBDCT flag in the LINST register is set to 1." added.
		362	Figure 17.10 Example of Header Field Reception Flowchart (3); "When the SBE bit in the LINCR register is 1 (Unmasked after Synch Field measurement is completed), timer RA is usable in timer mode after the SFDCT flag in the LINST register is set to 1." added.
		364	17.4.4 Hardware LIN End Processing and Figure 17.12 Example of Hardware LIN Communication Completion Flowchart added.
		372	Figure 18.6 C0MCTLi Register; NOTE1 revised.
		373	Figure 18.7 C0CTLR Register; NOTES revised.
		374	Figure 18.8 C0STR Register; NOTE1 revised.
		376	Figure 18.10 C0ICR Register; NOTE1 revised. Figure 18.11 C0IDR Register; NOTE1 revised.
		377	Figure 18.12 C0CONR Register; "CAN0 Configuration Register" → "CAN0 Configuration Register(2)" added. NOTE2 added.
		404	Figure 19.6 ADCON0 Register in Repeat Mode, in the Function of Frequency select bit 0; "1: Select fOCO-F" → "Do not set" revised.
		408	Figure 19.10 Internal Equivalent Circuit of Analog Input; "i = 4" → "i = 12" corrected.
		410	19.7 Notes on A/D Converter, on the 5th line from the bottom; "Do not select the fOCO-F for the ϕAD." added.
		413	20.2 Memory Map, on the 4th line from the bottom; "When rewriting the block 2 and block 3 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to 1 (rewrite enables)." added.
		414	Figure 20.1 Flash Memory Block Diagram for R8C/22 Group revised.

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1.00	Oct 27, 2006	415	Figure 20.2 Flash Memory Block Diagram for R8C/23 Group revised.
		417	Figure 20.4 OFS Register; NOTE2; "LVD0ON" → "LVD1ON" and "(voltage monitor 0 reset enabled after reset)" → "voltage monitor 0 reset enabled after reset)" corrected.
		418	Table 20.3 Differences between EW0 Mode and EW1 Mode; Modes After Read Status Register added.
		420	20.4.2.3 FMR02 Bit; "The block 1 and block 0 do not ~" → "The block0 block1 block2, and block3 do not ~" corrected.
		428	20.4.3.1 Read Array Command, on the bottom line; "In addition, the MCU enters read array mode after a reset." added. 20.4.3.2 Read Status Register Command, on the bottom line; "The MCU remains in read status register mode until the next read array command is written." added.
		430	Figure 20.13 Program Command (When Suspend Function Enabled) revised. NOTE3 added.
		432	Figure 20.15 Block Erase Command (When Erase-Suspend Function Enabled) revised. NOTE3 added.
		435	Figure 20.16 Full Status Check and Handling Procedure for Individual Errors; "FMR07 = 0?" → "FMR07 = 1?" and "FMR06 = 0?" → "FMR06 = 1?" corrected.
		437	Table 20.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3); P4_2/VREF deleted. P4_3 or P4_5 → P4_2 to P4_5 corrected.
		443	20.7.1.7 Reset Flash Memory deleted. 20.7.1.8 Entering Stop Mode or Wait Mode → 20.7.1.7 Entering Stop Mode or Wait Mode corrected.
		444	Table 21.1 Absolute Maximum Ratings; Power dissipation revised. Table 21.2 Recommended Operating Conditions; System clock revised.
		449	Table 21.8 Voltage Monitor 1 Reset Circuit Electrical Characteristics → Table 21.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(1) replaced. Table 21.8 revised. NOTE3 added. Table 21.9 Power-on Reset Circuit Electrical Characteristics deleted. Figure 21.3 Power-on Reset Circuit Electrical Characteristics revised.
		450	Table 21.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics → Table 21.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics revised.
		456	Table 21.15 Electrical Characteristics (1) [VCC = 5 V] → Table 21.14 Electrical Characteristics (1) [VCC = 5 V] revised. RAM Hold Voltage, Min.; "1.8" → "2.0" corrected.

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1.00	Oct 27, 2006	457	Table 21.16 Electrical Characteristics (2) [Vcc = 5 V] → Table 21.15 Electrical Characteristics (2) [Vcc = 5 V] revised. Wait mode revised.
		460	Table 21.21 Electrical Characteristics (3) [VCC = 3 V → Table 21.20 Electrical Characteristics (3) [VCC = 3 V] revised. RAM hold voltage, Min.; "1.8" → "2.0" corrected.
		461	Table 21.22 Electrical Characteristics (4) [Vcc = 3 V] → Table 21.21 Electrical Characteristics (4) [Vcc = 3 V] revised. Wait mode revised.
		464	22.1.1 Stop Mode and Wait Mode → 22.1.1 Stop Mode revised. 22.1.2 Wait Mode added.
		469	22.3.2 Notes on Timer RB; "Timer RB starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count)." deleted. On the 8th line from the bottom; "- If the TSTOP bit ~ stops immediately." added. On the 6th line from the bottom; "- If 1 is written to the TOSST or TOSSP bit ~ either 0 or 1." added.
		471	22.3.3.4 Count Source Switch; "count clock source" → "count source." corrected.
		485	22.8 Notes on A/D Converter; On the 6th line from the bottom; "Do not select the fOCO-F for the ϕAD." added.
		488	22.9.1.7 Reset Flash Memory deleted.
		490	23. Notes on On-Chip Debugger, (2); ROM 128 KB Product (R5F2122CJFP, R5F2122CKFP, R5F2123CJFP, R5F2123CKFP) addresses 23800h to 23FFFh added. (3); ROM 128 KB Product (R5F2122CJFP, R5F2122CKFP, R5F2123CJFP, R5F2123CKFP) addresses 03B00h to 03BFFh added.
		491	24. Notes on Emulator Debugger added.
1.10	Oct 31, 2007	2	Table 1.1; D version added.
		3	Table 1.2; D version added.
		5	Table 1.3; D version added and development status updated. Figure 1.2; D version added
		6	Table 1.4; D version added and development status updated. Figure 1.3; D version added
		7	Figure 1.4; NOTE 3 added.
		13	Figure 3.1; Part Number of D version added.
		14	Figure 3.2; Part Number of D version added.
		15	Table 4.1; • 000Ah: "00XXX000b" → "00h" • 000Fh: "00011111b" → "00X11111b"
		30	Figure 5.3 and Figure 5.4 NOTE1 revised.

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1.10	Oct 31, 2007	31	5.1.1 (2) and 5.1.2 (4) revised.
		32	Figure 5.5 and Figure 5.6 revised.
		33	5.2 and Figure 5.7 revised.
		38	Figure 6.4; VCA2 register NOTE5 revised.
		59	Table 7.17 revised.
		60	Table 7.19 revised.
		63	Table 7.29 and Table 7.30 revised.
		64	Table 7.33 revised.
		73	Figure 10.2; NOTE4 revised.
		76	Figure 10.5; FRA0 register NOTE2 revised and FRA1 register NOTE2 added.
		77	Figure 10.7; VCA2 register NOTE5 revised.
		80	10.2.2 revised, D version added.
		81	10.3.2 revised.
		84	10.4.1.3 revised.
		85	Table 10.3; Watchdog Timer Interrupt deleted.
		87	10.4.2.5 and Figure 10.11 revised.
		89	Figure 10.12; Remarks revised.
		91	10.5.1; the second line from the bottom revised.
		94	10.6.1; Program example and 10.6.2 revised.
		95	Figure 11.1; After Reset of PRCR register: “00XXX000b” → “00h”
		98	12.1.3.1 revised.
		110	12.2.1 revised.
		116	Table 12.6 revised and NOTE2 added.
		120	12.7.3 revised and Watchdog Timer Interrupt deleted.
		121	Figure 12.21; NOTE2 revised.
		124	Figure 13.2; • OFS register NOTE1 revised. • After Reset of WDC register: “000xxxxxb” → “00X11111b”
		135	Figure 14.6 Comment; “0 (During count)” → “1 (During count)”
		146	14.1.6 revised.
		147	14.2; the second line from the top revised.
		150	Figure 14.16; TRBSC register NOTE3: “TRBPRE” → “TRBSC” TRBPR register NOTE2: “TRBPRE” → “TRBPR”
		153	Figure 14.18 Comment; “0 (During count)” → “1 (During count)”
		157	Table 14.9; NOTE2 added.
		162	Table 14.10; NOTE2 added.

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		Page	Summary
1.10	Oct 31, 2007	165	14.2.5 revised and 14.2.5.1 added.
		166	14.2.5.2 added.
		167	14.2.5.3 added.
		168	14.2.5.4 added.
		180	Figure 14.33; “input capture signal” added.
		193	Figure 14.46 revised.
		195	Table 14.25; Count Stop Conditions revised.
		211	Table 14.27; Count Stop Conditions revised.
		224	Table 14.29; Count Stop Conditions revised.
		231	Figure 14.84; NOTE1 revised.
		248	Table 14.33; Count Stop Conditions revised.
		261	14.3.12.1 and Table 14.36 revised.
		277	Figure 15.3; Registers U0BRG and U1BRG: “U0BRG” → “UiBRG”
		281	Table 15.1; NOTE2 revised.
		286	Table 15.4; NOTE1 revised.
		287	Table 15.5; NOTE2 added.
		288	Figure 15.10 revised.
		291	15.3; the fourth line from the top added.
		297	Figure 16.4; NOTE2 deleted.
		298	Figure 16.5; NOTE1 deleted.
		299	Figure 16.6; NOTE2 and NOTE7 revised.
		300	Figure 16.7; NOTE5 revised.
		301	Figure 16.8; SSTDR NOTE1 and SSRDR NOTE2 deleted.
		321	16.2.8.1 deleted.
		325	Figure 16.24; NOTE6 revised.
		326	Figure 16.25; NOTE5 deleted.
		327	Figure 16.26; NOTE3 revised and NOTE7 deleted.
		328	Figure 16.27; NOTE3 deleted.
		329	Figure 16.28; NOTE7 revised.
		334	Figure 16.32 revised.
		336	Figure 16.33 and Figure 16.34 revised.
		338	Figure 16.35 revised.
		339	Figure 16.36 revised.
		354	16.3.8.1 replaced and 16.3.8.2 added.
		360	Figure 17.5; Procedure of Hardware LIN Clear the status flags: “LINST register ← 0” → “LINST register ← 1”
		362	Figure 17.7 revised.

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		Page	Summary
1.10	Oct 31, 2007	363	Figure 17.8; Bit name in the TRAMR register: "MOD0 to 2 bits" → "Bits TMOD0 to TMOD2"
		364	Figure 17.9; Procedure of Hardware LIN Clear the status flags: "LINST register ← 0" → "LINST register ← 1"
		366	Figure 17.11; Bit name in the LINST register: "SCDCT flag" → "BCDCT flag"
		367	Figure 17.12; Procedure of Hardware LIN Clear the status flags: "LINST register ← 0" → "LINST register ← 1"
		401	Figure 19.2; NOTE4 revised.
		403	Table 19.2; Stop Condition revised.
		404	Figure 19.4; NOTE4 revised.
		407	Figure 19.6; NOTE4 revised.
		411	Figure 19.10 revised. SW5 added.
		412	19.6; the six line from the bottom: "A/D conversion mode with" → "A/D conversion mode without"
		413	19.7 revised.
		415	Table 20.2; Function of CPU Rewrite Mode: "any area other than the flash memory" → "the RAM"
		420	Figure 20.4; NOTE1 revised.
		421	Table 20.3; EW1 Mode: "ROM area" → "ROM or RAM area"
		422	20.4.1 and 20.4.2; "td(SR-ES)" → "td(SR-SUS)"
		423	20.4.2.4; the third line from the top: "in other than the flash memory" → "transferred to the RAM"
		424	20.4.2.15 revised.
		425	Figure 20.5; NOTE3 and NOTE5 revised.
		427	Figure 20.7; NOTE5 revised.
		429	Figure 20.9; "any area other than the flash memory" → "the RAM"
		430	Figure 20.11; • "any area other than the flash memory" → "the RAM" • "15us" → "30us" • NOTE4 deleted.
		432	20.4.3.4 revised.
		433	Figure 20.13 revised and NOTE4 added.
		435	Figure 20.15 revised and NOTE4 added.
		439	Table 20.7; MODE pin revised.
		447	Table 21.1 and Table 21.2 NOTE1; D version added.
		448	Table 21.3 NOTE1; D version added.
		449	Table 21.4; NOTE1 revised.

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		Page	Summary
1.10	Oct 31, 2007	450	Table 21.5 NOTE1; D version added.
		451	Table 21.6 NOTE1 and Table 21.7 NOTE1; D version added. Table 21.6; NOTE4 added.
		452	Table 21.8 NOTE1; D version added.
		453	Table 21.9 revised. Table 21.9 NOTE1 and Table 21.10 NOTE1; D version added. Table 21.11; NOTE1 revised.
		454	Table 21.12 NOTE1; D version added.
		458	Table 21.13 NOTE1; D version added.
		459	Table 21.14 NOTE1; D version added.
		460	Table 21.15; D version added.
		462	Table 21.19 and Figure 21.11; "(i = 0,2,3)" → "(i = 0 to 3)"
		466	Table 21.25 and Figure 21.15; "(i = 0,2,3)" → "(i = 0 to 3)"
		467	22.1.1; Program example and 22.1.2 revised.
		468	22.2.3 revised and Watchdog Timer Interrupt deleted.
		469	Figure 22.1; NOTE2 revised.
		471	22.3.1 revised.
		472	22.3.2 revised and 22.3.2.1 added.
		473	22.3.2.2 added.
		474	22.3.2.3 added.
		475	22.3.2.4 added.
		476	22.3.3.1 and Table 22.1 revised.
		483	22.4; the fourth line from the top added.
		484	22.5.2.1 replaced and 22.5.2.2 added.
		490	22.8 revised.
		495	23 revised.
		498	Appendix Figure 2.2 revised.
		499	Appendix Figure 3.1 NOTE1 revised.
2.00	Aug 20, 2008	–	"RENESAS TECHNICAL UPDATE" reflected: TN-16C-A172A/E
		5, 6	Table 1.3, Table 1.4 revised Figure 1.2, Figure 1.3; ROM number "XXX" added
		13, 14	Figure 3.1, Figure 3.2; "Expanding area" deleted
		23	Table 4.9 135Fh Address "XXXX0000b" → "00h"
		33	Figure 5.7 revised
		130	Figure 14.1 "TSTART" → "TCSTF", "TCKCUT bit" revised
		147	Figure 14.13 "TCSTF" → "TSTART" revised and added
		157	Table 14.9 "TRBP pin function" → "TRBO pin function"

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		Page	Summary
2.00	Aug 20, 2008	182, 196, 235, 249	Figure 14.34, Figure 14.48, Figure 14.87, Figure 14.99; "0137Dh" → "0137h"
		209	Figure 14.62 revised
		211	Table 14.27 revised
		278	Figure 15.4; NOTE3: "... 1 (internal clock) ..." → "... 0 (internal clock) ..."
		296	Figure 16.3 revised
		312	16.2.5.4 added
		315	Figure 16.18 revised
		361	Figure 17.6 revised
		364	Figure 17.9 revised
		376	Figure 18.7; NOTE2: "... operation mode." → "... reset/initialization mode."
		414	Table 20.1; NOTE1 revised
		437	Table 20.6 "FRM0 Register" → "FMR0 Register"
		447	Table 21.2; NOTE2 revised
		449	Table 21.4; NOTE2 and NOTE4 revised
		450	Table 21.5; NOTE2 and NOTE5 revised
		451	Table 21.6; "td(Vdet1-A)" added, NOTE5 added Table 21.7; "td(Vdet2-A)" and NOTE2 revised, NOTE5 added
		452	Table 21.8; "trth" and NOTE2 revised Figure 21.3 revised

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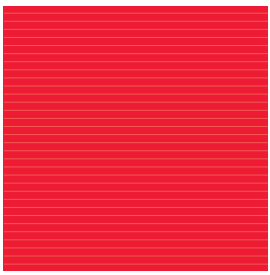

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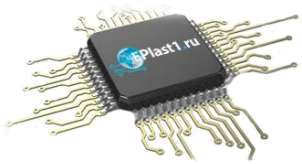

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