



## CMOS Static RAM 64K (8K x 8-Bit)

**IDT7164S**  
**IDT7164L**

### Features

- ◆ **High-speed address/chip select access time**
  - Military: 20/25/35/45/55/70/85/100ns (max.)
  - Industrial: 20/25ns (max.)
  - Commercial: 20/25ns (max.)
- ◆ **Low power consumption**
- ◆ **Battery backup operation – 2V data retention voltage (L Version only)**
- ◆ **Produced with advanced CMOS high-performance technology**
- ◆ **Inputs and outputs directly TTL-compatible**
- ◆ **Three-state outputs**
- ◆ **Available in 28-pin DIP, CERDIP and SOJ**
- ◆ **Military product compliant to MIL-STD-883, Class B**
- ◆ **Green parts available, see ordering information**

### Description

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available and the circuit offers a reduced power standby mode. When CS<sub>1</sub> goes HIGH or CS<sub>2</sub> goes LOW, the circuit will automatically go to, and remain in, a low-power standby mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil CERDIP, a 28-pin 600 mil CERDIP, 300mil Plastic DIP and 300mil SOJ

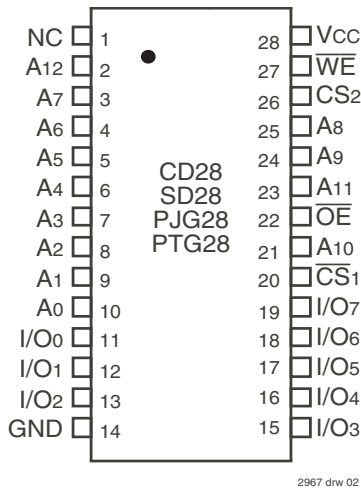
Military grade product is manufactured in compliance with MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

### Functional Block Diagram



**DECEMBER 2016**

## Pin Configurations



**DIP/SOJ  
Top View**

## Absolute Maximum Ratings<sup>(1)</sup>

| Symbol           | Rating                               | Com'l.       | Mil.         | Unit |
|------------------|--------------------------------------|--------------|--------------|------|
| $V_{TERM}^{(2)}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V    |
| $T_A$            | Operating Temperature                | 0 to +70     | -55 to +125  | °C   |
| $T_{BIAS}$       | Temperature Under Bias               | -55 to +125  | -65 to +135  | °C   |
| $T_{STG}$        | Storage Temperature                  | -55 to +125  | -65 to +150  | °C   |
| $P_T$            | Power Dissipation                    | 1.0          | 1.0          | W    |
| $I_{OUT}$        | DC Output Current                    | 50           | 50           | mA   |

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- $V_{TERM}$  must not exceed  $V_{CC} + 0.5V$ .

## Pin Descriptions

| Name                                | Description       |
|-------------------------------------|-------------------|
| A <sub>0</sub> - A <sub>12</sub>    | Address           |
| I/O <sub>0</sub> - I/O <sub>7</sub> | Data Input/Output |
| $\overline{CS}_1$                   | Chip Select       |
| CS <sub>2</sub>                     | Chip Select       |
| $\overline{WE}$                     | Write Enable      |
| $\overline{OE}$                     | Output Enable     |
| GND                                 | Ground            |
| V <sub>CC</sub>                     | Power             |

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## Truth Table<sup>(1,2,3)</sup>

| $\overline{WE}$ | $\overline{CS}_1$ | CS <sub>2</sub>                    | $\overline{OE}$ | I/O                 | Function                                 |
|-----------------|-------------------|------------------------------------|-----------------|---------------------|--|
| X               | H                 | X                                  | X               | High-Z              | Deselected - Standby (I <sub>SB</sub> )  |
| X               | X                 | L                                  | X               | High-Z              | Deselected - Standby (I <sub>SB</sub> )  |
| X               | V <sub>HC</sub>   | V <sub>HC</sub> or V <sub>LC</sub> | X               | High-Z              | Deselected - Standby (I <sub>SB1</sub> ) |
| X               | X                 | V <sub>LC</sub>                    | X               | High-Z              | Deselected - Standby (I <sub>SB1</sub> ) |
| H               | L                 | H                                  | H               | High-Z              | Output Disabled                          |
| H               | L                 | H                                  | L               | DATA <sub>OUT</sub> | Read Data                                |
| L               | L                 | H                                  | X               | DATA <sub>IN</sub>  | Write Data                               |

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### NOTES:

- CS<sub>2</sub> will power-down  $\overline{CS}_1$ , but  $\overline{CS}_1$  will not power-down CS<sub>2</sub>.
- H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = don't care.
- V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

## Recommended DC Operating Conditions

| Symbol          | Parameter          | Min.                | Typ. | Max.                  | Unit |
|-----------------|--------------------|---------------------|------|-----------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 4.5                 | 5.0  | 5.5                   | V    |
| GND             | Ground             | 0                   | 0    | 0                     | V    |
| V <sub>IH</sub> | Input HIGH Voltage | 2.2                 | —    | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub> | Input LOW Voltage  | -0.5 <sup>(1)</sup> | —    | 0.8                   | V    |

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### NOTE:

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 10ns, once per cycle.

## Recommended Operating Temperature and Supply Voltage

| Grade      | Temperature     | GND | V <sub>CC</sub> |
|------------|-----------------|-----|-----------------|
| Military   | -55°C to +125°C | 0V  | 5V ± 10%        |
| Industrial | -40°C to +85°C  | 0V  | 5V ± 10%        |
| Commercial | 0°C to +70°C    | 0V  | 5V ± 10%        |

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### Capacitance (TA = +25°C, f = 1.0MHz)

| Symbol          | Parameter <sup>(1)</sup> | Conditions            | Max. | Unit |
|-----------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub> | Input Capacitance        | V <sub>IN</sub> = 0V  | 8    | pF   |
| C <sub>VO</sub> | I/O Capacitance          | V <sub>OUT</sub> = 0V | 8    | pF   |

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**NOTE:**

1. This parameter is determined by device characterization, but is not production tested.

### DC Electrical Characteristics<sup>(1)</sup> (V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

| Symbol | Parameter   | Power | 7164S20<br>7164L20 |      |      | 7164S25<br>7164L25 |      |      | Unit |
|--------|---|-------|--------------------|------|------|--------------------|------|------|------|
|        |   |       | Com'l.             | Ind. | Mil. | Com'l.             | Ind. | Mil. |      |
| ICC1   | Operating Power Supply Current<br>CS <sub>1</sub> = V <sub>IL</sub> , CS <sub>2</sub> = V <sub>IH</sub> , Outputs Open<br>V <sub>CC</sub> = Max., f = 0 <sup>(2)</sup>  | S     | 100                | 110  | 110  | 90                 | 110  | 110  | mA   |
|        |   | L     | 90                 | 100  | 100  | 90                 | 100  | 100  |      |
| ICC2   | Dynamic Operating Current<br>CS <sub>1</sub> = V <sub>IL</sub> , CS <sub>2</sub> = V <sub>IH</sub> , Outputs Open<br>V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>  | S     | 170                | 170  | 180  | 170                | 170  | 180  | mA   |
|        |   | L     | 150                | 150  | 160  | 150                | 150  | 160  |      |
| ISB    | Standby Power Supply Current<br>(TTL Level), CS <sub>1</sub> ≥ V <sub>IH</sub> , CS <sub>2</sub> ≤ V <sub>IL</sub> ,<br>Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>                           | S     | 20                 | 20   | 20   | 20                 | 20   | 20   | mA   |
|        |   | L     | 3                  | 3    | 5    | 3                  | 3    | 5    |      |
| ISB1   | Full Standby Power Supply Current<br>(CMOS Level), f = 0 <sup>(2)</sup> , V <sub>CC</sub> = Max.<br>1. CS <sub>1</sub> ≥ V <sub>HC</sub> and CS <sub>2</sub> ≥ V <sub>HC</sub> , or<br>2. CS <sub>2</sub> ≤ V <sub>LC</sub> | S     | 15                 | 15   | 20   | 15                 | 15   | 20   | mA   |
|        |   | L     | 0.2                | 0.2  | 1    | 0.2                | 0.2  | 1    |      |

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| Symbol | Parameter   | Power | 7164S35<br>7164L35 | 7164S45<br>7164L45 | 7164S55<br>7164L55 | 7164S70<br>7164L70 | 7164S85/100<br>7164L85/100 | Unit |
|--------|---|-------|--------------------|--------------------|--------------------|--------------------|----------------------------|------|
|        |   |       | Mil.               | Mil.               | Mil.               | Mil.               | Mil.                       |      |
| ICC1   | Operating Power Supply Current<br>CS <sub>1</sub> = V <sub>IL</sub> , CS <sub>2</sub> = V <sub>IH</sub> , Outputs Open<br>V <sub>CC</sub> = Max., f = 0 <sup>(2)</sup>  | S     | 100                | 100                | 100                | 100                | 100                        | mA   |
|        |   | L     | 90                 | 90                 | 90                 | 90                 | 90                         |      |
| ICC2   | Dynamic Operating Current<br>CS <sub>1</sub> = V <sub>IL</sub> , CS <sub>2</sub> = V <sub>IH</sub> , Outputs Open<br>V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>  | S     | 160                | 160                | 160                | 160                | 160                        | mA   |
|        |   | L     | 140                | 130                | 125                | 120                | 120                        |      |
| ISB    | Standby Power Supply Current<br>(TTL Level), CS <sub>1</sub> ≥ V <sub>IH</sub> , CS <sub>2</sub> ≤ V <sub>IL</sub> ,<br>Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>                           | S     | 20                 | 20                 | 20                 | 20                 | 20                         | mA   |
|        |   | L     | 5                  | 5                  | 5                  | 5                  | 5                          |      |
| ISB1   | Full Standby Power Supply Current<br>(CMOS Level), f = 0 <sup>(2)</sup> , V <sub>CC</sub> = Max.<br>1. CS <sub>1</sub> ≥ V <sub>HC</sub> and CS <sub>2</sub> ≥ V <sub>HC</sub> , or<br>2. CS <sub>2</sub> ≤ V <sub>LC</sub> | S     | 20                 | 20                 | 20                 | 20                 | 20                         | mA   |
|        |   | L     | 1                  | 1                  | 1                  | 1                  | 1                          |      |

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**NOTES:**

1. All values are maximum guaranteed values.
2. f<sub>MAX</sub> = 1/TRC (all address inputs are cycling at f<sub>MAX</sub>); f = 0 means no address input lines are changing.

### DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

| Symbol          | Parameter              | Test Conditions   | IDT7164S             |        | IDT7164L |        | Unit   |    |
|-----------------|------------------------|---|----------------------|--------|----------|--------|--------|----|
|                 |                        |   | Min.                 | Max.   | Min.     | Max.   |        |    |
| I <sub>LI</sub> | Input Leakage Current  | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = GND to V <sub>CC</sub>                               | MIL.<br>COM'L. & IND | —<br>5 | 10<br>5  | —<br>2 | 5<br>2 | μA |
| I <sub>LO</sub> | Output Leakage Current | V <sub>CC</sub> = Max., $\overline{CS}_1 = V_{IH}$ ,<br>V <sub>OUT</sub> = GND to V <sub>CC</sub> | MIL.<br>COM'L. & IND | —<br>5 | 10<br>5  | —<br>2 | 5<br>2 | μA |
| V <sub>OL</sub> | Output Low Voltage     | I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.   | —                    | 0.4    | —        | 0.4    | V      |    |
|                 |                        | I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.  | —                    | 0.5    | —        | 0.5    | V      |    |
| V <sub>OH</sub> | Output High Voltage    | I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.  | 2.4                  | —      | 2.4      | —      | V      |    |

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### Data Retention Characteristics Over All Temperature Ranges (L Version Only) (V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

| Symbol                           | Parameter                            | Test Condition   | Min.                           | Typ. <sup>(1)</sup><br>V <sub>CC</sub> @ |          | Max.<br>V <sub>CC</sub> @ |           | Unit |
|----------------------------------|--------------------------------------|--|--------------------------------|--|----------|---------------------------|-----------|------|
|                                  |                                      |  |                                | 2.0V                                     | 3.0V     | 2.0V                      | 3.0V      |      |
| V <sub>DR</sub>                  | V <sub>CC</sub> for Data Retention   | —  | 2.0                            | —  | —        | —                         | —         | V    |
| I <sub>CCDR</sub>                | Data Retention Current               | MIL.<br>COM'L. & IND   | —<br>—                         | 10<br>10                                 | 15<br>15 | 200<br>60                 | 300<br>90 | μA   |
| t <sub>CDR</sub> <sup>(3)</sup>  | Chip Deselect to Data Retention Time | 1. $\overline{CS}_1 \geq V_{HC}$<br>CS <sub>2</sub> ≥ V <sub>HC</sub> , or<br>2. CS <sub>2</sub> ≤ V <sub>LC</sub> | 0                              | —  | —        | —                         | —         | ns   |
| t <sub>R</sub> <sup>(3)</sup>    | Operation Recovery Time              |  | t <sub>RC</sub> <sup>(2)</sup> | —  | —        | —                         | —         | ns   |
| I <sub>LI</sub>   <sup>(3)</sup> | Input Leakage Current                |  | —                              | —  | —        | 2                         | 2         | μA   |

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**NOTES:**

- TA = +25°C.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed by device characterization, but is not production tested.

### AC Test Conditions

|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise/Fall Times         | 5ns                 |
| Input Timing Reference Levels | 1.5V                |
| Output Reference Levels       | 1.5V                |
| AC Test Load                  | See Figures 1 and 2 |

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Figure 1. AC Test Load



Figure 2. AC Test Load

(for t<sub>CLZ1</sub>, t<sub>CLZ2</sub>, t<sub>OLZ</sub>, t<sub>CHZ1</sub>, t<sub>CHZ2</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, and t<sub>WHZ</sub>)

\*Includes scope and jig capacitances

**AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)**

| Symbol                             | Parameter  | 7164S20<br>7164L20 |      | 7164S25<br>7164L25 |      | Unit |
|------------------------------------|--|--------------------|------|--------------------|------|------|
|                                    |  | Min.               | Max. | Min.               | Max. |      |
| <b>Read Cycle</b>                  |  |                    |      |                    |      |      |
| t <sub>RC</sub>                    | Read Cycle Time  | 20                 | —    | 25                 | —    | ns   |
| t <sub>AA</sub>                    | Address Access Time  | —                  | 19   | —                  | 25   | ns   |
| t <sub>ACS1</sub> <sup>(1)</sup>   | Chip Select-1 Access Time                                      | —                  | 20   | —                  | 25   | ns   |
| t <sub>ACS2</sub> <sup>(1)</sup>   | Chip Select-2 Access Time                                      | —                  | 25   | —                  | 30   | ns   |
| t <sub>CLZ1,2</sub> <sup>(2)</sup> | Chip Select-1, 2 to Output in Low-Z                            | 5                  | —    | 5                  | —    | ns   |
| t <sub>OE</sub>                    | Output Enable to Output Valid                                  | —                  | 8    | —                  | 12   | ns   |
| t <sub>OLZ</sub> <sup>(2)</sup>    | Output Enable to Output in Low-Z                               | 0                  | —    | 0                  | —    | ns   |
| t <sub>CHZ1,2</sub> <sup>(2)</sup> | Chip Select-1,2 to Output in High-Z                            | —                  | 9    | —                  | 13   | ns   |
| t <sub>OHZ</sub> <sup>(2)</sup>    | Output Disable to Output in High-Z                             | —                  | 8    | —                  | 10   | ns   |
| t <sub>OH</sub>                    | Output Hold from Address Change                                | 5                  | —    | 5                  | —    | ns   |
| t <sub>PU</sub> <sup>(2)</sup>     | Chip Select to Power Up Time                                   | 0                  | —    | 0                  | —    | ns   |
| t <sub>PD</sub> <sup>(2)</sup>     | Chip Deselect to Power Down Time                               | —                  | 20   | —                  | 25   | ns   |
| <b>Write Cycle</b>                 |  |                    |      |                    |      |      |
| t <sub>WC</sub>                    | Write Cycle Time   | 20                 | —    | 25                 | —    | ns   |
| t <sub>CW1,2</sub>                 | Chip Select to End-of-Write                                    | 15                 | —    | 18                 | —    | ns   |
| t <sub>AW</sub>                    | Address Valid to End-of-Write                                  | 15                 | —    | 18                 | —    | ns   |
| t <sub>AS</sub>                    | Address Set-up Time  | 0                  | —    | 0                  | —    | ns   |
| t <sub>WP</sub>                    | Write Pulse Width  | 15                 | —    | 21                 | —    | ns   |
| t <sub>WR1</sub>                   | Write Recovery Time ( $\overline{CS}_1, \overline{WE}$ )       | 0                  | —    | 0                  | —    | ns   |
| t <sub>WR2</sub>                   | Write Recovery Time (CS <sub>2</sub> )                         | 5                  | —    | 5                  | —    | ns   |
| t <sub>WHZ</sub> <sup>(2)</sup>    | Write Enable to Output in High-Z                               | —                  | 8    | —                  | 10   | ns   |
| t <sub>DW</sub>                    | Data to Write Time Overlap                                     | 10                 | —    | 13                 | —    | ns   |
| t <sub>DH1</sub>                   | Data Hold from Write Time ( $\overline{CS}_1, \overline{WE}$ ) | 0                  | —    | 0                  | —    | ns   |
| t <sub>DH2</sub>                   | Data Hold from Write Time (CS <sub>2</sub> )                   | 5                  | —    | 5                  | —    | ns   |
| t <sub>OW</sub> <sup>(2)</sup>     | Output Active from End-of-Write                                | 4                  | —    | 4                  | —    | ns   |

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**NOTES:**

- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

**AC Electrical Characteristics (con't.) (Vcc = 5.0V ± 10%, Military Temperature Ranges)**

| Symbol                             | Parameter  | 7164S35<br>7164L35 |      | 7164S45<br>7164L45 |      | 7164S55<br>7164L55 |      | 7164S70<br>7164L70 |      | 7164S85/100<br>7164L85/100 |        | Unit |
|------------------------------------|--|--------------------|------|--------------------|------|--------------------|------|--------------------|------|----------------------------|--------|------|
|                                    |  | Max.               | Min. | Min.               | Max. | Min.               | Max. | Min.               | Max. | Min.                       | Max.   |      |
| <b>Read Cycle</b>                  |  |                    |      |                    |      |                    |      |                    |      |                            |        |      |
| t <sub>RC</sub>                    | Read Cycle Time  | 35                 | —    | 45                 | —    | 55                 | —    | 70                 | —    | 85/100                     | —      | ns   |
| t <sub>AA</sub>                    | Address Access Time  | —                  | 35   | —                  | 45   | —                  | 55   | —                  | 70   | —                          | 85/100 | ns   |
| t <sub>ACS1</sub> <sup>(1)</sup>   | Chip Select-1 Access Time                                      | —                  | 35   | —                  | 45   | —                  | 55   | —                  | 70   | —                          | 85/100 | ns   |
| t <sub>ACS2</sub> <sup>(1)</sup>   | Chip Select-2 Access Time                                      | —                  | 40   | —                  | 45   | —                  | 55   | —                  | 70   | —                          | 85/100 | ns   |
| t <sub>CLZ1,2</sub> <sup>(2)</sup> | Chip Select-1, 2 to Output in Low-Z                            | 5                  | —    | 5                  | —    | 5                  | —    | 5                  | —    | 5                          | —      | ns   |
| t <sub>OE</sub>                    | Output Enable to Output Valid                                  | —                  | 18   | —                  | 25   | —                  | 30   | —                  | 35   | —                          | 40     | ns   |
| t <sub>OLZ</sub> <sup>(2)</sup>    | Output Enable to Output in Low-Z                               | 0                  | —    | 0                  | —    | 0                  | —    | 0                  | —    | 0                          | —      | ns   |
| t <sub>CHZ1,2</sub> <sup>(2)</sup> | Chip Select-1,2 to Output in High-Z                            | —                  | 15   | —                  | 20   | —                  | 25   | —                  | 30   | —                          | 35     | ns   |
| t <sub>OHZ</sub> <sup>(2)</sup>    | Output Disable to Output in High-Z                             | —                  | 15   | —                  | 20   | —                  | 25   | —                  | 30   | —                          | 35     | ns   |
| t <sub>OH</sub>                    | Output Hold from Address Change                                | 5                  | —    | 5                  | —    | 5                  | —    | 5                  | —    | 5                          | —      | ns   |
| t <sub>PU</sub> <sup>(2)</sup>     | Chip Select to Power Up Time                                   | 0                  | —    | 0                  | —    | 0                  | —    | 0                  | —    | 0                          | —      | ns   |
| t <sub>PD</sub> <sup>(2)</sup>     | Chip Deselect to Power Down Time                               | —                  | 35   | —                  | 45   | —                  | 55   | —                  | 70   | —                          | 85/100 | ns   |
| <b>Write Cycle</b>                 |  |                    |      |                    |      |                    |      |                    |      |                            |        |      |
| t <sub>WC</sub>                    | Write Cycle Time   | 35                 | —    | 45                 | —    | 55                 | —    | 70                 | —    | 85/100                     | —      | ns   |
| t <sub>CW1,2</sub>                 | Chip Select to End-of-Write                                    | 25                 | —    | 33                 | —    | 50                 | —    | 60                 | —    | 75                         | —      | ns   |
| t <sub>AW</sub>                    | Address Valid to End-of-Write                                  | 25                 | —    | 33                 | —    | 50                 | —    | 60                 | —    | 75                         | —      | ns   |
| t <sub>AS</sub>                    | Address Set-up Time  | 0                  | —    | 0                  | —    | 0                  | —    | 0                  | —    | 0                          | —      | ns   |
| t <sub>WP</sub>                    | Write Pulse Width  | 25                 | —    | 25                 | —    | 50                 | —    | 60                 | —    | 75                         | —      | ns   |
| t <sub>WR1</sub>                   | Write Recovery Time ( $\overline{CS}_1, \overline{WE}$ )       | 0                  | —    | 0                  | —    | 0                  | —    | 0                  | —    | 0                          | —      | ns   |
| t <sub>WR2</sub>                   | Write Recovery Time (CS <sub>2</sub> )                         | 5                  | —    | 5                  | —    | 5                  | —    | 5                  | —    | 5                          | —      | ns   |
| t <sub>WHZ</sub> <sup>(2)</sup>    | Write Enable to Output in High-Z                               | —                  | 14   | —                  | 18   | —                  | 25   | —                  | 30   | —                          | 35     | ns   |
| t <sub>DW</sub>                    | Data to Write Time Overlap                                     | 15                 | —    | 20                 | —    | 25                 | —    | 30                 | —    | 35                         | —      | ns   |
| t <sub>DH1</sub>                   | Data Hold from Write Time ( $\overline{CS}_1, \overline{WE}$ ) | 0                  | —    | 0                  | —    | 0                  | —    | 0                  | —    | 0                          | —      | ns   |
| t <sub>DH2</sub>                   | Data Hold from Write Time (CS <sub>2</sub> )                   | 5                  | —    | 5                  | —    | 5                  | —    | 5                  | —    | 5                          | —      | ns   |
| t <sub>OW</sub> <sup>(2)</sup>     | Output Active from End-of-Write                                | 4                  | —    | 4                  | —    | 4                  | —    | 4                  | —    | 4                          | —      | ns   |

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**NOTES:**

- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

### Timing Waveform of Read Cycle No. 1<sup>(1)</sup>



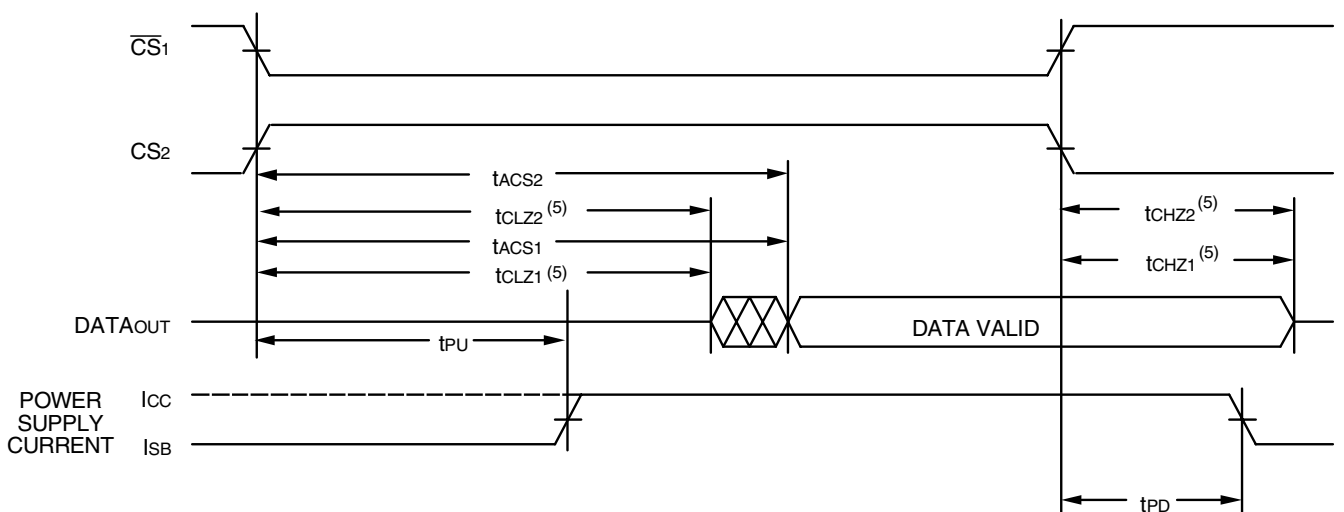
2967 drw 05

### Timing Waveform of Read Cycle No. 2<sup>(1,2,4)</sup>



2967 drw 06

### Timing Waveform of Read Cycle No. 3<sup>(1,3,4)</sup>

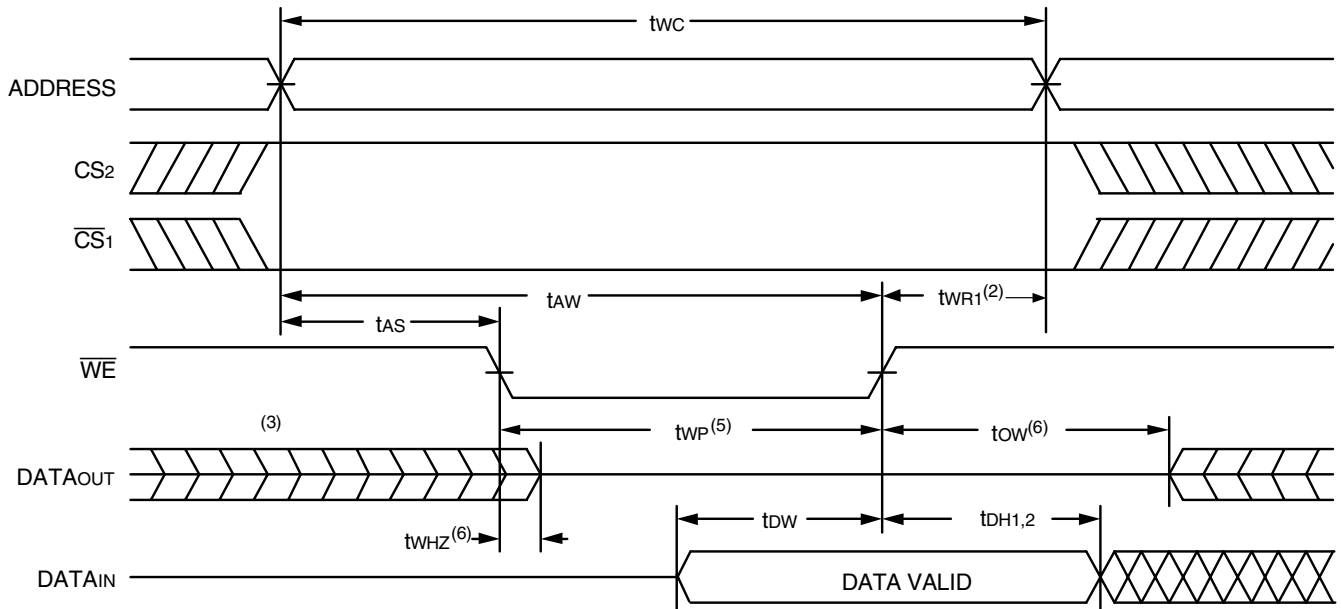


**NOTES:**

- $\overline{WE}$  is HIGH for Read cycle.
- Device is continuously selected,  $\overline{CS}_1$  is LOW,  $\overline{CS}_2$  is HIGH.
- Address valid prior to or coincident with  $\overline{CS}_1$  transition LOW and  $\overline{CS}_2$  transition HIGH.
- $\overline{OE}$  is LOW.
- Transition is measured  $\pm 200\text{mV}$  from steady state.

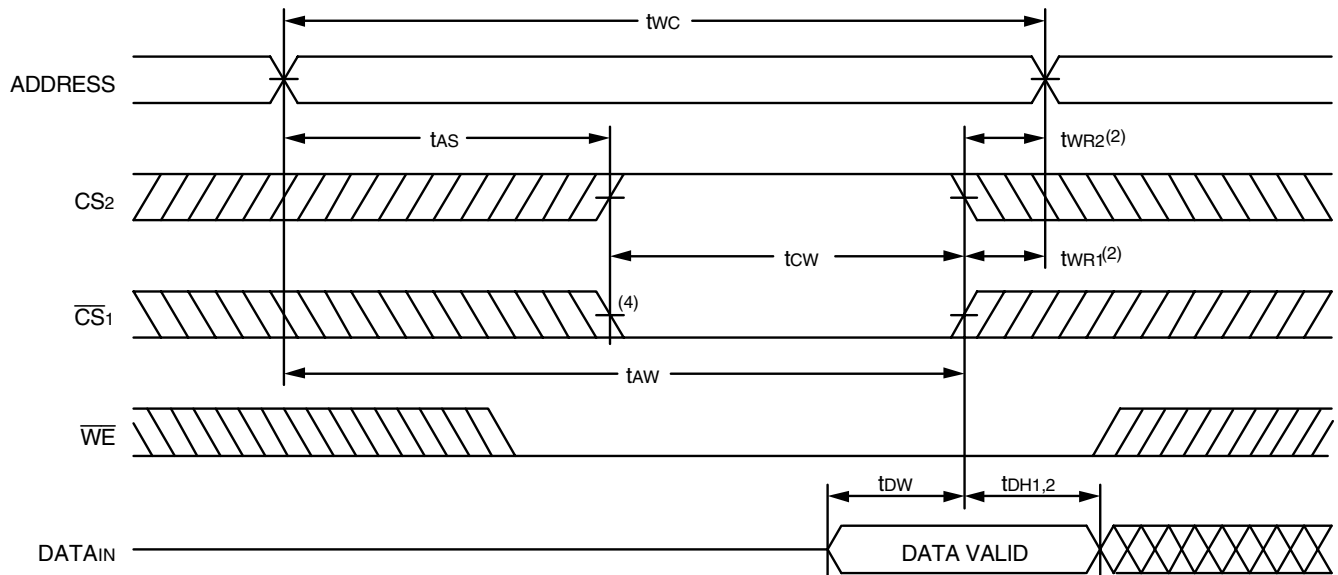
2967 drw 07

### Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled Timing)<sup>(1,5)</sup>



2967 drw 08

### Timing Waveform of Write Cycle No. 2 ( $\overline{CS}$ Controlled Timing)<sup>(1)</sup>



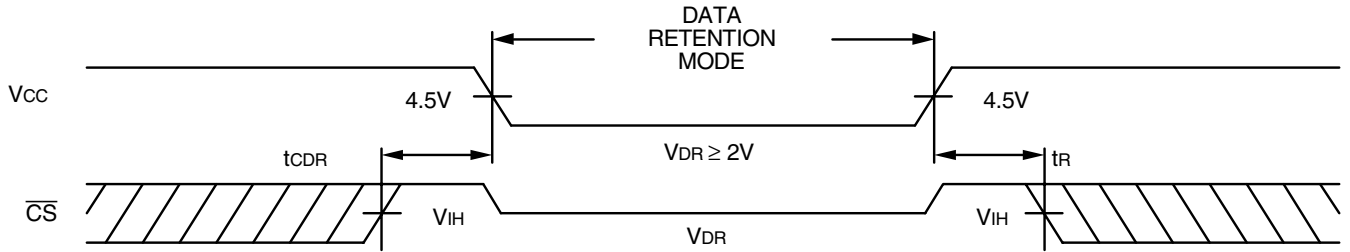
2967 drw 09

**NOTES:**

1. A write occurs during the overlap of a LOW  $\overline{WE}$ , a LOW  $\overline{CS}_1$  and a HIGH  $CS_2$ .
2.  $t_{WR1,2}$  is measured from the earlier of  $\overline{CS}_1$  or  $\overline{WE}$  going HIGH or  $CS_2$  going LOW to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the  $\overline{CS}_1$  LOW transition or  $CS_2$  HIGH transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
5.  $\overline{OE}$  is continuously HIGH. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WHZ} + t_{DW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified  $t_{WP}$ .
6. Transition is measured  $\pm 200mV$  from steady state.



## Low Vcc Data Retention Waveform



2967 drw 10

## Ordering Information

| 7164        | X     | XX    | XXX     | X | X                          | X |   |  |
|-------------|-------|-------|---------|---|----------------------------|---|---|--|
| Device Type | Power | Speed | Package |   | Process/ Temperature Range |   |   |  |
|             |       |       |         |   |                            |   | Blank 8                                       | Tube<br>Tape and Reel  |
|             |       |       |         |   |                            |   | Blank I <sup>(1)</sup><br>B                   | Commercial (0°C to +70°C)<br>Industrial (-40°C to +85°C)<br>Military (-55°C to +125°C)<br>Compliant with MIL-STD-883, Class B  |
|             |       |       |         |   |                            |   | G <sup>(2)</sup>                              | Green  |
|             |       |       |         |   |                            |   | Y<br>TP<br>D<br>TD                            | 300 mil SOJ (PJG28)<br>300 mil Plastic DIP (PTG28)<br>600 mil CERDIP (CD28)<br>300 mil CERDIP (SD28)   |
|             |       |       |         |   |                            |   | 20<br>25<br>35<br>45<br>55<br>70<br>85<br>100 | Commercial, Industrial & Military<br>Commercial, Industrial & Military<br>Military Only<br>Military Only<br>Military Only<br>Military Only<br>Military Only<br>Military Only |
|             |       |       |         |   |                            |   | S<br>L  | Standard Power<br>Low Power  |

} Speed in nanoseconds

2967 drw 11

### NOTES:

- Contact your local sales office for industrial temp range for other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your local sales office.

## Datasheet Document History

|          |                    |   |
|----------|--------------------|---|
| 01/13/00 |                    | Updated to new format   |
|          | Pp. 1, 2, 3, 5, 10 | Added Industrial Temperature range offerings  |
|          | Pp. 1, 3, 9        | Removed commercial 70ns speed grade offering  |
|          | Pp. 1, 3, 6, 10    | Added 100ns speed grade specification details   |
|          | Pg. 3              | Revised notes and footnotes in DC Electrical tables   |
|          | Pp. 5, 6           | Revised notes and footnotes in AC Electrical tables   |
|          | Pg. 8              | Removed Note 1 from Write Cycle No. 1 and No. 2 diagrams; renumbered notes and footnotes  |
|          | Pp. 9, 10          | Separated Ordering Information into commercial, industrial, and military offerings  |
|          | Pg. 11             | Added Datasheet Document History  |
| 08/09/00 |                    | Not recommended for new designs   |
| 02/01/01 |                    | Removed "Not recommended for new designs"   |
| 12/07/01 | Pg. 10             | Add PJ28 to Industrial temperature.   |
| 09/30/04 | Pg. 9,10           | Added "restricted hazardous substance device" to ordering information.  |
| 11/16/06 | Pg.3               | Added industrial temp power limits for 20ns part. Changed power limits for 25ns part for commercial and industrial. Changed power limits for commercial and industrial for 35ns part.                         |
|          | Pg.10              | Added 20ns part to ordering information. Refer to PCN SR-0602-01  |
| 02/20/07 | Pg. 9, 10          | Added L generation die step to data sheet ordering information.   |
| 04/27/11 | Pg. 1-3,5,6,9      | Obsoleted 24-pin 600 mil, 15ns for Commercial and 35ns for Industrial & Commercial.<br>Added Tape and Reel to Ordering information and updated description of Restricted hazardous substance device to Green. |
| 10/30/13 | Pg. 1              | In the Description: Removed reference to IDT's fabrication and removed "the latest revision of".  |
| 12/06/16 | Pg. 2              | Removed half moon from the pin configuration diagram for all packages to reflect pin 1 orientation and added dot at pin 1   |
|          |                    | Updated the package codes in the DIP/SOJ pin configuration  |
|          | Pg. 9              | Updated the package codes in the Ordering Information   |
|          |                    | Updated the BLANK designator from "Tube and Tray" to "Tube" in Ordering Information   |
|          | Pg. 1 & 9          | Added standard footnotes to Ordering Information with instructions for ordering Industrial temp and Green parts   |



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[7164S55TDB](#) [7164L45DB](#) [7164S100DB](#) [7164L70DB](#) [5962-3829414MZA](#) [5962-3829414MXA](#) [5962-3829406MZA](#)  
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