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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP55N055SDG is N-channel MOS Field Effect Transistor designed for high current switching applications.

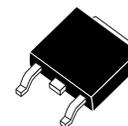
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP55N055SDG	TO-252 (MP-3ZK)

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
 $R_{DS(on)1} = 9.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 28 \text{ A)}$
- Low C_{iss} : $C_{iss} = 3200 \text{ pF TYP.}$
- Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	55	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	±20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	±55	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	±220	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	77	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	-55 to +175	°C
Repetitive Avalanche Current ^{Note2}	I_{AR}	27	A
Repetitive Avalanche Energy ^{Note2}	E_{AR}	73	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. $T_{ch} < 150^\circ\text{C}$, $V_{DD} = 28 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.95	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

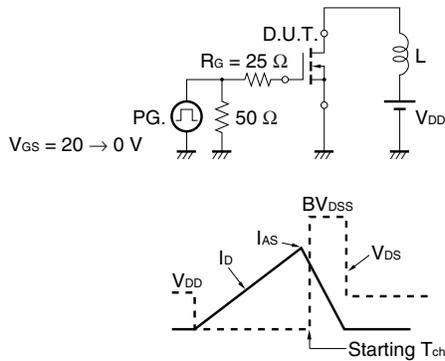
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

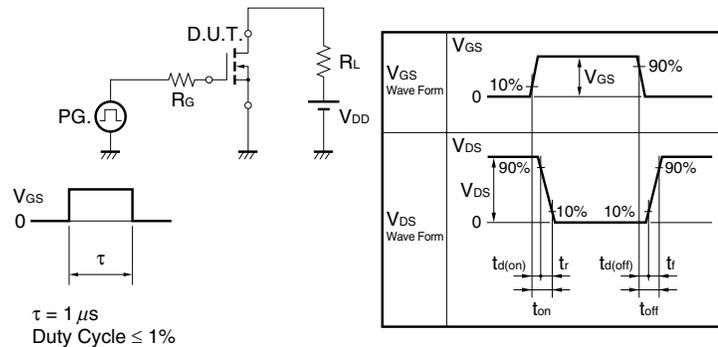
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			1.0	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 28 A	15	32		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 28 A		7.4	9.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 28 A		8.9	12	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V		3200	4800	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		270	410	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		170	310	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 28 A		17	38	ns
Rise Time	t _r	V _{GS} = 10 V		16	40	ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		71	142	ns
Fall Time	t _f			6	15	ns
Total Gate Charge	Q _G	V _{DD} = 44 V		64	96	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		10		nC
Gate to Drain Charge	Q _{GD}	I _D = 55 A		18		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 55 A, V _{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 55 A, V _{GS} = 0 V		35		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		38		nC

Note Pulsed

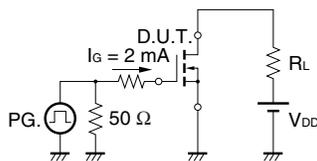
TEST CIRCUIT 1 AVALANCHE CAPABILITY



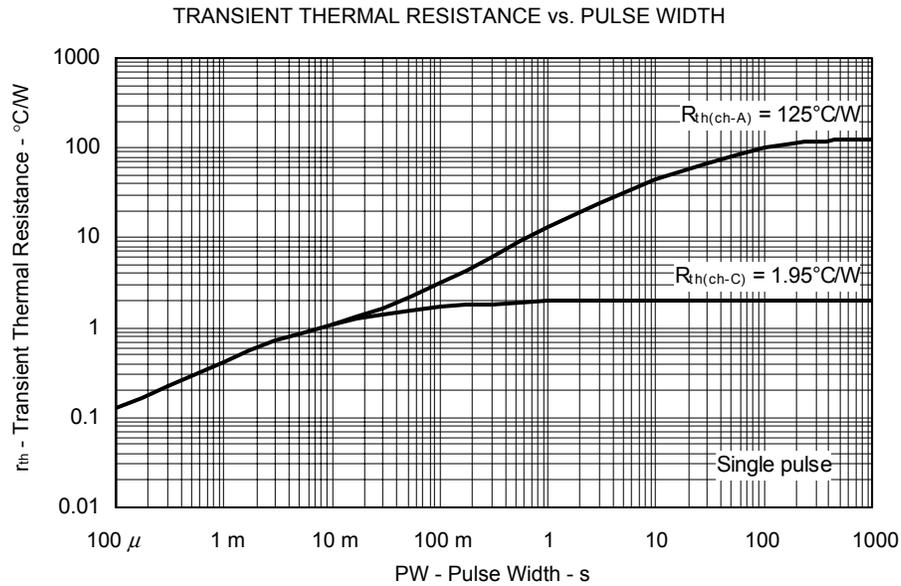
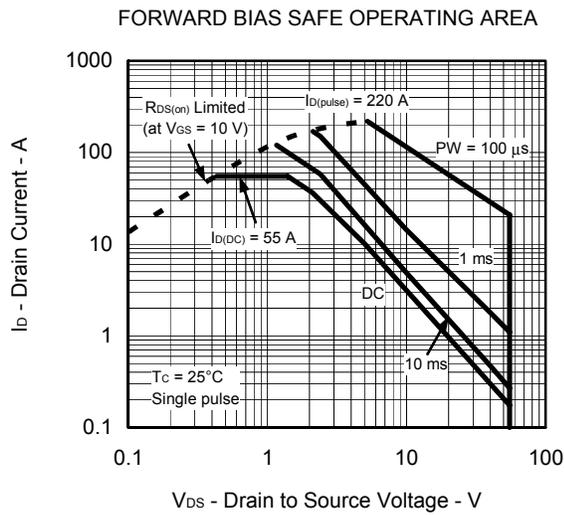
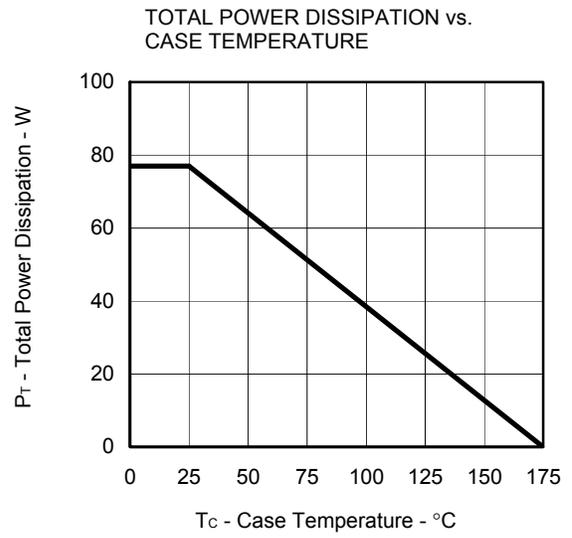
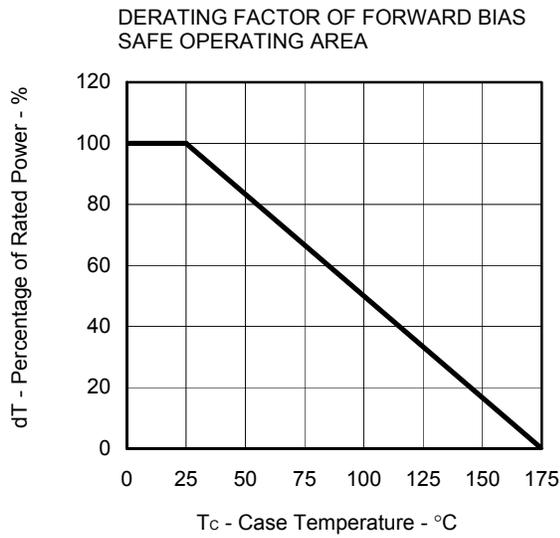
TEST CIRCUIT 2 SWITCHING TIME



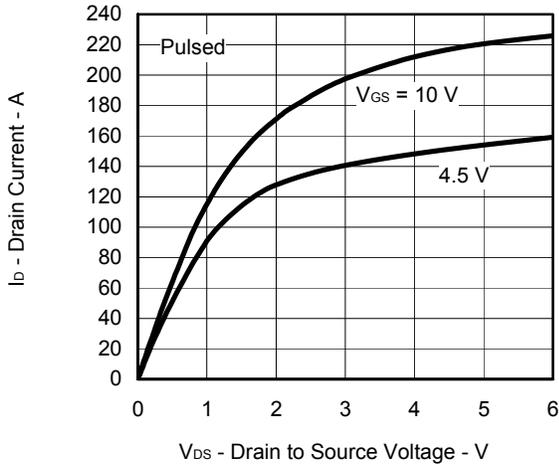
TEST CIRCUIT 3 GATE CHARGE



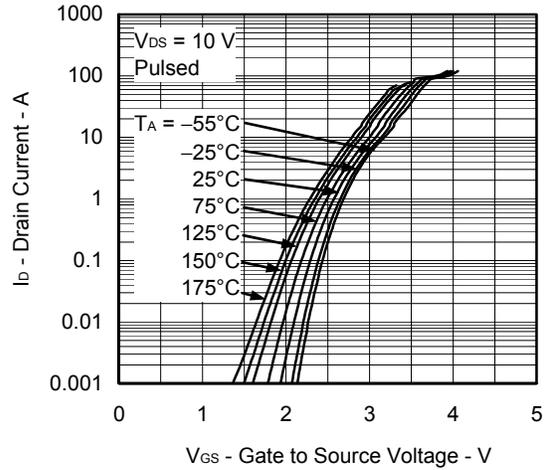
TYPICAL CHARACTERISTICS (T_A = 25°C)



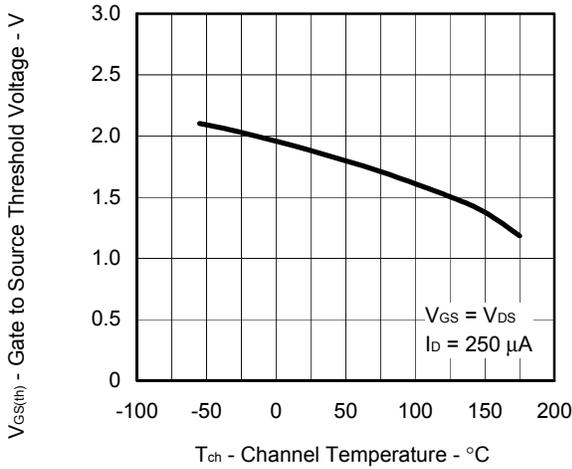
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



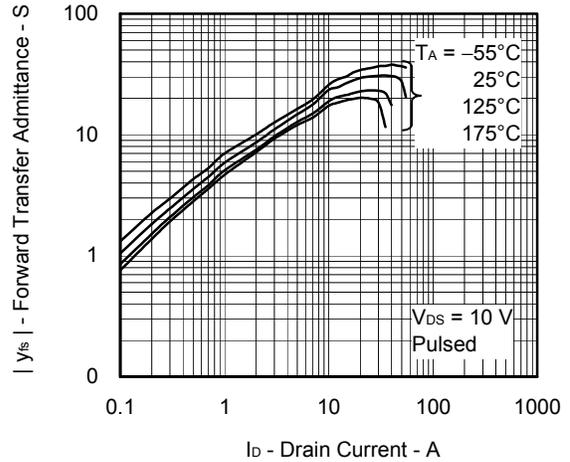
FORWARD TRANSFER CHARACTERISTICS



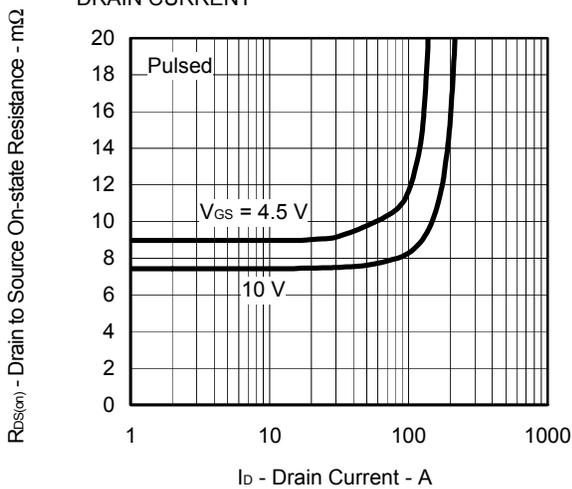
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



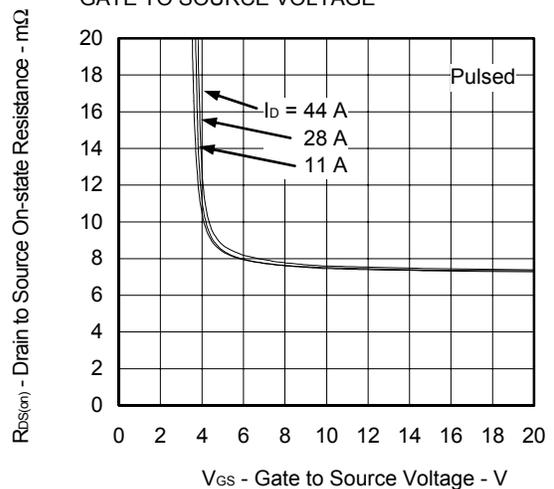
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



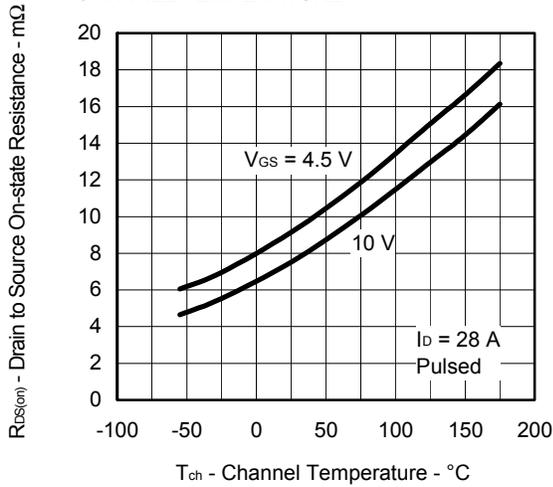
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



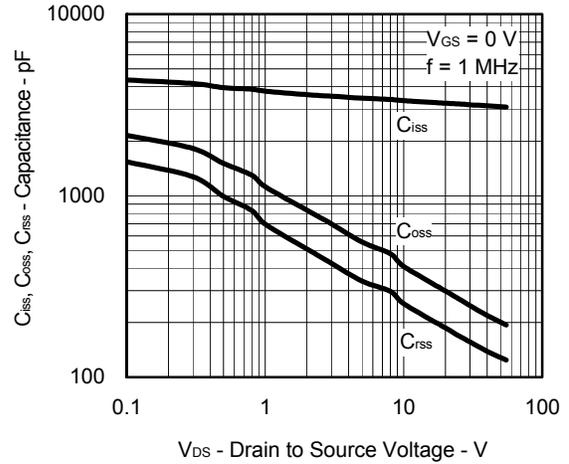
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



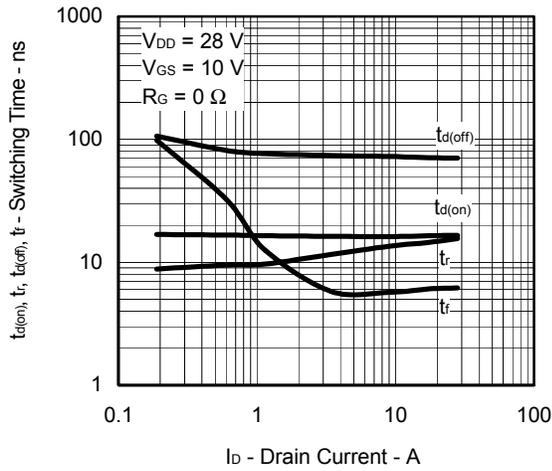
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



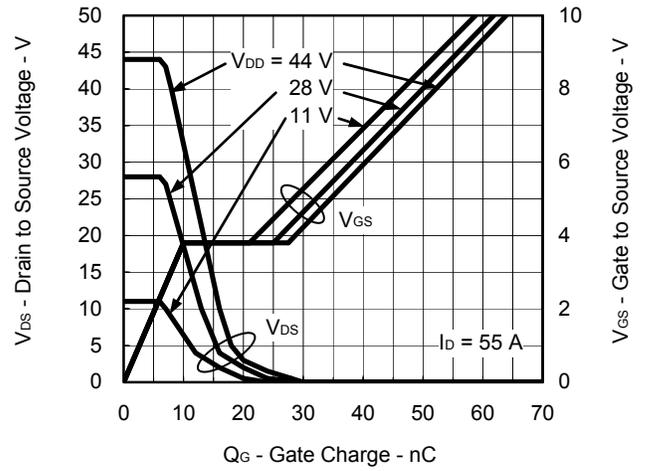
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



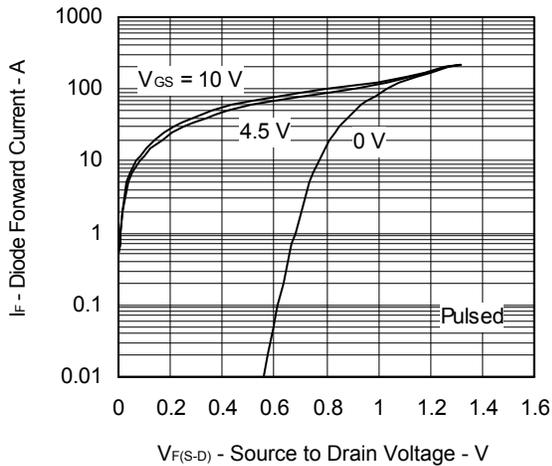
SWITCHING CHARACTERISTICS



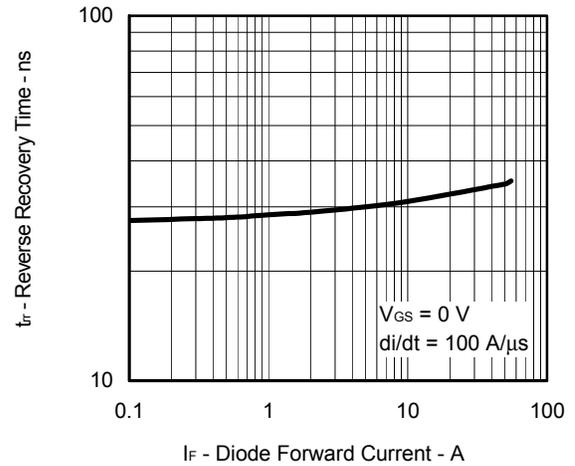
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

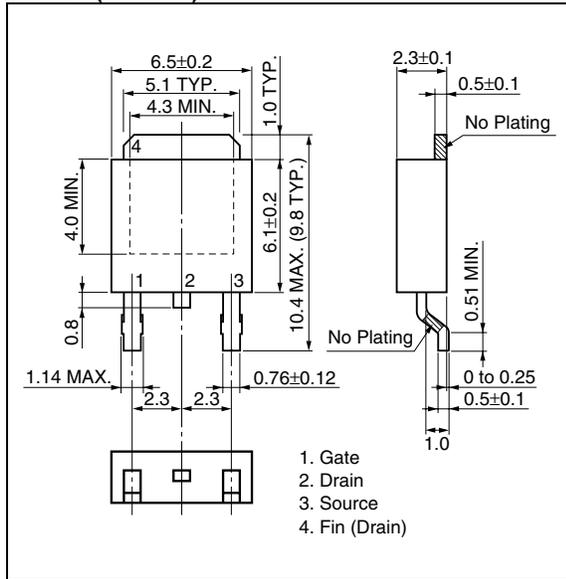


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

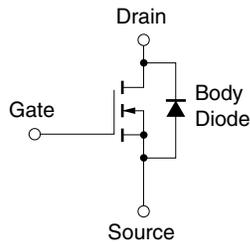


★ PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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