

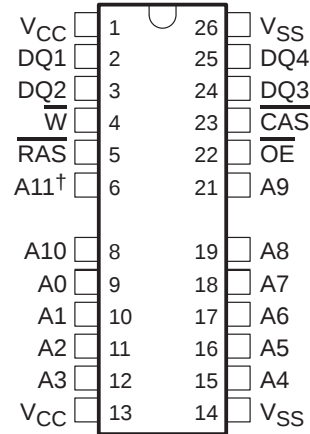
*This data sheet is applicable to all TMS41x400As symbolized by Revision "B", Revision "E" and subsequent revisions as described in the device symbolization section.*

- **Organization . . . 4194304 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **2048-Cycle Refresh in 32 ms for TMS417400A**
- **4096-Cycle Refresh in 64 ms for TMS416400A**
- **Performance Ranges:**

|             | ACCESS<br>TIME          | ACCESS<br>TIME          | ACCESS<br>TIME         | READ OR<br>WRITE<br>CYCLE<br>MIN |
|-------------|-------------------------|-------------------------|------------------------|----------------------------------|
|             | t <sub>RAC</sub><br>MAX | t <sub>CAC</sub><br>MAX | t <sub>AA</sub><br>MAX |                                  |
| '41x400A-50 | 50 ns                   | 13 ns                   | 25 ns                  | 90 ns                            |
| '41x400A-60 | 60 ns                   | 15 ns                   | 30 ns                  | 110 ns                           |
| '41x400A-70 | 70 ns                   | 18 ns                   | 35 ns                  | 130 ns                           |

- **Enhanced Page-Mode Operation With CAS-Before-RAS (CBR) Refresh**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 24/26-Lead 300-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package (DJ Suffix)**
- **Ambient Temperature Range:  
0°C to 70°C**

**DJ PACKAGE  
(TOP VIEW)**



**PIN NOMENCLATURE**

|                      |                        |
|----------------------|------------------------|
| A[0:11] <sup>†</sup> | Address Inputs         |
| CAS                  | Column-Address Strobe  |
| DQ[1:4]              | Data In/Data Out       |
| OE                   | Output Enable          |
| NC                   | No Internal Connection |
| RAS                  | Row-Address Strobe     |
| VCC                  | 5-V Supply             |
| VSS                  | Ground                 |
| W                    | Write Enable           |

<sup>†</sup> A11 is NC for TMS417400A

## description

The TMS41x400A is a set of 16 777 216-bit dynamic random-access memory (DRAMs) devices organized as 4194304 words of 4 bits each. The TMS41x400A employs state-of-the-art technology for high performance, reliability, and low power.

These devices feature maximum  $\overline{\text{RAS}}$  access times of 50-, 60-, and 70 ns. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416400A and TMS417400A are offered in a 24/26-lead plastic surface-mount SOJ package (DJ suffix). This package is designed for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

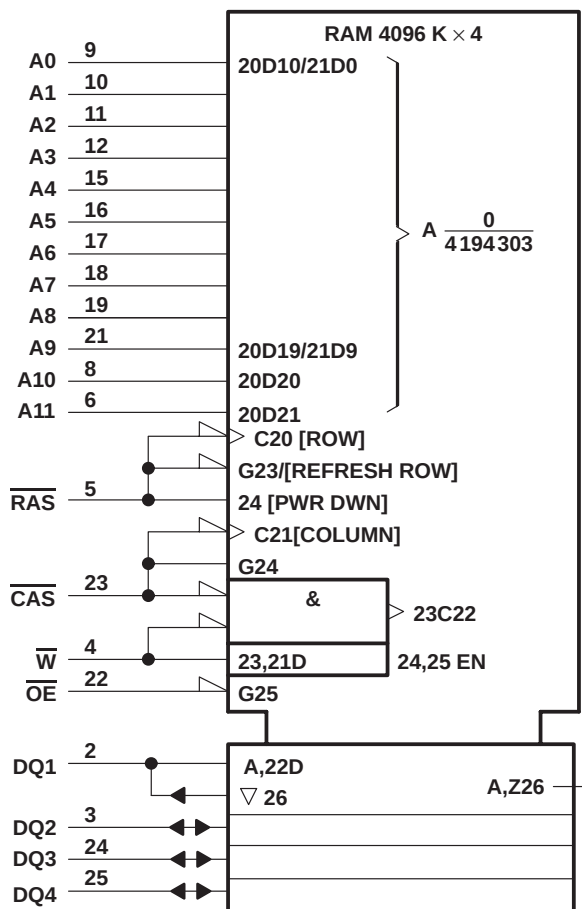
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**TMS416400A, TMS417400A**  
**4194304 BY 4-BIT**  
**DYNAMIC RANDOM-ACCESS MEMORIES**

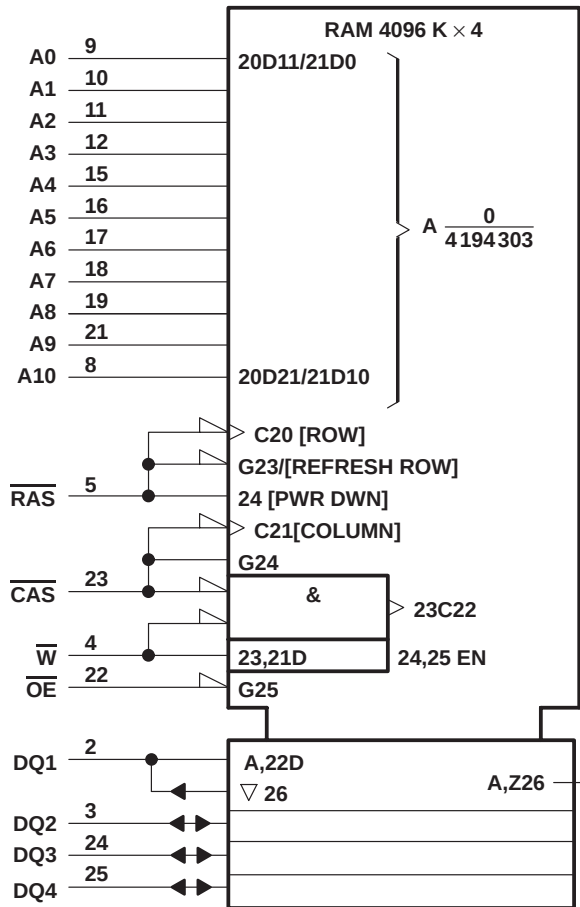
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**logic symbol (TMS416400A)<sup>†</sup>**



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

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# TMS416400A, TMS417400A

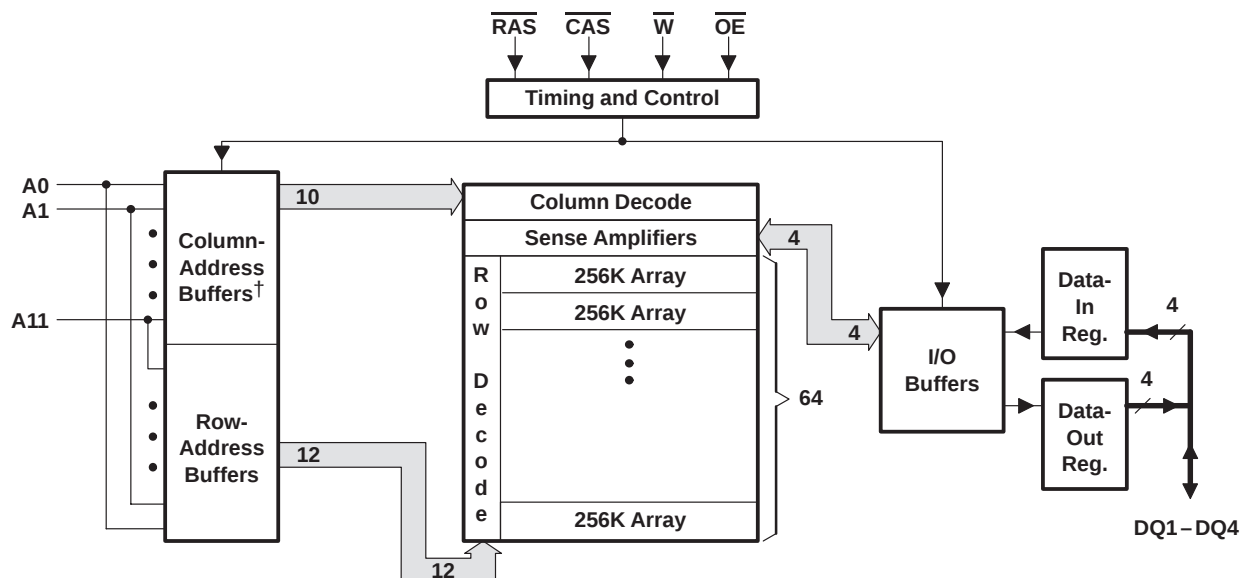
## 4194304 BY 4-BIT

### DYNAMIC RANDOM-ACCESS MEMORIES

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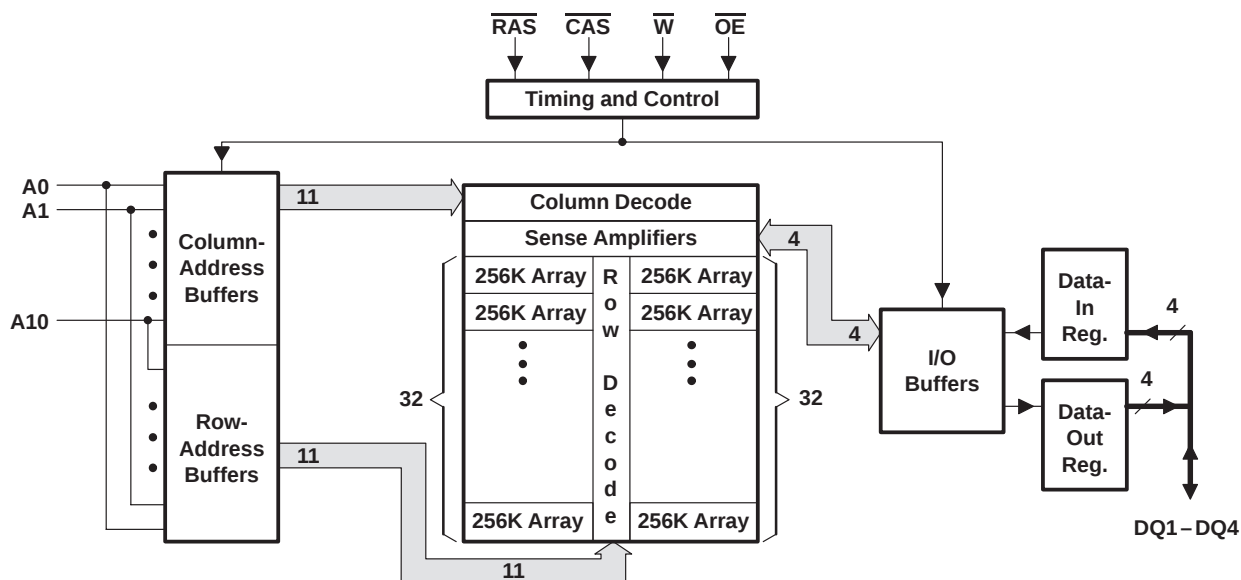
#### functional block diagram

##### TMS416400A



† Column addresses A10 and A11 are not used.

##### TMS417400A



## operation

### enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by  $t_{RASP}$ , the maximum  $\overline{RAS}$  low time.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of  $\overline{RAS}$ . The buffers act as transparent or flow-through latches while  $\overline{CAS}$  is high. The falling edge of  $\overline{CAS}$  latches the column addresses and enables the output. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode devices because data retrieval begins as soon as the column address is valid rather than when  $\overline{CAS}$  transitions low. This performance improvement is referred to as enhanced-page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of  $\overline{CAS}$ . In this case, data is obtained after  $t_{CAC}$  max (access time from  $\overline{CAS}$  low) if  $t_{AA}$  max (access time from column address) and  $t_{RAC}$  have been satisfied. In the event that column address for the next cycle is valid at the time  $\overline{CAS}$  goes high, access time for the next cycle is determined by the later occurrence of  $t_{CPA}$  or  $t_{CAC}$ .

### address: A0–A11 (TMS416400A) and A0–A10 (TMS417400A)

Twenty-two address bits are required to decode each of the 4194304 storage cell locations. For the TMS416400A, 12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe ( $\overline{RAS}$ ). Ten column-address bits are set up on A0 through A9. For TMS417400A, 11 row-address bits are set up on inputs A0 through A10 and latched onto the chip by  $\overline{RAS}$ . Eleven column-address bits are set up on A0 through A10. All addresses must be stable on or before the falling edge of  $\overline{RAS}$  and  $\overline{CAS}$ .  $\overline{RAS}$  is similar to a chip enable because it activates the sense amplifiers as well as the row decoder.  $\overline{CAS}$  is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

### write enable ( $\overline{W}$ )

The read- or write mode is selected through  $\overline{W}$ . A logic high on  $\overline{W}$  selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{CAS}$  (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with  $\overline{OE}$  grounded.

### data in (DQ1–DQ4)

Data is written during a write- or read-modify-write cycle. Depending on the mode of operation, the falling edge of  $\overline{CAS}$  or  $\overline{W}$  strobes data into the on-chip data latch. In an early-write cycle,  $\overline{W}$  is brought low prior to  $\overline{CAS}$ , and the data is strobed in by  $\overline{CAS}$  with setup-and-hold times referenced to this signal. In a delayed-write- or read-modify-write cycle,  $\overline{CAS}$  is already low, and the data is strobed in by  $\overline{W}$  with the setup-and-hold time referenced to this signal. Also,  $\overline{OE}$  must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

### data out (DQ1–DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until  $\overline{CAS}$  and  $\overline{OE}$  are brought low. In a read cycle, the output becomes valid after the access-time interval  $t_{CAC}$  (which begins with the negative transition of  $\overline{CAS}$ ) as long as  $t_{RAC}$  and  $t_{AA}$  are satisfied.

# TMS416400A, TMS417400A

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### DYNAMIC RANDOM-ACCESS MEMORIES

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#### $\overline{\text{RAS}}$ -only refresh

##### **TMS416400A**

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4 096 rows (A0–A11). A normal read- or write cycle refreshes all bits in each row that is selected. A  $\overline{\text{RAS}}$ -only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a  $\overline{\text{RAS}}$ -only refresh.

##### **TMS417400A**

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 2 048 rows (A0–A10). A normal read- or write cycle refreshes all bits in each row that is selected. A  $\overline{\text{RAS}}$ -only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a  $\overline{\text{RAS}}$ -only refresh.

#### hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding  $\overline{\text{CAS}}$  at  $V_{IL}$  after a read operation and cycling  $\overline{\text{RAS}}$  after a specified precharge period, similar to a  $\overline{\text{RAS}}$ -only refresh cycle. The external address is ignored, and the refresh address is generated internally.

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is utilized by bringing  $\overline{\text{CAS}}$  low earlier than  $\overline{\text{RAS}}$  (see parameter  $t_{CSR}$ ) and holding it low after  $\overline{\text{RAS}}$  falls (see parameter  $t_{CHR}$ ). For successive CBR refresh cycles,  $\overline{\text{CAS}}$  can remain low while cycling  $\overline{\text{RAS}}$ . The external address is ignored, and the refresh address is generated internally.

#### power up

To achieve proper device operation, an initial pause of 200  $\mu\text{s}$ , followed by a minimum of eight initialization cycles, is required after power up to the full  $V_{CC}$  level. These eight initialization cycles must include at least one refresh ( $\overline{\text{RAS}}$ -only or CBR) cycle.

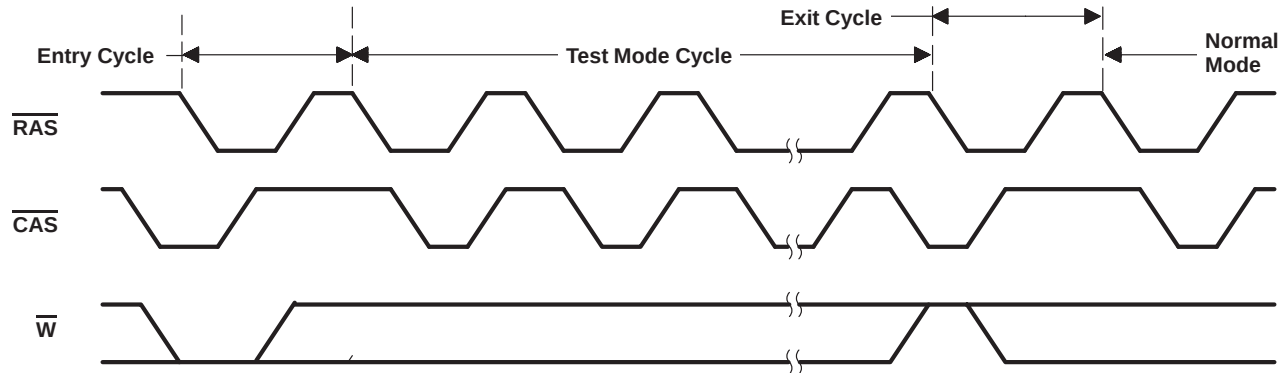
#### test mode

The test mode is initiated with a CBR-refresh cycle while simultaneously holding the  $\overline{\text{W}}$  input low. The entry cycle performs an internal-refresh cycle while internally setting the device to perform a parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits test mode if a CBR-refresh cycle (with  $\overline{\text{W}}$  held high) or a  $\overline{\text{RAS}}$ -only refresh cycle is performed.

In the test mode, the device is configured as 1 024K bits  $\times$  4 bits for each DQ. Each DQ pin has a separate 4-bit parallel-read- and write data bus that ignores column addresses A0 and A1. During a read cycle, the four internal bits are compared for each DQ pin separately. If the four bits agree, DQ goes high; if not, DQ goes low. Test time is reduced by a factor of four for this series of events.



test mode (continued)



NOTE A: The states of  $\overline{W}$ , data in, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

absolute maximum ratings over ambient temperature range (unless otherwise noted)<sup>†</sup>

|                                             |                 |
|---------------------------------------------|-----------------|
| Supply voltage range, V <sub>CC</sub>       | – 1 V to 7 V    |
| Voltage range on any pin (see Note 1)       | –1 V to 7 V     |
| Short-circuit output current                | 50 mA           |
| Power dissipation                           | 1 W             |
| Ambient temperature range, T <sub>A</sub>   | 0°C to 70°C     |
| Storage temperature range, T <sub>stg</sub> | – 55°C to 125°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V<sub>SS</sub>.

recommended operating conditions

|                                                      | TMS41x400A |     |     | UNIT |
|------------------------------------------------------|------------|-----|-----|------|
|                                                      | MIN        | NOM | MAX |      |
| V <sub>CC</sub> Supply voltage                       | 4.5        | 5   | 5.5 | V    |
| V <sub>SS</sub> Supply voltage                       |            | 0   |     | V    |
| V <sub>IH</sub> High-level input voltage             | 2.4        |     | 6.5 | V    |
| V <sub>IL</sub> Low-level input voltage (see Note 2) | – 1        |     | 0.8 | V    |
| T <sub>A</sub> Ambient temperature                   | 0          |     | 70  | °C   |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

**electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)**

**TMS416400A**

| PARAMETER           | TEST CONDITIONS†                                                                                                                                                    | '416400A-50 |      | '416400A-60 |      | '416400A-70 |      | UNIT |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|-------------|------|-------------|------|------|
|                     |                                                                                                                                                                     | MIN         | MAX  | MIN         | MAX  | MIN         | MAX  |      |
| V <sub>OH</sub>     | High-level output voltage<br>I <sub>OH</sub> = – 5 mA                                                                                                               | 2.4         |      | 2.4         |      | 2.4         |      | V    |
| V <sub>OL</sub>     | Low-level output voltage<br>I <sub>OL</sub> = 4.2 mA                                                                                                                |             | 0.4  |             | 0.4  |             | 0.4  | V    |
| I <sub>I</sub>      | Input current (leakage)<br>V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V to 6.5 V,<br>All others = 0 V to V <sub>CC</sub>                                           |             | ± 10 |             | ± 10 |             | ± 10 | µA   |
| I <sub>O</sub>      | Output current (leakage)<br>V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> ,<br>CAS high                                                          |             | ± 10 |             | ± 10 |             | ± 10 | µA   |
| I <sub>CC1</sub> ‡§ | Average read- or write-cycle current<br>V <sub>CC</sub> = 5.5 V, Minimum cycle                                                                                      |             | 100  |             | 80   |             | 70   | mA   |
| I <sub>CC2</sub>    | Average standby current<br>V <sub>IH</sub> = 2.4 V (TTL),<br>After one memory cycle,<br>RAS and CAS high                                                            |             | 2    |             | 2    |             | 2    | mA   |
|                     | V <sub>IH</sub> = V <sub>CC</sub> – 0.2 V (CMOS),<br>After one memory cycle,<br>RAS and CAS high                                                                    |             | 1    |             | 1    |             | 1    | mA   |
| I <sub>CC3</sub> ‡§ | Average refresh current (RAS-only refresh or CBR)<br>V <sub>CC</sub> = 5.5 V, Minimum cycle,<br>RAS cycling,<br>CAS high (RAS only),<br>RAS low after CAS low (CBR) |             | 100  |             | 80   |             | 70   | mA   |
| I <sub>CC4</sub> ‡¶ | Average page current<br>V <sub>CC</sub> = 5.5 V, t <sub>PC</sub> = MIN,<br>RAS low, CAS cycling                                                                     |             | 80   |             | 70   |             | 60   | mA   |

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while  $\overline{\text{RAS}} = V_{IL}$

¶ Measured with a maximum of one address change during each page-mode cycle, t<sub>PC</sub>.

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**electrical characteristics over recommended ranges of supply voltage and ambient temperature  
(unless otherwise noted) (continued)**

**TMS417400A**

| PARAMETER                      | TEST CONDITIONS <sup>†</sup>                                                                                                                                     | '417400A - 50 |      | '417400A - 60 |      | '417400A - 70 |      | UNIT |
|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------|---------------|------|---------------|------|------|
|                                |                                                                                                                                                                  | MIN           | MAX  | MIN           | MAX  | MIN           | MAX  |      |
| V <sub>OH</sub>                | High-level output voltage<br>I <sub>OH</sub> = – 5 mA                                                                                                            | 2.4           |      | 2.4           |      | 2.4           |      | V    |
| V <sub>OL</sub>                | Low-level output voltage<br>I <sub>OL</sub> = 4.2 mA                                                                                                             |               | 0.4  |               | 0.4  |               | 0.4  | V    |
| I <sub>I</sub>                 | Input current (leakage)<br>V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V to 6.5 V,<br>All others = 0 V to V <sub>CC</sub>                                        |               | ± 10 |               | ± 10 |               | ± 10 | µA   |
| I <sub>O</sub>                 | Output current (leakage)<br>V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> ,<br>CAS high                                                       |               | ± 10 |               | ± 10 |               | ± 10 | µA   |
| I <sub>CC1</sub> <sup>‡§</sup> | Average read- or write-cycle current<br>V <sub>CC</sub> = 5.5 V, Minimum cycle                                                                                   |               | 130  |               | 110  |               | 100  | mA   |
| I <sub>CC2</sub>               | Average standby current<br>V <sub>IH</sub> = 2.4 V (TTL),<br>After one memory cycle,<br>RAS and CAS high                                                         |               | 2    |               | 2    |               | 2    | mA   |
|                                | V <sub>IH</sub> = V <sub>CC</sub> – 0.2 V (CMOS),<br>After one memory cycle,<br>RAS and CAS high                                                                 |               | 1    |               | 1    |               | 1    | mA   |
| I <sub>CC3</sub> <sup>‡§</sup> | Average refresh current (RAS-only refresh or CBR)<br>V <sub>CC</sub> = 5.5 V, Minimum cycle,<br>RAS cycling, CAS high (RAS only),<br>RAS low after CAS low (CBR) |               | 130  |               | 110  |               | 100  | mA   |
| I <sub>CC4</sub> <sup>‡¶</sup> | Average page current<br>V <sub>CC</sub> = 5.5 V, t <sub>PC</sub> = MIN,<br>RAS low, CAS cycling                                                                  |               | 90   |               | 70   |               | 60   | mA   |

<sup>†</sup> For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

<sup>‡</sup> Measured with outputs open

<sup>§</sup> Measured with a maximum of one address change while RAS = V<sub>IL</sub>

<sup>¶</sup> Measured with a maximum of one address change during each page-mode cycle, t<sub>PC</sub>.



capacitance over recommended ranges of supply voltage and ambient temperature,  
f = 1 MHz (see Note 3)

| PARAMETER          |                                                          | MIN | MAX | UNIT |
|--------------------|----------------------------------------------------------|-----|-----|------|
| C <sub>i(A)</sub>  | Input capacitance, A0–A11 <sup>†</sup>                   |     | 5   | pF   |
| C <sub>i(OE)</sub> | Input capacitance, $\overline{OE}$                       |     | 7   | pF   |
| C <sub>i(RC)</sub> | Input capacitance, $\overline{CAS}$ and $\overline{RAS}$ |     | 7   | pF   |
| C <sub>i(W)</sub>  | Input capacitance, $\overline{W}$                        |     | 7   | pF   |
| C <sub>o</sub>     | Output capacitance <sup>‡</sup>                          |     | 7   | pF   |

<sup>†</sup> A11 is NC (no internal connection) for TMS417400A.

<sup>‡</sup>  $\overline{CAS} = V_{IH}$  to disable outputs.

NOTE 3:  $V_{CC} = 5\text{ V} \pm 10\%$ , and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature  
(see Note 4)

| PARAMETER        | '41x400A - 50                                                   |     | '41x400A - 60 |     | '41x400A - 70 |     | UNIT |
|------------------|-----------------------------------------------------------------|-----|---------------|-----|---------------|-----|------|
|                  | MIN                                                             | MAX | MIN           | MAX | MIN           | MAX |      |
| t <sub>AA</sub>  | Access time from column address                                 |     | 25            | 30  | 35            |     | ns   |
| t <sub>CAC</sub> | Access time from $\overline{CAS}$                               |     | 13            | 15  | 18            |     | ns   |
| t <sub>CPA</sub> | Access time from $\overline{CAS}$ precharge                     |     | 30            | 35  | 40            |     | ns   |
| t <sub>RAC</sub> | Access time from $\overline{RAS}$                               |     | 50            | 60  | 70            |     | ns   |
| t <sub>OEa</sub> | Access time from $\overline{OE}$                                |     | 13            | 15  | 18            |     | ns   |
| t <sub>CLZ</sub> | Delay time, $\overline{CAS}$ to output in low-impedance state   |     | 0             | 0   | 0             |     | ns   |
| t <sub>OH</sub>  | Output data hold time from $\overline{CAS}$                     |     | 3             | 3   | 3             |     | ns   |
| t <sub>OH0</sub> | Output data hold time from $\overline{OE}$                      |     | 3             | 3   | 3             |     | ns   |
| t <sub>OFF</sub> | Output buffer turn-off delay from $\overline{CAS}$ (see Note 5) |     | 0             | 13  | 0             | 18  | ns   |
| t <sub>OEZ</sub> | Output buffer turn-off delay from $\overline{OE}$ (see Note 5)  |     | 0             | 13  | 0             | 18  | ns   |

NOTES: 4. With ac parameters, it is assumed that  $t_T = 5\text{ ns}$ .

5. t<sub>OFF</sub> and t<sub>OEZ</sub> are specified when the output is no longer driven. Data-in should not be enabled until one of the maximum values is satisfied.

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**ac timing requirements (see Note 4)**

|                   |                                                                                    | '41x400A-50 |         | '41x400A-60 |         | '41x400A-70 |         | UNIT |
|-------------------|------------------------------------------------------------------------------------|-------------|---------|-------------|---------|-------------|---------|------|
|                   |                                                                                    | MIN         | MAX     | MIN         | MAX     | MIN         | MAX     |      |
| t <sub>RC</sub>   | Cycle time, read                                                                   | 90          |         | 110         |         | 130         |         | ns   |
| t <sub>WC</sub>   | Cycle time, write                                                                  | 90          |         | 110         |         | 130         |         | ns   |
| t <sub>RWC</sub>  | Cycle time, read-write                                                             | 131         |         | 155         |         | 181         |         | ns   |
| t <sub>PC</sub>   | Cycle time, page-mode read or write (see Note 6)                                   | 35          |         | 40          |         | 45          |         | ns   |
| t <sub>PRWC</sub> | Cycle time, page-mode read-write                                                   | 76          |         | 85          |         | 96          |         | ns   |
| t <sub>RASP</sub> | Pulse duration, $\overline{\text{RAS}}$ active, page mode (see Note 7)             | 50          | 100 000 | 60          | 100 000 | 70          | 100 000 | ns   |
| t <sub>RAS</sub>  | Pulse duration, $\overline{\text{RAS}}$ active, nonpage mode (see Note 7)          | 50          | 10 000  | 60          | 10 000  | 70          | 10 000  | ns   |
| t <sub>CAS</sub>  | Pulse duration, $\overline{\text{CAS}}$ active (see Note 8)                        | 13          | 10 000  | 15          | 10 000  | 18          | 10 000  | ns   |
| t <sub>CP</sub>   | Pulse duration, $\overline{\text{CAS}}$ precharge                                  | 8           |         | 10          |         | 10          |         | ns   |
| t <sub>RP</sub>   | Pulse duration, $\overline{\text{RAS}}$ precharge                                  | 30          |         | 40          |         | 50          |         | ns   |
| t <sub>WP</sub>   | Pulse duration, write command                                                      | 10          |         | 10          |         | 10          |         | ns   |
| t <sub>ASC</sub>  | Setup time, column address                                                         | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>ASR</sub>  | Setup time, row address                                                            | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>DS</sub>   | Setup time, data-in (see Note 9)                                                   | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>RCS</sub>  | Setup time, read command                                                           | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>CWL</sub>  | Setup time, write command before $\overline{\text{CAS}}$ precharge                 | 13          |         | 15          |         | 18          |         | ns   |
| t <sub>RWL</sub>  | Setup time, write command before $\overline{\text{RAS}}$ precharge                 | 13          |         | 15          |         | 18          |         | ns   |
| t <sub>WCS</sub>  | Setup time, write command before $\overline{\text{CAS}}$ active (early-write only) | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>WRP</sub>  | Setup time, write before $\overline{\text{RAS}}$ active (CBR refresh only)         | 10          |         | 10          |         | 10          |         | ns   |
| t <sub>WTS</sub>  | Setup time, write command before $\overline{\text{RAS}}$ active (test mode only)   | 10          |         | 10          |         | 10          |         | ns   |
| t <sub>CAH</sub>  | Hold time, column address                                                          | 10          |         | 10          |         | 15          |         | ns   |
| t <sub>DH</sub>   | Hold time, data-in (see Note 9)                                                    | 10          |         | 10          |         | 15          |         | ns   |
| t <sub>RAH</sub>  | Hold time, row address                                                             | 8           |         | 10          |         | 10          |         | ns   |
| t <sub>RCH</sub>  | Hold time, read command referenced to $\overline{\text{CAS}}$ (see Note 10)        | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>RRH</sub>  | Hold time, read command referenced to $\overline{\text{RAS}}$ (see Note 10)        | 0           |         | 0           |         | 0           |         | ns   |
| t <sub>WCH</sub>  | Hold time, write command during $\overline{\text{CAS}}$ active (early-write only)  | 10          |         | 10          |         | 15          |         | ns   |
| t <sub>RHCP</sub> | Hold time, $\overline{\text{RAS}}$ active from $\overline{\text{CAS}}$ precharge   | 30          |         | 35          |         | 40          |         | ns   |
| t <sub>OEH</sub>  | Hold time, $\overline{\text{OE}}$ command                                          | 13          |         | 15          |         | 18          |         | ns   |
| t <sub>ROH</sub>  | Hold time, $\overline{\text{RAS}}$ referenced to $\overline{\text{OE}}$            | 10          |         | 10          |         | 10          |         | ns   |
| t <sub>WRH</sub>  | Hold time, write after $\overline{\text{RAS}}$ active (CBR refresh only)           | 10          |         | 10          |         | 10          |         | ns   |
| t <sub>WTH</sub>  | Hold time, write command after $\overline{\text{RAS}}$ active (test mode only)     | 10          |         | 10          |         | 10          |         | ns   |

- NOTES:
4. With ac parameters, it is assumed that  $t_T = 5$  ns.
  6. To assure  $t_{PC}$  min,  $t_{ASC}$  should be  $\geq t_{CP}$ .
  7. In a read-write cycle,  $t_{RWD}$  and  $t_{RWL}$  must be observed.
  8. In a read-write cycle,  $t_{CWD}$  and  $t_{CWL}$  must be observed.
  9. Referenced to the later of  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$  in write operations
  10. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.

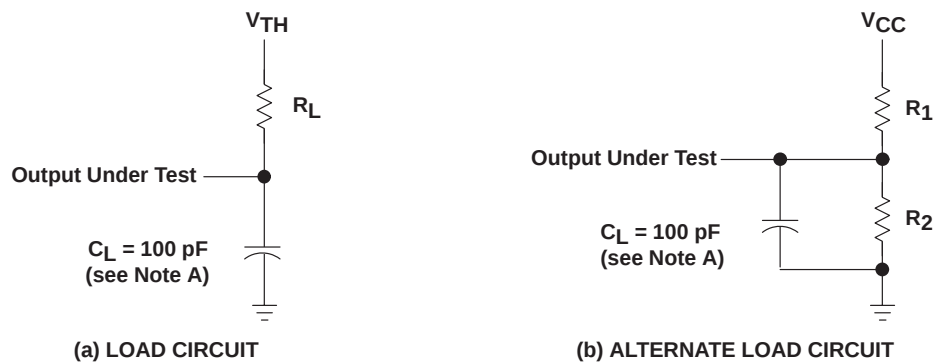


**ac timing requirements (see Note 4) (continued)**

|                   |                                                                                              |          | '41x400A - 50 |     | '41x400A - 60 |     | '41x400A - 70 |     | UNIT |
|-------------------|----------------------------------------------------------------------------------------------|----------|---------------|-----|---------------|-----|---------------|-----|------|
|                   |                                                                                              |          | MIN           | MAX | MIN           | MAX | MIN           | MAX |      |
| t <sub>AWD</sub>  | Delay time, column address to write command (read-write operation only)                      |          | 48            |     | 55            |     | 63            |     | ns   |
| t <sub>CHR</sub>  | Delay time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$ (CBR refresh only) |          | 10            |     | 10            |     | 10            |     | ns   |
| t <sub>CRP</sub>  | Delay time, $\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$                     |          | 5             |     | 5             |     | 5             |     | ns   |
| t <sub>CSH</sub>  | Delay time, $\overline{\text{RAS}}$ active to $\overline{\text{CAS}}$ precharge              |          | 50            |     | 60            |     | 70            |     | ns   |
| t <sub>CSR</sub>  | Delay time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$ (CBR refresh only) |          | 5             |     | 5             |     | 5             |     | ns   |
| t <sub>CWD</sub>  | Delay time, $\overline{\text{CAS}}$ to write command (read-write operation only)             |          | 36            |     | 40            |     | 46            |     | ns   |
| t <sub>OED</sub>  | Delay time, $\overline{\text{OE}}$ to data in                                                |          | 13            |     | 15            |     | 18            |     | ns   |
| t <sub>RAD</sub>  | Delay time, $\overline{\text{RAS}}$ to column address (see Note 11)                          |          | 13            | 25  | 15            | 30  | 15            | 35  | ns   |
| t <sub>RAL</sub>  | Delay time, column address to $\overline{\text{RAS}}$ precharge                              |          | 25            |     | 30            |     | 35            |     | ns   |
| t <sub>CAL</sub>  | Delay time, column address to $\overline{\text{CAS}}$ precharge                              |          | 25            |     | 30            |     | 35            |     | ns   |
| t <sub>RCD</sub>  | Delay time, $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ (see Note 11)                 |          | 18            | 37  | 20            | 45  | 20            | 52  | ns   |
| t <sub>RPC</sub>  | Delay time, $\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ active              |          | 5             |     | 5             |     | 5             |     | ns   |
| t <sub>RSH</sub>  | Delay time, $\overline{\text{CAS}}$ active to $\overline{\text{RAS}}$ precharge              |          | 13            |     | 15            |     | 18            |     | ns   |
| t <sub>RWD</sub>  | Delay time, $\overline{\text{RAS}}$ to write command (read-write operation only)             |          | 73            |     | 85            |     | 98            |     | ns   |
| t <sub>CPW</sub>  | Delay time, $\overline{\text{CAS}}$ precharge to write command (read-write only)             |          | 53            |     | 60            |     | 68            |     | ns   |
| t <sub>TAA</sub>  | Access time from address (test mode)                                                         |          | 30            |     | 35            |     | 40            |     | ns   |
| t <sub>TCPA</sub> | Access time from column precharge (test mode)                                                |          | 35            |     | 40            |     | 45            |     | ns   |
| t <sub>TRAC</sub> | Access time from $\overline{\text{RAS}}$ (test mode)                                         |          | 55            |     | 65            |     | 75            |     | ns   |
| t <sub>REF</sub>  | Refresh time interval                                                                        | '416400A | 64            |     | 64            |     | 64            |     | ms   |
|                   |                                                                                              | '417400A | 32            |     | 32            |     | 32            |     |      |
| t <sub>T</sub>    | Transition time                                                                              |          | 2             | 30  | 2             | 30  | 2             | 30  | ns   |

NOTES: 4. With ac parameters, it is assumed that  $t_T = 5$  ns.  
 11. The maximum value is specified only to ensure access time.

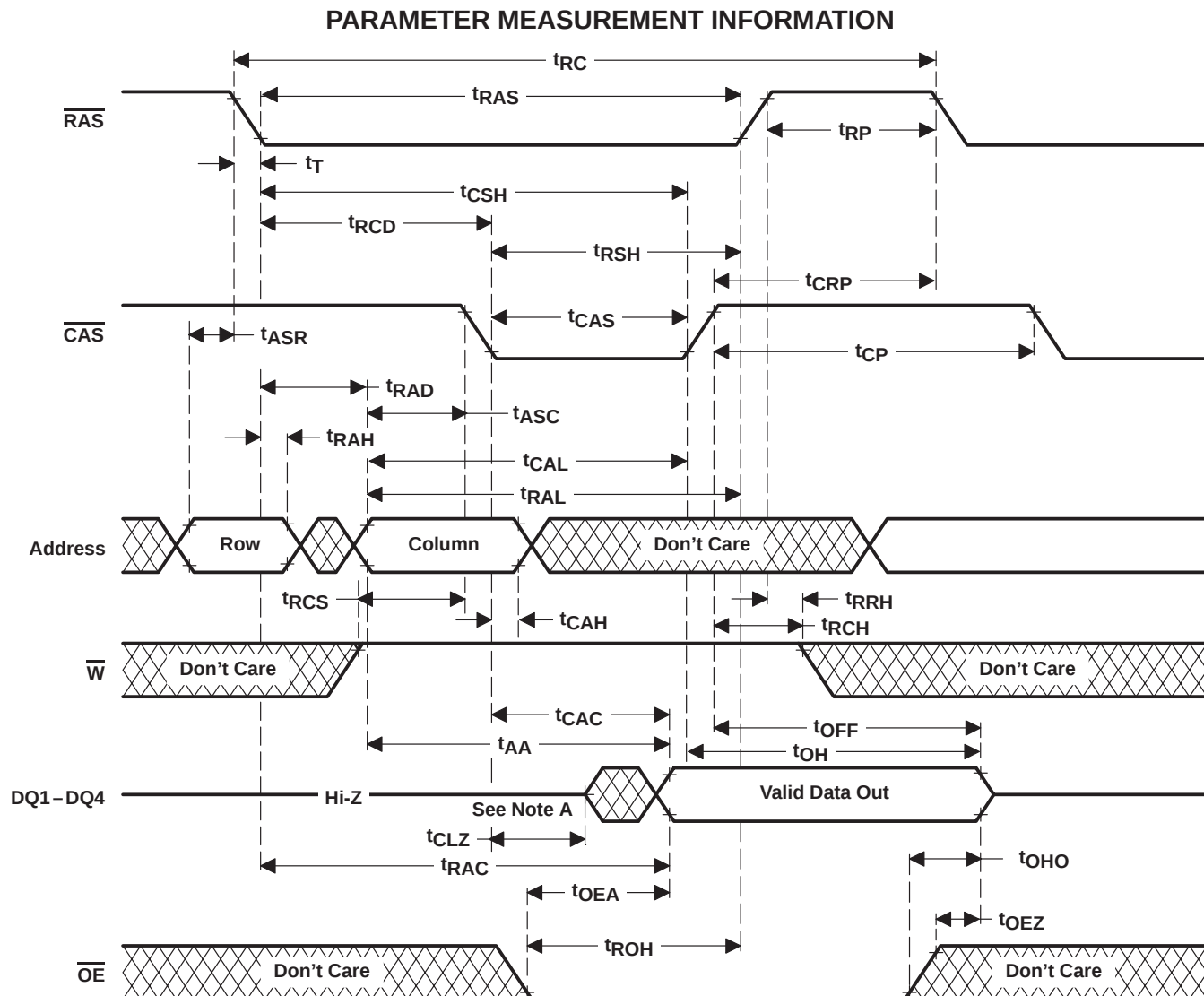
**PARAMETER MEASUREMENT INFORMATION**



NOTE A:  $C_L$  includes probe and fixture capacitance.

| DEVICE   | $V_{CC}$ (V) | $R_1$ ( $\Omega$ ) | $R_2$ ( $\Omega$ ) | $V_{TH}$ (V) | $R_L$ ( $\Omega$ ) |
|----------|--------------|--------------------|--------------------|--------------|--------------------|
| '41x400A | 5            | 828                | 295                | 1.31         | 218                |

**Figure 2. Load Circuits for Timing Parameters**



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

**Figure 3. Read-Cycle Timing**

# PARAMETER MEASUREMENT INFORMATION

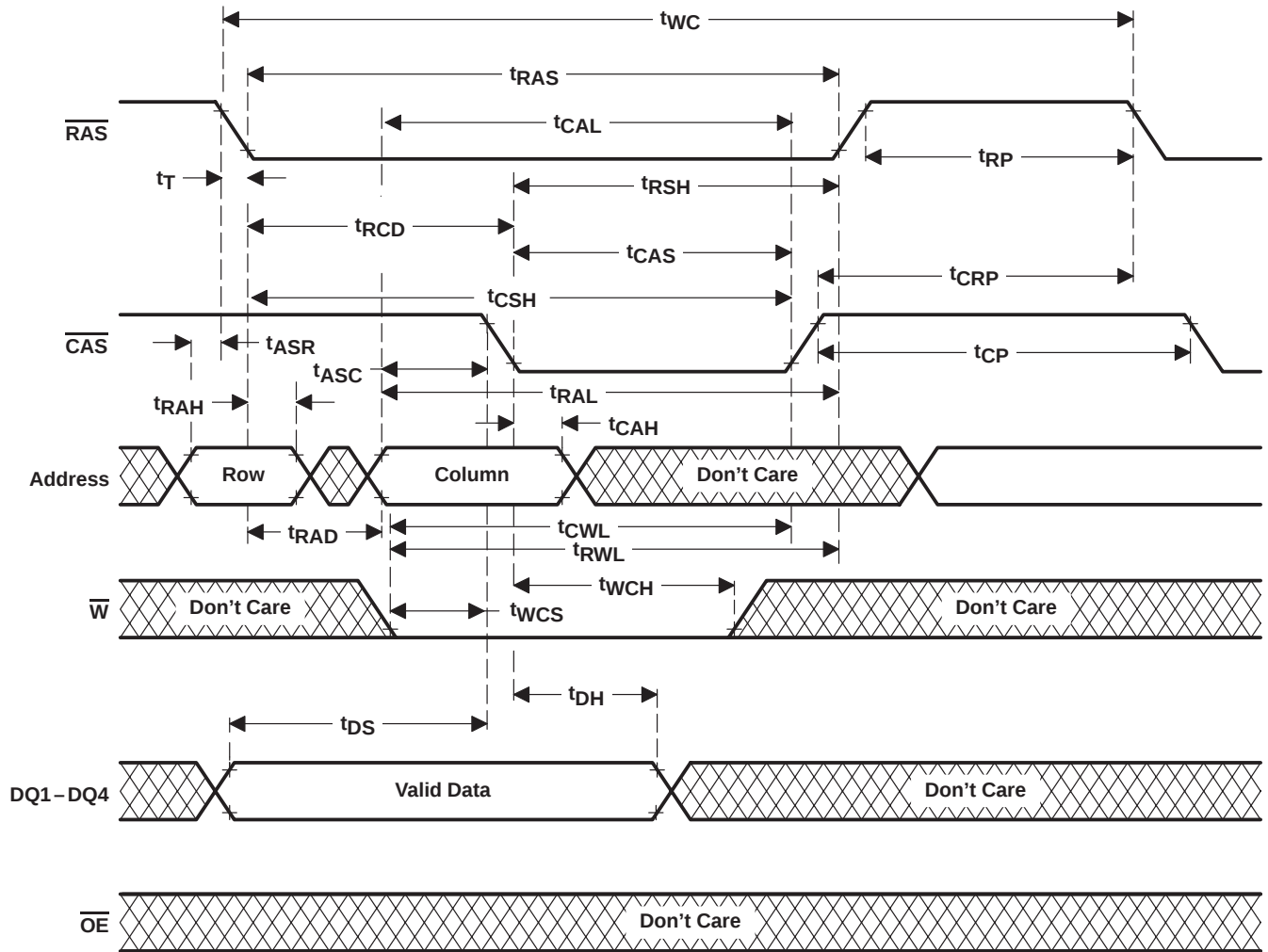


Figure 4. Early-Write-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

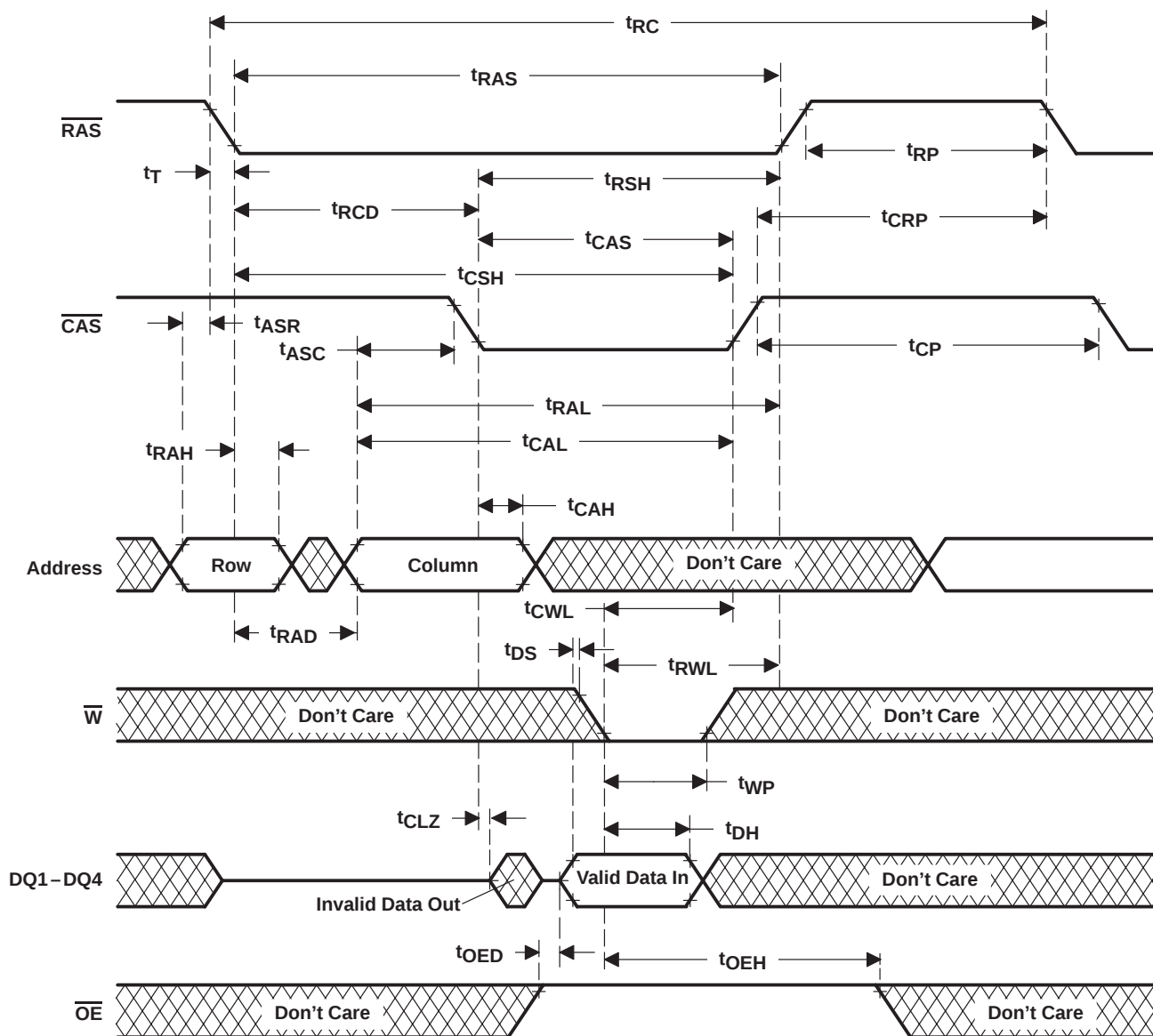
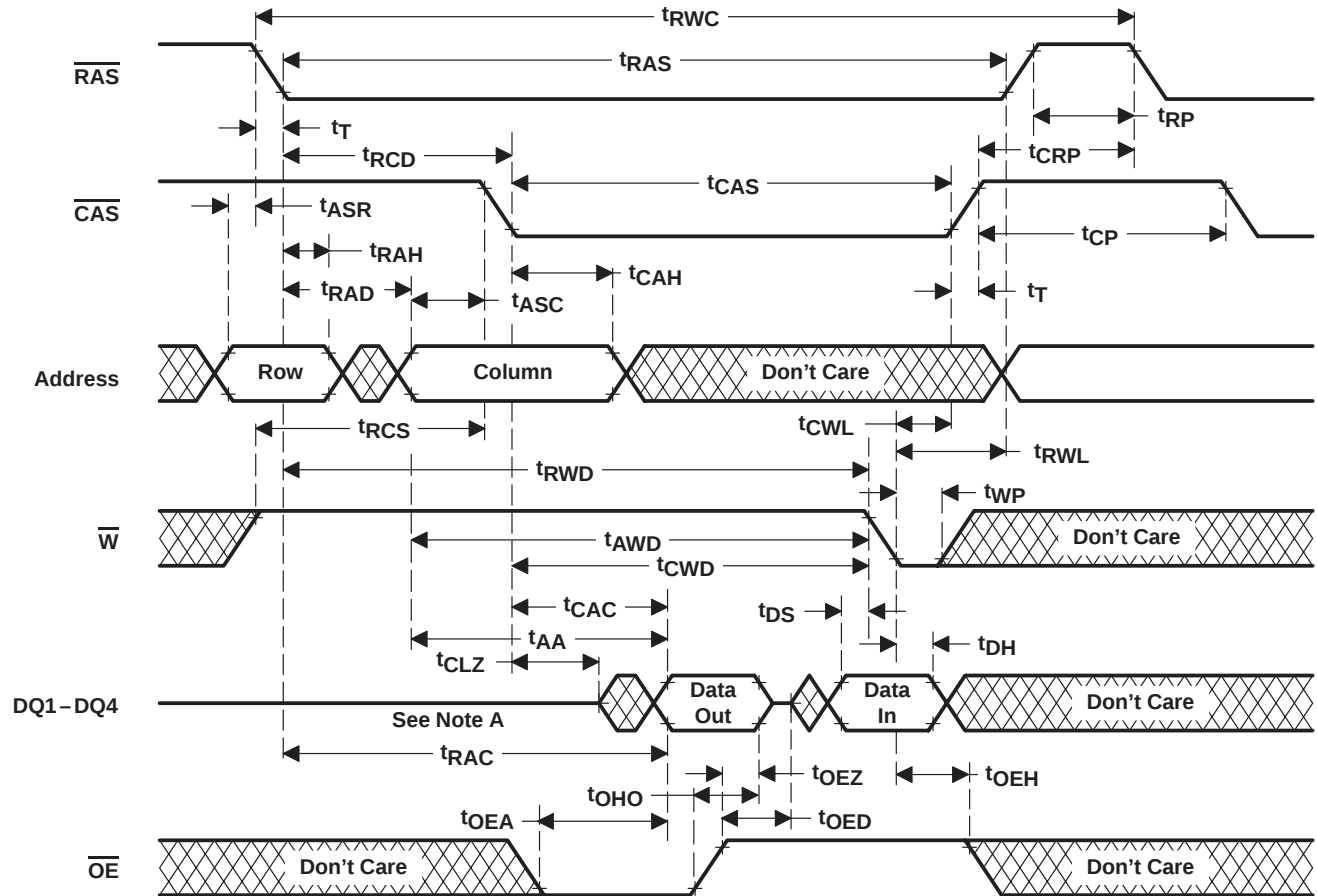


Figure 5. Write-Cycle Timing

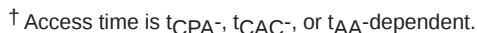
# PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

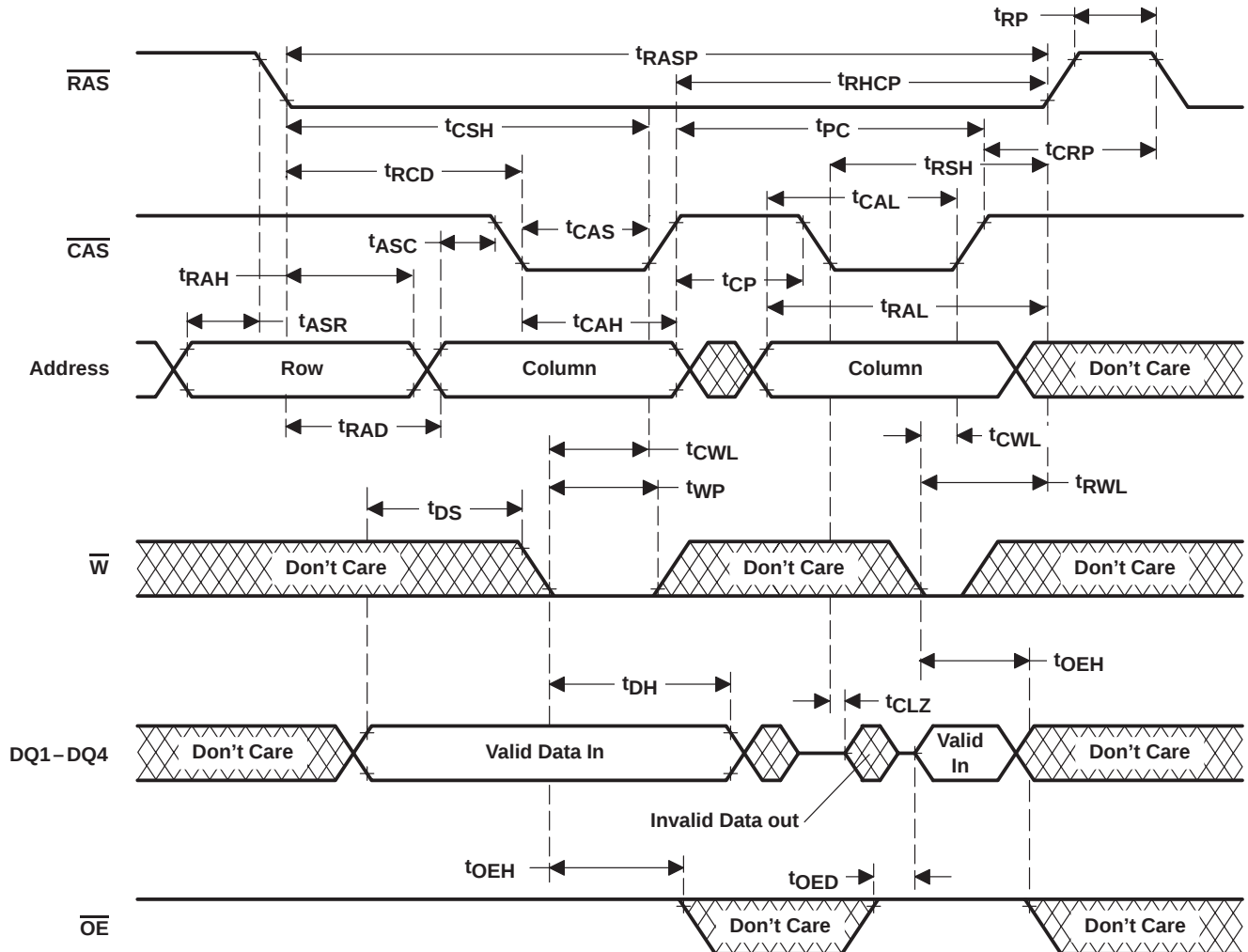
## PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

### Figure 7. Enhanced-Page-Mode Read-Cycle Timing

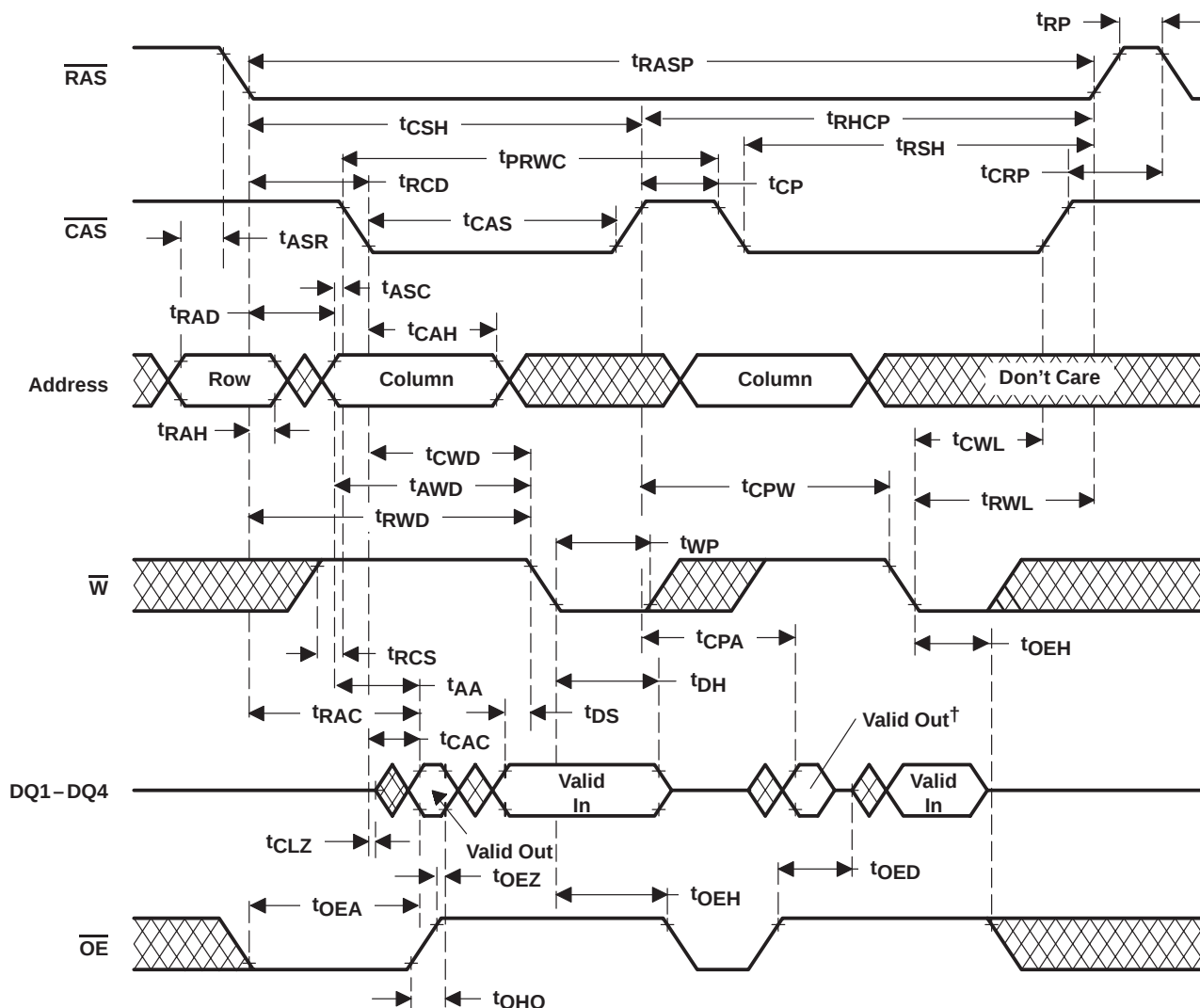
## PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

NOTE A: A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION

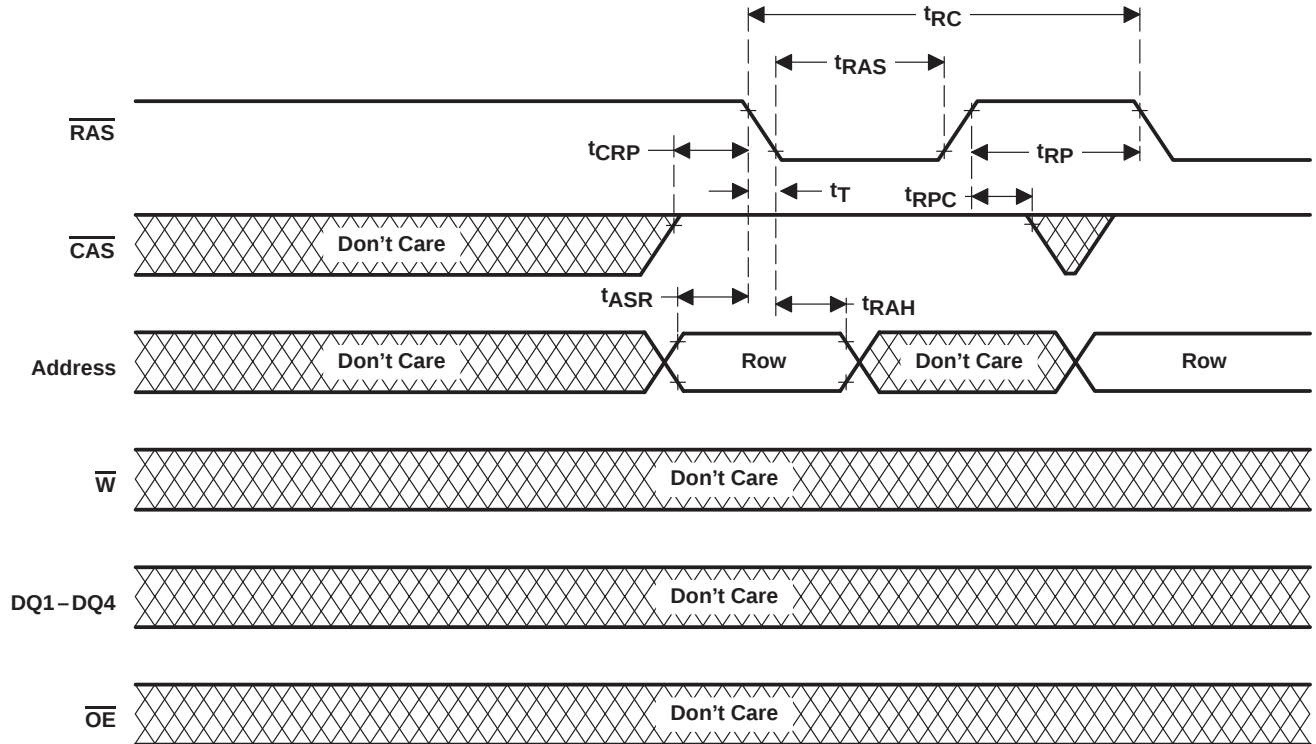


Figure 10.  $\overline{\text{RAS}}$ -Only Refresh Timing

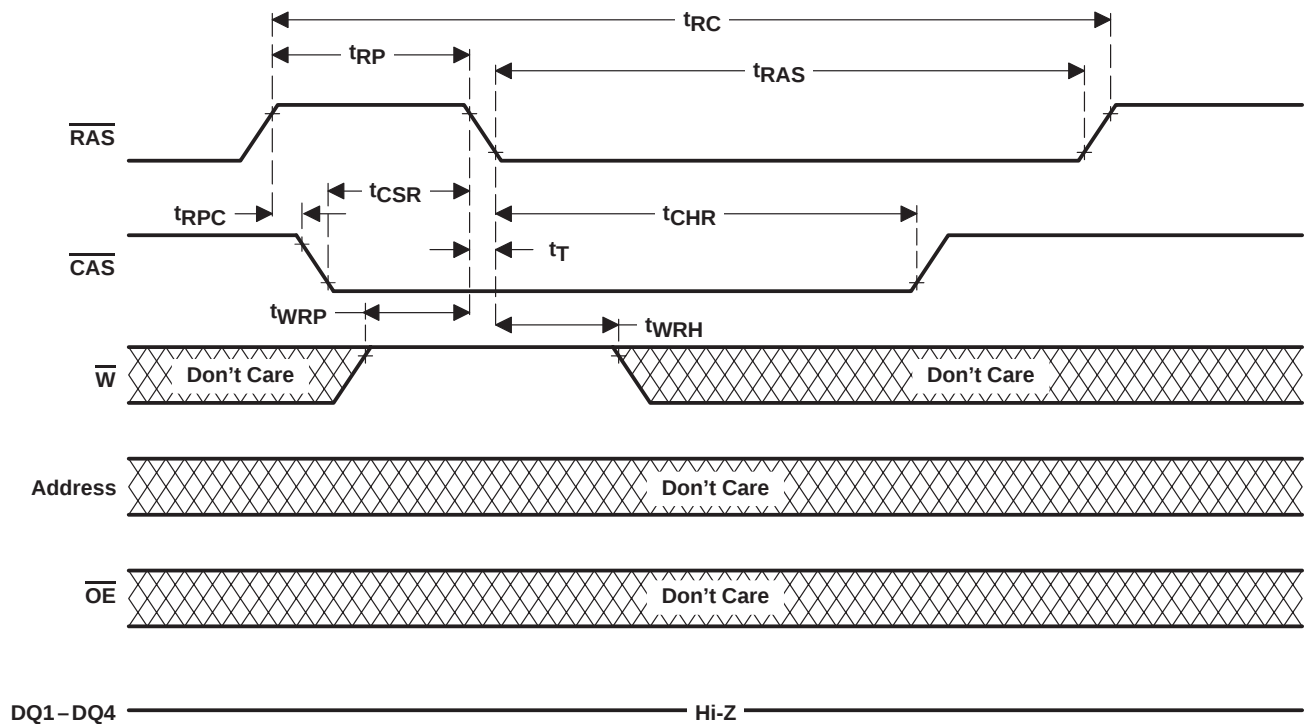


Figure 11. Automatic-CBR-Refresh-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

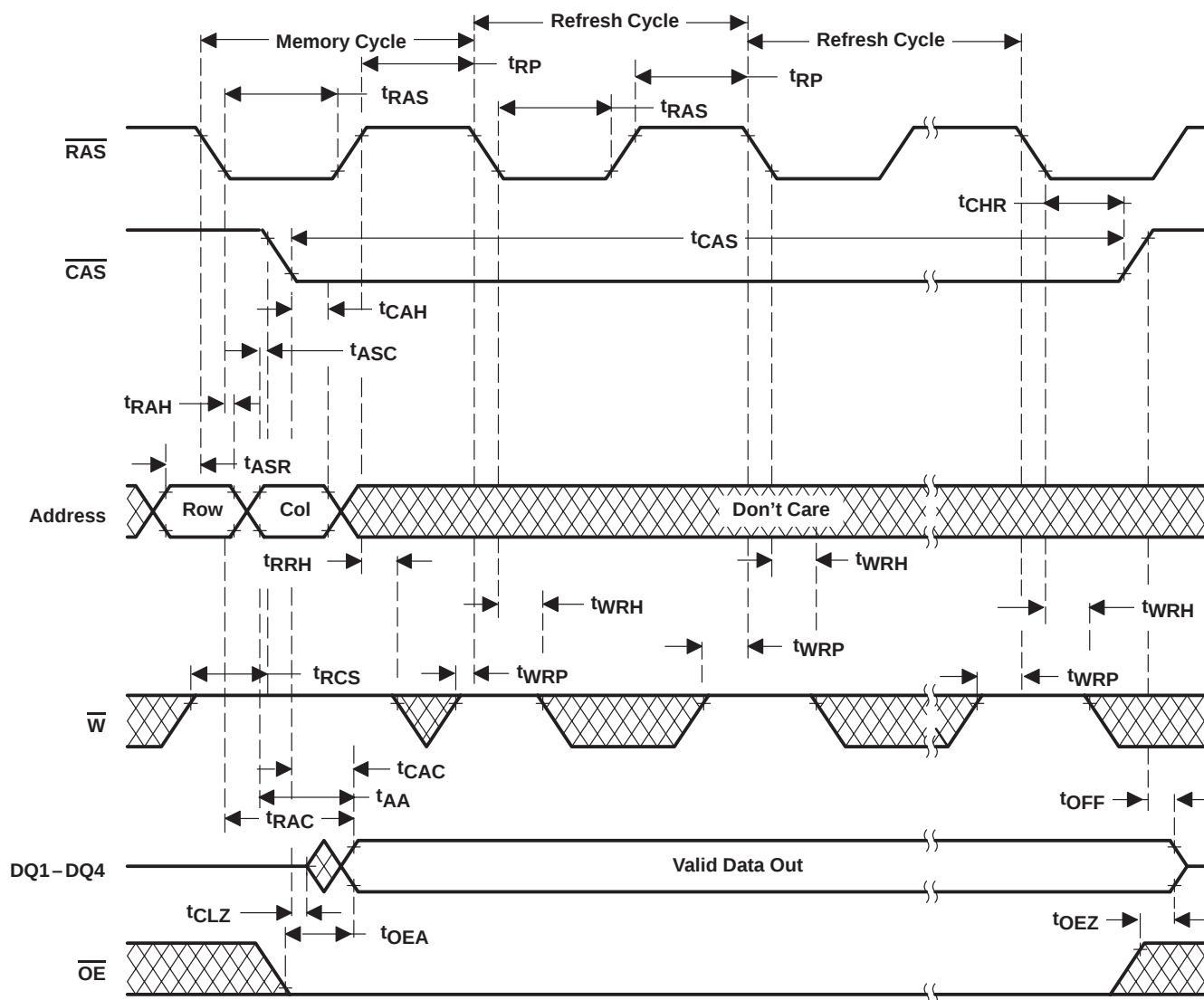


Figure 12. Hidden-Refresh-Cycle (Read) Timing

# PARAMETER MEASUREMENT INFORMATION

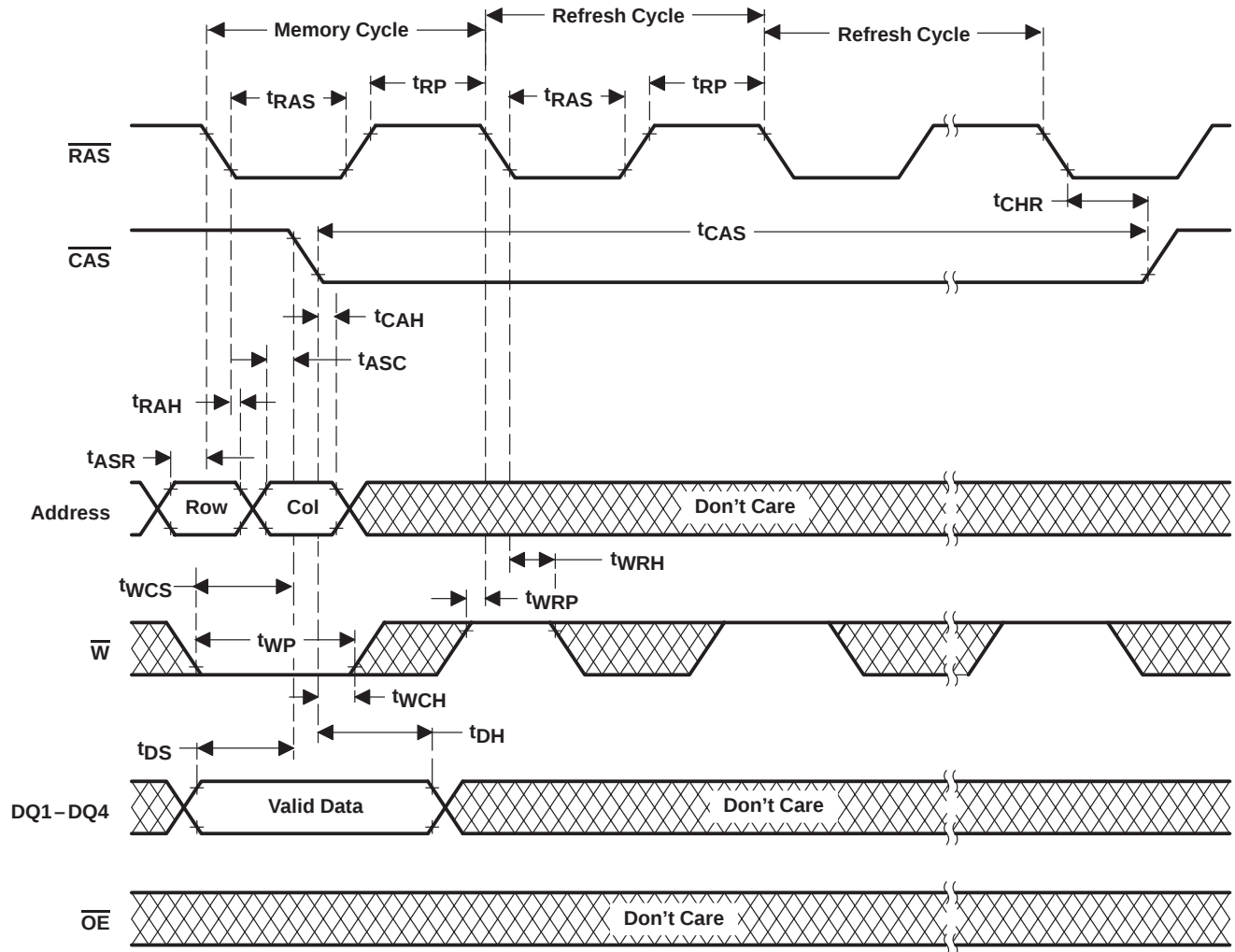


Figure 13. Hidden-Refresh-Cycle (Write) Timing

# PARAMETER MEASUREMENT INFORMATION

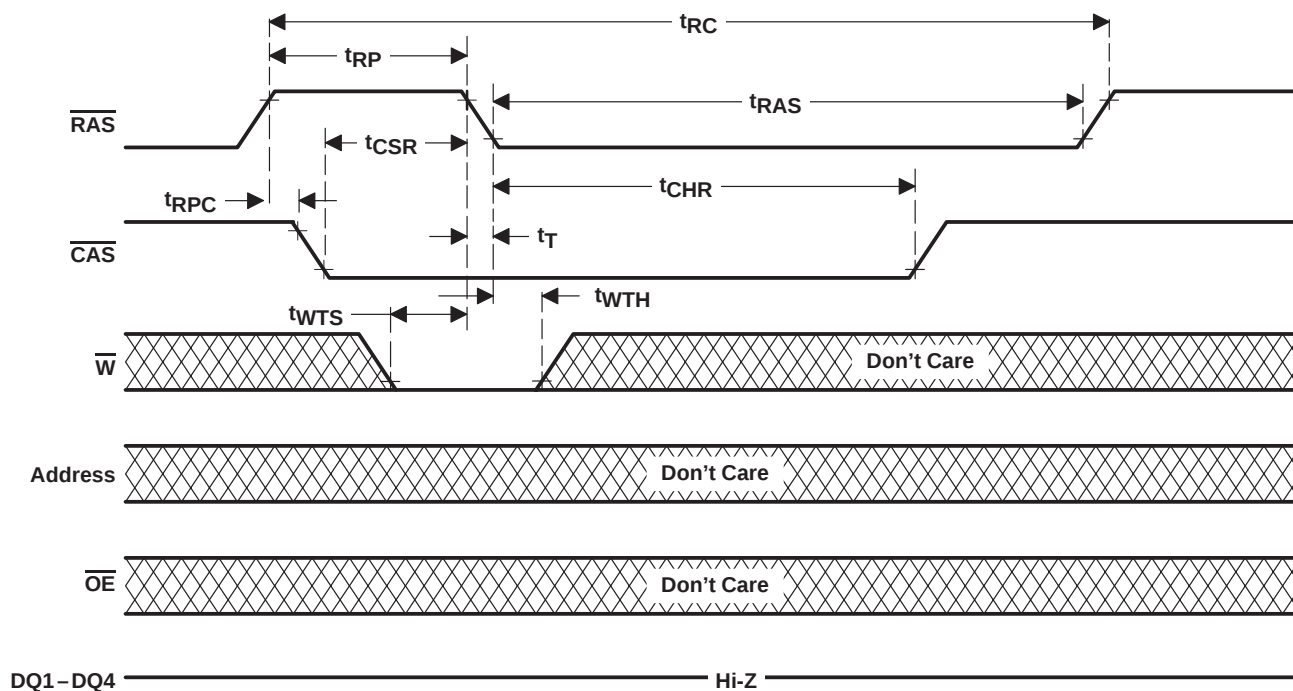


Figure 14. Test-Mode-Entry-Cycle Timing

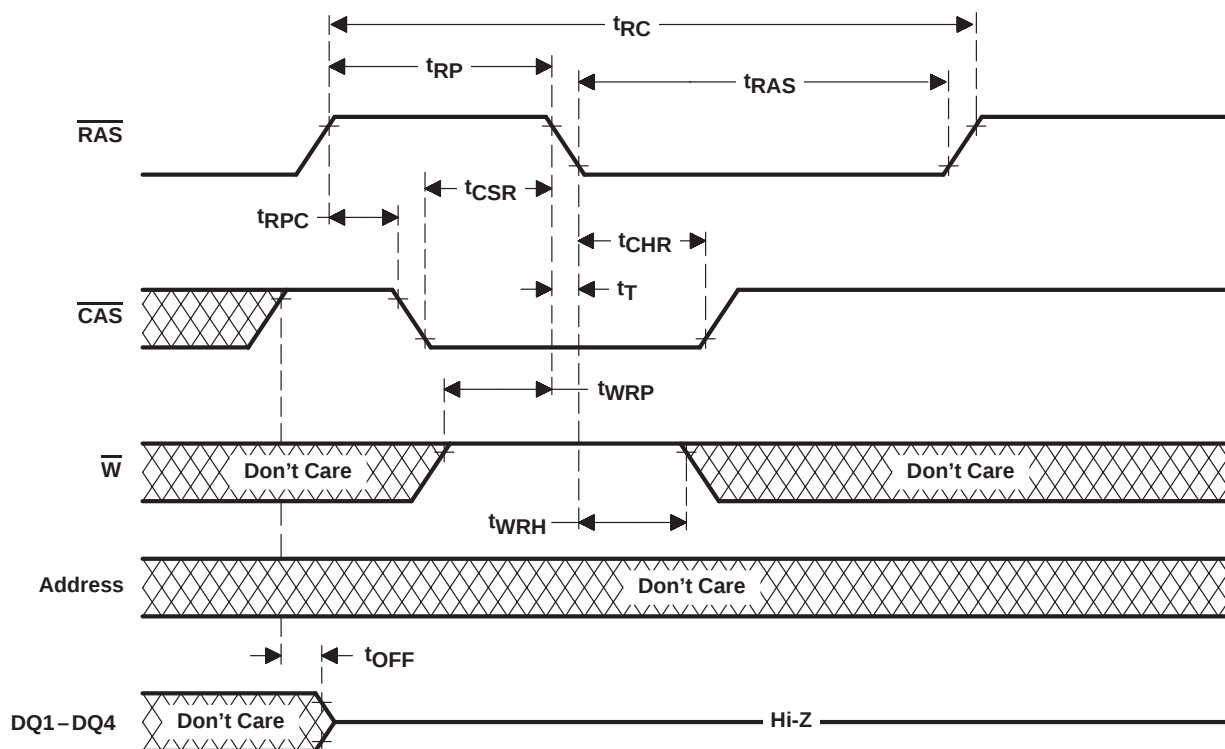
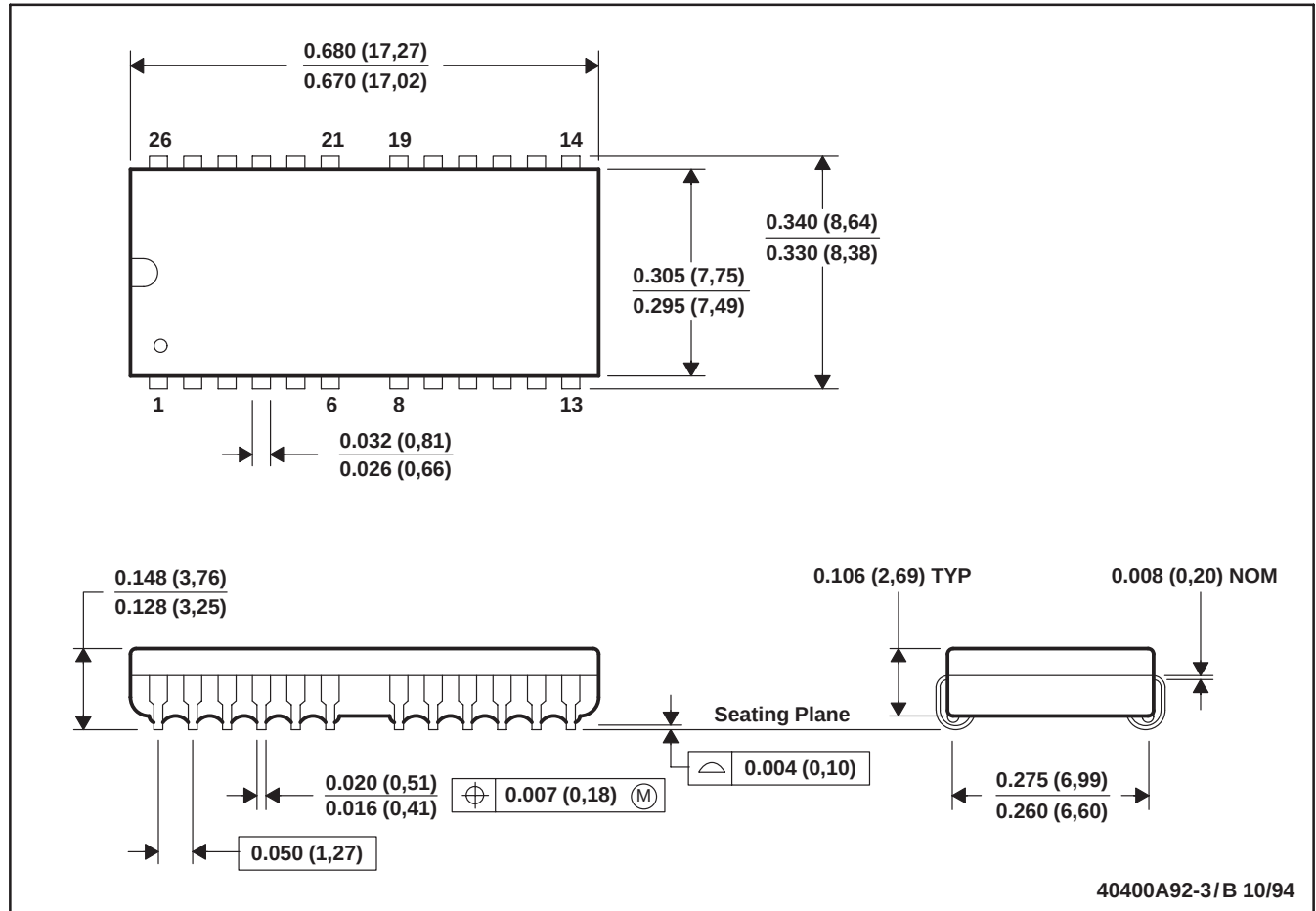


Figure 15. Test-Mode-Exit-Cycle CBR-Refresh-Cycle Timing

## MECHANICAL DATA

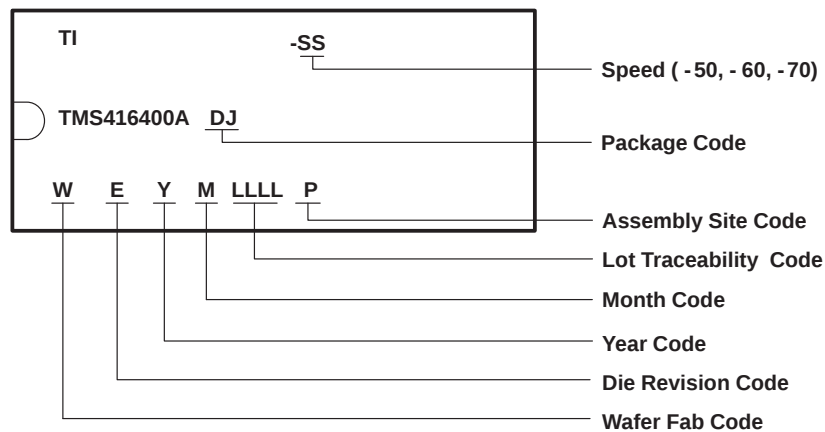
DJ (R-PDSO-J24/26)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

## device symbolization (TMS416400A illustrated)





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