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PEMB15; **PUMB15**

PNP/PNP resistor-equipped transistors; R1 = 4.7 k Ω , R2 = 4.7 k Ω

Rev. 5 — 16 December 2011

Product data sheet

1. Product profile

1.1 General description

PNP/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		-	NPN/NPN	Package
	NXP	JEITA	complement	complement	configuration
PEMB15	SOT666	-	PEMD15	PEMH15	ultra small and flat lead
PUMB15	SOT363	SC-88	PUMD15	PUMH15	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transist	or					
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V
Io	output current		-	-	-100	mA
R1	bias resistor 1 (input)		3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		8.0	1	1.2	



2. Pinning information

Table 3. Pinning

1 GND (emitter) TR1 2 input (base) TR1 3 output (collector) TR2 4 GND (emitter) TR2 5 input (base) TR2 6 output (collector) TR1	Pin	Description	Simplified outline	Graphic symbol
2 input (base) TR1 3 output (collector) TR2 4 GND (emitter) TR2 5 input (base) TR2	1	GND (emitter) TR1		
4 GND (emitter) TR2 5 input (base) TR2	2	input (base) TR1	6 5 4	6 5 4
5 input (base) TR2	3	output (collector) TR2		
1 2 3 /	4	GND (emitter) TR2		
	5	input (base) TR2		TR1
	6	output (collector) TR1		R2 R1
				1 2 3 006aaa212

3. Ordering information

Table 4. Ordering information

Type number	Package	Package			
	Name	Description	Version		
PEMB15	-	plastic surface-mounted package; 6 leads	SOT666		
PUMB15	SC-88	plastic surface-mounted package; 6 leads	SOT363		

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PEMB15	5D
PUMB15	B*6

[1] * = placeholder for manufacturing site code

PNP/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 4.7 kΩ

5. Limiting values

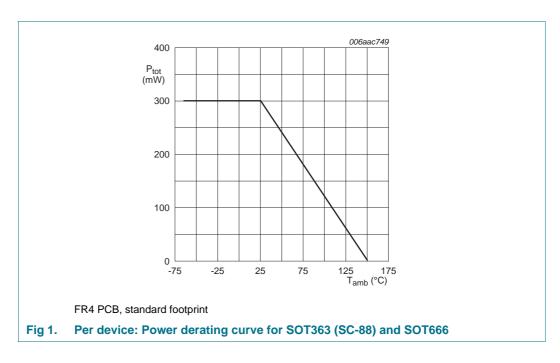
Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transis	stor				
V_{CBO}	collector-base voltage	open emitter	-	-50	V
V_{CEO}	collector-emitter voltage	open base	-	-50	V
V_{EBO}	emitter-base voltage	open collector	-	-10	V
V_{I}	input voltage				
	positive		-	+10	V
	negative		-	-30	V
Io	output current		-	-100	mA
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	-100	mA
P _{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$			
	PEMB15 (SOT666)		[1][2]	200	mW
	PUMB15 (SOT363)		<u>[1]</u> _	200	mW
Per device)				
P _{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$			
	PEMB15 (SOT666)		[1][2] -	300	mW
	PUMB15 (SOT363)		<u>[1]</u> -	300	mW
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

^[2] Reflow soldering is the only recommended soldering method.



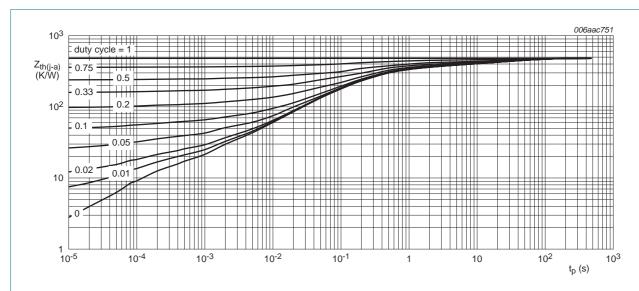
6. Thermal characteristics

Table 7. Thermal characteristics

Parameter	Conditions	onditions Min		Max	Unit
tor					
thermal resistance from junction to ambient	in free air				
PEMB15 (SOT666)		[1][2]	-	625	K/W
PUMB15 (SOT363)		<u>[1]</u> _	-	625	K/W
thermal resistance from junction to ambient	in free air				
PEMB15 (SOT666)		[1][2] _	-	417	K/W
PUMB15 (SOT363)		<u>[1]</u> -	-	417	K/W
	thermal resistance from junction to ambient PEMB15 (SOT666) PUMB15 (SOT363) thermal resistance from junction to ambient PEMB15 (SOT666)	thermal resistance from in free air junction to ambient PEMB15 (SOT666) PUMB15 (SOT363) thermal resistance from in free air junction to ambient PEMB15 (SOT666)	thermal resistance from in free air junction to ambient PEMB15 (SOT666) PUMB15 (SOT363) Ill - thermal resistance from in free air junction to ambient PEMB15 (SOT666) In free air junction to ambient PEMB15 (SOT666)	thermal resistance from in free air junction to ambient PEMB15 (SOT666) PUMB15 (SOT363) Ill thermal resistance from in free air junction to ambient PEMB15 (SOT666) Ill	thermal resistance from junction to ambient PEMB15 (SOT666) PUMB15 (SOT363) Ill 625 thermal resistance from junction to ambient PEMB15 (SOT666) Ill 417

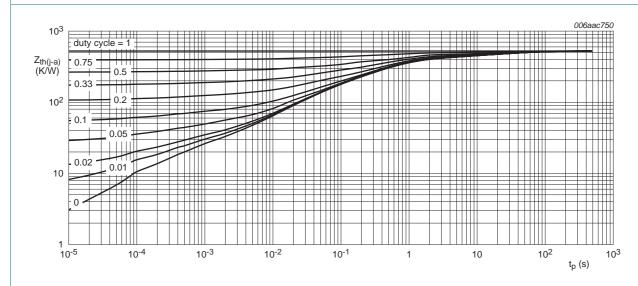
^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMB15 (SOT666); typical values



FR4 PCB, standard footprint

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PUMB15 (SOT363); typical values

PNP/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 4.7 kΩ

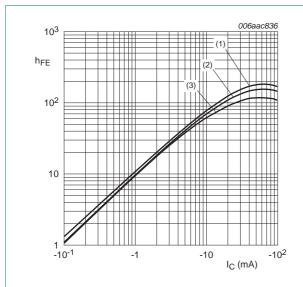
7. Characteristics

Table 8. Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

ramb — 20	o unicos otrici vioc spec	inica.				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per trans	istor					
I _{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$	-	-	-100	nA
I _{CEO}	collector-emitter cut-off	$V_{CE} = -30 \text{ V}; I_{B} = 0 \text{ A}$	-	-	-1	μΑ
	current	$V_{CE} = -30 \text{ V}; I_{B} = 0 \text{ A};$ $T_{j} = 150 ^{\circ}\text{C}$	-	-	-5	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$	-	-	-900	μΑ
h _{FE}	DC current gain	$V_{CE} = -5 \text{ V}; I_{C} = -10 \text{ mA}$	30	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$	-	-	-150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}; I_{C} = -100 \mu\text{A}$	-	-1.1	-0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V};$ $I_{C} = -20 \text{ mA}$	-2.5	-1.9	-	V
R1	bias resistor 1 (input)		3.3	4.7	6.1	$k\Omega$
R2/R1	bias resistor ratio		8.0	1	1.2	
C _c	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	-	-	3	pF
f _T	transition frequency	$V_{CE} = -5 \text{ V; } I_{C} = -10 \text{ mA;}$ [1] $f = 100 \text{ MHz}$	-	180	-	MHz

^[1] Characteristics of built-in transistor



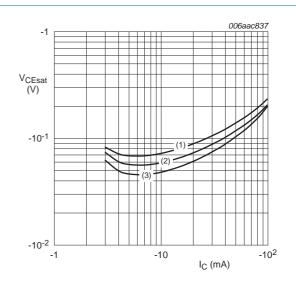
$$V_{CE} = -5 \text{ V}$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -40 \, ^{\circ}C$$

Fig 4. DC current gain as a function of collector current; typical values



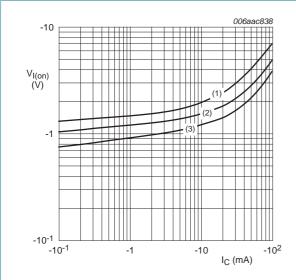
$$I_{\rm C}/I_{\rm B} = 20$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -40 \, ^{\circ}C$$

Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values



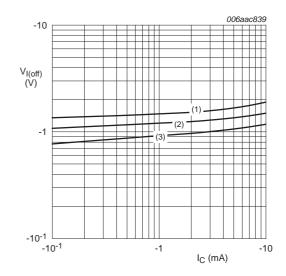
$$V_{CE} = -0.3 \text{ V}$$

(1)
$$T_{amb} = -40 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = 100 \, ^{\circ}C$$

Fig 6. On-state input voltage as a function of collector current; typical values



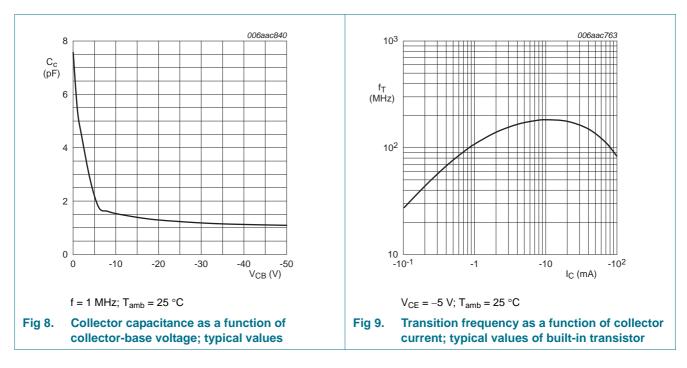
$$V_{CE} = -5 \text{ V}$$

(1)
$$T_{amb} = -40 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = 100 \, ^{\circ}C$$

Fig 7. Off-state input voltage as a function of collector current; typical values

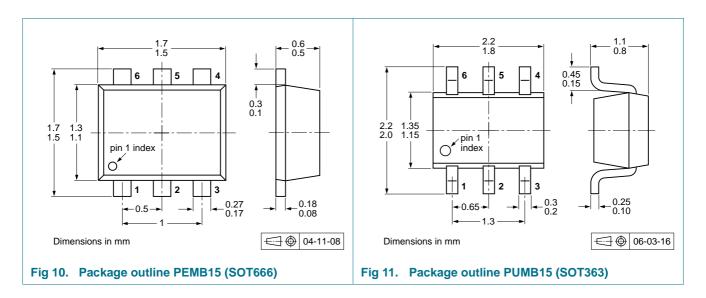


8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



PEMB15_PUMB15

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10. Packing information

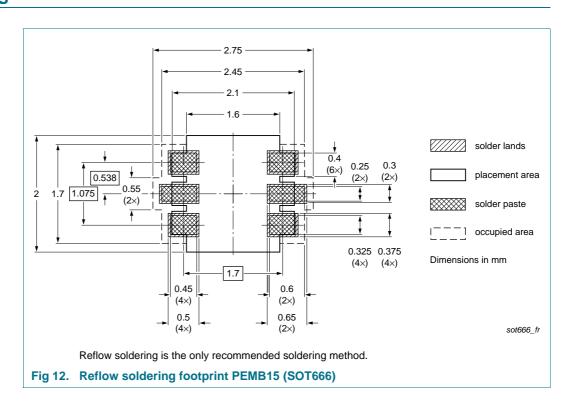
Table 9. Packing methods

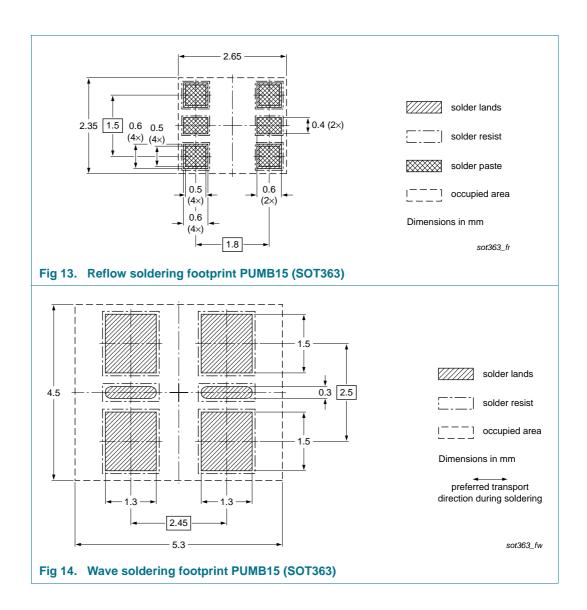
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

		3						
Type F number	Package	Description		Packing quantity				
				4000	8000	10000		
PEMB15 SOT666	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-		
		4 mm pitch, 8 mm tape and reel	-	-115	-	-		
PUMB15	SOT363	4 mm pitch, 8 mm tape and reel; T1	-115	-	-	-135		
		4 mm pitch, 8 mm tape and reel; T2	-125	-	-	-165		

- [1] For further information and the availability of packing methods, see Section 14.
- [2] T1: normal taping
- [3] T2: reverse taping

11. Soldering





PNP/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 4.7 kΩ

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMB15_PUMB15 v.5	20111216	Product data sheet	-	PEMB15_PUMB15 v.4
Modifications:	 Section 4 "I Figure 1 to Section 6 " Figure 4 to Table 8 "Ch Section 8 " Section 9 "I Section 11 " 	Thermal characteristics": up	f _T added ed by minimized packag	e outline drawings
PEMB15_PUMB15 v.4	20090831	Product data sheet	-	PEMB15_PUMB15 v.3
PEMB15_PUMB15 v.3	20050203	Product data sheet	-	PUMB15 v.2
PUMB15 v.2	20040414	Product specification	-	PUMB15 v.1
PUMB15 v.1	20031107	Product specification	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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PEMB15_PUMB15

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PEMB15; PUMB15

PNP/PNP resistor-equipped transistors; R1 = 4.7 k Ω , R2 = 4.7 k Ω

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15. Contents

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