

DEMO MANUAL DC1843B

DC1842B and DC1680B LTC4290B/LTC4271 8-Port PSE with Digital Isolation

DESCRIPTION

Demonstration kit DC1843B is an 8-port Ethernet Alliance™ certified IEEE 802.3at Type 2 power sourcing equipment (PSE) composed of a DC1842B daughter card and DC1680B motherboard. The kit is used for evaluation of the [LTC4290B](#) and [LTC4271](#) PSE chipset. Up to 8 powered devices (PDs) can be connected and powered from this system using a single power supply. A DC590 is connected to the DC1843 for I²C interfacing with QuikEval™. This demonstration manual provides a Quick Start Procedure, a DC1842B overview, a DC1680B overview, schematics, and layout

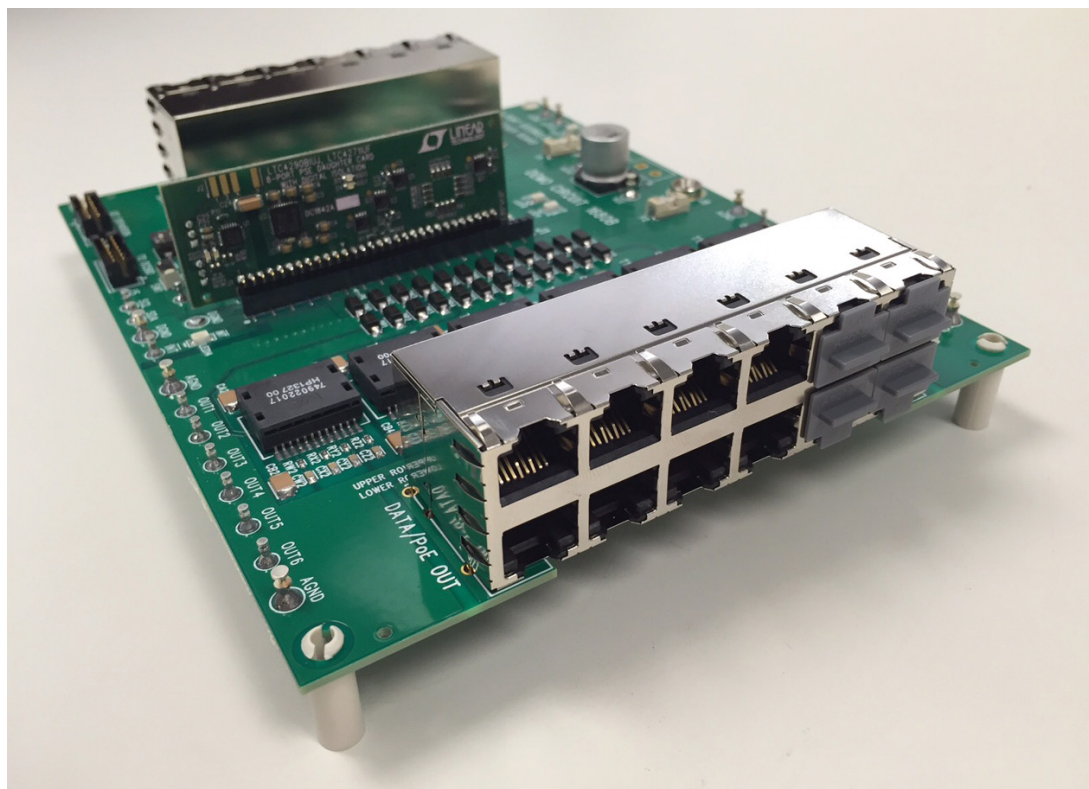
printouts. Refer to the Layout Guide for Demonstration Circuit 1842B when laying out the LTC4290B/LTC4271 circuit. Contact Analog Devices for this document.

The DC1842B has increased surge protection over the DC1842A. The DC1680B uses discrete Ethernet transformers while the DC1680A has an integrated 12-port RJ45 jack.

[Design files for this circuit board are available.](#)

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BOARD PHOTO



QUICK START PROCEDURE

Demonstration kit DC1843B includes the DC1842B daughter card and DC1680B motherboard. The kit is set up for evaluating the LTC4290B/LTC4271. Follow the procedure below and refer to Figures 1 through 4 for proper equipment setup.

NOTE (DC1843B Kit): Connector J1 on the DC1680B has four pegs blocking the unused last four pins to match the 30-pin connector of the DC1842B. Dust caps block the four unused ports at each RJ45 connector on the DC1680B for the 8-Port.

1. On the DC1842B set AUTO jumper JP1 to HI (Figure 1) to enable AUTO pin mode.
2. On the DC1842B set MID jumper JP2 to LO (Figure 1) to disable midspan mode.
3. Align pin 1 of the 30-pin male connector on the DC1842B with pin 1 of the 30-pin female connector on the DC1680B (Figure 2). Pin 12 is polarized to assist with the alignment. Carefully push the DC1842B straight down until the two 30-pin connectors are flush with each other.
4. On the DC1680B, connect a supply with the positive rail to POS and negative rail to NEG (Figure 3). Use a power supply capable of sourcing the maximum load expected ($8 \text{ ports} \times 850\text{mA} \geq 6.8\text{A}$). Ramp the supply up to 51V to 57V.
5. Connect up to 8 PDs to ports 1-8 at the DC1680B, J4 (Figure 3).
6. The DC590 is optionally connected to the DC1680B connector J5 with a 14-pin ribbon cable (Figure 3). A GUI for the LTC4290B/LTC4271 is brought up by QuikEval for I²C interfacing from a PC (Figure 4).

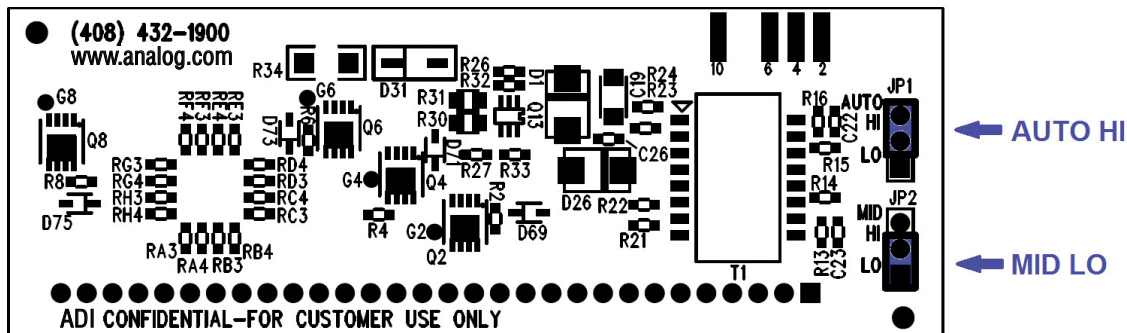


Figure 1. DC1842 Backside. Setting AUTO and MID Jumpers

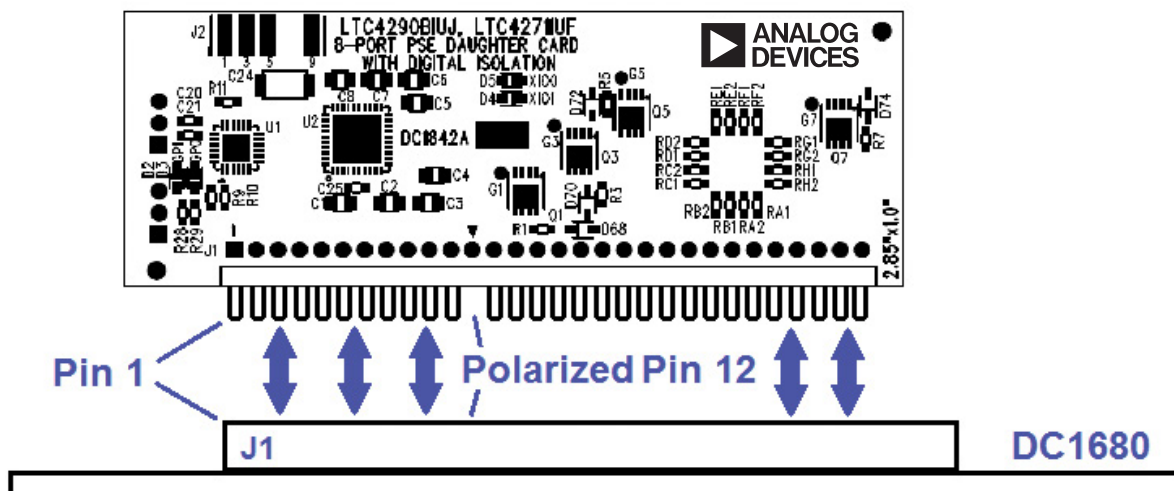


Figure 2. Inserting the DC1842 into J1 of the DC1680

QUICK START PROCEDURE

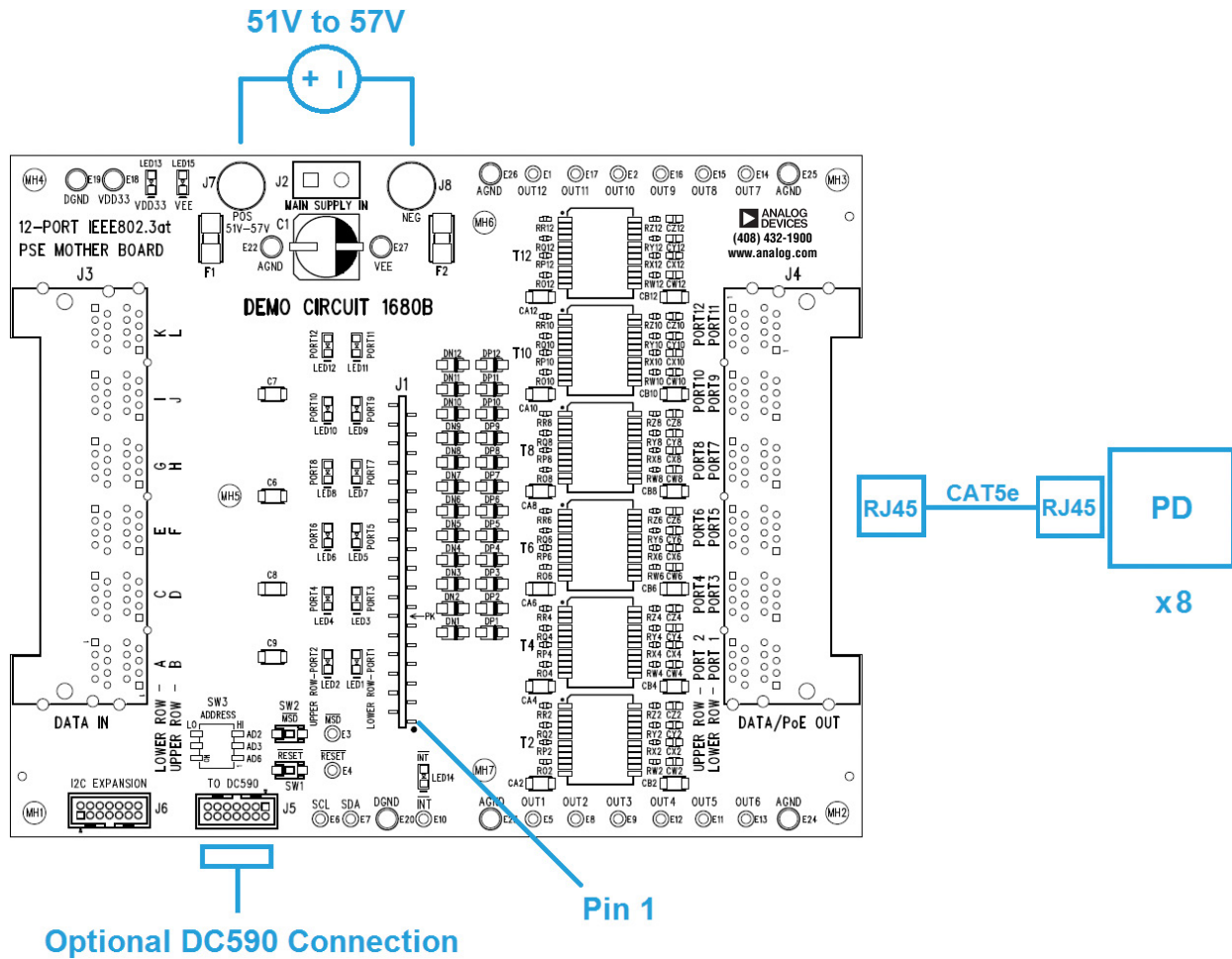


Figure 3. DC1843B Basic Setup

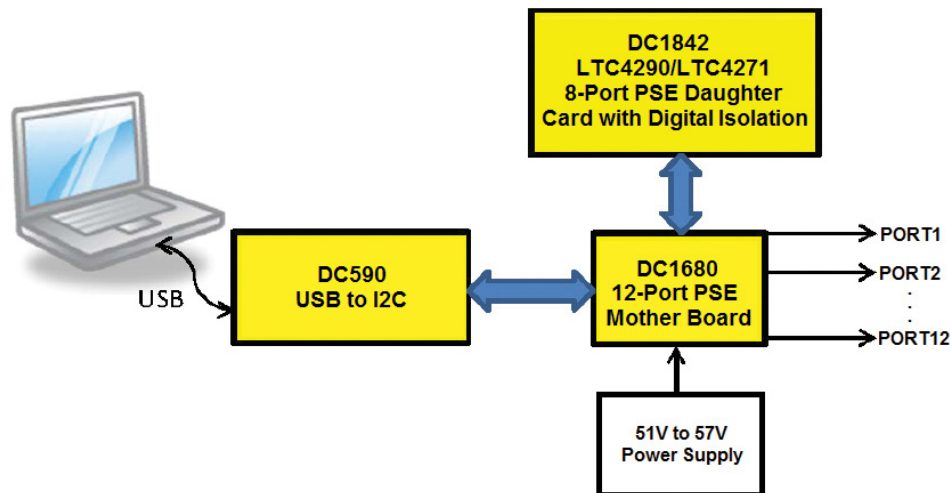


Figure 4. DC1843 System Setup with the DC590, DC1680, DC1842 and 51V to 57V Power Supply

DEMONSTRATION CIRCUIT 1842B OPERATION

8-Port PSE Daughter Card with Digital Isolation

Demonstration circuit 1842B (Figure 5) features the LTC4290B/LTC4271 chipset on a compact daughter card with digital isolation. The LTC4290B/LTC4271 chipset is an 8-port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 1 and Type 2 (high power) compliant Power over Ethernet (PoE) systems. A transformer isolated communication protocol replaces expensive opto-couplers and complex isolated 3.3V supply resulting in significant BOM cost savings. The LTC4290B/LTC4271 chipset delivers lowest-in-industry heat dissipation by utilizing low R_{ON} external MOSFETs and 0.25Ω sense resistors, eliminating the need for expensive heat sinks.

Advanced power management features in the LTC4290B/LTC4271 chipset include: per port 12-bit current monitoring ADCs, DAC programmable current limit, and versatile quick shutdown of preselected ports. PD discovery uses a

proprietary dual mode 4-point detection mechanism ensuring excellent immunity from false PD detection. Midspan PSEs are supported with 2-event classification and a two second backoff timer. The LTC4290B/LTC4271 includes an I²C serial interface operable up to 1MHz.

The DC1842B demonstrates proper LTC4290B/LTC4271 board layout that is approximately the height and width of a 2×4 RJ45 connector. The compact layout is made possible by the small package size of key components. The LTC4290B is in a $6\text{mm} \times 6\text{mm}$ QFN, while the LTC4271 is in a $4\text{mm} \times 4\text{mm}$ QFN. Each port has a PSMN075-100MSE MOSFET in a $3\text{mm} \times 3\text{mm}$ LFPAK33 package.

The daughter card inserts in the DC1680B motherboard through J1, a polarized 30-pin connector. Isolated 3.3V and logic control signals are brought in on this connector. Also connected at J1 is the PoE V_{EE} supply from the motherboard and 8 PSE controlled outputs.

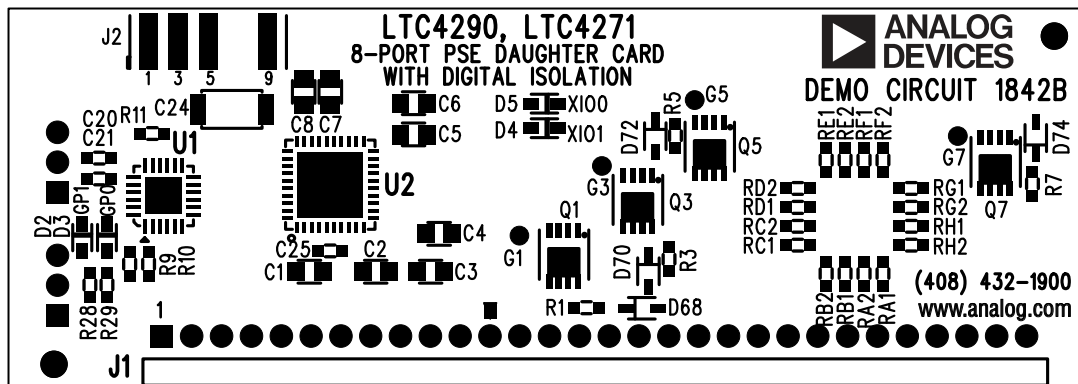


Figure 5. DC1842B 8-Port PSE Daughter Card with Digital Isolation Features the LTC4290B and LTC4271

DEMONSTRATION CIRCUIT 1842B OPERATION

Board Layout

Proper board layout is crucial for proper LTC4290B/LTC4271 chipset operation, robustness, and accuracy. When laying out, pay attention to parts placement, Kelvin sensing, power paths, and copper fill. It is imperative to follow the LTC4290B/LTC4271 Layout Guide document when laying out the board. Contact Analog Devices for this document.

Isolation and Power Supplies

The LTC4290B/LTC4271 chipset provides communication across an isolation barrier through a data transformer (Figure 6). This eliminates the need for expensive optocouplers. All digital pins reside on the digital ground reference and are isolated from the analog PoE supply. A 3.3V supply for V_{DD} and an isolated V_{EE} supply are connected to the DC1842B through the 30-pin connector.

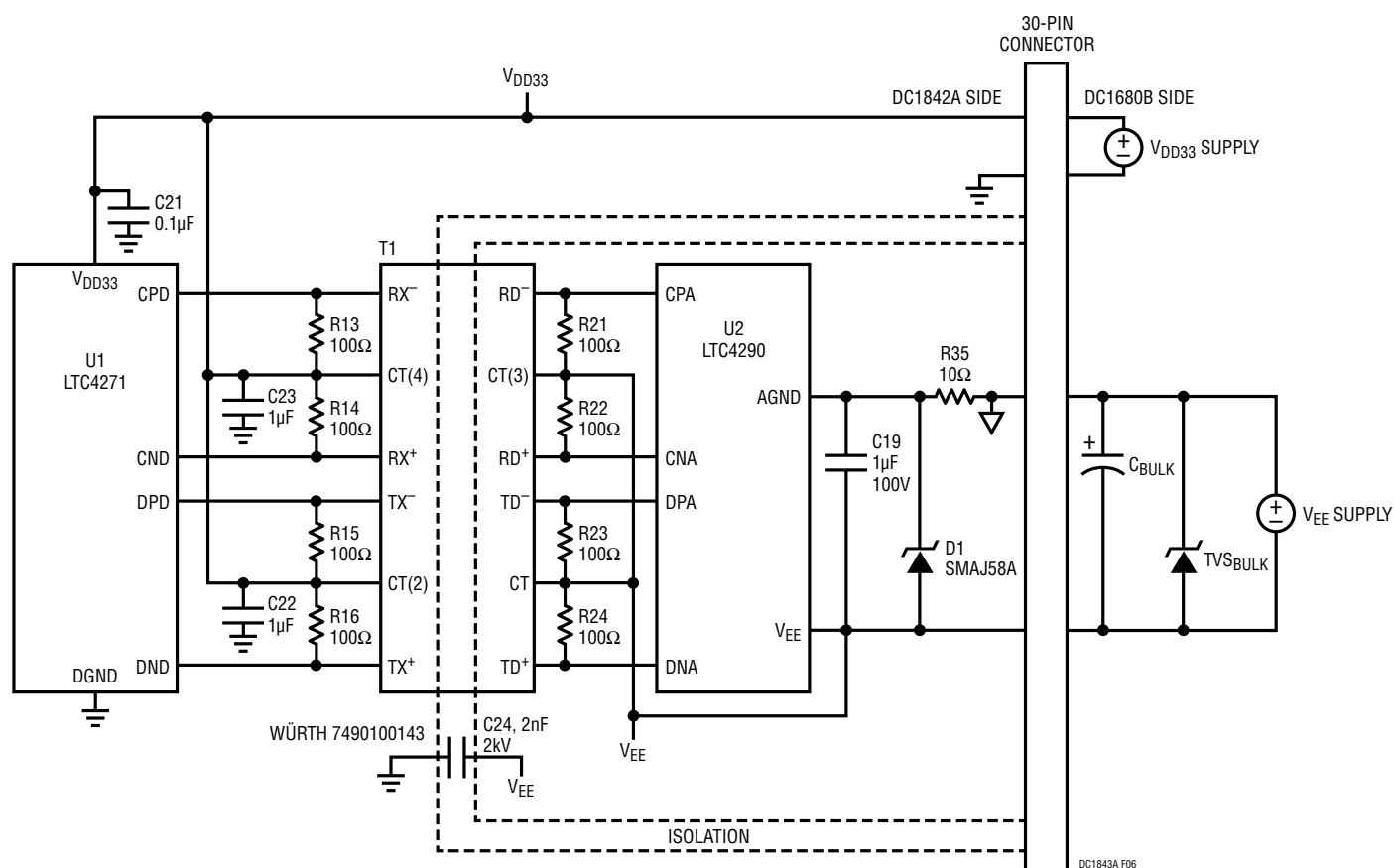


Figure 6. DC1842B Digital and Analog Isolation

DEMONSTRATION CIRCUIT 1842B OPERATION

I²C Communication and Addressing

The LTC4271 internal registers are accessed via I²C to read and/or write configuration, status, and interrupt registers. The I²C lines SDAOUT, SDAIN and SCL connect to the 30-pin connector (Figure 7). Subsequently, the I²C bus is accessed on the DC1680B.

The LTC4290B/LTC4271 chipset has an address of (A₆A₃A₂A₁A₀b), where A₆, A₃, A₂, A₁, and A₀ are the logic state of the AD₆, AD₃, AD₂, AD₁, and AD₀ pins respectively. On the DC1842B, AD₀ and AD₁ are tied low with pull-down resistors. AD₂, AD₃ and AD₆ are brought out to the 30-pin connector (Figure 7) and set with three switches on the DC1680B.

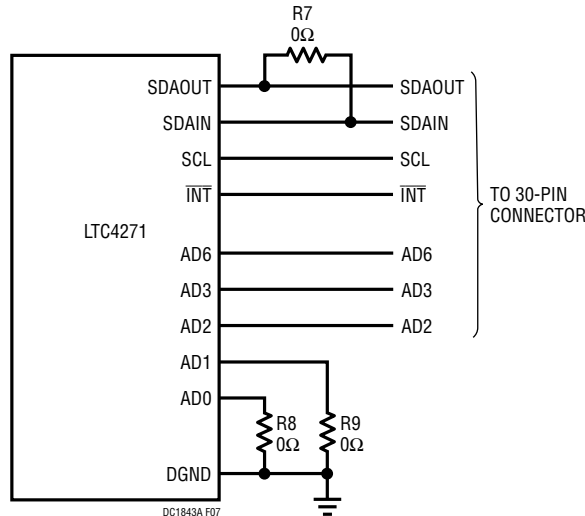


Figure 7. DC1842B, LTC4271 I²C and Address Connections

I/O LED Indicators

The DC1842B features four LEDs to indicate the states of the LTC4290B/LTC4271 chipset general purpose input output pins. These pins are configured as inputs or outputs via I²C. GP1 and GP0 are referenced to DGND and driven by the LTC4271 when set as outputs (Figure 8). XIO0 and XIO1 are referenced to V_{EE} and are driven by the LTC4290B when set as outputs (Figure 9). J2 provides test points for access to these I/Os.

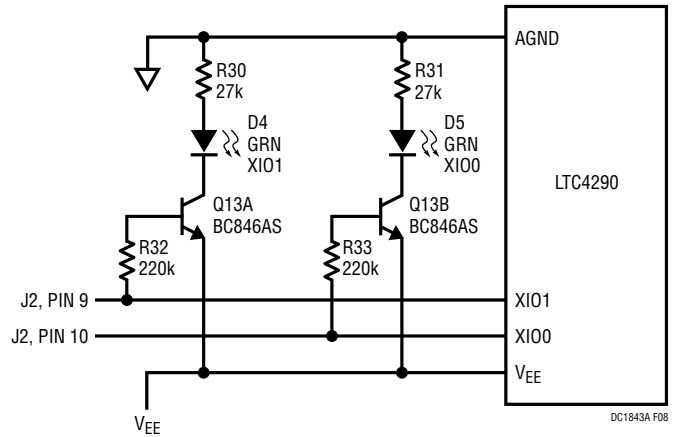


Figure 8. DC1842B, LTC4290B General Purpose I/O LED Indicators

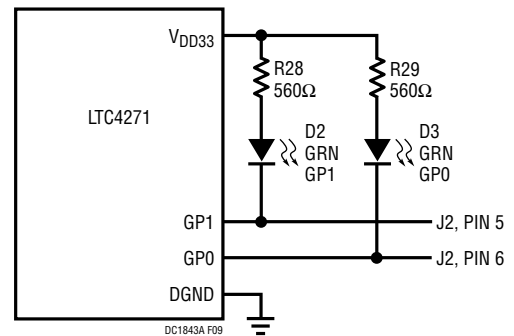


Figure 9. DC1842B, LTC4271 General Purpose I/O LED Indicators

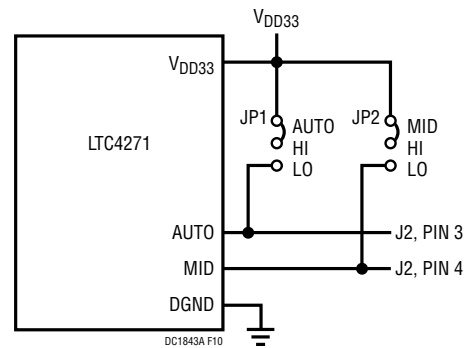


Figure 10. DC1842B AUTO and MID Jumpers

DEMONSTRATION CIRCUIT 1842B OPERATION

AUTO and MID Jumpers

The AUTO and MID pins of the LTC4271 are set by jumpers JP1 and JP2 respectively on the DC1842B (Figure 10). Setting JP1 to HI enables the AUTO pin mode in the LTC4290B/LTC4271 chipset. J2 provides test points for access to AUTO and MID.

In AUTO pin mode (JP1 high), the LTC4290B/LTC4271 chipset internal I²C registers default to the AUTO pin high state after a software or hardware reset, or system power on. The LTC4290B/LTC4271 chipset autonomously detects, powers on and disconnects power to PDs without the need for I²C host control.

Setting JP1 to LO disables AUTO pin mode and sets the LTC4290B/LTC4271 chipset to a low current shutdown mode. An I²C host controller can then be used to configure the LTC4290B/LTC4271 chipset to semi-auto mode for controlled PSE operation or to manual mode for test purposes.

Setting JP2 to HI enables the midspan mode detection backoff timer in the LTC4290B/LTC4271 chipset. For endpoint PSEs, set JP2 to LO to disable midspan mode.

For quick PSE evaluation in AUTO pin mode with MIDSPAN disabled, set JP1 HI and JP2 LO on the DC1842B.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 11, are required at the main supply, at the LTC4270 supply pins and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements.

Each LTC4290 requires a 10 Ω , 0805 resistor (R1) in series from supply AGND to the LTC4290 AGND pin. Across the LTC4290 AGND pin and V_{EE} pin are an SMAJ58A, 58V TVS (D1) and a 1 μ F, 100V bypass capacitor (C19). These components must be placed close to the LTC4290 pins.

Finally, each port requires a pair of S1B clamp diodes: one from OUT_n to supply AGND and one from OUT_n to supply V_{EE}. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance. These S1B diodes are placed on the DC1680 mother board of the DC1843 kit.

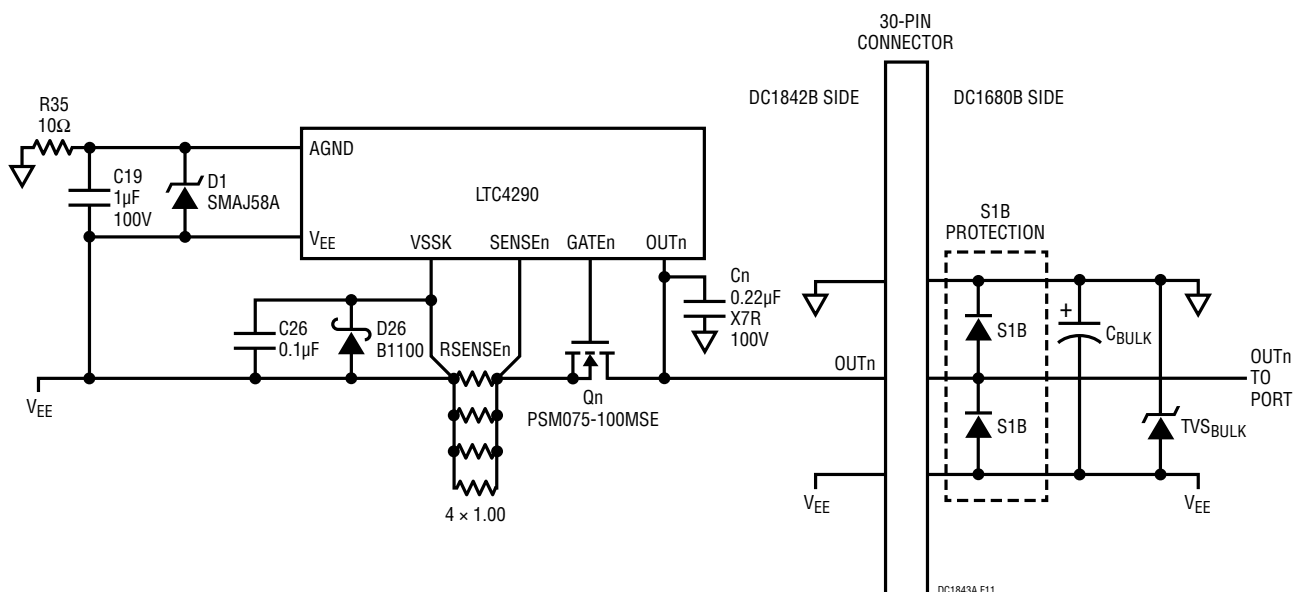


Figure 11. DC1842B, 1 of 8 Port Outputs. Surge Protection

DEMONSTRATION CIRCUIT 1680B OPERATION

Demonstration circuit 1680B is configured as an 8-Port, IEEE802.3at Type 1 and Type 2 PoE PSE motherboard in the DC1843B kit. This board accepts various PSE daughter cards featuring Analog Devices PSE controllers. The DC1680B is capable of powering up to 8 PDs.

Daughter Card Insertion Precautions

When inserting or removing the daughter card into the DC1680B, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment.

V_{EE} Supply

Connect a power supply for V_{EE} with the positive rail to POS and negative rail to NEG as shown in Figure 3 of the Quick Start Procedure. Set the voltage within the range in Table 1 depending on whether the application is a Type 1 or Type 2. Choose a power supply rating and set the current limit high enough to provide power for the maximum number of PDs connected and to meet each PD power requirements.

Table 1. DC1843B V_{EE} Power Range for Type 1 and Type 2 PSEs

PSE TYPE	V _{EE} SUPPLY RANGE	MAX DELIVERED PORT POWER	POWER SUPPLY*
Type 1	45V to 57V	13W	200W
Type 2	51V to 57V	25.5W	400W

*Recommended DC1843B power supply minimum to avoid drooping in a worst-case scenario with I_{LIM} current at all 8 ports.

PD Connection

PDs are connected using an Ethernet cable to any of the 8 ports at the 2×6, RJ45 connector J4 on the DC1680B (Figure 3). Test points for port outputs OUT1 through OUT8 are provided.

8-Port Configuration

The DC1680B is configured for an 8-port PSE motherboard for the DC1843B kit. Four RJ45 dust caps at J3 and four dust caps at J4 are inserted to block off the four unused

Ethernet ports. Additional pegs are placed in the last 4 pins of connector J1 to block off the unused pins when the DC1842B daughter card is inserted.

DC1680B USER FEATURES

Refer to Figure 12 and Figure 13 for the following user features.

Onboard 3.3V Supply

The DC1680B has an onboard V_{DD33} digital supply generated from the V_{EE} supply. DGND is a negative voltage referenced to AGND. If an external 3.3V supply is to be used, contact Analog Devices Applications for proper connection.

V_{EE} and V_{DD33} LED Indicators

LEDs for V_{EE} and V_{DD33} indicate if voltage is present at these supplies. Verify these LEDs are off before inserting or removing the daughter card.

Digital Connections

The DC1680B has connections for I²C control from a host controller. The DC590 is optionally connected to the DC1680B at J5 through a 14-pin ribbon cable. The QuikEval software will automatically detect the DC1680B and open the LTC4271 GUI. A second 14-pin ribbon cable can be connected to J6 for I²C expansion to another DC1680B board with slight board modifications. Contact Analog Devices Applications for instructions.

Digital test points include SCL, SDA, DGND, $\overline{\text{INT}}$, $\overline{\text{MSD}}$, and $\overline{\text{RESET}}$. I²C address pin AD6, AD3, and AD2 are set with a 3-bit switch SW3.

Midspan PSE

The DC1843B can be configured as a midspan PSE. Upstream switch data comes in to J3. Data and PoE go out to a PD at J4. Set both MID and AUTO pins logic high.

DEMONSTRATION CIRCUIT 1680B OPERATION

$\overline{\text{MSD}}$ and $\overline{\text{RESET}}$ Pushbuttons

Pushbutton switch SW1, when pressed, pulls the $\overline{\text{RESET}}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off and all internal registers reset to their power-up states. When SW1 is released, $\overline{\text{RESET}}$ is pulled high, and the PSE begins normal operation.

Pushbutton switch SW2 when pressed pulls the maskable shutdown input ($\overline{\text{MSD}}$) pin of the daughter card logic low. When pressed, all ports that have their corresponding mask bit set in the mconfig register of the PSE controller will be shutdown. These ports must then be manually re-enabled via I²C or by resetting the PSE.

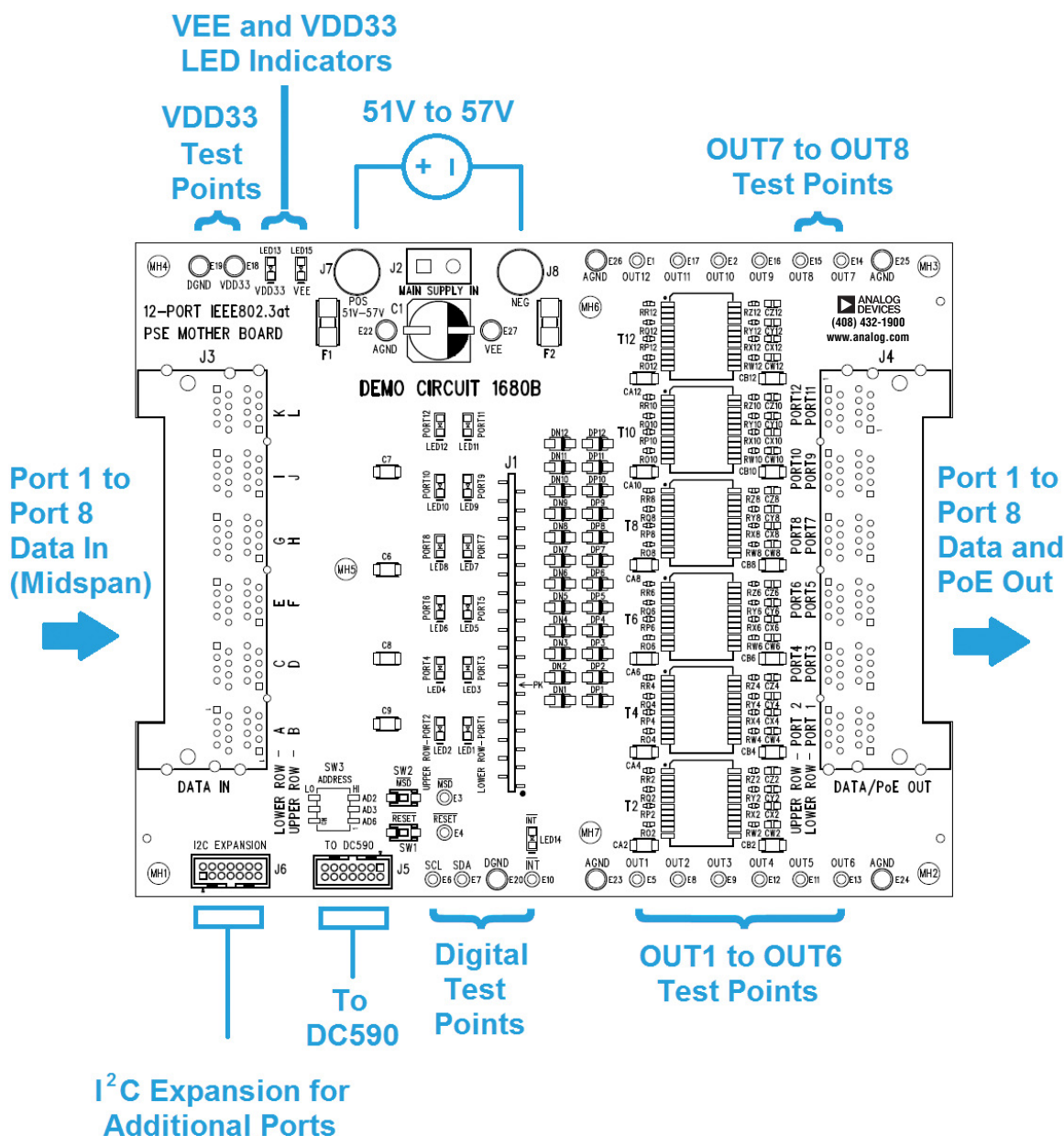


Figure 12. DC1680B Connections and Supply LEDs

DEMONSTRATION CIRCUIT 1680B OPERATION

Interrupt LED

A red LED indicates when the $\overline{\text{INT}}$ line is pulled logic low by the daughter card. When the interrupt is cleared (high) via I²C servicing, the LED is turned off.

Port 1 Through 8 Power LED Indicators

Each PSE port has a green LED indicator to show when PoE power is present at the port. The LEDs are driven by the respective port OUT voltage.

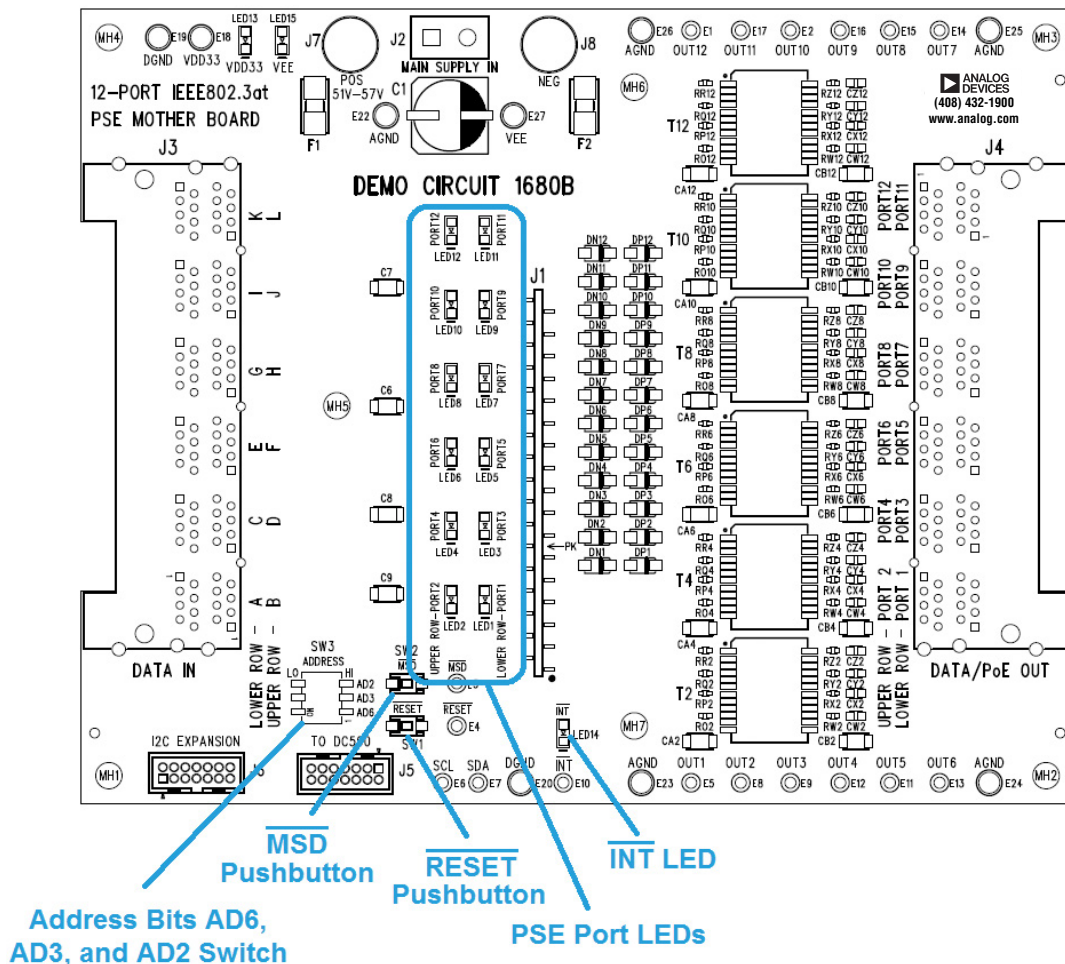


Figure 13. DC1680B Address Switch, Pushbutton Switches, INT LED, and Port Power LEDs

DEMONSTRATION CIRCUIT 1843B SYSTEM

DC1843B System Setup

Figure 14 shows a basic DC1843B system setup. The DC1842B daughter card is inserted in the 30-pin connector J1 on the DC1680B motherboard. A power supply is connected to V_{EE} with banana cables. The DC590 connects

with a 14-pin ribbon cable to the DC1680B and to a PC via USB. On the PC, a GUI communicates with the board. At the PSE output, PDs are connected. A sample PD demo board is shown in Figure 14.

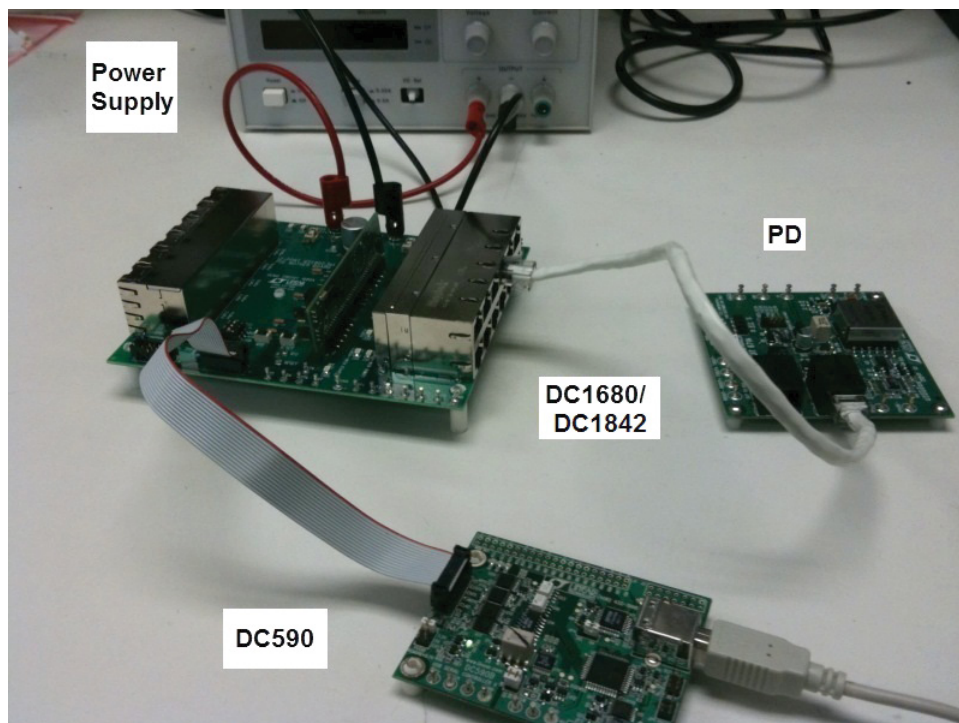


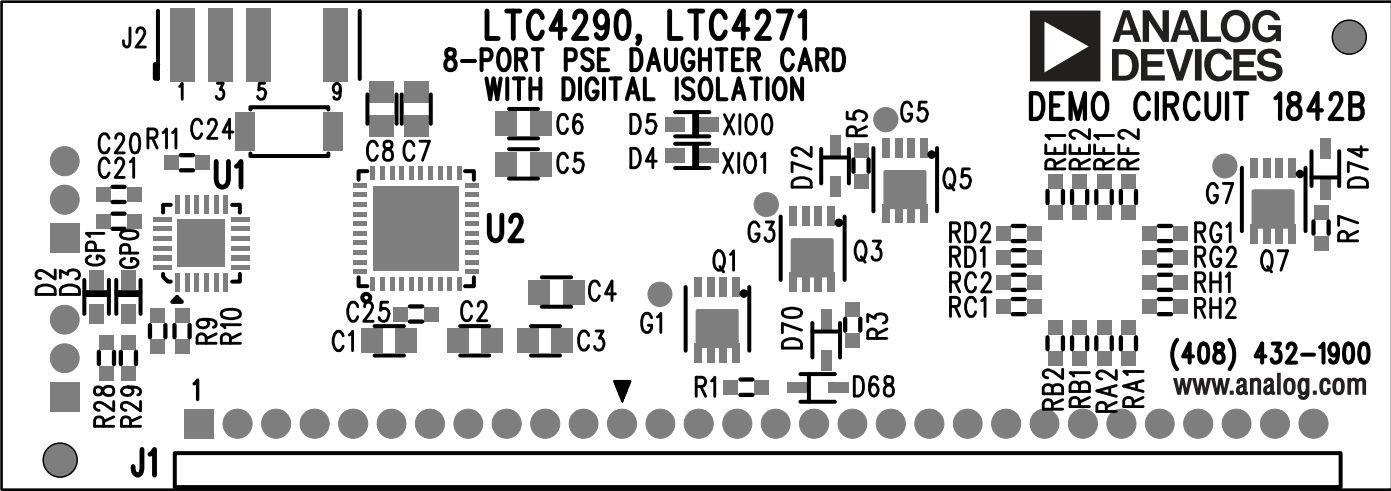
Figure 14. DC1680B and DC1842B System Setup with Power Supply, DC590 and PD Demo Board

Table 2. DC1843 Kit Versions

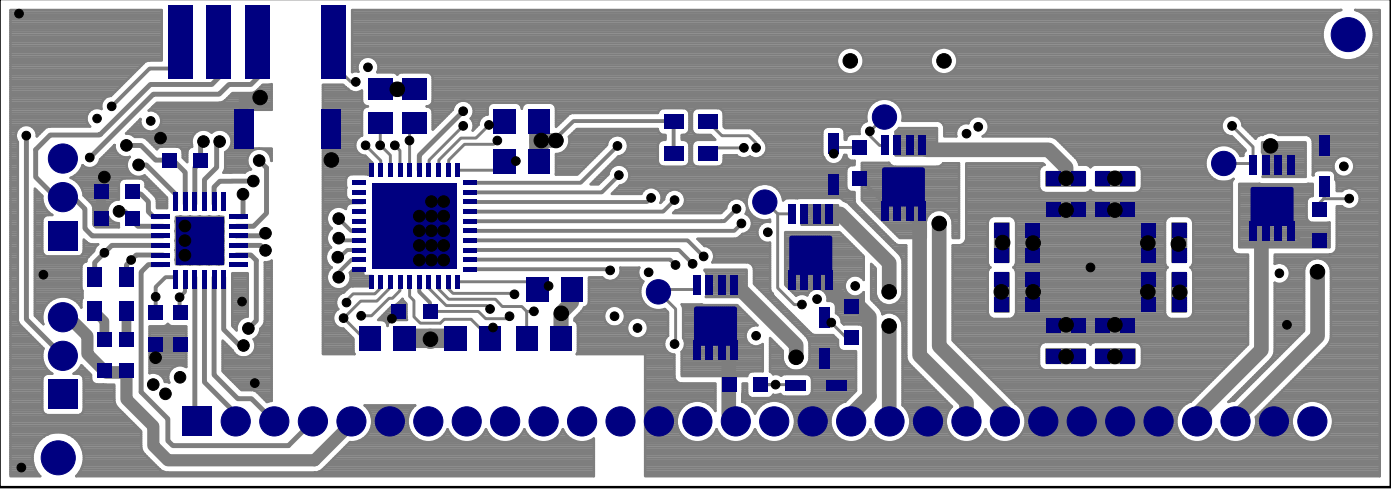
VERSION	FEATURES
DC1843A	DC1680A: Motherboard with Integrated Magjack DC1842A: 8-Port PSE Daughter Card
DC1843B	DC1680B: Motherboard with Discrete Ethernet Transformers DC1842B: 8-Port PSE Daughter Card with Increased Surge Protection

DEMONSTRATION CIRCUIT 1842B LAYOUT

Top Assembly

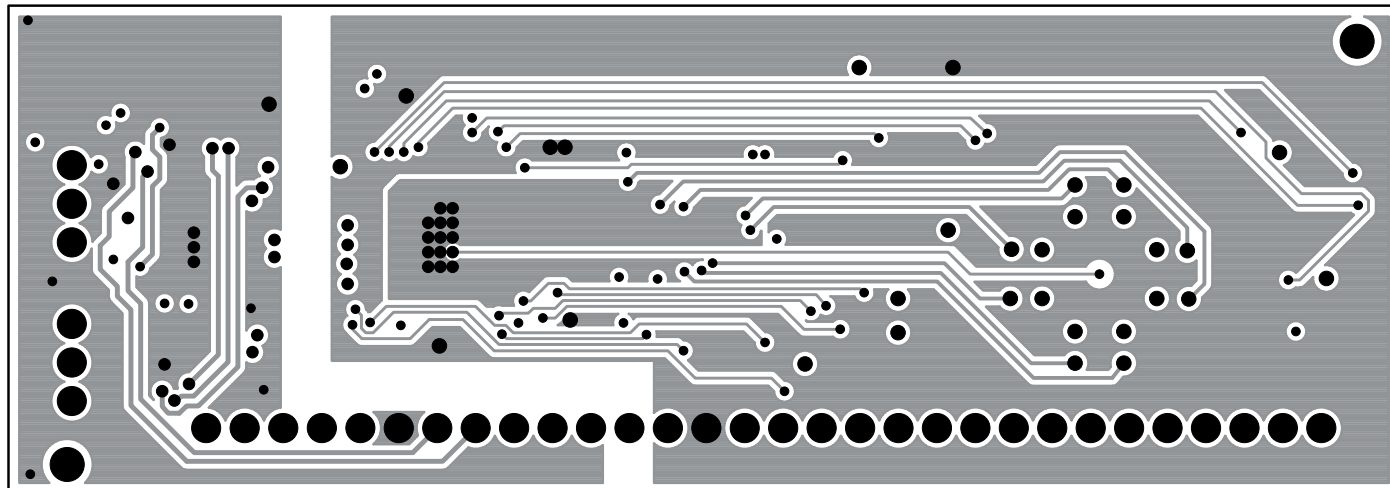


Layer 1: Top Layer

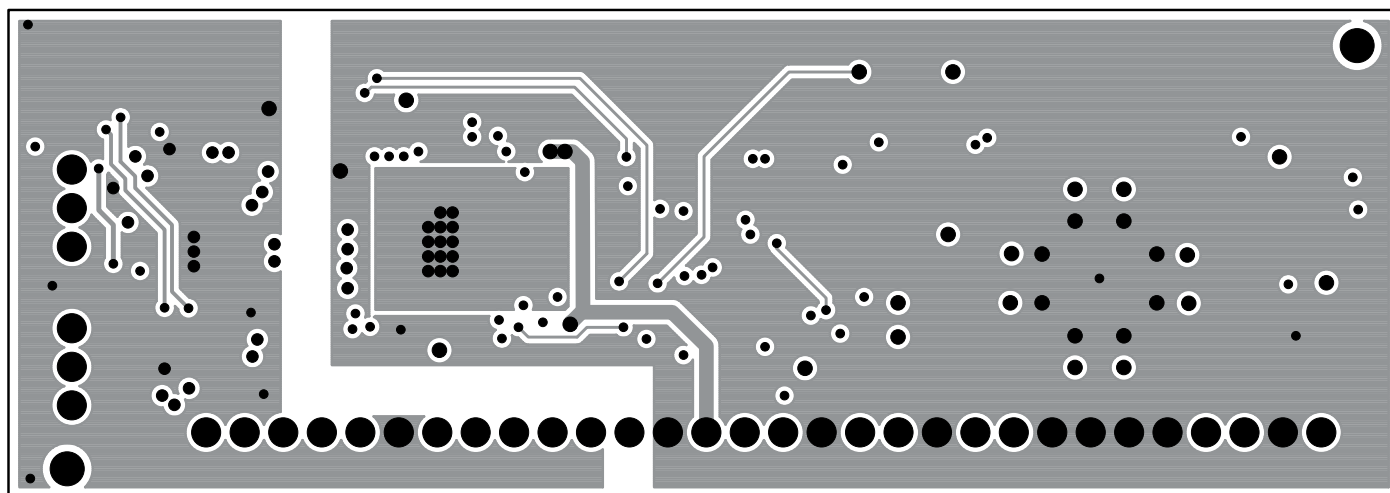


DEMONSTRATION CIRCUIT 1842B LAYOUT

Layer 2: V_{EE} Plane 1

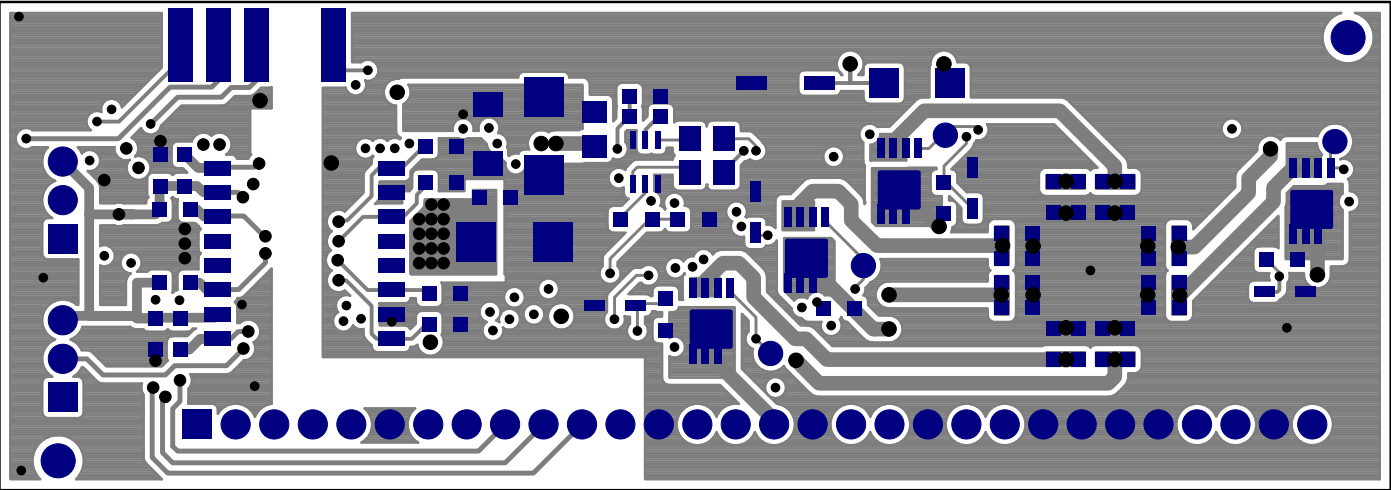


Layer 3: V_{EE} Plane 2

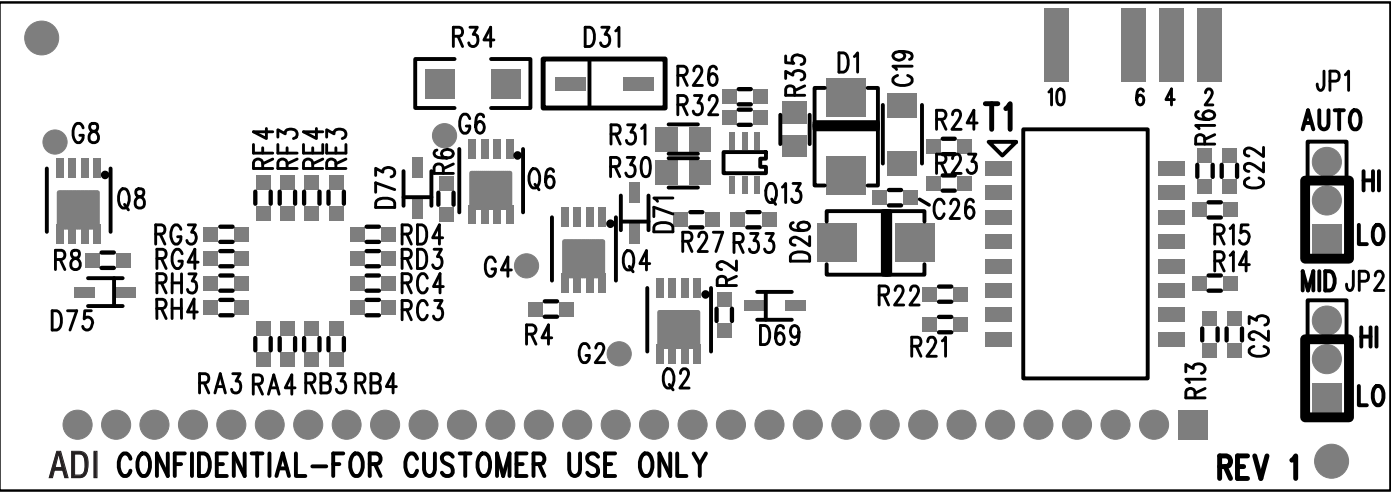


DEMONSTRATION CIRCUIT 1842B LAYOUT

Layer 4: Bottom Layer

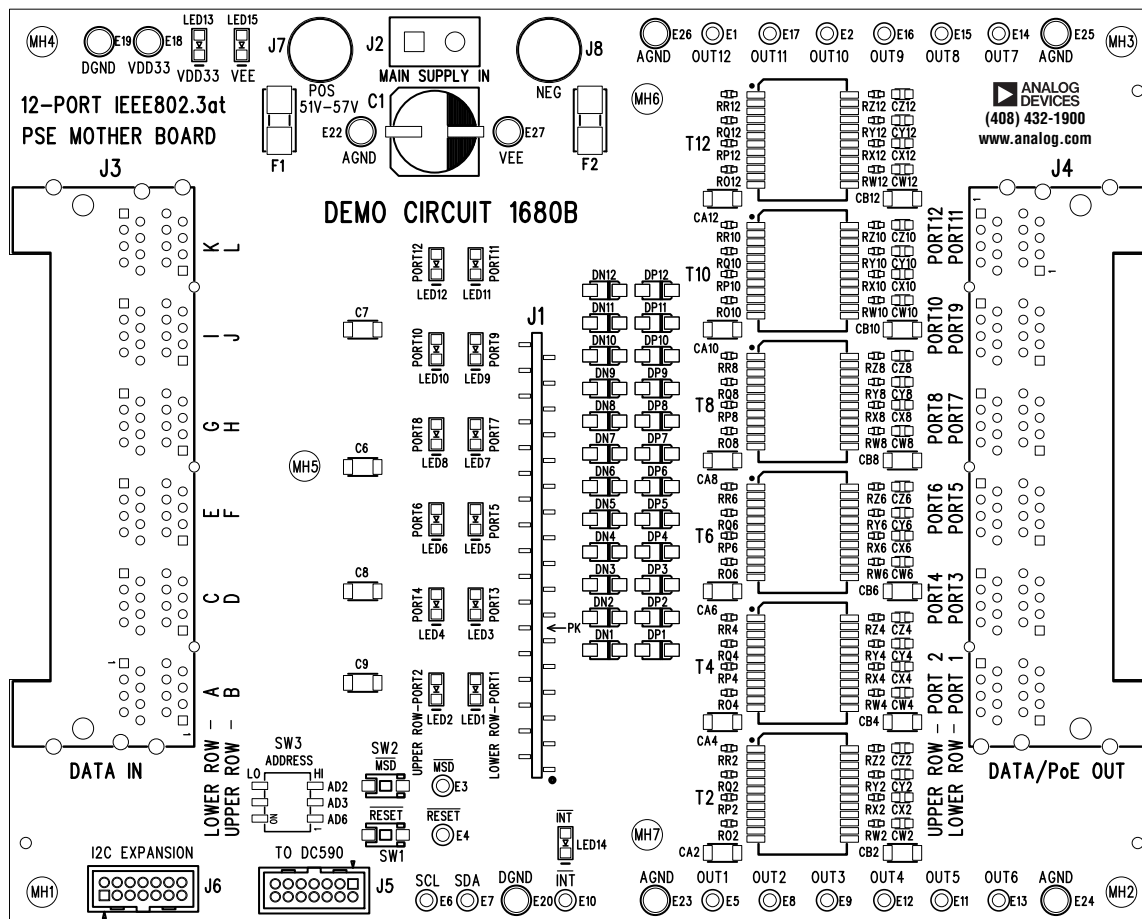


Bottom Assembly



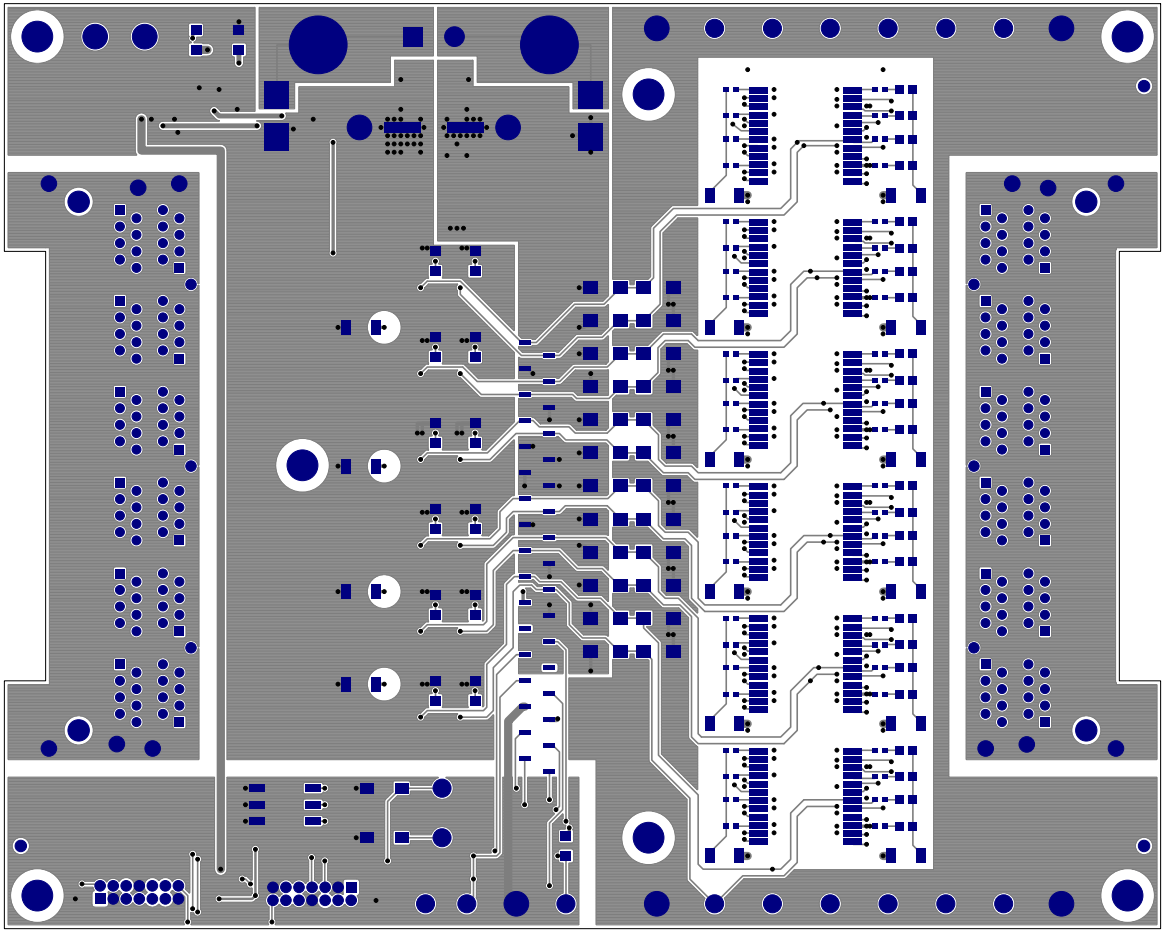
DEMONSTRATION CIRCUIT 1680B LAYOUT

Top Assembly



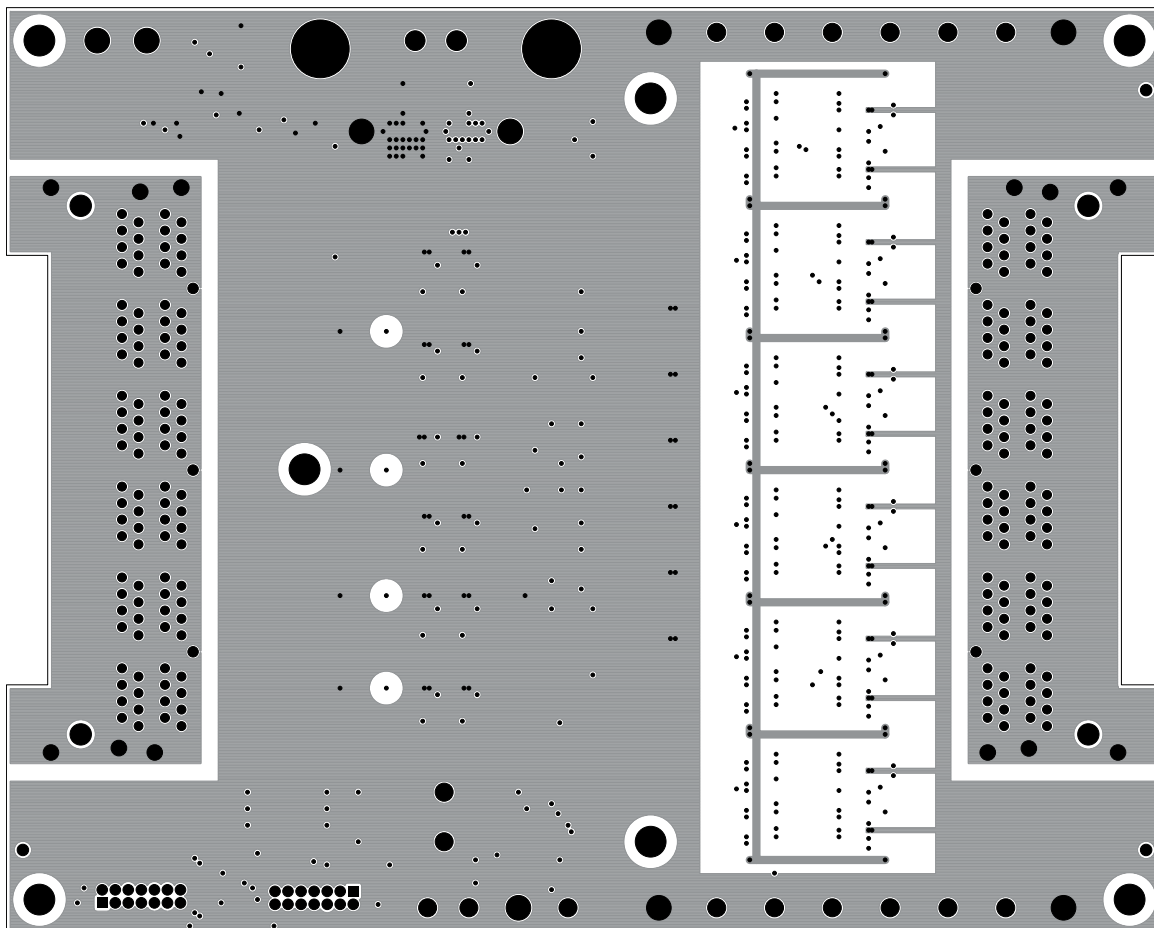
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 1: Top Layer



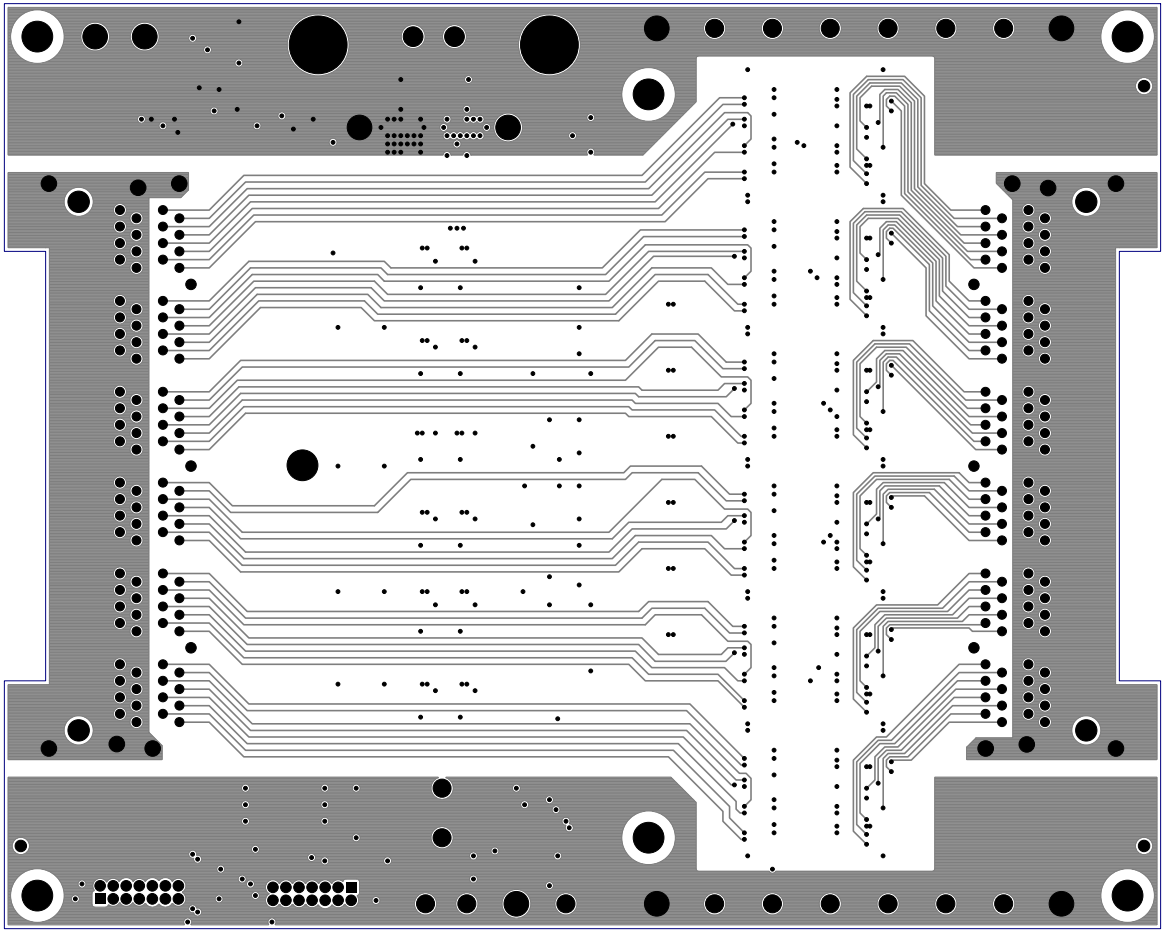
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 2: AGND, CGND Plane 1



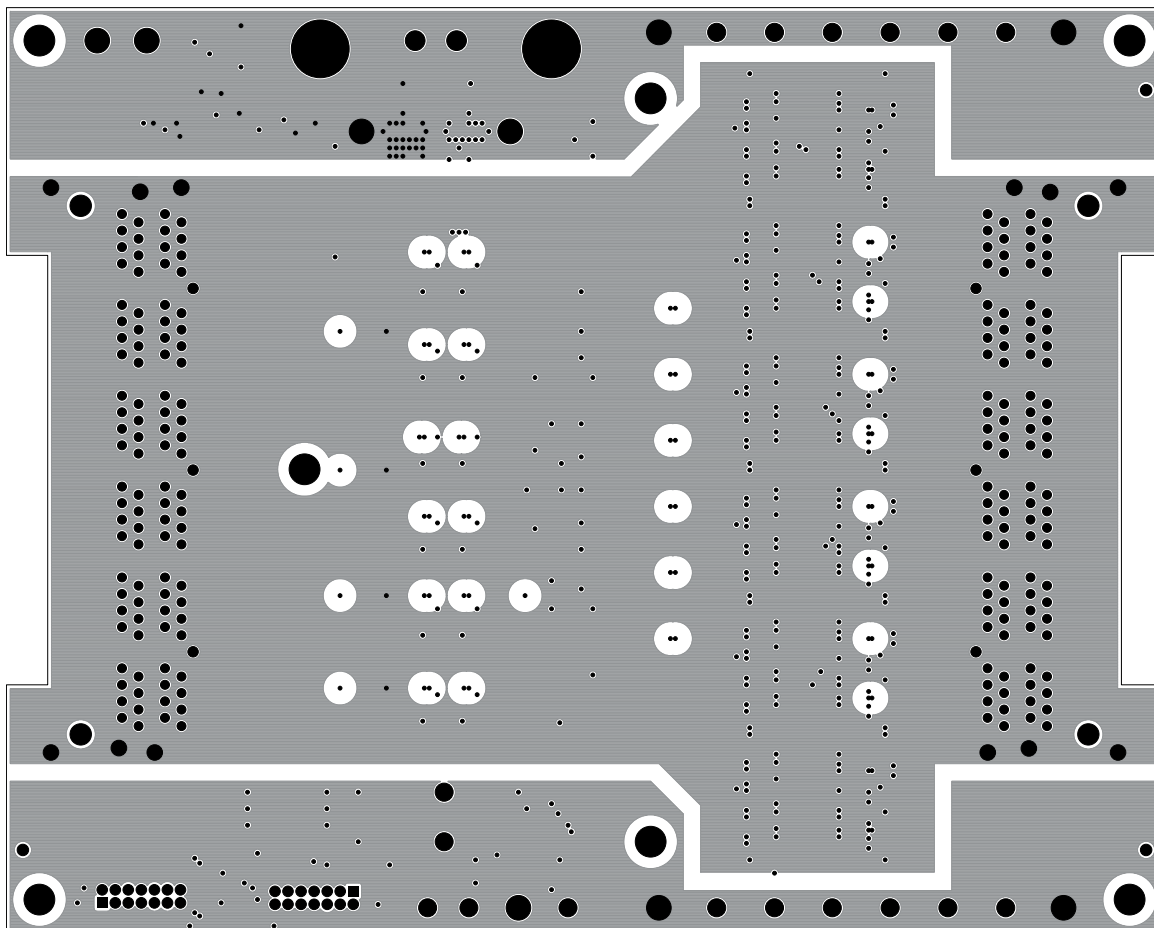
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 3: SIG, AGND, CGND Plane 2



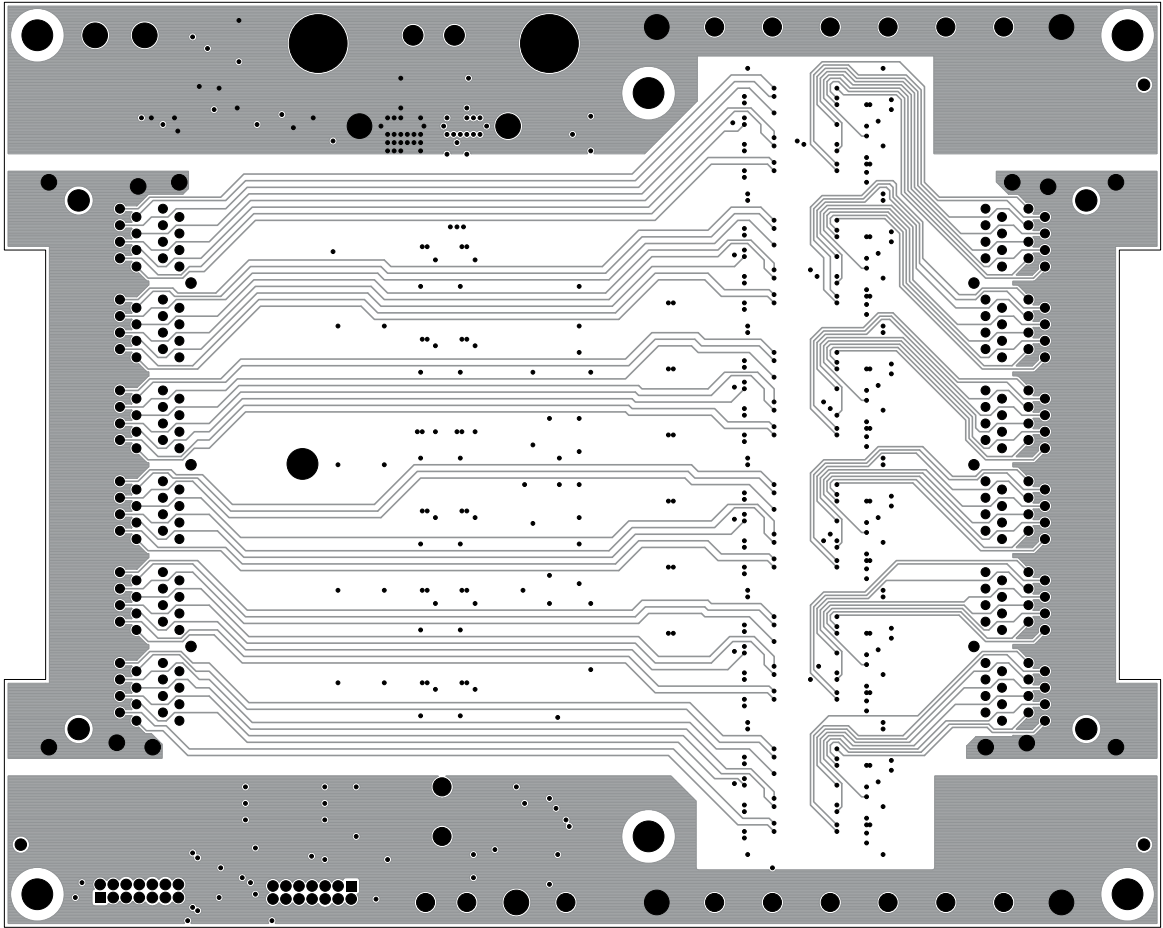
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 4: SIG, AGND, CGND Plane 3



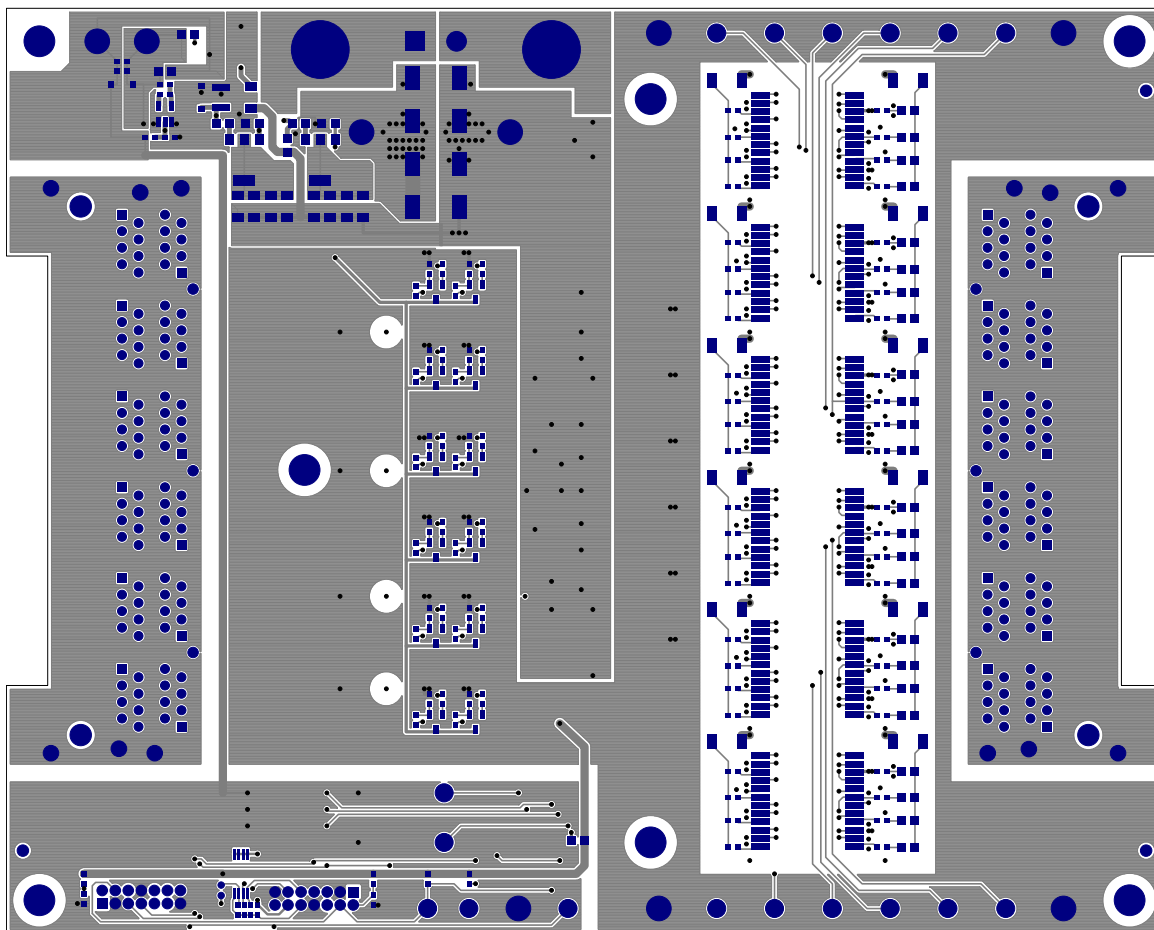
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 5: SIG, AGND, CGND Plane 4



DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 6: Bottom Layer

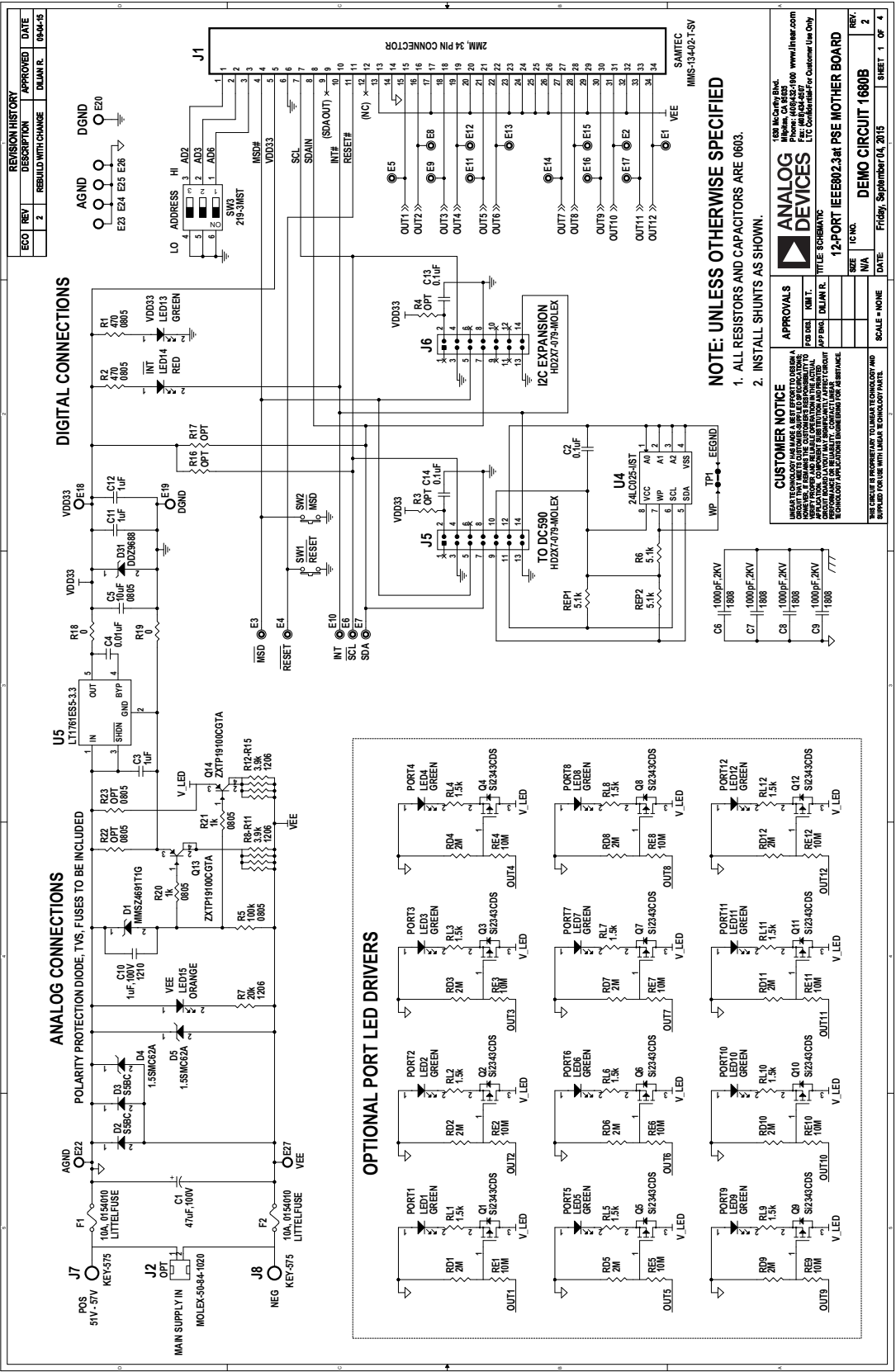


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LOWER ROW - PORT 1 PORT3 PORT5 PORT7 PORT9 PORT11
101 107 81 87 61 67 41 47 21 27 1 5 7 11 17 23 29 35 41 47 53 59 65 71 77 83 89 95 101 107 113 119 125 131 137 143 149 155 161 167 173 179 185 191 197 203 209 215 221 227 233 239 245 251 257 263 269 275 281 287 293 299 305 311 317 323 329 335 341 347 353 359 365 371 377 383 389 395 401 407 413 419 425 431 437 443 449 455 461 467 473 479 485 491 497 503 509 515 521 527 533 539 545 551 557 563 569 575 581 587 593 599 605 611 617 623 629 635 641 647 653 659 665 671 677 683 689 695 701 707 713 719 725 731 737 743 749 755 761 767 773 779 785 791 797 803 809 815 821 827 833 839 845 851 857 863 869 875 881 887 893 899 905 911 917 923 929 935 941 947 953 959 965 971 977 983 989 995 1001 1007 1013 1019 1025 1031 1037 1043 1049 1055 1061 1067 1073 1079 1085 1091 1097 1103 1109 1115 1121 1127 1133 1139 1145 1151 1157 1163 1169 1175 1181 1187 1193 1199 1205 1211 1217 1223 1229 1235 1241 1247 1253 1259 1265 1271 1277 1283 1289 1295 1301 1307 1313 1319 1325 1331 1337 1343 1349 1355 1361 1367 1373 1379 1385 1391 1397 1403 1409 1415 1421 1427 1433 1439 1445 1451 1457 1463 1469 1475 1481 1487 1493 1499 1505 1511 1517 1523 1529 1535 1541 1547 1553 1559 1565 1571 1577 1583 1589 1595 1601 1607 1613 1619 1625 1631 1637 1643 1649 1655 1661 1667 1673 1679 1685 1691 1697 1703 1709 1715 1721 1727 1733 1739 1745 1751 1757 1763 1769 1775 1781 1787 1793 1799 1805 1811 1817 1823 1829 1835 1841 1847 1853 1859 1865 1871 1877 1883 1889 1895 1901 1907 1913 1919 1925 1931 1937 1943 1949 1955 1961 1967 1973 1979 1985 1991 1997 2003 2009 2015 2021 2027 2033 2039 2045 2051 2057 2063 2069 2075 2081 2087 2093 2099 2105 2111 2117 2123 2129 2135 2141 2147 2153 2159 2165 2171 2177 2183 2189 2195 2201 2207 2213 2219 2225 2231 2237 2243 2249 2255 2261 2267 2273 2279 2285 2291 2297 2303 2309 2315 2321 2327 2333 2339 2345 2351 2357 2363 2369 2375 2381 2387 2393 2399 2405 2411 2417 2423 2429 2435 2441 2447 2453 2459 2465 2471 2477 2483 2489 2495 2501 2507 2513 2519 2525 2531 2537 2543 2549 2555 2561 2567 2573 2579 2585 2591 2597 2603 2609 2615 2621 2627 2633 2639 2645 2651 2657 2663 2669 2675 2681 2687 2693 2699 2705 2711 2717 2723 2729 2735 2741 2747 2753 2759 2765 2771 2777 2783 2789 2795 2801 2807 2813 2819 2825 2831 2837 2843 2849 2855 2861 2867 2873 2879 2885 2891 2897 2903 2909 2915 2921 2927 2933 2939 2945 2951 2957 2963 2969 2975 2981 2987 2993 2999 3005 3011 3017 3023 3029 3035 3041 3047 3053 3059 3065 3071 3077 3083 3089 3095 3101 3107 3113 3119 3125 3131 3137 3143 3149 3155 3161 3167 3173 3179 3185 3191 3197 3203 3209 3215 3221 3227 3233 3239 3245 3251 3257 3263 3269 3275 3281 3287 3293 3299 3305 3311 3317 3323 3329 3335 3341 3347 3353 3359 3365 3371 3377 3383 3389 3395 3401 3407 3413 3419 3425 3431 3437 3443 3449 3455 3461 3467 3473 3479 3485 3491 3497 3503 3509 3515 3521 3527 3533 3539 3545 3551 3557 3563 3569 3575 3581 3587 3593 3599 3605 3611 3617 3623 3629 3635 3641 3647 3653 3659 3665 3671 3677 3683 3689 3695 3701 3707 3713 3719 3725 3731 3737 3743 3749 3755 3761 3767 3773 3779 3785 3791 3797 3803 3809 3815 3821 3827 3833 3839 3845 3851 3857 3863 3869 3875 3881 3887 3893 3899 3905 3911 3917 3923 3929 3935 3941 3947 3953 3959 3965 3971 3977 3983 3989 3995 4001 4007 4013 4019 4025 4031 4037 4043 4049 4055 4061 4067 4073 4079 4085 4091 4097 4103 4109 4115 4121 4127 4133 4139 4145 4151 4157 4163 4169 4175 4181 4187 4193 4199 4205 4211 4217 4223 4229 4235 4241 4247 4253 4259 4265 4271 4277 4283 4289 4295 4301 4307 4313 4319 4325 4331 4337 4343 4349 4355 4361 4367 4373 4379 4385 4391 4397 4403 4409 4415 4421 4427 4433 4439 4445 4451 4457 4463 4469 4475 4481 4487 4493 4499 4505 4511 4517 4523 4529 4535 4541 4547 4553 4559 4565 4571 4577 4583 4589 4595 4601 4607 4613 4619 4625 4631 4637 4643 4649 4655 4661 4667 4673 4679 4685 4691 4697 4703 4709 4715 4721 4727 4733 4739 4745 4751 4757 4763 4769 4775 4781 4787 4793 4799 4805 4811 4817 4823 4829 4835 4841 4847 4853 4859 4865 4871 4877 4883 4889 4895 4901 4907 4913 4919 4925 4931 4937 4943 4949 4955 4961 4967 4973 4979 4985 4991 4997 5003 5009 5015 5021 5027 5033 5039 5045 50

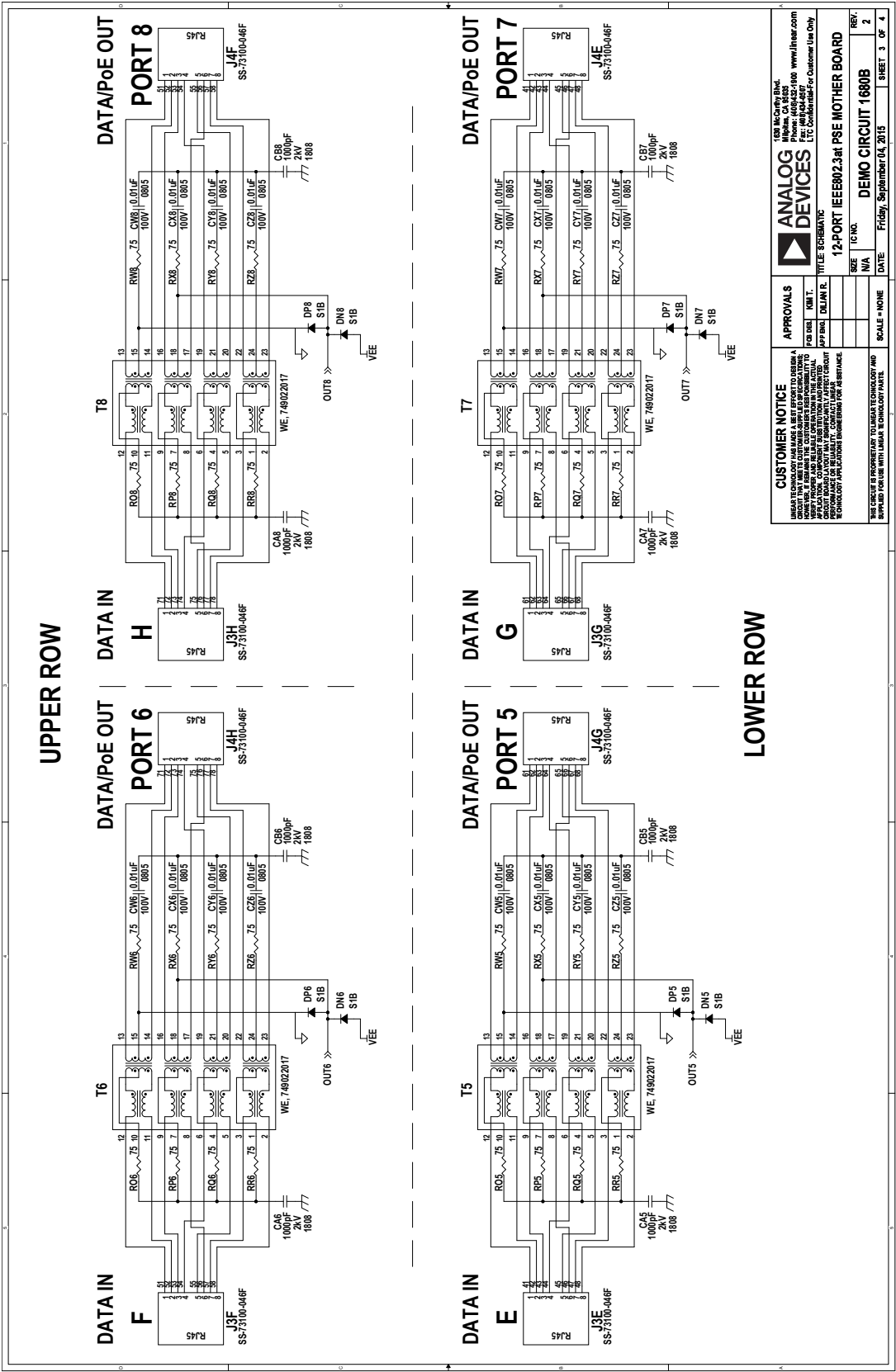


DC1680B SCHEMATIC DIAGRAM

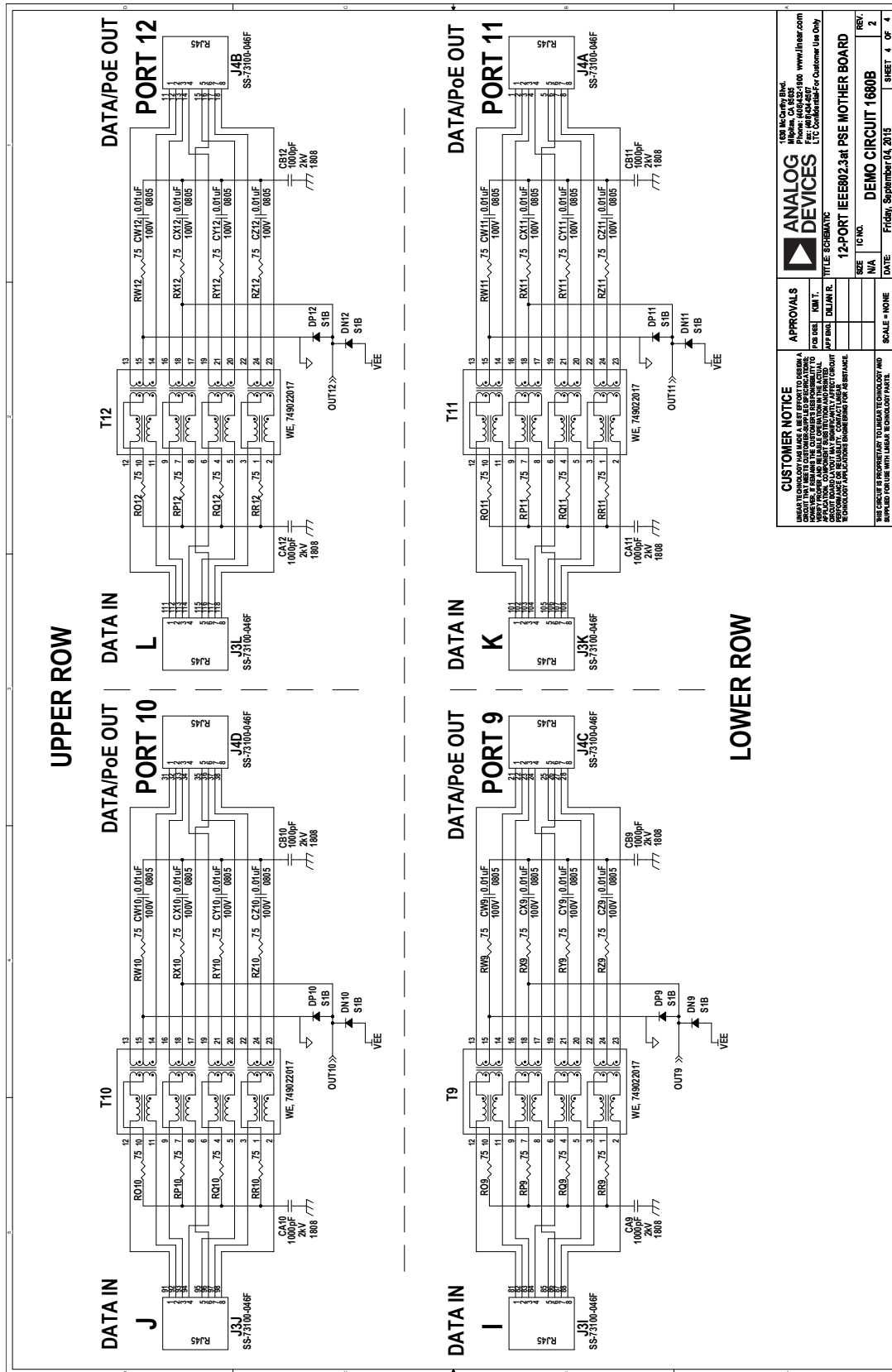




DC1680B SCHEMATIC DIAGRAM



DC1680B SCHEMATIC DIAGRAM



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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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