# 74ALVC125

## Quad buffer/line driver; 3-state

Rev. 02 — 10 January 2008 Product data sheet

## 1. General description

The 74ALVC125 is a quad non-inverting buffer/line driver with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH on the $n\overline{OE}$ pin causes the outputs to assume a high-impedance OFF-state.

## 2. Features

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A 115-A exceeds 200 V

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74ALVC125D | –40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74ALVC125PW | –40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74ALVC125BQ | –40 °C to +85 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

## 4. Functional diagram

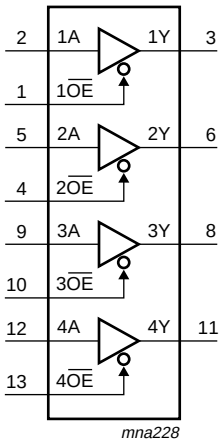



**Fig 1. Logic symbol**

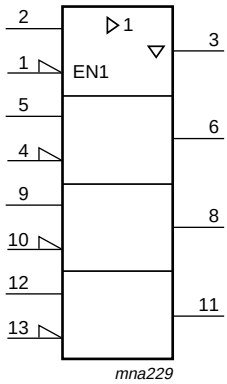



**Fig 2. IEC logic symbol**

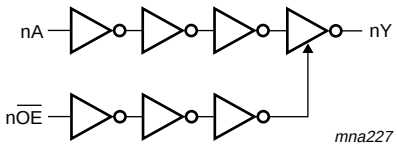



**Fig 3. Logic diagram (one buffer)**

## 5. Pinning information

### 5.1 Pinning

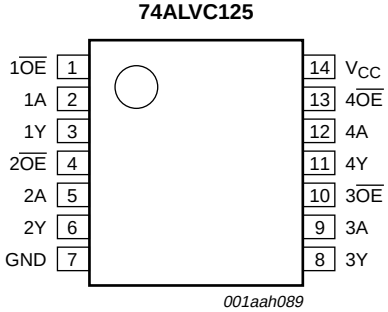
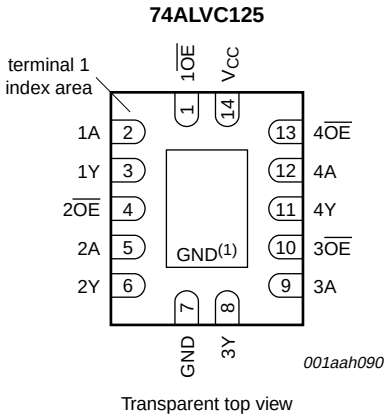



**Fig 4. Pin configuration SO14 and TSSOP14**




Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

**Fig 5. Pin configuration DHVQFN14**

### 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| nA | 2, 5, 9, 12 | data input |
| nY | 3, 6, 8, 11 | bus output |
| $n\overline{OE}$ | 1, 4, 10, 13 | output enable (active LOW) |
| $V_{CC}$ | 14 | supply voltage |
| GND | 7 | ground (0 V) |

## 6. Functional description

**Table 3. Function table[1]**

| Input | | Output |
|---|---|---|
| $n\overline{OE}$ | nA | nY |
| L | L | L |
| L | H | H |
| H | X | Z |

[1] H = HIGH voltage level
L = LOW voltage level
X= don't care
Z = high-impedance OFF-state

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –50 | - | mA |
| $V_I$ | input voltage | | [1] | –0.5 | +4.6 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | output HIGH or LOW state | [1][2] | –0.5 | $V_{CC}$ + 0.5 | V |
| | | output 3-state | | –0.5 | +4.6 | V |
| | | Power-down mode, $V_{CC}$ = 0 V | [2] | –0.5 | +4.6 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | –100 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +85 °C | [3] | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] When $V_{CC}$ = 0 V (Power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 3.6 | V |
| $V_O$ | output voltage | output HIGH or LOW state | 0 | $V_{CC}$ | V |
| | | output 3-state | 0 | 3.6 | V |
| | | Power-down mode; $V_{CC}$ = 0 V | 0 | 3.6 | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | 0 | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 10 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = –100 µA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ – 0.2 | - | - | V |
| | | $I_O$ = –6 mA; $V_{CC}$ = 1.65 V | 1.25 | 1.51 | - | V |
| | | $I_O$ = –12 mA; $V_{CC}$ = 2.3 V | 1.8 | 2.10 | - | V |
| | | $I_O$ = –18 mA; $V_{CC}$ = 2.3 V | 1.7 | 2.01 | - | V |
| | | $I_O$ = –12 mA; $V_{CC}$ = 2.7 V | 2.2 | 2.53 | - | V |
| | | $I_O$ = –18 mA; $V_{CC}$ = 3.0 V | 2.4 | 2.76 | - | V |
| | | $I_O$ = –24 mA; $V_{CC}$ = 3.0 V | 2.2 | 2.68 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 3.6 V | - | - | 0.2 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 1.65 V | - | 0.11 | 0.3 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.3 V | - | 0.17 | 0.4 | V |
| | | $I_O$ = 18 mA; $V_{CC}$ = 2.3 V | - | 0.25 | 0.6 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | 0.16 | 0.4 | V |
| | | $I_O$ = 18 mA; $V_{CC}$ = 3.0 V | - | 0.23 | 0.4 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | 0.30 | 0.55 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = 3.6 V or GND | - | ±0.1 | ±5 | µA |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 1.65 V to 3.6 V; $V_O$ = 3.6 V or GND; | - | ±0.1 | ±10 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 3.6 V | - | ±0.1 | ±10 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I = V_{CC}$ or GND; $I_O$ = 0 A | - | 0.2 | 10 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3.0 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; $I_O$ = 0 A | - | 5 | 750 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | pF |

[1] All typical values are measured at $V_{CC}$ = 3.3 V (unless stated otherwise) and $T_{amb}$ = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $t_{pd}$ | propagation delay | nA to nY; see Figure 6 | [2] | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 1.3 | 2.4 | 5.3 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.0 | 1.7 | 3.2 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 2.0 | 3.1 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.1 | 1.8 | 2.8 | ns |
| $t_{en}$ | enable time | $n\overline{OE}$ to nY; see Figure 7 | [2] | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 1.4 | 3.9 | 6.4 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.0 | 2.2 | 4.1 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 2.7 | 4.3 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.0 | 1.9 | 3.5 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nY; see Figure 7 | [2] | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 1.8 | 3.9 | 5.9 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.0 | 2.1 | 3.4 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 2.9 | 4.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.4 | 2.7 | 4.0 | ns |

**Table 7. Dynamic characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.*

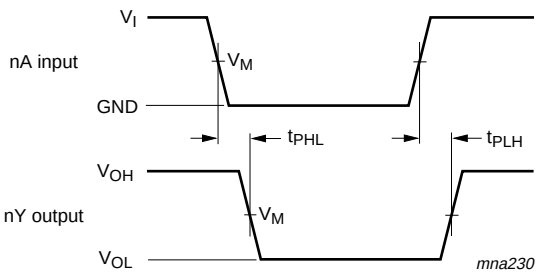
| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $C_{PD}$ | power dissipation capacitance | per buffer; $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.3 V [3] | | | | |
| | | outputs HIGH or LOW state | - | 27 | - | pF |
| | | outputs 3-state | - | 5 | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C

[2] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.
$t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.
$t_{dis}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

## 11. Waveforms



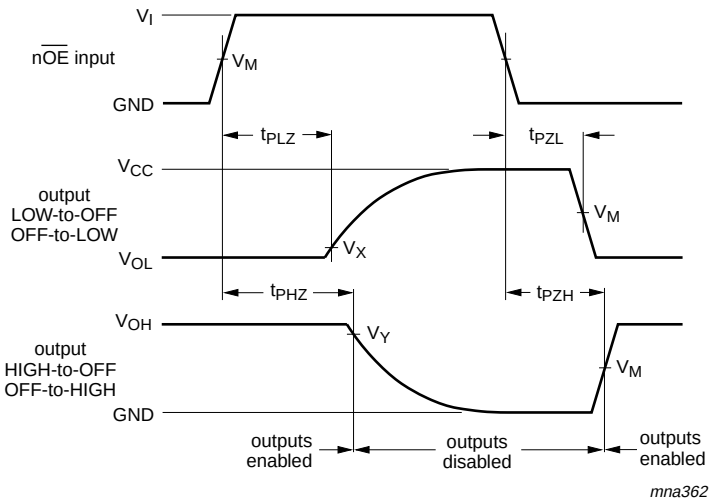

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 6. Input nA to output nY propagation delay times**

**Table 8. Measurement points**

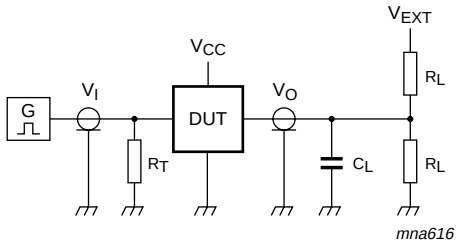
| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ – 0.15 V |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ – 0.15 V |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ – 0.3 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ – 0.3 V |




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 7. Enable and disable times**




Test data is given in Table 9.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

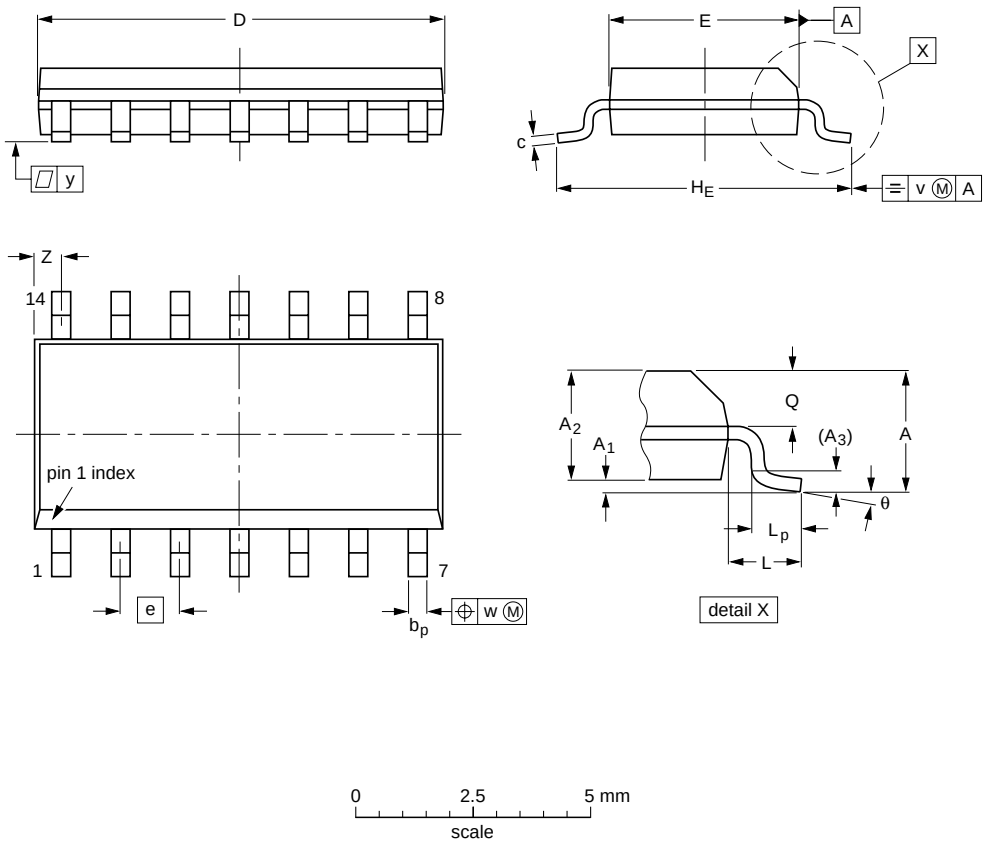
**Fig 8. Test circuitry for switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | open | $2 \times V_{CC}$ | GND |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 6 V | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 6 V | GND |

## 12. Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

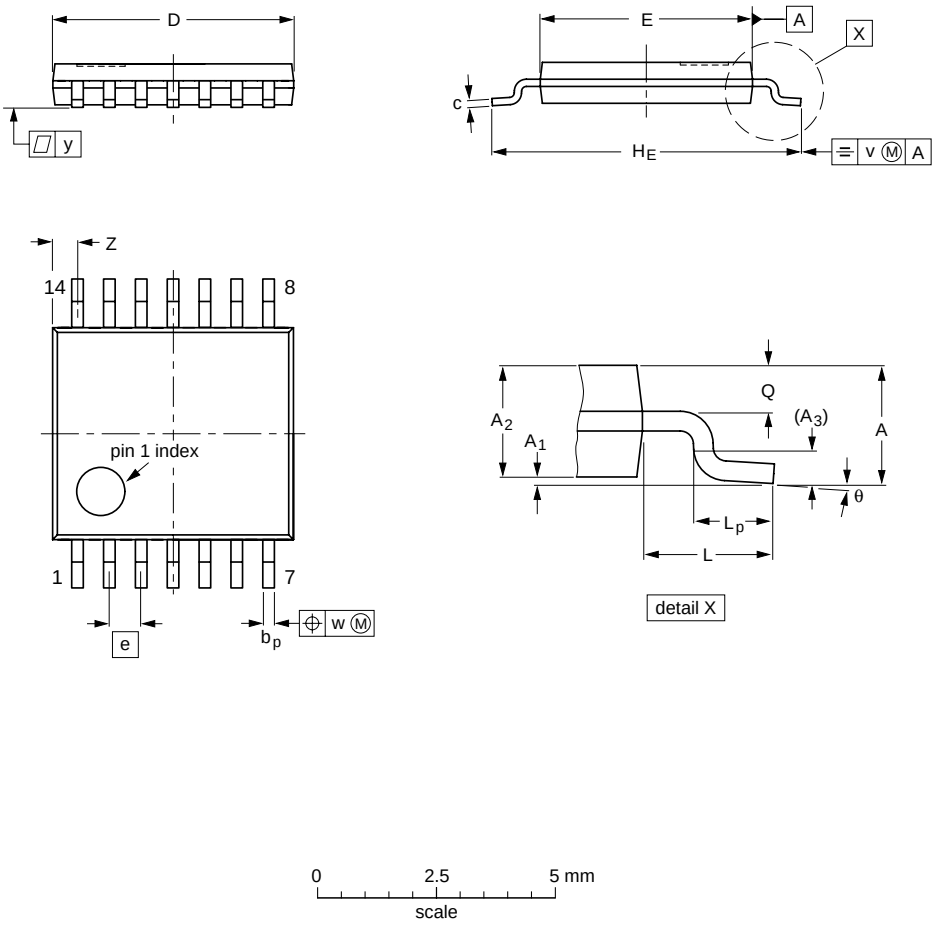
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT108-1 (SO14)**

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | $8^o$<br>$0^o$ |

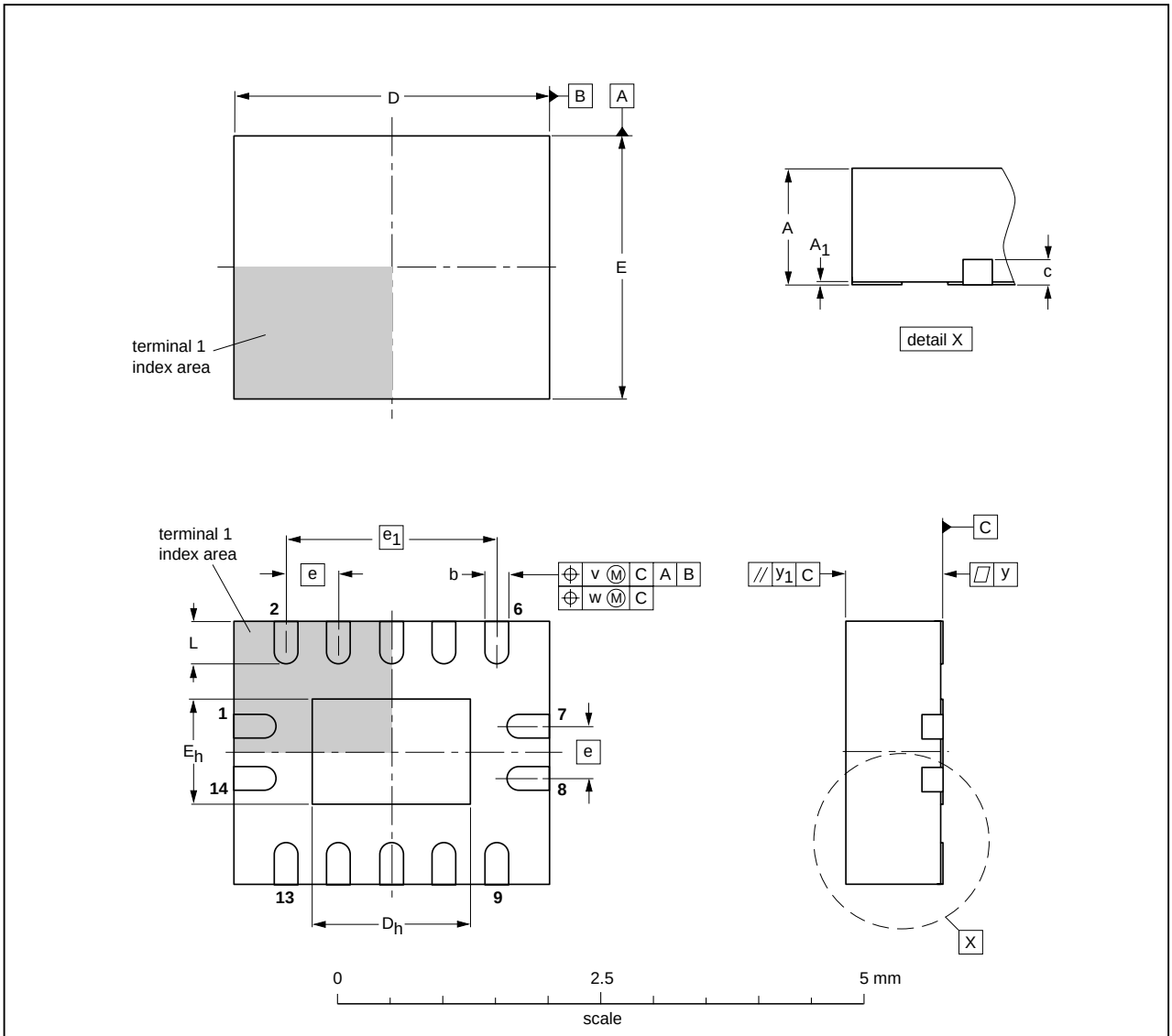
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 10. Package outline SOT402-1 (TSSOP14)**

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm** **SOT762-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.1<br>2.9 | 1.65<br>1.35 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT762-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 11. Package outline SOT762-1 (DHVQFN14)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged-Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVC125_2 | 20080110 | Product data sheet | - | 74ALVC125_1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 3: DHVQFN14 package added.<br>• Section 7: derating values added for DHVQFN14 package.<br>• Section 12: outline drawing added for DHVQFN14 package. | | | |
| 74ALVC125_1 | 20021118 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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# 16. Contact information

For additional information, please visit: **http://www.nexperia.com**

For sales office addresses, send an email to: **salesaddresses@nexperia.com**

## 17. Contents





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**Date of release: 10 January 2008**

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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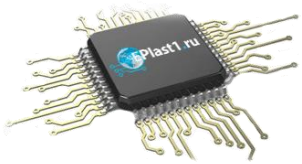
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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