

TET2000 Series

AC-DC / HVDC Front-End Power Supplies

The TET2000 Series is a 2100 Watt AC-DC power-factor-corrected (PFC) and DC/DC power supply that converts standard AC mains power or high voltage DC bus voltages into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The TET2000-12-086 Series meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- Best-in-class, 80 PLUS certified “Titanium” efficiency
- Wide input voltage range: 180 - 264 VAC / 2100 W, 90 - 180 VAC / Linear derating
- AC input with power factor correction
- Always-on 24 W standby output (12 V / 2 A)
- Hot-plug capability
- Parallel operation with active current sharing thru analog bus
- Full digital controls for improved performance
- High density design: 51 W/in³
- Small form factor: 195 x 86 x 40 mm (7.68 x 3.39 x 1.57 in)
- Up to 400 kHz
- I2C communication interface with Power Management Bus protocol for monitoring, control, and firmware update via bootloader
- RoHS Compliant
- Status LED with fault signaling
- Safety-approved to IEC 62368-1:2014 2nd ed. and UL 62368-1 2nd ed.
- US patents



Applications

- High Performance Servers
- Routers
- Switches



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1. ORDERING INFORMATION

| TET | 2000 | - | 12 | - | 086 | x | A | Option Code |
|----------------|-------------|------|-----------|------|-------|---|-------|--------------------------|
| Product Family | Power Level | Dash | V1 Output | Dash | Width | Airflow | Input | |
| TET Front-End | 2000 W | | 12 V | | 86 mm | N: Normal ¹⁾ R: Reverse ²⁾ | A: AC | Blank: Standard model |

¹⁾ Rear to front

²⁾ Front to rear

2. OVERVIEW

The TET2000-12-086 Series is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonant-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range and minimal linear derating of output power with respect to ambient temperature, the TET2000-12-86NA maximizes power availability in demanding server, switch, and router applications. The power supply is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on +12V standby provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LED. In addition, the power supply can be monitored and controlled (i.e. fan speed setpoint) via I2C communication interface with Power Management Bus protocol. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The same I2C bus supports the bootloader to allow field update of the firmware in the DSP controllers.

Cooling is managed by a fan, controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C buses.

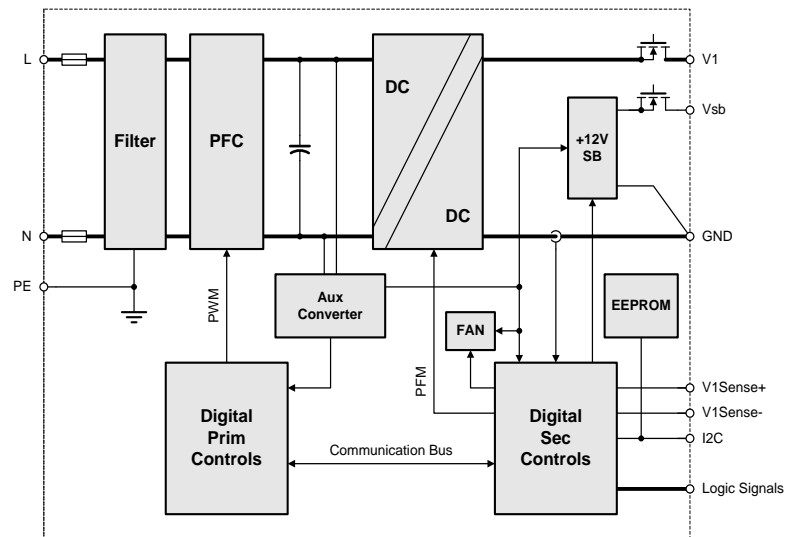


Figure 1. TET2000-12-086 Series Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the supply.

| PARAMETER | CONDITIONS / DESCRIPTION | MIN | MAX | UNITS |
|------------|--------------------------|------------|-----|-------|
| V_i maxc | Maximum Input | Continuous | 264 | VAC |

4. INPUT

General Condition: $T_A = 0 \dots +50 \text{ }^\circ\text{C}$, unless otherwise noted.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT | | |
|-----------------|--------------------------------------|---|-------|-------|------------------|------|-----|
| $V_{i,nom}$ | AC Nominal Input Voltage | 100 | 230 | 240 | VAC | | |
| V_i | AC Input Voltage Ranges | Normal operating ($V_{i,min}$ to $V_{i,max}$) | | 264 | VAC | | |
| $V_{i,nom,DC}$ | DC Nominal Input Voltage | Rated HVDC | | 240 | VDC | | |
| $V_{i,DC}$ | DC Input Voltage Ranges | Normal operating ($V_{i,min}$ to $V_{i,max}$) | | 300 | VDC | | |
| $V_{i,derated}$ | Derated Input Voltage Range | See section 10.3 | | 180 | VAC | | |
| $I_{i,max}$ | Max Input Current | $V_i > 200 \text{ VAC}, >100 \text{ VAC}$ | | 13.5 | A _{rms} | | |
| $I_{i,p}$ | Inrush Current Limitation | $V_{i,min}$ to $V_{i,max}, T_{NTC} = 25^\circ\text{C}$ (See Figure 2) | | 35 | A _p | | |
| F_i | Input Frequency | 47 | 50/60 | 63 | Hz | | |
| PF | Power Factor | $V_{i,nom}, 50\text{Hz}, > 0.2 I_{i,nom}$ | | 0.95 | 0.96 | W/VA | |
| $V_{i,on}$ | Turn-on Input Voltage ²⁾ | Ramping up | | 84 | 87 | 90 | VAC |
| $V_{i,off}$ | Turn-off Input Voltage ²⁾ | Ramping down | | 79 | 82 | 85 | VAC |
| η | Efficiency Without Fan | $V_i = 230 \text{ VAC}, 0.1 \cdot I_{x,nom}, V_{x,nom}, T_A = 25^\circ\text{C}$ | | 94.2 | | % | |
| | | $V_i = 230 \text{ VAC}, 0.2 \cdot I_{x,nom}, V_{x,nom}, T_A = 25^\circ\text{C}$ | | 95.6 | | | |
| | | $V_i = 230 \text{ VAC}, 0.5 \cdot I_{x,nom}, V_{x,nom}, T_A = 25^\circ\text{C}$ | | 96.35 | | | |
| | | $V_i = 230 \text{ VAC}, I_{x,nom}, V_{x,nom}, T_A = 25^\circ\text{C}$ | | 94.75 | | | |
| T_{hold} | Hold-up Time | After last AC 45C degree (Worst case), $V_i > 11.7\text{V}, V_{SB}$ within regulation, $V_i = 230 \text{ VAC}, P_{x,nom}$ | | 10 | 12 | ms | |

²⁾ The Front-End is provided with a typical hysteresis of 5 V during turn-on and turn-off within the ranges.

4.1 INPUT FUSE

Quick-acting 16 A input fuses (5.4 × 22.5 in mm) in series with the L-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 3.88 μF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through a PTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations below 5sec interval time at maximum input, high temperature condition, or else the internal in-rush current limiting device PTC may not sufficiently cool down and self over temperature protection may result.

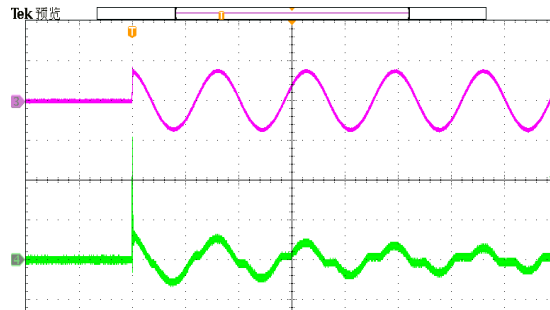


Figure 2. Inrush current, $V_{in} = 264\text{Vac}, 90^\circ$
 CH3: V_{in} (500V/div), CH4: I_{in} (10A/div)

4.3 INPUT UNDER-VOLTAGE

If the RMS value of input voltage (either AC or DC) stays below the input undervoltage lockout threshold $V_{i,on}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) (see *Figure 3*) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform. At DC input voltage the PFC is still in operation, but the input current will be DC in this case.

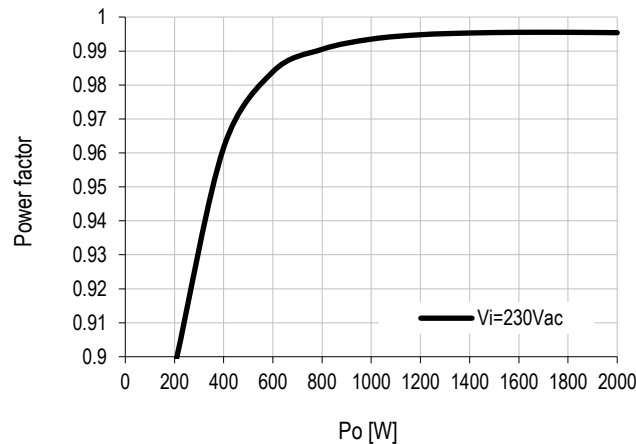


Figure 3. Power Factor vs. Load

4.5 EFFICIENCY

The high efficiency (see *Figure 4*) is achieved by using state-of-the-art GaN power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

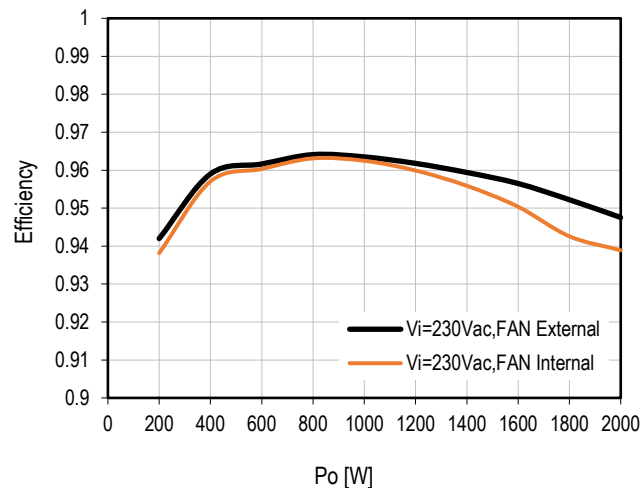


Figure 4. Power Factor vs. Load

5. OUTPUT

General Condition: $T_a = 0 \dots +50^\circ\text{C}$ unless otherwise specified.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|--|------------------------------|--|--|--------|-------------------------------|
| Main Output V_1 | | | | | |
| $V_1 \text{ nom}$ | Nominal Output Voltage | | 12.3 | | VDC |
| $V_1 \text{ set}$ | Output Setpoint Accuracy | $0.5 \cdot I_1 \text{ nom}$, $T_{\text{amb}} = 25^\circ\text{C}$ | | +0.5 | % $V_1 \text{ nom}$ |
| $dV_1 \text{ tot}$ | Total Regulation | $V_1 \text{ min}$ to $V_1 \text{ max}$, 0 to 100% $I_1 \text{ nom}$, $T_a \text{ min}$ to $T_a \text{ max}$ | | +2 | % $V_1 \text{ nom}$ |
| $P_1 \text{ nomll}$ | Nominal Output Power | $V_1 = 12.3 \text{ VDC}$, $V_{\text{in}} < 180 \text{ VAC}$ | See Section 10.3 <i>Figure 42</i> | | |
| $I_1 \text{ nomll}$ | Nominal Output Current | $V_1 = 12.3 \text{ VDC}$, $V_{\text{in}} < 180 \text{ VAC}$ | See Section 6.3 <i>Figure 24 and Table 1</i> | | |
| $P_1 \text{ nom}$ | Nominal Output Power | $V_1 = 12.3 \text{ VDC}$, $V_{\text{in}} > 180 \text{ VAC}$ | 2079 | | W |
| $I_1 \text{ nom}$ | Nominal Output Current | $V_1 = 12.3 \text{ VDC}$, $V_{\text{in}} > 180 \text{ VAC}$ | 169 | | A |
| $I_1 \text{ ol}$ | Short Time Over Load Current | $V_1 = 12.3 \text{ VDC}$, $V_{\text{in}} > 180 \text{ VAC}$ $T_a \text{ min}$ to $T_a \text{ max}$, maximum duration 20 ms (See Section 5.2) | | 203 | A |
| $V_1 \text{ pp}$ | Output Ripple Voltage | $V_1 \text{ nom}$, $I_1 \text{ nom}$, 20MHz BW (See Section 5.1) (see <i>Figure 11, 12</i>) | 80 | 120 | mVpp |
| $dV_1 \text{ Load}$ | Load Regulation | $V_1 = V_1 \text{ nom}$, 0 - 100 % $I_1 \text{ nom}$ | 110 | | mV |
| $dV_1 \text{ Line}$ | Line Regulation | $V_1 = V_1 \text{ min} \dots V_1 \text{ max}$ | 0 | | mV |
| dI_{share} | Current Sharing | $(I_x - I_y) / I_{\text{tot}}$, $I_{\text{tot}} > 25\% I_1 \text{ nom}$ | -5 | +5 | % |
| dV_{dyn} | Dynamic Load Regulation | $\Delta I_1 = 50\% I_1 \text{ nom}$, $I_1 = 5 \dots 100\% I_1 \text{ nom}$, $dI_1/dt = 1\text{A}/\mu\text{s}$, recovery within 1% of $V_1 \text{ nom}$ (see <i>Figure 13, 14, 15, 16</i>) | -0.6 | 0.6 | V |
| T_{rec} | Recovery Time | (see <i>Figure 13, 14, 15, 16</i>) | 0.5 | 1 | ms |
| $t_{\text{AC } V_1}$ | Start-up Time from AC | $V_1 = 10.8 \text{ VDC}$ (see <i>Figure 5</i>) | 2.7 | 3 | sec |
| $t_{V_1 \text{ rise}}$ | Rise Time | $V_1 = 10 \dots 90\% V_1 \text{ nom}$ (see <i>Figure 8</i>) | | 30 | ms |
| C_{Load} | Capacitive Loading | $T_a = 25^\circ\text{C}$ | | 20,000 | μF |
| Standby Output V_{SB} | | | | | |
| $V_{\text{SB}} \text{ nom}$ | Nominal Output Voltage | | 12.0 | | VDC |
| $V_{\text{SB}} \text{ set}$ | Output Setpoint Accuracy | $0.5 \cdot I_{\text{SB}} \text{ nom}$, $T_{\text{amb}} = 25^\circ\text{C}$ | -1 | +1 | % $V_{\text{SB}} \text{ nom}$ |
| $dV_{\text{SB}} \text{ tot}$ | Total Regulation | $V_{\text{SB}} \text{ min}$ to $V_{\text{SB}} \text{ max}$, 0 to 100% $I_{\text{SB}} \text{ nom}$, $T_a \text{ min}$ to $T_a \text{ max}$ | -3 | +3 | % $V_{\text{SB}} \text{ nom}$ |
| $P_{\text{SB}} \text{ nom}$ | Nominal Output Power | $V_{\text{SB}} = 12.0 \text{ VDC}$ | 24 | | W |
| $I_{\text{SB}} \text{ nom}$ | Nominal Output Current | $V_{\text{SB}} = 12.0 \text{ VDC}$ | 2 | | A |
| $V_{\text{SB}} \text{ pp}$ | Output Ripple Voltage | $V_{\text{SB}} \text{ nom}$, $I_{\text{SB}} \text{ nom}$, 20 MHz BW (See Section 5.1) (see <i>Figure 9, 10</i>) | 60 | 120 | mVpp |
| dV_{SB} | Droop | 0 - 100 % $I_{\text{SB}} \text{ nom}$ | 180 | | mV |
| dV_{SBdyn} | Dynamic Load Regulation | $\Delta I_{\text{SB}} = 50\% I_{\text{SB}} \text{ nom}$, $I_{\text{SB}} = 5 \dots 100\% I_{\text{SB}} \text{ nom}$, $dI_{\text{SB}}/dt = 1\text{A}/\mu\text{s}$, recovery within 1% of $V_1 \text{ nom}$ | -0.6 | 0.6 | V |
| T_{rec} | Recovery Time | | | 0.5 | ms |
| $t_{\text{AC } V_{\text{SB}}}$ | Start-up Time from AC | $V_{\text{SB}} = 90\% V_{\text{SB}} \text{ nom}$ (see <i>Figure 5</i>) | 2.5 | 3 | sec |
| $t_{V_{\text{SB}} \text{ rise}}$ | Rise Time | $V_{\text{SB}} = 10 \dots 90\% V_{\text{SB}} \text{ nom}$ (see <i>Figure 7</i>) | | 30 | ms |
| C_{Load} | Capacitive Loading | $T_{\text{amb}} = 25^\circ\text{C}$ | | 1,000 | μF |

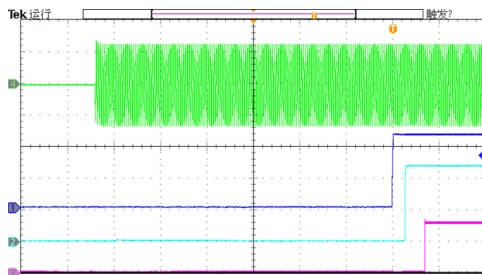


Figure 5. Turn-On AC Line 230VAC, full load (400ms/div)

CH1: V_{SB} (5V/div) CH2: V_1 (5V/div)
CH3: PWOK (2V/div) CH4: V_{in} (250V/div)

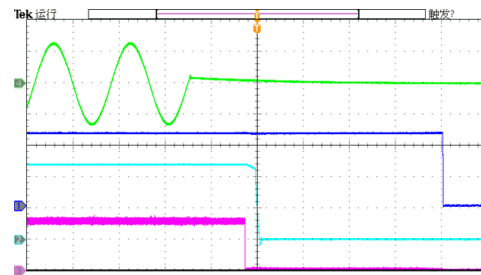


Figure 6. Turn-Off AC Line 230VAC, full load (10ms/div)

CH1: V_{SB} (5V/div) CH2: V_1 (5V/div)
CH3: PWOK (2V/div) CH4: V_{in} (250V/div)

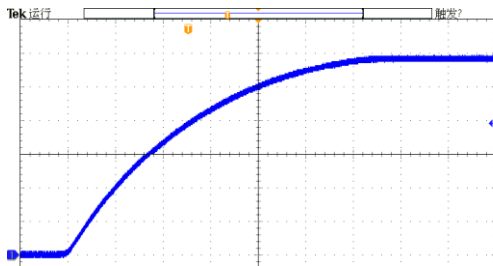


Figure 7. Turn-On AC Line 230VAC, full load (4ms/div)

CH1: V_{SB} (2V/div)

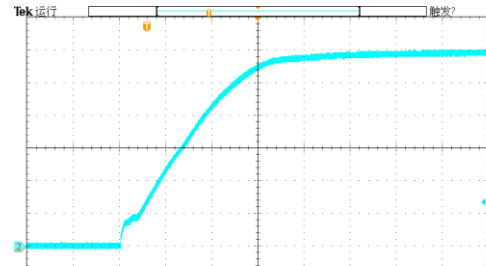


Figure 8. Turn-On AC Line 230VAC, full load (2ms/div)

CH2: V_1 (2V/div)

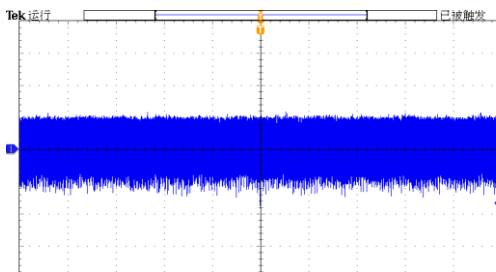


Figure 9. V_{SB} Ripple 230VAC, full load (10ms/div)

CH1: V_{SB} (20mV/div)

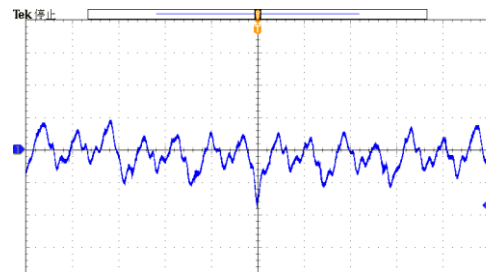


Figure 10. V_{SB} Ripple 230VAC, full load (10us/div)

CH1: V_{SB} (20mV/div)

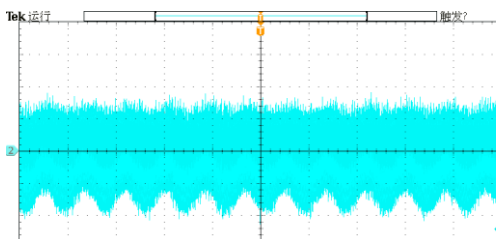


Figure 11. V_1 Ripple 230VAC, full load (10ms/div)

CH2: V_1 (20mV/div)

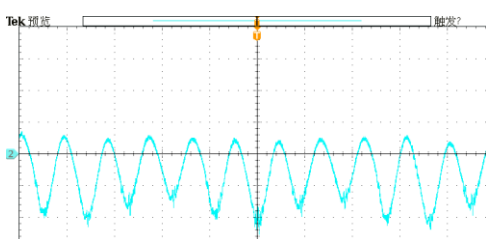


Figure 12. V_1 Ripple 230VAC, full load (2us/div)

CH2: V_1 (20mV/div)

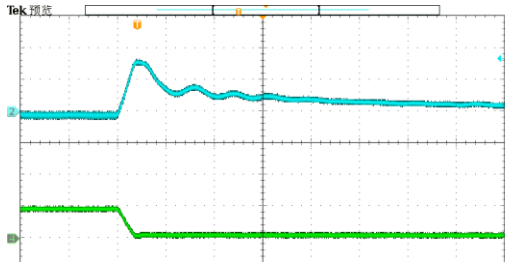


Figure 13. Load Transient V1, 92.95 to 8.45 A, 1A/uS (200 µs/div)
CH2: V_i (200mV/div) CH4: I_i (100A/div)

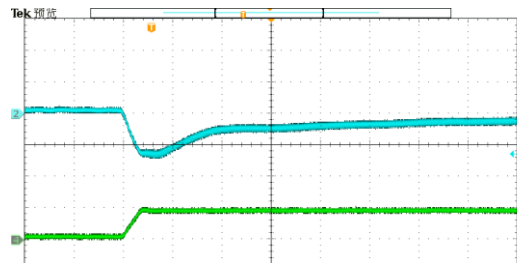


Figure 14. Load Transient V1, 8.45 to 92.95 A, 1A/uS (200 µs/div)
CH2: V_i (200mV/div) CH4: I_i (100A/div)

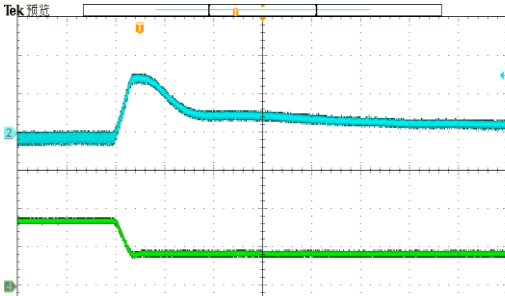


Figure 15. Load Transient V1, 169 to 84.5 A, 1A/uS (200 µs/div)
CH2: V_i (200mV/div) CH4: I_i (100A/div)

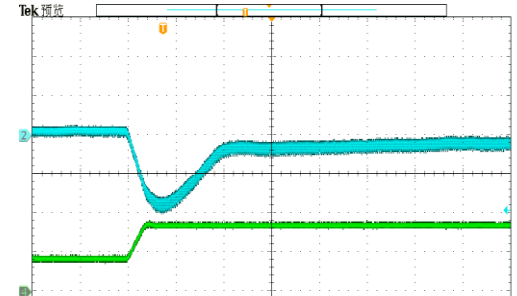


Figure 16. Load Transient V1, 84.5 to 169 A, 1A/uS (200 µs/div)
CH2: V_i (200mV/div) CH4: I_i (100A/div)

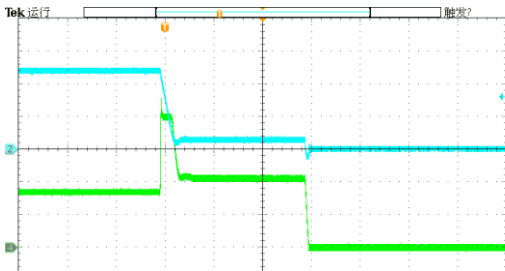


Figure 17. Short circuit on V1 (4ms/Div), Short with 400A
CH2: V_i (5V/div) CH4: I_i (100A/div)

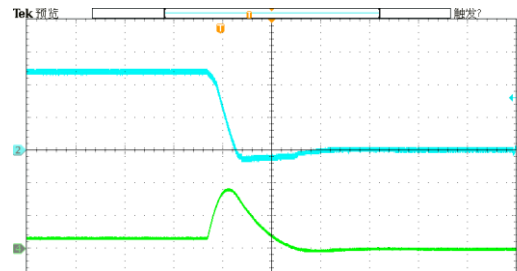


Figure 18. Short circuit on V1 (0.4ms/Div), Short without control
CH2: V_i (5V/div) CH4: I_i (500A/div)

5.1 OUTPUT VOLTAGE RIPPLE

Ripple and noise shall be measured using the following methods:

- Outputs bypassed at the point of measurement with a parallel combination of 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitors, referring the setup in Figure 19.
- The ripple voltage is measured with 20 MHz BWL.

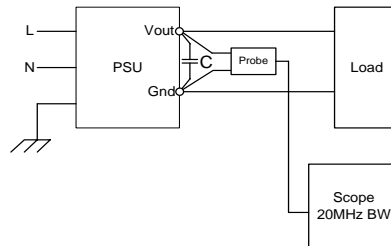


Figure 19. Output Ripple Test Setup

5.2 SHORT TIME OVERLOAD

The main output has the capability to allow load current up to 20% above the nominal output current rating for a maximum duration of 20ms. This allows the system to consume extended power for short time dynamic processes.

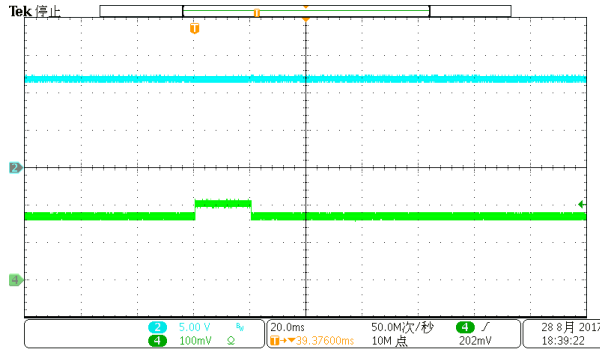


Figure 20. Short circuit on V1 (20ms/Div)
 CH2: V₁ (5V/div) CH4: V_{in} (100A/div)

5.3 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in Figure 21. Alternatively, separated ground signals can be used as shown in Figure 22. In this case the two ground planes should be connected at the power supplies ground pins.

NOTE: Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal on the AC inlet. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

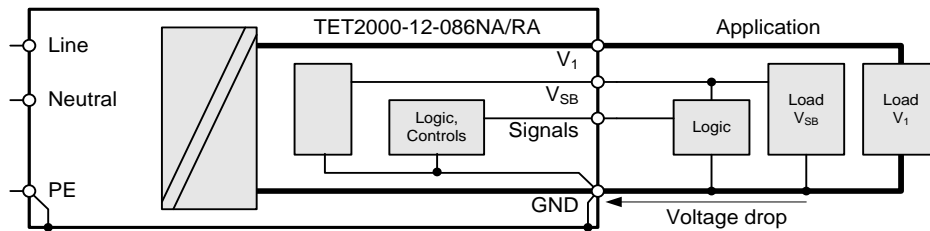


Figure 21. Common Low Impedance Ground Plane

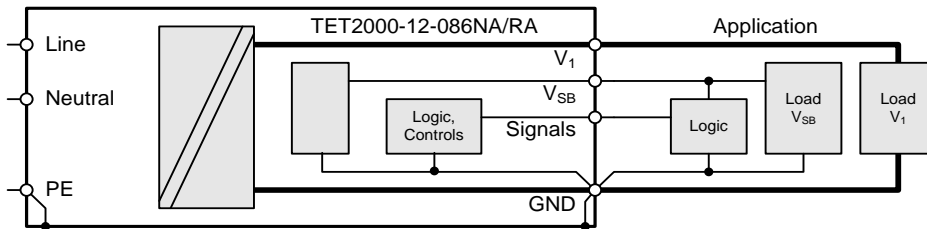


Figure 22. Separated Power and Signal Ground

6. PROTECTION SPECIFICATIONS

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|------------------------|--|--|-------|-------|---------------------|
| F | Input Fuse (Line) | Not user accessible, quick-acting (F) | | | A_{rms} |
| $V_{1\text{OV}}$ | OV Threshold V_1 | 13.3 | 13.9 | 14.5 | VDC |
| $t_{\text{OV } V_1}$ | OV Latch Off Time V_1 | | | | 1 ms |
| $V_{\text{SB OV}}$ | OV Threshold V_{SB} | 13.3 | 13.9 | 14.5 | VDC |
| $t_{\text{OV VSB}}$ | OV Latch Off Time V_{SB} | | | | 1 ms |
| $I_{V_1\text{lim}}$ | Current Limitation V_1 | See Figure 24 and Table 1 | | | A |
| | | $V_1 < 180\text{ VAC}, T_a < 50^\circ\text{C}$ | | | |
| | | $V_1 < 180\text{ VAC}, T_a = 55^\circ\text{C}^{(3)}$ | | | |
| | | $V_1 < 180\text{ VAC}, T_a = 60^\circ\text{C}^{(3)}$ | | | |
| | | $V_1 > 180\text{ VAC}, T_a < 50^\circ\text{C}$ | 177 | 185 | 193 |
| | | $V_1 > 180\text{ VAC}, T_a = 55^\circ\text{C}^{(3)}$ | 160 | 166.5 | 173 |
| | | $V_1 > 180\text{ VAC}, T_a = 60^\circ\text{C}^{(3)}$ | 141.6 | 148 | 154.4 |
| $t_{V_1\text{lim}}$ | Current Limit Blanking Time | Time to latch off when in over current | | | 20 ms |
| $I_{V_1\text{ol lim}}$ | Current Limit During Short Time Overload V_1 | Maximum duration 20 ms | | | 203 A |
| $I_{V_1\text{sc}}$ | Max Short Circuit Current V_1 | $V_1 < 3\text{V}$ | | | 210 ⁴⁾ A |
| $t_{V_1\text{sc off}}$ | Short Circuit Latch Off Time | Time to latch off when in short circuit (Short circuit current < 400 A) See Figure 17 | | | 10 ms |
| | | (Short circuit current > 400 A) See Figure 18 | | | 0.2 ms |
| $I_{\text{SB lim}}$ | Current Limitation V_{SB} | 2.2 | 2.5 | 2.8 | A |
| $t_{\text{SB lim}}$ | Current Limit Blanking Time | Time to hit hiccup when in over current | | | 1 ms |

3) See Figure 24 and Table 1 for linear derating > 50°C

4) Limit set doesn't include effects of main output capacitive discharge.

6.1 OVERVOLTAGE PROTECTION

The TET2000-12-086 Series front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. The standby output will continuously try to restart with a 1 s interval after OV condition has occurred.

6.2 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. PWOK pin signal if the output voltage exceeds $\pm 5\%$ of its nominal voltage.

The main output will latch off if the main output voltage when V_1 falls below 11.2V (typically in an overload condition), the latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

If the standby output leaves its regulation bandwidth for more than 10ms then the main output is disabled to protect the system, and the standby output will continuously try to restart with a 1s interval after UV condition has occurred.

6.3 CURRENT LIMITATION

MAIN OUTPUT

The main output current limitation level $I_{V_1\text{lim}}$ will decrease if the ambient (inlet) temperature increases beyond 50 °C (see Figure 24 and Table 1). Note that the current limitation on V_1 will kick in at a current level approximately 10A-16A higher nominal output current than is shown.

The 2nd protection is a substantially rectangular output characteristic controlled by a software feedback loop. This protects the power supply and system during the 20ms blanking time of the static over current protection. If the output current is rising fast and reaches $I_{V_1\text{ol lim}}$, the supply will immediately reduce its output voltage to prevent the output current from exceeding $I_{V_1\text{ol lim}}$. When the output current is reduced below $I_{V_1\text{ol lim}}$, the output voltage will return to its nominal value.

When the main output over current, the V_1 will shut down and latch off. The latch can be cleared by recycling the input voltage or the PSON_L input. A failure on the Main output will shut down only the Main output, while Standby continues to operate.



Asia-Pacific
+86 755 298 85888

Europe, Middle East
+353 61 225 977

North America
+1 408 785 5200

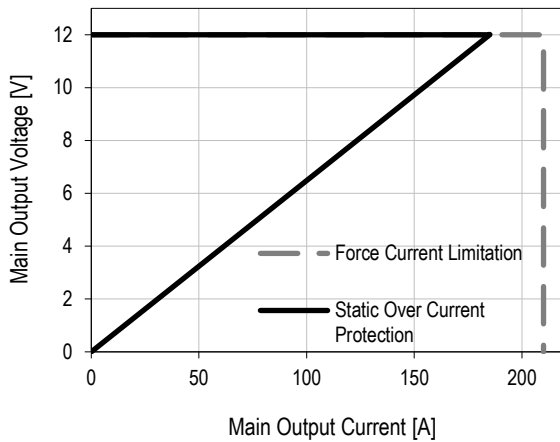


Figure 23. Current Limitation on V_1 ($V_i = 230$ VAC)

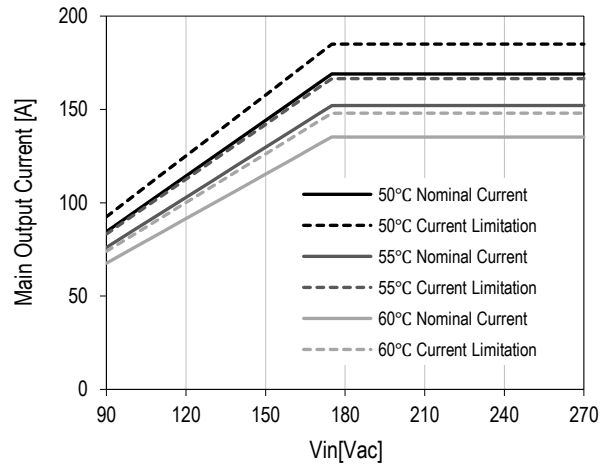


Figure 24. Derating on V_1 vs T_a & V_{in}

| $V_{in}(Vac)$ | $\leq 50^{\circ}C$ $I_{out_Nom}(A)$ | $\leq 50^{\circ}C$ $I_{out_OCP}(A)$ | $55^{\circ}C$ $I_{out_Nom}(A)$ | $55^{\circ}C$ $I_{out_OCP}(A)$ | $60^{\circ}C$ $I_{out_Nom}(A)$ | $60^{\circ}C$ $I_{out_OCP}(A)$ |
|---------------|---|---|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| 90.00 | 84.49 | 92.49 | 76.041 | 83.24 | 67.59 | 73.99 |
| 100.00 | 94.44 | 103.38 | 84.996 | 93.04 | 75.55 | 82.70 |
| 110.00 | 104.38 | 114.26 | 93.942 | 102.83 | 83.50 | 91.41 |
| 120.00 | 114.32 | 125.14 | 102.89 | 112.63 | 91.46 | 100.11 |
| 130.00 | 124.27 | 136.02 | 111.84 | 122.42 | 99.41 | 108.82 |
| 140.00 | 134.20 | 146.90 | 120.79 | 132.21 | 107.37 | 117.52 |
| 150.00 | 144.15 | 157.78 | 129.74 | 142.00 | 115.32 | 126.22 |
| 160.00 | 154.09 | 168.67 | 138.68 | 151.80 | 123.28 | 134.94 |
| 170.00 | 164.04 | 179.55 | 147.63 | 161.6 | 131.23 | 143.64 |
| 180.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 190.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 200.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 210.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 220.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 230.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 240.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 250.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 260.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |
| 270.00 | 169 | 185 | 152.1 | 166.5 | 135.2 | 148 |

Table1. Main Output Nominal Output Current I_{1_nom} & Current Limitation I_{V1_lim} vs Inlet Temperature (degC) & $V_{in}(Vac)$

STANDBY OUTPUT

On the standby output a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds I_{SB_lim} . After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

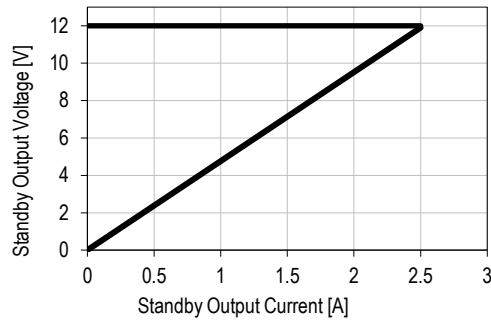


Figure 25. Current Limitation on V_{SB}

7. MONITORING

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---------------------|--|------------|-----|------------|-----------------------|
| V _{I mon} | Input RMS Voltage V _{min} ≤ V ≤ V _{max} | -2.5 | | +2.5 | % |
| I _{I mon} | Input RMS Current I > 6 A _{rms} I ≤ 6 A _{rms} | -5 -0.3 | | +5 +0.3 | % A _{rms} |
| P _{I mon} | True Input Power P > 700 W P ≤ 700 W | -5 -35 | | +5 +35 | % W |
| V _{1 mon} | V ₁ Voltage | -2 | | +2 | % |
| I _{1 mon} | V ₁ Current I ₁ > 30 A I ₁ ≤ 30 A | -2 -1 | | +2 +1 | % A |
| P _{O nom} | Total Output Power P _O > 200 W P _O ≤ 200 W | -5 -10 | | +5 +10 | % W |
| V _{SB mon} | Standby Voltage | -2 | | +2 | % |
| I _{SB mon} | Standby Current I _{SB} ≤ I _{SB nom} | -0.2 | | +0.2 | A |

Table 2. Monitoring accuracy

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS (INPUT SIGNALS)

All Input signals versus signal ground SGND pin of output connector in PSU

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNIT |
|-------------------------------|---|-----------------------------------|-----|------|------|
| <i>PSKILL / PSON_L inputs</i> | | | | | |
| V _L | Input low level voltage | -0.2 | | 0.5 | V |
| V _H | Input high level voltage | 2.0 | | 5.25 | V |
| I _{L, H} | Maximum input sink or source current | V _I = -0.2 V to +3.5 V | | 4 | mA |
| R _{puPSKILL} | Internal pull up resistor to internal 3.3 V on PSKILL | | 10 | | kΩ |
| R _{puPSON_L} | Internal pull up resistor to internal 3.3 V on PSON_L | | 10 | | kΩ |

Table 3. Input signals

8.1.1 PSKILL INPUT

The PSKILL input is an active-high and normally a trailing pin in the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND on the system. The standby output will remain on regardless of the PSKILL input state.



Asia-Pacific
+86 755 298 85888

Europe, Middle East
+353 61 225 977

North America
+1 408 785 5200

8.1.2 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable / disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. Figure 26 shows PSON_L circuit used in PSU and proposed connections.

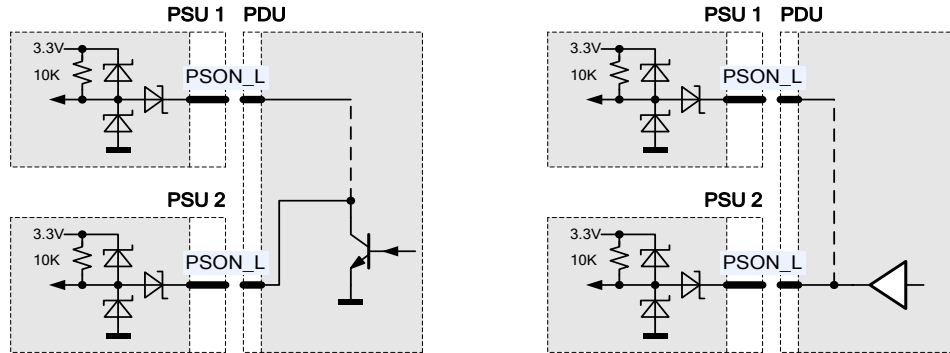


Figure 26. PSON_L Connection

8.1.3 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.2 ELECTRICAL CHARACTERISTICS (OUTPUT SIGNALS)

All Output signals versus signal ground SGND in PSU.

| PARAMETER | DESCRIPTION | | MIN | NOM | MAX | UNIT |
|--------------------------|---|---|-----------|----------------------|------|------------|
| PWOK output | | | | | | |
| V_{OL} | Output low level voltage | V1 or VSB out of regulation $I_{sink}=400\mu A$ | 0 | | 0.4 | V |
| V_{OH} | Output high level voltage | V1 and VSB in regulation $I_{source}=200\mu A$ | 2.4 | | 3.46 | V |
| I_{OL} | Maximum Sink Current | PWOK = low | | | 400 | μA |
| I_{OH} | Maximum Source Current | PWOK = high | | | 2 | mA |
| R_{puPWOK} | Recommended external pull up resistor on PWOK at $V_{puPWOK} = 3.3 V$ $V_{puPWOK} = 5 V$ | | 6.8 10 | 10 15 | | k Ω |
| ACOK output | | | | | | |
| V_{OL} | Output low level voltage | $I_{sink} < 4mA$ | 0 | | 0.4 | V |
| V_{OH} | Output open collector | | | External pull up VDD | | V |
| R_{puACOK} | Recommended external pull up resistor on ACOK at $V_{puACOK} = 3.3V$ | | | 10 | | k Ω |
| <i>Low level output</i> | Input voltage is not within range for PSU to operate | | | | | |
| <i>High level output</i> | Input voltage is within range for PSU to operate | | | | | |

| SMB_ALERT_L output | | | | | |
|---------------------------|---|------------------------------------|----------------------|-----|------------|
| V_{OL} | Output low level voltage | $I_{sink} < 4 \text{ mA}$ | 0 | 0.4 | V |
| V_{OH} | Output open collector | | External pull up VDD | | V |
| $R_{puSMB_ALERT_L}$ | Recommended external pull up resistor on SMB_ALERT_L at $V_{puSMB_ALERT_L} = 3.3\text{V}$ | | 10 | | k Ω |
| <i>Low level output</i> | PSU in warning or failure condition | | | | |
| <i>High level output</i> | PSU is ok | | | | |
| PRESENT_L output | | | | | |
| V_{OL} | Output low level voltage | $I_{sink} < 4 \text{ mA}$ | 0 | 0.4 | V |
| V_{OH} | N.A | This pin is shorted to SGND in PSU | | | V |
| $R_{puPRESENT_L}$ | Recommended external pull up resistor on PRESENT_L at $V_{puPRESENT_L} = 3.3\text{V}$ | | 10 | | k Ω |
| <i>Low level output</i> | PSU is present | | | | |
| <i>High level output</i> | PSU is not present | | | | |

Table 4. Output signals

8.2.1 PWOK

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state.

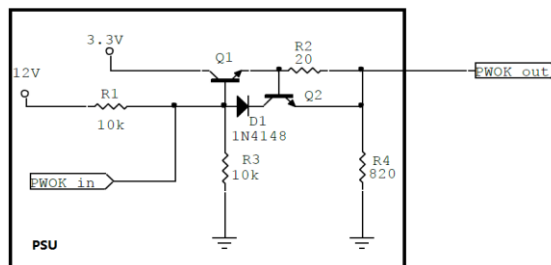


Figure 27. PWOK circuit in PSU

8.2.2 ACOK

The ACOK is an open collector output that requires an external pull-up to a maximum of 12V indicating whether the input is within the range the power supply can use and turn on. A 15V zener diode is added on this signal pin versus signal ground SGND to protect internal circuits from negative and high positive voltage. The ACOK signal is active-high.

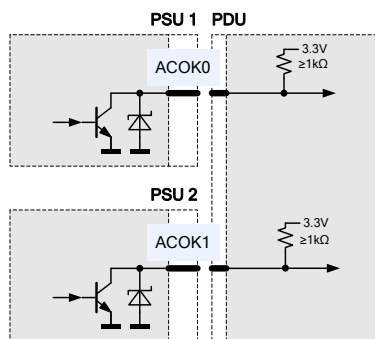


Figure 28. ACOK Connection

8.2.3 SMB_ALERT_L

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Amber.

The power supply shall assert the over temperature SMB_ALERT_L signal when a hot spot or inlet temperature sensor crosses a warning threshold. The inlet temperature warning threshold must be set at 62.5°C, preventing exhaust air and cord temperatures temperature exceeding safety ratings. The warning gets deserted once inlet air temperature returns into specified operating temperature range. Fan speed control algorithm shall ramp up the fan speed to the maximum prior to the SMB_ALERT_L insertion. A 15V zener diode is added on this signal pin versus signal ground SGND to protect internal circuits from negative and high positive voltage.

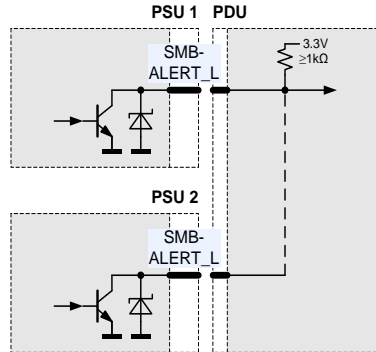


Figure 29. SMB_ALERT_L Connection

8.2.4 PRESENT_L OUTPUT

The PRESENT_L pin is wired to internal SGND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 4 mA to guarantee a low level voltage if power supply is seated.

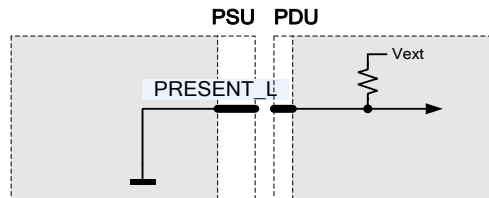


Figure 30. PRESENT_L Signal Pin

8.3 ELECTRICAL CHARACTERISTICS (BIDIRECTIONAL SIGNALS)

8.3.1 CURRENT SHARE

All Output signals versus signal ground SGND in PSU

The TET front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 5% at full load.

ISHARE pins must be interconnected without any additional components. This in-/output has a 15 V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

The 12 VSB output is not required to actively share current between power supplies (passive sharing).

| No of paralleled PSUs | Maximum available power on main 12V without redundancy | Maximum available power on main 12V with n+1 redundancy | Maximum available power on standby output |
|-----------------------|--|---|---|
| 1 | 2000 W | - | 24 W |
| 2 | 3900 W | 2000 W | 24 W |
| 3 | 5800 W | 3900 W | 24 W |
| 4 | 7700 W | 5800 W | 24 W |
| 5 | 9600 W | 7700 W | 24 W |
| 6 | 11500 W | 9600 W | 24 W |

Table 5. Power Available When PSU in Redundant Operation

8.4 FRONT LEDS

The front-end has 1 front LED showing the status of the supply. LED is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the position of the LED see *Table* lists the different LED status.

| OPERATING CONDITION | LED State |
|---|-----------------|
| Output ON and OK | Solid GREEN |
| No AC power to all power supplies | OFF |
| AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power. | OFF |
| AC present / Only 12VSB on (Standby mode) | 1Hz Blink GREEN |
| Power supply warning events where the power supply continues to operate; high temp, high current, slow fan. | 1Hz Blink AMBER |
| Power supply critical event causing a shutdown; eg. OCP, OVP, OTP, Fan Fail | Solid AMBER |
| Power supply in FW upload mode | 2Hz Blink GREEN |

Table 6. LED Status

8.5 SIGNAL TIMING

| OPERATING CONDITION | MIN | MAX | UNIT |
|--|-----|------|------|
| $t_{AC\ VSB}$ AC Line to 90% V_{SB} | | 3 | sec |
| $t_{AC\ V1}$ AC Line to 90% V_1 | | 3 | sec |
| $t_{ACOK\ on1}$ ACOK signal on delay (start-up) | | 1700 | ms |
| $t_{ACOK\ on2}$ ACOK signal on delay (dips) | 0 | 100 | ms |
| $t_{V1\ holdup}$ Effective V_1 holdup time | 10 | 300 | ms |
| $t_{VSB\ holdup}$ Effective V_{SB} holdup time | 40 | 300 | ms |
| $t_{ACOK\ V1}$ ACOK to V_1 holdup | 7 | | ms |
| $t_{ACOK\ VSB}$ ACOK to V_{SB} holdup | 27 | | ms |
| $t_{V1\ off}$ Minimum V_1 off time | 500 | | ms |
| $t_{VSB\ off}$ Minimum V_{SB} off time | 500 | | ms |
| $t_{V1\ dropout}$ Minimum V_1 dropout time | 10 | | ms |
| $t_{VSB\ dropout}$ Minimum V_{SB} dropout time | 40 | | ms |
| $t_{V1\ rise}$ V_1 rise time | | 30 | ms |
| $t_{VSB\ rise}$ V_{SB} rise time | | 30 | ms |
| $t_{PSON_L\ V1on}$ PSON_L to V_1 Delay (on) | 5 | 400 | ms |
| $t_{PSON_L\ V1off}$ PSON_L to V_1 Delay (off) | 0 | 100 | ms |
| $t_{PWOK\ del}$ V_1 to PWOK Delay (on) | 100 | 500 | ms |
| $t_{PWOK\ warn}$ PWOK Delay (off) to V_1 | 1 | | ms |

Table 7. Timing



Asia-Pacific
+86 755 298 85888

Europe, Middle East
+353 61 225 977

North America
+1 408 785 5200

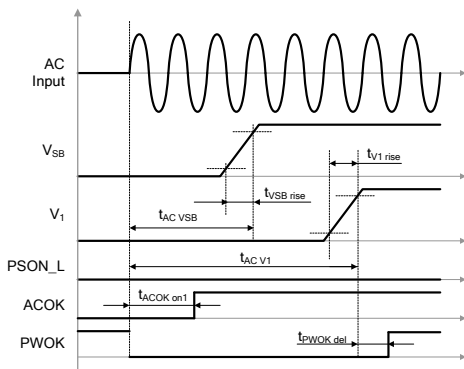


Figure 31. AC Turn-On Timing

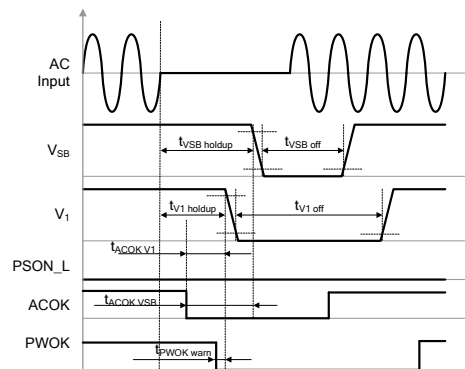


Figure 32. AC Long Dips

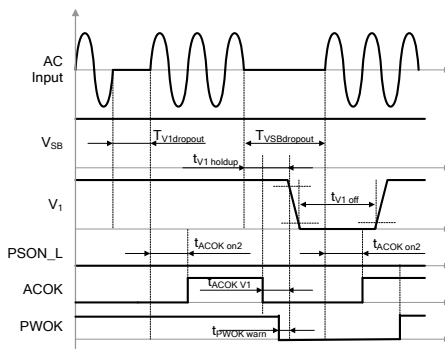


Figure 33. AC Short Dips

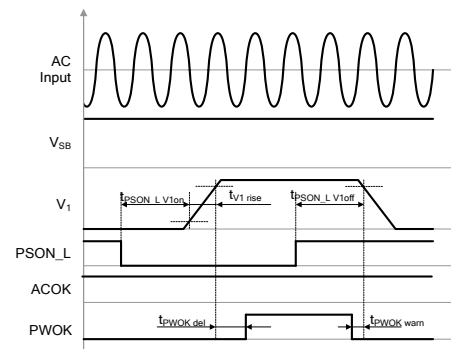


Figure 34. PSON_L Turn-on/off Timing

8.6 I2C / Power Management Bus COMMUNICATION

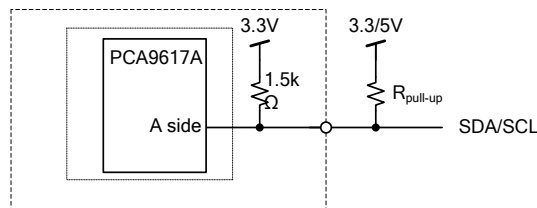


Figure 35. Physical Layer of Communication Interface

The TET front-end is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in *Table 8* further characterized through:

- The SDA/SCL IOs use 3V3 logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 400 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of > 25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible if it is connected to a life 12 V or 12 VSB output (provided e.g. by the redundant unit).

| PARAMETER | DESCRIPTION | CONDITION | MIN | MAX | UNIT |
|----------------------|---------------------------------------|--|-----------------------------------|---------------------------------------|------|
| SCL / SDA | | | | | |
| V _{IL} | Input low voltage | | -0.5 | 1.0 | V |
| V _{IH} | Input high voltage | | 2.3 | 3.5 | V |
| V _{hys} | Input hysteresis | | 0.15 | | V |
| V _{oL} | Output low voltage | 3 mA sink current | 0 | 0.4 | V |
| t _r | Rise time for SDA and SCL | | 20+0.1C _b ¹ | 300 | ns |
| t _{of} | Output fall time ViHmin → ViLmax | 10 pF < C _b ¹ < 400 pF | 20+0.1C _b ¹ | 250 | ns |
| I _i | Input current SCL/SDA | 0.1 VDD < Vi < 0.9 VDD | -10 | 10 | μA |
| C _i | Internal Capacitance for each SCL/SDA | | | 0 | pF |
| f _{SCL} | SCL clock frequency | | 0 | 400 | kHz |
| R _{pull-up} | External pull-up resistor | f _{SCL} ≤ 400 kHz | | 1000 ns / C _b ¹ | Ω |
| t _{HDSTA} | Hold time (repeated) START | f _{SCL} ≤ 400 kHz | 0.6 | | μs |
| t _{LOW} | Low period of the SCL clock | f _{SCL} ≤ 400 kHz | 1.3 | | μs |
| t _{HIGH} | High period of the SCL clock | f _{SCL} ≤ 400 kHz | 0.6 | | μs |
| t _{SUSTA} | Setup time for a repeated START | f _{SCL} ≤ 400 kHz | 0.6 | | μs |
| t _{HDDAT} | Data hold time | f _{SCL} ≤ 400 kHz | 0 | 0.9 | μs |
| t _{SUDAT} | Data setup time | f _{SCL} ≤ 400 kHz | 100 | | ns |
| t _{SUSTO} | Setup time for STOP condition | f _{SCL} ≤ 400 kHz | 0.6 | | μs |
| t _{BUF} | Bus free time between STOP and START | f _{SCL} ≤ 400 kHz | 1 | | ms |

¹ C_b = Capacitance of bus line in pF, typically in the range of 10...400 pF

Table 8. I2C / SMBus Specification

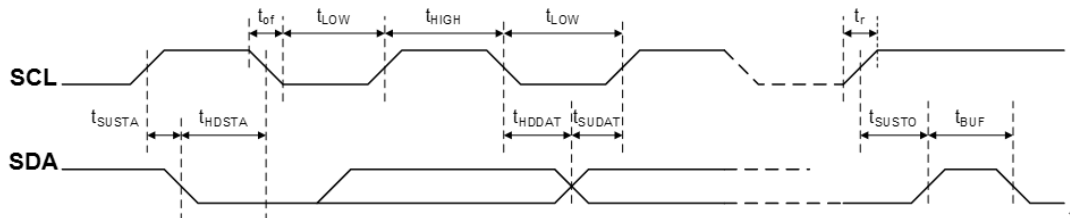


Figure 36. I2C / SMBus Timing

ADDRESS SELECTION

The address for I2C communication can be configured by pulling address input pins A0, A1 and A2 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor (10kohm) will cause the A0, A1 and A2 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

I2C ADDRESS

| A2 | A1 | A0 | I2C Address | |
|----|----|----|------------------------------|----------------|
| | | | Power Management Bus Address | EEPROM Address |
| 0 | 0 | 0 | 0xB0 | 0xA0 |
| 0 | 0 | 1 | 0xB2 | 0xA2 |
| 0 | 1 | 0 | 0xB4 | 0xA4 |
| 0 | 1 | 1 | 0xB6 | 0xA6 |
| 1 | 0 | 0 | 0xB8 | 0xA8 |
| 1 | 0 | 1 | 0xBA | 0xAA |
| 1 | 1 | 0 | 0xBC | 0xAC |
| 1 | 1 | 1 | 0xBE | 0xAE |

Table 9. Address and Protocol Encoding



Asia-Pacific
+86 755 298 85888

Europe, Middle East
+353 61 225 977

North America
+1 408 785 5200

8.7 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see *Figure 37*) and can be accessed under different addresses, see *Table 9 Address and Protocol Encoding*.

The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3V3.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

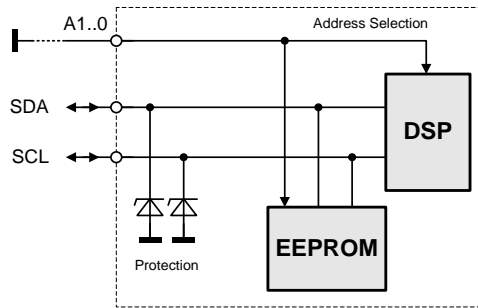


Figure 37. I2C Bus to DSP and EEPROM

8.8 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

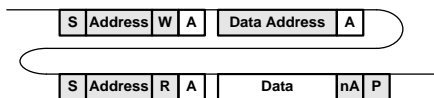
WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 1ms of the last STOP condition to allow the EEPROM to write the data into its memory.



READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



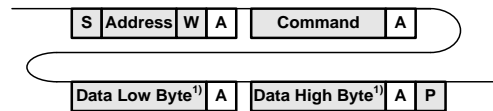
8.9 POWER MANAGEMENT BUS PROTOCOL

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org. Power Management Bus command codes are not register addresses. They describe a specific command to be executed. TET2000-12-086 Series supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

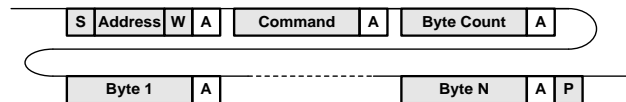
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



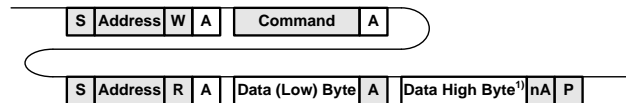
¹⁾ Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See TET2000-12-086 Series Programming Manual for further information.



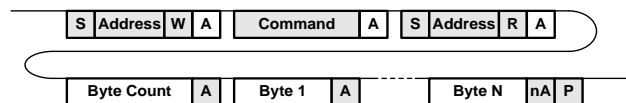
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



¹⁾ Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See TET2000-12-086 Series Power Management Bus Communication Manual URP.00560 for further information.



9. MECHANICAL SPECIFICATIONS

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|------------|-------------------------|-----|-----|-----|------|
| Dimensions | Width | | 86 | | mm |
| | Height | | 40 | | |
| | Depth | | 195 | | |
| M | Weight | | 1.2 | | kg |

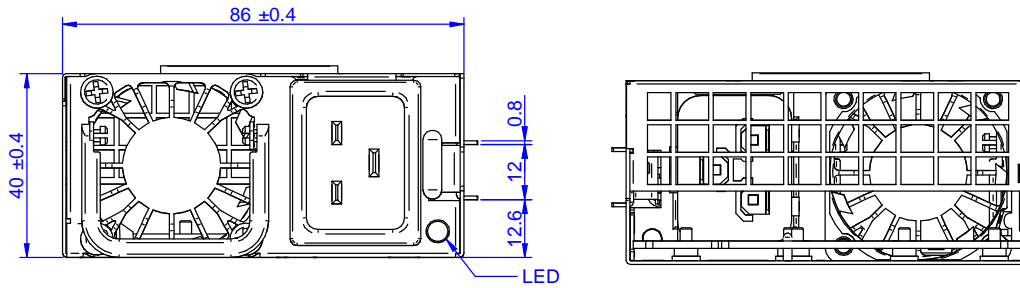


Figure 38. Mechanical Drawing - Front / Rear View

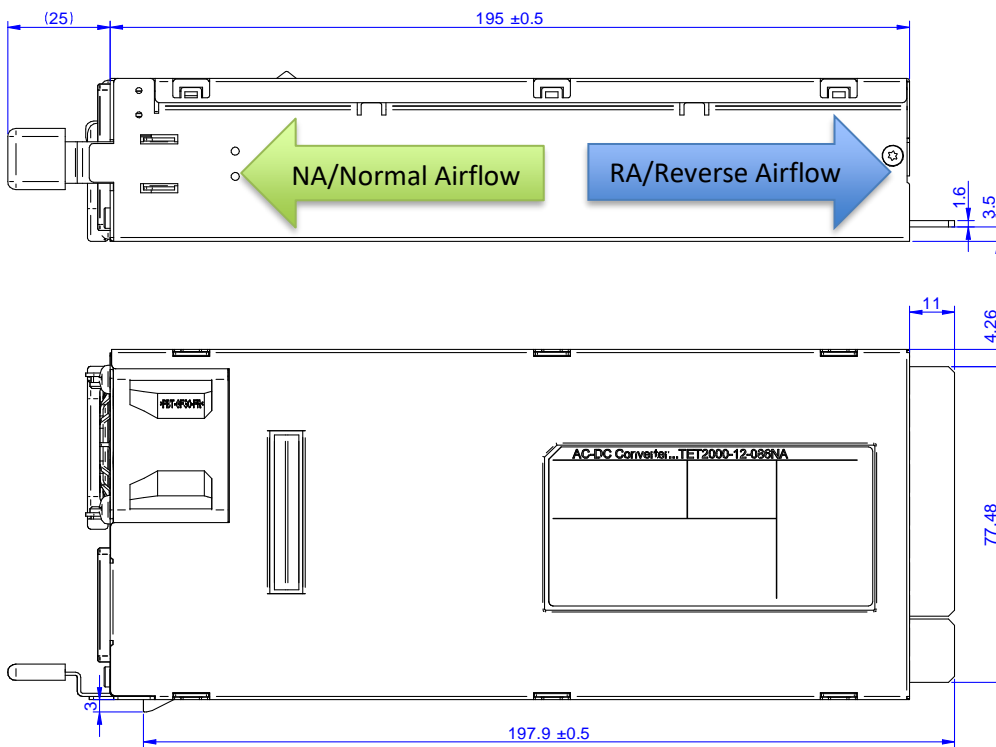


Figure 39. Mechanical Drawing - Side / Top View

NOTE: A 3D step file of the power supply casing is available on request.

10. TEMPERATURE AND FAN CONTROL

10.1 FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The TET2000-12-086NA is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet and TET2000-12-086RA is reversed. The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

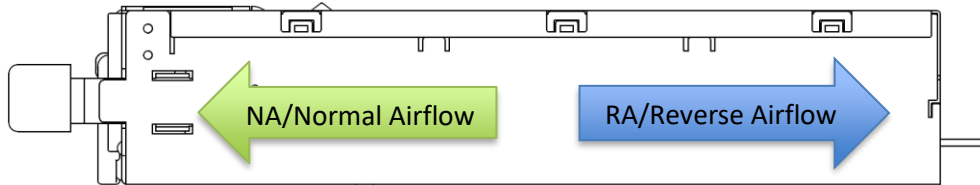


Figure 40. Airflow Direction

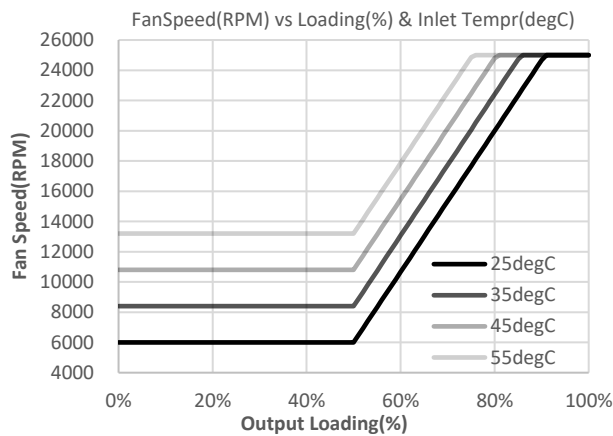


Figure 41. Fan Speed vs. Main Output Load

10.2 TEMPERATURE MONITOR AND OVER TEMPERATURE PROTECTION

The TET2000-12-086 Series provides access via I2C to the measured temperatures of in total 4 sensors within the power supply, see Table 10. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signaled accordingly through LED, PWOK and SMB_ALERT_L.

| TEMPERATURE SENSOR | DESCRIPTION / CONDITION | POWER MANAGEMENT BUS REGISTER | WARNING THRESHOLD | SHUT DOWN THRESHOLD |
|------------------------|---|-------------------------------|----------------------|---------------------|
| Inlet air temperature | Sensor located on control board close to DC end of power supply | 0x8D | NA:62.5C RA:62.5C | NA:65C RA:65C |
| Oring Mosfet | Sensor located close to Oring Mosfet | 0x8E | NA:90C RA:105C | NA:95C RA:110C |
| Outlet air temperature | Sensor located on main board close to AC front of power supply | 0x8F | NA:80C RA:85C | NA:85C RA:90C |
| PFC&DC-DC heat sink | Sensor located on PFC heat sink and DC-DC heatsink | | | NA&RA:130C |

Table 10. NA revision Temperature Sensor Location and Thresholds

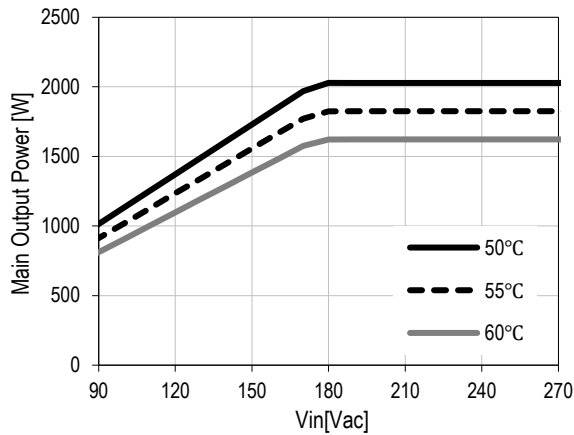


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10.3 TEMPERATURE MONITOR AND OVER TEMPERATURE PROTECTION



| Vin (Vac) | 50°C Pout_Nom (W) | 55°C Pout_Nom (W) | 60°C Pout_Nom (W) |
|-----------|-------------------|-------------------|-------------------|
| 90 | 1039 | 935 | 831 |
| 100 | 1162 | 1045 | 929 |
| 110 | 1284 | 1155 | 1027 |
| 120 | 1406 | 1266 | 1125 |
| 130 | 1529 | 1376 | 1223 |
| 140 | 1651 | 1486 | 1321 |
| 150 | 1773 | 1596 | 1418 |
| 160 | 1895 | 1706 | 1516 |
| 170 | 2018 | 1816 | 1614 |
| 180 | 2079 | 1871 | 1663 |
| 190 | 2079 | 1871 | 1663 |
| 200 | 2079 | 1871 | 1663 |
| 210 | 2079 | 1871 | 1663 |
| 220 | 2079 | 1871 | 1663 |
| 230 | 2079 | 1871 | 1663 |
| 270 | 2079 | 1871 | 1663 |

Figure 42. Output power VS Input voltage and inlet temperature

11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|---------------------------------|--|-------------------------|
| ESD Contact Discharge | IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body) | A |
| ESD Air Discharge | IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces) | A |
| Radiated Electromagnetics Filed | IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 μs Pulse Modulation, 10 kHz...2 GHz | A |
| Burst | IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute | A |
| Surge | IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV | A |
| RF Conducted Immunity | IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 ... 80 MHz | A |
| Voltage Dips and Interruptions | IEC/EN 61000-4-11 1) Vi 230Volts, 80% Load, Dip 100%, Duration 10ms 2) Vi 230Volts, 100% Load, Dip 100%, Duration < 50 ms 3) Vi 230Volts, 100% Load, Dip 100%, Duration > 50 ms | A V1: B; VSB: A B |

Table 11. Immunity

11.2 EMISSION

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|--------------------|---|-----------|
| Conducted Emission | EN55022 / CISPR 22: 0.15 ... 30 MHz, QP and AVG | Class A |
| Radiated Emission | EN55022 / CISPR 22: 30 MHz ... 1 GHz, QP | Class A |
| Harmonic Emissions | IEC61000-3-2, Vin = 230 VAC, 50 Hz, 100% Load | Class A |
| AC Flicker | IEC / EN 61000-3-3, d _{max} < 3.3% | Pass |
| Acoustical Noise | Sound power statistical declaration (ISO 7779) @ 50% load, V _{nom} , T _A = 25°C | 50 dBA |

Table 12. Emission

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62638, and UL 62368. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|--------------------------|---|-----|-----|------------|------|
| Agency Approvals | UL 60950-1 Second Edition | | | | |
| | CAN/CSA-C22.2 No. 60950-1-07 Second Edition | | | | |
| | IEC 60950-1:2005 | | | | |
| | EN 60950-1:2006 | | | | |
| | IEC 62368-1:2014 Second Edition | | | | |
| | EN 62368-1:2014 | | | | |
| Isolation Strength | Input (L/N) to case (PE) | | | Basic | |
| | Input (L/N) to output | | | Reinforced | |
| Creepage / Clearance | Primary (L/N) to protective earth (PE) | 3.0 | | | mm |
| | Primary to secondary | 6.0 | | | |
| Electrical Strength Test | Input to case | 2.1 | | | kVDC |
| | Input to output | 4.3 | | | |

Table 13. Safety/Approvals

13. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as “Handle, knobs, grips, etc. held for short periods of time only”.

In case the exit air temperature requirement cannot be met, the power supply must have a warning label for high touch temperature in compliance with IEC/UL 60950-1 and additionally 85C rated power cords must also be used with this power supply.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|-----------------------------------|---|-----|-----|------|------|
| T_A Ambient Temperature | $V_{I\ min}$ to $V_{I\ max}$, $I_{I\ nom}$, $I_{SB\ nom}$ at 5000 m | 0 | | +40 | °C |
| | $V_{I\ min}$ to $V_{I\ max}$, $I_{I\ nom}$, $I_{SB\ nom}$ at 2000 m | 0 | | +50 | °C |
| $T_{A\ ext}$ Extended Temp. Range | Derated output at 2000 m | +50 | | +60 | °C |
| T_S Storage Temperature | Non-operational | -40 | | +70 | °C |
| Altitude | Operational, above Sea Level (see derating) | - | | 5000 | m |

Table 14. Operation Environmental



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14. CONNECTIONS

The AC input receptacle shall be a 3 pins IEC320 C20 inlet.

For the pin assignment of DC connector, please refer to *Figure 43* and *Table 15*.

The Mating connector should be FCI 10121510-480020ALF.

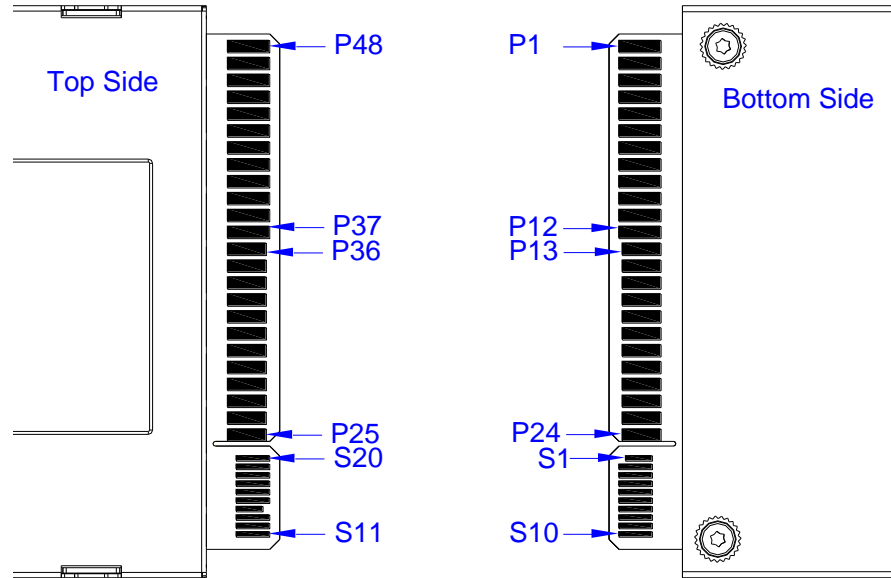


Figure 43. Pin Assignment of DC Connector

| PIN | NAME | DESCRIPTION |
|----------------|-------------|---|
| P13-24, P25-36 | V1 | +12 VDC main output |
| P1-12, P37-48 | PGND | +12 VDC main output ground |
| S1 | PSKILL | Power supply kill (trailing pin) ⁵⁾ : active-high |
| S2 | ACOK | AC input OK signal: active-high |
| S3 | SDA | I ² C DATA I ² C data signal line |
| S4 | SCL | I ² C CLOCK I ² C clock signal line |
| S5 | ISHARE | 12 V Load Share V ₁ Current share bus |
| S6 | A0 | I ² C Address I ² C address selection input |
| S7 | A1 | I ² C Address I ² C address selection input |
| S8 | PWOK | Power OK signal output: active-high |
| S9 | A2 | I ² C address selection input |
| S10 | EEPROM_WP | EEPROM write protect |
| S11 | SGND | Signal ground ⁶⁾ (return) |
| S12 | PSON_L | Power supply on input: active-low |
| S13 | SMB_ALERT_L | SMB Alert signal output: active-low |
| S14 | PRESENT_L | Power supply present (trailing pin): active-low |
| S15-16 | VSB_GND | Standby Ground ⁵⁾ |
| S17-18 | VSB | Standby positive output |
| S19 | V1_SENSE- | Main output negative sense |
| S20 | V1_SENSE+ | Main output positive sense |



⁵⁾ This pin should be connected to SGND on the system

⁶⁾ This pin should be connected to PGND on the system

All signal pins are referred to SGND

Table 15. Connector pin assignment

15. ACCESSORIES

| ITEM | DESCRIPTION | ORDERING PART NUMBER | SOURCE |
|---|---|----------------------|--|
|  | I²C Utility Windows XP/Vista/7 compatible GUI to program, control and monitor TET2000-12-086NA/RA Front-Ends (and other I ² C units) | N/A | befuse.com/lpower-solutions |
|  | Single Connector Board Connector board to operate TET2000-12-086NA/RA unit. Includes an on-board USB to I ² C converter (use <i>I²C Utility</i> as desktop software). | YTM.G1Z01.0 | befuse.com/lpower-solutions |

16. REVISION HISTORY

| REVISION | DESCRIPTION OF CHANGES | DATE | ORIGINATOR |
|----------|--|------------|-----------------------|
| AA | Initial release | 2018-02-27 | Jun.li |
| AA1 | 1) Disclaimer on the first page (PMBus is a registered trademark of SMIF, Inc.): was removed 2) PMBus needs to be fully spelled out every time it is used: Power Management Bus 3) No trademark symbols used with Power Management Bus | 2019-03-29 | Stefancova, Vladimira |
| AB | 1) Change the Max Input Current to 13.5A from 12A in section4 page3 2) Remove HVDC Input efficiency in Figure 4 page 4 3) Correct max power typo in section10.3 page22 4) <i>Change $t_{1\text{ off}}$ and $t_{\text{VSB off}}$ from 1000ms to 500ms min in section8.5 page15</i> 5) Add ACCESSORIES information in section15 page 25 6) Change Electrical Strength Test Input to case voltage from 2.8 to 2.1 kVDC in section12 page23 | 2019-06-18 | Jun.li |

For more information on these products consult: tech.support@psbel.com

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