

MAX13450E/MAX13451E

General Description

The MAX13450E/MAX13451E are half-duplex and full-duplex RS-485/RS-422 transceivers. These devices feature internal 100Ω and 120Ω termination resistors. The resistor values are pin selectable. A logic supply input allows interfacing to logic levels down to +1.8V.

The MAX13450E/MAX13451E feature strong drivers specified to drive low-impedance lines found when a fully loaded bus, based on today's 100Ω characteristic impedance cable, is doubly terminated. Both devices allow slew-rate limiting of the driver output to reduce EMI and reflections for data rates up to 500kbps.

The MAX13451E has a FAULT alarm indication output to signal to the system that an error condition exists in the driver. The MAX13451E also features a logic inversion function. The logic inversion allows phase reversal of the A-B signals in case these are inadvertently connected wrongly.

The MAX13450E/MAX13451E have 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. All driver outputs are protected to ±30kV ESD using the Human Body Model (HBM).

The MAX13450E/MAX13451E are available in a 14-pin TSSOP package and operate over the automotive -40°C to +125°C temperature range.

Applications

- Industrial Control Systems
- Portable Industrial Equipment
- Motor Control
- Security Networks
- Medical Networks

Ordering Information/Selector Guide

| PART | HALF/FULL DUPLEX | PIN-PACKAGE |
|---------------|------------------|--------------|
| MAX13450EAUD+ | Full | 14 TSSOP-EP* |
| MAX13451EAUD+ | Half | 14 TSSOP-EP* |

Note: All devices are specified over the -40°C to +125°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

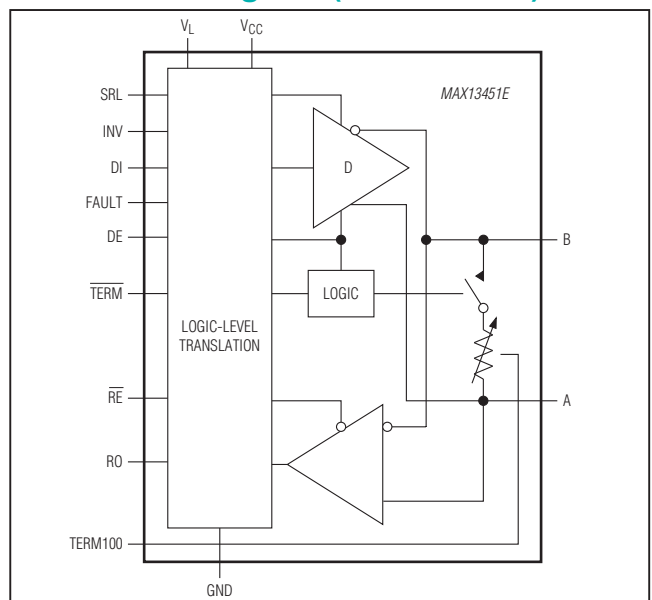
*EP = Exposed pad.

RS-485 Transceivers with Integrated 100Ω/120Ω Termination Resistors

Benefits and Features

- Easy Configuration of RS-422 and RS-485 Networks Up to 20Mbps (max) Data Rate
- Software/Pin-Selectable 100Ω/120Ω Termination
- Integrated, Switchable Resistors Eliminate the Need for External Resistors or DIP Switches
- Driver Drives 100Ω Double Termination and Supports Cat-5/Cat-6 and 24-AWG Cables
- Pin-Selectable Slew-Rate Limiting Reduces EMI for Data Rates Up to 500kbps
- 1/8 Unit Load Allows Up to 256 Transceivers On the Bus
- Designed to Perform in Harsh Environments
 - Extended ESD Protection
 - ±30kV Human Body Model
 - ±15kV Air Gap Discharge per IEC 61000-4-2
 - ±7kV Contact Discharge per IEC 61000-4-2
 - Inverting of A, B Line Polarity (MAX13451E) Allows Phase Reversal if Misconnected
 - Thermal and Overcurrent Protection
 - Driver Fault Indication (MAX13451E)
 - Fail-Safe Receivers
 - -40°C to +125°C Temperature Range
 - +4.5V to +5.5V Supply Voltage Range
- Integrated Low-Voltage Logic Interface (Down to 1.8V) Interfaces with Small-Geometry ASICs and FPGA

Functional Diagram (MAX13451E)



Absolute Maximum Ratings

(All voltages referenced to GND.)

| | |
|--|----------------------------------|
| V _{CC} , V _L | -0.3V to +6V |
| DE, \overline{RE} , DI, RO, \overline{TERM} , TERM100, SRL | -0.3V to (V _L + 0.3V) |
| INV, FAULT | -0.3V to (V _L + 0.3V) |
| A, B, Z, Y | -8V to +13V |
| A to B (High-Z State) | +14V |
| B to A (High-Z State) | +14V |
| Short-Circuit Duration (RO, Y, Z) to GND | Continuous |

Continuous Power Dissipation (T_A = +70°C)

| | |
|---|-----------------|
| TSSOP (derate 25.6mW/°C above +70°C)..... | 2051mW |
| Operating Temperature Range | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Soldering Temperature (reflow) | +260°C |

Package Thermal Characteristics (Note 1)

TSSOP

| | |
|---|--------|
| Junction-to-Ambient Thermal Resistance (θ _{JA}) | 39°C/W |
| Junction-to-Case Thermal Resistance (θ _{JC}) | 3°C/W |

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +4.5V to +5.5V, V_L = +1.62V to V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +1.8V, and T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|------|--------------------|-----------------|-------|
| Supply Voltage | V _{CC} | | 4.5 | | 5.5 | V |
| Logic Supply Voltage | V _L | | 1.62 | 1.8 | V _{CC} | V |
| Supply Current | I _{CC} | DE = \overline{RE} = high, \overline{TERM} = high, no load | | | 6 | mA |
| | | DE = \overline{RE} = low, \overline{TERM} = low, no load | | | 12 | |
| Logic Supply Current | I _L | Current into V _L , no load on RO, device not switching, DE = \overline{RE} = high | | | 2 | μA |
| Shutdown Current | I _{SHDN} | Current into V _{CC} , DE = low, \overline{RE} = \overline{TERM} = high | | | 30 | μA |
| | | Current into V _{CC} , DE = low, \overline{RE} = high, \overline{TERM} = low | | | 8 | mA |
| DRIVER | | | | | | |
| Differential Driver Output | V _{OD} | R _{DIFF} = 100Ω, Figure 1 (Note 3) | 2.0 | | V _{CC} | V |
| | | R _{DIFF} = 46Ω, Figure 1 (Note 3) | 1.5 | | V _{CC} | |
| Change in Magnitude of Differential Output Voltage | ΔV _{OD} | R _{DIFF} = 100Ω or 46Ω, Figure 1 (Note 3) | | | 0.2 | V |
| Driver Common-Mode Output Voltage | V _{OC} | R _{DIFF} = 100Ω or 46Ω, Figure 1 (Note 3) | | V _{CC} /2 | 3 | V |
| Change In Magnitude of Common-Mode Voltage | ΔV _{OC} | R _{DIFF} = 100Ω or 46Ω, Figure 1 (Note 3) | | | 0.2 | V |
| Driver Short-Circuit Output Current | I _{OSD} | 0V ≤ V _{OUT} ≤ +12V | | | +280 | mA |
| | | -7V ≤ V _{OUT} ≤ 0V | -250 | | | |

Electrical Characteristics (continued)

($V_{CC} = +4.5V$ to $+5.5V$, $V_L = +1.62V$ to V_{CC} , $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$, $V_L = +1.8V$, and $T_A = +25^{\circ}C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|--|-----------------------|-------|------------------|---------|
| Driver Short-Circuit Foldback Output Current | I_{OSDF} | $(V_{CC} - 1V) \leq V_{OUT} \leq +12V$ | +15 | | | mA |
| | | $-7V \leq V_{OUT} \leq 0V$ | | | -15 | |
| RECEIVER | | | | | | |
| Input Current (A and B) | $I_{A, B}$ | DE = \overline{RE} = GND; $\overline{TERM} = V_L$; $V_{CC} = GND$ or 5.5V | V_A or $V_B = +12V$ | | 125 | μA |
| | | | V_A or $V_B = -7V$ | -100 | | |
| Receiver Differential Threshold Voltage | V_{TH} | $-7V \leq V_{CM} \leq +12V$, DE = \overline{RE} = GND; $\overline{TERM} = V_L$; $V_{CC} = GND$ | V_A or $V_B = +12V$ | -200 | -50 | mV |
| Receiver Input Hysteresis | ΔV_{TH} | $V_A + V_B = 0V$ | | 15 | | mV |
| LOGIC INTERFACE | | | | | | |
| Input High Voltage | V_{IH} | DI, DE, \overline{RE} , \overline{TERM} , SRL, TERM100, INV | $2/3 \times V_L$ | | | V |
| Input Low Voltage | V_{IL} | DI, DE, \overline{RE} , \overline{TERM} , SRL, TERM100, INV | | | $1/3 \times V_L$ | V |
| Input Current | I_{IN} | DI, DE, \overline{RE} , \overline{TERM} , TERM100, SRL, INV | -1 | | +1 | μA |
| Receiver Output High Voltage | V_{ROH} | $I_{OUT} = -1mA$ | $V_L - 0.6$ | | | V |
| Receiver Output Low Voltage | V_{ROL} | $I_{OUT} = +1mA$ | | | 0.4 | V |
| Three-State Output Current at Receiver | I_{OZR} | $0V \leq V_{RO} \leq V_L$ | -1 | +0.01 | +1 | μA |
| Receiver Output Short-Circuit Current | I_{OSR} | $0V \leq V_{RO} \leq V_L$ | ± 1 | | ± 80 | mA |
| Fault Output High Voltage (MAX13451E) | V_{FAULTH} | Fault condition, $I_{OUT} = -1mA$ | $V_L - 0.6$ | | | V |
| Fault Output Low Voltage (MAX13451E) | V_{FAULTL} | Nonfault condition; $I_{OUT} = +1mA$ | | | 0.4 | V |
| TERMINATION RESISTOR | | | | | | |
| 100Ω Termination Resistor | R_{100} | $\overline{TERM} = \text{low}$, TERM100 = high | 85 | 100 | 115 | Ω |
| 120Ω Termination Resistor | R_{120} | $\overline{TERM} = \text{low}$, TERM100 = low | 101 | 120 | 139 | Ω |
| Single-Ended Input Capacitance vs. GND | C_{IN} | $f = 1MHz$ (MAX13451E only) | | 40 | | pF |
| ESD PROTECTION | | | | | | |
| ESD Protection (A, B, Y, Z) | | Human Body Model | | | ± 30 | kV |
| | | IEC 61000-4-2 Air Gap Discharge | | | ± 15 | |
| | | IEC 61000-4-2 Contact Discharge | | | ± 7 | |
| ESD Protection (All Other Pins) | | Human Body Model | | | ± 2 | |

Switching Characteristics—SRL = HIGH

(V_{CC} = +4.5V to +5.5V, V_L = +1.62V to V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +1.8V and T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------------------------|---|-----|-----|------|-------|
| DRIVER | | | | | | |
| Driver Propagation Delay | t _{DPLH} | R _{DIFF} = 54Ω, C _L = 50pF, Figures 2 and 3 | | | 800 | ns |
| | t _{DPHL} | | | | 800 | |
| Differential Driver Output Skew t _{DPLH} - t _{DPHL} | t _{DSKEW} | R _{DIFF} = 54Ω, C _L = 50pF, Figure 3 | | | 100 | ns |
| Driver Differential Output Rise or Fall Time | t _{HL} | R _{DIFF} = 54Ω, C _L = 50pF, Figures 2 and 3 | 100 | | 600 | ns |
| | t _{LH} | | 100 | | 600 | |
| Maximum Data Rate | DR _{MAX} | | 500 | | | kbps |
| Driver Enable from Shutdown to Output High | t _{DZH(SHDN)} | S2 closed, R _L = 500Ω, C _L = 100pF, Figures 4 and 5 | | | 4500 | ns |
| Driver Enable from Shutdown to Output Low | t _{DZL(SHDN)} | S1 closed, R _L = 500Ω, C _L = 100pF, Figures 4 and 5 | | | 5200 | ns |
| Driver Disable Delay | t _{DLZ} , t _{DHZ} | Figures 4 and 5 | | | 100 | ns |
| Driver Enable Delay | t _{DZL} , t _{DZH} | Figures 4 and 5 | | | 2500 | ns |
| RECEIVER | | | | | | |
| Receiver Propagation Delay | t _{RPLH} | C _L = 15pF, V _{ID} ≥ 2.0V; t _{LH} , t _{HL} ≤ 15ns, Figures 6 and 7 | | | 200 | ns |
| | t _{RPHL} | | | | 200 | |
| Receiver Output Skew | t _{RSKEW} | C _L = 15pF, Figures 6 and 7 | | | 30 | ns |
| Maximum Data Rate | DR _{MAX} | | 500 | | | kbps |
| Receiver Enable to Output High | t _{RZH} | S2 closed, C _L = 100pF, R _L = 500Ω, Figures 8 and 9 | | | 50 | ns |
| Receiver Enable to Output Low | t _{RZL} | S1 closed, C _L = 100pF, R _L = 500Ω, Figures 8 and 9 | | | 50 | ns |
| Receiver Disable from High | t _{RHZ} | Figures 8 and 9 | | | 50 | ns |
| Receiver Disable from Low | t _{RLZ} | Figures 8 and 9 | | | 50 | ns |
| Receiver Enable from Shutdown to Output High | t _{RZH(SHDN)} | Figures 8 and 9 | | | 5000 | ns |
| Receiver Enable from Shutdown to Output Low | t _{RZL(SHDN)} | Figures 8 and 9 | | | 5000 | ns |
| TERMINATION RESISTOR | | | | | | |
| Turn-Off Time | t _{RTZ} | Figure 10 | | 120 | | μs |
| Turn-On Time | t _{RTEN} | Figure 10 | | 1 | | μs |

Switching Characteristics—SRL = LOW

($V_{CC} = +4.5V$ to $+5.5V$, $V_L = +1.62V$ to V_{CC} , $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$, $V_L = +1.8V$, and $T_A = +25^{\circ}C$.) (Note 2)

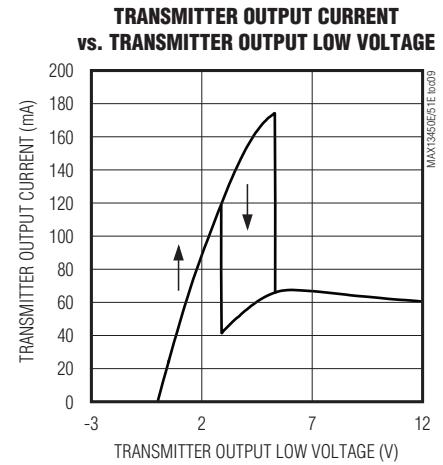
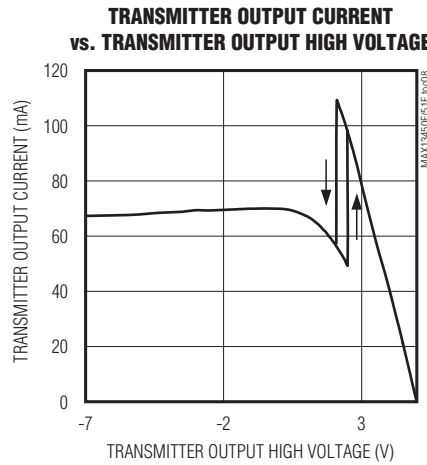
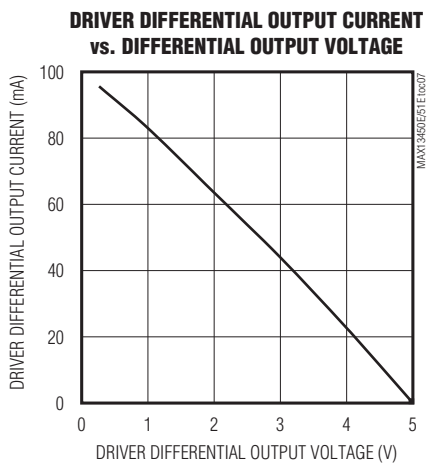
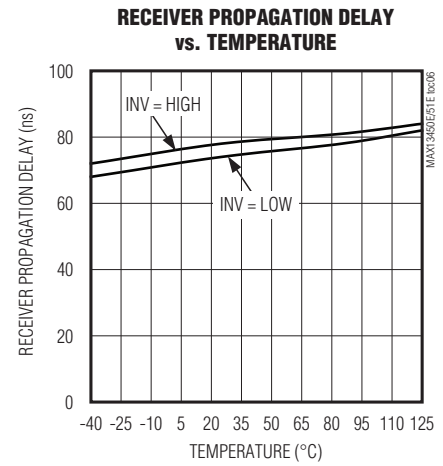
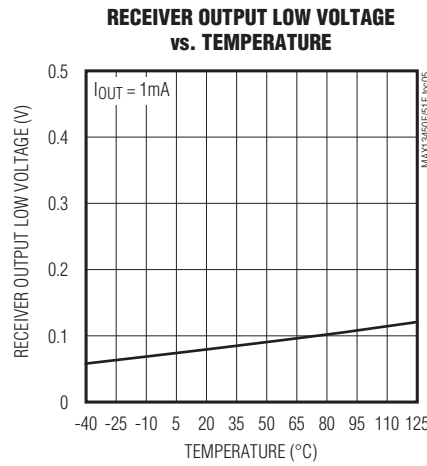
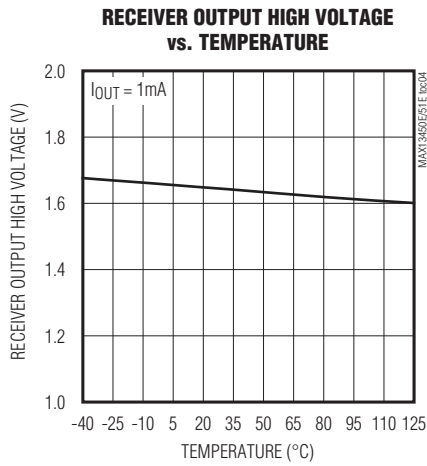
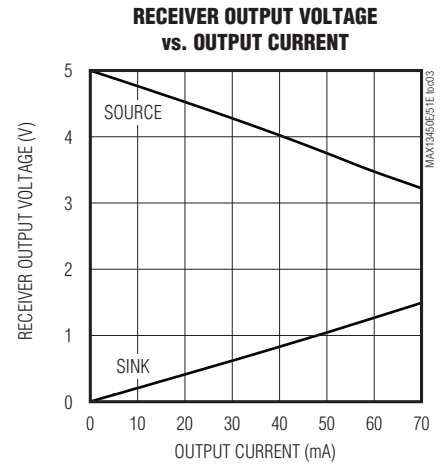
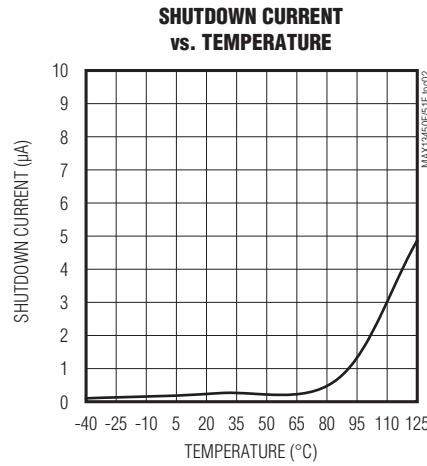
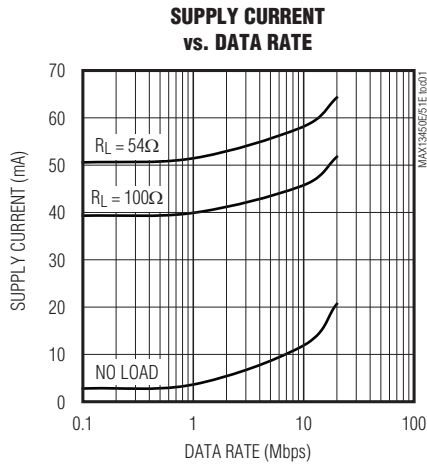
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------------------------|--|-----|-----|------|-------|
| DRIVER | | | | | | |
| Driver Propagation Delay | t _{DPLH} | R _{DIFF} = 54Ω, C _L = 50pF, Figures 2 and 3 | | | 50 | ns |
| | t _{DPHL} | | | | 50 | |
| Differential Driver Output Skew t _{DPLH} - t _{DPHL} | t _{DSKEW} | R _{DIFF} = 54Ω, C _L = 50pF, Figure 3 | | | 6 | ns |
| Driver Differential Output Rise or Fall Time | t _{HL} , t _{LH} | R _{DIFF} = 54Ω, C _L = 50pF, Figures 2 and 3 | | | 15 | ns |
| Maximum Data Rate | DR _{MAX} | | 20 | | | Mbps |
| Driver Enable from Shutdown to Output High | t _{DZH} (SHDN) | S2 closed, R _L = 500Ω, C _L = 100pF, Figures 4 and 5 | | | 2000 | ns |
| Driver Enable from Shutdown to Output Low | t _{DZL} (SHDN) | S1 closed, R _L = 500Ω, C _L = 100pF, Figures 4 and 5 | | | 2000 | ns |
| Driver Disable Delay | t _{DLZ} , t _{DHZ} | Figures 4 and 5 | | | 100 | ns |
| Driver Enable Delay | t _{DZL} , t _{DZH} | Figures 4 and 5 | | | 100 | ns |
| RECEIVER | | | | | | |
| Receiver Propagation Delay | t _{RPLH} | C _L = 15pF, V _{IDI} ≥ 2.0V; t _{LH} , t _{HL} ≤ 15ns, Figures 6 and 7 | | | 50 | ns |
| | t _{RPHL} | | | | 50 | |
| Receiver Output Skew | t _{RSKEW} | C _L = 15pF, Figures 6 and 7 | | | 6 | ns |
| Maximum Data Rate | DR _{MAX} | | 20 | | | Mbps |
| Receiver Enable to Output High | t _{RZH} | S2 closed, C _L = 100pF, R _L = 500Ω, Figures 8 and 9 | | | 50 | ns |
| Receiver Enable to Output Low | t _{RZL} | S1 closed, C _L = 100pF, R _L = 500Ω, Figures 8 and 9 | | | 50 | ns |
| Receiver Disable Time from High | t _{RHZ} | Figures 8 and 9 | | | 50 | ns |
| Receiver Disable Time from Low | t _{RLZ} | Figures 8 and 9 | | | 50 | ns |
| Receiver Enable from Shutdown to Output High | t _{RZH} (SHDN) | Figures 8 and 9 | | | 2000 | ns |
| Receiver Enable from Shutdown to Output Low | t _{RZL} (SHDN) | Figures 8 and 9 | | | 2000 | ns |
| TERMINATION RESISTOR | | | | | | |
| Turn-Off Time | t _{RTZ} | Figure 10 | | 120 | | μs |
| Turn-On Time | t _{RTEN} | Figure 10 | | 1 | | μs |

Note 2: All devices are 100% production tested at $T_A = +25^{\circ}C$. Limits over temperature are guaranteed by design.

Note 3: Termination resistance is disabled ($\overline{TERM} = \text{high}$).

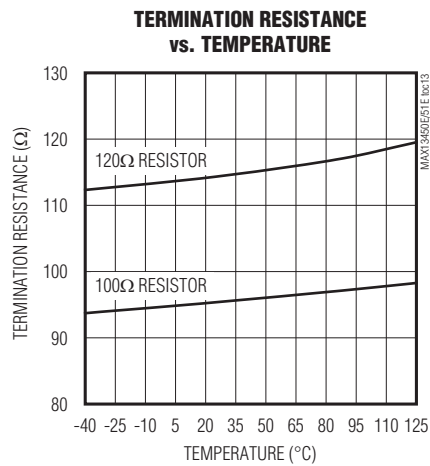
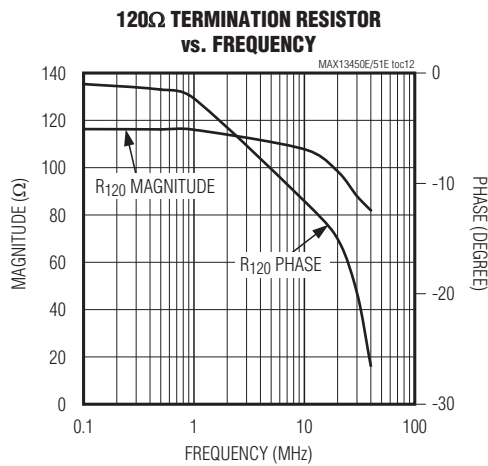
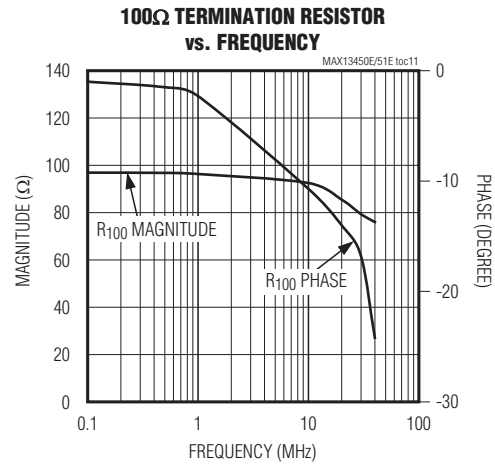
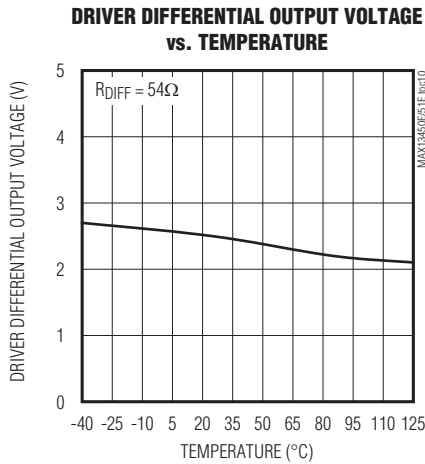
Typical Operating Characteristics

(VCC = +5V, VL = +1.8V, TA = +25°C, unless otherwise noted.)

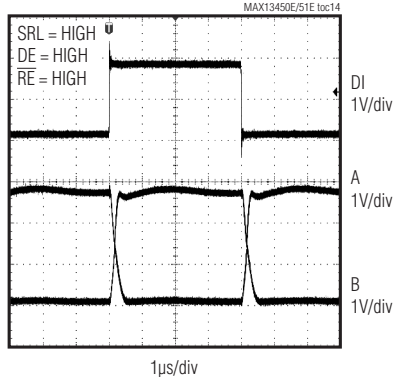


Typical Operating Characteristics (continued)

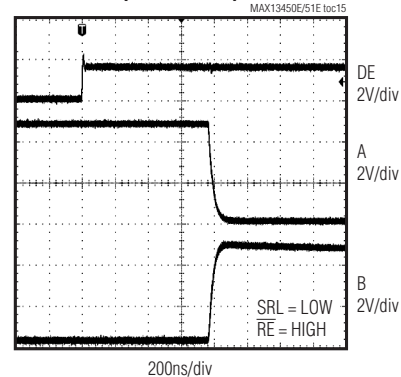
(VCC = +5V, VL = +1.8V, TA = +25°C, unless otherwise noted.)



DRIVER PROPAGATION DELAY (250kbps) (MAX13451E)



DRIVER ENABLE TIME FROM SHUTDOWN (MAX13451E)



Test Circuits and Waveforms

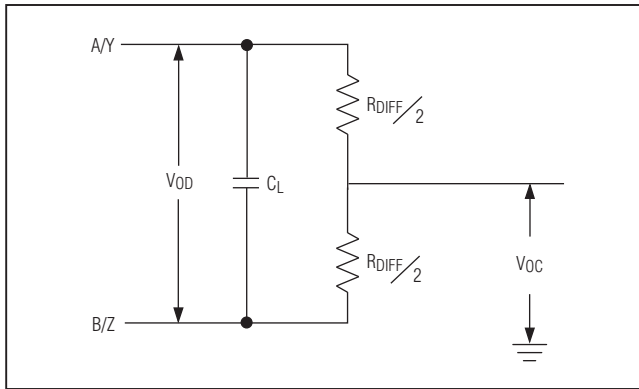


Figure 1. Driver DC Test Load

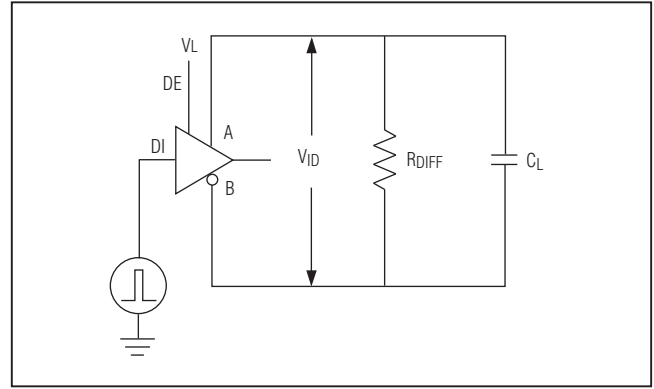


Figure 2. Driver Timing Test Circuit

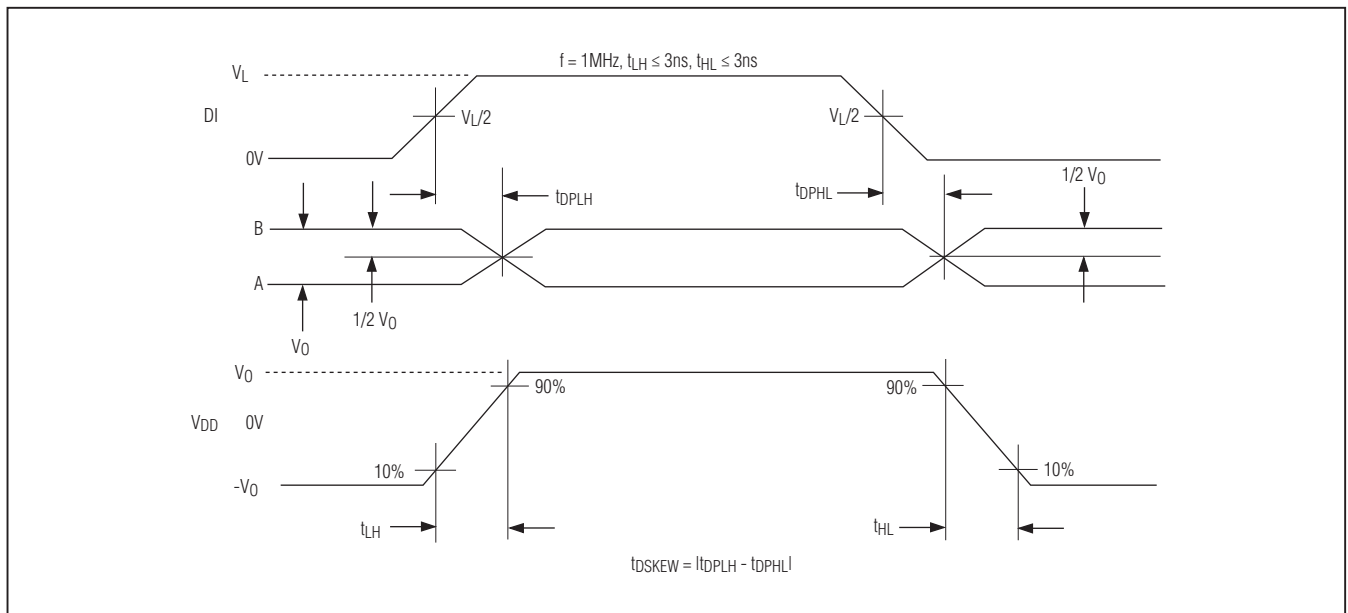


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

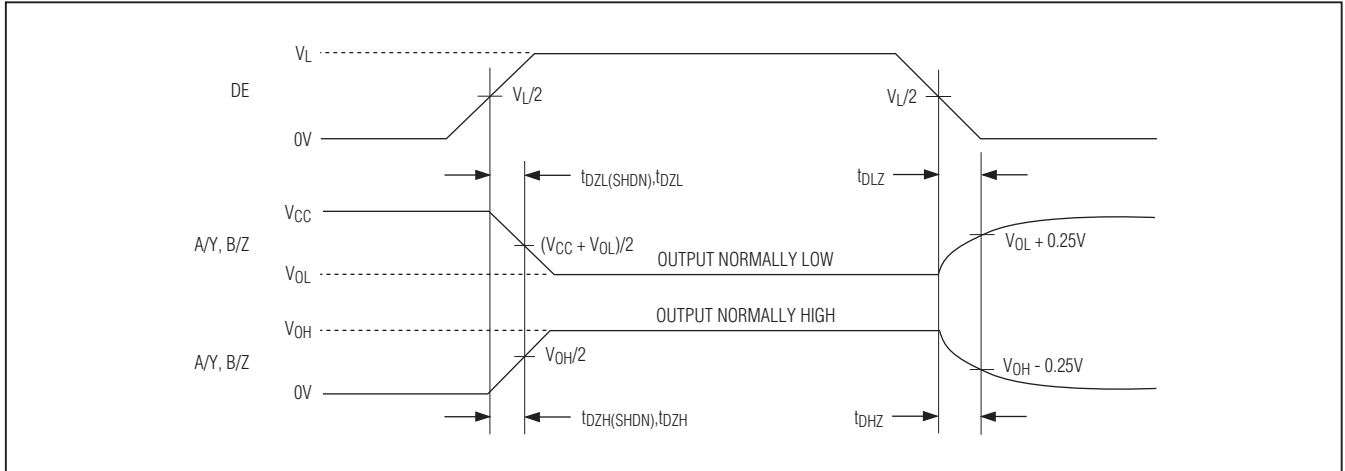


Figure 4. Driver Enable and Disable Times

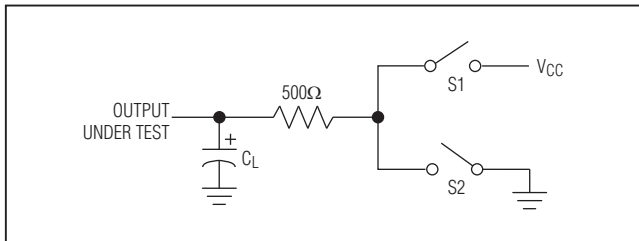


Figure 5. Driver-Enable and Disable-Timing Test Load

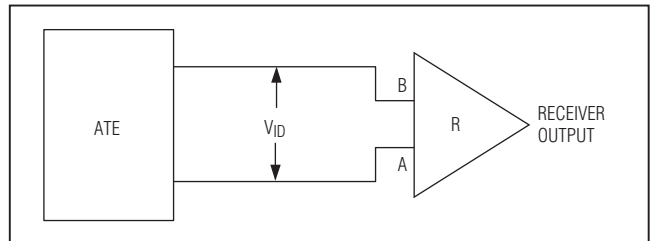


Figure 6. Receiver Propagation Delay Test Circuit

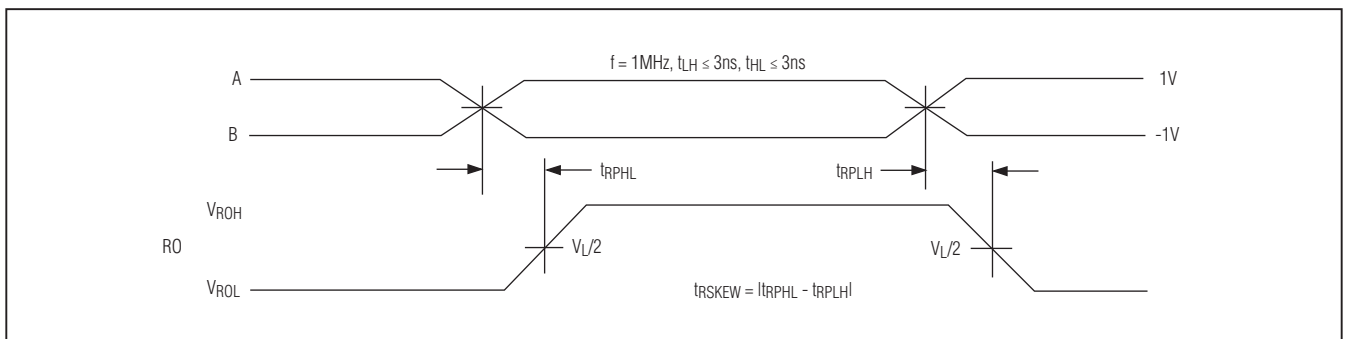


Figure 7. Receiver Propagation Delays

Test Circuits and Waveforms (continued)

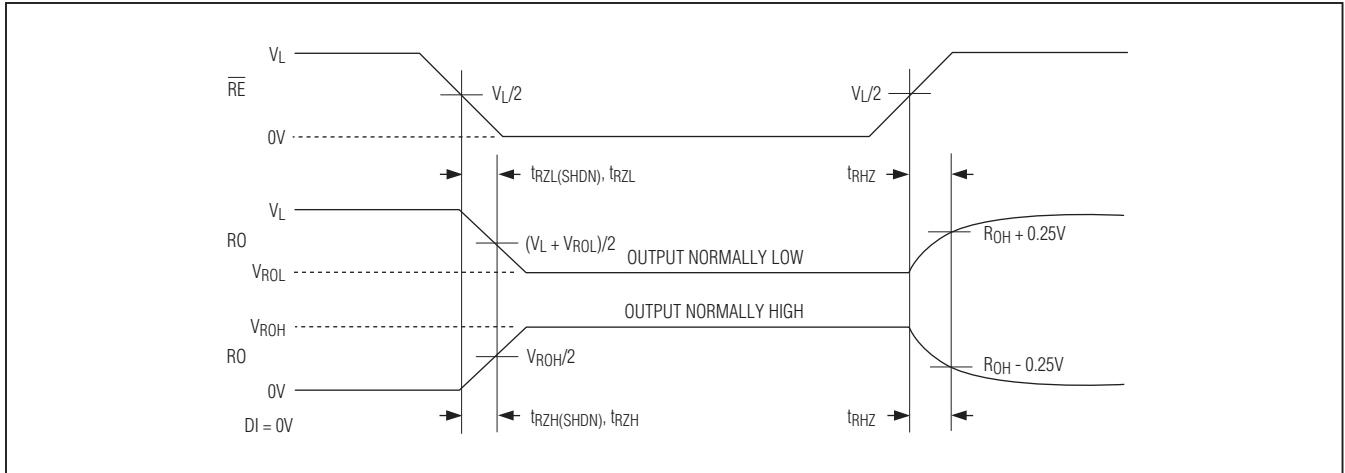


Figure 8. Receiver Enable and Disable Times

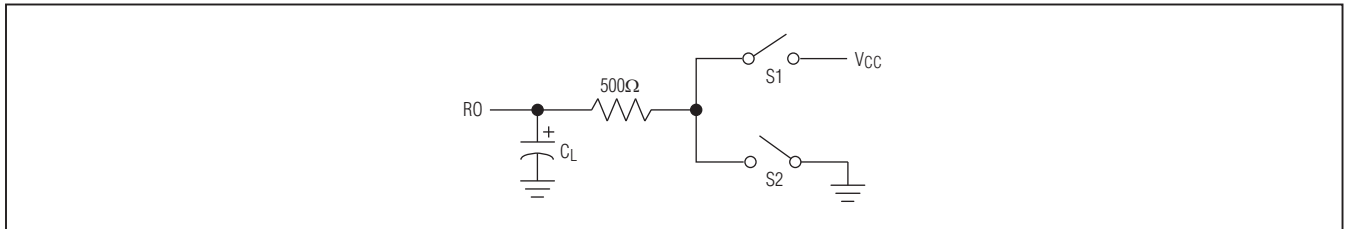


Figure 9. Receiver Enable and Disable Times

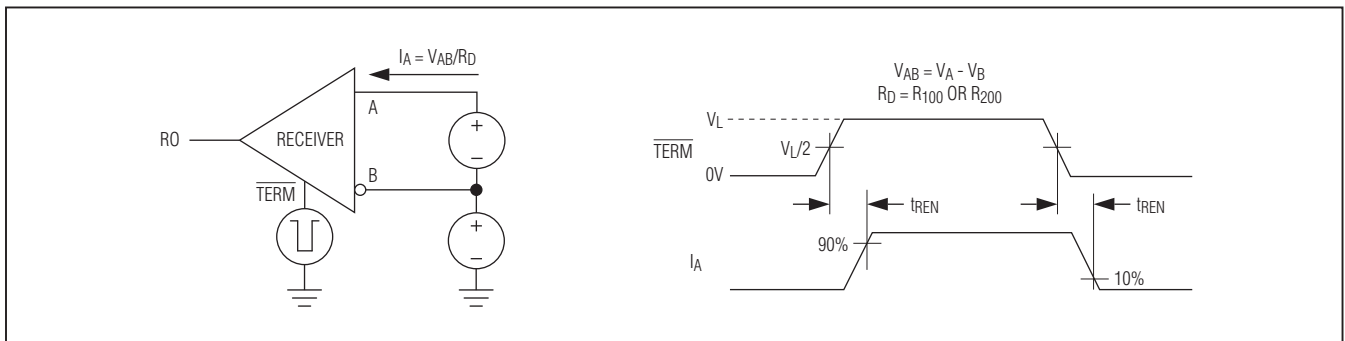
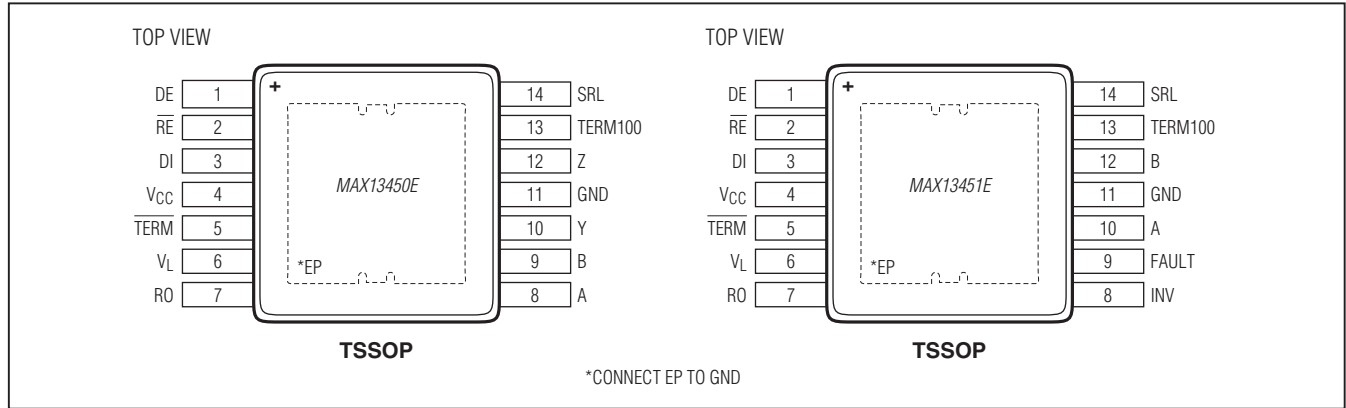


Figure 10. Termination Resistor Turn-On/Off Times

Pin Configurations



Pin Description

| PIN | | NAME | FUNCTION |
|-----------|-----------|------|---|
| MAX13450E | MAX13451E | | |
| 1 | 1 | DE | Driver-Output Enable. Drive DE low to put the driver output in three-state. Drive DE high to enable the driver. DE is referenced to VL. |
| 2 | 2 | RE | Receiver-Output Enable. Drive RE low to enable the RO. Drive RE high to disable the RO output and put the RO output in a high-impedance state. RE is referenced to VL. |
| 3 | 3 | DI | Driver Input. Drive DI low to force the noninverting output low and the inverting output high. Drive DI high to force the noninverting output high and inverting output low. DI is referenced to VL. |
| 4 | 4 | VCC | Power-Supply Voltage. Bypass VCC to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. |
| 5 | 5 | TERM | Active-Low Termination Resistor Enable. Drive TERM low to enable the internal termination resistor. TERM is referenced to VL. |
| 6 | 6 | VL | Logic Supply Voltage. Bypass VL to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. |
| 7 | — | RO | Receiver Output. When receiver is enabled and VA - VB ≥ -50mV, RO is high. If VA - VB ≤ -200mV, RO is low. RO is referenced to VL. |
| — | 7 | RO | Receiver Output. When INV is low, receiver is enabled and VA - VB ≥ -50mV, RO is high. If VA - VB ≤ -200mV, RO is low. When INV is high, receiver is enabled and VA - VB ≥ -50mV, RO is low. If VA - VB ≤ -200mV, RO is high. RO is referenced to VL. |
| 8 | — | A | Noninverting Receiver Input |
| — | 10 | A | If INV is low, A is a noninverting receiver input and a noninverting driver output. If INV is high, A is an inverting receiver input and an inverting driver output. |
| 9 | — | B | Inverting Receiver Input |
| — | 12 | B | If INV is low, B is an inverting receiver input and an inverting driver output. If INV is high, B is a noninverting receiver input and a noninverting driver output. |

Pin Description (continued)

| PIN | | NAME | FUNCTION |
|-----------|-----------|---------|---|
| MAX13450E | MAX13451E | | |
| 10 | — | Y | Noninverting Driver Output |
| 11 | 11 | GND | Ground |
| 12 | — | Z | Inverting Driver Output |
| 13 | 13 | TERM100 | Termination Resistor Value Selection Input. Drive TERM100 low to select a 120Ω termination and high to select a 100Ω termination. The TERM100 input is referenced to V _L . |
| 14 | 14 | SRL | Slew-Rate Limiting-Enable Input. Drive SRL high to enable slew-rate limiting and low to disable slew-rate limiting. The SRL input is referenced to V _L . |
| — | 8 | INV | Inversion Input. Drive INV high to internally swap RO logic level with respect to A and B signals. |
| — | 9 | FAULT | Fault Flag Output. FAULT asserts high in overcurrent conditions or if A/B are forced below GND or above V _{CC} when the driver is enabled. FAULT is referenced to V _L . |
| — | — | EP | Exposed Pad. Connect EP to GND. Do not use EP as the only GND connection. |

Function Tables

Table 1. Termination Resistor Control (MAX13450E/MAX13451E)

| TERM | DE | RE | TERMINATION RESISTOR |
|------|----|----|----------------------|
| Low | X | X | Activated |
| High | X | X | Not activated |

Table 2. Shutdown Control (MAX13450E/MAX13451E)

| DE | RE | TERM | STATE |
|-----|------|------|----------|
| Low | High | High | Shutdown |

Table 3. Function Table for Transmitter (MAX13450E)

| INPUT | | OUTPUT | |
|-------|------|--------|--------|
| DE | DI | Y | Z |
| Low | X | High-Z | High-Z |
| High | Low | Low | High |
| | High | High | Low |

Table 4. Function Table for Receiver (MAX13450E)

| INPUT | | OUTPUT |
|-------|-----------------|--------|
| RE | A-B | RO |
| High | X | High-Z |
| Low | ≥ -50mV or Open | High |
| | ≤ -200mV | Low |

Table 5. INV Input Function Table for Transmitter (MAX13451E)

| INPUT | | | OUTPUT | |
|-------|------|------|--------|--------|
| DE | INV | DI | A | B |
| Low | X | X | High-Z | High-Z |
| High | Low | Low | Low | High |
| | | High | High | Low |
| | High | Low | High | Low |
| | | High | Low | High |

Function Tables (continued)

Table 6. INV Input Function Table for Receiver (MAX13451E)

| INPUT | | | OUTPUT |
|-----------------|------|--------------------------------------|--------|
| \overline{RE} | INV | A-B | RO |
| High | X | X | High-Z |
| Low | Low | $\geq -50\text{mV}$ or Short or Open | High |
| | | $\leq -200\text{mV}$ | Low |
| | High | $\geq -50\text{mV}$ or Open | Low |
| | | $\leq -200\text{mV}$ | High |

Detailed Description

The MAX13450E is a full-duplex, RS-485/RS-422-compatible transceiver and the MAX13451E is a half-duplex, RS-485/RS-422-compatible transceiver. Both devices have an internal 100Ω/120Ω termination resistor. The MAX13450E/MAX13451E have a V_L supply voltage input to support down to a +1.8V voltage logic interface.

The MAX13450E/MAX13451E feature a 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. All line interface pins are protected to $\pm 30\text{kV}$ ESD based on the HBM. These devices also include fail-safe circuitry, guaranteeing a defined logic-level receiver output when the receiver inputs are open or shorted.

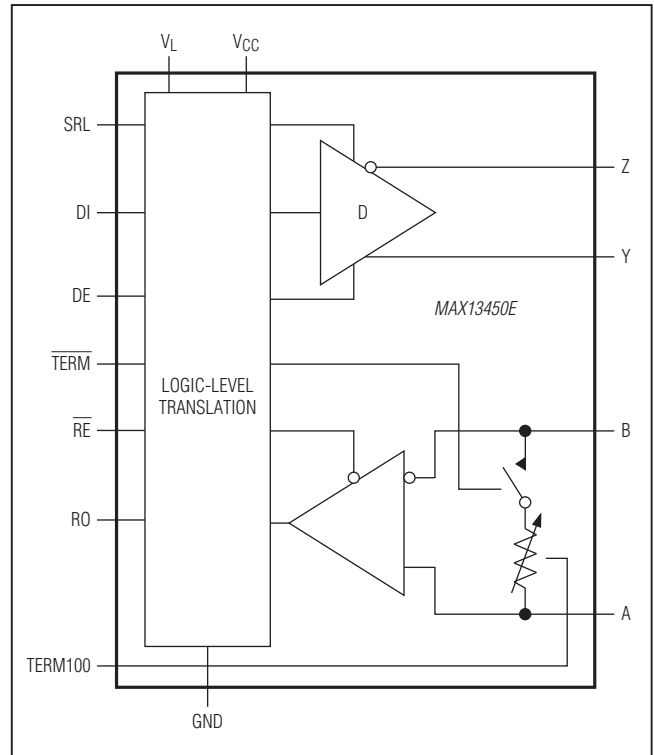
The MAX13450E/MAX13451E allow slew-rate-limited driver outputs for lower data rates below 500kbps. The SRL reduces the slew rate, which reduces EMI emissions and reflections caused by improperly terminated cables.

The MAX13451E has a FAULT output that indicates a fault condition on the driver. The MAX13451E also has an INV input that inverts the phase of A and B pins.

Termination Resistor

The MAX13450E/MAX13451E feature a selectable internal termination resistor. Drive the \overline{TERM} input low to enable the internal termination resistor. Drive the \overline{TERM} input high to disable the internal termination resistor.

Functional Diagram (MAX13450E)



Drive the TERM100 input high to select the 100Ω termination resistor. Drive TERM100 input low to select the 120Ω termination resistor.

INV Input (MAX13451E)

The INV input of the MAX13451E reverses the polarity of the RO receiver output (see Table 5 and 6). If the INV input is high then the RO output is low under fail-safe receiver conditions. This is the opposite polarity of normal fail-safe operations.

Fault Condition (MAX13451E)

The MAX13451E also has a FAULT output to indicate a fault condition. The FAULT output is active high when there is a short circuit at the driver's output, an over/undervoltage at the driver's outputs, or the device's temperature is higher than +150°C.

Thermal Shutdown

When the devices' temperature goes over +150°C, the termination resistor turns off, and the transmitter shuts down while the receiver stays active.

Fail Safe

The MAX13450E guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination resistor. With the receiver thresholds of the MAX13450E, this results in RO being logic-high.

The MAX13451E has the same fail-safe receiver behavior as the MAX13450E when the INV input is low. When the INV input is high, RO is low under the fail-safe condition.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13450E/MAX13451E have extra protection against static electricity. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13450E/MAX13451E keep working without latchup or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13450E/MAX13451E are characterized for protection to the following limits:

- ±30kV using the Human Body Model
- ±15kV using the Air Gap Discharge Method specified in IEC 61000-4-2
- ±7kV using the Contact Discharge Method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11a shows the Human Body Model, and Figure 11b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13450E/MAX13451E help equipment designs to meet IEC 61000-4-2, without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 11c shows the IEC 61000-4-2 model, and Figure 11d shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

Applications Information

Typical Applications

The MAX13450E transceiver is designed for full-duplex, bidirectional data communications on point-to-point or multipoint bus transmission lines (Figure 12). The MAX13451E transceiver is designed for half-duplex, bidirectional data communications on point-to-point or multipoint bus transmission lines (Figure 13).

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is one-unit load, and the standard driver can drive up to 32-unit loads. The MAX13450E/MAX13451E have a 1/8-unit load receiver input impedance, allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices, as well as other RS-485 transceivers with a total of 32-unit loads or fewer, can be connected to the line.

Reduced EMI and Reflections

The MAX13450E/MAX13451E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

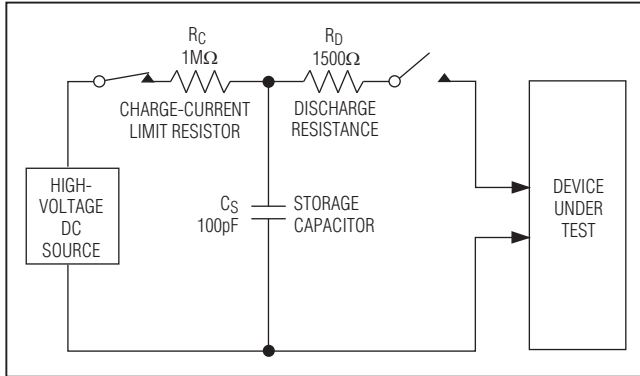


Figure 11a. Human Body ESD Test Model

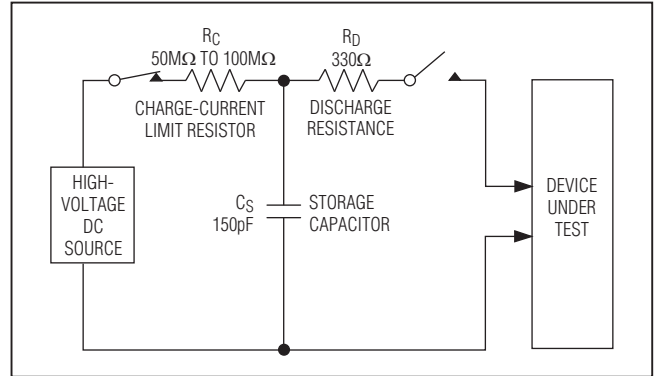


Figure 11c. IEC 61000-4-2 ESD Test Model

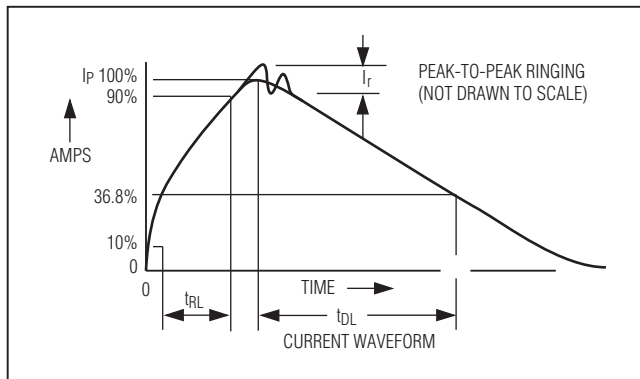


Figure 11b. Human Body Current Waveform

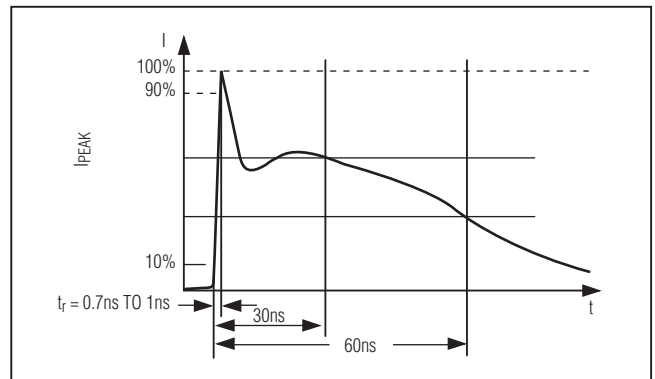


Figure 11d. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuits

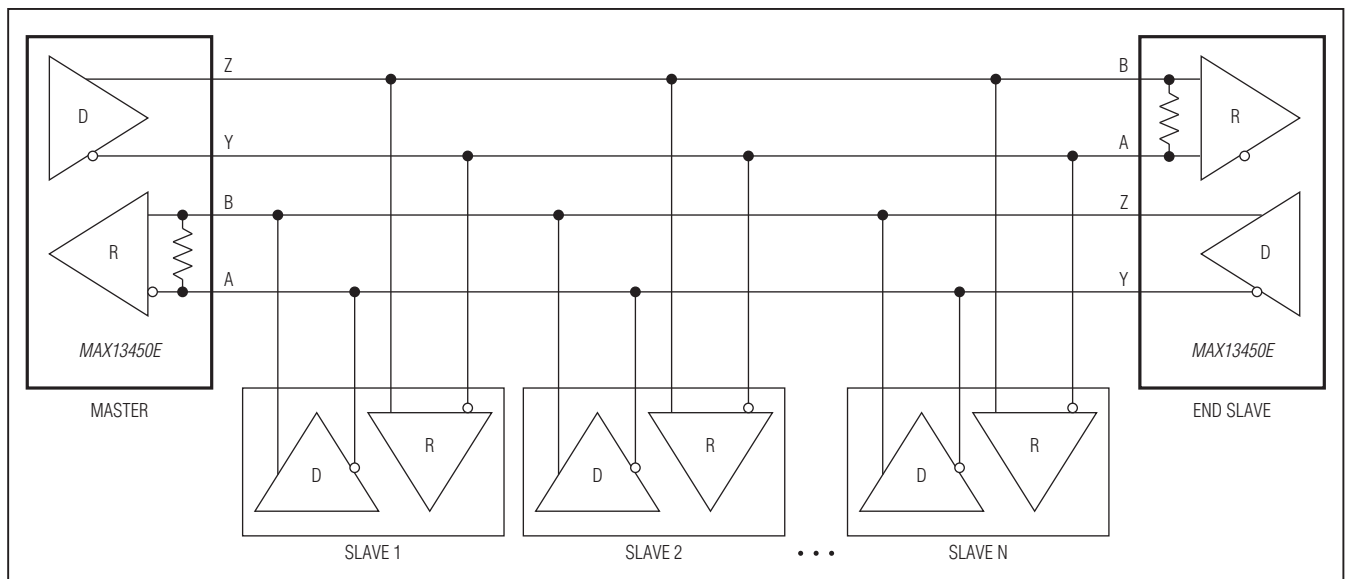


Figure 12. Full-Duplex, Multidrop (MAX13450E)

Typical Application Circuits (continued)

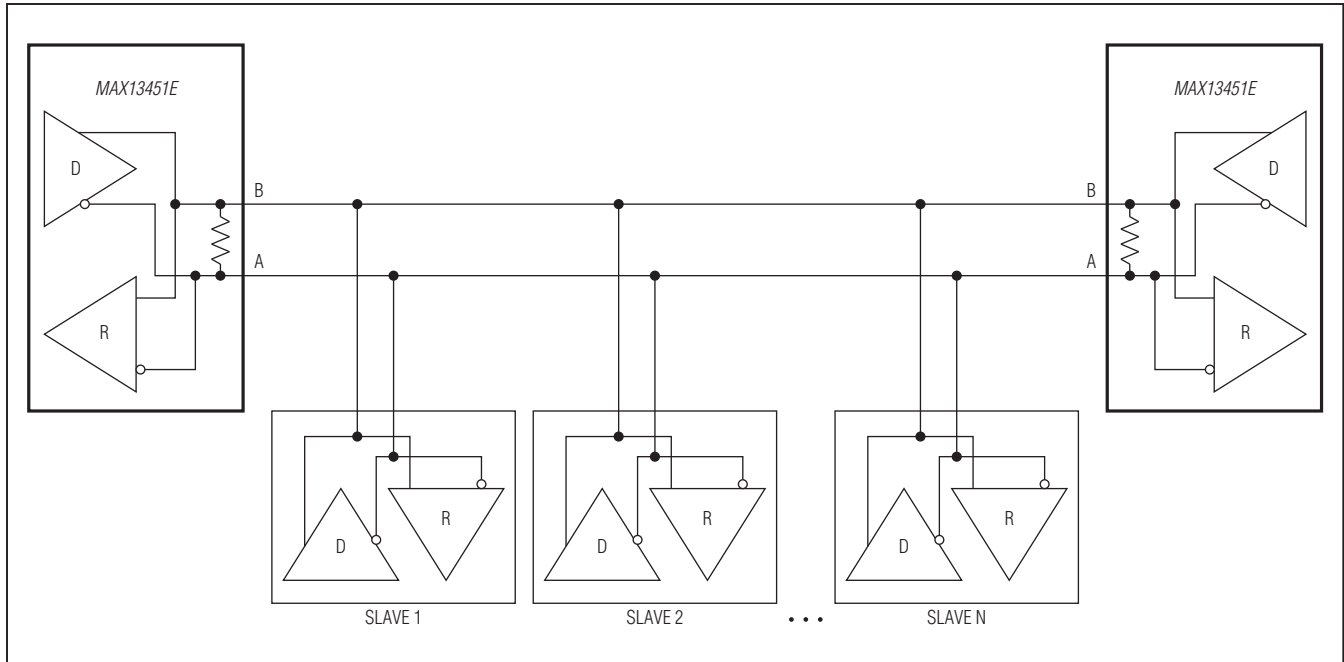


Figure 13. Half-Duplex, Multidrop, and Point-to-Point Systems (MAX13451E)

Low-Power Shutdown Mode

Drive \overline{RE} high, DE low, and \overline{TERM} high to enter low-power shutdown mode (see Table 2).

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 14 TSSOP-EP | U14E+3 | 21-0108 | 90-0119 |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0 | 4/10 | Initial release | — |
| 1 | 11/10 | Updated the V_L specification in the <i>Electrical Characteristics</i> and <i>Switching Characteristics</i> tables | 2-5 |
| 2 | 2/15 | Added the <i>Benefits and Features</i> section | 1 |

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