## AMIS-30523

## Product Preview

## CAN Micro-Stepping Motor Driver

## Introduction

The AMIS-30523 is a micro-stepping stepper motor driver for bipolar stepper motors with an embedded CAN transceiver.

The motor driver is connected through I/O pins and a SPI interface with an external microcontroller. It has an on-chip voltage regulator, reset-output and watchdog reset, able to supply peripheral devices. It contains a current-translation table and takes the next micro-step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin.

The CAN transceiver is the interface between a (CAN) protocol controller and the physical bus. It provides differential transmit capability to the bus and differential receive capability to the CAN controller. To cope with the long bus delay the communication speed needs to be low. The integrated transceiver allows low transmit data rates down 10 kbit/s or lower.

The AMIS-30523 is ideally suited for general-purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on-chip voltage regulator and embedded CAN transceiver it further reduces the BOM for mechatronic stepper applications.
Key Features
Motor Driver

- Dual H-Bridge for 2-Phase Stepper Motors
- Programmable Peak-Current up to 1.2 A Continuous (1.6 A for a Short Time)*
- On-Chip Current Translator
- SPI Interface
- Seven Step Modes from Full Step up to 32 Micro-Steps
- PWM Current Control with Automatic Selection of Fast and Slow Decay and Fully Integrated Current-Sense
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Integrated 5 V Regulator to Supply External Microcontroller


## CAN Transceiver

- Compatible with the ISO 11898 Standard
- Wide Range of Bus Communication Speed (0 up to 1 Mbit/s)
- Allows Low Transmit Data Rate in Networks Exceeding 1 km
- Extremely Low Current Standby Mode with Wake-up via the Bus
*Output Current Level May be Limited by Ambient Temperature and Heat Sinking


## BLOCK DIAGRAM




Figure 2. Pin Out AMIS-30523

Table 1. PIN DESCRIPTION

| Name | Pin | Description | Type | Equivalent Schematic |
| :---: | :---: | :--- | :---: | :---: |
| GND | 1,2 | Ground | Supply |  |
| $/$ | 3 | No function (to be left open in normal operation) |  |  |
| VCC | 4 | CAN Supply voltage | Supply |  |
| $/$ | 5 | No function (to be left open in normal operation) |  |  |
| RXD | 6 | CAN Receive data output; dominant transmitter $\rightarrow$ low output | Digital Output |  |
| VSPLIT | 7 | CAN common-mode stabilization output | Supply |  |
| DI | 8 | SPI Data In | Digital Input | Type 2 |
| CLK | 9 | SPI Clock Input | Digital Input | Type 2 |
| NXT | 10 | Next micro-step input | Digital Input | Type 2 |
| $/$ | $11 . .16$ | No function (to be left open in normal operation) | Digital Output | Type 2 |
| DIR | 17 | Direction input | Analog Output | Type 5 |
| ERRB | 18 | Error output (open drain) | High Voltage |  |
| SLA | 19 | Speed load angle output | High Voltage |  |
| CPN | 20 | Negative connection of charge pump capacitor | High Voltage |  |
| CPP | 21 | Positive connection of charge pump capacitor | Digital Input | Type 1 |
| VCP | 22 | Charge pump filter-capacitor | Digital Input | Type 2 |
| CLR | 23 | "Clear" = chip reset input | Supply | Type 3 |
| CSB | 24 | SPI chip select input | Driver Output |  |
| VBB | 25,26 | High voltage supply Input | Supply |  |
| MOTYP | 27,28 | Negative end of phase Y coil output |  |  |
| GND | 29,30 | Ground, heat sink |  |  |
|  |  |  |  |  |

## AMIS-30523

Table 1. PIN DESCRIPTION

| Name | Pin | Description | Type | Equivalent Schematic |
| :---: | :---: | :--- | :---: | :---: |
| MOTYN | 31,32 | Positive end of phase Y coil output | Driver Output |  |
| $/$ | 33 | No function (to be left open in normal operation) |  |  |
| MOTXN | 34,35 | Positive end of phase X coil output | Driver Output |  |
| GND | 36,37 | Ground, heat sink | Supply |  |
| MOTXP | 38,39 | Negative end of phase X coil output | Driver Output | Supply |
| VBB | 40,41 | High voltage supply input | Type 3 |  |
| PORB/WD | 42 | Power-on-reset and watchdog reset output (open drain) | Digital Output | Type 2 |
| TSTO | 43 | Test pin input (to be tied to ground in normal operation) | Digital Input |  |
| $/$ | 44 | No function (to be left open in normal operation) |  | Type 4 |
| DO | 45 | SPI data output (open drain) | Supply | Type 6 |
| VDD | 46 | $5 V$ Logic Supply Output (needs external decoupling <br> capacitor) | Supply |  |
| GND | 47 | Ground | Analog Output |  |
| CANH | 48 | High-level CAN bus line (high in dominant mode) | Analog Output |  |
| CANL | 49 | Low-level CAN bus line (low in dominant mode) |  |  |
| $/$ | 50 | No function (to be left open in normal operation) | Digital Input |  |
| STB | 51 | CAN stand-by mode control input | Digital Input |  |
| TXD | 52 | CAN transmit data input; low input $\rightarrow$ dominant driver; <br> internal pull-up current |  |  |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $V_{B B}$ | Analog DC supply voltage (Note 1) | -0.3 | +40 | V |
| $\mathrm{V}_{\mathrm{CC}}$ | CAN Supply voltage | -0.3 | +7 | V |
| $\mathrm{V}_{\text {CANH, }}$ <br> $V_{\text {CANL }}$, <br> $V_{\text {SPLIT }}$ | DC voltage CANH ,CANL and VSPLIT (Note 2) | -50 | +50 | V |
| $\mathrm{V}_{\text {TRANS }}$ | Transient voltage CANH, CANL and VSPLIT (Note 3) | -300 | +300 | V |
| $\mathrm{T}_{\text {ST }}$ | Storage temperature | -55 | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction Temperature under bias (Note 4) | -40 | +170 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {ESD }}$ | Electrostatic discharges on component level, All pins (Note 5) | -2 | +2 | kV |
| $V_{\text {ESD }}$ | Electrostatic discharges on component level, All pins (Note 7) | -500 | +500 | V |
| $V_{\text {ESD }}$ | Electrostatic discharges on CANH, CANL and VSPLIT (Note 6) | -6 | +6 | kV |
| $\mathrm{V}_{\text {ESD }}$ | Electrostatic discharges on CANH and CANL (Note 7) | -500 | +500 | V |
| $\mathrm{V}_{\text {ESD }}$ | Electrostatic discharges on component level, HiV pins (Note 6) | -6 | +6 | kV |
| Latch-up | Static latch-up at all pins |  | 100 | mA |

[^0]Table 3. THERMAL RESISTANCE

|  | Thermal Resistance |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $\begin{array}{c}\text { Junction-to-Exposed Pad } \\ \text { (Rth } \\$\end{array} | Junction-to-Ambient (Rth |  |$)$

EQUIVALENT SCHEMATICS
Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.


TYPE 1: CLR Input


TYPE 2: CLK, DI, $\overline{C S}$, NXT, DIR Inputs


TYPE 4: DO and ERR Open Drain Outputs


TYPE 5: SLA Analog Output


TYPE 3: $\mathrm{V}_{\mathrm{DD}}$ and $\mathrm{V}_{\mathrm{BB}}$ Power Supply
Figure 3. In- and Output Equivalent Diagrams

## PACKAGE THERMAL CHARACTERISTICS

The AMIS-30523 is available in a QFN-52 package. For cooling optimizations, the QFN has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer. Figure 4 gives an example for good power distribution solutions.

For precise thermal cooling calculations the major thermal resistances of the device are given. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the exposed pad)

The thermal resistances are presented in Table 5: DC Parameters Motor Driver.

The major thermal resistances of the device are the Rth from the junction to the ambient ( $\mathrm{Rth}_{\mathrm{J}-\mathrm{A}}$ ) and the overall Rth from the junction to exposed pad ( $\mathrm{Rth}_{\mathrm{J}-\mathrm{EP}}$ ). In Table 3 one can find the values for the $\mathrm{Rth}_{\mathrm{J}-\mathrm{A}}$ and $\mathrm{Rt} \mathrm{h}_{\mathrm{J}-\mathrm{EP}}$, simulated according to JESD-51:

The Rth ${ }_{\mathrm{J}-\mathrm{A}}$ for 2 S 2 P is simulated conform JEDEC JESD-51 as follows:

- A 4-layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- The 2 signal layers: $70 \mu \mathrm{~m}$ thick copper with an area of $5500 \mathrm{~mm}^{2}$ copper and $20 \%$ conductivity
- The 2 power internal planes: $36 \mu \mathrm{~m}$ thick copper with an area of $5500 \mathrm{~mm}^{2}$ copper and $90 \%$ conductivity The Rth ${ }_{\mathrm{J}-\mathrm{A}}$ for 1 SOP is simulated conform JEDEC JESD-51 as follows:
- A 1-layer printed circuit board with a single power and signal layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of $70 \mu \mathrm{~m}$ copper with an area of $5500 \mathrm{~mm}^{2}$ copper and $20 \%$ conductivity


Figure 4. Example of QFN-52 PCB Ground Plane Layout in Top View (preferred layout at top and bottom)

## ELECTRICAL SPECIFICATION

## Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating
ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4. OPERATING RANGES

| Symbol | Parameter | Min | Max |
| :---: | :--- | :---: | :---: |
| $V_{B B}$ | Motor Driver Analog DC supply | 6 | 30 |
| $\mathrm{~V}_{\mathrm{CC}}$ | CAN transceiver DC supply | V |  |
| $\mathrm{T}_{J}$ | Junction temperature (Note 8) | 4.75 | 5.25 |

8. No more than 100 cumulative hours in life time above $\mathrm{T}_{\mathrm{tw}}$.

## AMIS-30523

## Table 5. DC PARAMETERS MOTOR DRIVER

(The DC Parameters are Given for $\mathrm{V}_{\mathrm{BB}}$ and Temperature in Their Operating Ranges Unless Otherwise Specified) Convention: Currents Flowing in the Circuit are Defined as Positive.

| Symbol | Pin(s) | Parameter | Remark/ <br> Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: |

SUPPLY AND VOLTAGE REGULATOR

| $V_{B B}$ | VBB | Nominal operating supply range |  | 6 |  | 30 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {BB }}$ |  | Total internal current consumption | Unloaded outputs |  |  | 8 | mA |
| $\mathrm{I}_{\text {BBS }}$ |  | Sleep current in $\mathrm{V}_{\text {BB }}$ (Note 9) | Unloaded outputs |  |  | 100 | $\mu \mathrm{A}$ |
| $V_{\text {DD }}$ | VDD | Regulated Output Voltage |  | 4.50 | 5 | 5.50 | V |
| $\mathrm{I}_{\text {INT }}$ |  | Internal load current | Unloaded outputs |  |  | 8 | mA |
| ILOAD |  | Max. Output Current (external and internal loads) | $6 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}}<8 \mathrm{~V}$ | 15 |  |  | mA |
|  |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \vee 30 \mathrm{~V}$ | 40 |  |  | mA |
| IdDLIM |  | Current limitation | Pin shorted to ground |  |  | 200 | mA |
| ILOAD_pD |  | Output current in Power Down |  | 1 |  |  | mA |

POWER ON RESET (POR)

| $\mathrm{V}_{\text {DDH }}$ | VDD | Internal POR comparator threshold | VDD rising | 3.9 | 4.15 | 4.4 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DDL }}$ |  | Internal POR comparator threshold | VDD falling |  | 3.80 |  | V |
| $V_{\text {DDHYS }}$ |  | Hysteresis between $\mathrm{V}_{\text {DDH }}$ and $\mathrm{V}_{\text {DDL }}$ |  | 0.1 | 0.35 | 0.6 | V |

MOTORDRIVER

| IMDmax, Peak | MOTXP <br> MOTXN <br> MOTYP <br> MOTYN | Max current through motor coil in normal operation |  |  | 1600 |  | mA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {Mdmax, RMS }}$ |  | Max RMS current through coil in normal operation |  |  | 800 |  | mA |
| $1_{\text {Mdabs }}$ |  | Absolute error on coil current |  | -10 |  | 10 | \% |
| $I_{\text {Mdrel }}$ |  | Error on current ratio $\mathrm{I}_{\text {coil }} / \mathrm{I}_{\text {coily }}$ |  | -7 |  | 7 | \% |
| ISET_TC1 |  | Temperature coefficient of coil current set-level, CUR[4:0] = $0 . . .27$ (Note 10) | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 160^{\circ} \mathrm{C}$ |  | -240 |  | ppm/K |
| $\mathrm{I}_{\text {SET_TC2 }}$ |  | Temperature coefficient of coil current set-level, CUR[4:0] = 28 ... 31 (Note 10) | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 160^{\circ} \mathrm{C}$ |  | -490 |  | ppm/K |
| $\mathrm{R}_{\mathrm{HS}}$ |  | On-resistance high-side driver, CUR[4:0] = 0 ... 31 | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=27^{\circ} \mathrm{C}$ |  | 0.45 | 0.56 | $\Omega$ |
|  |  |  | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=160^{\circ} \mathrm{C}$ |  | 0.94 | 1.25 | $\Omega$ |
| RLS3 |  | On-resistance low-side driver, CUR[4:0] = $23 \ldots 31$ | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=27^{\circ} \mathrm{C}$ |  | 0.45 | 0.56 | $\Omega$ |
|  |  |  | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=160^{\circ} \mathrm{C}$ |  | 0.94 | 1.25 | $\Omega$ |
| RLS2 |  | On-resistance low-side driver, CUR[4:0] = 16 ... 22 | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=27^{\circ} \mathrm{C}$ |  | 0.90 | 1.2 | $\Omega$ |
|  |  |  | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=160^{\circ} \mathrm{C}$ |  | 1.9 | 2.5 | $\Omega$ |
| $\mathrm{R}_{\text {LS } 1}$ |  | On-resistance low-side driver, CUR[4:0] = $9 \ldots 15$ | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{J}=27^{\circ} \mathrm{C}$ |  | 1.8 | 2.3 | $\Omega$ |
|  |  |  | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=160^{\circ} \mathrm{C}$ |  | 3.8 | 5.0 | $\Omega$ |
| $\mathrm{R}_{\text {LSo }}$ |  | On-resistance low-side driver, CUR[4:0] = $0 . . .8$ | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=27^{\circ} \mathrm{C}$ |  | 3.6 | 4.5 | $\Omega$ |
|  |  |  | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=160^{\circ} \mathrm{C}$ |  | 7.5 | 10 | $\Omega$ |
| $\mathrm{I}_{\text {Mpd }}$ |  | Pull down current motor pins | HiZ mode |  | 1 |  | mA |

9. Characterization Data Only, not tested in production
10. The coil current at a given junction temperature is calculated as: $I_{\text {coil }} @ T_{J}=I_{\text {coil }}\left[1+\left(T_{J}-125\right) \times I_{\text {SET TCi }} \times 10^{-6}\right]$.

See also paragraph Programmable Peak Current.
11. Not valid for pins with internal Pull Down resistor.
12. No more than 100 cumulated hours in life time above $T_{t w}$.
13. Thermal shutdown is derived from Thermal Warning.

## Table 5. DC PARAMETERS MOTOR DRIVER

(The DC Parameters are Given for $V_{B B}$ and Temperature in Their Operating Ranges Unless Otherwise Specified)
Convention: Currents Flowing in the Circuit are Defined as Positive.

| Symbol | Pin(s) | Parameter | Remark/ <br> Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## DIGITAL INPUTS

| $l_{\text {leak }}$ | $\begin{aligned} & \text { DI, CLK } \\ & \text { NXT, } \\ & \text { DIR } \\ & \text { CLR, } \\ & \text { CSB } \end{aligned}$ | Input Leakage (Note 11) | $\mathrm{T}_{J}=160^{\circ} \mathrm{C}$ |  | 1 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ |  | Logic Low Threshold |  | 0 | 0.65 | V |
| $\mathrm{V}_{\mathrm{IH}}$ |  | Logic High Threshold |  | 2.20 | $V_{D D}$ | V |
| $\mathrm{R}_{\text {pd_CLR }}$ | CLR | Internal Pull Down Resistor |  | 120 | 300 | $\mathrm{k} \Omega$ |
| $\mathrm{R}_{\text {pd_TST }}$ | TSTO | Internal Pull Down Resistor |  | 3 | 9 | k $\Omega$ |

DIGITAL OUTPUTS

| $V_{\text {OL }}$ | DO, <br> ERRB, <br> PORB/ <br> WD | Logic Low level open drain | $\mathrm{IOL}=5 \mathrm{~mA}$ |  |  | 0.3 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

THERMAL WARNING \& SHUTDOWN

| $\mathrm{T}_{\mathrm{tw}}$ |  | Thermal Warning |  | 138 | 145 | 152 | ${ }^{\circ} \mathrm{C}$ |
| :---: | :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{tsd}}$ |  | Thermal shutdown (Notes 12 and 13) |  |  | $\mathrm{T}_{\mathrm{tw}}+20$ |  | ${ }^{\circ} \mathrm{C}$ |

## CHARGE PUMP

| $V_{\text {opCP }}$ | VCP | Output voltage | $6 \mathrm{~V}<\mathrm{V}_{\mathrm{BB}}<15 \mathrm{~V}$ |  | $\begin{aligned} & 2 * V_{B B} \\ & -2 \end{aligned}$ |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $15 \mathrm{~V}<\mathrm{V}_{\mathrm{BB}}<30 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{BB}}+9$ | $\begin{gathered} \mathrm{V}_{\mathrm{BB}}+ \\ 11.5 \end{gathered}$ | $\begin{gathered} \hline \mathrm{V}_{\mathrm{BB}}+ \\ 16 \end{gathered}$ | V |

## PACKAGE THERMAL RESISTANCE VALUE

| $\mathrm{Rth}_{J-A}$ | $\begin{gathered} \text { QFN } \\ \text { package } \end{gathered}$ | Thermal Resistance Junction-to-Ambient | Simulated Conform JEDEC JESD-51, (2S2P) | 30 | K/W |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Rth ${ }_{\text {J-EP }}$ |  | Thermal Resistance Junction-to-Exposed Pad |  | 0.95 | K/W |

SPEED AND LOAD ANGLE OUTPUT

| $\mathrm{V}_{\text {out }}$ | Output Voltage Range |  | 0.2 |  | $\mathrm{~V}_{\mathrm{DD}}-$ | V |
| :---: | :--- | :--- | :--- | :--- | :--- | :---: | :---: |
|  |  |  |  |  |  |  |$)$

9. Characterization Data Only, not tested in production
10. The coil current at a given junction temperature is calculated as: $I_{\text {coil }} @ T_{J}=I_{\text {coil }}\left[1+\left(T_{J}-125\right) \times I_{S E T}\right.$ TCi $\left.\times 10^{-6}\right]$.

See also paragraph Programmable Peak Current.
11. Not valid for pins with internal Pull Down resistor.
12. No more than 100 cumulated hours in life time above $T_{\text {tw }}$.
13. Thermal shutdown is derived from Thermal Warning.

Table 6. AC PARAMETERS MOTOR DRIVER (The AC Parameters are Given for $\mathrm{V}_{\mathrm{BB}}$ and Temperature in Their Operating Ranges)

| Symbol | Pin(s) | Parameter | Remark/ <br> Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

## INTERNAL OSCILLATOR

| $\mathrm{f}_{\text {osc }}$ |  | Frequency of internal oscillator |  | 3.6 | 4 | 4.4 | MHz |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

## MOTOR DRIVER

| $\mathrm{f}_{\text {PWM }}$ | MOTxx | PWM frequency | Frequency depends only on internal oscillator | 20.8 | 22.8 | 24.8 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Double PWM frequency |  | 41.6 | 45.6 | 49.6 | kHz |
| $\mathrm{f}_{\mathrm{d}}$ |  | PWM jitter Depth (Note 14) |  |  | 10 |  | \% fPWM |
| tbrise | MOTxx | Turn-on voltage slope, 10\% to 90\% | EMC[1:0] = 00 |  | 150 |  | V/us |
|  |  |  | EMC[1:0] = 01 |  | 100 |  | V/us |
|  |  |  | EMC[1:0] = 10 |  | 50 |  | V/us |
|  |  |  | EMC[1:0] = 11 |  | 25 |  | V/us |
| $t b_{\text {fall }}$ | MOTxx | Turn-off voltage slope, 90\% to 10\% | EMC[1:0] = 00 |  | 150 |  | V/us |
|  |  |  | EMC[1:0] = 01 |  | 100 |  | V/us |
|  |  |  | EMC[1:0] = 10 |  | 50 |  | V/us |
|  |  |  | EMC[1:0] = 11 |  | 25 |  | $\mathrm{V} / \mu \mathrm{s}$ |

DIGITAL OUTPUTS

| $\mathrm{t}_{\mathrm{H} 2 \mathrm{~L}}$ | DO <br> ERRB | Output fall-time from $\mathrm{V}_{\text {inH }}$ to $\mathrm{V}_{\text {inL }}$ (Note 14) | Capacitive load 400 pF <br> and pull--up resistor of <br> $1.5 \mathrm{k} \Omega$ | ns |
| :---: | :---: | :--- | :--- | :--- | :--- | :--- |

## CHARGE PUMP

| $\mathrm{f}_{\mathrm{CP}}$ | CPN <br> CPP | Charge pump frequency |  | 250 | kHz |  |  |
| :---: | :---: | :--- | :--- | :--- | :--- | :---: | :---: |
| $\mathrm{t}_{\text {CPU }}$ | MOTxx | Start-up time of charge pump (Note 14) | Spec external <br> components See <br> Table 10 |  |  | 5 | ms |

## CLR FUNCTION

| $\mathrm{t}_{\mathrm{CLR}}$ | CLR | Hard reset duration time |  | 100 |  |  | $\mu \mathrm{~s}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

POWER-UP

| $t_{\text {PU }}$ | PORB/ WD | Power-up time | $\begin{aligned} & \mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}= \\ & 50 \mathrm{~mA}, \mathrm{C}_{\mathrm{LOAD}}=220 \mathrm{nF} \end{aligned}$ |  | 110 | $\mu \mathrm{s}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {POR }}$ |  | Reset duration | See Figure 22 |  | 100 | ms |
| $\mathrm{t}_{\text {RF }}$ |  | Reset filter time | See Figure 22 | 1 |  | $\mu \mathrm{s}$ |

WATCHDOG

| $t_{\text {WDTO }}$ | $\begin{aligned} & \hline \text { PORB/ } \\ & \text { WD } \end{aligned}$ | Watchdog time out interval | See Figure 23 | 32 |  | 512 | ms |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| twDPR |  | Prohibited watchdog acknowledge delay | See Figure 23 |  | 2 |  | ms |

## NXT FUNCTION

| $\mathrm{t}_{\mathrm{NXT}} \mathrm{HI}^{\text {d }}$ | NXT | NXT Minimum, High Pulse Width | See Figure 5 | 2 |  | us |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{NXT}} \mathrm{HI}^{\text {d }}$ |  | NXT Minimum, Low Pulse Width | See Figure 5 | 2 |  | us |
| toir_SET |  | NXT Hold Time, Following Change of DIR | See Figure 5 |  | 2 | $\mu \mathrm{S}$ |
| tolR_HOLD |  | NXT Hold Time, Before Change of DIR | See Figure 5 |  | 2 | $\mu \mathrm{s}$ |

14. Characterization Data Only, not tested in production.


Figure 5. NXT-Input Timing Diagram
Table 7. SPI TIMING PARAMETERS

| Symbol | Parameter | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {CLK }}$ | SPI clock period | 1 |  |  | us |
| tclk_high | SPI clock high time | 100 |  |  | ns |
| tcLk_LOW | SPI clock low time | 100 |  |  | ns |
| tset_DI | DI set up time, valid data before rising edge of CLK | 50 |  |  | ns |
| thold_d | DI hold time, hold data after rising edge of CLK | 50 |  |  | ns |
| tCSB_HIGH | CSB high time | 2.5 |  |  | us |
| $\mathrm{t}_{\text {SET_CSB }}$ | CSB set up time, CSB low before rising edge of CLK | 100 |  |  | ns |
| $\mathrm{t}_{\text {SET_CLK }}$ | CLK set up time, CLK low before rising edge of CSB | 100 |  |  | ns |



Figure 6. SPI Timing

Table 8. DC PARAMETERS CAN TRANSCEIVER
(The DC parameters are given for $\mathrm{V}_{\mathrm{CC}}$ and temperature in its operating range; $\mathrm{T}_{J}=-40$ to $+150^{\circ} \mathrm{C} ; \mathrm{R}_{\mathrm{LT}}=60 \Omega$ unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark / <br> Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: | :---: |

SUPPLY

| Icc | VCC | Supply current | Dominant; $\mathrm{V}_{\mathrm{T}_{\times \mathrm{D}}}=0 \mathrm{~V}$ <br> Recessive; $\mathrm{V}_{\mathrm{TxD}}=\mathrm{V}_{\mathrm{CC}}$ | 45 | 65 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Iccs |  | Supply current in standby mode | $\mathrm{T}_{\mathrm{J}, \text { max }}=100^{\circ} \mathrm{C}$ | 4 | 8 | mA |

TRANSMITTER DATA INPUT

| $\mathrm{V}_{\mathrm{iH}}$ | TXD | High-level input voltage | CAN bus output recessive | 2.0 | - | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}+ \\ 0.3 \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{iL}}$ |  | Low-level input voltage | CAN bus output dominant | -0.3 | - | +0.8 | V |
| $\mathrm{l}_{\text {iH }}$ |  | High-level input current | $\mathrm{V}_{\mathrm{TXD}}=\mathrm{V}_{\mathrm{CC}}$ | -5 | 0 | +5 | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\text {iL }}$ |  | Low-level input current | $\mathrm{V}_{\text {TXD }}=0 \mathrm{~V}$ | -75 | -200 | -350 | $\mu \mathrm{A}$ |
| $\mathrm{C}_{\mathrm{i}}$ |  | Input capacitance | (Note 15) | - | 5 | 10 | pF |

TRANSMITTER MODE SELECT

| $\mathrm{V}_{\mathrm{iH}}$ | TXD | High-level input voltage | Standby mode | 2.0 | - | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}+ \\ 0.3 \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {iL }}$ |  | Low-level input voltage | Normal mode | -0.3 | - | +0.8 | V |
| $\mathrm{l}_{\mathrm{iH}}$ |  | High-level input current | $\mathrm{V}_{\text {STB }}=\mathrm{V}_{\text {CC }}$ | -5 | 0 | +5 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{iL}}$ |  | Low-level input current | $\mathrm{V}_{\text {STB }}=0 \mathrm{~V}$ | -1 | -4 | -10 | $\mu \mathrm{A}$ |
| $\mathrm{C}_{\mathrm{i}}$ |  | Input capacitance | (Note 15) | - | 5 | 10 | pF |

RECEIVER DATA OUTPUT

| $\mathrm{V}_{\mathrm{OH}}$ | RXD | High-level output voltage | $\mathrm{I}_{\mathrm{RXD}}=-10 \mathrm{~mA}$ | $\begin{aligned} & 0.6 x \\ & V_{C C} \end{aligned}$ |  | $\begin{aligned} & 0.75 x \\ & V_{C C} \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| V OL |  | Low-level output voltage | $\mathrm{I}_{\mathrm{RXD}}=5 \mathrm{~mA}$ |  | 0.25 | 0.45 | V |
| $\mathrm{I}_{\text {oh }}$ |  | High-level output current | $\mathrm{V}_{\mathrm{O}}=0.7 \times \mathrm{V}_{\text {CC }}$ | -5 | -10 | -15 | mA |
| 101 |  | Low-level output current | $\mathrm{V}_{\mathrm{O}}=0.3 \times \mathrm{V}_{\mathrm{CC}}$ | 5 | 10 | 15 | mA |
| $\mathrm{C}_{\mathrm{i}}$ |  | Input capacitance | (Note 15) | - | 5 | 10 | pF |

15. Characterization Data Only, not tested in production.

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Table 8. DC PARAMETERS CAN TRANSCEIVER
(The DC parameters are given for $\mathrm{V}_{\mathrm{CC}}$ and temperature in its operating range; $\mathrm{T}_{\mathrm{J}}=-40$ to $+150^{\circ} \mathrm{C}$; $\mathrm{R}_{\mathrm{LT}}=60 \Omega$ unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark / <br> Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: | :---: |

BUS LINES

| $V_{o \text { (reces) }}$ (norm) | CANH CANL | Recessive bus voltage | $\mathrm{V}_{\mathrm{TXD}}=\mathrm{V}_{\mathrm{CC}} ;$ no load normal mode | 2.0 | 2.5 | 3.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \hline \mathrm{V}_{\mathrm{O} \text { (reces) }} \text { (stby) } \end{gathered}$ |  | Recessive bus voltage | $\mathrm{V}_{\mathrm{TXD}}=\mathrm{V}_{\mathrm{CC}} ; \text { no load }$ standby mode | -100 | 0 | 100 | mV |
| $\mathrm{I}_{\mathrm{o}}$ (reces) (CANH) |  | Recessive output current at pin CANH | $\begin{aligned} & -35 \mathrm{~V}<\mathrm{V}_{\mathrm{CANH}}<+35 \mathrm{~V} ; \\ & 0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<5.25 \mathrm{~V} \end{aligned}$ | -2.5 | - | +2.5 | mA |
| $\mathrm{I}_{\mathrm{o}}$ (reces) (CANL) |  | Recessive output current at pin CANL | $\begin{aligned} & -35 \mathrm{~V}<\mathrm{V}_{\mathrm{CANL}}<+35 \mathrm{~V} ; \\ & 0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<5.25 \mathrm{~V} \end{aligned}$ | -2.5 | - | +2.5 | mA |
| $\mathrm{V}_{\mathrm{o} \text { (dom) }}$ <br> (CANH) |  | Dominant output voltage at pin CANH | $\mathrm{V}_{\text {TXD }}=0 \mathrm{~V}$ | 3.0 | 3.6 | 4.25 | V |
| $V_{\text {o(dom) }}$ (CANL) |  | Dominant output voltage at pin CANL | $\mathrm{V}_{\text {TXD }}=0 \mathrm{~V}$ | 0.5 | 1.4 | 1.75 | V |
| $\begin{gathered} \mathrm{V}_{\text {(diff) }} \\ \text { (bus_dom) } \end{gathered}$ |  | Differential bus output voltage ( $\mathrm{V}_{\mathrm{CANH}}-\mathrm{V}_{\mathrm{CANL}}$ ) | $\begin{aligned} & \mathrm{V}_{T \times D}=0 \mathrm{~V} \text {; dominant; } \\ & 42.5 \Omega<\mathrm{R}_{\mathrm{LT}}<60 \Omega \end{aligned}$ | 1.5 | 2.25 | 3.0 | V |
| $V_{\text {o(dif) }}$ (bus_rec) |  | Differential bus output voltage ( $\mathrm{V}_{\text {CANH }}$ - $\mathrm{V}_{\text {CANL }}$ ) | $\mathrm{V}_{\mathrm{TXD}}=\mathrm{V}_{\mathrm{CC}}$; recessive; no load | -120 | 0 | +50 | mV |
| $\mathrm{I}_{0 \text { (sc) (CANH) }}$ |  | Short circuit output current at pin CANH | $\mathrm{V}_{\text {CANH }}=0 \mathrm{~V} ; \mathrm{V}_{\text {TXD }}=0 \mathrm{~V}$ | -45 | -70 | -120 | mA |
| $\mathrm{I}_{\mathrm{O}(\mathrm{sc})}$ (CANL) |  | Short circuit output current at pin CANL | $\begin{aligned} & \mathrm{V}_{\mathrm{CANL}}=36 \mathrm{~V} ; \mathrm{V}_{\mathrm{TXD}}= \\ & 0 \mathrm{~V} \end{aligned}$ | 45 | 70 | 120 | mA |
| $\mathrm{V}_{\text {i(dif) }}$ (th) |  | Differential receiver threshold voltage (see Figure 8) | $\begin{aligned} & -5 \mathrm{~V}<\mathrm{V}_{\mathrm{CANL}}<+12 \mathrm{~V} ; \\ & -5 \mathrm{~V}<\mathrm{V}_{\mathrm{CANH}}<+12 \mathrm{~V} ; \end{aligned}$ | 0.5 | 0.7 | 0.9 | V |
| $\mathrm{V}_{\text {ihcm }}$ (dif) (th) |  | Differential receiver threshold voltage for high common-mode (see Figure 8)) | $\begin{aligned} & -35 \mathrm{~V}<\mathrm{V}_{\mathrm{CANL}}<+35 \mathrm{~V} ; \\ & -35 \mathrm{~V}<\mathrm{V}_{\mathrm{CANH}}<+35 \mathrm{~V} ; \end{aligned}$ | 0.40 | 0.7 | 1.00 | V |
| $\mathrm{V}_{\text {( } \text { (dif) (hys) }}$ |  | Differential receiver input voltage hysteresis (see Figure 8) | $\begin{aligned} & -35 \mathrm{~V}<\mathrm{V}_{\mathrm{CANL}}<+35 \mathrm{~V} ; \\ & -35 \mathrm{~V}<\mathrm{V}_{\mathrm{CANH}}<+35 \mathrm{~V} ; \end{aligned}$ | 50 | 70 | 100 | mV |
| $\mathrm{R}_{\mathrm{i}(\mathrm{cm})}$ (CANH) |  | Common-mode input resistance at pin CANH |  | 15 | 26 | 37 | $\mathrm{k} \Omega$ |
| $\mathrm{R}_{\mathrm{i}(\mathrm{cm})}$ (CANL) |  | Common-mode input resistance at pin CANL |  | 15 | 26 | 37 | k $\Omega$ |
| $\mathrm{R}_{\mathrm{i}(\mathrm{cm})(\mathrm{m})}$ |  | Matching between pin CANH and pin CANL common mode input resistance | $\mathrm{V}_{\text {CANH }}=\mathrm{V}_{\text {CANL }}$ | -3 | 0 | +3 | \% |
| $\mathrm{R}_{\mathrm{i} \text { (dif) }}$ |  | Differential input resistance |  | 25 | 50 | 75 | k $\Omega$ |
| $\mathrm{C}_{\mathrm{i} \text { (CANH) }}$ | CANH CANL | Input capacitance at pin CANH | $\mathrm{V}_{\text {TxD }}=\mathrm{V}_{\text {CC }}$; (Note 15) |  | 7.5 | 20 | pF |
| $\mathrm{C}_{\mathrm{i}(\text { CANL) }}$ |  | Input capacitance at pin CANL | $\mathrm{V}_{\text {TXD }}=\mathrm{V}_{\text {CC }}$; ( Note 15) |  | 7.5 | 20 | pF |
| $\mathrm{C}_{\text {i(dif) }}$ |  | Differential input capacitance | $\mathrm{V}_{\text {TXD }}=\mathrm{V}_{\mathrm{CC}}$; (Note 15) |  | 3.75 | 10 | pF |

COMMON-MODE STABILIZATION

| $\mathrm{V}_{\text {SPLIT }}$ | VSPLIT | Reference output voltage at pin $\mathrm{V}_{\text {SPLIT }}$ | Normal mode; $-500 \mu \mathrm{~A}<\mathrm{I}_{\text {SPLIT }}<$ $500 \mu \mathrm{~A}$ | $\begin{aligned} & 0.3 x \\ & V_{C C} \end{aligned}$ | - | $\begin{aligned} & 0.7 x \\ & V_{C C} \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ISPLIT(i) |  | $\mathrm{V}_{\text {SPLIT }}$ leakage current | Stand-by mode | -5 |  | +5 | $\mu \mathrm{A}$ |
| ISPLIT(lim) |  | $\mathrm{V}_{\text {SPLIT }}$ limitation current | Normal mode | -3 |  | +3 | mA |

## POWER ON RESET (POR)

| PORL | POR level | CANH, CANL, V Vef in <br> tri-state below POR <br> level | 2.2 | 3.5 | 4.7 | V |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |

15. Characterization Data Only, not tested in production.

Table 9. AC PARAMETER CAN TRANSCEIVER
The AC parameters are given for $V_{C C}$ and temperature in its operating range; $T_{J}=-40$ to $+150^{\circ} \mathrm{C} ; \mathrm{R}_{\mathrm{LT}}=60 \Omega$ unless otherwise specified

| Symbol | Pin(s) | Parameter | Remark/ <br> Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: | :---: |

## TIMING CHARACTERISTICS

| $\mathrm{t}_{\text {(TxD-BUSon) }}$ | Delay TXD to bus active | $\mathrm{C}_{\mathrm{l}}=100 \mathrm{pF}$ between CANH to CANL | 40 | 85 | 105 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {(T }}$ (xD-BUSoff) | Delay TXD to bus inactive | $\mathrm{C}_{\mathrm{I}}=100 \mathrm{pF}$ between CANH to CANL | 30 | 60 | 105 | ns |
| $\mathrm{t}_{\mathrm{d} \text { (BUSon-RXD) }}$ | Delay bus active to RXD | $\mathrm{C}_{\text {rxd }}=15 \mathrm{pF}$ | 25 | 55 | 105 | ns |
| $\mathrm{t}_{\mathrm{d} \text { (BUSoff-RXD) }}$ | Delay bus inactive to RXD | $\mathrm{C}_{\mathrm{rxd}}=15 \mathrm{pF}$ | 40 | 100 | 105 | ns |
| $\mathrm{t}_{\text {pd(rec-dom) }}$ | Propagation delay TXD to RXD from recessive to dominant | $\mathrm{C}_{\mathrm{I}}=100 \mathrm{pF}$ between CANH to CANL | 90 |  | 230 | ns |
| $\mathrm{t}_{\mathrm{d} \text { (dom-rec) }}$ | Propagation delay TXD to RXD from dominant to recessive | $\mathrm{C}_{\mathrm{l}}=100 \mathrm{pF}$ between CANH to CANL | 90 |  | 245 | ns |
| $\mathrm{t}_{\mathrm{d}(\mathrm{stb} \text {-nm) }}$ | Delay standby mode to normal mode |  | 5 | 7.5 | 10 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {dbus }}$ | Dominant time for wake-up via bus |  | 0.75 | 2.5 | 5 | $\mu \mathrm{s}$ |

16. Characterization Data Only, not tested in production


Figure 7. Test Circuit for Transients


Figure 8. Hysteresis of the Receiver

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Figure 9. Test Circuit for Timing Characteristics


Figure 10. Timing Diagram for AC Characteristics


Figure 11. Basic Test Set-up for EME


Figure 12. EME Measurements

TYPICAL APPLICATION SCHEMATIC


Figure 13. Typical Application Schematic AMIS-30523

Table 10. EXTERNAL COMPONENTS LIST AND DESCRIPTION

| Component | Function | Typ Value | Tolerance | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{1}$ | $\mathrm{V}_{\mathrm{BB}}$ buffer capacitor (Note 17) | 100 | -20 +80\% | $\mu \mathrm{F}$ |
| $\mathrm{C}_{2}, \mathrm{C}_{3}$ | $V_{\text {BB }}$ decoupling block capacitor | 100 | -20 +80\% | nF |
| $\mathrm{C}_{4}$ | Charge-pump pumping capacitor | 220 | $\pm 20 \%$ | nF |
| $\mathrm{C}_{5}$ | Charge-pump buffer capacitor | 220 | $\pm 20 \%$ | nF |
| $\mathrm{C}_{6}, \mathrm{C}_{7}$ | $\mathrm{V}_{\text {DD }}$ buffer capacitor | 100 | $\pm 20 \%$ | nF |
| $\mathrm{C}_{8}$ | Low pass filter SLA | 10 | $\pm 20 \%$ | nF |
| $\mathrm{C}_{9}$ | VSPLIT decoupling capacitor | 47 | $\pm 20 \%$ | nF |
| $\mathrm{R}_{1}$ | Low pass filter SLA | 100 | $\pm 1 \%$ | $\Omega$ |
| $\mathrm{R}_{2}$ | Pull up resistor open drain DO output | 1 | $\pm 1 \%$ | $k \Omega$ |
| $\mathrm{R}_{3}, \mathrm{R}_{4}$ | Pull up resistor open drain output | 10 | $\pm 1 \%$ | $\mathrm{k} \Omega$ |
| $\mathrm{R}_{5}, \mathrm{R}_{6}$ | CAN termination resistors | 56 | $\pm 1 \%$ | $\Omega$ |
| $\mathrm{D}_{1}$ | CAN protection diode | NUP2105 |  |  |

[^1]
## FUNCTIONAL DESCRIPTION MOTOR DRIVER

## Introduction

The AMIS-30523 is a micro-stepping stepper motor driver for bipolar stepper motors embedded with an integrated CAN transceiver.

The motor driver is connected through I/O pins and a SPI interface with an external microcontroller. It has an on-chip voltage regulator, reset-output and watchdog reset, able to supply peripheral devices. It contains a current-translation table and takes the next micro-step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin. A proprietary PWM algorithm is used for reliable current control. The motor driver provides a so-called "speed and load angle" output. This allows the creation of stall detection algorithms and control loops based on load-angle to adjust torque and speed.

## H-Bridge Drivers

A full H -bridge is integrated for each of the two stator windings. Each H-bridge consists of two low-side and two high-side N-type MOSFET switches. Writing logic ' 0 ' in bit <MOTEN> disables all drivers (high-impedance). Writing logic ' 1 ' in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H -bridge switches, it is guaranteed that the top- and bottom-switches of the same half-bridge are never conductive simultaneously (interlock delay).

A two-stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate-drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (see Table 15 SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so-called "active diodes": when a current is forced trough the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain-bulk diode of the transistor.
Depending on the desired current range and the micro-step position at hand, the $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ of the low-side transistors will be adapted such that excellent current-sense accuracy is maintained. The $\mathrm{R}_{\mathrm{DS}(\text { on })}$ of the high-side transistors remain unchanged; see Table 5 DC Parameters Motor driver, for more details.

## PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H -bridge switches. The switching points of the PWM duty-cycle are synchronized to the on-chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (see Table 15 SPI Control Parameter Overview PWMJ). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor-speed or load-conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

## Automatic Forward and Slow-Fast Decay

The PWM generation is in steady-state using a combination of forward and slow-decay. The absence of fast-decay in this mode, guarantees the lowest possible current-ripple "by design". For transients to lower current levels, fast-decay is automatically activated to allow high-speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.


Figure 14. Forward and Slow/Fast Decay PWM

## Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2 * Bemf, then the duty cycle of the PWM is adapted automatically to $>50 \%$ to maintain the requested average current in the coils. This
process is completely automatic and requires no additional parameters for operation. The over-all current-ripple is divided by two if PWM frequency is doubled (see Table 15 SPI Control Parameter Overview PWMF)


## Step Translator and Step Mode

The step translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI-bits SM[2:0] (see Table 15 SPI Control Parameter Overview ) After power-on or hard reset, the coil-current translator is set to the default $1 / 32$ micro-stepping at position ' 0 '. Upon changing the step mode, the translator jumps to position $0^{*}$ of the
corresponding stepping mode. When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1 . Table 12 lists the output current vs. the translator position.

As shown in Figure 16 the output current-pairs can be projected approximately on a circle in the $\left(\mathrm{I}_{\mathrm{x}}, \mathrm{I}_{\mathrm{y}}\right)$ plane. There are, however, two exceptions: uncompensated half step and full step. In these step modes the currents are not regulated to a fraction of $\mathrm{I}_{\text {max }}$ but are in all intermediate steps regulated at $100 \%$. In the $\left(\mathrm{I}_{\mathrm{x}}, \mathrm{I}_{\mathrm{y}}\right)$ plane the current-pairs are projected on a square. Table 11 lists the output current vs. the translator position for these cases.

Table 11. SQUARE TRANSLATOR TABLE FOR FULL STEP AND UNCOMPENSATED HALF STEP

| MSP[6:0] | Stepmode ( SM[2:0] ) |  | \% of Imax |  |
| :---: | :---: | :---: | :---: | :---: |
|  | 101 | 110 | Coil x | Coil y |
|  | Uncompensated Half-Step | Full Step |  |  |
| 0000000 | 0 | - | 0 | 100 |
| 0010000 | 1 | 1 | 100 | 100 |
| 0100000 | 2 | - | 100 | 0 |
| 0110000 | 3 | 2 | 100 | -100 |
| 1000000 | 4 | - | 0 | -100 |
| 1010000 | 5 | 3 | -100 | -100 |
| 1100000 | 6 | - | -100 | 0 |
| 1110000 | 7 | 0 | -100 | 100 |



1/4th Micro Step SM[2:0] = 011


Uncompensated Half Step SM[2:0] = 101


Full Step SM[2:0] = 110

Figure 16. Translator Table: Circular and Square

Table 12. CIRCULAR TRANSLATOR TABLE

| MSP[6:0] | Stepmode (SM[2:0]) |  |  |  |  | \% of $\mathrm{I}_{\text {max }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 000 | 001 | 010 | 011 | 100 |  |  |
|  | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | Coil x | Coil y |
| 0000000 | '0' | 0* | 0* | 0* | 0* | 0 | 100 |
| 0000001 | 1 | - | - | - | - | 3.5 | 98.8 |
| 0000010 | 2 | 1 | - | - | - | 8.1 | 97.7 |
| 0000011 | 3 | - | - | - | - | 12.7 | 96.5 |
| 0000100 | 4 | 2 | 1 | - | - | 17.4 | 95.3 |
| 0000101 | 5 | - | - | - | - | 22.1 | 94.1 |
| 0000110 | 6 | 3 | - | - | - | 26.7 | 93 |
| 0000111 | 7 | - | - | - | - | 31.4 | 91.8 |
| 0001000 | 8 | 4 | 2 | 1 | - | 34.9 | 89.5 |
| 0001001 | 9 | - | - | - | - | 38.3 | 87.2 |
| 0001010 | 10 | 5 | - | - | - | 43 | 84.9 |
| 0001011 | 11 | - | - | - | - | 46.5 | 82.6 |
| 0001100 | 12 | 6 | 3 | - | - | 50 | 79 |
| 0001101 | 13 | - | - | - | - | 54.6 | 75.5 |
| 0001110 | 14 | 7 | - | - | - | 58.1 | 72.1 |
| 0001111 | 15 | - | - | - | - | 61.6 | 68.6 |
| 0010000 | 16 | 8 | 4 | 2 | 1 | 65.1 | 65.1 |
| 0010001 | 17 | - | - | - | - | 68.6 | 61.6 |
| 0010010 | 18 | 9 | - | - | - | 72.1 | 58.1 |
| 0010011 | 19 | - | - | - | - | 75.5 | 54.6 |
| 0010100 | 20 | 10 | 5 | - | - | 79 | 50 |
| 0010101 | 21 | - | - | - | - | 82.6 | 46.5 |
| 0010110 | 22 | 11 | - | - | - | 84.9 | 43 |
| 0010111 | 23 | - | - | - | - | 87.2 | 38.3 |
| 0011000 | 24 | 12 | 6 | 3 | - | 89.5 | 34.9 |
| 0011001 | 25 | - | - | - | - | 91.8 | 31.4 |
| 0011010 | 26 | 13 | - | - | - | 93 | 26.7 |
| 0011011 | 27 | - | - | - | - | 94.1 | 22.1 |
| 0011100 | 28 | 14 | 7 | - | - | 95.3 | 17.4 |
| 0011101 | 29 | - | - | - | - | 96.5 | 12.7 |
| 0011110 | 30 | 15 | - | - | - | 97.7 | 8.1 |
| 0011111 | 31 | - | - | - | - | 98.8 | 3.5 |
| 0100000 | 32 | 16 | 8 | 4 | 2 | 100 | 0 |
| 0100001 | 33 | - | - | - | - | 98.8 | -3.5 |
| 0100010 | 34 | 17 | - | - | - | 97.7 | -8.1 |
| 0100011 | 35 | - | - | - | - | 96.5 | -12.7 |
| 0100100 | 36 | 18 | 9 | - | - | 95.3 | -17.4 |
| 0100101 | 37 | - | - | - | - | 94.1 | -22.1 |
| 0100110 | 38 | 19 | - | - | - | 93 | -26.7 |
| 0100111 | 39 | - | - | - | - | 91.8 | -31.4 |
| 0101000 | 40 | 20 | 10 | 5 | - | 89.5 | -34.9 |
| 0101001 | 41 | - | - | - | - | 87.2 | -38.3 |
| 0101010 | 42 | 21 | - | - | - | 84.9 | -43 |
| 0101011 | 43 | - | - | - | - | 82.6 | -46.5 |
| 0101100 | 44 | 22 | 11 | - | - | 79 | -50 |
| 0101101 | 45 | - | - | - | - | 75.5 | -54.6 |
| 0101110 | 46 | 23 | - | - | - | 72.1 | -58.1 |
| 0101111 | 47 | - | - | - | - | 68.6 | -61.6 |
| 0110000 | 48 | 24 | 12 | 6 | 3 | 65.1 | -65.1 |
| 0110001 | 49 | - | - | - | - | 61.6 | -68.6 |
| 0110010 | 50 | 25 | - | - | - | 58.1 | -72.1 |
| 0110011 | 51 | - | - | - | - | 54.6 | -75.5 |
| 0110100 | 52 | 26 | 13 | - | - | 50 | -79 |
| 0110101 | 53 | - | - | - | - | 46.5 | -82.6 |
| 0110110 | 54 | 27 | - | - | - | 43 | -84.9 |
| 0110111 | 55 | - | - | - | - | 38.3 | -87.2 |
| 0111000 | 56 | 28 | 14 | 7 | - | 34.9 | -89.5 |
| 0111001 | 57 | - | - | - | - | 31.4 | -91.8 |
| 0111010 | 58 | 29 | - | - | - | 26.7 | -93 |
| 0111011 | 59 | - | - | - | - | 22.1 | -94.1 |
| 0111100 | 60 | 30 | 15 | - | - | 17.4 | -95.3 |
| 0111101 | 61 | - | - | - | - | 12.7 | -96.5 |
| 0111110 | 62 | 31 | - | - | - | 8.1 | -97.7 |
| 0111111 | 63 | - | - | - | - | 3.5 | -98.8 |

Table 12. CIRCULAR TRANSLATOR TABLE

| MSP[6:0] | Stepmode ( SM[2:0] ) |  |  |  |  | \% of Imax |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 000 | 001 | 010 | 011 | 100 | Coil $x$ | Coil y |
|  | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 |  |  |
| 1000000 | 64 | 32 | 16 | 8 | 4 | 0 | -100 |
| 1000001 | 65 | - | - | - | - | -3.5 | -98.8 |
| 1000010 | 66 | 33 | - | - | - | -8.1 | -97.7 |
| 1000011 | 67 | - | - | - | - | -12.7 | -96.5 |
| 1000100 | 68 | 34 | 17 | - | - | -17.4 | -95.3 |
| 1000101 | 69 | - | - | - | - | -22.1 | -94.1 |
| 1000110 | 70 | 35 | - | - | - | -26.7 | -93 |
| 1000111 | 71 | - | - | - | - | -31.4 | -91.8 |
| 1001000 | 72 | 36 | 18 | 9 | - | -34.9 | -89.5 |
| 1001001 | 73 | - | - | - | - | -38.3 | -87.2 |
| 1001010 | 74 | 37 | - | - | - | -43 | -84.9 |
| 1001011 | 75 | - | - | - | - | -46.5 | -82.6 |
| 1001100 | 76 | 38 | 19 | - | - | -50 | -79 |
| 1001101 | 77 | - | - | - | - | -54.6 | -75.5 |
| 1001110 | 78 | 39 | - | - | - | -58.1 | -72.1 |
| 1001111 | 79 | - | - | - | - | -61.6 | -68.6 |
| 1010000 | 80 | 40 | 20 | 10 | 5 | -65.1 | -65.1 |
| 1010001 | 81 | - | - | - | - | -68.6 | -61.6 |
| 1010010 | 82 | 41 | - | - | - | -72.1 | -58.1 |
| 1010011 | 83 | - | - | - | - | -75.5 | -54.6 |
| 1010100 | 84 | 42 | 21 | - | - | -79 | -50 |
| 1010101 | 85 | - | - | - | - | -82.6 | -46.5 |
| 1010110 | 86 | 43 | - | - | - | -84.9 | -43 |
| 1010111 | 87 | - | - | - | - | -87.2 | -38.3 |
| 1011000 | 88 | 44 | 22 | 11 | - | -89.5 | -34.9 |
| 1011001 | 89 | - | - | - | - | -91.8 | -31.4 |
| 1011010 | 90 | 45 | - | - | - | -93 | -26.7 |
| 1011011 | 91 | - | - | - | - | -94.1 | -22.1 |
| 1011100 | 92 | 46 | 23 | - | - | -95.3 | -17.4 |
| 1011101 | 93 | - | - | - | - | -96.5 | -12.7 |
| 1011110 | 94 | 47 | - | - | - | -97.7 | -8.1 |
| 1011111 | 95 | - | - | - | - | -98.8 | -3.5 |
| 1100000 | 96 | 48 | 24 | 12 | 6 | -100 | 0 |
| 1100001 | 97 | - | - | - | - | -98.8 | 3.5 |
| 1100010 | 98 | 49 | - | - | - | -97.7 | 8.1 |
| 1100011 | 99 | - | - | - | - | -96.5 | 12.7 |
| 1100100 | 100 | 50 | 25 | - | - | -95.3 | 17.4 |
| 1100101 | 101 | - | - | - | - | -94.1 | 22.1 |
| 1100110 | 102 | 51 | - | - | - | -93 | 26.7 |
| 1100111 | 103 | - | - | - | - | -91.8 | 31.4 |
| 1101000 | 104 | 52 | 26 | 13 | - | -89.5 | 34.9 |
| 1101001 | 105 | - | - | - | - | -87.2 | 38.3 |
| 1101010 | 106 | 53 | - | - | - | -84.9 | 43 |
| 1101011 | 107 | - | - | - | - | -82.6 | 46.5 |
| 1101100 | 108 | 54 | 27 | - | - | -79 | 50 |
| 1101101 | 109 | - | - | - | - | -75.5 | 54.6 |
| 1101110 | 110 | 55 | - | - | - | -72.1 | 58.1 |
| 1101111 | 111 | - | - | - | - | -68.6 | 61.6 |
| 1110000 | 112 | 56 | 28 | 14 | 7 | -65.1 | 65.1 |
| 1110001 | 113 | - | - | - | - | -61.6 | 68.6 |
| 1110010 | 114 | 57 | - | - | - | -58.1 | 72.1 |
| 1110011 | 115 | - | - | - | - | -54.6 | 75.5 |
| 1110100 | 116 | 58 | 29 | - | - | -50 | 79 |
| 1110101 | 117 | - | - | - | - | -46.5 | 82.6 |
| 1110110 | 118 | 59 | - | - | - | -43 | 84.9 |
| 1110111 | 119 | - | - | - | - | -38.3 | 87.2 |
| 1111000 | 120 | 60 | 30 | 15 | - | -34.9 | 89.5 |
| 1111001 | 121 | - | - | - | - | -31.4 | 91.8 |
| 1111010 | 122 | 61 | - | - | - | -26.7 | 93 |
| 1111011 | 123 | - | - | - | - | -22.1 | 94.1 |
| 1111100 | 124 | 62 | 31 | - | - | -17.4 | 95.3 |
| 1111101 | 125 | - | - | - | - | -12.7 | 96.5 |
| 1111110 | 126 | 63 | - | - | - | -8.1 | 97.7 |
| 1111111 | 127 | - | - | - | - | -3.5 | 98.8 |

## Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI-controlled direction bit <DIRCTRL>. (see Table 15 SPI Control Parameter Overview)

## NXT input

Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled). Depending on the NXT-polarity bit <NXTP> (see Table 15 SPI Control Parameter Overview), the next step is initiated either on the rising edge or the falling edge of the NXT input.

## Translator Position

The translator position MSP[6:0] can be read in SPI Status Register 3 (See Table 18 SPI Status Registers). This is a 7 -bit number equivalent to the $1 / 32^{\text {th }}$ micro-step from Table 12 "Circular Translator Table". The translator position is updated immediately following a NXT trigger.

## Synchronization of Step Mode and NXT Input

When step mode is re-programmed to another resolution (Figure 18), then this is put in effect immediately upon the first arriving "NXT" input. If the micro-stepping resolution is increased, the coil currents will be regulated to the nearest micro-step, according to the fixed grid of the increased resolution. If however the micro-stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro-step translator table.
If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro-stepping is proceeds according to the translator table.
If the translator position is not shared both by the old and new resolution setting, then the micro-stepping proceeds with an offset relative to the translator table (See Figure 18 right hand side).

More information can be found in application note AND8399/D.


Figure 17. Translator Position Timing Diagram


Figure 18. NXT-Step-Mode Synchronization
Left: change from lower to higher resolution. The left-hand side depicts the ending half-step position during which a new step mode resolution was programmed. The right-hand side diagram shows the effect of subsequent NXT commands on the micro-step position.

Right: change from higher to lower resolution. The left-hand side depicts the ending micro-step position during which a new step mode resolution was programmed. The right-hand side diagram shows the effect of subsequent NXT commands on the half-step position.

NOTE: It is advised to reduce the micro-stepping resolution only at micro-step positions that overlap with desired micro-step positions of the new resolution.

## Programmable Peak-Current

The amplitude of the current waveform in the motor coils (coil peak current $=\mathrm{I}_{\max }$ ) is adjusted by means of an SPI parameter "CUR[4:0]" (see Table 15 SPI Control Parameter

Overview). Whenever this parameter is changed, the coil-currents will be updated immediately at the next PWM period. Figure 19 presents the Peak-Current and Current Ratings in conjunction to the Current setting CUR[4:0].


Figure 19. Programmable Peak-Current Overview

## Speed and Load Angle Output

The SLA-pin provides an output voltage that indicates the level of the Back-e.m.f. voltage of the motor. This Back-e.m.f. voltage is sampled during every so-called "coil
current zero crossings". Per coil, two zero-current positions exist per electrical period, yielding in total four zero-current observation points per electrical period.


Figure 20. Principle of Bemf Measurement

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage $\mathrm{V}_{\text {COIL }}$ shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see "SLA-transparency" in Table 15 SPI Control Parameter Overview). The SLA pin shows in "transparent mode" full visibility of the voltage transient behavior. This allows a sanity-check of the speed-setting versus motor operation and characteristics and supply voltage levels. If the bit "SLAT" is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA-pin. Because the transient behavior of the coil voltage is not visible anymore, this mode
generates smoother Back e.m.f. input for post-processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level ( 0 to 5 V ), the sampled coil voltage $\mathrm{V}_{\text {COIL }}$ is divided by 2 or by 4 . This divider is set through an SPI bit <SLAG> (see Table 15 SPI Control Parameter Overview).
The following drawing illustrates the operation of the SLA-pin and the transparency-bit. "PWMsh" and "I $I_{\text {coil }}=0 "$ are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.
More information can be found in application note AND8399/D.


Figure 21. Timing Diagram of SLA-Pin

## Warning, Error Detection and Diagnostics Feedback

## Thermal Warning and Shutdown

When junction temperature rises above $\mathrm{T}_{\mathrm{TW}}$, the thermal warning bit <TW> is set (Table 17 SPI Status registers Address SR0). If junction temperature increases above thermal shutdown level, then the circuit goes in "Thermal Shutdown" mode (<TSD>) and all driver transistors are disabled (high impedance) (see Table 17 SPI Status registers Address SR2). The conditions to reset flag <TSD> is to be at a temperature lower than $\mathrm{T}_{\mathrm{TW}}$ and to clear the $<\mathrm{TSD}>$ flag reading out Status Register 2.

## Over-Current Detection

The over-current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over-current detection threshold, then the over-current flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit in (see Table 17 SPI Status registers Address SR1 and SR2: <OVCXij> and <OVCYij>). Error condition is latched and the microcontroller needs to clear the status bits (by reading Status Register 1 or 2 ) to reactivate the drivers.

Note: Successive reading the SPI StatusRegisters 1 and 2 in case of a short circuit condition, may lead to damage to the drivers

## Open Coil/Current Not Reached Detection

Open coil detection is based on the observation of $100 \%$ duty cycle of the PWM regulator. If in a coil $100 \%$ duty cycle is detected for longer than 200 ms then the related driver transistors are disabled (high-impedance) and an appropriate bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 17 SPI Status Register Address SR0)

When the resistance of a motor coil is very large and the supply voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be $100 \%$ and after 200 ms the error pin and <OPENX>, <OPENY> will flag this situation (motor current is kept alive). This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil-current or else the coil current should be reduced.

## Charge Pump Failure

The charge pump is an important circuit that guarantees low $\mathrm{R}_{\mathrm{DS}(\text { on })}$ for all drivers, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee $\mathrm{R}_{\mathrm{DS}(\text { on })}$ of the drivers, then the bit <CPFAIL> is set in Table 17. Also after POR the charge pump voltage will need some time to exceed
the required threshold. During that time $\mathrm{t}_{\mathrm{CPU}}<\mathrm{CPFAIL}>$ will be set to " 1 ".

## Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

$$
\begin{aligned}
& \text { NOT(ERRB) }=\text { <TW> OR <TSD> OR <OVCXij> OR } \\
& \text { < OVCYij> OR <OPENi> OR <CPFAIL> }
\end{aligned}
$$

This open drain output can be wired OR-ed with error outputs other motor drivers.

## Logic Supply Regulator

AMIS-30523 has an on-chip 5 V low-drop regulator with external capacitor to supply the digital part of the chip, some low-voltage analog blocks and external circuitry. The voltage level is derived from an internal bandgap reference. To calculate the available drive-current for external circuitry, the specified $\mathrm{I}_{\text {load }}$ should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 5 DC parameters Motor Driver.

## Power-On Reset (POR) Function

The open drain output pin PORB/WD provides an "active low" reset for external purposes. At power-up of AMIS-30523, this pin will be kept low for some time to reset for example an external microcontroller. A small analogue filter avoids resetting due to spikes or noise on the $\mathrm{V}_{\mathrm{DD}}$ supply.


Figure 22. Power-on-Reset Timing Diagram

## Watchdog Function

The watchdog function is enabled/disabled through <WDEN> bit (See Table 15 SPI Control Registers address 00 h ). Once this bit has been set to " 1 " (watchdog enable), the microcontroller needs to re-write this bit to clear an internal timer before the watchdog timeout interval expires. In case
the timer is activated and WDEN is acknowledged too early (before $t_{\text {WDPR }}$ ) or not within the interval (after $t_{\text {WDTO }}$ ), then a reset of the microcontroller will occur through PORB/WD pin. In addition, a warm/cold boot bit <WD> is available in Table 17 for further processing when the external microcontroller is alive again. See Figure 23.


Figure 23. Watchdog Timing Diagram
NOTE: $\quad t_{D S P I}$ is the time needed by the external microcontroller to shift-in the <WDEN> bit after a power-up.
The duration of the watchdog timeout interval is programmable through the WDT[3:0] bits (See Table 14 SPI Control Registers address 00h). The timing is given in Table 13 below.

Table 13. WATCHDOG TIMEOUT INTERVAL AS FUNCTION OF WDT[3.0]

| Index | WDT[3:0] |  |  |  | $\mathbf{t}_{\text {WDTO }}$ (ms) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 32 |
| 1 | 0 | 0 | 0 | 1 | 64 |
| 2 | 0 | 0 | 1 | 0 | 96 |
| 3 | 0 | 0 | 1 | 1 | 128 |
| 4 | 0 | 1 | 0 | 0 | 160 |
| 5 | 0 | 1 | 0 | 1 | 192 |
| 6 | 0 | 1 | 1 | 0 | 224 |
| 7 | 0 | 1 | 1 | 1 | 256 |
| 8 | 1 | 0 | 0 | 0 | 288 |
| 9 | 1 | 0 | 0 | 1 | 320 |
| A | 1 | 0 | 1 | 0 | 352 |
| B | 1 | 0 | 1 | 1 | 384 |
| C | 1 | 1 | 0 | 0 | 416 |
| D | 1 | 1 | 0 | 1 | 448 |
| E | 1 | 1 | 1 | 0 | 480 |
| F | 1 | 1 | 1 | 1 | 512 |

## CLR Pin (= Hard Reset)

Logic 0 on CLR pin allows normal operation of the chip. To reset the complete digital inside AMIS-30523, the input CLR needs to be pulled to logic 1 during minimum time given by tCLR. (See Table 6 AC Parameters Motor Driver). This reset function clears all internal registers without the need of a power-cycle, except in sleep mode. The operation of all analog circuits is depending on the reset state of the
digital, charge pump remains active. Logic 0 on CLR pin resumes normal operation again.

The voltage regulator remains functional during and after the reset and the PORB/WD pin is not activated. Watchdog function is reset completely.

## Sleep Mode

The bit <SLP> in SPI Control Register 2 (See Table 14 SPI Control Registers address 03 h ) is provided to enter a so-called "sleep mode". This mode allows reduction of current-consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low-power mode
- All internal registers are maintaining their logic content
- NXT and DIR inputs are forbidden
- SPI communication remains possible (slight current increase during SPI communication)
- Oscillator and digital clocks are silent, except during SPI communication
The voltage regulator remains active but with reduced current-output capability ( $\mathrm{I}_{\text {LOADSLP }}$ ). The watchdog timer stops running and it's value is kept in the counter. Upon leaving sleep mode, this timer continues from the value it had before entering sleep mode.

Normal operation is resumed after writing logic ' 0 ' to bit <SLP>. A start-up time is needed for the charge pump to stabilize. After this time, (tcpu) NXT commands can be issued.

## SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS-30523. The implemented SPI block is designed to interface directly with numerous micro-controllers from several manufacturers. AMIS-30523 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

## SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI).

DO signal is the output from the Slave (AMIS-30523), and DI signal is the output from the Master. A chip select line (CSB) allows individual selection of a Slave SPI device in a multiple-slave system. The CSB line is active low. If AMIS-30523 is not selected, DO is pulled up with the external pull up resistor. Since AMIS-30523 operates as a Slave in MODE $0(\mathrm{CPOL}=0 ; \mathrm{CPHA}=0)$ it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.


Figure 24. Timing Diagram of a SPI Transfer
NOTE: At the falling edge of the eighth clock pulse the data-out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the AMIS-30523 system clock when $\overline{\mathrm{CS}}=\mathrm{High}$.

## Transfer Packet:

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.


Figure 25. SPI Transfer Packet

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS-30523 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS-30523 in a READ operation.

Two command types can be distinguished in the communication between master and AMIS-30523:

- READ from SPI Register with address ADDR[4:0]:

CMD2 = "0"

- WRITE to SPI Register with address ADDR[4:0]: CMD2 = " 1 "


## READ Operation

If the Master wants to read data from Status or Control Registers, it initiates the communication by sending a READ command. This READ command contains the
address of the SPI register to be read out. At the falling edge of the eight clock pulse the data-out shift register is updated with the content of the corresponding internal SPI register. In the next 8-bit clock pulse train this data is shifted out via DO pin. At the same time the data shifted in from DI (Master) should be interpreted as the following successive command or dummy data.


Figure 26. Single READ Operation where DATA from SPI Register with Address 1 is Read by the Master

All 4 Status Registers (see Table 17 SPI Registers) contain 7 data bits and a parity check bit The most significant bit (D7) represents a parity of $\mathrm{D}[6: 0]$. If the number of logical ones in $\mathrm{D}[6: 0]$ is odd, the parity bit D 7 equals " 1 ". If the number of logical ones in $\mathrm{D}[6: 0]$ is even then the parity bit D7 equals " 0 ". This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

Also the Control Registers can be read out following the same routine. Control Registers don't have a parity check.

The CSB line is active low and may remain low between successive READ commands as illustrated in Figure 28. There is however one exception. In case an error condition is latched in one of Status Registers (see Table 17 SPI Registers) the ERRB pin is activated. (See the Error Output section). This signal flags a problem to the external microcontroller. By reading the Status Registers information about the root cause of the problem can be determined. After this READ operation the Status Registers are cleared. Because the Status Registers and ERRB pin (see SPI Registers) are only updated by the internal system clock when the CSB line is high, the Master should force CSB high
immediately after the READ operation. For the same reason it is recommended to keep the CSB line high always when the SPI bus is idle.

## WRITE Operation

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after CSB goes from low to high! AMIS-30523 responds on every incoming byte by shifting out via DO the data stored in the last received address.

It is important that the writing action (command - address and data) to the Control Register is exactly 16 bits long. If more or less bits are transmitted the complete transfer packet is ignored (with the exception of preceding read commands (see Figure 28)).

A WRITE command executed for a read-only register (e.g. Status Registers) will not affect the addressed register and the device operation.

Because after a power-on-reset the initial address is unknown the data shifted out via DO is not valid.


Figure 27. Single WRITE Operation where DATA from the Master is Written in SPI Register with Address 3

## Examples of Combined READ and WRITE Operations

In the following examples successive READ and WRITE operations are combined. In Figure 28 the Master first reads the status from Register at ADDR4 and at ADDR5 followed
by writing a control byte in Control Register at ADDR2. Note that during the write command the old data of the pointed register is returned at the moment the new data is shifted in


Figure 28. Two Successive READ Commands Followed by a WRITE Command
After the write operation the Master could initiate a read back command in order to verify the data correctly written as illustrated in Figure 29. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is


Figure 29. A WRITE Operation where DATA from the Master is Written in SPI Register with Address 2 Followed by a READ Back Operation to Verify a Correct WRITE Operation

NOTE: The internal data-out shift buffer of the AMIS-30523 is updated with the content of the selected SPI register only at the last (every eighth) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

Table 14. SPI CONTROL REGISTERS (All SPI control registers have Read/Write Access and default to "0" after power-on or hard reset.)

| Address | Content | Structure |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|  | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WR (00h) | Data | WDEN | WDT[3:0] |  |  |  | - | - | - |
| CR0 (01h) | Data | SM[2:0] |  |  | CUR[4:0] |  |  |  |  |
| CR1 (02h) | Data | DIRCTRL | NXTP | - | - | PWMF | PWMJ | EMC[1:0] |  |
| CR2 (03h) | Data | MOTEN | SLP | SLAG | SLAT | - | - | - | - |

## Where:

R/W
Read and Write access
Reset: $\quad$ Status after power-On or hard reset

Table 15. SPI CONTROL PARAMETER OVERVIEW

| Symbol | Description | Status |  | Value |
| :---: | :---: | :---: | :---: | :---: |
| DIRCTRL | Controls the direction of rotation (in combination with logic level on input DIR) | <DIR> $=0$ | <DIRCTRL> $=0$ | CW motion |
|  |  |  | <DIRCTRL> = 1 | CCW motion |
|  |  | <DIR> = 1 | <DIRCTRL> $=0$ | CCW motion |
|  |  |  | <DIRCTRL> = 1 | CW motion |
| NXTP | Selects if NXT triggers on rising or falling edge | <NXTP> = 0 | Trigger on rising edge |  |
|  |  | <NXTP> = 1 | Trigger on falling edge |  |
| EMC[1:0] | Turn On - Turn-off Slopes of motor driver (Note 18) | 00 | Very Fast |  |
|  |  | 01 | Fast |  |
|  |  | 10 | Slow |  |
|  |  | 11 | Very Slow |  |
| SLAT | Speed load angle transparency bit | <SLAT> = 0 | SLA is transparent |  |
|  |  | <SLAT> = 1 | SLA is NOT transparent |  |
| SLAG | Speed load angle gain setting | <SLAG> $=0$ | Gain $=0.5$ |  |
|  |  | <SLAG> = 1 | Gain $=0.25$ |  |
| PWMF | Enables doubling of the PWM frequency (Note 18) | <PWMF> = 0 | Default Frequency |  |
|  |  | <PWMF> = 1 | Double Frequency |  |
| PWMJ | Enables jittery PWM | <PWMJ> = 0 | Jitter disabled |  |
|  |  | <PWMJ> = 1 | Jitter enabled |  |
| SM[2:0] | Stepmode | 000 | 1/32 Micro - Step |  |
|  |  | 001 | 1/16 Micro - Step |  |
|  |  | 010 | 1/8 Micro - Step |  |
|  |  | 011 | 1/4 Micro - Step |  |
|  |  | 100 | Compensated Half Step |  |
|  |  | 101 | Uncompensated Half Step |  |
|  |  | 110 | Full Step |  |
|  |  | 111 | n.a. |  |
| SLP | Enables sleep mode | <SLP> $=0$ | Active mode |  |
|  |  | <SLP> = 1 | Sleep mode |  |
| MOTEN | Activates the motor driver outputs | <MOTEN> = 0 | Drivers disabled |  |
|  |  | <MOTEN> = 1 | Drivers enabled |  |

18. The typical values can be found in Table 5: DC Parameters Motor Driver and in Table 6: AC parameters Motor Driver

CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

Table 16. SPI CONTROL PARAMETER OVERVIEW CUR[4:0]

19. Typical current amplitude at $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$
20. Reducing the current over different current ranges might trigger overcurrent detection. See application note AND8372/D for solutions.

## SPI Status Register Description

All 4 SPI status registers have Read Access and are default to " 0 " after power-on or hard reset.

Table 17. SPI STATUS REGISTERS

| Address | Content | Structure |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|  | Access | R | R | R | R | R | R | R | R |
|  | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SR0 (04h) | Data is not latched | PAR | TW | CPfail | WD | OPENX | OPENY | - | - |
| SR1 (05h) | Data is latched | PAR | OVCXPT | OVCXPB | OVCXNT | OVCXNB | - | - | - |
| SR2 (06h) | Data is latched | PAR | OVCYPT | OVCYPB | OVCYYNT | OVCYNB | TSD | - | - |
| SR3 (07h) | Data is not latched | PAR | MSP[6:0] |  |  |  |  |  |  |

Where:

| R | Read only mode access |
| :--- | :--- |
| Reset | Status after power-on or hard reset |
| PAR | Parity check |

Table 18. SPI STATUS FLAGS OVERVIEW

| Mnemonic | Flag | Length (bit) | Related SPI Register | Comment | Reset State |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CPFail | Charge pump failure | 1 | Status Register 0 | ' 0 ' = no failure <br> ' 1 ' = failure: indicates that the charge pump <br> does not reach the required voltage level. | '0' |
| MSP[6:0] | Micro-step position | 7 | Status Register 3 | Translator micro step position | '0000000' |
| OPENX | OPEN Coil X | 1 | Status Register 0 | '1' = Open coil detected | '0' |
| OPENY | OPEN Coil $Y$ | 1 | Status Register 0 | ' 1 ' = Open coil detected | '0' |
| OVCXNB | OVer Current on X H-bridge; MOTXN terminal; Bottom tran. | 1 | Status Register 1 | ' 0 ' = no failure <br> ' 1 ' = failure: indicates that over current is detected at bottom transistor XN-terminal | '0' |
| OVCXNT | OVer Current on X H-bridge; MOTXN terminal; Top transist. | 1 | Status Register 1 | ' 0 ' = no failure <br> ' 1 ' = failure: indicates that over current is detected at top transistor XN-terminal | '0' |
| OVCXPB | OVer Current on X H-bridge; MOTXP terminal; Bottom transist. | 1 | Status Register 1 | $\begin{aligned} & \text { ' } 0 \text { ' = no failure } \\ & \text { ' } 1 \text { ' = failure: indicates that over current is } \\ & \text { detected at bottom transistor XP-terminal } \end{aligned}$ | '0' |
| OVCXPT | OVer Current on X H-bridge; MOTXP terminal; Top transist. | 1 | Status Register 1 | ' 0 ' = no failure <br> ' 1 ' = failure: indicates that over current is detected at top transistor XP-terminal | '0' |
| OVCYNB | OVer Current on Y H-bridge; MOTYN terminal; Bottom transist. | 1 | Status Register 2 | $\text { ' } 0 \text { ' = no failure }$ <br> ' 1 ' = failure: indicates that over current is detected at bottom transistor YN -terminal | '0' |
| OVCYNT | OVer Current on Y H-bridge; MOTYN terminal; Top transist. | 1 | Status Register 2 | $\begin{aligned} & \text { ' } 0 \text { ' = no failure } \\ & \text { ' } 1 \text { ' = failure: indicates that over current is } \\ & \text { detected at top transistor YN-terminal } \end{aligned}$ | '0' |
| OVCYPB | OVer Current on Y H-bridge; MOTYP terminal; Bottom transist. | 1 | Status Register 2 | ' 0 ' = no failure <br> ' 1 ' = failure: indicates that over current is detected at bottom transistor YP-terminal | '0' |
| OVCYPT | OVer Current on Y H-bridge; MOTYP terminal; Top transist. | 1 | Status Register 2 | ' 0 ' = no failure <br> ' 1 ' = failure: indicates that over current is detected at top transistor YP-terminal | '0' |
| TSD | Thermal shutdown | 1 | Status Register 2 |  | '0' |
| TW | Thermal warning | 1 | Status Register 0 |  | '0' |
| WD | Watchdog event (Note 21) | 1 | Status Register 0 | ' 1 ' = watchdog reset after time-out | '0' |

21.WD - This bit indicates that the watchdog timer has not been cleared properly. If the master reads that WD is set to " 1 " after reset, it means that a watchdog reset occurred (warm boot) instead of POR (cold boot). WD bit will be cleared only when the master writes " 0 " to WDEN bit.

## FUNCTIONAL DESCRIPTION CAN TRANSCEIVER

## Introduction

The CAN transceiver is the interface between a (CAN) protocol controller and the physical bus. It provides differential transmit capability to the bus and differential receive capability to the CAN controller. Due to the wide common-mode voltage range of the receiver inputs, it is able to reach outstanding levels of electro-magnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Additional features are the ideal passive behavior when the supply voltage is removed; a wake-up over bus and the extreme low current in stand-by mode.

To cope with the long bus delay the communication speed needs to be low. The integrated transceiver allows low transmit data rates down $10 \mathrm{kbit} / \mathrm{s}$ or lower.

## Operating Modes

The CAN transceiver provides two modes of operation as illustrated in Table 19. These modes are selectable through pin STB

Table 19. OPERATING MODES

| Mode |  | RXD |  |
| :---: | :---: | :---: | :---: |
|  | STB | Low | High |
| Normal | Low | Bus <br> dominant | Bus <br> recessive |
| Standby | High | Wake-up <br> request <br> detected | No <br> wake-up <br> request <br> detected |

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

In stand-by mode both the transmitter and receiver are disabled and a very low-power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically $10 \mu \mathrm{~A}$. When a wake-up request is detected by the low-power differential receiver, the signal is first filtered and then verified as a valid wake signal after
a time period of $t_{\text {BUS }}$, the RxD pin is driven low by the transceiver to inform the controller of the wake-up request.

## Split Circuit

The VSPLIT pin is operational only in normal mode. In standby mode this pin is floating. The $\mathrm{V}_{\text {SPLIT }}$ is connected as shown in Figure 13 and its purpose is to provide a stabilized DC voltage of $0.5 \times \mathrm{V}_{\mathrm{CC}}$ to the bus avoiding possible steps in the common-mode signal therefore reducing EME. These unwanted steps could be caused by an un-powered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal $0.5 \mathrm{x} \mathrm{V}_{\mathrm{CC}}$ voltage.

## Wake-up

Once a valid wake-up (dominant state longer than $\mathrm{t}_{\mathrm{BUS}}$ ) has been received during the standby mode the RxD pin is driven low

## Over-Temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately $160^{\circ} \mathrm{C}$. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

## High Communication Speed Range

The transceiver is primarily intended for industrial applications. It allows very low baud rates needed for long bus length applications. But also high speed communication is possible up to $1 \mathrm{Mbit} / \mathrm{s}$.

## Fail Safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.
The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 7). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the $\mathrm{V}_{\mathrm{CC}}$ supply be removed.

## DEVICE ORDERING INFORMATION

| Part Number | Temperature <br> Range | Peak <br> Current | Package Type | Shipping $^{\dagger}$ |
| :--- | :---: | :---: | :---: | :---: |
| AMIS30523C5231RG | $-40^{\circ} \mathrm{C}-125^{\circ} \mathrm{C}$ | 1600 mA | QFN-52 <br> $(\mathrm{Pb}-\mathrm{Free})$ | Tape \& Reel |
| AMIS30523C5231G | $-40^{\circ} \mathrm{C}-125^{\circ} \mathrm{C}$ | 1600 mA | QFN-52 <br> $(\mathrm{Pb}-\mathrm{Free})$ | Tube |

[^2]
## PACKAGE DIMENSIONS

QFN52 8x8, 0.5P
CASE 485M-01
ISSUE C


[^3]
## PUBLICATION ORDERING INFORMATION

## LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
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[^0]:    Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

    1. For limited time $<0.5 \mathrm{~s}$.
    2. For $0<\mathrm{V}_{\mathrm{CC}}<5.25 \mathrm{~V}$ unlimited time
    3. Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b.
    4. Circuit functionality not guaranteed.
    5. Standardized Human body model ( 100 pF via $1.5 \mathrm{k} \Omega$, according to JEDEC EIA-JESD22-A114-B).
    6. Standardized human body model electrostatic discharge (ESD) pulses ( 100 pF via $1.5 \mathrm{k} \Omega$ ) stressed pin to ground.
    7. Standardized charged device model ESD pulses when tested according to ESD STM5.3.1-1999.
[^1]:    17. Low ESR < $1 \Omega$.
[^2]:    $\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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