

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D $T_A = +25^\circ C$
50V	2.0Ω @ $V_{GS} = 10V$	360mA
	3.0Ω @ $V_{GS} = 5V$	250mA

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

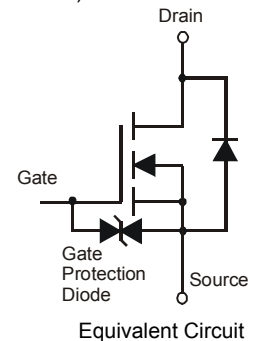
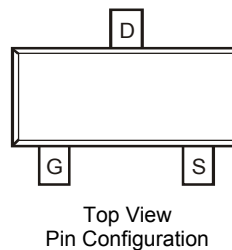
- DC-DC Converters
- Power management functions
- Battery Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc

Features

- N-Channel MOSFET
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT323
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 ^{Ⓔ3}
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)

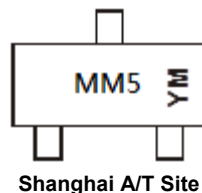


Ordering Information (Note 4)

Part Number	Case	Packaging
DMN53D0LW-7	SOT323	3,000/Tape & Reel
DMN53D0LW-13	SOT323	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



MM5 = Product Type Marking Code
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 Y = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	50	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C	I _D	360	mA
		T _A = +70°C		250	
Continuous Drain Current (Note 6) V _{GS} = 5V	Steady State	T _A = +25°C	I _D	250	mA
		T _A = +70°C		200	
Pulsed Drain Current (10μs pulse, duty cycle = 1%)			I _{DM}	700	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation	(Note 5)	P _D	320	mW
	(Note 6)		420	
Thermal Resistance, Junction to Ambient	(Note 5)	R _{θJA}	395	°C/W
	(Note 6)		301	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	50	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1.0	μA	V _{DS} = 50V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.8	—	1.5	V	V _{DS} = V _{GS} , I _D = 100μA
Gate Threshold Voltage Temperature Coefficient (Note 8)	$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	—	-3.4	—	mV/°C	—
Static Drain-Source On-Resistance	R _{DS(on)}	—	—	2.0	Ω	V _{GS} = 10V, I _D = 270mA
		—	—	3.0		V _{GS} = 5V, I _D = 200mA
Forward Transconductance	g _{FS}	80	—	—	mS	V _{DS} = 10V, I _D = 200mA
Diode Forward Voltage	V _{SD}	—	0.75	1.2	V	V _{GS} = 0V, I _S = 115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	45.8	—	pF	V _{DS} = 25V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	5.3	—		
Reverse Transfer Capacitance	C _{rss}	—	3.9	—		
Total Gate Charge V _{GS} = 10V	Q _g	—	1.2	—	nC	V _{GS} = 10V, V _{DS} = 10V, I _D = 250mA
Total Gate Charge V _{GS} = 4.5V	Q _g	—	0.6	—		
Gate-Source Charge	Q _{gs}	—	0.2	—		
Gate-Drain Charge	Q _{gd}	—	0.1	—		
Turn-On Delay Time	t _{D(on)}	—	2.7	—	nS	V _{DD} = 30V, V _{GS} = 10V, R _G = 25Ω, I _D = 200mA
Turn-On Rise Time	t _r	—	2.5	—		
Turn-Off Delay Time	t _{D(off)}	—	18.9	—		
Turn-Off Fall Time	t _f	—	11.0	—		

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
 7. Short duration pulse test used to minimize self-heating effect.
 8. Guaranteed by design. Not subject to production testing.

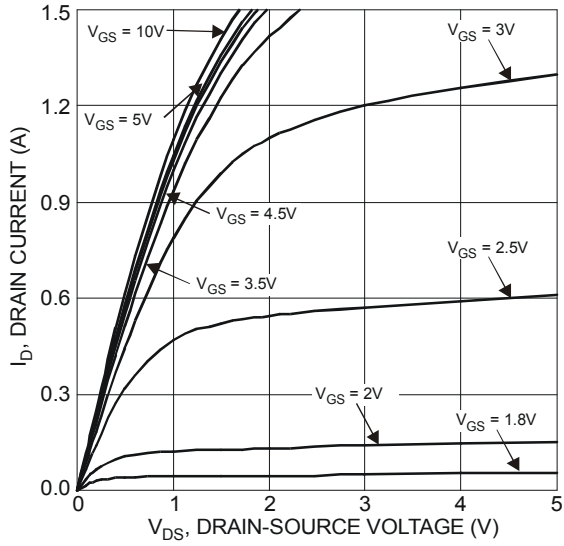


Figure 1 Typical Output Characteristics

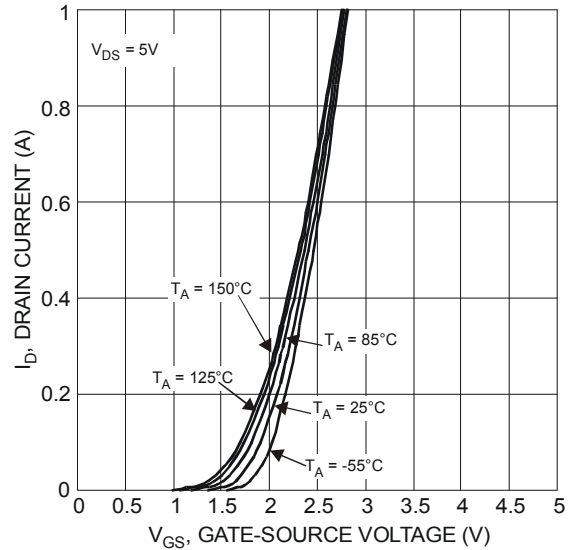


Figure 2 Typical Transfer Characteristics

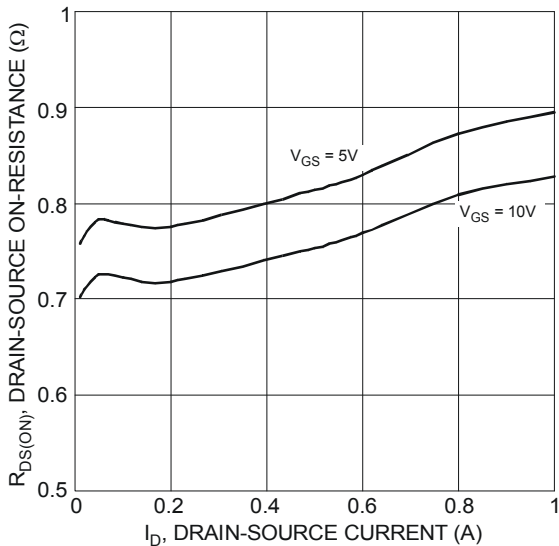


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

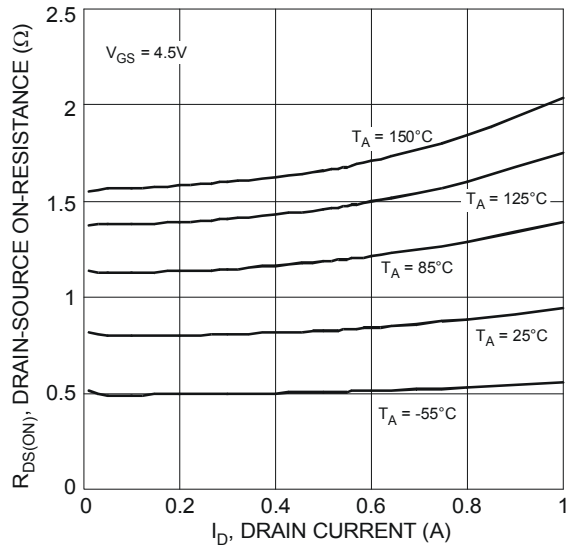


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

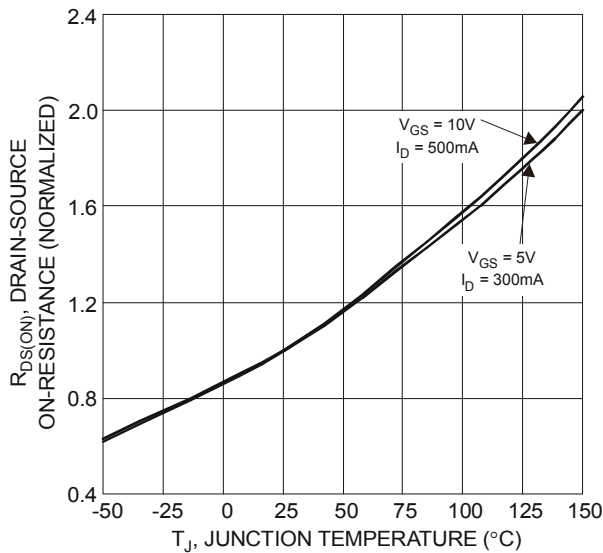


Figure 5 On-Resistance Variation with Temperature

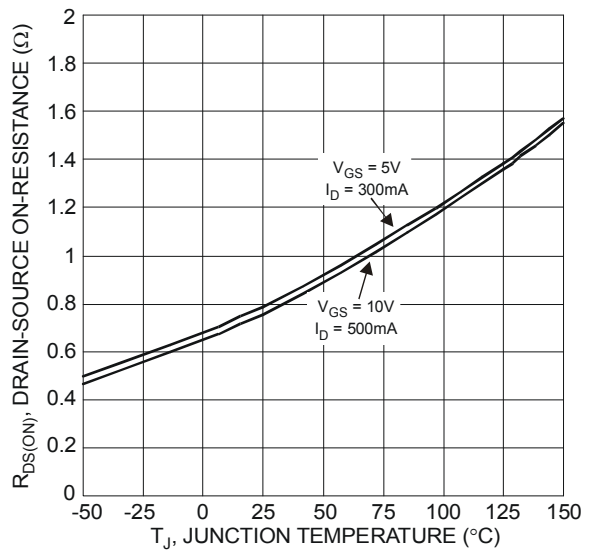


Figure 6 On-Resistance Variation with Temperature

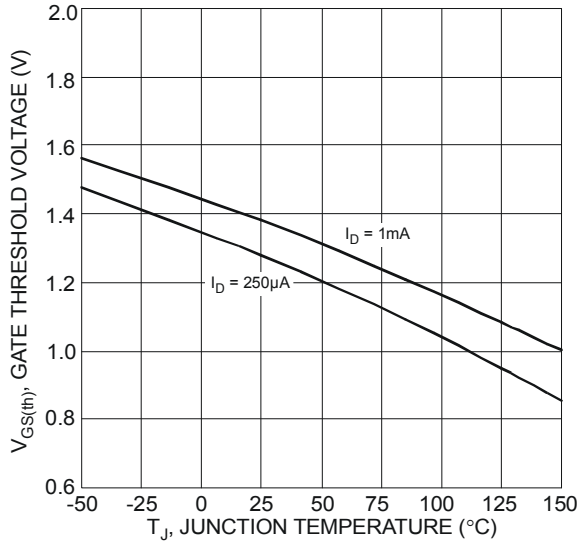


Figure 7 Gate Threshold Variation vs. Ambient Temperature

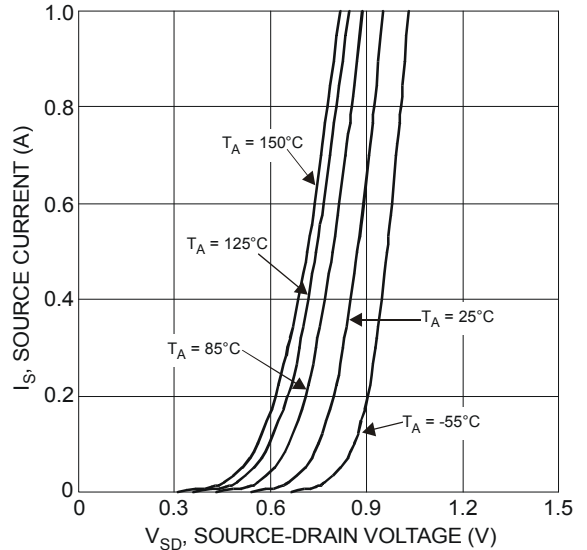


Figure 8 Diode Forward Voltage vs. Current

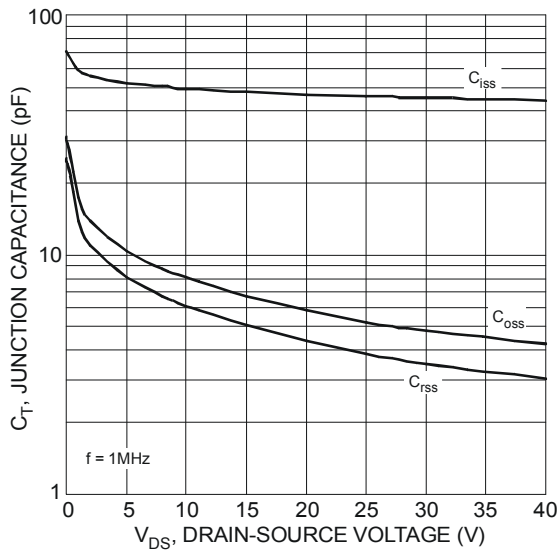


Figure 9 Typical Junction Capacitance

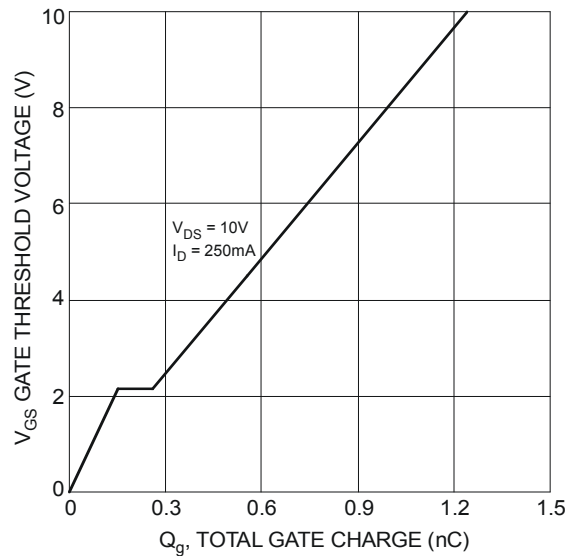
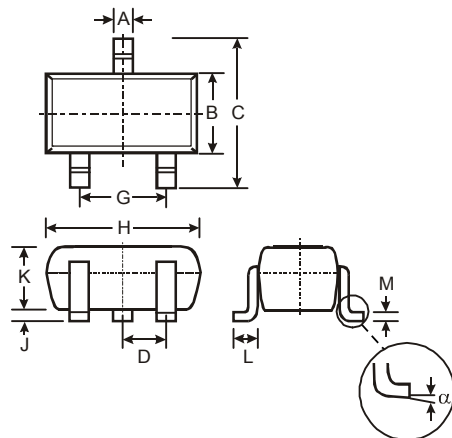


Figure 10 Gate Charge

Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

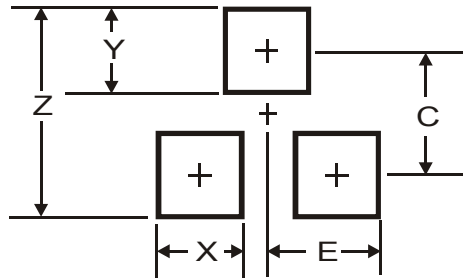


SOT323			
Dim	Min	Max	Typ
A	0.25	0.40	0.30
B	1.15	1.35	1.30
C	2.00	2.20	2.10
D	-	-	0.65
G	1.20	1.40	1.30
H	1.80	2.20	2.15
J	0.0	0.10	0.05
K	0.90	1.00	1.00
L	0.25	0.40	0.30
M	0.10	0.18	0.11
α	0°	8°	-

All Dimensions in mm

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	2.8
X	0.7
Y	0.9
C	1.9
E	1.0

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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