KSZ8841-16/32MQL/MVL/MVLI/MBL

Single-Port Ethernet MAC Controller

with Non-PCI Interface

Rev. 1.6

General Description

The KSZ8841-series single-port chip includes PCI and non-PCI CPU interfaces, and are available in 8/16-bit and 32-bit bus designs. This datasheet describes the KSZ8841M-series of non-PCI CPU interface chips. For information on the KSZ8841 PCI CPU interface chips, refer to the KSZ8841P datasheet.

The KSZ8841M is a single chip, mixed analog/digital device offering Wake-on-LAN technology for effectively addressing Fast Ethernet applications. It consists of a Fast Ethernet MAC controller, an 8-bit, 16-bit, and 32-bit generic host processor interface and incorporates a unique dynamic memory pointer with 4-byte buffer boundary and a fully utilizable 8KB for both TX and RX directions in host buffer interface.

The KSZ8841M is designed to be fully compliant with the appropriate IEEE 802.3 standards. An industrial temperature-grade version of the KSZ8841M, the KSZ8841MVLI, also can be ordered (see "Ordering Information section).

LinkMD®

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower-power consumption. The KSZ8841M is designed using a low-power CMOS process that features a single 3.3V power supply with 5V tolerant I/O. It has an extensive feature set that offers management information base (MIB) counters and CPU control/data interfaces.

The KSZ8841M includes a unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8841M supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

Functional Diagram

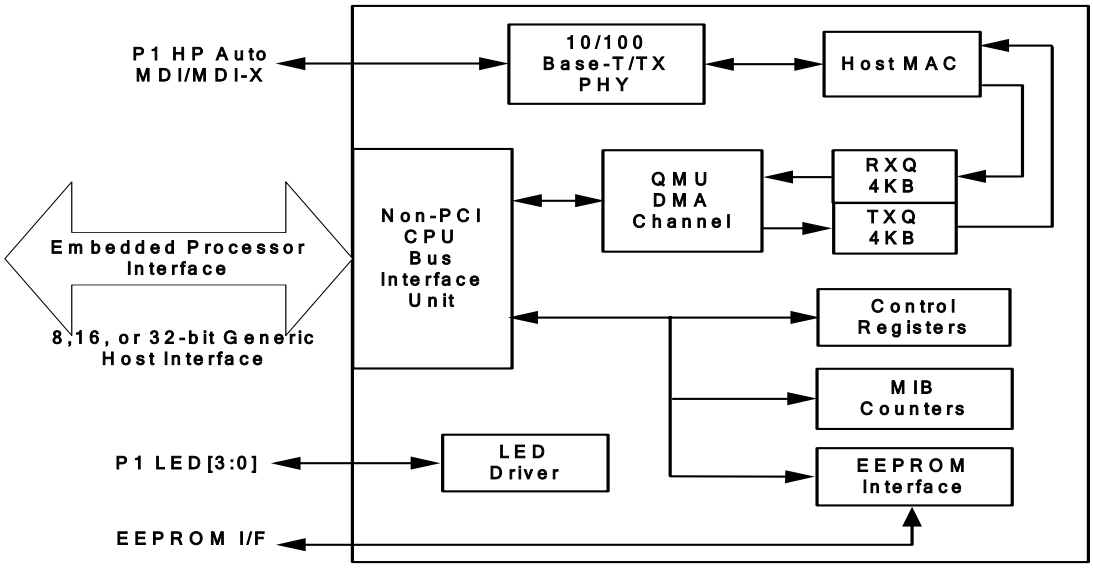

Figure 1. KSZ8841M Functional Diagram

Features

- Single chip Ethernet controller with IEEE802.3u support
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x full-duplex flow control and half-duplex backpressure collision flow control
- Supports burst data transfers
- 8KB internal memory for RX/TX FIFO buffers
- Early TX/RX functions to minimize latency through the device
- Optional to use external serial EEPROM configuration for both KSZ8841-16MQL and KSZ8841-32MQL
- Single 25MHz reference clock for both PHY and MAC

Network Features

- Fully integrated to comply with IEEE802.3u standards
- 10BASE-T and 100BASE-TX physical layer support
- Auto-negotiation: 10/100Mbps full and half duplex
- Adaptive equalizer
- Baseline wander correction

Power Modes, Power Supplies, and Packaging

- Single power supply (3.3V) with 5V tolerant I/O buffers
- Enhanced power management feature with power-down feature to ensure low-power dissipation during device idle periods
- Comprehensive LED indicator support for link, activity, full/half duplex, and 10/100 speed (4 LEDs)
  – User programmable
- Low-power CMOS design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-pin PQFP and 100-ball LFBGA (128-pin LQFP optional)

Additional Features

In addition to offering all of the features of a Layer 2 controller, the KSZ8841M offers:

- Dynamic buffer memory scheme
  – Essential for applications such as Video over IP where image jitter is unacceptable
- Flexible 8-bit, 16-bit, and 32-bit generic host processor interfaces
- Micrel LinkMD™ cable diagnostic capabilities to determine cable length, diagnose faulty cables, and determine distance to fault
- Wake-on-LAN functionality
  – Incorporates Magic Packet™, network link state, and wake-up frame technology
- HP Auto MDI-X™ crossover with disable/enable option
- Ability to transmit and receive frames up to 1916 bytes

Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

Ordering Information

Part Number	Temperature Range	Package
KSZ8841-16MQL	0°C to 70°C	128-Pin PQFP
KSZ8841-32MQL	0°C to 70°C	128-Pin PQFP
KSZ8841-16MVL	0°C to 70°C	128-Pin LQFP
KSZ8841-32MVL	0°C to 70°C	128-Pin LQFP
KSZ8841-16MVLI	–40°C to +85°C	128-Pin LQFP
KSZ8841-32MVLI	–40°C to +85°C	128-Pin LQFP
KSZ8841-16MBL	0°C to 70°C	100-Ball LFBGA
KSZ8841-16MBLI	–40°C to +85°C	100-Ball LFBGA
KSZ8841-16MQL-Eval	Evaluation Board for the KSZ8841-16MQL	
KSZ8841-16MBL-Eval	Evaluation Board for the KSZ8841-16MBL	

Revision History

Revision	Date	Summary of Changes
1.0	06/30/05	First released Preliminary Information.
1.1	08/08/05	Updated General Description, Functional Diagram, Pin Description and Features. Added this Revision History Table and Loopback support sections.
1.2	10/04/05	Update Power Saving bit description in P1PHYCTRL and P1SCSLMD registers.
1.3	11/01/05	Updated Figure 12/13/14 Asynchronous Timing and Table 16/17/18 parameters, PQFP package information.
1.4	03/31/06	Added QMU RX Flow Control High Watermark QRFCR register and updated body text
1.5	4/10/07	Improve the ARDY low time in read cycle to 40 ns and in write cycle to 50 ns during QMU data register access
1.6	10/22/07	Add KSZ8841-16MBL 100-Ball BGA package information

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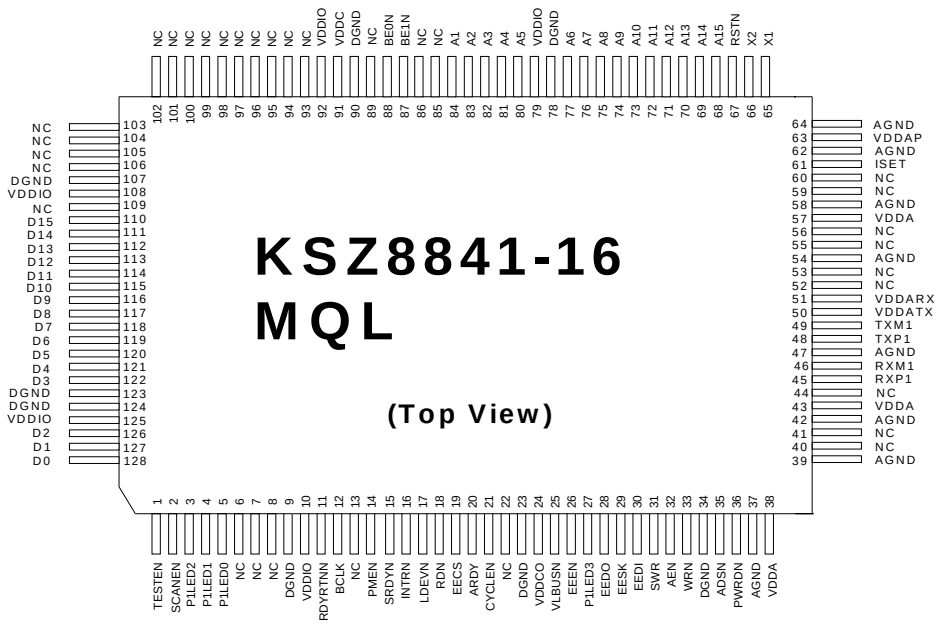


Figure 2. Standard – KSZ8841-16MQL 128-Pin PQFP

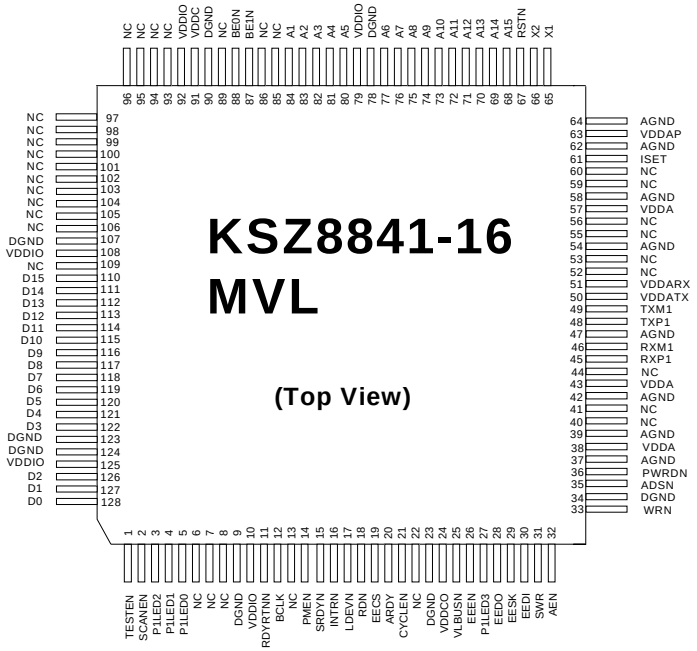


Figure 3. Option – KSZ8841-16MVL 128-Pin LQFP

Ball Configuration for KSZ8841-16 Chip (8/16-Bit)

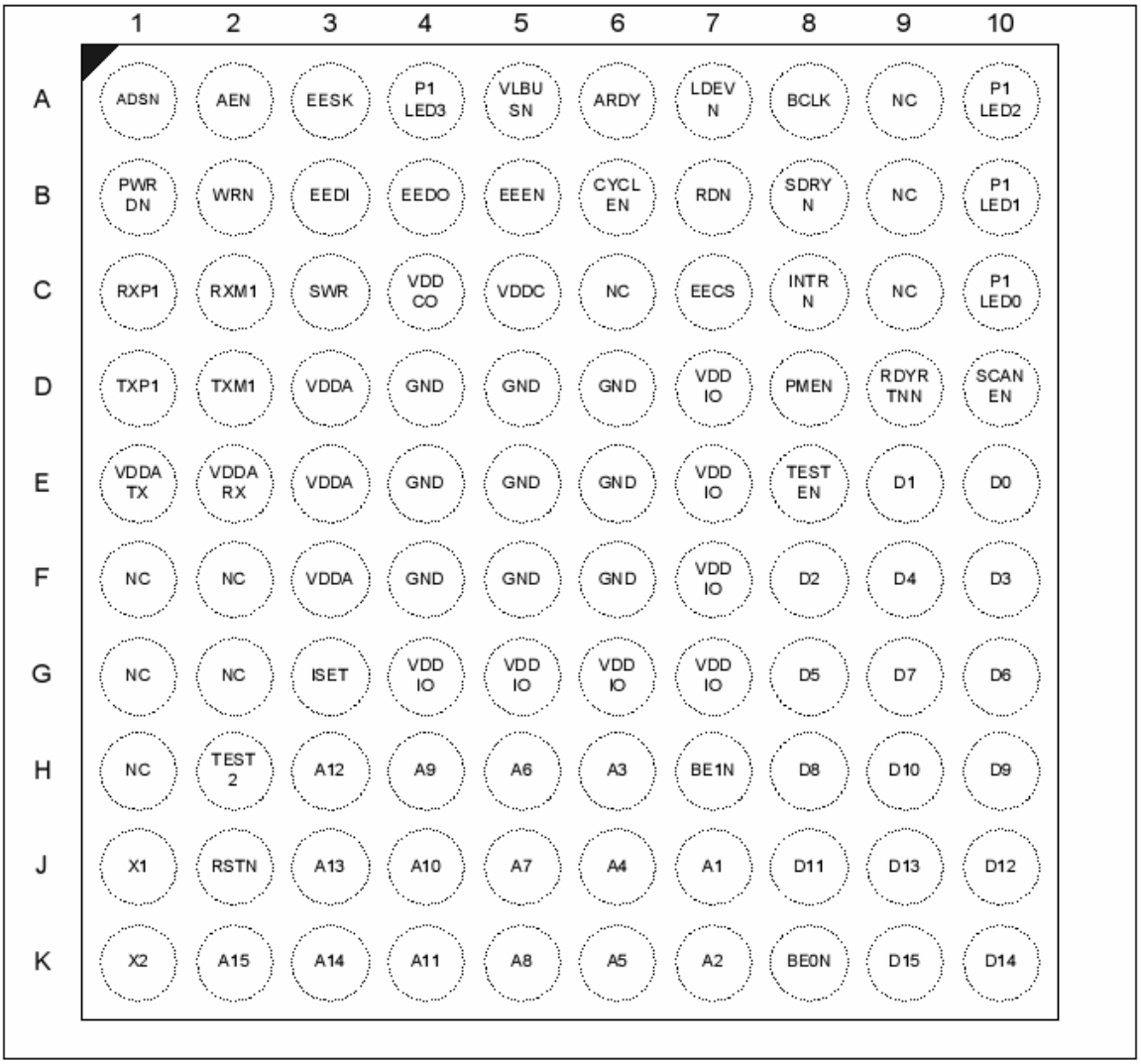


Figure 4. KSZ8841-16MBL 100-Ball LFBGA (Top View)

Pin Description for KSZ8841-16 Chip (8/16-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>3</td><td>P1LED2</td><td>Opu</td><td rowspan="3">Port 1 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27.</td></tr>
<tr><td>4</td><td>P1LED1</td><td>Opu</td></tr>
<tr><td>5</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>6</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>7</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>8</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.
This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>NC</td><td>Ipu</td><td>No Connect.</td></tr>
<tr><td>14</td><td>PMEN</td><td>Opu</td><td>Power Management Event Not
When asserted (Low), this signal indicates that a power management event has occurred in the system when a wake-up signal is detected by KSZ8841M.</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
15	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8841M drives this pin low to signal wait states.
16	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor.
17	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
19	EECS	Opu	EEPROM Chip Select This signal is used to select an external EEPROM device.
20	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7K pull-up resistor.
21	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	NC	Opd	No Connect
23	DGND	Gnd	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. It is recommended this pin should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors).
25	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	EEPROM Serial Clock A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.

Pin Number	Pin Name	Type	Pin Function
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bus mode or don't care for 32-bus mode when EEEN is pull-down (without EEPROM).
31	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
33	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
34	DGND	Gnd	Digital IO ground
35	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	Ipu	Full-chip power-down. Active Low (Low = Power down; High or floating = Normal operation).
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
39	AGND	Gnd	Analog ground
40	NC	—	No Connect
41	NC	—	No Connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
44	NC	—	No Connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No Connect
53	NC	—	No Connect
54	AGND	Gnd	Analog ground
55	NC	—	No Connect
56	NC	—	No Connect
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
58	AGND	Gnd	Analog ground
59	NC	Ipu	No connect
60	NC	Ipu	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground

Pin Number	Pin Name	Type	Pin Function
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
64	AGND	Gnd	Analog ground
65	X1	I	25MHz crystal or oscillator clock connection.
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is 50ppm for either crystal or oscillator.
67	RSTN	Ipu	Reset Not Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	Gnd	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	NC	I	No Connect
86	NC	I	No Connect
87	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
88	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
89	NC	I	No Connect
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	NC	I	No Connect
94	NC	I	No Connect
95	NC	I	No Connect
96	NC	I	No Connect
97	NC	I	No Connect
98	NC	I	No Connect
99	NC	I	No Connect
100	NC	I	No Connect
101	NC	I	No Connect
102	NC	I	No Connect

Pin Number	Pin Name	Type	Pin Function
103	NC	I	No Connect
104	NC	I	No Connect
105	NC	I	No Connect
106	NC	I	No Connect
107	DGND	Gnd	Digital IO ground
108	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	NC	I	No Connect
110	D15	I/O	Data 15
111	D14	I/O	Data 14
112	D13	I/O	Data 13
113	D12	I/O	Data 12
114	D11	I/O	Data 11
115	D10	I/O	Data 10
116	D9	I/O	Data 9
117	D8	I/O	Data 8
118	D7	I/O	Data 7
119	D6	I/O	Data 6
120	D5	I/O	Data 5
121	D4	I/O	Data 4
122	D3	I/O	Data 3
123	DGND	Gnd	Digital IO ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
126	D2	I/O	Data 2
127	D1	I/O	Data 1
128	D0	I/O	Data 0

Legend:

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output.

Ipd = Input with internal pull-down.

Ipu = Input with internal pull-up.

Opd = Output with internal pull-down.

Opu = Output with internal pull-up.

Ball Description for KSZ8841-16 Chip (8/16-Bit)

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type</th><th>Ball Function</th></tr>
<tr><td>E8</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this ball to ground.</td></tr>
<tr><td>D10</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this ball to ground.</td></tr>
<tr><td>A10
B10
C10</td><td>P1LED2
P1LED1
P1LED0</td><td>Opu
Opu
Opu</td><td>Port 1 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is ball A4.</td></tr>
<tr><td>D9</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this ball, assert this ball.</td></tr>
<tr><td>A8</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.
This ball should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>D8</td><td>PMEN</td><td>Opu</td><td>Power Management Event Not
When asserted (Low), this signal indicates that a power management event has occurred in the system when a wake-up signal is detected by KSZ8841M.</td></tr>
<tr><td>B8</td><td>SRDYN</td><td>Opu</td><td>Synchronous Ready Not
Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses.
For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK.</td></tr>
<tr><td>C8</td><td>INTRN</td><td>Opd</td><td>Interrupt
Active Low signal to host CPU to indicate an interrupt status bit is set, this ball need an external 4.7K pull-up resistor.</td></tr>
<tr><td>A7</td><td>LDEVN</td><td>Opd</td><td>Local Device Not</td></tr>
</table>

Ball Number	Ball Name	Type	Ball Function
			Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
B7	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
C7	EECS	Opu	EEPROM Chip Select
A6	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This ball needs an external 4.7K pull-up resistor.
B6	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this ball follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this ball stays High for read cycles and Low for write cycles.
A5	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
B5	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this ball is pull-up. EEPROM is disabled when this ball is pull-down or no connect.
A4	P1LED3	Opd	Port 1 LED indicator See the description in balls A10, B10, and C10.
B4	EEDO	Opd	EEPROM Data Out This ball is connected to DI input of the serial EEPROM.
A3	EESK	Opd	EEPROM Serial Clock A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.
B3	EEDI	Ipd	EEPROM Data In This ball is connected to DO output of the serial EEPROM when EEEN is pull-up. This ball can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don't care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
C3	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
A2	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
B2	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
A1	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
B1	PWRDN	Ipu	Full-chip power-down. Low = Power down; High or floating = Normal operation.

Ball Number	Ball Name	Type	Ball Function
C1	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
C2	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
D1	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
D2	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
H2	TEST2	Ipu	Test input 2 For normal operation, left this ball open.
G3	ISET	O	Set physical transmits output current. Pull-down this ball with a 3.01K 1% resistor to ground.
J1	X1	I	25MHz crystal or oscillator clock connection.
K1	X2	O	Balls (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ± 50ppm for either crystal or oscillator.
J2	RSTN	Ipu	Hardware reset ball (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
K2	A15	I	Address 15
K3	A14	I	Address 14
J3	A13	I	Address 13
H3	A12	I	Address 12
K4	A11	I	Address 11
J4	A10	I	Address 10
H4	A9	I	Address 9
K5	A8	I	Address 8
J5	A7	I	Address 7
H5	A6	I	Address 6
K6	A5	I	Address 5
J6	A4	I	Address 4
H6	A3	I	Address 3
K7	A2	I	Address 2
J7	A1	I	Address 1
H7	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
K8	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
K9	D15	I/O	Data 15
K10	D14	I/O	Data 14
J9	D13	I/O	Data 13
J10	D12	I/O	Data 12
J8	D11	I/O	Data 11
H9	D10	I/O	Data 10
H10	D9	I/O	Data 9
H8	D8	I/O	Data 8
G9	D7	I/O	Data 7
G10	D6	I/O	Data 6
G8	D5	I/O	Data 5
F9	D4	I/O	Data 4
F10	D3	I/O	Data 3

Ball Number	Ball Name	Type	Ball Function
F8	D2	I/O	Data 2
E9	D1	I/O	Data 1
E10	D0	I/O	Data 0
C4	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output ball provides power to all VDDC/VDDA balls. It is recommended this ball should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application. Note: Internally generated power voltage. Do not connect an external power supply to this ball. This ball is used for connecting external filter (Ferrite bead and capacitors).
C5	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (ball C4) through external Ferrite bead and capacitor.
D3, E3, F3	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (ball C4) through external Ferrite bead and capacitor.
E1	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
E2	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
D7, E7, F7, G4, G5, G6, G7	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
D4, D5, D6, E4, E5, E6, F4, F5, F6	GND	Gnd	All digital and analog grounds
H1, A9, B9, C9, C6, F2, F1, G2, G1	NC	I/O	No Connect

Pin Configuration for KSZ8841-32 Chip (32-Bit)

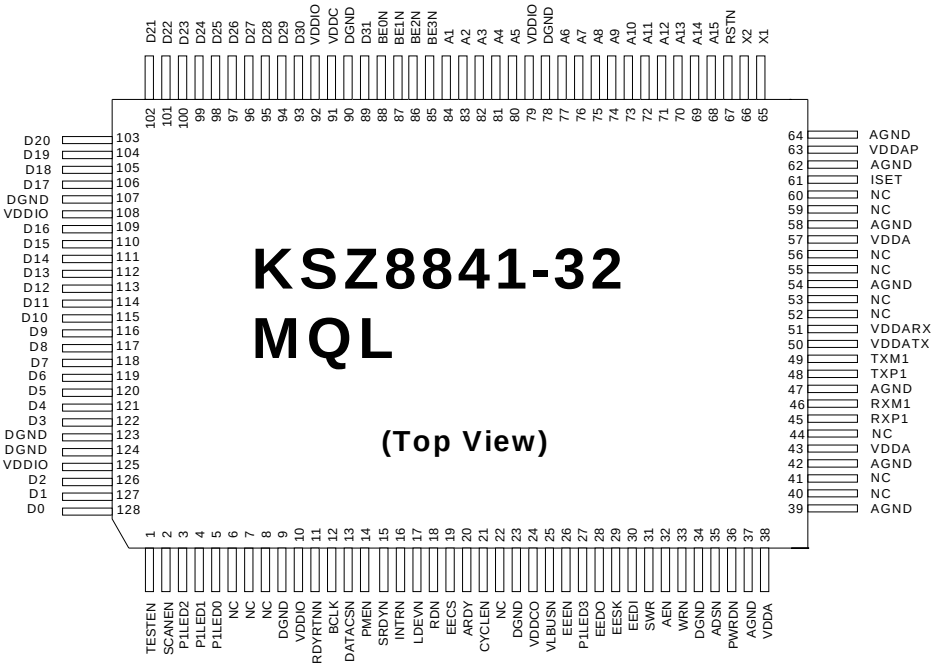


Figure 5. Standard – KSZ8841-32MQL 128-Pin PQFP

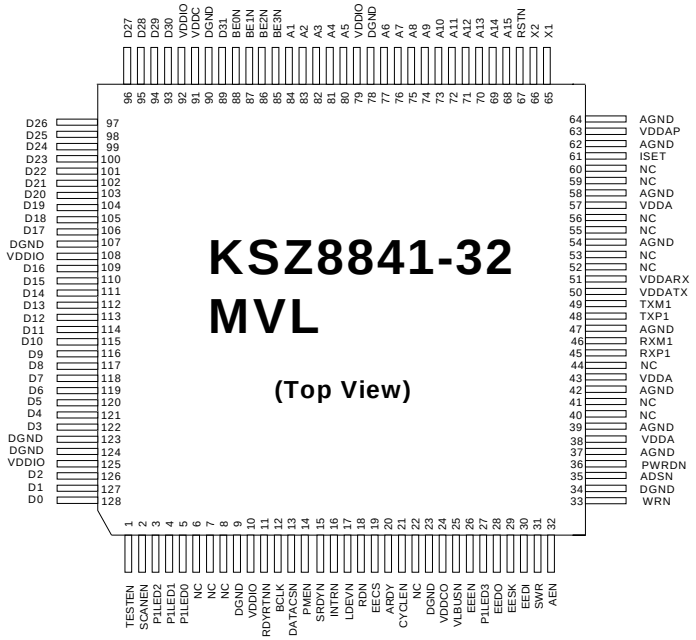


Figure 6. Option – KSZ8841-32MVL 128-Pin LQFP

Pin Description for KSZ8841-32 Chip (32-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>3</td><td>P1LED2</td><td>Opu</td><td rowspan="3">Port 1 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27.</td></tr>
<tr><td>4</td><td>P1LED1</td><td>Opu</td></tr>
<tr><td>5</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>6</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>7</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>8</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.
This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>DATACSN</td><td>Ipu</td><td>DATA Chip Select Not (For KSZ8841-32 Mode only)
Chip select signal for QMU data register (QDRH, QDRL), active Low.
When DATACSN is Low, the data path can be accessed regardless of the value of AEN, A15-A1, and the content of the BANK select register.</td></tr>
<tr><td>14</td><td>PMEN</td><td>Opu</td><td>Power Management Event Not
When asserted (Low), this signal indicates that a power management event has occurred in the system when a wake-up signal is detected by KSZ8841M.</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
15	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8841M drives this pin low to signal wait states.
16	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor
17	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
19	EECS	Opu	EEPROM Chip Select This signal is used to select an external EEPROM device.
20	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7K pull-up resistor.
21	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	NC	Opd	No Connect
23	DGND	Gnd	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. It is recommended this ball should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application. Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors).
25	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 32-bit asynchronous mode or EISA-like burst mode.
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	EEPROM Serial Clock A 4µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.

Pin Number	Pin Name	Type	Pin Function
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bus mode or don't care for 32-bus mode when EEEN is pull-down (without EEPROM).
31	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
33	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
34	DGND	Gnd	Digital IO ground
35	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	Ipu	Full-chip power-down. Active Low (Low = Power down; High or floating = Normal operation).
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
39	AGND	Gnd	Analog ground
40	NC	—	No Connect
41	NC	—	No Connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
44	NC	—	No Connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No Connect
53	NC	—	No Connect
54	AGND	Gnd	Analog ground
55	NC	—	No Connect
56	NC	—	No Connect
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
58	AGND	Gnd	Analog ground
59	NC	Ipu	No connect
60	NC	Ipu	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground

Pin Number	Pin Name	Type	Pin Function
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
64	AGND	Gnd	Analog ground
65	X1	I	25MHz crystal or oscillator clock connection.
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is 50ppm for either crystal or oscillator.
67	RSTN	Ipu	Reset Not Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	Gnd	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	BE3N	I	Byte Enable 3 Not, Active low for Data byte 3 enable
86	BE2N	I	Byte Enable 2 Not, Active low for Data byte 2 enable
87	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable
88	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable
89	D31	I/O	Data 31
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	D30	I/O	Data 30
94	D29	I/O	Data 29
95	D28	I/O	Data 28
96	D27	I/O	Data 27
97	D26	I/O	Data 26
98	D25	I/O	Data 25
99	D24	I/O	Data 24
100	D23	I/O	Data 23
101	D22	I/O	Data 22
102	D21	I/O	Data 21

Pin Number	Pin Name	Type	Pin Function
103	D20	I/O	Data 20
104	D19	I/O	Data 19
105	D18	I/O	Data 18
106	D17	I/O	Data 17
107	DGND	Gnd	Digital IO ground
108	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	D16	I/O	Data 16
110	D15	I/O	Data 15
111	D14	I/O	Data 14
112	D13	I/O	Data 13
113	D12	I/O	Data 12
114	D11	I/O	Data 11
115	D10	I/O	Data 10
116	D9	I/O	Data 9
117	D8	I/O	Data 8
118	D7	I/O	Data 7
119	D6	I/O	Data 6
120	D5	I/O	Data 5
121	D4	I/O	Data 4
122	D3	I/O	Data 3
123	DGND	Gnd	Digital IO ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
126	D2	I/O	Data 2
127	D1	I/O	Data 1
128	D0	I/O	Data 0

Legend:

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output.

Ipd = Input with internal pull-down.

Ipu = Input with internal pull-up.

Opd = Output with internal pull-down.

Opu = Output with internal pull-up.

Functional Description

The KSZ8841M is a single-chip Fast Ethernet MAC controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a Bus Interface Unit (BIU) that controls the KSZ8841M via an 8-bit, 16-bit, or 32-bit host bus interface.

The KSZ8841M is fully compliant to IEEE802.3u standards.

Functional Overview

Power Management

Power down

The KSZ8841M features a port power-down mode. To save power, the user can power-down the port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for this port. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full chip power-down mode PWRDN (pin 36). When this pin is pulled-down, the entire chip powers down. Transitioning this pin from pull-down to pull-up results in a power up and chip reset.

Wake-on-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic.

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working).

A wake-up signal is caused by:

1. Detection of a change in the network link state
2. Receipt of a network wake-up frame
3. Receipt of a Magic Packet

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own way.

Link Change

Link status wake events are useful to indicate a change in the network's availability, especially when this change may impact the level at which the system should re-enter the sleeping state. For example, a change from link off to link on may trigger the system to re-enter sleep at a higher level (D2 versus D3[1]) so that wake frames can be detected. Conversely, a transition from link on to link off may trigger the system to re-enter sleep at a deeper level (D3 versus D2) since the network is not currently available.

Wake-up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a 'wake up' frame. The KSZ8841M supports up to four users defined wake-up frames as below:

1. Wake-up frame 0 is defined in registers 0x00-0x0A of Bank 4 and is enabled by bit 0 in wakeup frame control register.
2. Wake-up frame 1 is defined in registers 0x00-0x0A of Bank 5 and is enabled by bit 1 in wakeup frame control register.
3. Wake-up frame 2 is defined in registers 0x00-0x0A of Bank 6 and is enabled by bit 2 in wakeup frame control register.
4. Wake-up frame 4 is defined in registers 0x00-0x0A of Bank 7 and is enabled by bit 3 in wakeup frame control register.

Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up.

[1] References to D0, D1, D2, and D3 are power management states defined in a similar fashion to the way they are defined for PCI. For more information, refer to the PCI specification at www.pcisig.com/specifications/conventional/pcipm1.2.pdf.

Magic Packet is a standard feature integrated into the KSZ8841M. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8841M has been put into Magic Packet Enable mode (WFCR[7]=1), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

example

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8841M controller detects the data sequence, however, it then alerts the PC's power management circuitry (assert the PMEN pin) to wake up the system.

Physical Layer Transceiver (PHY)

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 1% 3.01KΩ resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

PLL Clock Synthesizer (Recovery)

The internal PLL clock synthesizer generates 125MHz, 62.5MHz, 41.66MHz, and 25MHz clocks by setting the on-chip bus speed control register for KSZ8841M system timing. These internal clocks are generated from an external 25Mhz crystal or oscillator.

Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.4V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8841M decodes a data frame.

The receiver clock is maintained active during idle periods in between data reception.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8841M supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8841M device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are:

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 1. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram shows a typical straight cable connection between a network interface card (NIC) and a chip (MDI), or hub (MDI-X).

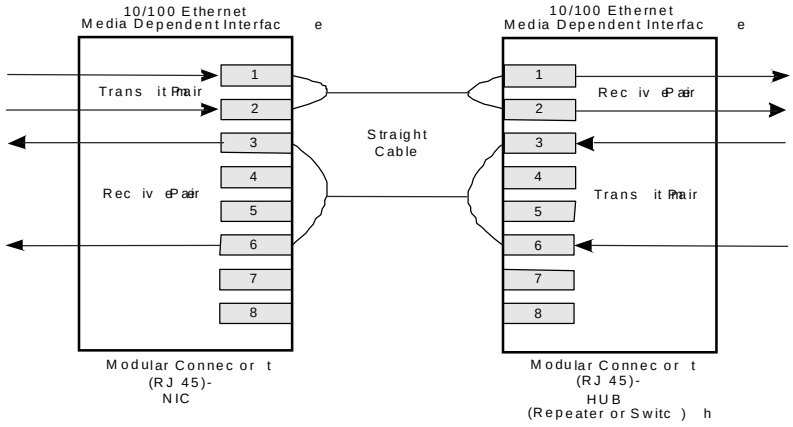


Figure 7. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two chips or hubs (two MDI-X devices).

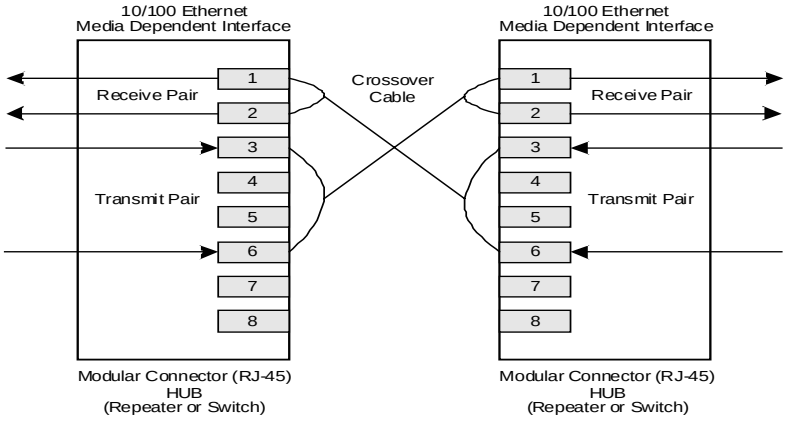


Figure 8. Typical Crossover Cable Connection

Auto Negotiation

The KSZ8841M conforms to the auto negotiation protocol as described by the 802.3 committee to allow the port to operate at either 10Base-T or 100Base-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8841M is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the following flow diagram (Figure 9).

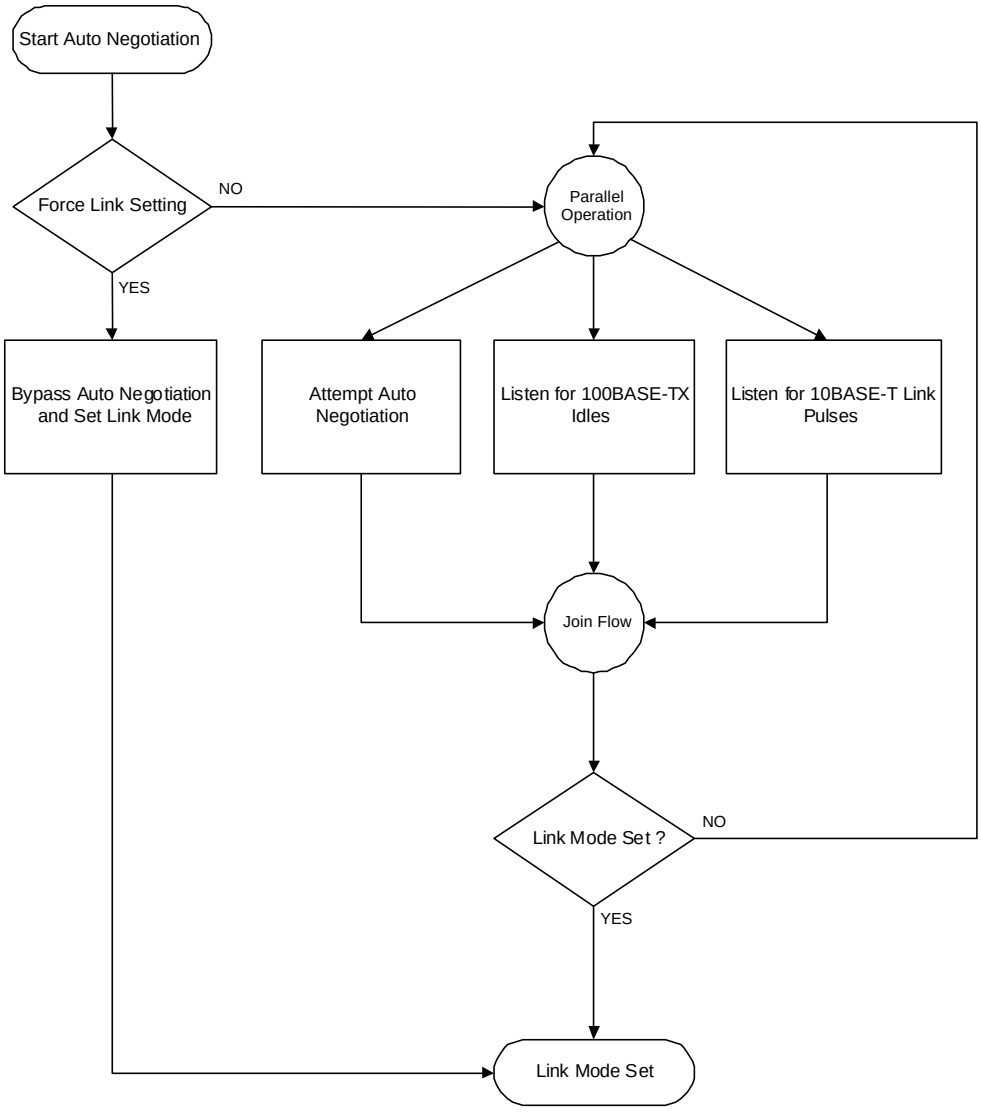


Figure 9. Auto Negotiation and Parallel Operation

LinkMD Cable Diagnostics

The KSZ8841M LinkMD uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of +/–2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1VCT[8:0].

Note: cable diagnostics are only valid for copper connections – fiber-optic operation is not supported.

Access

LinkMD is initiated by accessing register P1VCT, the LinkMD Control/Status register, in conjunction with register P1CR4, the 100BASE-TX PHY Controller register.

Usage

LinkMD can be run at any time by ensuring that Auto-MDIX has been disabled. To disable Auto-MDIX, write a ‘1’ to P1CR4[10] to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1VCT[15], is set to ‘1’ to start the test on this pair.

When bit P1VCT[15] returns to ‘0’, the test is complete. The test result is returned in bits P1VCT[14:13] and the distance is returned in bits P1VCT[8:0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

If P1VCT[14:13]=11, this indicates an invalid test, and occurs when the KSZ8841M is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8841M to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by the following formula:

P1VCT[8:0] x 0.4m for port 1 cable distance

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

Media Access Control (MAC) Operation

The KSZ8841M strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

Back-Off Algorithm

The KSZ8841M implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

Flow Control

The KSZ8841M supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8841M receives a pause control frame, the KSZ8841M will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8841M are transmitted.

On the transmit side, the KSZ8841M has intelligent and efficient ways to determine when to invoke flow control. The flow

control is based on availability of the system resources.

The KSZ8841M issues a flow control frame (Xoff, or transmitter off), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8841M sends out the another flow control frame (Xon, or transmitter on) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

Half-Duplex Backpressure

A half-duplex backpressure option (non-IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If backpressure is required, the KSZ8841M sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8841M discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

Clock Generator

The X1 and X2 pins are connected to a 25MHz crystal. X1 can also serve as the connector to a 3.3V, 25MHz oscillator (as described in the pin description).

The bus interface unit (BIU) uses BCLK (Bus Clock) for synchronous accesses. The maximum frequency is 50MHz for VLBus-like and EISA-like slave direct memory access (DMA).

Bus Interface Unit (BIU)

The BIU host interface is a generic bus interface, designed to communicate with embedded processors. The use of glue logic may be required when it talks to various standard buses and processors.

Supported Transfers

In terms of transfer type, the BIU can support two transfers: asynchronous transfer and synchronous transfer. To support these transfers (asynchronous and synchronous), the BIU provides three groups of signals:

Synchronous signals

Asynchronous signals

Common signals are used for both synchronous and asynchronous transfers.

Since both synchronous and asynchronous signals are independent of each other, synchronous transfer and asynchronous transfer can be mixed or interleaved but cannot be overlapped (due to the sharing of common signals).

Physical Data Bus Size

The BIU supports an 8-bit, 16-bit, or 32-bit host standard data bus. Depending on the size of the physical data bus, the KSZ8841M supports 8-bit, 16-bit, or 32-bit data transfers

For example,

For a 32-bit system/host data bus, the KSZ8841M allows an 8-bit, 16-bit, and 32-bit data transfer (KSZ8841-32MQL).

For a 16-bit system/host data bus, the KSZ8841M allows an 8-bit and 16-bit data transfer (KSZ8841-16MQL).

For an 8-bit system/host data bus, the KSZ8841M only allows an 8-bit data transfer (KSZ8841-16MQL).

The KSZ8841M does not support internal data byte-swap but it does support internal data word-swap. This means that the system/host data bus HD[7:0] must connect to both D[7:0] and D[15:8] for an 8-bit data bus interface. For a 16-bit data bus, the system/host data bus HD[15:8] and HD[7:0] only need to connect to D[15:8] and D[7:0] respectively, and there is no need to connect HD[15:8] and HD[7:0] to D[31:24] and D[23:16].

Table 2 describes the BIU signal grouping.

<table>
<tr><th>Signal</th><th>Type(1)</th><th>Function</th></tr>
<tr><td colspan="3">Common Signals</td></tr>
<tr><td>A[15:1]</td><td>I</td><td>Address</td></tr>
<tr><td>AEN</td><td>I</td><td>Address Enable
Address Enable asserted indicates memory address on the bus for DMA access and since the device is an I/O device, address decoding is only enabled when AEN is Low.</td></tr>
<tr><td>BE3N, BE2N, BE1N, BE0N</td><td>I</td><td>Byte Enable
<table>
<tr><th>BE0N</th><th>BE1N</th><th>BE2N</th><th>BE3N</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>32-bit access</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Lower 16-bit (D[15:0]) access</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Higher 16-bit (D[31:16]) access</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 0 (D[7:0]) access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Byte 1 (D[15:8]) access</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Byte 2 (D[23:16]) access</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Byte 3 (D[31:24]) access</td></tr>
</table>
Note 1: BE3N, BE2N, BE1N and BE0N are ignored when DATACSN is low because 32 bit transfers are assumed.
Note 2: BE2N and BE3N are valid only for the KSZ8841-32 mode, and are No Connect for the KSZ8841-16 mode.</td></tr>
<tr><td>D[31:16]</td><td>I/O</td><td>Data
For KSZ8841M-32 mode only.</td></tr>
<tr><td>D[15:0]</td><td>I/O</td><td>Data
For both KSZ8841-32 and KSZ8841-16 Modes</td></tr>
<tr><td>ADSN</td><td>I</td><td>Address Strobe
The rising edge of ADSN is used to latch A[15:1], AEN, BE3N, BE2N, BE1N and BE0N.</td></tr>
<tr><td>LDEVN</td><td>O</td><td>Local Device
This signal is a combinatorial decode of AEN and A[15:4]. This A[15:4] is used to compare against the Base Address Register.</td></tr>
<tr><td>DATACSN</td><td>I</td><td>Data Register Chip Select (For KSZ8841-32MQL Mode only)
This signal is used for central decoding architecture (mostly for embedded application). When asserted, the device’s local decoding logic is ignored and the 32-bit access to QMU Data Register is assumed.</td></tr>
<tr><td>INTR</td><td>O</td><td>Interrupt</td></tr>
<tr><td colspan="3">Synchronous Transfer Signals</td></tr>
<tr><td>VLBUSN</td><td>I</td><td>VLBUS
VLBUSN = 0, VLBus-like cycle.
VLBUSN = 1, burst cycle (both host/system and KSZ8841M can insert wait state)</td></tr>
<tr><td>CYCLEN</td><td>I</td><td>CYCLEN
For VLBus-like access: used to sample SWR when asserted.
For burst access: used to connect to IOWC# bus signal to indicate burst write.</td></tr>
<tr><td>SWR</td><td>I</td><td>Write/Read
For VLBus-like access: used to indicate write (High) or read (Low) transfer.
For burst access: used to connect to IORC# bus signal to indicate burst read.</td></tr>
<tr><td>SRDYN</td><td>O</td><td>Synchronous Ready
For VLBus-like access: exactly the same signal definition of nSRDY in VLBus.
For burst access: insert wait state by KSZ8841M whenever necessary during the Data Register access.</td></tr>
<tr><td>RDYRTNN</td><td>I</td><td>Ready Return
For VLBus-like access: exactly like RDYRTNN signal in VLBus to end the cycle.</td></tr>
</table>

Signal	Type[1]	Function
		For burst access: exactly like EXRDY signal in EISA to insert wait states. Note that the wait states are inserted by system logic (memory) not by KSZ8841M.
BCLK	I	**Bus Clock**
Asynchronous Transfer Signals		
RDN	I	**Asynchronous Read**
WRN	I	**Asynchronous Write**
ARDY	O	**Asynchronous Ready** This signal is asserted (Low) to insert wait states.

Note 1: I = Input. O = Output. I/O = Bi-directional.

Table 2. Bus Interface Unit Signal Grouping

Regardless of whether the transfer is synchronous or asynchronous, if the address latch is required, use the rising edge of ADSN to latch the incoming signals A[15:1], AEN, BE3N, BE2N, BE1N, and BE0N.

Note: If the local device decoder is used in either synchronous or asynchronous transfers, LDEVN will be asserted to indicate that the KSZ8841M is successfully targeted. The signal LDEVN is a combinatorial decode of AEN and A[15:4].

Asynchronous Interface

For asynchronous transfers, the asynchronous dedicated signals RDN (for read) or WRN (for write) toggle, but the synchronous dedicated signals CYCLEN, SWR, and RDYRTNN are de-asserted and stay at the same logic level throughout the entire asynchronous transfer.

There is no data burst support for asynchronous transfer. All asynchronous transfers are single-data transfers. The BIU, however, provides flexible asynchronous interfacing to communicate with various applications and architectures. Three major ways of interfacing with the system (host) are.

1. Interfacing with the system/host relying on local device decoding and having stable address throughout the whole transfer: The typical example for this application is ISA-like bus interface using latched address signals as shown in Figure 13. No additional address latch is required, therefore ADSN should be connected Low. The BIU decodes A[15:4] and qualifies with AEN (Address Enable) to determine if the KSZ8841M device is the intended target. The host utilizes the rising edge of RDN to latch read data and the BIU will use rising edge of WRN to latch write data.

Interfacing with the system/host relying on local device decoding but not having stable address throughout the entire transfer: The typical example for this application is EISA-like bus (non-burst) interface as shown in the Figure 14. This type of interface requires ADSN to latch the address on the rising edge. The BIU decodes latched A[15:4] and qualifies with AEN to determine if the KSZ8841M device is the intended target. The data transfer is the same as the first case.

Interfacing with the system/host relying on central decoding (KSZ8841-32MQL only).

The typical example for this application is for an embedded processor having a central decoder on the system board or within the processor. Connecting the chip select (CS) from system/host to DATACSN bypasses the local device decoder. When the DATACSN is asserted, it only allows access to the Data Register in 32 bits and BE3N, BE2N, BE1N, and BE0N are ignored as shown in the Figure 15. No other registers can be accessed by asserting DATACSN. The data transfer is the same as in the first case. Independent of the type of asynchronous interface used. To insert a wait state, the BIU will assert ARDY to prolong the cycle.

Synchronous Interface

For synchronous transfers, the synchronous dedicated signals CYCLEN, SWR, and RDYRTNN will toggle but the asynchronous dedicated signals RDN and WRN are de-asserted and stay at the same logic level throughout the entire synchronous transfer.

The synchronous interface mainly supports two applications, one for VLBus-like and the other for EISA-like (DMA type C) burst transfers. The VLBus-like interface supports only single-data transfer. The pin option VLBUSN determines if it is a VLBus-like or EISA-like burst transfer – if VLBUSN = 0, the interface is for VLBus-like transfer; if VLBUSN = 1, the interface is for EISA-like burst transfer.

For VLBus-like transfer interface (VLBUSN = 0):

This interface is used in an architecture in which the device's local decoder is utilized; that is, the BIU decodes latched A[15:4] and qualifies with AEN (Address Enable) to determine if the KSZ8841M device is the intended target. No burst is supported in this application. The M/nIO signal connection in VLBus is routed to AEN. The CYCLEN in this application is used to sample the SWR signal when it is asserted. Usually, CYCLEN is one clock delay of ADSN. There is a handshaking process to end the cycle of VLBus-like transfers. When the KSZ8841M is ready to finish the cycle, it asserts SRDYN. The system/host acknowledges SRDYN by asserting RDYRTNN after the system/host has latched the read data. The KSZ8841M holds the read data until RDYRTNN is asserted. The timing waveform is shown in Figures 19 and 20.

For EISA-like burst transfer interface (VLBUSN = 1):

The SWR is connected to IORC# in EISA to indicate the burst read and CYCLEN is connected to IOWC# in EISA to indicate the burst write. Note that in this application, both the system/host/memory and KSZ8841M are capable of inserting wait states. For system/host/memory to insert a wait state, assert the RDYRTNN signal; for the KSZ8841M to insert the wait state, assert the SRDYN signal. The timing waveform is shown in Figures 17 and 18.

BIU Summation

Figure 10 shows the mapping from ISA-like, EISA-like and VLBus-like transactions to the chip's BIU.

Figure 11 shows the connection for different data bus sizes.

Note: For the 8-bit data bus mode, the internal inverter is enabled and connected between BE0N and BE1N, so an even address will enable the BE0N and an odd address will enable the BE1N.

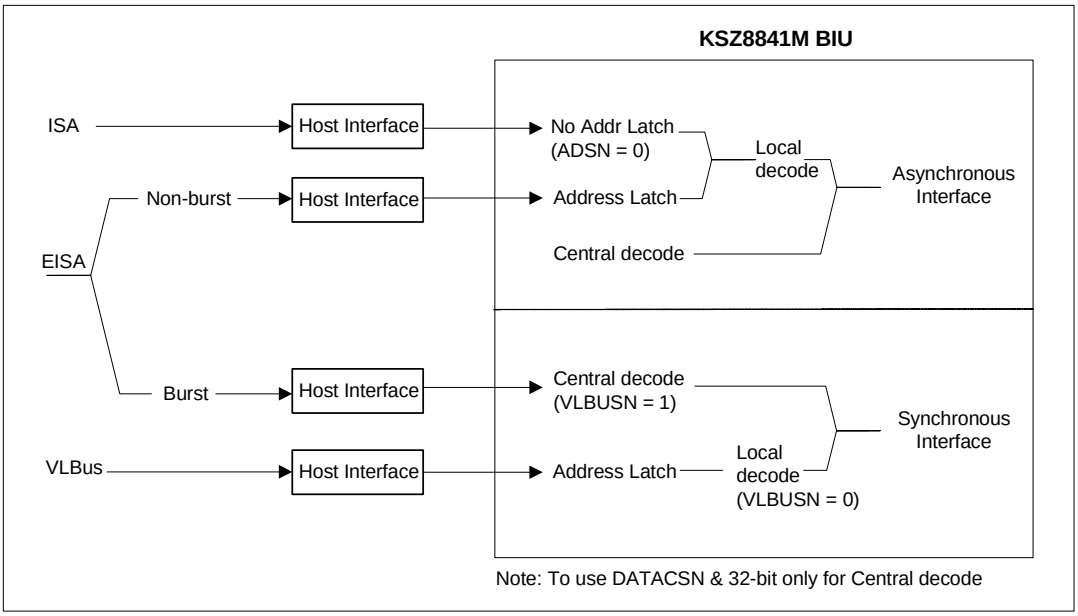


Figure 10. Mapping from the ISA, EISA, and VLBus to the KSZ8841M Bus Interface

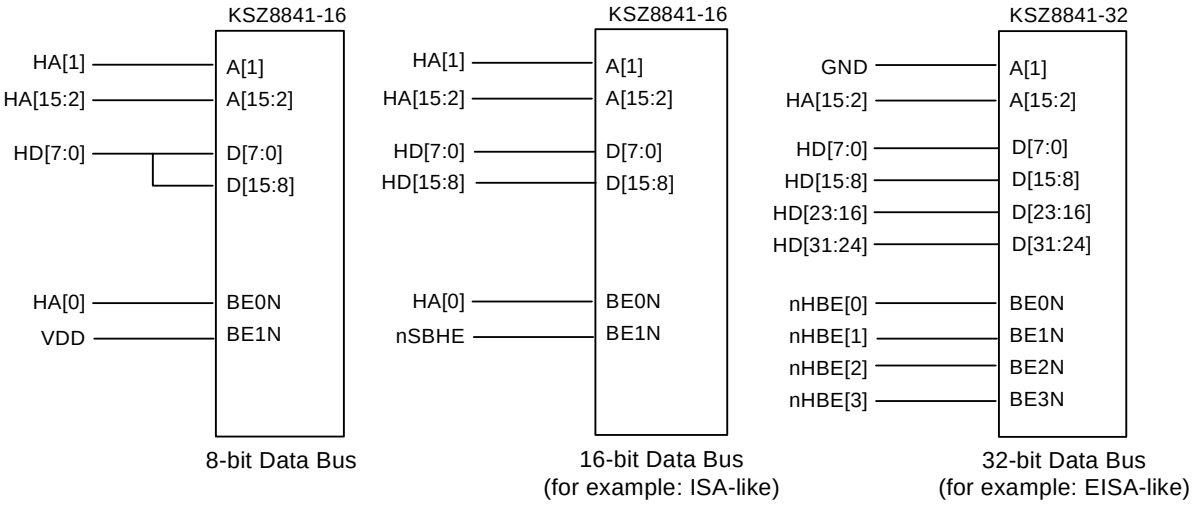


Figure 11. KSZ8841M 8-Bit, 16-Bit, and 32-Bit Data Bus Connections

BIU Implementation Principles

Since KSZ8841M is an I/O device with 16 addressable locations, address decoding is based on the values of A15-A4 and AEN. Whenever DATACSN is asserted, the address decoder is disabled and a 32-bit transfer to Data Register is assumed (BE3N – BE0N are ignored).

If address latching is required, the address is latched on the rising edge of ADSN and is transparent when ADSN=0.

1. Byte, word, and double word data buses and accesses (transfers) are supported.
2. Internal byte swapping is not implemented and word swapping is supported internally. Refer to Figure 11 for the appropriate 8-bit, 16-bit, and 32-bit data bus connection.
3. Since independent sets of synchronous and asynchronous signals are provided, synchronous and asynchronous cycles can be mixed or interleaved as long as they are not active simultaneously.

4. The asynchronous interface uses RDN and WRN signal strobes for data latching. If necessary, ARDY is de-asserted on the leading edge of the strobe.
5. The VLBUS-like synchronous interface uses BCLK, ADSN, and SWR and CYCLEN to control read and write operations and generate SRDYN to insert the wait state, if necessary, when VLBUSN = 0. For read, the data must be held until RDYRTNN is asserted.

The EISA-like burst transfer is supported using synchronous interface signals and DATACSN when I/O signal VLBUSN = 1. Both the system/host/memory and KSZ8841M are capable of inserting wait states. To set the system/host/memory to insert a wait state, assert RDYRTNN signal. To set the KSZ8841M to insert a wait state, assert SRDYN signal.

Queue Management Unit (QMU)

The Queue Management Unit (QMU) manages packet traffic between the MAC/PHY interface and the system host. It has built-in packet memory for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). Each queue contains 4KB of memory for back-to-back, non-blocking frame transfer performance. It provides a group of control registers for system control, frame status registers for current packet transmit/receive status, and interrupts to inform the host of the real time TX/RX status.

Transmit Queue (TXQ) Frame Format

The frame format for the transmit queue is shown in the following Table 3. The first word contains the control information for the frame to transmit. The second word is used to specify the total number of bytes of the frame. The packet data follows. The packet data area holds the frame itself. It may or may not include the CRC checksum depending upon whether hardware CRC checksum generation is enabled.

Multiple frames can be pipelined in both the transmit queue and receive queue as long as there is enough queue memory, thus avoiding overrun. For each transmitted frame, the transmit status information for the frame is located in the TXSR register.

Packet Memory Address Offset	**Bit 15** **2nd Byte** **Bit 0** **1st Byte**
0	Control Word
2	Byte Count
4 - up	Transmit Packet Data (maximum size is 1916)

Table 3. Frame Format for Transmit Queue

Since multiple packets can be pipelined into the TX packet memory for transmit, the transmit status reflects the status of the packet that is currently being transferred on the MAC interface, which may or may not be the last queued packet in the TX queue.

The transmit control word is the first 16-bit word in the TX packet memory, followed by a 16-bit byte count. It must be word aligned. Each control word corresponds to one TX packet. Table 4 gives the transmit control word bit fields.

Bit	**Description**
15	**TXIC Transmit Interrupt on Completion** When this bit is set, the KSZ8841M sets the transmit interrupt after the present frame has been transmitted.
14-6	Reserved.
5-0	**TXFID Transmit Frame ID** This field specifies the frame ID that is used to identify the frame and its associated status information in the transmit status register.

Table 4. Transmit Control Word Bit Fields

The transmit Byte Count specifies the total number of bytes to be transmitted from the TXQ. Its format is given in Table 5.

Bit	Description
15-11	Reserved.
10-0	**TXBC Transmit Byte Count** Transmit Byte Count. Hardware uses the byte count information to conserve the TX buffer memory for better utilization of the packet memory. Note: The hardware behavior is unknown if an incorrect byte count information is written to this field. Writing a 0 value to this field is not permitted.

Table 5. Transmit Byte Count Format

The data area contains six bytes of Destination Address (DA) followed by six bytes of Source Address (SA), followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The KSZ8841M does not insert its own SA. The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the KSZ8841M. It is treated transparently as data both for transmit operations.

Receive Queue (RXQ) Frame Format

The frame format for the receive queue is shown in Table 6. The first word contains the status information for the frame received. The second word is the total number of bytes of the RX frame. Following that is the packet data area. The packet data area holds the frame itself. It may or may not include the CRC checksum depending on whether hardware CRC stripping is enabled.

Packet Memory Address Offset	Bit 15 2^{nd} Byte	Bit 0 1^{st} Byte
0	Status Word	
2	Byte Count	
4 - up	Receive Packet Data (maximum size is 1916)	

Table 6. Frame Format for Receive Queue

For receive, the packet receive status always reflects the receive status of the packet received in the current RX packet memory (see Table 7). The RXSR register indicates the status of the current received frame.

Bit	Description
15	**RXFV Receive Frame Valid** When set, this field indicates that the present frame in the receive packet memory is valid. The status information currently in this location is also valid. When clear, it indicates that there is either no pending receive frame or that the current frame is still in the process of receiving.
14-8	Reserved.
7	**RXBF Receive Broadcast Frame** When set, it indicates that this frame has a broadcast address.
6	**RXMF Receive Multicast Frame** When set, it indicates that this frame has a multicast address (including the broadcast address).
5	**RXUF Receive Unicast Frame** When set, it indicates that this frame has a unicast address.
4	Reserved.
3	**RXFT Receive Frame Type** When set, it indicates that the frame is an Ethernet-type frame (frame length is greater than 1500 bytes). When clear, it indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames.
2	**RXTL Receive Frame Too Long** When set, it indicates that the frame length exceeds the maximum size of 1518 bytes. Frames that are too long are passed to the host only if the pass bad frame bit is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.

Bit	Description
1	**RXRF Receive Runt Frame** When set, it indicates that a frame was damaged by a collision or had a premature termination before the collision window passed. Runt frames are passed to the host only if the pass bad frame bit is set.
0	**RXCE Receive CRC Error** When set, it indicates that a CRC error has occurred on the current received frame. CRC error frames are passed to the host only if the pass bad frame bit is set.

Table 7. RXQ Receive Packet Status Word

Table 8 gives the format of the RX byte count field.

Bit	Description
15-11	Reserved
10-0	RXBC Receive Byte Count Receive Byte Count up to 1916 bytes

Table 8. RXQ Receive Packet Byte Count Word

EEPROM Interface

It is optional in the KSZ8841M to use an external EEPROM. In the case that an EEPROM is not used, the EEEN pin must be tied Low or floating.

An external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the host MAC address, base address, and default configuration settings. The KSZ8841M can detect if the EEPROM is a 1KB (93C46) or 4KB (93C66) EEPROM device (the 93C46 and the 93C66 are typical EEPROM devices). The EEPROM is organized as 16-bit mode.

If the EEEN pin is pulled high, then the KSZ8841M performs an automatic read of the external EEPROM words 0H to 6H after the de-assertion of Reset. The EEPROM values are placed in certain host-accessible registers. EEPROM read/write functions can also be performed by software read/writes to the EEPCR registers.

The KSZ8841M EEPROM format is given in Table 9.

WORD	15 8	7 0
0H	Base Address	
1H	Host MAC Address Byte 2	Host MAC Address Byte 1
2H	Host MAC Address Byte 4	Host MAC Address Byte 3
3H	Host MAC Address Byte 6	Host MAC Address Byte 5
4H	Reserved	
5H	Reserved	
6H	ConfigParam (see Table 10)	
7H-3FH	Not used for KSZ8841M (available for user to use)	

Table 9. KSZ8841M EEPROM Format

The format for ConfigParam is shown in Table 10.

Bit	Bit Name	Description
15	Reserved	Reserved
14	NO_SRST	**No Soft Reset** When this bit is set, indicates that KSZ8841M transitioning from D3_hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3_hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When this bit is clear, KSZ8841M performs an internal reset upon transitioning from D3_hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon trasition from the D3_hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3_hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. This bit is loaded to bit 3 of PMCS register
13	Reserved	Reserved.
12	PME_D2	**PME Support D2** When this bit is set, the KSZ8841M asserts PME event (pin 14) when the KSZ8841M is in D2 state and PME_EN is set. Otherwise, the KSZ8841M does not assert PME event when the KSZ8841M is in D2 state. This bit is loaded to bit 13 of PMCR register
11	PME_D1	**PME Support D1** When this bit is set, the KSZ8841M asserts PME event (pin 14) when the KSZ8841M is in D1 state and PME_EN is set. Otherwise, the KSZ8841M does not assert PME event when the KSZ8841M is in D1 state. This bit is loaded to bit 12 of PMCR register.
10	D2_SUP	**D2 Support** When this bit is set, the KSZ8841M supports D2 power state. This bit is loaded to bit 10 of PMCR register.
9	D1_SUP	**D1 Support** When this bit is set, the KSZ8841M supports D1 power state. This bit is loaded to bit 9 of PMCR register.
8-2	Reserved	Reserved.
1	Clock_Rate	Internal clock rate selection 0: 125 MHz 1: 25 MHz Note: At power up, this chip operates on 125 MHz clock. The internal frequency can be dropped to 25 MHz via the external EEPROM.
0	ASYN_8bit	**Async 8-bit bus select** 1= bus is configured for 16-bit width 0= bus is configured for 8-bit width This bit is loaded to bit 0 of PMCR register (32-bit width, KSZ8841-32MQL, don't care this bit setting)

Table 10. ConfigParam Word in EEPROM Format

Loopback Support

The KSZ8841M provides Near-end (Remote) loopback support for remote diagnostic of failure. In loopback mode, the speed at the PHY port will be set to 100BASE-TX full-duplex mode.

Near-end (Remote) Loopback

Near-end (Remote) loopback is conducted at PHY port 1of the KSZ8841M. The loopback path starts at the PHY port's receive inputs (RXP1/RXM1), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXP1/TXM1).

Bit [1] of register P1PHYCTRL is used to enable near-end loopback for port 1. Alternatively, Bit [9] of register P1SCSLMD can also be used to enable near-end loopback. The ports 1 near-end loopback path is illustrated in the following Figure 12.

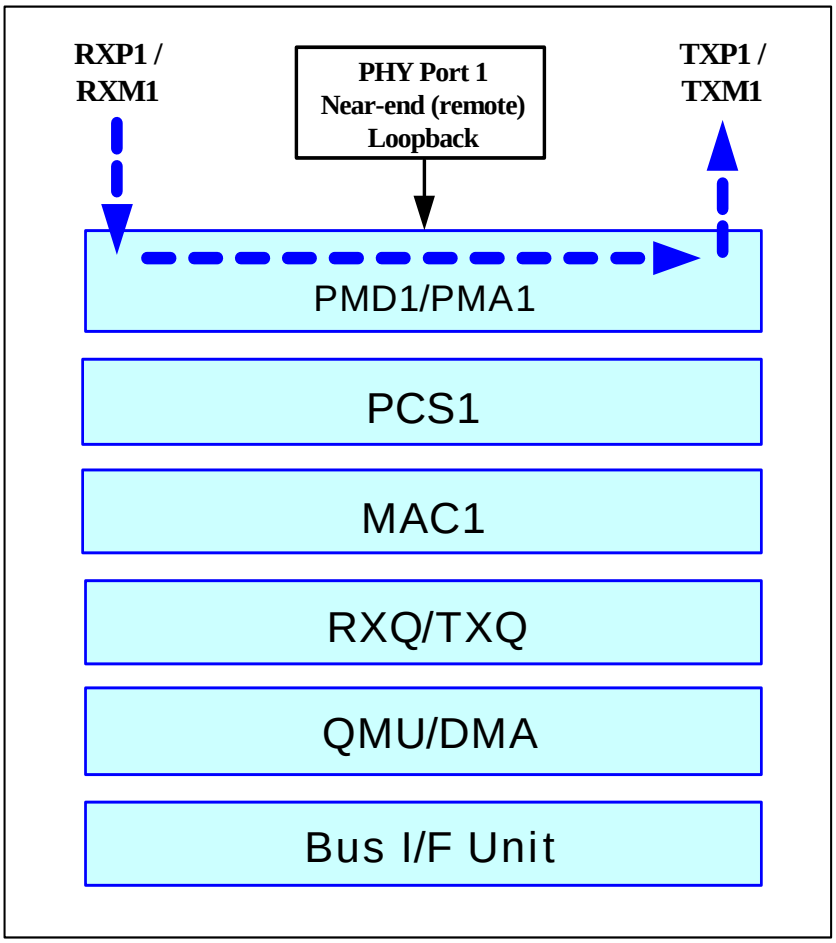


Figure 12. PHY Port 1 Near-end (Remote) Loopback Path

CPU Interface I/O Registers

The KSZ8841M provides an EISA-like, ISA-like, or VLBUS-like bus interface for the CPU to access its internal I/O registers. I/O registers serve as the address that the microprocessor uses when communicating with the device. This is used for configuring operational settings, reading or writing control, status information, and transferring packets by reading and writing through the packet data registers.

I/O Registers

Input/Output (I/O) registers are limited to 16 locations as required by most ISA bus-based systems; therefore, registers are assigned to different banks. The last word of the I/O register locations (0xE - 0xF) is shared by all banks and can be used to change the bank in use.

The following I/O Space Mapping Tables apply to 8, 16 or 32-bit bus products. Depending upon the bus interface used and byte enable signals (BE[3:0]N control byte access), each I/O access can be performed as an 8-bit, 16-bit, or 32-bit operation. (The KSZ8841M is not limited to 8/16-bit performance and 32-bit read/write are also supported).

Internal I/O Space Mapping

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 0**	**Bank 1**	**Bank 2**	**Bank 3**	**Bank 4**	**Bank 5**	**Bank 6**	**Bank 7**
0x0 To 0x3	0x0 - 0x1	0x0	Base Address [7:0]	Reserved	Host MAC Address Low [7:0]	On-Chip Bus Control [7:0]	Wakeup Frame0 CRC0 [7:0]	Wakeup Frame1 CRC0 [7:0]	Wakeup Frame2 CRC0 [7:0]	Wakeup Frame3 CRC0 [7:0]
		0x1	Base Address [15:8]		Host MAC Address Low [15:8]	On-Chip Bus Control [15:8]	Wakeup Frame0 CRC0 [15:8]	Wakeup Frame1 CRC0 [15:8]	Wakeup Frame2 CRC0 [15:8]	Wakeup Frame3 CRC0 [15:8]
	0x2 - 0x3	0x2	Reserved	Reserved	Host MAC Address Mid [7:0]	EEPROM Control [7:0]	Wakeup Frame0 CRC1 [7:0]	Wakeup Frame1 CRC1 [7:0]	Wakeup Frame2 CRC1 [7:0]	Wakeup Frame3 CRC1 [7:0]
		0x3			Host MAC Address Mid [15:8]	EEPROM Control [15:8]	Wakeup Frame0 CRC1 [15:8]	Wakeup Frame1 CRC1 [15:8]	Wakeup Frame2 CRC1 [15:8]	Wakeup Frame3 CRC1 [15:8]
0x4 To 0x7	0x4 - 0x5	0x4	QMU RX Flow Control Watermark [7:0]	Reserved	Host MAC Address High [7:0]	Memory BIST Info [7:0]	Wakeup Frame0 Byte Mask0 [7:0]	Wakeup Frame1 Byte Mask0 [7:0]	Wakeup Frame2 Byte Mask0 [7:0]	Wakeup Frame3 Byte Mask0 [7:0]
		0x5	QMU RX Flow Control Watermark [15:8]		Host MAC Address High [15:8]	Memory BIST Info [15:8]	Wakeup Frame0 Byte Mask0 [15:8]	Wakeup Frame1 Byte Mask0 [15:8]	Wakeup Frame2 Byte Mask0 [15:8]	Wakeup Frame3 Byte Mask0 [15:8]
	0x6 - 0x7	0x6	Bus Error Status [7:0]	Reserved	Reserved	Global Reset [7:0]	Wakeup Frame0 Byte Mask1 [7:0]	Wakeup Frame1 Byte Mask1 [7:0]	Wakeup Frame2 Byte Mask1 [7:0]	Wakeup Frame3 Byte Mask1 [7:0]
		0x7	Bus Error Status [15:8]			Global Reset [15:8]	Wakeup Frame0 Byte Mask1 [15:8]	Wakeup Frame1 Byte Mask1 [15:8]	Wakeup Frame2 Byte Mask1 [15:8]	Wakeup Frame3 Byte Mask1 [15:8]
0x8 To 0xB	0x8 - 0x9	0x8	Bus Burst Length [7:0]	Reserved	Reserved	Power Management Capabilities [7:0]	Wakeup Frame0 Byte Mask2 [7:0]	Wakeup Frame1 Byte Mask2 [7:0]	Wakeup Frame2 Byte Mask2 [7:0]	Wakeup Frame3 Byte Mask2 [7:0]
		0x9	Bus Burst Length [15:8]			Power Management Capabilities [15:8]	Wakeup Frame0 Byte Mask2 [15:8]	Wakeup Frame1 Byte Mask2 [15:8]	Wakeup Frame2 Byte Mask2 [15:8]	Wakeup Frame3 Byte Mask2 [15:8]
	0xA - 0xB	0xA	Reserved			Wakeup Frame Control [7:0]	Wakeup Frame0 Byte Mask3 [7:0]	Wakeup Frame1 Byte Mask3 [7:0]	Wakeup Frame2 Byte Mask3 [7:0]	Wakeup Frame3 Byte Mask3 [7:0]
		0xB				Wakeup Frame Control [15:8]	Wakeup Frame0 Byte Mask3 [15:8]	Wakeup Frame1 Byte Mask3 [15:8]	Wakeup Frame2 Byte Mask3 [15:8]	Wakeup Frame3 Byte Mask3 [15:8]
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Internal I/O Space Mapping (continued)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 8**	**Bank 9**	**Bank 10**	**Bank 11**	**Bank 12**	**Bank 13**	**Bank 14**	**Bank 15**
0x0 To 0x3	0x0 - 0x1	0x0	Reserved							
		0x1								
	0x2 - 0x3	0x2	Reserved							
		0x3								
0x4 To 0x7	0x4 - 0x5	0x4	Reserved							
		0x5								
	0x6 - 0x7	0x6	Reserved							
		0x7								
0x8 To 0xB	0x8 - 0x9	0x8	Reserved							
		0x9								
	0xA - 0xB	0xA	Reserved							
		0xB								
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Internal I/O Space Mapping (continued)

<table>
<tr><th colspan="3">I/O Register Location</th><th colspan="8">Bank Location</th></tr>
<tr><th>32-Bit</th><th>16-Bit</th><th>8-Bit</th><th>Bank 16</th><th>Bank 17</th><th>Bank 18</th><th>Bank 19</th><th>Bank 20</th><th>Bank 21</th><th>Bank 22</th><th>Bank 23</th></tr>
<tr><td rowspan="8">0x0
To
0x3</td><td rowspan="2">0x0
- 0x1</td><td>0x0</td><td>Transmit Control [7:0]</td><td>TXQ Command [7:0]</td><td>Interrupt Enable [7:0]</td><td>Multicast Table 0 [7:0]</td><td colspan="4" rowspan="2">Reserved</td></tr>
<tr><td>0x1</td><td>Transmit Control [15:8]</td><td>TXQ Command [15:8]</td><td>Interrupt Enable [15:8]</td><td>Multicast Table 0 [15:8]</td></tr>
<tr><td rowspan="2">0x2
- 0x3</td><td>0x2</td><td>Transmit Status [7:0]</td><td>RXQ Command [7:0]</td><td>Interrupt Status [7:0]</td><td>Multicast Table 1 [7:0]</td><td colspan="4" rowspan="2">Reserved</td></tr>
<tr><td>0x3</td><td>Transmit Status [15:8]</td><td>RXQ Command [15:8]</td><td>Interrupt Status [15:8]</td><td>Multicast Table 1 [15:8]</td></tr>
<tr><td rowspan="8">0x4
To
0x7</td><td rowspan="2">0x4
- 0x5</td><td>0x4</td><td>Receive Control [7:0]</td><td>TX Frame Data Pointer [7:0]</td><td>Receive Status [7:0]</td><td>Multicast Table 2 [7:0]</td><td colspan="4" rowspan="2">Reserved</td></tr>
<tr><td>0x5</td><td>Receive Control [15:8]</td><td>TX Frame Data Pointer [15:8]</td><td>Receive Status [15:8]</td><td>Multicast Table 2 [15:8]</td></tr>
<tr><td rowspan="2">0x6
- 0x7</td><td>0x6</td><td rowspan="2">Reserved</td><td>RX Frame Data Pointer [7:0]</td><td>Receive Byte Counter [7:0]</td><td>Multicast Table 3 [7:0]</td><td colspan="4" rowspan="2">Reserved</td></tr>
<tr><td>0x7</td><td>RX Frame Data Pointer [15:8]</td><td>Receive Byte Counter [15:8]</td><td>Multicast Table 3 [15:8]</td></tr>
<tr><td rowspan="8">0x8
To
0xB</td><td rowspan="2">0x8
- 0x9</td><td>0x8</td><td>TXQ Memory Information [7:0]</td><td>QMU Data Low [7:0]</td><td>Early Transmit [7:0]</td><td>Power Management Control/Status [7:0]</td><td colspan="4" rowspan="2">Reserved</td></tr>
<tr><td>0x9</td><td>TXQ Memory Information [15:8]</td><td>QMU Data Low [15:8]</td><td>Early Transmit [15:8]</td><td>Power Management Control/Status [15:8]</td></tr>
<tr><td rowspan="2">0xA
- 0xB</td><td>0xA</td><td>RXQ Memory Information [7:0]</td><td>QMU Data High [7:0]</td><td>Early Receive [7:0]</td><td colspan="5" rowspan="2">Reserved</td></tr>
<tr><td>0xB</td><td>RXQ Memory Information [15:8]</td><td>QMU Data High [15:8]</td><td>Early Receive [15:8]</td></tr>
<tr><td rowspan="4">0xC
To
0xF</td><td rowspan="2">0xC
- 0xD</td><td>0xC</td><td colspan="8" rowspan="2">Reserved</td></tr>
<tr><td>0xD</td></tr>
<tr><td rowspan="2">0xE
- 0xF</td><td>0xE</td><td colspan="8">Bank Select [7:0]</td></tr>
<tr><td>0xF</td><td colspan="8">Bank Select [15:8]</td></tr>
</table>

Internal I/O Space Mapping (continued)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 24**	**Bank 25**	**Bank 26**	**Bank 27**	**Bank 28**	**Bank 29**	**Bank 30**	**Bank 31**
0x0 To 0x3	0x0 - 0x1	0x0	Reserved							
		0x1								
	0x2 - 0x3	0x2	Reserved							
		0x3								
0x4 To 0x7	0x4 - 0x5	0x4	Reserved							
		0x5								
	0x6 - 0x7	0x6	Reserved							
		0x7								
0x8 To 0xB	0x8 - 0x9	0x8	Reserved							
		0x9								
	0xA - 0xB	0xA	Reserved							
		0xB								
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Internal I/O Space Mapping (continued)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 32**	**Bank 33**	**Bank 34**	**Bank 35**	**Bank 36**	**Bank 37**	**Bank 38**	**Bank 39**
0x0 To 0x3	0x0 - 0x1	0x0	Chip ID and Enable [7:0]	Reserved						
		0x1	Chip ID and Enable [15:8]							
	0x2 - 0x3	0x2	Reserved							
		0x3								
0x4 To 0x7	0x4 - 0x5	0x4	Reserved							
		0x5								
	0x6 - 0x7	0x6	Reserved							
		0x7								
0x8 To 0xB	0x8 - 0x9	0x8	Reserved							
		0x9								
	0xA - 0xB	0xA	Chip Global Control [7:0]	Reserved						
		0xB	Chip Global Control [15:8]							
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Internal I/O Space Mapping (continued)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 40**	**Bank 41**	**Bank 42**	**Bank 43**	**Bank 44**	**Bank 45**	**Bank 46**	**Bank 47**
0x0 To 0x3	0x0 - 0x1	0x0	Reserved		Indirect Access Control. [7:0]	Reserved		PHY1 MII-Register Basic Control [7:0]	Reserved	PHY1 LinkMD Control/Status [7:0]
		0x1			Indirect Access Control. [15:8]			PHY1 MII-Register Basic Control [15:8]		PHY1 LinkMD Control/Status [15:8]
	0x2 - 0x3	0x2	Reserved		Indirect Access Data 1 [7:0]	Reserved		PHY1 MII-Register Basic Status [7:0]	Reserved	PHY1 Special Control/Status [7:0]
		0x3			Indirect Access Data 1 [15:8]			PHY1 MII-Register Basic Status [15:8]		PHY1 Special Control/Status [15:8]
0x4 To 0x7	0x4 - 0x5	0x4	Reserved		Indirect Access Data 2 [7:0]	Reserved		PHY1 PHYID Low [7:0]	Reserved	
		0x5			Indirect Access Data 2 [15:8]			PHY1 PHYID Low [15:8]		
	0x6 - 0x7	0x6	Reserved		Indirect Access Data 3 [7:0]	Reserved		PHY1 PHYID High [7:0]	Reserved	
		0x7			Indirect Access Data 3 [15:8]			PHY1 PHYID High [15:8]		
0x8 To 0xB	0x8 - 0x9	0x8	Reserved		Indirect Access Data 4 [7:0]	Reserved		PHY1 A.N. Advertisement [7:0]	Reserved	
		0x9			Indirect Access Data 4 [15:8]			PHY1 A.N. Advertisement [15:8]		
	0xA - 0xB	0xA	Reserved		Indirect Access Data 5 [7:0]	Reserved		PHY1 A.N. Link Partner Ability [7:0]	Reserved	
		0xB			Indirect Access Data 5 [15:8]			PHY1 A.N. Link Partner Ability [15:8]		
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Internal I/O Space Mapping (continued)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 48**	**Bank 49**	**Bank 50**	**Bank 51**	**Bank 52**	**Bank 53**	**Bank 54**	**Bank 55**
0x0 To 0x3	0x0 - 0x1	0x0	Reserved	Port 1 PHY Special Control/Status, LinkMD [7:0]	Reserved					
		0x1		Port 1 PHY Special Control/Status, LinkMD [15:8]						
	0x2 - 0x3	0x2	Reserved	Port 1 Control 4 [7:0]	Reserved					
		0x3		Port 1 Control 4 [15:8]						
0x4 To 0x7	0x4 - 0x5	0x4	Reserved	Port 1 Status [7:0]	Reserved					
		0x5		Port 1 Status [15:8]						
	0x6 - 0x7	0x6	Reserved							
		0x7								
0x8 To 0xB	0x8 - 0x9	0x8	Reserved							
		0x9								
	0xA - 0xB	0xA	Reserved							
		0xB								
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Internal I/O Space Mapping (continued)

I/O Register Location			Bank Location							
32-Bit	**16-Bit**	**8-Bit**	**Bank 56**	**Bank 57**	**Bank 58**	**Bank 59**	**Bank 60**	**Bank 61**	**Bank 62**	**Bank 63**
0x0 To 0x3	0x0 - 0x1	0x0	Reserved							
		0x1								
	0x2 - 0x3	0x2	Reserved							
		0x3								
0x4 To 0x7	0x4 - 0x5	0x4	Reserved							
		0x5								
	0x6 - 0x7	0x6	Reserved							
		0x7								
0x8 To 0xB	0x8 - 0x9	0x8	Reserved							
		0x9								
	0xA - 0xB	0xA	Reserved							
		0xB								
0xC To 0xF	0xC - 0xD	0xC	Reserved							
		0xD								
	0xE - 0xF	0xE	Bank Select [7:0]							
		0xF	Bank Select [15:8]							

Register Map: MAC and PHY

Do not write to bit values or to registers defined as Reserved. Manipulating reserved bits or registers causes unpredictable and often fatal results. If the user wants to write to these reserved bits, the user has to read back these reserved bits (RO or RW) first, then “OR” with the read value of the reserved bits and write back to these reserved bits.

Bit Type Definition

RO = Read only.

RW = Read/Write.

W1C = Write 1 to Clear (writing a one to this bit clears it).

Bank 0-63 Bank Select Register (0x0E): BSR (same location in all Banks)

The bank select register is used to select or to switch between different sets of register banks for I/O access.

There are a total of 64 banks available to select, including the built-in switch engine registers.

Bit	Default Value	R/W	Description
15-6	0x000	RO	Reserved
5-0	0x00	R/W	**BSA Bank Select Address Bits** BSA bits select the I/O register bank in use. This register is always accessible regardless of the register bank currently selected. Notes: The bank select register can be accessed as a doubleword (32-bit) at offset 0xC, as a word (16-bit) at offset 0xE, or as a byte (8-bit) at offset 0xE. A doubleword write to offset 0xC writes to the BANK Select Register but does not write to registers 0xC and 0xD; it only writes to register 0xE.

Bank 0 Base Address Register (0x00): BAR

This register holds the base address for decoding a device access. Its value is loaded from the external EEPROM (0x0H) upon a power-on reset if the EEPROM Enable (EEEN) pin is tied to High. Its value can also be modified after reset. Writing to this register does not store the value into the EEPROM. When the EEEN pin is tied to Low, the default base address is 0x300.

Bit	Default Value	R/W	Description
15-8	0x03 if EEEN is Low or, the value from EEPROM if EEEN is High	RW	**BARH Base Address High** These bits are compared against the address on the bus ADDR[15:8] to determine the BASE for the KSZ8841M registers.
7-5	0x00 if EEEN is Low or, the value from EEPROM if EEEN is High	RW	**BARL Base Address Low** These bits are compared against the address on the bus ADDR[7:5] to determine the BASE for the KSZ8841M registers.
4-0	0x00	RO	Reserved

Bank 0 QMU RX Flow Control High Watermark Configuration Register (0x04): QRFCR

This register contains the user defined QMU RX Queue high watermark configuration bit as below.

Bit	Default Value	R/W	Description
15-13	0x0	RO	Reserved
12	0	RW	**QMU RX Flow Control High Watermark Configuration** 0: 3 KBytes 1: 2 KBytes
11-0	0x000	RO	Reserved

Bank 0 Bus Error Status Register (0x06): BESR

This register flags the different kinds of errors on the host bus.

Bit	Default Value	R/W	Description
15	0	RO	**IBEC Illegal Byte Enable Combination** 1: illegal byte enable combination occurs. The illegal combination value can be found from bit 14 to bit 11. 0: legal byte enable combination. Write 1 to clear.
14-11	-	RO	**IBECV Illegal Byte Enable Combination Value** Bit 14: byte enable 3. Bit 13: byte enable 2. Bit 12: byte enable 1. Bit 11: byte enable 0. This value is valid only when bit 15 is set to 1.
10	0	RO	**SSAXFER Simultaneous Synchronous and Asnychronous Transfers** 1: Synchronous and Asnychronous Transfers occur simultaneously. 0: normal. Write 1 to clear.
9-0	0x000	RO	Reserved.

Bank 0 Bus Burst Length Register (0x08): BBLR

Before the burst can be sent, the burst length needs to be programmed.

Bit	Default Value	R/W	Description
15	0	RO	Reserved.
14-12	0x0	RW	**BRL Burst Length** (for burst read and write) 000: single. 011: fixed burst read length of 4. 101: fixed burst read length of 8. 111: fixed burst read length of 16.
11-0	0x000	RO	Reserved.

Bank 1: Reserved

Except Bank Select Register (0xE).

Bank 2 Host MAC Address Register Low (0x00): MARL

This register along with the other two Host MAC address registers are loaded starting at word location 0x1 of the EEPROM upon hardware reset. The software driver can modify the register, but it will not modify the original Host MAC address value in the EEPROM. These six bytes of Host MAC address in external EEPROM are loaded to these three registers as mapping below:

MARL[15:0] = EEPROM 0x1(MAC Byte 2 and 1)

MARM[15:0] = EEPROM 0x2(MAC Byte 4 and 3)

MARH[15:0] = EEPROM 0x3(MAC Byte 6 and 5)

The Host MAC address is used to define the individual destination address that the KSZ8841M responds to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received from right to left (LSB to MSB). For example, the actual transmitted and received bits are on the order of 10000000 11000100 10100010 11100110 10010001 11010101. These three registers value for Host MAC address 01:23:45:67:89:AB will be held as below:

MARL[15:0] = 0x89AB

MARM[15:0] = 0x4567

MARH[15:0] = 0x0123

The following table shows the register bit fields for Low word of Host MAC address.

Bit	Default Value	R/W	Description
15-0	-	RW	**MARL MAC Address Low** The least significant word of the MAC address.

Bank 2 Host MAC Address Register Middle (0x02): MARM

The following table shows the register bit fields for middle word of Host MAC address.

Bit	Default Value	R/W	Description
15-0	-	RW	**MARM MAC Address Middle** The middle word of the MAC address.

Bank 2 Host MAC Address Register High (0x04): MARH

The following table shows the register bit fields for high word of Host MAC address.

Bit	Default Value	R/W	Description
15-0	-	RW	**MARH MAC Address High** The Most significant word of the MAC address.

Bank 3 On-Chip Bus Control Register (0x00): OBCR

This register controls the on-chip bus speed for the KSZ8841M. It is used for power management when the external host CPU is running at a slow frequency. The default of the on-chip bus speed is 125 MHz without EEPROM. When the external host CPU is running at a higher clock rate, the on-chip bus should be adjusted for the best performance.

Bit	Default Value	R/W	Description
15-2	-	RO	Reserved.
1-0	0x0	RW	**OBSC On-Chip Bus Speed Control** 00: 125MHz. 01: 62.5MHz. 10: 41.66MHz. 11: 25MHz. Note: When external EEPROM is enabled, the bit 1 in Configparm word (0x6H) is used to contol this speed as below: Bit 1 = 0 , this value will be 00 for 125 MHz. Bit 1 = 1 , this value will be 11 for 25 MHz. (User still can write these two bits to change speed after EEPROM data loaded)

Bank 3 EEPROM Control Register (0x02): EEPCR

To support an external EEPROM, tie the EEPROM Enable (EEEN) pin to High; otherwise, tie it to Low. If an external EEPROM is not used, the default chip Base Address (0x300), and the software programs the host MAC address. If an EEPROM is used in the design (EEPROM Enable pin to High), the chip Base Address and host MAC address are loaded from the EEPROM immediately after reset. The KSZ8841M allows the software to access (read and write) the EEPROM directly; that is, the EEPROM access timing can be fully controlled by the software if the EEPROM Software Access bit is set.

Bit	Default Value	R/W	Description
15-5	-	RO	Reserved.
4	0	RW	**EESA EEPROM Software Access** 1: enable software to access EEPROM through bit 3 to bit 0. 0: disable software to access EEPROM.
3	-	RO	**EECB EEPROM Status Bit** Data Receive from EEPROM. This bit directly reads the EEDI pin.
2-0	0x0	RW	**EECB EEPROM Control Bits** Bit 2: Data Transmit to EEPROM. This bit directly controls the device's EEDO pin. Bit 1: Serial Clock. This bit directly controls the device's EESK pin. Bit 0: Chip Select for EEPROM. This bit directly controls the device's EECS pin.

Bank 3 Memory BIST Info Register (0x04): MBIR

Bit	Default Value	R/W	Description
15-13	0x0	RO	Reserved.
12	-	RO	**TXMBF TX Memory Bist Finish** When set, it indicates the Memory Built In Self Test completion for the TX Memory.
11	-	RO	**TXMBFA TX Memory Bist Fail** When set, it indicates the Memory Built In Self Test has failed.
10-5	-	RO	Reserved
4	-	RO	**RXMBF RX Memory Bist Finish** When set, it indicates the Memory Built In Self Test completion for the RX Memory.
3	-	RO	**RXMBFA RX Memory Bist Fail** When set, it indicates the Memory Built In Self Test has failed.
2-0	-	RO	Reserved.

Bank 3 Global Reset Register (0x06): GRR

This register controls the global reset function with information programmed by the CPU.

Bit	Default Value	R/W	Description
15-1	0x0000	RO	Reserved.
0	0	RW	**Global Soft Reset** = 1 software reset is active. = 0 software reset is inactive. Software reset will affect PHY, MAC, QMU, DMA, and the switch core, only the BIU (base address registers) remains unaffected by a software reset.

Bank 3 Power Management Capabilities Register (0x08): PMCR

This register is a read-only register that provides information on the K8841M power management capabilities. These bits are automatically downloaded from Configparam word of EEPROM , if pin EEEN is high (enabled EEPROM)

Bit	Default Value	R/W	Description
15	0	RO	**PME Support D3 (cold)** This bit defaults to 0, so the KSZ8841M does not support D3(cold)
14	1	RO	**PME Support D3 (hot)** This bit is 1 only,it is indicating that the KSZ8841M can assert PME event (PMEN pin 14) in D3(hot) power state.(see bit1:0 in PMCS register)
13	0	RO	**PME Support D2** If this bit is set, the wake-up signals will assert PME event (PMEN pin 14) when the KSZ8841M is in D2 power state and PME_EN (see bit8 in PMCS register) is set. Otherwise, the KSZ8841M does not assert PME event (PMEN pin 14) when the KSZ8841M is in D2 power state. The value of this bit is loaded from the PME_D2 bit of 0x6 in the serial EEPROM (without an EEPROM, this bit defaults to 0).
12	0	RO	**PME Support D1** If this bit is set, the wake-up signals will assert PME event (PMEN pin 14) when the KSZ8841M is in D1 power state and PME_EN (see bit8 in PMCS register) is set. Otherwise, the KSZ8841M does not assert PME event (PMEN pin 14) when the KSZ8841M is in D1 power state. The value of this bit loaded from the PME_D1 bit of 0x6 in the serial EEPROM (without an EEPROM, this bit defaults to 0).
11	0	RO	**PME Support D0** This bit defaults to 0, it is indicating that the KSZ8841M does not assert PME event

Bit	Default Value	R/W	Description
			(PMEN pin 14) in D0 power state.
10	0	RO	**D2 Support** If this bit is set, it indicates that the KSZ8841M support D2 power state. The value of this bit is loaded from the D2_SUP bit of 0x6 in the serial EEPROM (without an EEPROM, this bit defaults to 0).
9	0	RO	**D1 Support** If this bit is set, it indicates that the KSZ8841M support D1 power state. The value of this bit is loaded from the D1_SUP bit of 0x6 in the serial EEPROM (without an EEPROM, this bit defaults to 0).
8-1	-	RO	Reserved.
0	-	RO	**Bus Configuration** (only for KSZ8841-16MQL device) 1: bus width is 16 bits. 0: bus width is 8 bits. (this bit, ASYN_8bit, is only avaiable when EEPROM is enabled)

Bank 3 Wakeup Frame Control Register (0x0A): WFCR

This register holds control information programmed by the CPU to control the wake up frame function.

Bit	Default Value	R/W	Description
15-8	0x00	RO	Reserved.
7	0	RW	**MPRXE** Magic Packet RX Enable When set, it enables the magic packet pattern detection. When reset, the magic packet pattern detection is disabled.
6-4	0x0	RO	Reserved.
3	0	RW	**WF3E** Wake up Frame 3 Enable When set, it enables the Wake up frame 3 pattern detection. When reset, the Wake up frame 3 pattern detection is disabled.
2	0	RW	**WF2E** Wake up Frame 2 Enable When set, it enables the Wake up frame 2 pattern detection. When reset, the Wake up frame 2 pattern detection is disabled.
1	0	RW	**WF1E** Wake up Frame 1 Enable When set, it enables the Wake up frame 1 pattern detection. When reset, the Wake up frame 1 pattern detection is disabled.
0	0	RW	**WF0E** Wake up Frame 0 Enable When set, it enables the Wake up frame 0 pattern detection. When reset, the Wake up frame 0 pattern detection is disabled.

Bank 4 Wakeup Frame 0 CRC0 Register (0x00): WF0CRC0

This register contains the expected CRC values of the Wake up frame 0 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0x0000	RW	**WF0CRC0** Wake up Frame 0 CRC (lower 16 bits) The expected CRC value of a Wake up frame 0 pattern.

Bank 4 Wakeup Frame 0 CRC1 Register (0x02): WF0CRC1

This register contains the expected CRC values of the Wake up frame 0 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF0CRC1** Wake up Frame 0 CRC (upper 16 bits). The expected CRC value of a Wake up frame 0 pattern.

Bank 4 Wakeup Frame 0 Byte Mask 0 Register (0x04): WF0BM0

This register contains the first 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the first byte of the Wake up frame 0, setting bit 15 selects the 16th byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF0BM0** Wake up Frame 0 Byte Mask 0 The first 16 bytes mask of a Wake up frame 0 pattern.

Bank 4 Wakeup Frame 0 Byte Mask 1 Register (0x06): WF0BM1

This register contains the next 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 0. Setting bit 15 selects the 32nd byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF0BM1** Wake up Frame 0 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake up frame 0 pattern.

Bank 4 Wakeup Frame 0 Byte Mask 2 Register (0x08): WF0BM2

This register contains the next 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 0. Setting bit 15 selects the 48th byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF0BM2** Wake-up Frame 0 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 0 pattern.

Bank 4 Wakeup Frame 0 Byte Mask 3 Register (0x0A): WF0BM3

This register contains the last 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 0. Setting bit 15 selects the 64th byte of the Wake up frame 0.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF0BM3** Wake-up Frame 0 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 0 pattern.

Bank 5 Wakeup Frame 1 CRC0 Register (0x00): WF1CRC0

This register contains the expected CRC values of the Wake up frame 1 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF1CRC0** Wake-up frame 1 CRC (lower 16 bits). The expected CRC value of a Wake-up frame 1 pattern.

Bank 5 Wakeup Frame 1 CRC1 Register (0x02): WF1CRC1

This register contains the expected CRC values of the Wake up frame 1 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF1CRC1** Wake-up frame 1 CRC (upper 16 bits). The expected CRC value of a Wake-up frame 1 pattern.

Bank 5 Wakeup Frame 1 Byte Mask 0 Register (0x04): WF1BM0

This register contains the first 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the first byte of the Wake up frame 1, setting bit 15 selects the 16th byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF1BM0** Wake-up frame 1 Byte Mask 0. The first 16 bytes mask of a Wake-up frame 1 pattern.

Bank 5 Wakeup Frame 1 Byte Mask 1 Register (0x06): WF1BM1

This register contains the next 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 1. Setting bit 15 selects the 32nd byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF1BM1** Wake-up frame 1 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake-up frame 1 pattern.

Bank 5 Wakeup Frame 1 Byte Mask 2 Register (0x08): WF1BM2

This register contains the next 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 1. Setting bit 15 selects the 48th byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF1BM2** Wake-up frame 1 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 1 pattern.

Bank 5 Wakeup Frame 1 Byte Mask 3 Register (0x0A): WF1BM3

This register contains the last 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 1. Setting bit 15 selects the 64th byte of the Wake up frame 1.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF1BM3** Wake-up frame 1 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 1 pattern.

Bank 6 Wakeup Frame 2 CRC0 Register (0x00): WF2CRC0

This register contains the expected CRC values of the Wake up frame 2 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2CRC0** Wake-up frame 2 CRC (lower 16 bits). The expected CRC value of a Wake-up frame 2 pattern.

Bank 6 Wakeup Frame 2 CRC1 Register (0x02): WF2CRC1

This register contains the expected CRC values of the wake-up frame 2 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2CRC1** Wake-up frame 2 CRC (upper 16 bits). The expected CRC value of a Wake-up frame 2 pattern.

Bank 6 Wakeup Frame 2 Byte Mask 0 Register (0x04): WF2BM0

This register contains the first 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the first byte of the Wake up frame 2, setting bit 15 selects the 16th byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2BM0** Wake-up frame 2 Byte Mask 0. The first 16 bytes mask of a Wake-up frame 2 pattern.

Bank 6 Wakeup Frame 2 Byte Mask 1 Register (0x06): WF2BM1

This register contains the next 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 2. Setting bit 15 selects the 32nd byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2BM1** Wake-up frame 2 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake-up frame 2 pattern.

Bank 6 Wakeup Frame 2 Byte Mask 2 Register (0x08): WF2BM2

This register contains the next 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 2. Setting bit 15 selects the 48th byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2BM2** Wake-up frame 2 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 2 pattern.

Bank 6 Wakeup Frame 2 Byte Mask 3 Register (0x0A): WF2BM3

This register contains the last 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 2. Setting bit 15 selects the 64th byte of the Wake up frame 2.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF2BM3** Wake-up frame 2 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 2 pattern.

Bank 7 Wakeup Frame 3 CRC0 Register (0x00): WF3CRC0

This register contains the expected CRC values of the Wake up frame 3 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake-up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3CRC0** Wake-up frame 3 CRC (lower 16 bits). The expected CRC value of a Wake up frame 3pattern.

Bank 7 Wakeup Frame 3 CRC1 Register (0x02): WF3CRC1

This register contains the expected CRC values of the Wake up frame 3 pattern.

The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3CRC1** Wake-up frame 3 CRC (upper 16 bits). The expected CRC value of a Wake up frame 3 pattern.

Bank 7 Wakeup Frame 3 Byte Mask 0 Register (0x04): WF3BM0

This register contains the first 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the first byte of the Wake up frame 3, setting bit 15 selects the 16th byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM0** Wake up Frame 3 Byte Mask 0 The first 16 byte mask of a Wake up frame 3 pattern.

Bank 7 Wakeup Frame 3 Byte Mask 1 Register (0x06): WF3BM1

This register contains the next 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 3. Setting bit 15 selects the 32nd byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM1** Wake up Frame 3 Byte Mask 1 The next 16 bytes mask covering bytes 17 to 32 of a Wake up frame 3 pattern.

Bank 7 Wakeup Frame 3 Byte Mask 2 Register (0x08): WF3BM2

This register contains the next 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 3. Setting bit 15 selects the 48th byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM2** Wake up Frame 3 Byte Mask 2 The next 16 bytes mask covering bytes 33 to 48 of a Wake up frame 3 pattern.

Bank 7 Wakeup Frame 3 Byte Mask 3 Register (0x0A): WF3BM3

This register contains the last 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 3. Setting bit 15 selects the 64th byte of the Wake up frame 3.

Bit	Default Value	R/W	Description
15-0	0	RW	**WF3BM3** Wake up Frame 3 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake up frame 3 pattern.

Bank 8 – 15: Reserved

Except Bank Select Register (0xE).

Bank 16 Transmit Control Register (0x00): TXCR

This register holds control information programmed by the CPU to control the QMU transmit module function.

Bit	Default Value	R/W	Description
15	-	RO	Reserved.
14-13	0x0	RW	Reserved.
12-4	-	RO	Reserved.
3	0x0	RW	**TXFCE Transmit Flow Control Enable** When this bit is set and the KSZ8841M is in full-duplex mode, flow control is enabled. The KSZ8841M transmits a PAUSE frame when the Receive Buffer capacity reaches a threshold level that will cause the buffer to overflow. When this bit is set and the KSZ8841M is in half-duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
2	0x0	RW	**TXPE Transmit Padding Enable** When this bit is set, the KSZ8841M automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit requires enabling the add CRC feature to avoid CRC errors for the transmit packet.
1	0x0	RW	**TXCE Transmit CRC Enable** When this bit is set, the KSZ8841M automatically adds a CRC checksum field to the end of a transmit frame.
0	0x0	RW	**TXE Transmit Enable** When this bit is set, the transmit module is enabled and placed in a running state. When reset, the transmit process is placed in the stopped state after the transmission of the current frame is completed.

Bank 16 Transmit Status Register (0x02): TXSR

This register keeps the status of the last transmitted frame.

Bit	Default Value	R/W	Description
15	0x0	RO	Reserved.
14	0x0	RO	**TXUR Transmit Underrun** This bit is set when underrun occurs. Note: This is a fatal status. Software should guarantee that no underrun condition occurred when enabling the early transmit function. The system or the QMU requires a reset or restart to recover from an underrun condition. To aviod transmit underun condition, the user has to make sure that the host interface speed (bandwidth) is faster than the ethernet port.
13	0x0	RO	**TXLC Transmit Late Collision** This bit is set when a transmit Late Collision occurs.
12	0x0	RO	**TXMC Transmit Maximum Collision** This bit is set when a transmit Maximum Collision is reached.
11-6	-	RO	Reserved.
5-0	-	RO	**TXFID Transmit Frame ID** This field identifies the transmitted frame. All of the transmit status information in this register belongs to the frame with this ID.

Bank 16 Receive Control Register (0x04): RXCR

This register holds control information programmed by the CPU to control the receive function.

Bit	Default Value	R/W	Description
15-11	-	RO	Reserved.
10	0x0	RW	**RXFCE Receive Flow Control Enable** When this bit is set and the KSZ8841M is in full-duplex mode, flow control is enabled, and the KSZ8841M will acknowledge a PAUSE frame from the receive interface; i.e., the outgoing packets are pending in the transmit buffer until the PAUSE frame control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, flow control is not enabled.
9	0x0	RW	**RXEFE Receive Error Frame Enable** When this bit is set, CRC error frames are allowed to be received into the RX queue. When this bit is cleared, all CRC error frames are discarded.
8	-	RO	Reserved.
7	0x0	RW	**RXBE Receive Broadcast Enable** When this bit is set, the RX module receives all the broadcast frames.
6	0x0	RW	**RXME Receive Multicast Enable** When this bit is set, the RX module receives all the multicast frames (including broadcast frames).
5	0x0	RW	**RXUE Receive Unicast** When this bit is set, the RX module receives unicast frames that match the 48-bit Station MAC address of the module.
4	0x0	RW	**RXRA Receive All** When this bit is set, the KSZ8841M receives all incoming frames, regardless of the frame's destination address.
3	0x0	RW	**RXSCE Receive Strip CRC** When this bit is set, the KSZ8841M strips the CRC on the received frames. Once cleared, the CRC is stored in memory following the packet.
2	0x0	RW	**QMU Receive Multicast Hash-Table Enable** When this bit is set, this bit enables the RX function to receive multicast frames that pass the CRC Hash filtering mechanism.
1	-	RO	Reserved.
0	0x0	RW	**RXE Receive Enable** When this bit is set, the RX block is enabled and placed in a running state. When this bit is cleared, the receive process is placed in the stopped state upon completing reception of the current frame.

Bank 16 TXQ Memory Information Register (0x08): TXMIR

This register indicates the amount of free memory available in the TXQ of the QMU module.

Bit	Default Value	R/W	Description
15-13	-	RO	Reserved.
12-0	-	RO	**TXMA Transmit Memory Available** The amount of memory available is represented in units of byte. The TXQ memory is used for both frame payload, control word. Note: Software must be written to ensure that there is enough memory for the next transmit frame including control information before transmit data is written to the TXQ.

Bank 16 RXQ Memory Information Register (0x0A): RXMIR

This register indicates the amount of receive data available in the RXQ of the QMU module.

Bit	Default Value	R/W	Description
15-13	-	RO	Reserved.
12-0	-	RO	**RXMA Receive Packet Data Available** The amount of Receive packet data available is represented in units of byte. The RXQ memory is used for both frame payload, status word. There is total 4096 bytes in RXQ. This counter will update after a complete packet is received and also issues an interrupt when receive interrupt enable IER[13] in Bank 18 is set. Note: Software must be written to empty the RXQ memory to allow for the new RX frame. If this is not done, the frame may be discarded as a result of insufficient RXQ memory.

Bank 17 TXQ Command Register (0x00): TXQCR

This register is programmed by the Host CPU to issue a transmit command to the TXQ. The present transmit frame in the TXQ memory is queued for transmit.

Bit	Default Value	R/W	Description
15-1	-	RO	Reserved
0	0x0	RW	**TXETF Enqueue TX Frame** When this bit is written as 1, the current TX frame prepared in the TX buffer is queued for transmit. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting up another new TX frame.

Bank 17 RXQ Command Register (0x02): RXQCR

This register is programmed by the Host CPU to issue release command to the RXQ. The current frame in the RXQ frame buffer is read only by the host and the memory space is released.

Bit	Default Value	R/W	Description
15-1	-	RO	Reserved.
0	0x0	RW	**RXRRF Release RX Frame** When this bit is written as 1, the current RX frame buffer is released. Note: This bit is self-clearing after the frame memory is released. The software should wait for the bit to be cleared before processing new RX frame.

Bank 17 TX Frame Data Pointer Register (0x04): TXFDPR

The value of this register determines the address to be accessed within the TXQ frame buffer. When the AUTO increment is set, It will automatically increment the pointer value on Write accesses to the data register.

The counter is incremented by one for every byte access, by two for every word access, and by four for every double word access.

Bit	Default Value	R/W	Description
15	-	RO	Reserved.
14	0x0	RW	**TXFPAI TX Frame Data Pointer Auto Increment** When this bit is set, the TX Frame data pointer register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every doubleword access. When this bit is reset, the TX frame data pointer is manually controlled by user to access the TX frame location.
13-11	-	RO	Reserved.
10-0	0x000	RW	**TXFP TX Frame Pointer** TX Frame Pointer index to the Frame Data register for access. This field reset to next available TX frame location when the TX Frame Data has been enqueued through the TXQ command register.

Bank 17 RX Frame Data Pointer Register (0x06): RXFDPR

The value of this register determines the address to be accessed within the RXQ frame buffer. When the Auto Increment is set, it will automatically increment the RXQ Pointer on read accesses to the data register.

The counter is incremented is by one for every byte access, by two for every word access, and by four for every double word access.

Bit	Default Value	R/W	Description
15	-	RO	Reserved.
14	0x0	RW	**RXFPAI RX Frame Pointer Auto Increment** When this bit is set, the RXQ Address register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every double word access. When this bit is reset, the RX frame data pointer is manually controlled by user to access the RX frame location.
13-11	-	RO	Reserved.
10-0	0x000	RW	**RXFP RX Frame Pointer** RX Frame data pointer index to the Data register for access. This field reset to next available RX frame location when RX Frame release command is issued (through the RXQ command register).

Bank 17 QMU Data Register Low (0x08): QDRL

This register QDRL(0x08-0x09) contains the Low data word presently addressed by the pointer register. Reading maps from the RXQ, and writing maps to the TXQ.

Bit	Default Value	R/W	Description
15-0	-	RW	**QDRL Queue Data Register Low** This register is mapped into two uni-directional buffers for 16-bit buses, and one uni-directional buffer for 32-bit buses, (TXQ when Write, RXQ when Read) that allow moving words to and from the KSZ8841M regardless of whether the pointer is even, odd, or Dword aligned. Byte, word, and Dword access can be mixed on the fly in any order. This register along with DQRH is mapped into two consecutive word locations for 16-bit buses, or one word location for 32-bit buses, to facilitate Dword move operations.

Bank 17 QMU Data Register High (0x0A): QDRH

This register QDRH(0x0A-0x0B) contains the High data word presently addressed by the pointer register. Reading maps from the RXQ, and writing maps to the TXQ.

Bit	Default Value	R/W	Description
15-0	-	RW	**QDRL Queue Data Register High** This register is mapped into two uni-directional buffers for 16-bit buses, and one uni-directional buffer for 32-bit buses, (TXQ when Write, RXQ when Read) that allow moving words to and from the KSZ8841M regardless of whether the pointer is even, odd, or dword aligned. Byte, word, and Dword access can be mixed on the fly in any order. This register along with DQRL is mapped into two consecutive word locations for 16-bit buses, or one word location for 32-bit buses, to facilitate Dword move operations.

Bank 18 Interrupt Enable Register (0x00): IER

This register enables the interrupts from the QMU and other sources.

Bit	Default Value	R/W	Description
15	0x0	RW	**LCIE Link Change Interrupt Enable** When this bit is set, the link change interrupt is enabled. When this bit is reset, the link change interrupt is disabled.
14	0x0	RW	**TXIE Transmit Interrupt Enable** When this bit is set, the transmit interrupt is enabled. When this bit is reset, the transmit interrupt is disabled.
13	0x0	RW	**RXIE Receive Interrupt Enable** When this bit is set, the receive interrupt is enabled. When this bit is reset, the receive interrupt is disabled.
12	0x0	RW	**TXUIE Transmit Underrun Interrupt Enable** When this bit is set, the transmit underrun interrupt is enabled. When this bit is reset, the transmit underrun interrupt is disabled.
11	0x0	RW	**RXOIE Receive Overrun Interrupt Enable** When this bit is set, the Receive Overrun interrupt is enabled. When this bit is reset, the Receive Overrun interrupt is disabled.
10	0x0	RW	**RXEIE Receive Early Receive Interrupt Enable** When this bit is set, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.
9	0x0	RW	**TXPSIE Transmit Process Stopped Interrupt Enable** When this bit is set, the Transmit Process Stopped interrupt is enabled. When this bit is reset, the Transmit Process Stopped interrupt is disabled.
8	0x0	RW	**RXPSIE Receive Process Stopped Interrupt Enable** When this bit is set, the Receive Process Stopped interrupt is enabled. When this bit is reset, the Receive Process Stopped interrupt is disabled.
7	0x0	RW	**RXEFIE Receive Error Frame Interrupt Enable** When this bit is set, the Receive error frame interrupt is enabled. When this bit is reset, the Receive error frame interrupt is disabled.
6-0	-	RO	Reserved.

Bank 18 Interrupt Status Register (0x02): ISR

This register contains the status bits for all QMU and other interrupt sources.

When the corresponding enable bit is set, it causes the interrupt pin to be asserted.

This register is usually read by the host CPU and device drivers during interrupt service routine or polling. The register bits are not cleared when read. The user has to write “1” to clear

Bit	Default Value	R/W	Description
15	0x0	RO (W1C)	**LCIS Link Change Interrupt Status** When this bit is set, it indicates that the link status has changed from link up to link down, or link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
14	0x0	RO (W1C)	**TXIS Transmit Status** When this bit is set, it indicates that the TXQ MAC has transmitted at least a frame on the MAC interface and the QMU TXQ is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
13	0x0	RO (W1C)	**RXIS Receive Interrupt Status** When this bit is set, it indicates that the QMU RXQ has received a frame from the MAC interface and the frame is ready for the host CPU to process. This edge-triggered interrupt status is cleared by writing 1 to this bit.
12	0x0	RO (W1C)	**TXUIS Transmit Underrun Interrupt Status** When this bit is set, it indicates that the transmit underrun condition has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
11	0x0	RO (W1C)	**RXOIS Receive Overrun Interrupt Status** When this bit is set, it indicates that the Receive Overrun status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
10	0x0	RO (W1C)	**RXEIS Receive Early Receive Interrupt Status** When this bit is set, it indicates that the Early Receive status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
9	0x1	RO (W1C)	**TXPSIE Transmit Process Stopped Status** When this bit is set, it indicates that the Transmit Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
8	0x1	RO (W1C)	**RXPSIE Receive Process Stopped Status** When this bit is set, it indicates that the Receive Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
7	0x0	RO (W1C)	**RXEFIE Receive Error Frame Interrupt Status** When this bit is set, it indicates that the Receive error frame status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
6-0	-	RO	Reserved.

Bank 18 Receive Status Register (0x04): RXSR

This register indicates the status of the current received frame and mirrors the Receive Status word of the Receive Frame in the RXQ.

Bit	Default Value	R/W	Description
15	-	RO	**RXFV Receive Frame Valid** When set, it indicates that the present frame in the receive packet memory is valid. The status information currently in this location is also valid. When clear, it indicates that there is either no pending receive frame or that the current frame is still in the process of receiving.
14-8	-	RO	Reserved.
7	-	RO	**RXBF Receive Broadcast Frame** When set, it indicates that this frame has a broadcast address.
6	-	RO	**RXMF Receive Multicast Frame** When set, it indicates that this frame has a multicast address (including the broadcast address).
5	-	RO	**RXUF Receive Unicast Frame** When set, it indicates that this frame has a unicast address.
4	-	RO	**RXMR Receive MII Error** When set, it indicates that there is an MII symbol error on the received frame.
3	-	RO	**RXFT Receive Frame Type** When set, it indicates that the frame is an Ethernet-type frame (frame length is greater than 1500 bytes). When clear, it indicate that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames.
2	-	RO	**RXTL Receive Frame Too Long** When set, it indicates that the frame length exceeds the maximum size of 1916 bytes. Frames that are too long are passed to the host only if the pass bad frame bit is set (bit 9 in RXCR register). Note: Frame too long is only a frame length indication and does not cause any frame truncation.
1	-	RO	**RXRF Receive Runt Frame** When set, it indicates that a frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed to the host only if the pass bad frame bit is set (bit 9 in RXCR register).
0	-	RO	**RXCE Receive CRC Error** When set, it indicates that a CRC error has occurred on the current received frame. A CRC error frame is passed to the host only if the pass bad frame bit is set (bit 9 in RXCR register)

Bank 18 Receive Byte Count Register (0x06): RXBC

This register indicates the status of the current received frame and mirrors the Receive Byte Count word of the Receive Frame in the RXQ.

Bit	Default Value	R/W	Description
15-11	-	RO	Reserved.
10-0	-	RO	**RXBX Receive Byte Count** Receive byte count.

Bank 18 Early Transmit Register (0x08): ETXR

This register specifies the threshold for the early transmit.

Bit	Default Value	R/W	Description
15-8	-	RO	Reserved.
7	0x0	RW	**TXEE Early Transmit Enable** When this bit is set, the Early Transmit function is enabled. When this bit is cleared, normal operation is assumed.
6-5	-	RO	Reserved.
4-0	0x00	RW	**ETXTH Early Transmit Threshold** The threshold for Early Transmit. Specified in unit of 64-byte. Whenever the number of bytes written in memory for the presently transmitting packet exceeds the threshold, Early Transmit will be started on the network interface. When early transmit is enabled, setting this field to 0 is invalid, and the hardware behavior is unknown.

Bank 18 Early Receive Register (0x0A): ERXR

This register specify the threshold for early receive and interrupt condition.

Bit	Default Value	R/W	Description
15-8	-	RO	Reserved.
7	0x0	RW	**RXEE Early Receive Enable** When this bit is set, the Early Receive function is enabled. When this bit is cleared, normal operation is assumed.
6-5	-	RO	Reserved.
4-0	0x1F	RW	**ERXTH Early Receive Threshold** The threshold for Early Receive and Interrupt. Specified in unit of 64-byte. Whenever the number of bytes written in memory for the presently received packet exceeds the threshold, early receive status will be set, and Early Receive interrupt will be asserted if its interrupt is enabled. When early receive is enabled, setting this field to 0 is invalid, and the hardware behavior is unknown.

Bank 19 Multicast Table Register 0 (0x00): MTR0

The 64-bit multicast table is used for group address filtering. This value is defined as the six most significant bits from CRC circuit calculation result that is based on 48-bit of DA input. The two most significant bits select one of the four registers to be used, while the others determine which bit within the register.

Multicast table register 0.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**MTR0 Multicast Table 0** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Multicast Table Register 1 (0x02): MTR1

Multicast table register 1.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**MTR0 Multicast Table 1** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Multicast Table Register 2 (0x04): MTR2

Multicast table register 2.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**MTR0 Multicast Table 2** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Multicast Table Register 3 (0x06): MTR3

Multicast table register 3.

Bit	Default Value	R/W	Description
15-0	0x0	RW	**MTR0 Multicast Table 3** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR, all multicast addresses are received regardless of the multicast table value.

Bank 19 Power Management Control and Status Register (0x08): PMCS

The following control and status register provides information on the KSZ8841M power management capabilities. The following table shows the register bit fields.

Bit	Default Value	R/W	Description
15	0	RO (W1C)	**PME_Status** This bit indicates that the KSZ8841M has detected a power-management event. If bit PME_Enable is set, the KSZ8841M also asserts the PMEN pin. This bit is cleared on power-up reset or by write 1. It is not modified by either hardware or software reset. When this bit is cleared, the KSZ8841M deasserts the PMEN pin.
14-9	0x00	RO	Reserved.
8	0	RW	**PME_Enable** If this bit is set, the KSZ8841M can assert the PMEN pin. Otherwise, assertion of the PMEN pin is disabled. This bit is cleared on power-up reset and will be not modified by software reset.
7-4	0x0	RO	Reserved.

Bit	Default Value	R/W	Description
3	0	RO	**No Soft Reset** If this bit is set (“1”), the KSZ8841M does not perform an internal reset when transitioning from D3_hot to D0 because of PowerState commands. Configuration context is preserved. Upon transition from D3_hot to the D0 Initialized state, no additional operating system intervention is required to preserve configuration context beyond writing the PowerState bits. If this bit is cleared (“0”), the KSZ8841M does perform an internal reset when transitioning from D3_hot to D0 via software control of the PowerState bits. Configuration context is lost when performing the soft reset. Upon transition from D3_hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3_hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. The value of this bit is loaded from the NO_SRST bit in the serial EEPROM.
2	0	RO	Reserved.
1-0	0x0	RW	**Power State** This field is used to set the new power state of the KSZ8841M as well as to determine its current power state. The definitions of the field values are: 00: D0 -> System is on and running 01: D1 -> Low-power state 10: D2 -> Low-power state 11: D3 (hot) -> System is off and not running

Banks 20 – 31: Reserved

Except Bank Select Register (0xE).

Bank 32 Chip ID and Enable Register (0x00): CIDER

This register contains the chip ID and the chip enable bit.

Bit	Default	R/W	Description
15-8	0x88	RO	**Family ID** Chip family ID
7-4	0x1	RO	**Chip ID** 0x1 is assigned to KSZ8841M
3-1	0x1	RO	**Revision ID**
0	0	RO	Reserved.

Bank 32 Chip Global Control Register (0x0A): CGCR

This register contains the global control for the chip function.

<table>
<tr><th>Bit</th><th>Default</th><th>R/W</th><th>Description</th></tr>
<tr><td>15</td><td>0</td><td>RW</td><td>LEDSEL1
See description for bit 9.</td></tr>
<tr><td>14-12</td><td>0</td><td>RW</td><td>Reserved.</td></tr>
<tr><td>11-10</td><td>0x2</td><td>RW</td><td>Reserved.</td></tr>
<tr><td>9</td><td>0</td><td>RW</td><td>LEDSEL0
This register bit sets the LEDSEL0 selection only.
Port 1 LED indicators, defined as below:
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P1LED3</td><td>------</td><td>------</td></tr>
<tr><td>P1LED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr>
<tr><td>P1LED1</td><td>FULL_DPX/COL</td><td>10LINK/ACT</td></tr>
<tr><td>P1LED0</td><td>SPEED</td><td>FULL_DPX</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P1LED3</td><td>ACT</td><td>------</td></tr>
<tr><td>P1LED2</td><td>LINK</td><td>------</td></tr>
<tr><td>P1LED1</td><td>FULL_DPX/COL</td><td>------</td></tr>
<tr><td>P1LED0</td><td>SPEED</td><td>------</td></tr>
</table></td></tr>
<tr><td>8</td><td>0</td><td>R/W</td><td>Reserved.</td></tr>
<tr><td>7-0</td><td>0x35</td><td>RW</td><td>Reserved.</td></tr>
</table>

Banks 33 – 41: Reserved

Except Bank Select Register (0xE)

Bank 42 Indirect Access Control Register (0x00): IACR

This register contains the indirect control for the MIB counter (Write IACR triggers a command. Read or write access is determined by register bit 12).

Bit	Default	R/W	Description
15-13	0x0	RW	Reserved.
12	0	RW	**Read High. Write Low** 1 = read cycle. 0 = write cycle.
11-10	0x0	RW	**Table Select** 00 = reserved. 01 = reserved. 10 = reserved. 11 = MIB counter selected.
9-0	0x000	RW	**Indirect Address** Bit 9-0 of indirect address.

Bank 42 Indirect Access Data Register 1 (0x02): IADR1

This register contains the indirect data for the chip function.

Bit	Default	R/W	Description
15-0	0x0000	RO	Reserved.

Bank 42 Indirect Access Data Register 2 (0x04): IADR2

This register contains the indirect data for the chip function.

Bit	Default	R/W	Description
15-0	0x0000	RO	Reserved.

Bank 42 Indirect Access Data Register 3 (0x06): IADR3

This register contains the indirect data for the chip function.

Bit	Default	R/W	Description
15-0	0x0000	RO	Reserved.

Bank 42 Indirect Access Data Register 4 (0x08): IADR4

This register contains the indirect data for the chip function.

Bit	Default	R/W	Description
15-0	0x0000	RW	**Indirect Data** Bit 15-0 of indirect data.

Bank 42 Indirect Access Data Register 5 (0x0A): IADR5

This register contains the indirect data for the chip function.

Bit	Default	R/W	Description
15-0	0x0000	RW	**Indirect Data** Bit 31-16 of indirect data.

Bank 43– 44: Reserved

Except Bank Select Register (0xE)

Bank 45 PHY 1 MII-Register Basic Control Register (0x00): P1MBCR

This register contains Media Independent Interface (MII) register for port 1 as defined in the IEEE 802.3 specification.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Soft reset** Not supported.	
14	0	RW	Reserved.	
13	0	RW	**Force 100** 1 = force 100Mbps if AN is disabled (bit 12) 0 = force 10Mbps if AN is disabled (bit 12)	Bank49 0x2 bit6
12	1	RW	**AN Enable** 1 = auto-negotiation enabled. 0 = auto-negotiation disabled.	Bank49 0x2 bit7
11	0	RW	**Power-Down** 1 = power-down. 0 = normal operation.	Bank49 0x2 bit11
10	0	RO	**Isolate** Not supported.	
9	0	RW	**Restart AN** 1 = restart auto-negotiation. 0 = normal operation.	Bank49 0x2 bit13
8	0	RW	**Force Full Duplex** 1 = force full duplex 0 = force half duplex. if AN is disabled (bit 12) or AN is enabled but failed.	Bank49 0x2 bit5
7	0	RO	**Collision test** Not supported.	
6	0	RO	Reserved.	
5	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Micrel Auto MDI-X mode.	Bank49 0x4 bit15
4	0	RW	**Force MDI-X** 1 = force MDI-X. 0 = normal operation.	Bank49 0x2 bit9
3	0	RW	**Disable MDI-X** 1 = disable auto MDI-X. 0 = normal operation.	Bank49 0x2 bit10
2	0	RW	Reserved.	Bank49 0x2 bit12
1	0	RW	**Disable Transmit** 1 = disable transmit. 0 = normal operation.	Bank49 0x2 bit14
0	0	RW	**Disable LED** 1 = disable LED. 0 = normal operation.	Bank49 0x2 bit15

Bank 45 PHY 1 MII-Register Basic Status Register (0x02): P1MBSR

This register contains the MII register status for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**T4 Capable** 1 = 100 BASE-T4 capable. 0 = not 100 BASE-T4 capable.	
14	1	RO	**100 Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = not 100BASE-TX full duplex.capable.	
13	1	RO	**100 Half Capable** 1= 100BASE-TX half-duplex capable. 0= not 100BASE-TX half-duplex capable.	
12	1	RO	**10 Full Capable** 1 = 10BASE-T full-duplex capable. 0 = not 10BASE-T full-duplex capable.	
11	1	RO	**10 Half Capable** 1 = 10BASE-T half-duplex capable. 0 = not 10BASE-T half-duplex capable.	
10-7	0	RO	Reserved**.**	
6	0	RO	**Preamble suppressed** Not supported.	
5	0	RO	**AN Complete** 1 = auto-negotiation complete. 0 = auto-negotiation not completed.	Bank49 0x4 bit6
4	0	RO	Reserved	Bank49 0x4 bit8
3	1	RO	**AN Capable** 1 = auto-negotiation capable. 0 = not auto-negotiation capable.	
2	0	RO	**Link Status** 1 = link is up. 0 = link is down.	Bank49 0x4 bit5
1	0	RO	**Jabber test** Not supported.	
0	0	RO	**Extended Capable** 1 = extended register capable. 0 = not extended register capable.	

Bank 45 PHY 1 PHYID Low Register (0x04): PHY1ILR

This register contains the PHY ID (low) for the chip.

Bit	Default	R/W	Description
15-0	0x1430	RO	**PHYID Low** Low order PHYID bits.

Bank 45 PHY 1 PHYID High Register (0x06): PHY1IHR

This register contains the PHY ID (high) for the chip.

Bit	Default	R/W	Description
15-0	0x0022	RO	**PHYID High** High order PHYID bits.

Bank 45 PHY 1 Auto-Negotiation Advertisement Register (0x08): P1ANAR

This register contains the auto-negotiation advertisement for the PHY function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Next page** Not supported.	
14	0	RO	Reserved	
13	0	RO	**Remote fault** Not supported.	
12-11	0	RO	Reserved	
10	1	RW	**Pause (flow control capability)** 1 = advertise pause capability. 0 = do not advertise pause capability.	Bank49 0x2 bit4
9	0	RW	Reserved.	
8	1	RW	**Adv 100 Full** 1 = advertise 100 full-duplex capability. 0 = do not advertise 100 full-duplex capability	Bank49 0x2 bit3
7	1	RW	**Adv 100 Half** 1= advertise 100 half-duplex capability. 0 = do not advertise 100 half-duplex capability.	Bank49 0x2 bit2
6	1	RW	**Adv 10 Full** 1 = advertise 10 full-duplex capability. 0 = do not advertise 10 full-duplex capability.	Bank49 0x2 bit1
5	1	RW	**Adv 10 Half** 1 = advertise 10 half-duplex capability. 0 = do not advertise 10 half-duplex capability.	Bank49 0x2 bit0
4-0	0x01	RO	**Selector Field** 802.3	

Bank 45 PHY 1 Auto-Negotiation Link Partner Ability Register (0x0A): P1ANLPR

This register contains the auto-negotiation link partner ability for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RO	**Next page** Not supported.	
14	0	RO	**LP ACK** Not supported.	
13	0	RO	**Remote fault** Not supported.	
12-11	0	RO	Reserved	

Bit	Default	R/W	Description	Bit is same as:
10	0	RO	**Pause** Link partner pause capability.	Bank49 0x4 bit4
9	0	RO	Reserved.	
8	0	RO	**Adv 100 Full** Link partner 100 full capability.	Bank49 0x4 bit3
7	0	RO	**Adv 100 Half** Link partner 100 half capability.	Bank49 0x4 bit2
6	0	RO	**Adv 10 Full** Link partner 10 full capability.	Bank49 0x4 bit1
5	0	RO	**Adv 10 Half** Link partner 10 half capability.	Bank49 0x4 bit0
4-0	0x01	RO	Reserved.	

Bank 46: Reserved

Except Bank Select Register (0xE)

Bank 47 PHY1 LinkMD Control/Status (0x00): P1VCT

This register contains the LinkMD control and status information of PHY 1.

Bit	Default	R/W	Description	Bit is same as:
15	0	RW (Self-Clear)	**Vct_enable** 1 = cable diagnostic test is enabled. It is self-cleared after the VCT test is done. 0 = indicates that the cable diagnostic test is completed and the status information is valid for read.	Bank49 0x0 bit 12
14-13	0	RO	**Vct_result** [00] = normal condition. [01] = open condition detected in the cable. [10] = short condition detected in the cable. [11] = cable diagnostic test failed.	Bank49 0x0 bit 14-13
12	-	RO	**Vct 10M Short** 1 = Less than 10m short.	Bank49 0x0 bit 15
11-9	0x0	RO	Reserved.	
8-0	0x000	RO	**Vct_fault_count** Distance to the fault. The distance is approximately 0.4m*vct_fault_count.	Bank49 0x0 bit 8-0

Bank 47 PHY1 Special Control/Status Register (0x02): P1PHYCTRL

This register contains the control and status information of PHY1.

Bit	Default	R/W	Description	Bit is same as:
15-6	0x000	RO	Reserved.	
5	0	RO	**Polarity Reverse (polrvs)** 1 = polarity is reversed. 0 = polarity is not reversed.	Bank49 0x04 bit13
4	0	RO	**MDIX Status (mdix_st)** 1 = MDI 0 = MDIX	Bank49 0x04 bit7
3	0	RW	**Force Link (force_lnk)** 1 = force link pass. 0 = normal operation.	Bank49 0x00 bit11
2	1	RW	**Power Saving (pwrsave)** 1 = disable power saving. 0 = enable power saving.	Bank49 0x00 bit10
1	0	RW	**Remote (Near-end) Loopback (rlb)** 1 = perform remote loopback at PHY (RXP1/RXM1 -> TXP1/TXM1, see Figure 12) 0 = normal operation	Bank49 0x00 bit9
0	0	RW	Reserved.	

Bank 48: Reserved

Except Bank Select Register (0xE)

Bank 49 Port 1 PHY Special Control/Status, LinkMD (0x00): P1SCSLMD

Bit	Default	R/W	Description	Is same as:
15	0	RO	**Vct_10m_short** 1 = Less than 10 meter short.	Bank 47 0x00 bit 12
14-13	0	RO	**Vct_result** VCT result. [00] = normal condition. [01] = open condition has been detected in cable. [10] = short condition has been detected in cable. [11] = cable diagnostic test is failed.	Bank 47 0x00 bit 14-13
12	0	RW (Self-Clear)	**Vct_en** Vct enable. 1 = the cable diagnostic test is enabled. It is self-cleared after the VCT test is done. 0 = it indicates the cable diagnostic test is completed and the status information is valid for read.	Bank 47 0x00 bit 15
11	0	RW	**Force_lnk** Force link. 1 = force link pass. 0 = normal operation.	Bank 47 0x02 bit 3
10	1	RW	**pwrsave** Power-saving. 1 = disable power saving. 0 = enable power saving.	Bank 47 0x02 bit 2
9	0	RW	**Remote (Near-end) loopback** (rlb) 1 = perform remote loopback at PHY (RXP1/RXM1 -> TXP1/TXM1, see Figure 12) 0 = normal operation	Bank 47 0x02 bit 1
8-0	0x000	RO	**Vct_fault_count** VCT fault count. Distance to the fault. It's approximately 0.4m*vct_fault_count.	Bank 47 0x00 bit 8-0

Bank 49 Port 1 Control Register 4 (0x02): P1CR4

This register contains the global per port control for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	0	RW	**LED Off** 1 = Turn off all of the port 1 LEDs (P1LED3, P1LED2, P1LED1, P1LED0). These pins are driven high if this bit is set to one. 0 = normal operation.	Bank 45 0x00 bit 0
14	0	RW	**Txids** 1 = disable the port's transmitter. 0 = normal operation.	Bank45 0x00 bit 1
13	0	RW	**Restart AN** 1 = restart auto-negotiation. 0 = normal operation.	Bank 45 0x00 bit 9
12	0	RW	Reserved	Bank 45 0x00 bit 2
11	0	RW	**Power Down** 1 = power down. 0 = normal operation.	Bank 45 0x00 bit 11
10	0	RW	**Disable auto MDI/MDI-X** 1 = disable auto MDI/MDI-X function. 0 = enable auto MDI/MDI-X function.	Bank 45 0x00 bit 3
9	0	RW	**Force MDI-X** 1= if auto MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = do not force PHY into MDI-X mode.	Bank 45 0x00 bit 4
8	0	RW	Reserved	
7	1	RW	**Auto Negotiation Enable** 1 = auto negotiation is enabled. 0 = disable auto negotiation, speed, and duplex are decided by bits 6 and 5 of the same register.	Bank 45 0x00 bit 12
6	0	RW	**Force Speed** 1 = force 100BT if AN is disabled (bit 7). 0 = force 10BT if AN is disabled (bit 7).	Bank 45 0x00 bit 13
5	0	RW	**Force Duplex** 1 = force full duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = force half duplex if (1) AN is disabled or (2) AN is enabled but failed.	Bank 45 0x00 bit 8
4	1	RW	**Advertised flow control capability.** 1 = advertise flow control (pause) capability. 0 = suppress flow control (pause) capability from transmission to link partner.	Bank 45 0x08 bit 10
3	1	RW	**Advertised 100BT full-duplex capability.** 1 = advertise 100BT full-duplex capability. 0 = suppress 100BT full-duplex capability from transmission to link partner.	Bank 45 0x08 bit 8

Bit	Default	R/W	Description	Bit is same as:
2	1	RW	**Advertised 100BT half-duplex capability.** 1 = advertise 100BT half-duplex capability. 0 = suppress 100BT half-duplex capability from transmission to link partner.	Bank 45 0x08 bit 7
1	1	RW	**Advertised 10BT full-duplex capability.** 1 = advertise 10BT full-duplex capability. 0 = suppress 10BT full-duplex capability from transmission to link partner.	Bank 45 0x08 bit 6
0	1	RW	**Advertised 10BT half-duplex capability.** 1 = advertise 10BT half-duplex capability. 0 = suppress 10BT half-duplex capability from transmission to link partner.	Bank 45 0x08 bit 5

Bank 49 Port 1 Status Register (0x04): P1SR

This register contains the global per port status for the chip function.

Bit	Default	R/W	Description	Bit is same as:
15	1	RW	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Micrel Auto MDI-X mode.	Bank 45 0x00 bit 5
14	0	RO	Reserved	
13	0	RO	**Polarity Reverse** 1 = polarity is reversed. 0 = polarity is not reversed.	Bank 47 0x02 bit 5
12	0	RO	**Receive Flow Control Enable** 1 = receive flow control feature is active. 0 = receive flow control feature is inactive.	
11	0	RO	**Transmit Flow Control Enable** 1 = transmit flow control feature is active. 0 = transmit flow control feature is inactive.	
10	0	RO	**Operation Speed** 1 = link speed is 100Mbps. 0 = link speed is 10Mbps.	
9	0	RO	**Operation Duplex** 1 = link duplex is full. 0 = link duplex is half.	
8	0	RO	Reserved	Bank 45 0x02 bit 4
7	0	RO	**MDI-X status** 1 = MDI. 0 = MDI-X.	Bank 47 0x02 bit 4
6	0	RO	**AN Done** 1 = AN done. 0 = AN not done.	Bank 45 0x02 bit 5
5	0	RO	**Link Good** 1= link good.	Bank 45 0x02 bit 2

Bit	Default	R/W	Description	Bit is same as:
			0 = link not good.	
4	0	RO	**Partner flow control capability.** 1 = link partner flow control (pause) capable. 0 = link partner not flow control (pause) capable.	Bank 45 0x0A bit 10
3	0	RO	**Partner 100BT full-duplex capability.** 1 = link partner 100BT full-duplex capable. 0 = link partner not 100BT full-duplex capable.	Bank 45 0x0A bit 8
2	0	RO	**Partner 100BT half-duplex capability.** 1 = link partner 100BT half-duplex capable. 0= link partner not 100BT half-duplex capable.	Bank 45 0x0A bit 7
1	0	RO	**Partner 10BT full-duplex capability.** 1= link partner 10BT full-duplex capable. 0 = link partner not 10BT full-duplex capable.	Bank 45 0x0A bit 6
0	0	RO	**Partner 10BT half-duplex capability.** 1 = link partner 10BT half-duplex capable. 0 = link partner not 10BT half-duplex capable.	Bank 45 0x0A bit 5

Banks 50 – 63: Reserved

Except Bank Select Register (0xE)

MIB (Management Information Base) Counters

The KSZ8841M provides 32 MIB counters to monitor the port activity for network management. The MIB counters are formatted as shown below.

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = counter overflow. 0 = no counter overflow.	0
30	Count valid	RO	1 = counter value is valid. 0 = 0 counter value is not valid.	0
29-0	Counter values	RO	Counter value (read clear)	0x00000000

Table 11. Format of MIB Counters

Ethernet port MIB counters are read using indirect memory access. The address offset range is 0x00 to 0x1F.

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	Reserved	Reserved.
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 bytes)
0x5	RxJabbers	Rx packets longer than 1536 bytes w/ either CRC errors, alignment errors, or symbol errors
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1916) bytes w/ an integral number of bytes and a bad CRC
0x8	RxAlignmentError	Rx packets within (64,1916) bytes w/ a non-integral number of bytes and a bad CRC
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1916 octets in length
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	Reserved	Reserved.
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets)

Offset	Counter Name	Description
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

Table 12. Port 1 MIB Counters Indirect Memory Offsets

Example:

1. MIB Counter Read (read port 1 “Rx64Octets” counter at indirect address offset 0x0E)

Write to reg. IACR with 0x1C0E (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR5 (MIB counter value 31-16) // If bit 31 = 1, there was a counter overflow
// If bit 30 = 0, restart (re-read) from this register

Read reg. IADR4 (MIB counter value 15-0)

Additional MIB Information

In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.

Absolute Maximum Ratings(1)

Description	Pins	Value
Supply Voltage	VDDATX, VDDARX, VDDIO	–0.5V to +4.0V
Input Voltage	All Inputs	–0.5V to +5V
Output Voltage	All Outputs	–0.5V to +4.0V
Lead Temperature (soldering, 10 sec)	N/A	270°C
Storage Temperature (TS)	N/A	–55°C to +150°C

Table 13. Maximum Ratings

Note:
Exceeding the absolute maximum rating may damage the device. Stresses greater than those listed in the table above may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

Operating Ratings(1)

Parameter	Symbol	Min	Typ	Max
Supply Voltages	VDDATX,VDDARX	3.1V	3.3V	3.5V
	VDDIO	3.1V	3.3V	3.5V
Ambient Temperature for Commercial	T_A	0°C		+70°C
Ambient Temperature for Industrial	T_A	-40°C		+85°C
Maximum Junction Temperature	T_J			+125°C
Thermal Resistance Junction-to-Ambient(2)	θ_{JA}		42.91 °C/W	
Thermal Resistance Junction-to-Case(2)	θ_{JC}		19.6 °C/W	

Table 14. Operating Ratings

Notes:
1. **The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to VDD).**
2. **No (HS) heat spreader in this package. The θ_{JC}/θ_{JA} is under air velocity 0 m/s.**

Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Typ	Max
Supply Current for 100BASE-TX Operation (Single Port@100% Utilization)					
100BASE-TX (analog core + PLL + digital core + transceiver + digital I/O)	I_{ddxio}	VDDATX, VDDARX, VDDIO = 3.3V; Chip only (no transformer)		100 mA	
Supply Current for 10BASE-T Operation (Single Port@100% Utilization)					
10BASE-T (analog core + PLL + digital core + transceiver + digital I/O)	I_{ddxio}	VDDATX, VDDARX, VDDIO = 3.3V; Chip only (no transformer)		85 mA	
TTL Inputs					
Input High Voltage	V_{ih}		2.0V		
Input Low Voltage	V_{il}				0.8V
Input Current	I_{in}	Vin = GND ~ VDDIO	-10µA		10µA
TTL Outputs					
Output High Voltage	V_{oh}	I_{oh} = -8 mA	2.4V		
Output Low Voltage	V_{ol}	I_{ol} = 8 mA			0.4V
Output Tri-state Leakage	$\|I_{oz}\|$				10µA
100BaseTX Transmit (measured differentially after 1:1 transformer)					
Peak Differential Output Voltage	V_o	100Ω termination on the differential output.	±0.95V		±1.05V
Output Voltage Imbalance	V_{imb}	100Ω termination on the differential output			2%
Rise/Fall Time	T_r/T_f		3ns		5ns
Rise/Fall Time Imbalance			0ns		0.5ns
Duty Cycle Distortion					± 0.25ns
Overshoot					5%
Reference Voltage of ISET	V_{set}			0.5V	
Output Jitter		Peak-to-peak		0.7ns	1.4ns
10BaseT Receive					
Squelch Threshold	V_{sq}	5MHz square wave.		400mV	
10BaseT Transmit (measured differentially after 1:1 transformer)					
Peak Differential Output Voltage	V_p	100Ω termination on the differential output.		2.4V	
Jitter Added		100Ω termination on the differential output.(Peak-to-peak)		1.8ns	3.5ns

Table 15. Electrical Characteristics

Notes:
1. **TA = 25°C. Specification for packaged product only.**
2. **Single Port's transformer consumes an additional 45mA @3.3V for 100BASE-TX and 70mA @3.3V for 10BASE-T.**

Timing Specifications

Asynchronous Timing without using Address Strobe (ADSN = 0)

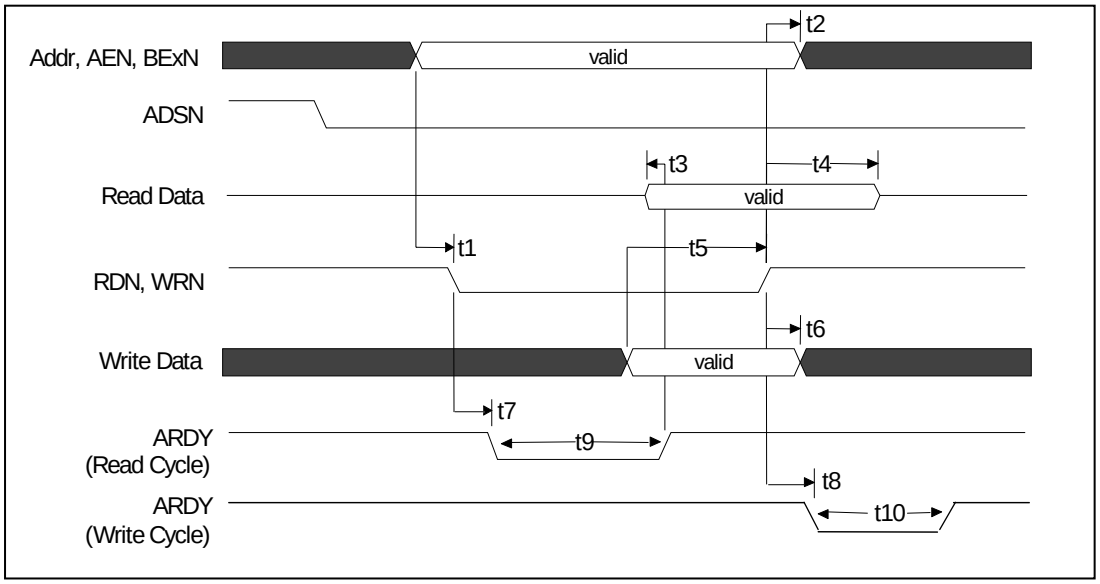


Figure 13. Asynchronous Cycle – ADSN = 0

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] valid to RDN, WRN active	0			ns
t2	A1-A15, AEN, BExN[3:0] hold after RDN inactive (assume ADSN tied Low)	0			ns
	A1-A15, AEN, BExN[3:0] hold after WRN inactive (assume ADSN tied Low)	1			ns
t3	Read data valid to ARDY rising			0.8	ns
t4	Read data to hold RDN inactive	4			ns
t5	Write data setup to WRN inactive	4			ns
t6	Write data hold after WRN inactive	2			ns
t7	Read active to ARDY Low			8	ns
t8	Write inactive to ARDY Low			8	ns
t9	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register and 40ns to read QMU data register in turbo mode) (Note2)	0	40		ns
	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register and 80ns to read QMU data register in normal mode)	0	80		ns
t10	ARDY low (wait time) in write cycle (Note1) (It is 0ns to write bank select register) (It is 36ns to write QMU data register)	0	50		ns

Table 16. Asynchronous Cycle (ADSN = 0) Timing Parameters

Notes:

1. **When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.**
2. **In order to speed up the ARDY low time to 40 ns, user has to use the turbo software driver which is only supported in the A6 devi**ce. Please refer to the "KSZ88xx Programmer's Guide" for detail.

Asynchronous Timing using Address Strobe (ADSN)

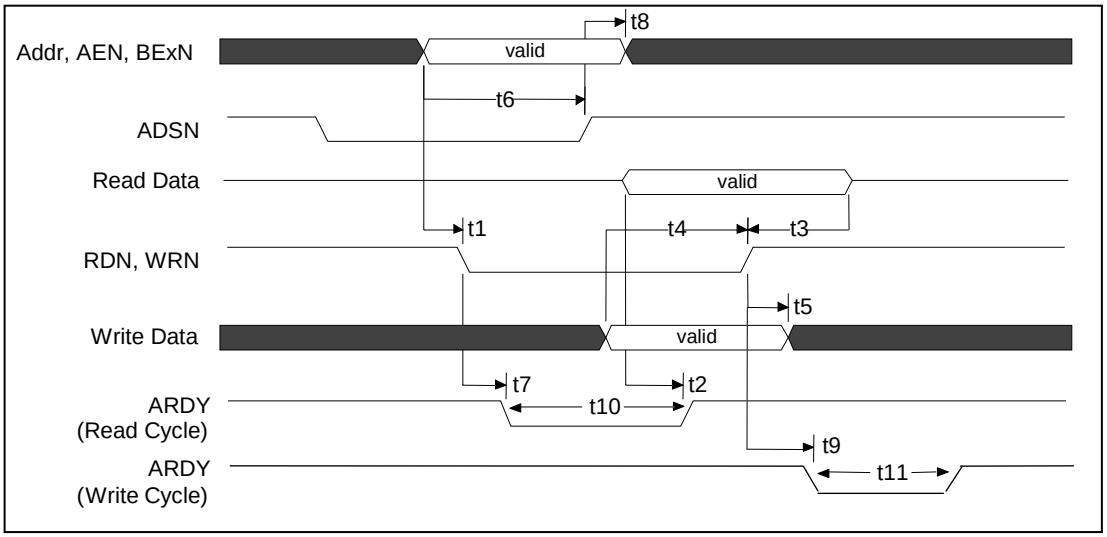


Figure 14. Asynchronous Cycle – Using ADSN

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] valid to RDN, WRN active	0			ns
t2	Read data valid to ARDY rising			0.8	ns
t3	Read data hold to RDN inactive	4			ns
t4	Write data setup to WRN inactive	4			ns
t5	Write data hold after WRN inactive	2			ns
t6	A1-A15, AEN, nBE[3:0] setup to ADSN rising	4			ns
t7	Read active to ARDY Low			8	ns
t8	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2			ns
t9	Write inactive to ARDY Low			8	ns
t10	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register and 40ns to read QMU data register in turbo mode) (Note2)	0	40		ns
	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register and 80ns to read QMU data register in normal mode)	0	80		ns
t11	ARDY low (wait time) in write cycle (Note1) (It is 0ns to write bank select register) (It is 36ns to write QMU data register)	0	50		ns

Table 17. Asynchronous Cycle using ADSN Timing Parameters

Notes:
1. When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.
2. In order to speed up the ARDY low time to 40ns, user has to use the turbo software driver which is only supported in the A6 device. Please refer to the “KSZ88xx Programmer's Guide” for detail.

Asynchronous Timing using DATACSN

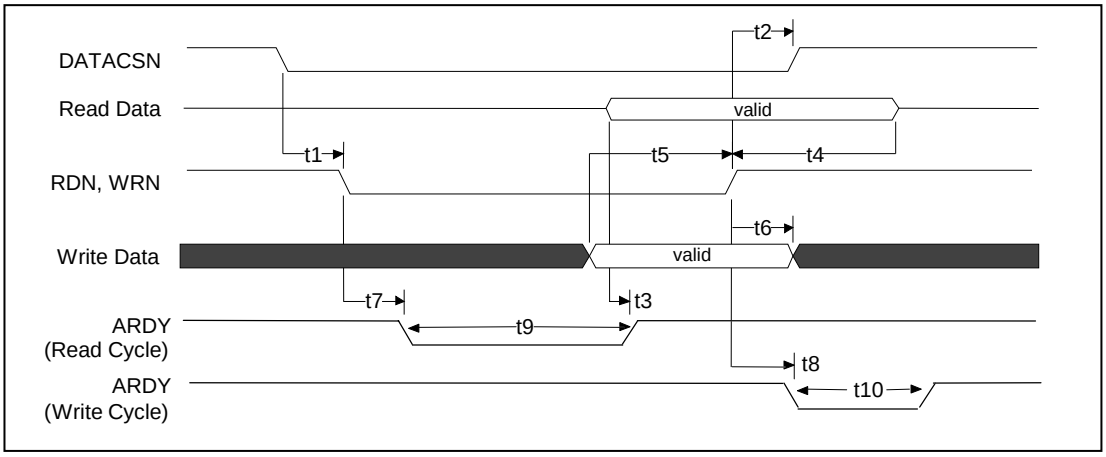


Figure 15. Asynchronous Cycle – Using DATACSN

Symbol	Parameter	Min	Typ	Max	Unit
t1	DATACSN setup to RDN, WRN active	2			ns
t2	DATACSN hold after RDN, WRN inactive (assume ADSN tied Low)	0			ns
t3	Read data hold to ARDY rising			0.8	ns
t4	Read data to RDN hold	4			ns
t5	Write data setup to WRN inactive	4			ns
t6	Write data hold after WRN inactive	2			ns
t7	Read active to ARDY Low			8	ns
t8	Write inactive to ARDY Low			8	ns
t9	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register and 40ns to read QMU data register in turbo mode) (Note2)	0	40		ns
	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register and 80ns to read QMU data register in normal mode)	0	80		ns
t10	ARDY low (wait time) in write cycle (Note1) (It is 0ns to write bank select register) (It is 36ns to write QMU data register)	0	50		ns

Table 18. Asynchronous Cycle using DATACSN Timing Parameters

Notes:
1. **When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.**
2. **In order to speed up the ARDY low time to 40 ns, user has to use the turbo software driver which is only supported in the A6 device. Please refer to the "KSZ88xx Programmer's Guide" for detail.**

Address Latching Timing for All Modes

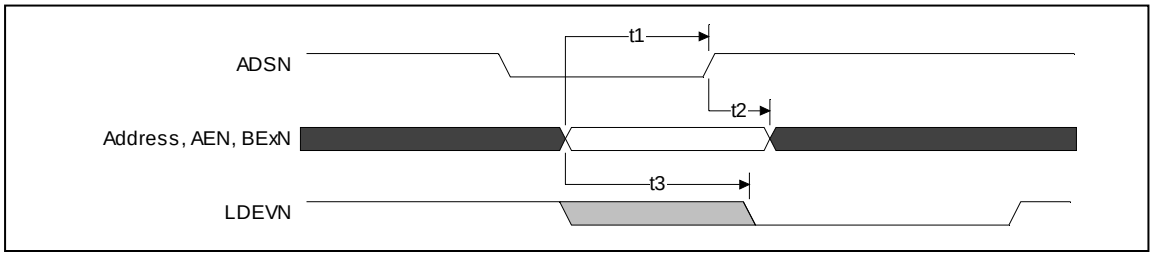


Figure 16. Address Latching Cycle for All Modes

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] setup to ADSN	4			ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2			ns
t3	A4-A15, AEN to LDEVN delay			5	ns

Table 19. Address Latching Timing Parameters

Synchronous Timing in Burst Write (VLBUSN = 1)

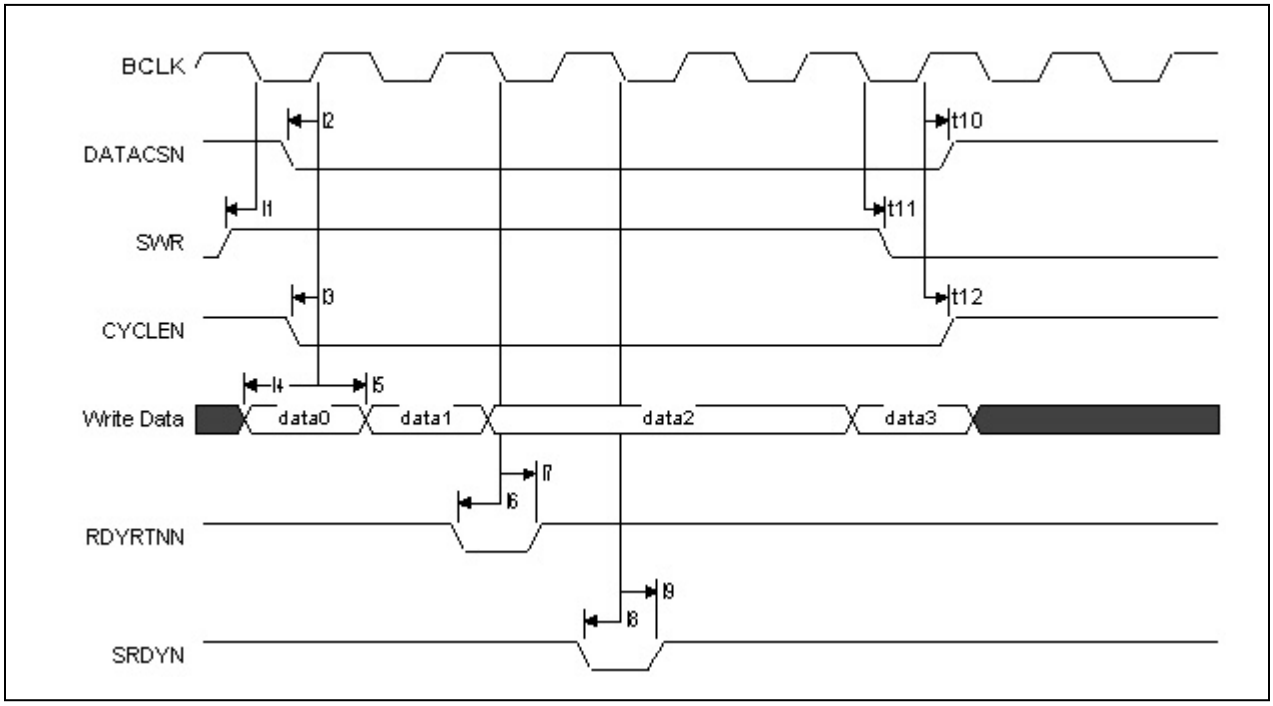


Figure 17. Synchronous Burst Write Cycles – VLBUSN = 1

Symbol	Parameter	Min	Typ	Max	Unit
t1	SWR setup to BCLK falling	4			ns
t2	DATDCSN setup to BCLK rising	4			ns
t3	CYCLEN setup to BCLK rising	4			ns
t4	Write data setup to BCLK rising	6			ns
t5	Write data hold to BCLK rising	2			ns
t6	RDYRTNN setup to BCLK falling	5			ns
t7	RDYRTNN hold to BCLK falling	3			ns
t8	SRDYN setup to BCLK rising	4			ns
t9	SRDYN hold to BCLK rising	3			ns
t10	DATACSN hold to BCLK rising	2			ns
t11	SWR hold to BCLK falling	2			ns
t12	CYCLEN hold to BCLK	2			ns

Table 20. Synchronous Burst Write Timing Parameters

Synchronous Timing in Burst Read (VLBUSN = 1)

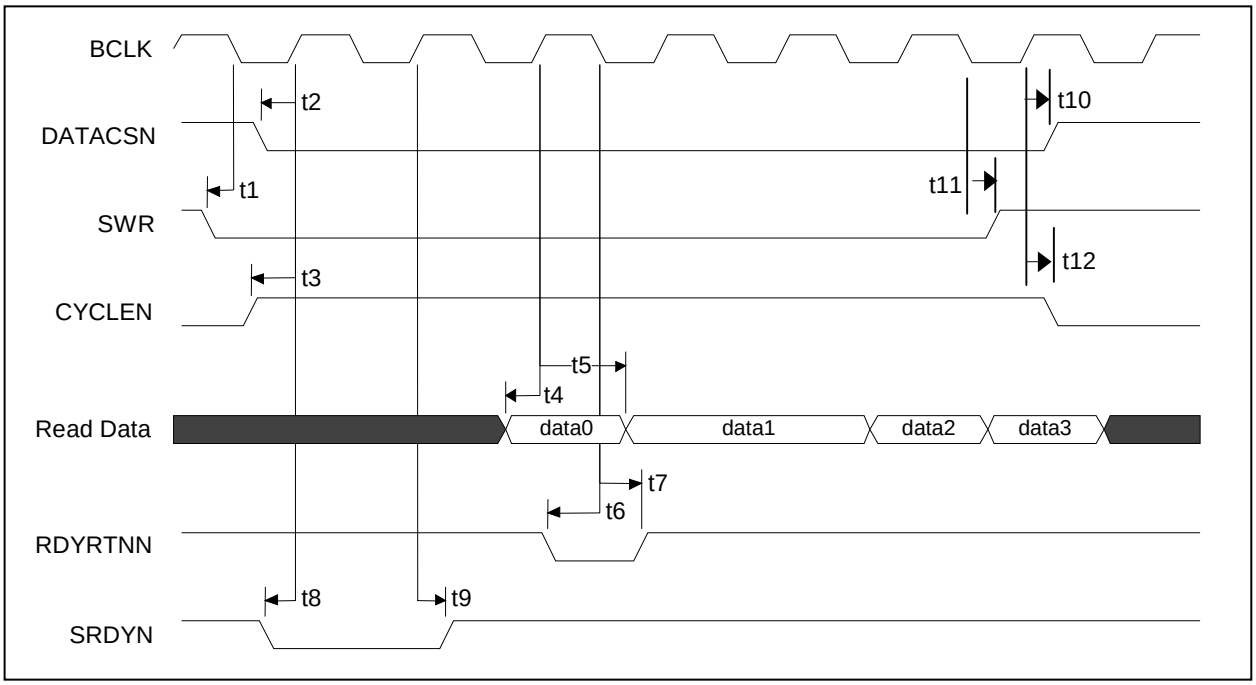


Figure 18. Synchronous Burst Read Cycles – VLBUSN = 1

Symbol	Parameter	Min	Typ	Max	Unit
t1	SWR setup to BCLK falling	4			ns
t2	DATDCSN setup to BCLK rising	4			ns
t3	CYCLEN setup to BCLK rising	4			ns
t4	Read data setup to BCLK rising	6			ns
t5	Read data hold to BCLK rising	2			ns
t6	RDYRTNN setup to BCLK falling	5			ns
t7	RDYRTNN hold to BCLK falling	3			ns
t8	SRDYN setup to BCLK rising	4			ns
t9	SRDYN hold to BCLK rising	3			ns
t10	DATACSN hold to BCLK rising	2			ns
t11	SWR hold to BCLK falling	2			ns
t12	CYCLEN hold to BCLK	2			ns

Table 21. Synchronous Burst Read Timing Parameters

Synchronous Write Timing (VLBUSN = 0)

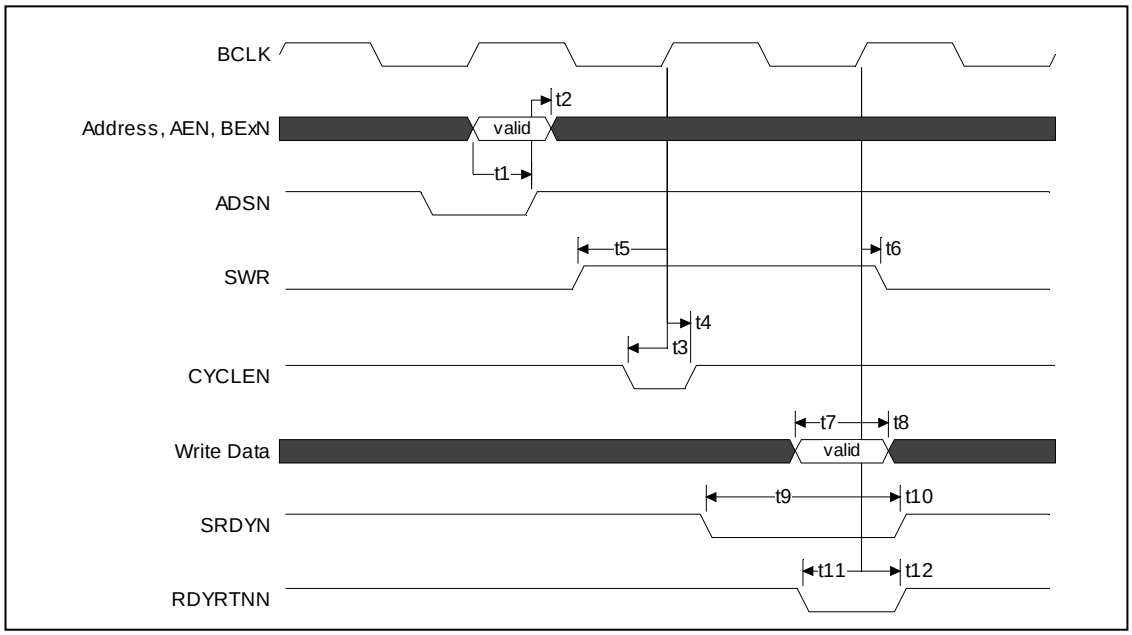


Figure 19. Synchronous Write Cycle – VLBUSN = 0

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] setup to ADSN rising	4			ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2			ns
t3	CYCLEN setup to BCLK rising	4			ns
t4	CYCLEN hold after BCLK rising (non-burst mode)	2			ns
t5	SWR setup to BCLK	4			ns
t6	SWR hold after BCLK rising with SRDYN active	0			ns
t7	Write data setup to BCLK rising	5			ns
t8	Write data hold from BCLK rising	1			ns
t9	SRDYN setup to BCLK	8			ns
t10	SRDYN hold to BCLK	1			ns
t11	RDYRTNN setup to BCLK	4			ns
t12	RDYRTNN hold to BCLK	1			ns

Table 22. Synchronous Write (VLBUSN = 0) Timing Parameters

Synchronous Read Timing (VLBUSN = 0)

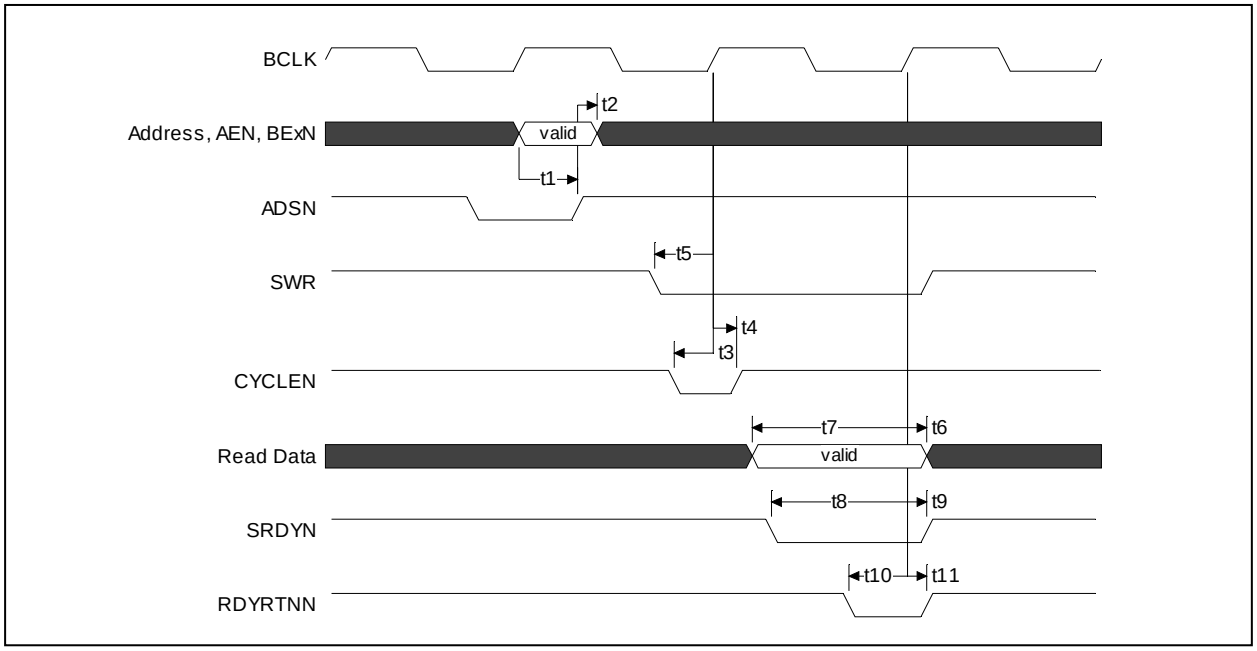


Figure 20. Synchronous Read Cycle – VLBUSN = 0

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] setup to ADSN rising	4			ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2			ns
t3	CYCLEN setup to BCLK rising	4			ns
t4	CYCLEN hold after BCLK rising (non-burst mode)	2			ns
t5	SWR setup to BCLK	4			ns
t6	Read data hold from BCLK rising	1			ns
t7	Read data setup to BCLK	8			ns
t8	SRDYN setup to BCLK	8			ns
t9	SRDYN hold to BCLK	1			ns
t10	RDYRTNN setup to BCLK rising	4			ns
t11	RDYRTNN hold after BCLK rising	1			ns

Table 23. Synchronous Read (VLBUSN = 0) Timing Parameters

Auto Negotiation Timing

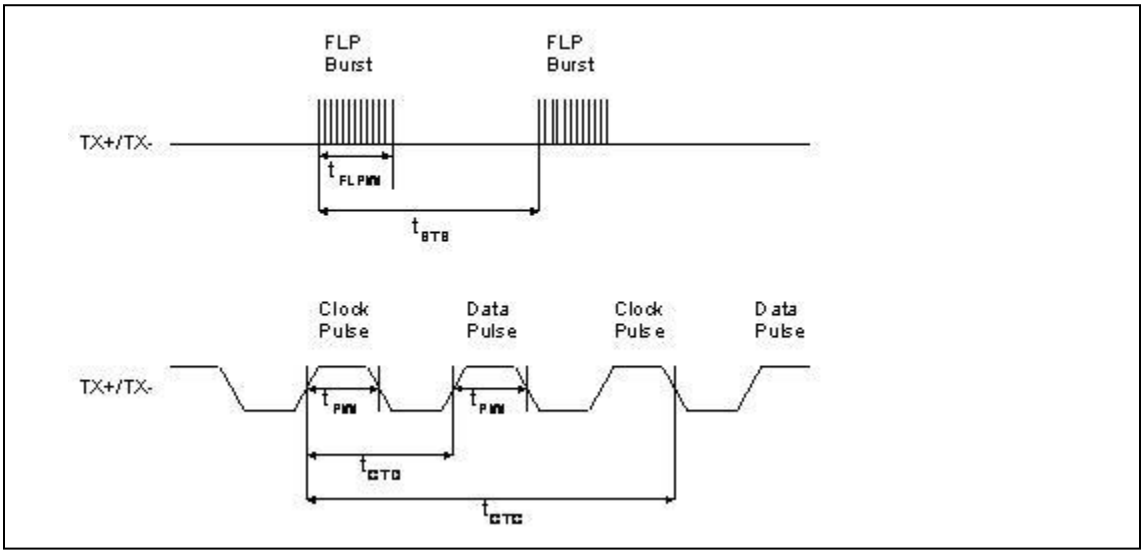


Figure 21. Auto Negotiation Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of Clock/Data pulses per burst	17		33	

Table 24. Auto Negotiation Timing Parameters

Reset Timing

As long as the stable supply voltages to reset High timing (minimum of 10ms) are met, there is no power-sequencing requirement for the KSZ8841M supply voltages (3.3V).

The reset timing requirement is summarized in the Figure 22 and Table 25.

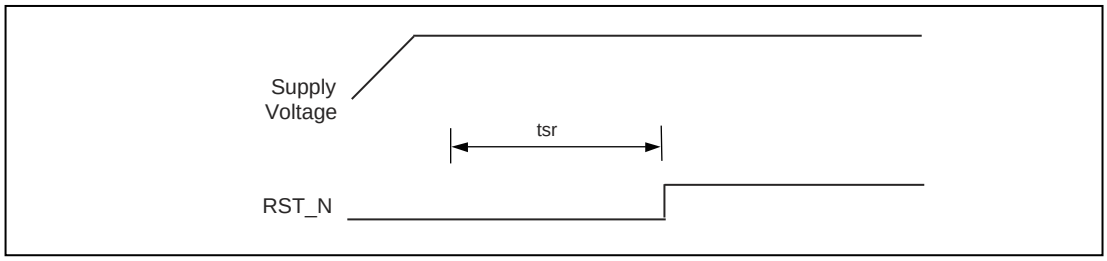


Figure 22. Reset Timing

Symbol	Parameter	Min	Max	Unit
tsr	Stable supply voltages to reset High	10		ms

Table 25. Reset Timing Parameters

EEPROM Timing

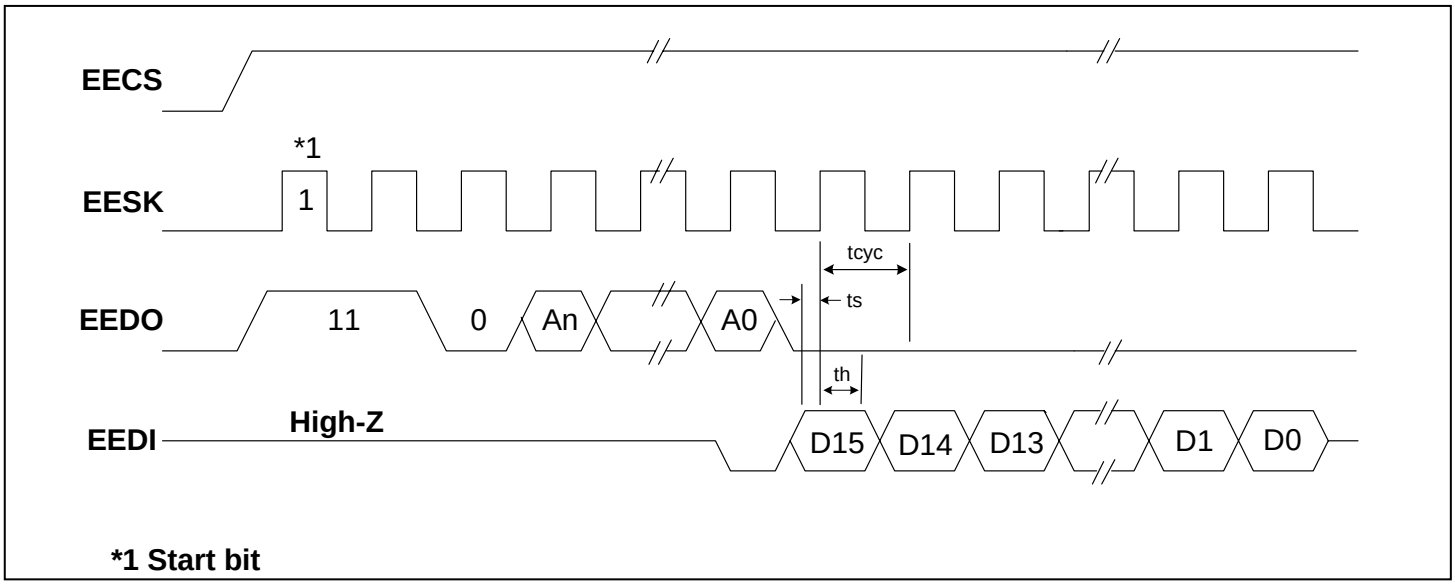


Figure 23. EEPROM Read Cycle Timing Diagram

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc	Clock cycle		4 (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 0.8 (OBCR[1:0]=00 on-chip bus speed @ 125 MHz)		µs
ts	Setup time	20			ns
th	Hold time	20			ns

Table 26. EEPROM Timing Parameters

Selection of Isolation Transformers

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 27 gives recommended transformer characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min)	350μH	100mV, 100kHz, 8mA
Leakage inductance (max)	0.4μH	1MHz (min)
Inter-winding capacitance (max)	12pF	
D.C. resistance (max)	0.9Ω	
Insertion loss (max)	1.0dB	0MHz – 65MHz
HIPOT (min)	1500Vrms	

Table 27. Transformer Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
TDK (Mag Jack)	TLA-6T718	Yes	1

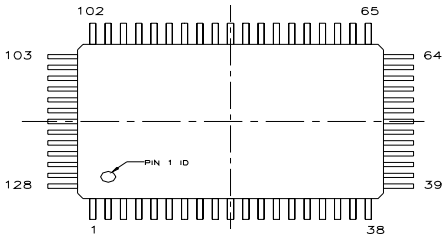
Table 28. Qualified Single Port Magnetics

Selection of Reference Crystal

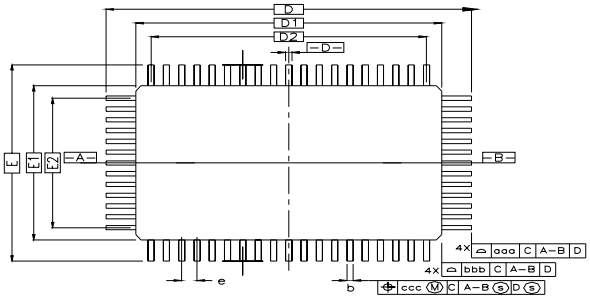
Chacteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm
Load capacitance (max)	20	pF
Series resistance	25	Ω

Table 29. Typical Reference Crystal Characteristics

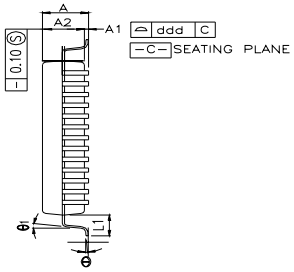
Package Information



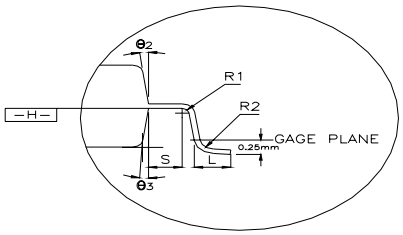
TOP VIEW



BOTTOM VIEW



SIDE VIEW

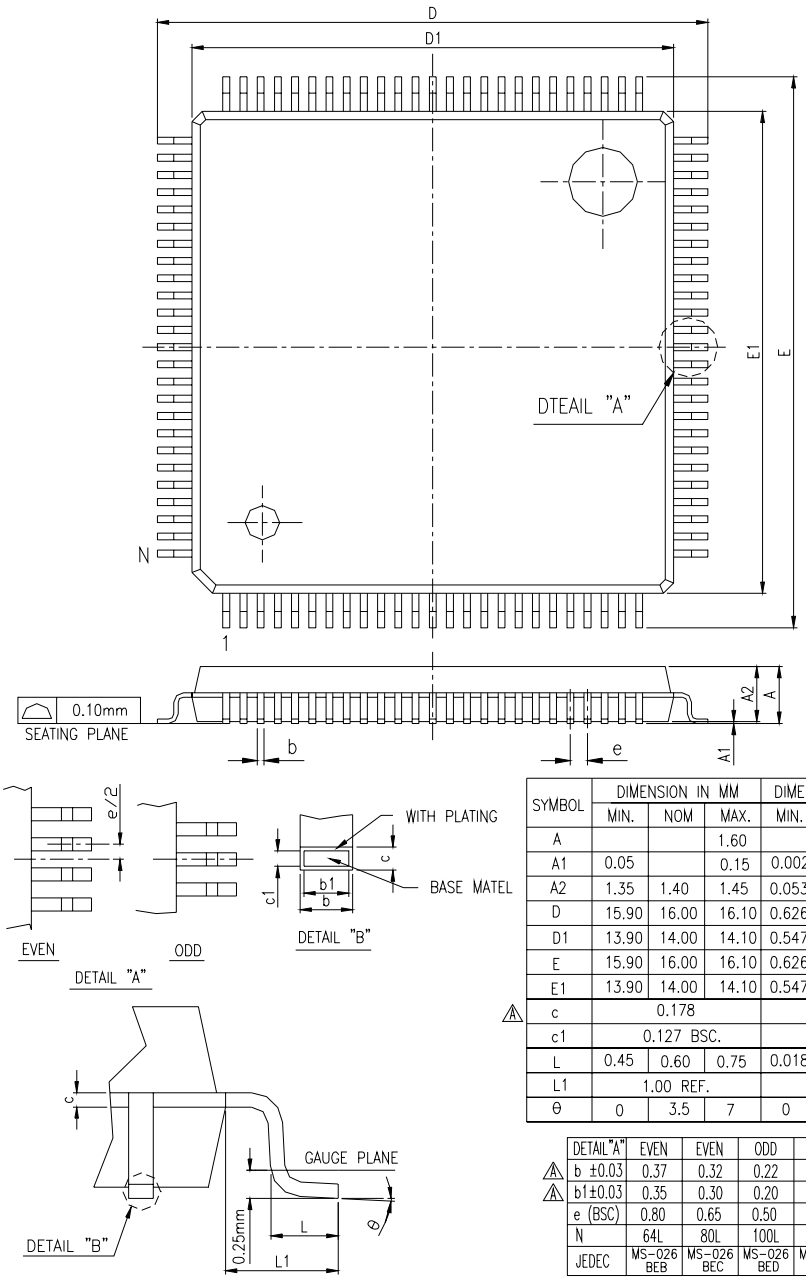


DETAILED VIEW

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	——	——	3.40	——	——	0.134
A1	0.25	——	——	0.010	——	——
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	——	0.30	0.005	——	0.012
R1	0.13	——	——	0.005	——	——
θ	0°	——	7°	0°	——	7°
θ1	0°	——	——	0°	——	——
θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L 1	1.60 REF			0.063 REF		
S	0.20	——	——	0.008	——	——
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

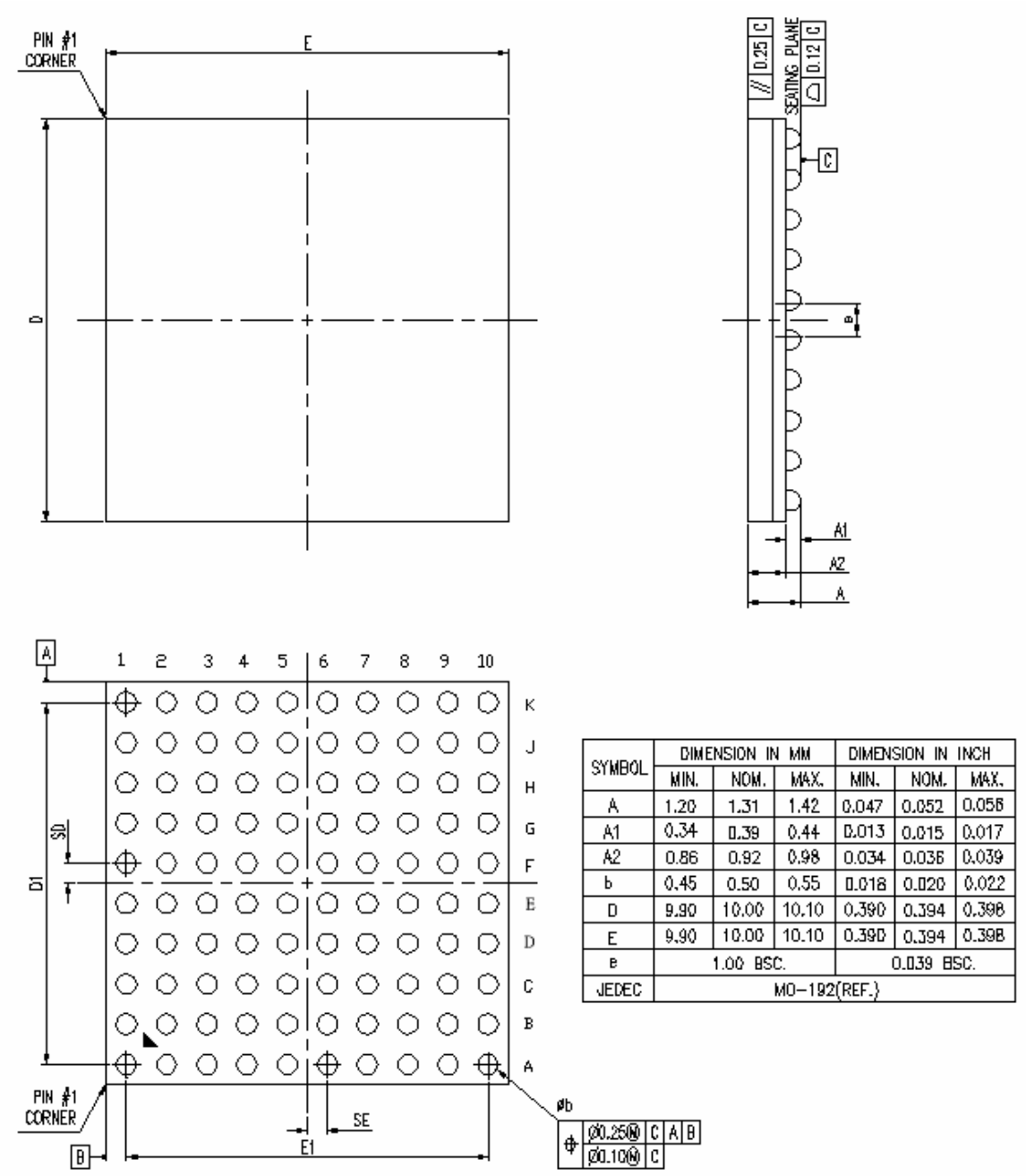
Figure 24. 128-Pin PQFP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.90	16.00	16.10	0.626	0.630	0.634
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
⚠4 c		0.178			0.007	
c1		0.127 BSC.			0.005 BSC.	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF.			0.039 REF.	
θ	0	3.5	7	0	3.5	7

DETAIL"A"	EVEN	EVEN	ODD	EVEN	EVEN
⚠3 b ±0.03	0.37	0.32	0.22	0.18	0.18
⚠3 b1±0.03	0.35	0.30	0.20	0.16	0.16
e (BSC)	0.80	0.65	0.50	0.40	0.40
N	64L	80L	100L	120L	128L
JEDEC	MS-026 BEB	MS-026 BEC	MS-026 BED	MS-026 BEE	

Figure 25. Optional 128-Pin LQFP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.20	1.31	1.42	0.047	0.052	0.056
A1	0.34	0.39	0.44	0.013	0.015	0.017
A2	0.86	0.92	0.98	0.034	0.036	0.039
b	0.45	0.50	0.55	0.018	0.020	0.022
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC.			0.039 BSC.		
JEDEC	MO-192(REF.)					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)	JEDEC(Ref.)
100	0.50 BSC.	0.50 BSC.	8.00 BSC.	9.00 BSC.	

Figure 26. Optional 100-Ball LFBGA Package

Acronyms and Glossary

BIU	Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
Cut-through switch		A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EEPROM	Electronically Erasable Programmable Read-only Memory	A design in which memory on a chip can be erased by exposing it to an electrical charge.
EISA	Extended Industry Standard Architecture	A bus architecture designed for PCs using 80x86 processors, or an Intel 80386, 80486 or Pentium microprocessor. EISA buses are 32 bits wide and support multiprocessing.
EMI	Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP	Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
Jumbo Packet		A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore 'media dependent.'

MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID	Non Port VLAN ID	The Port VLAN ID value is used as a VLAN reference.
PLL	Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PME	Power Management Event	An occurrence that affects the directing of power to different components of a system.
QMU	Queue Management Unit	Manages packet traffic between MAC/PHY interface and the system host. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).
SA	Source Address	The address from which information has been sent.
TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal -- or part of the signal -- to return.
UTP	Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

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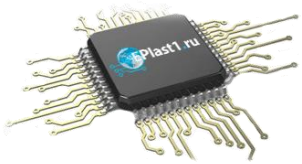

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