LTC2380-24/LTC2368-24: 24-Bit, 2Msps/1Msps, Low Power, SAR ADCs with Digital Filter

DESCRIPTION

The LTC®2380-24 and LTC2368-24 are low power, low noise, high speed, 24-bit SAR ADCs with an integrated digital averaging filter that operates from a single 2.5V supply. The following text refers to the LTC2380-24 but applies to both parts. The LTC2380-24 has fully differential inputs and samples at 2Msps, while the LTC2368-24 has pseudo-differential inputs and samples at 1Msps. The LTC2380-24 has –117dB THD, consumes only 28mW and achieves ±3.5ppm INL max with no missing codes at 24 bits. The DC2289A demonstrates the DC and AC performance of the LTC2380-24 in conjunction with the DC590 or DC2026 QuikEval™ and DC890 PScope™ data collection boards. Use the DC590 or DC2026 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The Demonstration Circuit 2289A is intended to show recommended grounding, component placement and selection, routing and bypassing for this ADC.

Design files for this circuit board including the schematic, BOM and layout are available at http://www.linear.com/demo/DC2289A or scan the QR code on the back of the board.

BOARD PHOTO

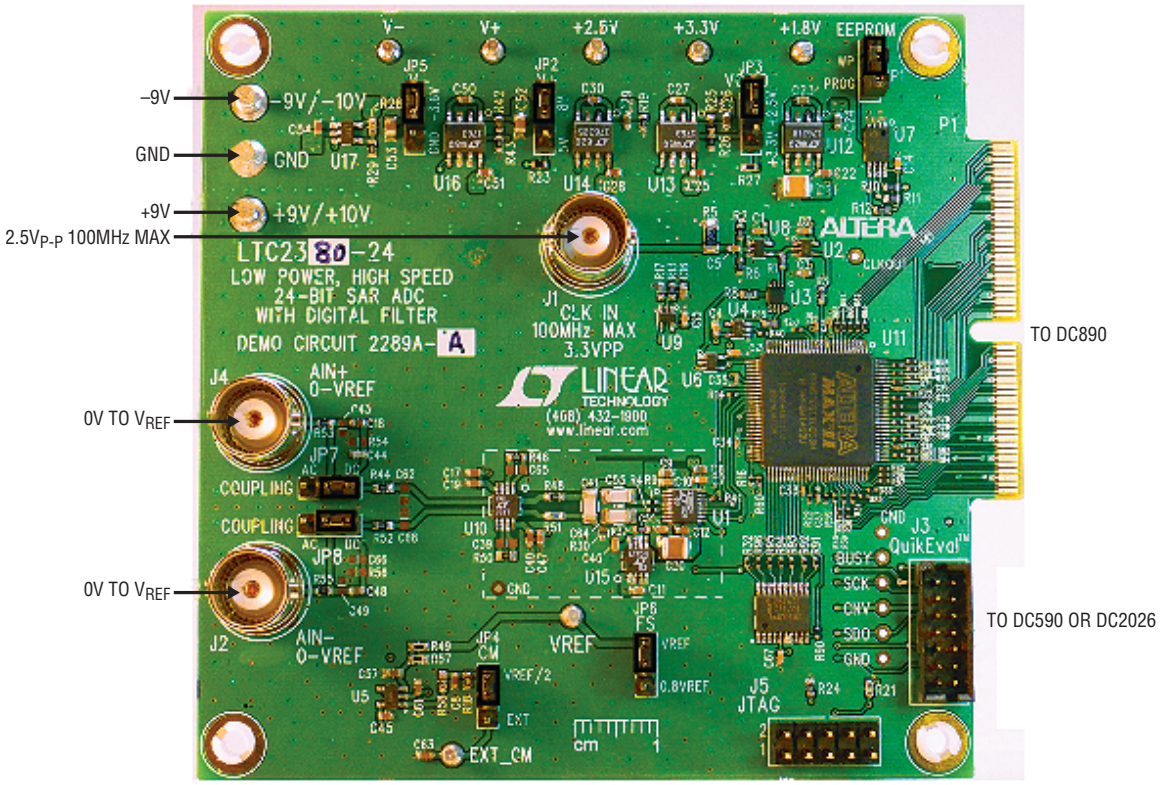

Figure 1. DC2289A Connection Diagram

ASSEMBLY OPTIONS

Table 1. DC2289A Assembly and Clock Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX SAMPLE RATE (Msps)	NUMBER OF BITS	MAX CLKIN FREQUENCY (MHz)	MODE	DIVIDER
DC2289A-A	LTC2380IMS-24	1.515	24	100	Normal	66
		1.205		100	Normal/Verify	83
		1.923		100	Distributed Read	52
DC2289A-B	LTC2368IMS-24	0.909	24	60	Normal	66
		0.746		62	Normal/Verify	83
		1.0		52	Distributed Read	52

DC890 QUICK START PROCEDURE

Check to make sure that all jumpers are set as described in the DC2289A Jumpers paragraph. In particular make sure that VCCIO (JP3) is set to the 2.5V position. Controlling the DC2289A with the DC890 while JP3 of the DC2289A is in the 3.3V position will cause noticeable performance degradation in SNR and THD. The default jumper connections configure the ADC to use the onboard reference and regulators. The analog input is DC coupled by default. Connect the DC2289A to a DC890 USB High Speed Data Collection Board using connector P1. (Do not connect a PScope controller and QuikEval controller at the same time.) Next, connect the DC890 to a host PC with a standard USB A/B cable. Apply ±9V to the indicated terminals. Next apply a low jitter differential sine source to J2 and J4. (The voltage applied at the inputs J2 and J4 should be out of phase and have a common mode voltage of $V_{REF}/2$ ±100mV.) Connect a low jitter $2.5V_{P-P}$ sine wave or square wave to connector J1, using Table 1 as a guide for the appropriate clock frequency. Note that J1 has a 49.9Ω termination resistor to ground.

Run the PScope software (PScope.exe version K80 or later) supplied with the DC890 or download it from www.linear.com/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2289A and configure itself automatically. The default setup is for a normal data capture with the number of averages set to one. To change this, click on the Set Demo Bd Options setting of the PScope Tool Bar as shown in Figure 2. The Configuration Options box shown in Figure 3 allows the number of averages and data capture mode to be selected. Normal mode clocks out 24 bits of data. If Verify is selected the number of bits clocked out is increased to 40 which includes the number of samples taken for the current output. Distributed Read allows a slow clock (one clock pulse per conversion) but requires the number of averages to be at least 25. With Distributed Read selected, Verify is not allowed. The number of averages can be set to an integer between 1 and 65535. Increasing N will improve the SNR. Theoretically, SNR will improve by 6dB if the number of averages is increased by a factor of four. In practice, reference noise will eventually limit the SNR improvement. Increasing the REF bypass capacitor (C20) or using a lower noise external reference will extend this limit.

Click the Collect button (see Figure 4) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

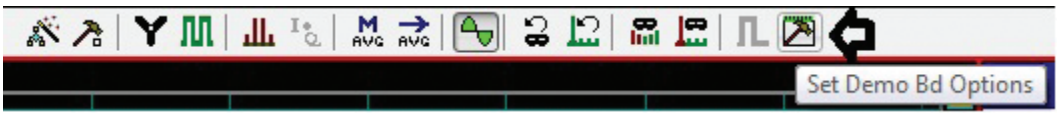

Figure 2. PScope Toolbar

DC890 QUICK START PROCEDURE

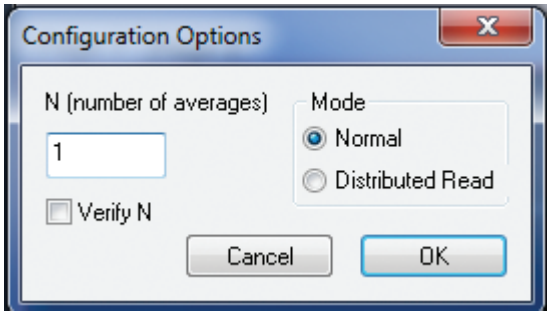

Figure 3. Configuration Options

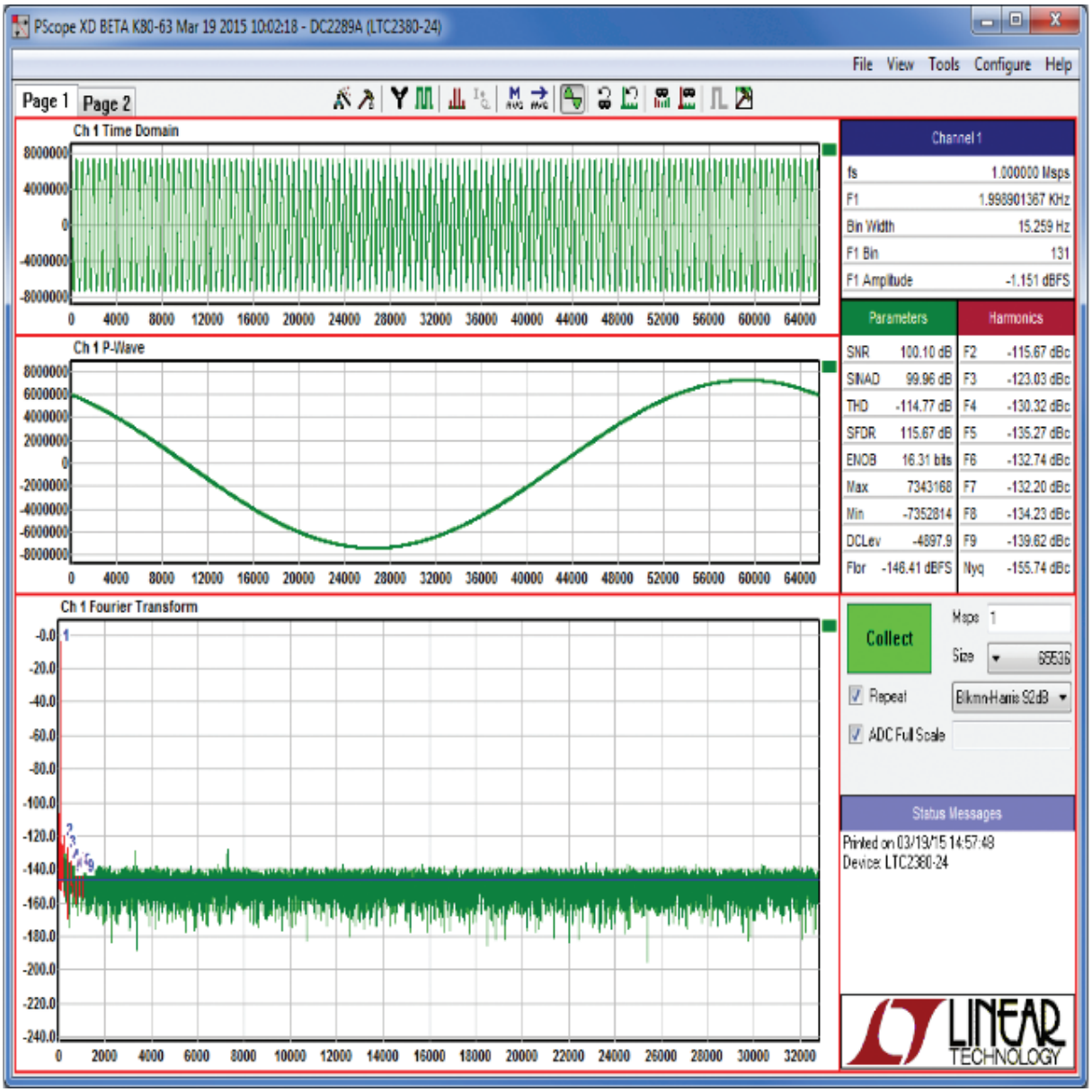

Figure 4. PScope Screen Shot

DC590 OR DC2026 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2289A, make sure that JP6 of the DC590 or JP3 of the DC2026 is set to 3.3V before connecting to the DC2289A.

VCCIO (JP3) of the DC2289A should be in the 3.3V position for DC590 or DC2026 (QuikEval) operation. To use a QuikEval controller with the DC2289A, it is necessary to apply –9V and ground to the –9V and GND terminals. Connect the QuikEval controller to a host PC with a standard USB A/B cable. Connect the DC2289A to a QuikEval controller using the supplied 14-conductor ribbon cable. (Do not connect both a QuikEval and PScope controller at the same time.) Apply a fully differential signal source to J4 and J2. The voltage inputs at J2 and J4 should be out of phase and have a common mode voltage of $V_{REF}/2$ ±100mV. No clock signal is necessary at J1 when using a QuikEval controller. The clock signal is provided through the QuikEval connector (J3). +9V for the DC2289A is also provided through the QuikEval connector.

Run the QuikEval software (version K105 or later) supplied with the QuikEval controller or download it from www.linear.com/software. The correct control panel will be loaded automatically. Click the COLLECT button (see Figure 5) to begin reading the ADC.

Increasing the number of averages will reduce the noise as shown in the histogram of Figure 6. The noise will be reduced by the square root of the number of times the number of samples is increased. In practice, reference noise will eventually limit the noise improvement. Increasing the REF bypass capacitor (C20) or using a lower noise external reference will extend this limit.

The maximum number of averages allowed by QuikEval is 65535.

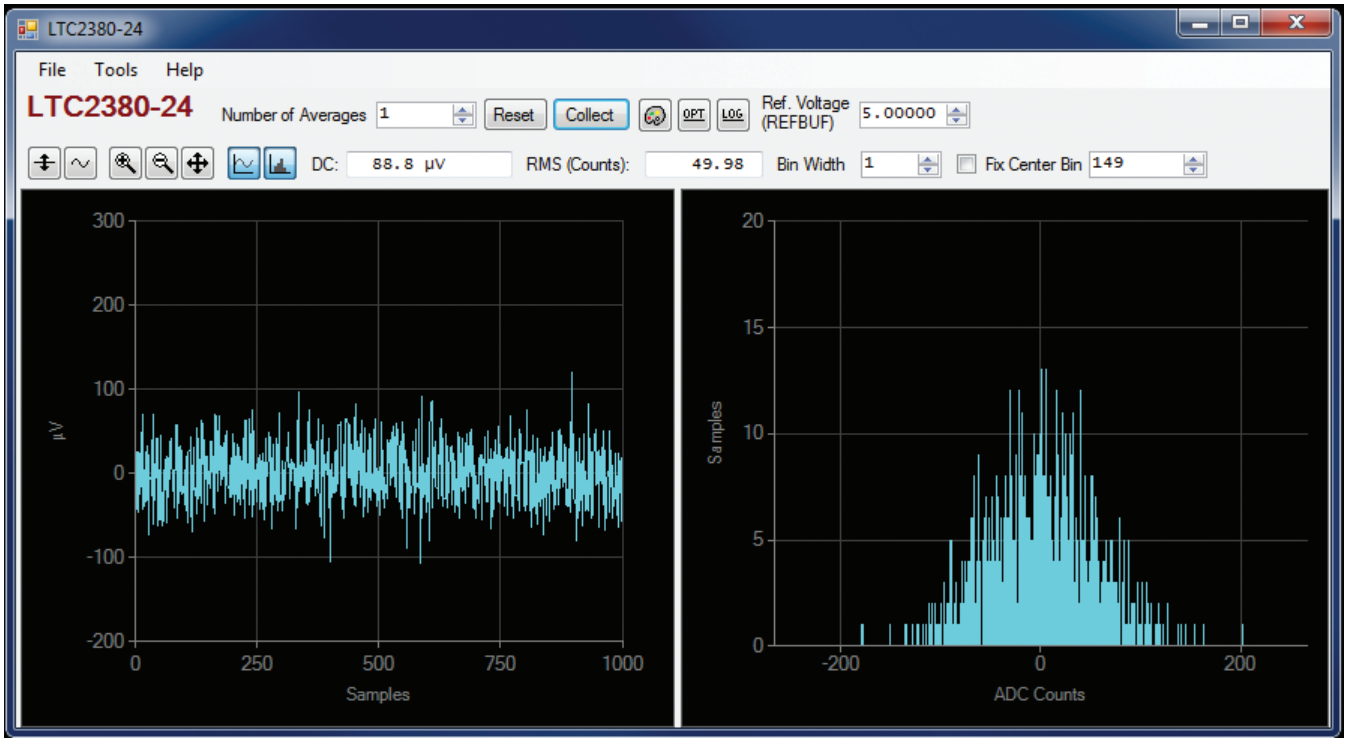

Figure 5. QuikEval Histogram with Number of Averages = 1

DC590 OR DC2026 QUICK START PROCEDURE

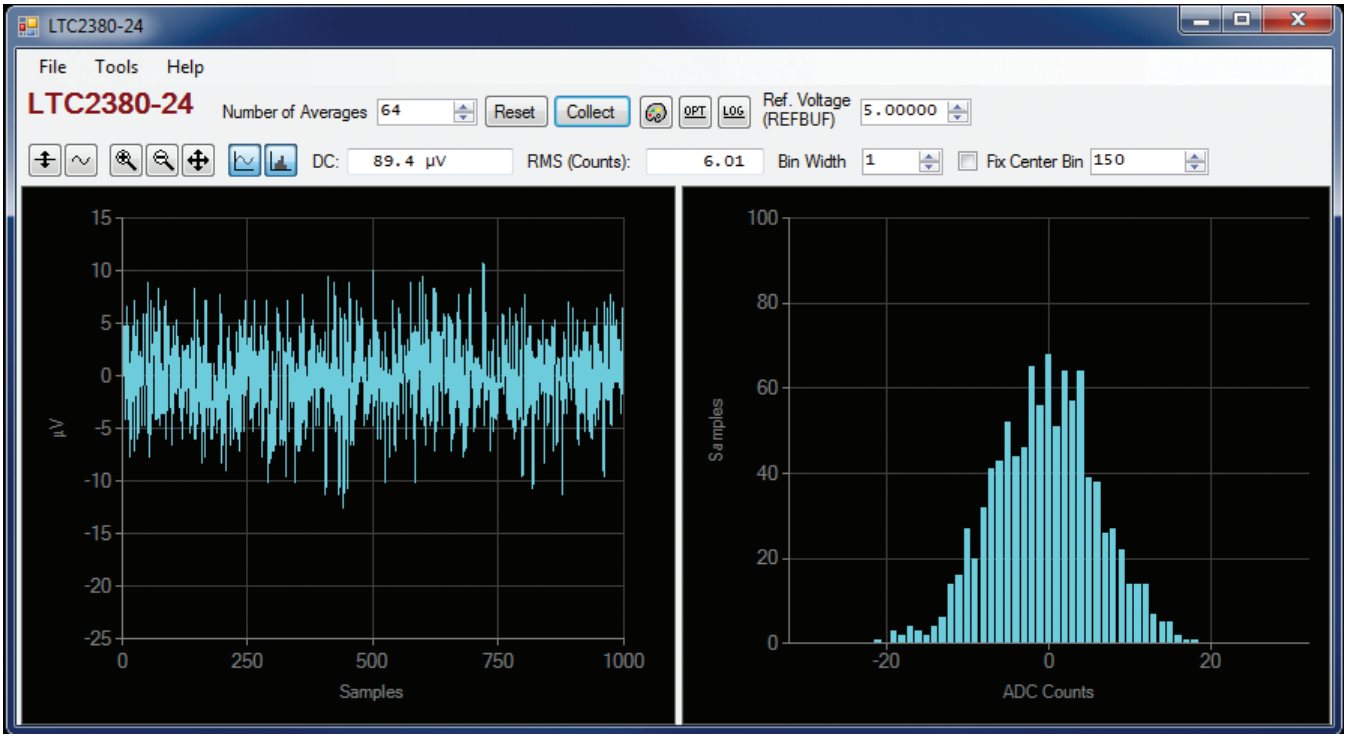

Figure 6. QuikEval Histogram with Number of Averages = 64

HARDWARE SETUP

DC2289A JUMPERS DEFINITIONS

JP1 – EEPROM is for factory use only. Leave this in the default WP position.

JP2 – V+ Selects 8V or 5V for the positive op amp supply. The default position is 8V. Setting V+ to 5V is useful for evaluating single 5V supply operation of the buffer when operating the ADC with Digital Gain Compression turned on.

JP3 – VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890 which is the default setting. Use 3.3V to interface to the DC590 or DC2026.

JP4 – VCM sets the DC bias for A_{IN}^+ and A_{IN}^- if the inputs are AC coupled. To enable AC coupling, R35 and R36 (R = 1k) must be installed. Installing these resistors will degrade the THD of the input signal to the ADC. $V_{REF}/2$ is the default setting.

JP5 – V– Selects –3.6V or ground for the negative op amp supply. The default is setting is –3.6V. Setting V– to ground is useful for evaluating single supply operation of the buffer when operating the ADC with Digital Gain Compression turned on.

JP6 – FS selects whether the Digital Gain Compression is on or off. In the V_{REF} position, Digital Gain Compression is off and the analog input range at A_{IN}^+ and A_{IN}^- is 0V to V_{REF}. In the $0.8V_{REF}$ position, Digital Gain Compression is turned on and the analog input range at A_{IN}^+ and A_{IN}^- is $0.1V_{REF}$ to $0.9V_{REF}$. The default setting is V_{REF}, disabling DGC.

JP7 – Coupling selects AC or DC coupling of A_{IN}^+. The default setting is DC.

JP8 – Coupling selects AC or DC coupling of A_{IN}^-. The default setting is DC.

DC2289A SETUP

DC POWER

The DC2289A requires ±9VDC and draws approximately +65mA/–10mA when operating with a 100MHz clock. Most of the supply current is consumed by the CPLD, op amps, regulators and discrete logic on the board. The +9VDC input voltage powers the ADC through LT®1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and op amps. See Figure 1 for connection details.

CLOCK SOURCE

You must provide a low jitter $2.5V_{P-P}$ (If VCCIO is in the 3.3V position, the clock amplitude should be $3.3V_{P-P}$.) sine or square wave to J1. The clock input is AC coupled so the DC level of the clock signal is not important. A clock generator like the Rohde & Schwarz SMB100A or the DC1216A is recommended. Even a good clock generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired input frequency. The ratio of clock frequency to conversion rate is shown in Table 1. If the clock input is to be driven with logic, it is recommended that the 50Ω terminator (R5) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high-amplitude higher frequency input signals.

DATA OUTPUT

Parallel data output from this board (0V to 2.5V by default), if not connected to the DC890, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 50 of P1 to latch the data. The data can be latched using the falling edge of this signal. In Verify mode, two falling edges are required for each data sample with the data output as indicated on the P1 connector of the schematic. The data output signal levels at P1 can also be changed to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving VCCIO (JP3) to the 3.3V position.

REFERENCE

The default reference is the LTC6655 5V reference. If an external reference is used, it must settle quickly in the presence of glitches on the REF pin. To use an external reference, unsolder R37 and apply the reference voltage to the V_{REF} terminal.

ANALOG INPUT

The default driver for the analog inputs of the LTC2380-24 on the DC2289A is shown in Figure 7. This circuit buffers a fully differential 0V to 5V input signal applied at A_{IN}^+ and A_{IN}^-. (The inputs at J2 and J4 should be out of phase and have a common mode voltage of $V_{REF}/2$ ±100mV.) In addition, this circuit band limits the input frequencies at the ADC input to approximately 940kHz.

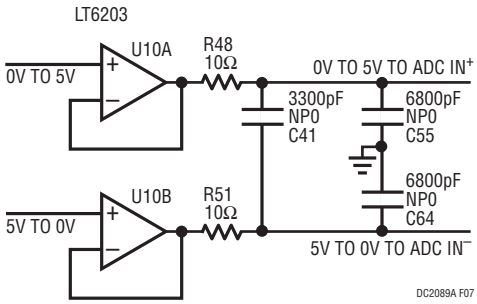

Figure 7. Fully Differential Driver

DATA COLLECTION

For SINAD, THD or SNR testing a low noise, low distortion differential output sine generator such as the Stanford Research SR1 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A or DC1216A is used as the clock source.

This demo board is tested in house by attempting to duplicate the FFT plot shown in the typical performance characteristics of the LTC2380-24 data sheet. This involves using a 100MHz clock source, along with a differential output sinusoidal generator at a frequency of 2kHz. The input signal level is approximately –1dBFS. The input is level shifted and filtered with the circuit shown in Figure 8. A typical FFT obtained with DC2289A is shown in Figure 4.

DC2289A SETUP

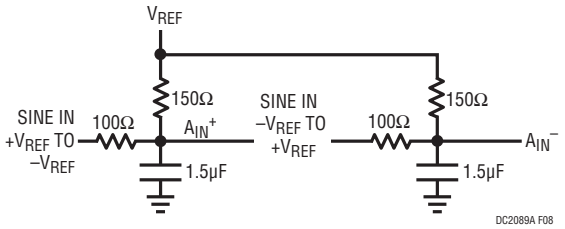

Figure 8. Differential Level Shifter

Note that to calculate the real SNR, the signal level (F1 amplitude = –1.151dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 4, this means that the actual SNR would be 101.251dB instead of the 100.10dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 101.06dB which is fairly close to the typical number for this ADC.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a submultiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a sine generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If windowing is required, the Blackman-Harris 92dB window is recommended. If an amplifier or clock source with poor phase noise is used, windowing will not improve the SNR.

LAYOUT

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2289A should be used as a guideline for placement and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2380-24. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use low impedance returns directly to the ground plane for each bypass capacitor. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

COMPONENT SELECTION

When driving a low noise, low distortion ADC such as the LTC2380-24, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2380-24 should have low distortion, low noise and a fast settling time such as the LT6203.

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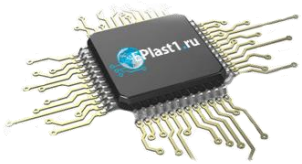

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