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R8C/11 Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0034-0160
Rev.1.60
Jan 27, 2006

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

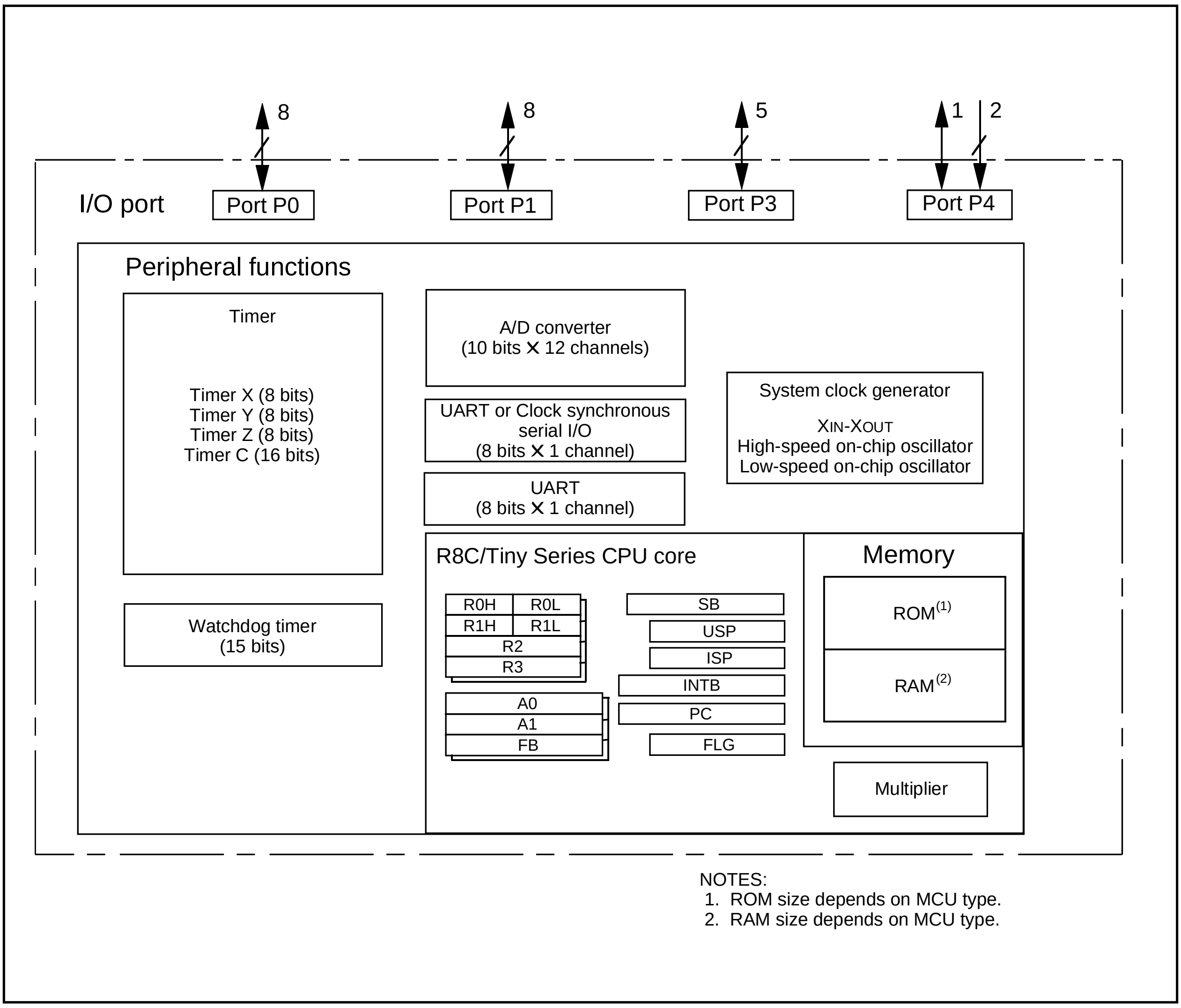
Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(X_{IN})$ = 20 MHz, V_{CC} = 3.0 to 5.5 V) 100 ns ($f(X_{IN})$ = 10 MHz, V_{CC} = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Circuits of input capture and output compare)
	Serial Interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high speed, low speed) On High-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	Included
	Power on reset circuit	Included
Electrical characteristics	Supply voltage	V_{CC} = 3.0 to 5.5 V ($f(X_{IN})$ = 20 MHz) V_{CC} = 2.7 to 5.5 V ($f(X_{IN})$ = 10 MHz)
	Power consumption	Typ. 9 mA (V_{CC} = 5.0 V, ($f(X_{IN})$ = 20 MHz) Typ. 5 mA (V_{CC} = 3.0 V, ($f(X_{IN})$ = 10 MHz) Typ. 35 µA (V_{CC} = 3.0 V, Wait mode, Peripheral clock off) Typ. 0.7 µA (V_{CC} = 3.0 V, Stop mode)
Flash memory	Program/erase supply voltage	V_{CC} = 2.7 to 5.5 V
	Program/erase endurance	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.



NOTES:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21112FP	8K bytes	512 bytes	PLQP0032GB-A	Flash memory version
R5F21113FP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21114FP	16K bytes	1K bytes	PLQP0032GB-A	
R5F21112DFP	8K bytes	512 bytes	PLQP0032GB-A	D version
R5F21113DFP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21114DFP	16K bytes	1K bytes	PLQP0032GB-A	

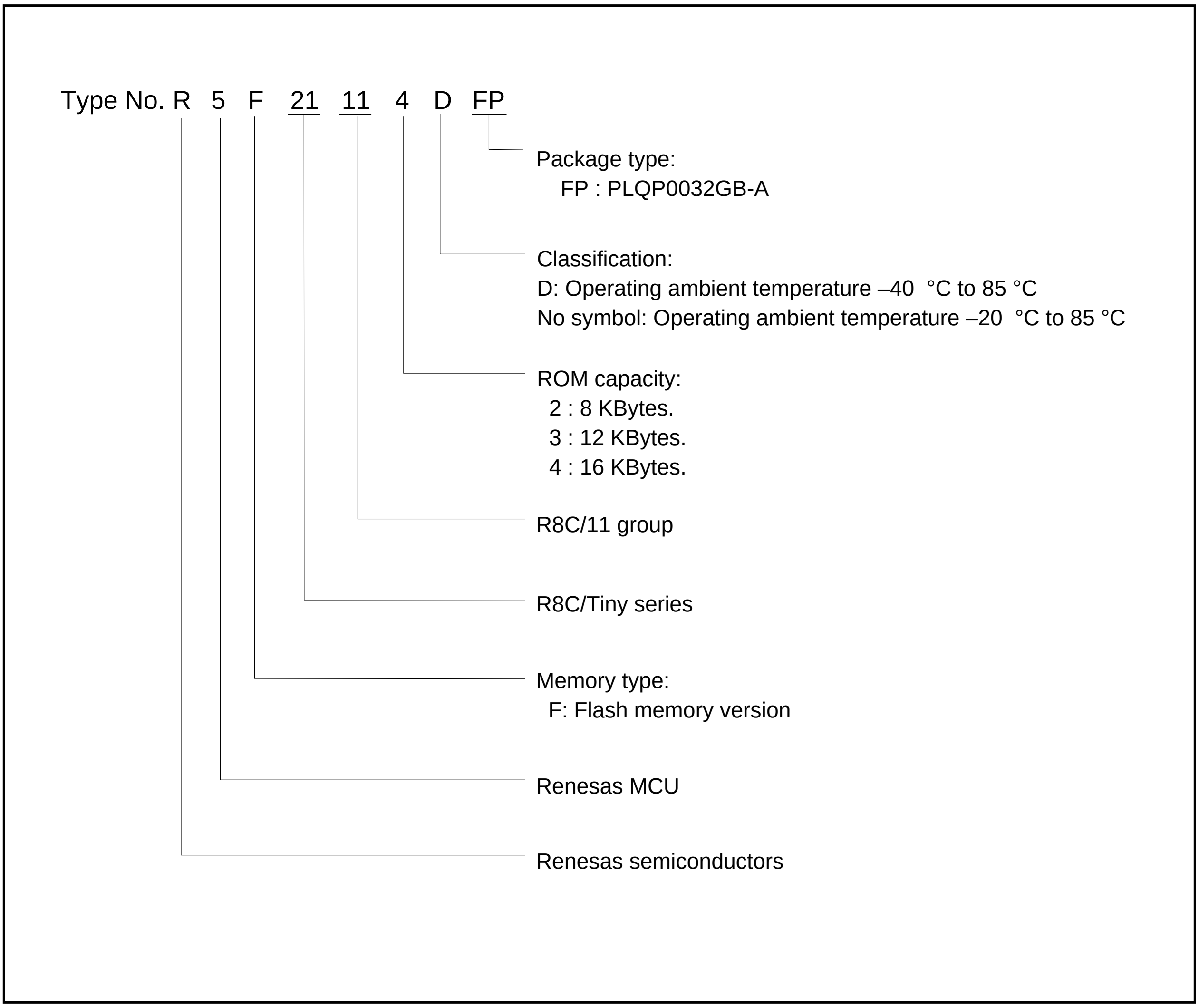
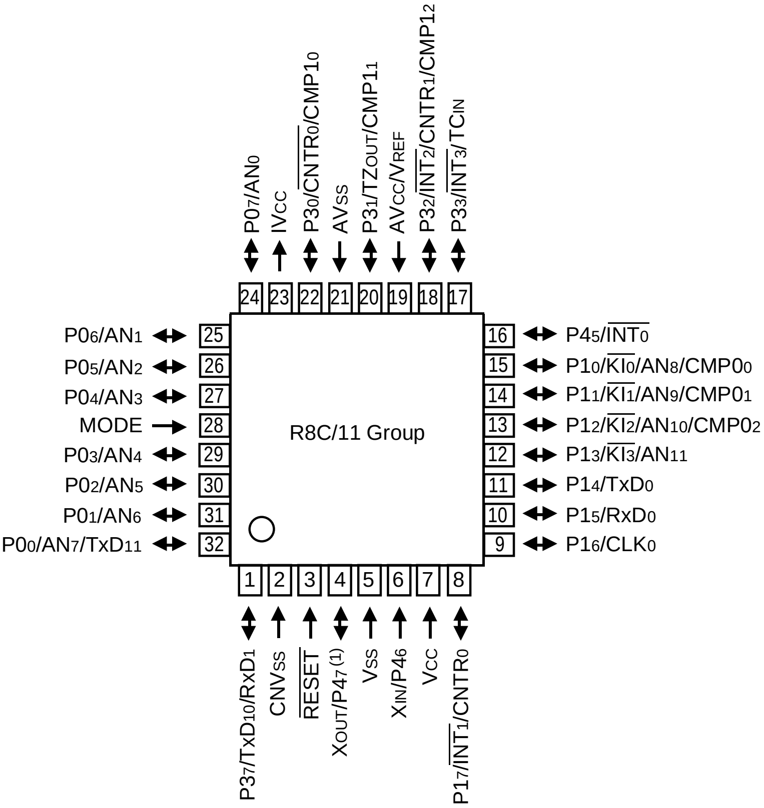


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

PIN CONFIGURATION (top view)



NOTES:
1. P4$_7$ functions only as an input port.
2. When using On-chip debugger, do not use pins P0$_0$/AN$_7$/TxD$_{11}$ and P3$_7$/TxD$_{10}$/RxD$_1$.
3. Do not connect IVcc to Vcc.

Package: PLQP0032GB-A (32P6U-A)

Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

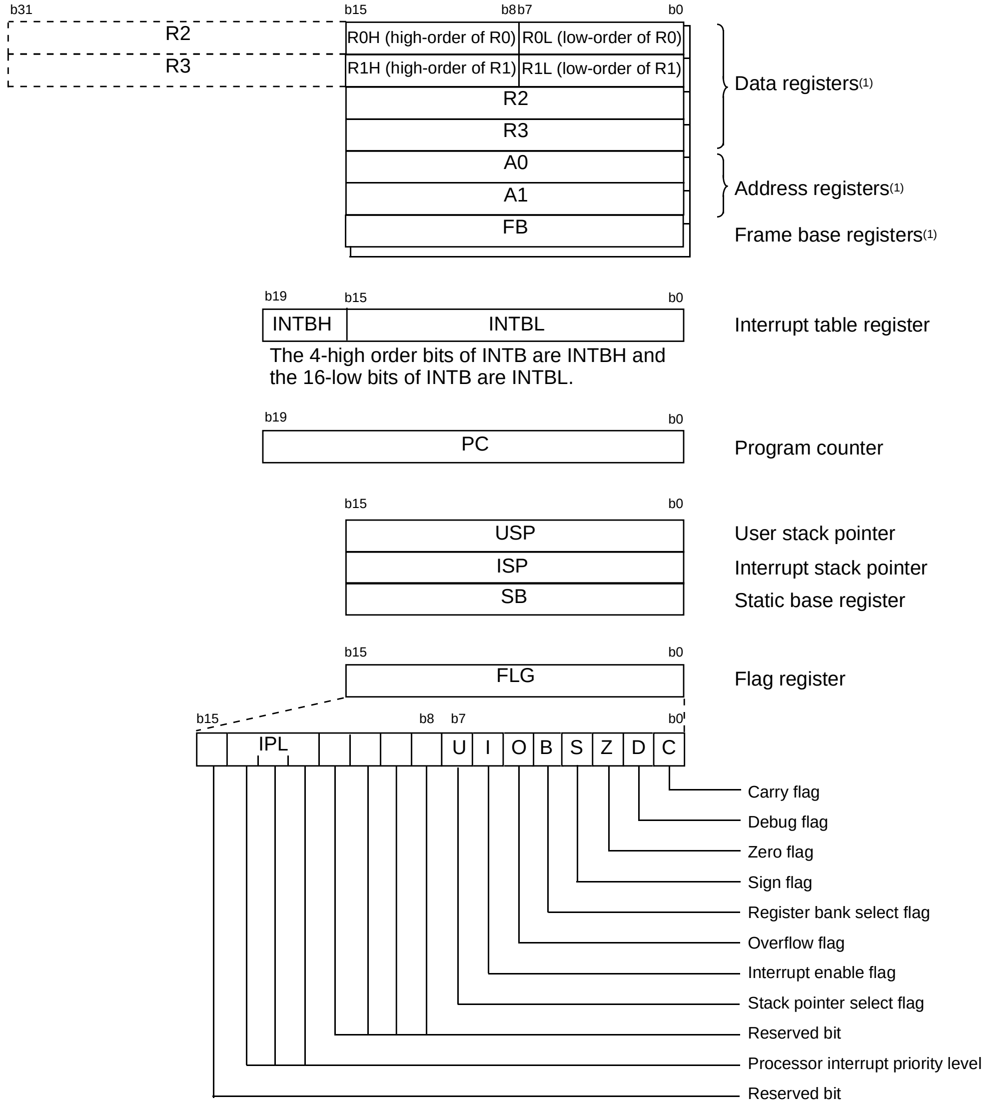
Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 µF). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP00 to CMP02, CMP10 to CMP12	O	Timer C output pins
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.



NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided

Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.

The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to “0”.

2.8.3 Zero Flag (Z)

The Z flag is set to “1” when an arithmetic operation resulted in 0; otherwise, “0”.

2.8.4 Sign Flag (S)

The S flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, “0”.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is “0”. The register bank 1 is selected when this flag is set to “1”.

2.8.6 Overflow Flag (O)

The O flag is set to “1” when the operation resulted in an overflow; otherwise, “0”.

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to “0”, and are enabled when the I flag is set to “1”. The I flag is set to “0” when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to “0”, USP is selected when the U flag is set to “1”.

The U flag is set to “0” when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

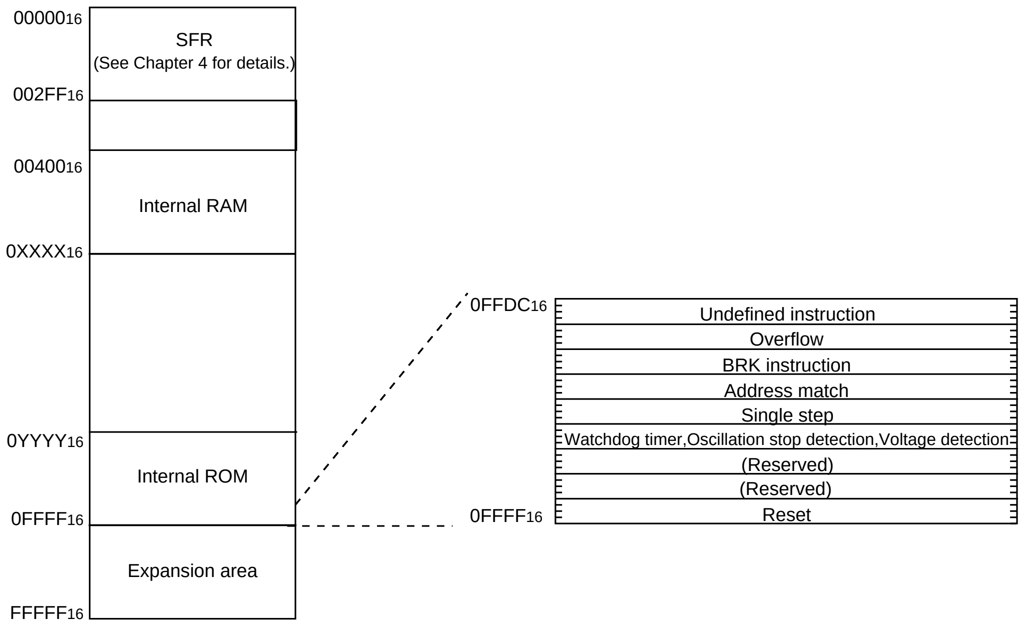
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to “0”. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$.
The internal ROM is allocated lower addresses beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated addresses from $0C000_{16}$ to $0FFFF_{16}$.
The fixed interrupt vector table is allocated addresses $0FFDC_{16}$ to $0FFFF_{16}$. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated addresses 00400_{16} to $007FF_{16}$. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.
Special function registers (SFR) are allocated addresses 00000_{16} to $002FF_{16}$. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



NOTES :
1. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address $0YYYY_{16}$	Size	Address $0XXXX_{16}$
R5F21114FP, R5F21114DFP	16K bytes	$0C000_{16}$	1K bytes	$007FF_{16}$
R5F21113FP, R5F21113DFP	12K bytes	$0D000_{16}$	768 bytes	$006FF_{16}$
R5F21112FP, R5F21112DFP	8K bytes	$0E000_{16}$	512 bytes	$005FF_{16}$

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000$_{16}$			
0001$_{16}$			
0002$_{16}$			
0003$_{16}$			
0004$_{16}$	Processor mode register 0	PM0	00$_{16}$
0005$_{16}$	Processor mode register 1	PM1	00$_{16}$
0006$_{16}$	System clock control register 0	CM0	01101000$_2$
0007$_{16}$	System clock control register 1	CM1	00100000$_2$
0008$_{16}$	High-speed on-chip oscillator control register 0	HR0	00$_{16}$
0009$_{16}$	Address match interrupt enable register	AIER	XXXXXX00$_2$
000A$_{16}$	Protect register	PRCR	00XXX000$_2$
000B$_{16}$	High-speed on-chip oscillator control register 1	HR1	40$_{16}$
000C$_{16}$	Oscillation stop detection register	OCD	00000100$_2$
000D$_{16}$	Watchdog timer reset register	WDTR	XX$_{16}$
000E$_{16}$	Watchdog timer start register	WDTS	XX$_{16}$
000F$_{16}$	Watchdog timer control register	WDC	00011111$_2$
0010$_{16}$	Address match interrupt register 0	RMAD0	00$_{16}$
0011$_{16}$			00$_{16}$
0012$_{16}$			X0$_{16}$
0013$_{16}$			
0014$_{16}$	Address match interrupt register 1	RMAD1	00$_{16}$
0015$_{16}$			00$_{16}$
0016$_{16}$			X0$_{16}$
0017$_{16}$			
0018$_{16}$			
0019$_{16}$	Voltage detection register 1(2)	VCR1	00001000$_2$
001A$_{16}$	Voltage detection register 2(2)	VCR2	00$_{16}$(3) 10000000$_2$(4)
001B$_{16}$			
001C$_{16}$			
001D$_{16}$			
001E$_{16}$	$\overline{\text{INT0}}$ input filter select register	INT0F	XXXXX000$_2$
001F$_{16}$	Voltage detection interrupt register(2)	D4INT	00$_{16}$(3) 01000001$_2$(4)
0020$_{16}$			
0021$_{16}$			
0022$_{16}$			
0023$_{16}$			
0024$_{16}$			
0025$_{16}$			
0026$_{16}$			
0027$_{16}$			
0028$_{16}$			
0029$_{16}$			
002A$_{16}$			
002B$_{16}$			
002C$_{16}$			
002D$_{16}$			
002E$_{16}$			
002F$_{16}$			
0030$_{16}$			
0031$_{16}$			
0032$_{16}$			
0033$_{16}$			
0034$_{16}$			
0035$_{16}$			
0036$_{16}$			
0037$_{16}$			
0038$_{16}$			
0039$_{16}$			
003A$_{16}$			
003B$_{16}$			
003C$_{16}$			
003D$_{16}$			
003E$_{16}$			
003F$_{16}$			

X : Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of $\overline{\text{RESET}}$ pin = H retaining.

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After reset
0040_{16}			
0041_{16}			
0042_{16}			
0043_{16}			
0044_{16}			
0045_{16}			
0046_{16}			
0047_{16}			
0048_{16}			
0049_{16}			
$004A_{16}$			
$004B_{16}$			
$004C_{16}$			
$004D_{16}$	Key input interrupt control register	KUPIC	$XXXXX000_2$
$004E_{16}$	AD conversion interrupt control register	ADIC	$XXXXX000_2$
$004F_{16}$			
0050_{16}	Compare 1 interrupt control register	CMP1IC	$XXXXX000_2$
0051_{16}	UART0 transmit interrupt control register	S0TIC	$XXXXX000_2$
0052_{16}	UART0 receive interrupt control register	S0RIC	$XXXXX000_2$
0053_{16}	UART1 transmit interrupt control register	S1TIC	$XXXXX000_2$
0054_{16}	UART1 receive interrupt control register	S1RIC	$XXXXX000_2$
0055_{16}	INT2 interrupt control register	INT2IC	$XXXXX000_2$
0056_{16}	Timer X interrupt control register	TXIC	$XXXXX000_2$
0057_{16}	Timer Y interrupt control register	TYIC	$XXXXX000_2$
0058_{16}	Timer Z interrupt control register	TZIC	$XXXXX000_2$
0059_{16}	$\overline{\text{INT1}}$ interrupt control register	INT1IC	$XXXXX000_2$
$005A_{16}$	$\overline{\text{INT3}}$ interrupt control register	INT3IC	$XXXXX000_2$
$005B_{16}$	Timer C interrupt control register	TCIC	$XXXXX000_2$
$005C_{16}$	Compare 0 interrupt control register	CMP0IC	$XXXXX000_2$
$005D_{16}$	$\overline{\text{INT0}}$ interrupt control register	INT0IC	$XX00X000_2$
$005E_{16}$			
$005F_{16}$			
0060_{16}			
0061_{16}			
0062_{16}			
0063_{16}			
0064_{16}			
0065_{16}			
0066_{16}			
0067_{16}			
0068_{16}			
0069_{16}			
$006A_{16}$			
$006B_{16}$			
$006C_{16}$			
$006D_{16}$			
$006E_{16}$			
$006F_{16}$			
0070_{16}			
0071_{16}			
0072_{16}			
0073_{16}			
0074_{16}			
0075_{16}			
0076_{16}			
0077_{16}			
0078_{16}			
0079_{16}			
$007A_{16}$			
$007B_{16}$			
$007C_{16}$			
$007D_{16}$			
$007E_{16}$			
$007F_{16}$			

X : Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080$_{16}$	Timer Y, Z mode register	TYZMR	00$_{16}$
0081$_{16}$	Prescaler Y register	PREY	FF$_{16}$
0082$_{16}$	Timer Y secondary register	TYSC	FF$_{16}$
0083$_{16}$	Timer Y primary register	TYPR	FF$_{16}$
0084$_{16}$	Timer Y, Z waveform output control register	PUM	00$_{16}$
0085$_{16}$	Prescaler Z register	PREZ	FF$_{16}$
0086$_{16}$	Timer Z secondary register	TZSC	FF$_{16}$
0087$_{16}$	Timer Z primary register	TZPR	FF$_{16}$
0088$_{16}$			
0089$_{16}$			
008A$_{16}$	Timer Y, Z output control register	TYZOC	00$_{16}$
008B$_{16}$	Timer X mode register	TXMR	00$_{16}$
008C$_{16}$	Prescaler X register	PREX	FF$_{16}$
008D$_{16}$	Timer X register	TX	FF$_{16}$
008E$_{16}$	Timer count source set register	TCSS	00$_{16}$
008F$_{16}$			
0090$_{16}$ 0091$_{16}$	Timer C register	TC	00$_{16}$ 00$_{16}$
0092$_{16}$			
0093$_{16}$			
0094$_{16}$			
0095$_{16}$			
0096$_{16}$	External input enable register	INTEN	00$_{16}$
0097$_{16}$			
0098$_{16}$	Key input enable register	KIEN	00$_{16}$
0099$_{16}$			
009A$_{16}$	Timer C control register 0	TCC0	00$_{16}$
009B$_{16}$	Timer C control register 1	TCC1	00$_{16}$
009C$_{16}$ 009D$_{16}$	Capture, compare 0 register	TM0	00$_{16}$ 00$_{16}$ (2)
009E$_{16}$ 009F$_{16}$	Compare 1 register	TM1	FF$_{16}$ FF$_{16}$
00A0$_{16}$	UART0 transmit/receive mode register	U0MR	00$_{16}$
00A1$_{16}$	UART0 bit rate register	U0BRG	XX$_{16}$
00A2$_{16}$ 00A3$_{16}$	UART0 transmit buffer register	U0TB	XX$_{16}$ XX$_{16}$
00A4$_{16}$	UART0 transmit/receive control register 0	U0C0	00001000$_2$
00A5$_{16}$	UART0 transmit/receive control register 1	U0C1	00000010$_2$
00A6$_{16}$ 00A7$_{16}$	UART0 receive buffer register	U0RB	XX$_{16}$ XX$_{16}$
00A8$_{16}$	UART1 transmit/receive mode register	U1MR	00$_{16}$
00A9$_{16}$	UART1 bit rate register	U1BRG	XX$_{16}$
00AA$_{16}$ 00AB$_{16}$	UART1 transmit buffer register	U1TB	XX$_{16}$ XX$_{16}$
00AC$_{16}$	UART1 transmit/receive control register 0	U1C0	00001000$_2$
00AD$_{16}$	UART1 transmit/receive control register 1	U1C1	00000010$_2$
00AE$_{16}$ 00AF$_{16}$	UART1 receive buffer register	U1RB	XX$_{16}$ XX$_{16}$
00B0$_{16}$	UART transmit/receive control register 2	UCON	00$_{16}$
00B1$_{16}$			
00B2$_{16}$			
00B3$_{16}$			
00B4$_{16}$			
00B5$_{16}$			
00B6$_{16}$			
00B7$_{16}$			
00B8$_{16}$			
00B9$_{16}$			
00BA$_{16}$			
00BB$_{16}$			
00BC$_{16}$			
00BD$_{16}$			
00BE$_{16}$			
00BF$_{16}$			

X : Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.
2. When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is set to “FFFF$_{16}$”.

Table 4.4 SFR Information(4)[1]

Address	Register	Symbol	After reset
00C0$_{16}$ 00C1$_{16}$	AD register	AD	XX$_{16}$ XX$_{16}$
00C2$_{16}$			
00C3$_{16}$			
00C4$_{16}$			
00C5$_{16}$			
00C6$_{16}$			
00C7$_{16}$			
00C8$_{16}$			
00C9$_{16}$			
00CA$_{16}$			
00CB$_{16}$			
00CC$_{16}$			
00CD$_{16}$			
00CE$_{16}$			
00CF$_{16}$			
00D0$_{16}$			
00D1$_{16}$			
00D2$_{16}$			
00D3$_{16}$			
00D4$_{16}$	AD control register 2	ADCON2	00$_{16}$
00D5$_{16}$			
00D6$_{16}$	AD control register 0	ADCON0	00000XXX$_{2}$
00D7$_{16}$	AD control register 1	ADCON1	00$_{16}$
00D8$_{16}$			
00D9$_{16}$			
00DA$_{16}$			
00DB$_{16}$			
00DC$_{16}$			
00DD$_{16}$			
00DE$_{16}$			
00DF$_{16}$			
00E0$_{16}$	Port P0 register	P0	XX$_{16}$
00E1$_{16}$	Port P1 register	P1	XX$_{16}$
00E2$_{16}$	Port P0 direction register	PD0	00$_{16}$
00E3$_{16}$	Port P1 direction register	PD1	00$_{16}$
00E4$_{16}$			
00E5$_{16}$	Port P3 register	P3	XX$_{16}$
00E6$_{16}$			
00E7$_{16}$	Port P3 direction register	PD3	00$_{16}$
00E8$_{16}$	Port P4 register	P4	XX$_{16}$
00E9$_{16}$			
00EA$_{16}$	Port P4 direction register	PD4	00$_{16}$
00EB$_{16}$			
00EC$_{16}$			
00ED$_{16}$			
00EE$_{16}$			
00EF$_{16}$			
00F0$_{16}$			
00F1$_{16}$			
00F2$_{16}$			
00F3$_{16}$			
00F4$_{16}$			
00F5$_{16}$			
00F6$_{16}$			
00F7$_{16}$			
00F8$_{16}$			
00F9$_{16}$			
03FA$_{16}$			
00FB$_{16}$			
00FC$_{16}$	Pull-up control register 0	PUR0	00XX0000$_{2}$
00FD$_{16}$	Pull-up control register 1	PUR1	XXXXXX0X$_{2}$
00FE$_{16}$	Port P1 drive capacity control register	DRR	00$_{16}$
00FF$_{16}$	Timer C output control register	TCOUT	00$_{16}$
01B3$_{16}$	Flash memory control register 4	FMR4	01000000$_{2}$
01B4$_{16}$			
01B5$_{16}$	Flash memory control register 1	FMR1	0100XX0X$_{2}$
01B6$_{16}$			
01B7$_{16}$	Flash memory control register 0	FMR0	00000001$_{2}$

X : Undefined

NOTES:

1. Blank columns, 0100$_{16}$ to 01B2$_{16}$ and 01B8$_{16}$ to 02FF$_{16}$ are all reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	—	5.5	V
AVcc	Analog supply voltage			—	V_{CC}(3)	—	V
Vss	Supply voltage			—	0	—	V
AVss	Analog supply voltage			—	0	—	V
V_{IH}	"H" input voltage			0.8V_{CC}	—	V_{CC}	V
V_{IL}	"L" input voltage			0	—	0.2V_{CC}	V
$I_{OH\ (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		—	—	-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current			—	—	-10.0	mA
$I_{OH\ (avg)}$	"H" average output current			—	—	-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		—	—	60	mA
$I_{OL\ (peak)}$	"L" peak output current	Except $P1_0$ to $P1_7$		—	—	10	mA
		$P1_0$ to $P1_7$	Drive capacity HIGH	—	—	30	mA
			Drive capacity LOW	—	—	10	mA
$I_{OL\ (avg)}$	"L" average output current	Except $P1_0$ to $P1_7$		—	—	5	mA
		$P1_0$ to $P1_7$	Drive capacity HIGH	—	—	15	mA
			Drive capacity LOW	—	—	5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0	—	20	MHz
			2.7V ≤ Vcc < 3.0V	0	—	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold Vcc=AVcc.

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = V_{CC}	—	—	10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)	—	—	±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)		—	±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=V_{CC}	10	—	40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3	—	—	µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8	—	—	µs
V_{REF}	Reference voltage			—	V_{CC}(4)	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
–	A/D operating clock frequency(2)	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:
1. V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f_{AD} exceeds 10 MHz more, divide the f_{AD} and hold A/D operating clock frequency ($\varnothing_{AD}$) 10 MHz or below.
3. If the AVcc is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency ($\varnothing_{AD}$) f_{AD}/2 or below.
4. Hold Vcc=Vref.

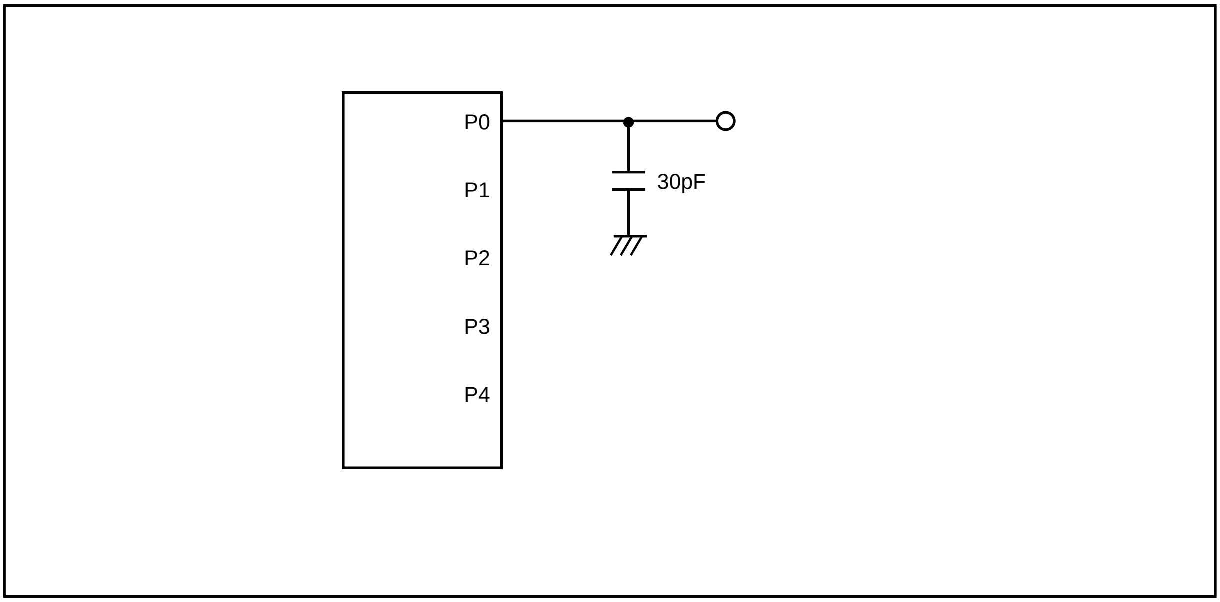


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory Version Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/erase endurance		100	—	—	times
–	Byte program time		—	50	400	µs
–	Block erase time		—	0.4	9	s
td(SR-ES)	Time delay from suspend request until erase suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase voltage		2.7	—	5.5	V
–	Read voltage		2.7	—	5.5	V
–	Program, Erase temperature		0	—	60	°C
–	Data hold time(2)	Ambient temperature=55 °C	20	—	—	year

NOTES:
1. Referenced to VCC1=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.
2. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
—	Voltage detection interrupt request generating time(2)		—	40	—	µs
—	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V	—	600	—	nA
td(E-A)	Waiting time till voltage detection circuit operation starts(3)		—	—	20	µs
Vccmin	Minimum value of microcomputer operation voltage		2.7	—	—	V

NOTES:
1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr= -40°C to 85 °C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to “0”.

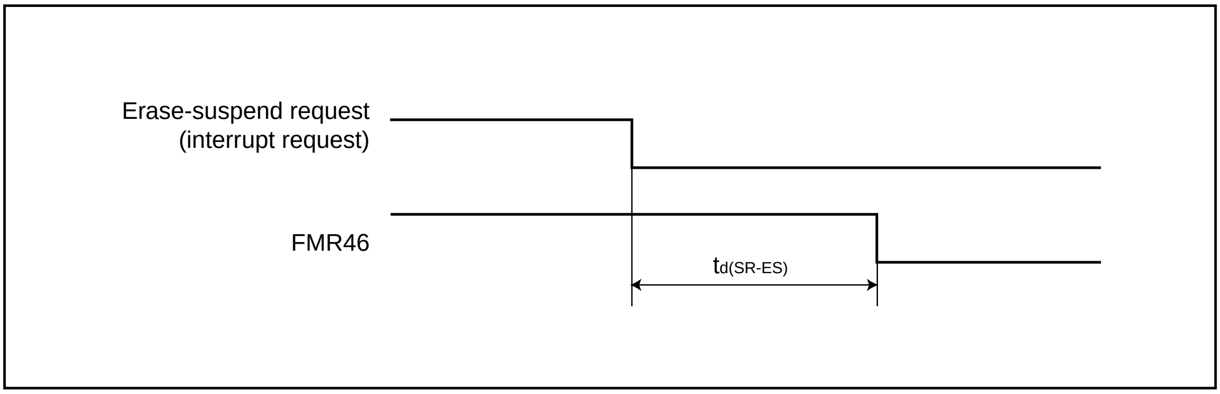


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2(1, 3))

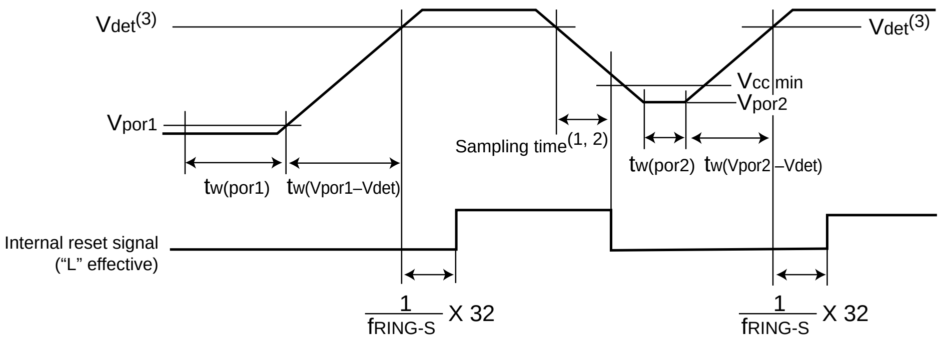
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage	–20°C ≤ Topr < 85°C	—	—	Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled(2)	–20°C ≤ Topr < 85°C, tw(por2) ≥ 0s(4)	—	—	100	ms

NOTES:
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual for details.
2. This condition is not applicable when using with Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage (Vpor1) for greater than 10 seconds, refer to Table 5.7 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.7 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage	–20°C ≤ Topr < 85°C	—	—	0.1	V
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s(2)	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	–20°C ≤ Topr < 0°C, tw(por1) ≥ 30s(2)	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	–20°C ≤ Topr < 0°C, tw(por1) ≥ 10s(2)	—	—	1	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s(2)	—	—	0.5	ms

NOTES:
1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock is selectable. Refer to "5.4 Voltage Detection Circuit" of Hardware Manual for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to "5.4 Voltage Detection Circuit" for details.
4. Refer to "Table 16.6 Reset Circuit Electrical Characteristics" for electrical characteristics.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.8 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released	VCC=5.0V, Topr=25 °C Set "40_{16}" in the HR1 register	6	8	10	MHz
td(HRoffset)	Settable high-speed on-chip oscillator minimum period	VCC=5.0V, Topr=25 °C Set "00_{16}" in the HR1 register	—	61	—	ns
td(HR)	High-speed on-chip oscillator period adjusted unit	Differences when setting "01_{16}" and "00_{16}" in the HR register	—	1	—	ns
—	High-speed on-chip oscillator frequency temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C	—	±5	—	%
—	High-speed on-chip oscillator frequency temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 85 °C	—	±10	—	%

NOTES:
1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.9 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on(2)		1	—	2000	µs
td(R-S)	STOP release time(3)		—	—	150	µs

NOTES:
1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2. This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.10 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		V_{CC}-2.0	—	V_{CC}	V
			I_{OH}=-200µA		V_{CC}-0.3	—	V_{CC}	V
		X_{OUT}	Drive ability HIGH	I_{OH}=-1 mA	V_{CC}-2.0	—	V_{CC}	V
			Drive ability LOW	I_{OH}=-500µA	V_{CC}-2.0	—	V_{CC}	V
V_{OL}	"L" output voltage	Except $P1_0$ to $P1_7$, X_{OUT}	I_{OL}= 5 mA		—	—	2.0	V
			I_{OL}= 200 µA		—	—	0.45	V
		$P1_0$ to $P1_7$	Drive capacity HIGH	I_{OL}= 15 mA		—	2.0	V
			Drive capacity LOW	I_{OL}= 5 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 200 µA	—	—	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 1 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}=500 µA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{\text{INT}_0}$, $\overline{\text{INT}_1}$, $\overline{\text{INT}_2}$, $\overline{\text{INT}_3}$, $\overline{\text{KI}_0}$, $\overline{\text{KI}_1}$, $\overline{\text{KI}_2}$, $\overline{\text{KI}_3}$, CNTR_0, CNTR_1, TC_{IN}, RxD_0, RxD_1, $P4_5$			0.2	—	1.0	V
		$\overline{\text{RESET}}$			0.2	—	2.2	V
I_{IH}	"H" input current		V_I=5V		—	—	5.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	1.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:
1. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.11 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	9	15	mA
			X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	8	14	mA
			X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	4	—	mA
			X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	3	—	mA
			X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	2	—	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	4	8	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.5	—	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	470	900	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation VC27="0"	—	40	80	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off VC27="0"	—	38	76	µA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"	—	0.8	3.0	µA

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at Topr = 25 °C) [V_{CC}=5V]

Table 5.12 X_{IN} input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C}(X_{IN})$	X_{IN} input cycle time	50	–	ns
$t_{WH}(X_{IN})$	X_{IN} input HIGH pulse width	25	–	ns
$t_{WL}(X_{IN})$	X_{IN} input LOW pulse width	25	–	ns

Table 5.13 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C}(CNTR0)$	CNTR0 input cycle time	100	–	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	40	–	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	40	–	ns

Table 5.14 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C}(TCIN)$	TCIN input cycle time	400(1)	–	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	200(2)	–	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	200(2)	–	ns

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.15 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C}(CK)$	CLKi input cycle time	200	–	ns
$t_{W}(CKH)$	CLKi input HIGH pulse width	100	–	ns
$t_{W}(CKL)$	CLKi input LOW pulse width	100	–	ns
$t_{d}(C-Q)$	TxDi output delay time	–	80	ns
$t_{h}(C-Q)$	TxDi hold time	0	–	ns
$t_{su}(D-C)$	RxDi input setup time	35	–	ns
$t_{h}(C-D)$	RxDi input hold time	90	–	ns

Table 5.16 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W}(INH)$	$\overline{\text{INT0}}$ input HIGH pulse width	250(1)	–	ns
$t_{W}(INL)$	$\overline{\text{INT0}}$ input LOW pulse width	250(2)	–	ns

NOTES:

1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

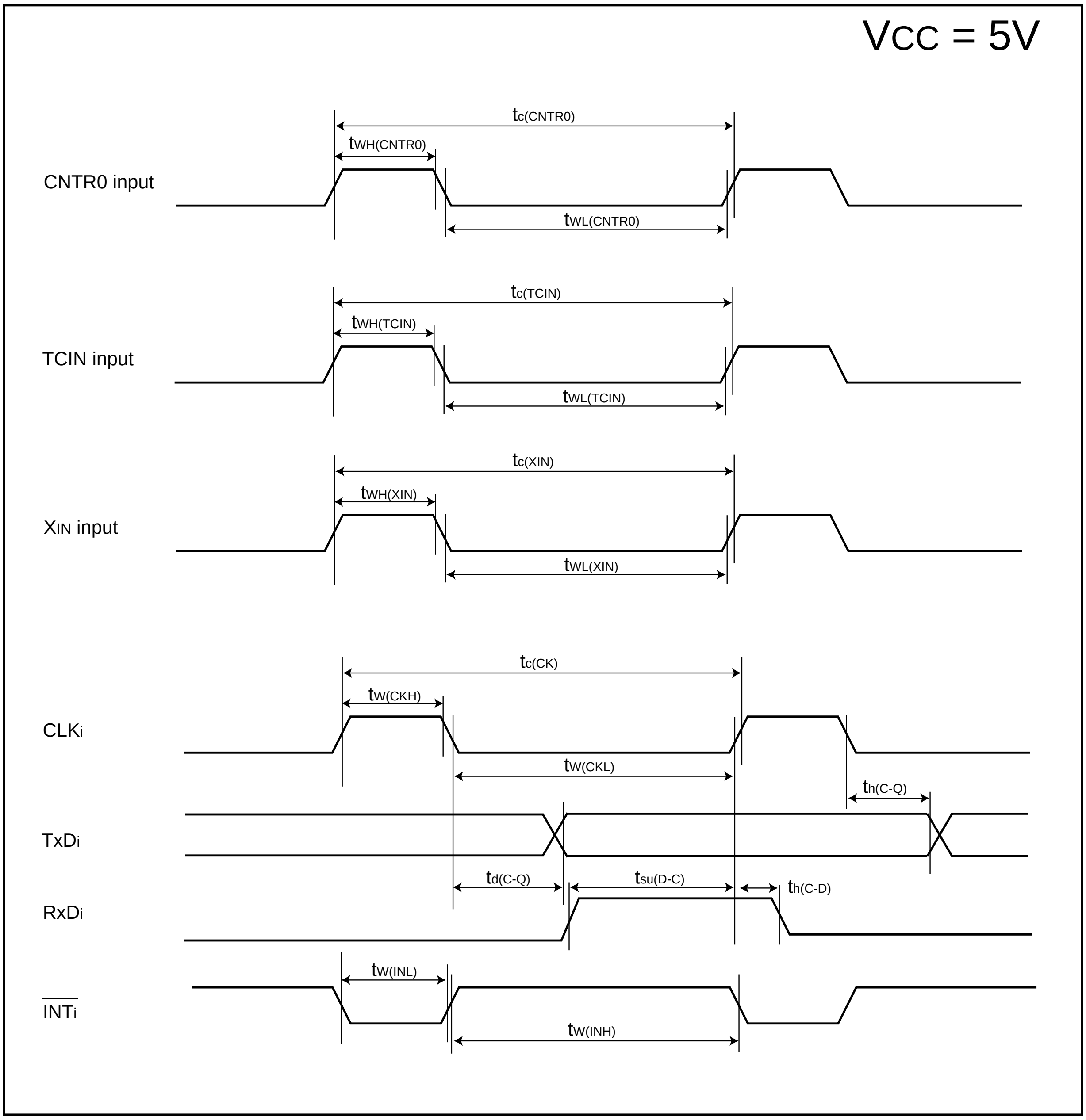


Figure 5.4 Vcc=5V timing diagram

Table 5.17 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		V_{CC}-0.5	—	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-0.1 mA	V_{CC}-0.5	—	V_{CC}	V
			Drive capacity LOW	I_{OH}=-50 µA	V_{CC}-0.5	—	V_{CC}	V
V_{OL}	"L" output voltage	Except $P1_0$ to $P1_7$, X_{OUT}	I_{OL}= 1 mA		—	—	0.5	V
		$P1_0$ to $P1_7$	Drive capacity HIGH	I_{OL}= 2 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}= 1 mA	—	—	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}=50 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $CNTR_0$, $CNTR_1$, TC_{IN}, RxD_0, RxD_1, $P4_5$			0.2	—	0.8	V
		$\overline{RESET}$			0.2	—	1.8	V
I_{IH}	"H" input current		V_I=3V		—	—	4.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	3.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:

1. Referenced to V_{CC} = AV_{CC} = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Table 5.18 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	8	13	mA
			X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	7	12	mA
			X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	3	—	mA
			X_{IN}=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
			X_{IN}=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8	—	1.5	—	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8	—	420	800	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation VC27="0"	—	37	74	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off VC27="0"	—	35	70	µA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"	—	0.7	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: V_{CC} = 3V, V_{SS} = 0V at Topr = 25 °C) [V_{CC}=3V]

Table 5.19 X_{IN} input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XIN)}$	X_{IN} input cycle time	100	–	ns
$t_{WH(XIN)}$	X_{IN} input HIGH pulse width	40	–	ns
$t_{WL(XIN)}$	X_{IN} input LOW pulse width	40	–	ns

Table 5.20 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CNTR0)}$	CNTR0 input cycle time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 input HIGH pulse width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 input LOW pulse width	120	–	ns

Table 5.21 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TCIN)}$	TCIN input cycle time	1200(1)	–	ns
$t_{WH(TCIN)}$	TCIN input HIGH pulse width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN input LOW pulse width	600(2)	–	ns

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input HIGH pulse width	150	–	ns
$t_{W(CKL)}$	CLKi input LOW pulse width	150	–	ns
$t_{d(C-Q)}$	TxDi output delay time	–	160	ns
$t_{h(C-Q)}$	TxDi hold time	0	–	ns
$t_{su(D-C)}$	RxDi input setup time	55	–	ns
$t_{h(C-D)}$	RxDi input hold time	90	–	ns

Table 5.23 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input HIGH pulse width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input LOW pulse width	380(2)	–	ns

NOTES:

1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

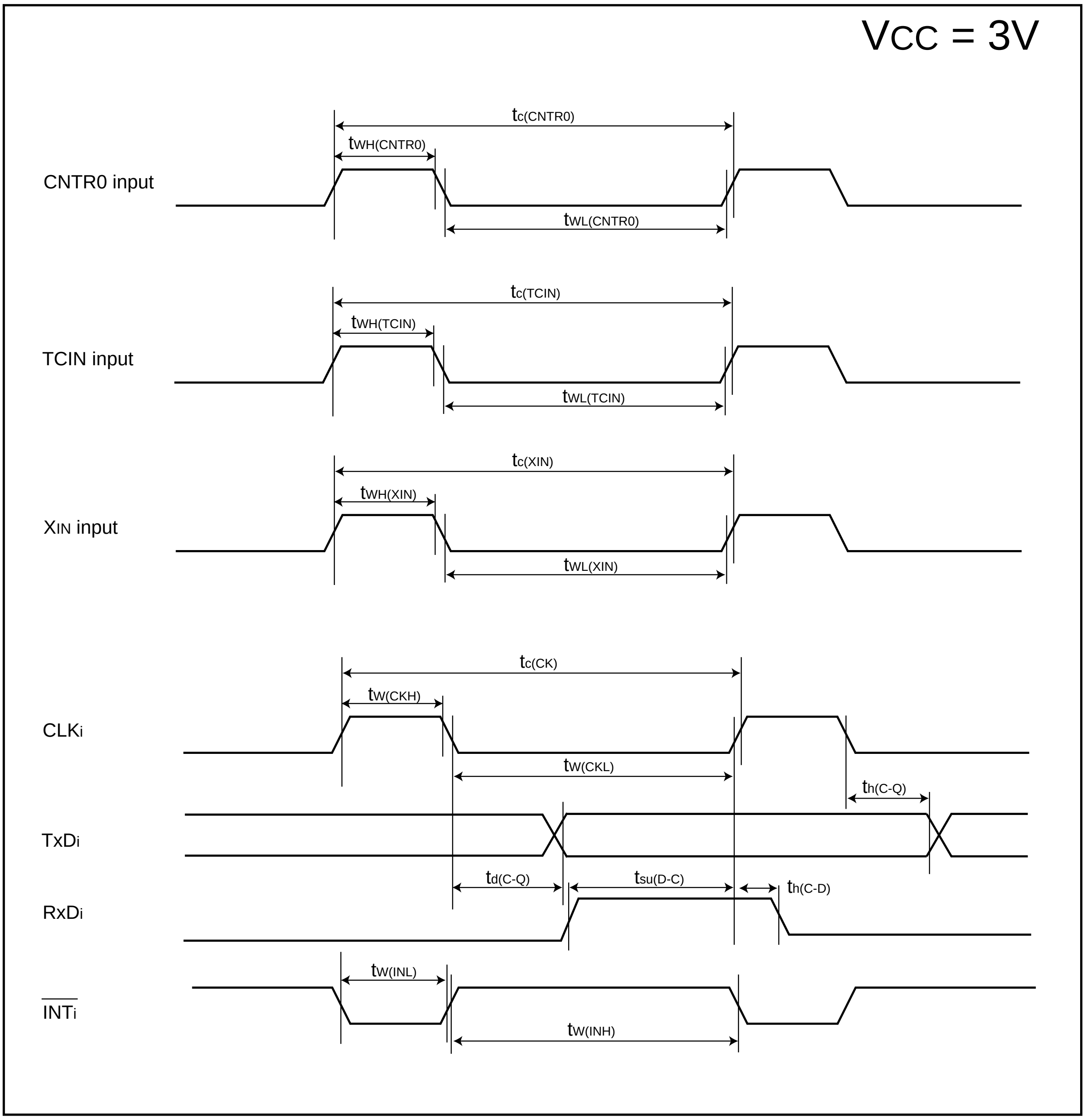
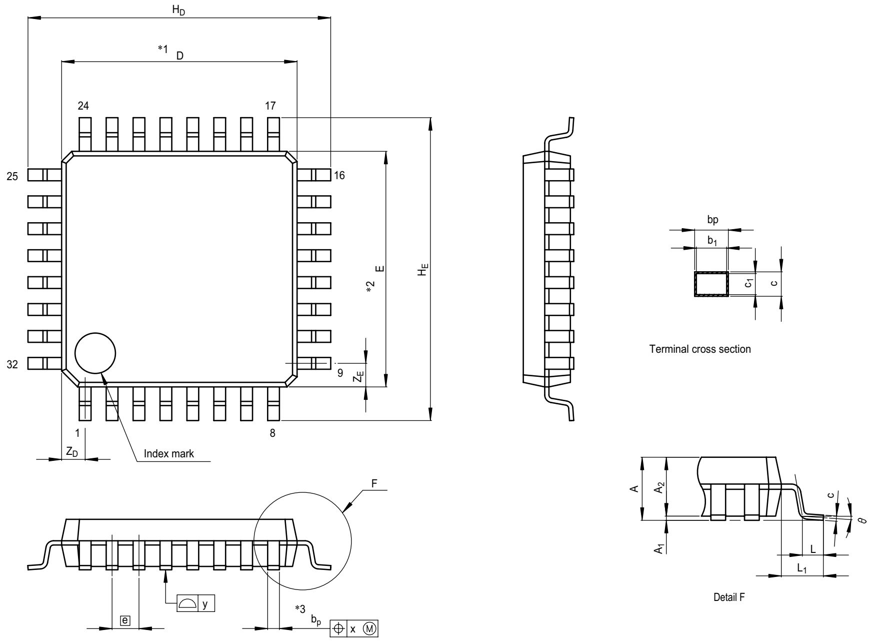


Figure 5.5 Vcc=3V timing diagram

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
$\boxed{e}$	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	R8C/11 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2	Table 1.1: Shortest instruction execution time and f(X_{IN}) changed
		5	Figure 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR_0}$
		6	Table 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR_0}$
		10	The value of HR1 register after reset changed
		12	The value of TC register after reset changed
		14	Chapter “5. Electrical Characteristics” added
1.20	Oct. 31, 2003	2	Table 1.1: Power consumption values added
		6	Table 1.3: Resistor value for CNVss and MODE deleted
		11	Register name of address 0050_{16} modified from CMP2IC to CMP1IC, register name of address $005C_{16}$ modified from CMP1IC to CMP0IC
		14	Table 5.2: Note 3 and Note 4 deleted
		15	t_{samp} in Table 5.3 deleted
		17	Figure 5.1 added
		19	Table 5.10: Vcc changed from “4.2 to 5.5V” to “3.3V to 5.5V”, low-power on-chip oscillator changed from “on 100kHz” to “125kHz”, X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, VC27=”0” added in stop mode measuring condition, data added and modified
		20	Table 11 to Table 15 added
		21	Figure 5.2 added
		22	Table 5.16: Note 1, $f_{(BCLK)}$=5 MHz changed to 10 MHz
		23	Table 5.17: low-power ring oscillator changed from “on 100kHz” to “125kHz”, X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, VC27=”0” added in stop mode measuring condition, data added and modified
		24	Table 5.18 to Table 5.22 added
		25	Figure 5.3 added
1.30	Dec 05, 2003	4	Table 1.2 : ** deleted
		15	Table 5.4 revised
1.40	Sep 30, 2004	all pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Title of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 revised ; Table 16.5 revised
		17	Table 5.6, 5.7 adn 5.8 revised ; Figure 5.3 revised
		18	Table 5.9 revised ; Table 5.10 revised

Rev.	Date	Description	
		Page	Summary
1.40	Sep 30, 2004	20	Table 5.12 revised ; Table 5.16 revised
		22	Table 16.17 revised
		24	Table 16.19 revised
1.50	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		15	Table 5.3 partly revised
		16	Table 5.4 partly added
		17	Table 5.6, Table 5.7 revised
		18	Table 5.9, Table 10 partly revised
		22	Table 5.17 partly revised
		26	Package Dimensions revised
1.60	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2 “Product List” → “Product Informaton” revised Figure 1.2 Type No., Memory Size, and Package partly revised
		6	Table 1.3 Pin description revised
		7-8	2 Central Processing Unit (CPU) revised Figure 2.1 CPU register revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised
		11	Table 4.2 SFR Information(2) NOTES:1 revised
		12	Table 4.3 SFR Information(3); 0081_{16}: “Prescaler Y” → “Prescaler Y Register” 0082_{16}: “Timer Y Secondary” → “Timer Y Secondary Register” 0083_{16}: “Timer Y Primary” → “Timer Y Primary Register” 0085_{16}: “Prescaler Z” → “Prescaler Z Register” 0086_{16}: “Timer Z Secondary” → “Timer Z Secondary Register” 0087_{16}: “Timer Z Primary” → “Timer Z Primary Register” $008C_{16}$: “Prescaler X” → “Prescaler X Register” revised NOTES:1, 2 revised
		13	Table 4.4 SFR Information(4) NOTES:1 revised
		14	Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised
		15	Table 5.3 A/D Conversion Characteristics; “A/D operation clock frequency” → “A/D operating clock frequency” revised NOTES: 1, 2, 3, 4 revised
		16	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; “Topr” → “Ambient temperature” revised Measuring condition of byte program time and block erase time deleted
		17	Table 5.6 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2) NOTES: 3 revised
		18	Table 5.8 High-speed On-Chip Oscillator Circuit Electrical Characteristics; “High-speed on-chip oscillator temperature dependence” → “High-speed on-chip oscillator frequency temperature dependence” revised Table 5.10 Electrical Characteristics (1) [V_{CC}=5V]; “$P1_0$ to $P1_7$ Except X_{OUT}” → “Except $P1_0$ to $P1_7$, X_{OUT}” revised

Rev.	Date	Description	
		Page	Summary
1.60	Jan.27.2006	19	Table 5.11 Electrical Characteristics (2) [V_{CC}=5V] NOTES: 1, 2 revised Measuring condition Stop mode: “Topr = 25 °C”
		22	Table 5.17 Electrical Characteristics (3) [V_{CC}=3V] “$P1_0$ to $P1_7$ Except X_{OUT}” → “Except $P1_0$ to $P1_7$, X_{OUT}” revised
		23	Table 5.18 Electrical Characteristics (4) [V_{CC}=3V] NOTES: 1, 2 revised Measuring condition Stop mode: “Topr = 25 °C”

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