PRELIMINARY

# Switching Driver with Regulator for Class-D Headphone Amplifier

## ■ GENERAL DESCRIPTION

The **NJU8715** is a switching driver with regulator for class-D headphone amplifier. It incorporates an optimum regulator for the driver of headphone amplifier, class–D line amplifier and a beep amplifier. The **NJU8715** converts 1bit digital signal of the PWM or the PDM to an analog signal output through a simple external LC low-pass filter.

The **NJU8715** provides a completed digital system and high power-efficiency with class-D operation. Therefore, it is suitable for portable audio applications.

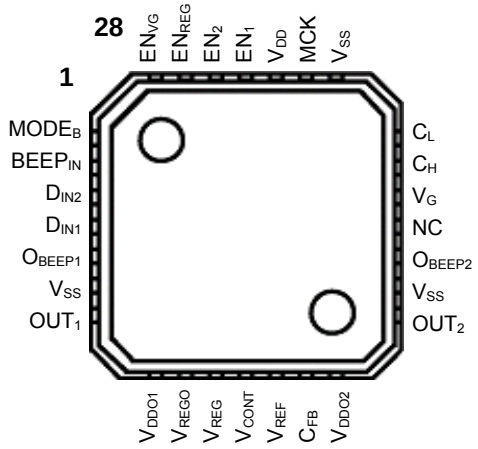
## ■ PACKAGE OUTLINE

**NJU8715KN1**

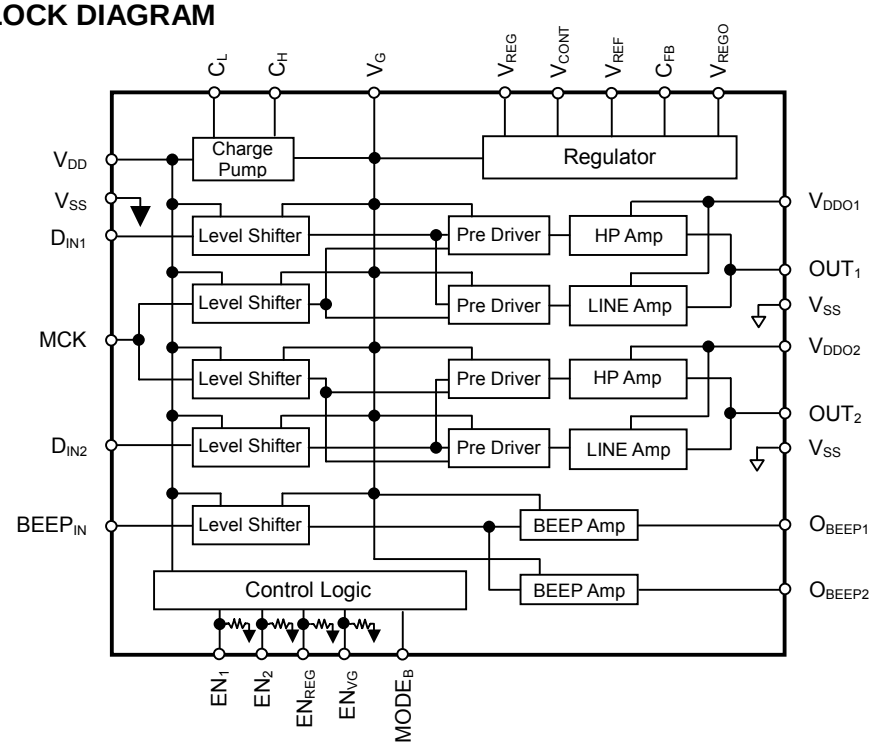
## ■ FEATURES

- 2-channel 1bit Audio Signal Input
- Headphone Output
- Built-in Class D Line Amplifier
- Built-in Regulator for Driver
- Beep Function
- Logic Operating Voltage 1.9 to 2.6V ($V_{DD}$)
- Regulator Operating Voltage 4.0 to 5.75V ($V_G$)
  1.9 to 4.0V ($V_{REG}$)
- C-MOS Technology
- Package Outline QFN28

## ■ PIN CONFIGURATION




## ■ BLOCK DIAGRAM



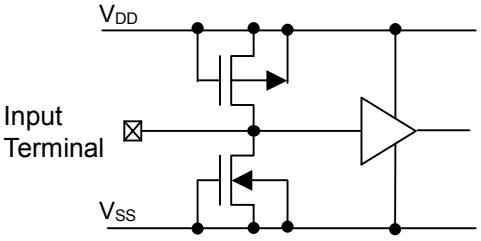
## ■ TERMINAL DESCRIPTION

| No. | SYMBOL | I/O | Function |
|---|---|---|---|
| 1 | $MODE_B$ | I | BEEP Output Level Control Terminal<br>H: -39dBm, L: -48dBm  The load of 16Ω (Note.1) |
| 2 | $BEEP_{IN}$ | I | BEEP Signal Input Terminal |
| 3 | $D_{IN2}$ | I | Audio Signal Input Terminal 2 |
| 4 | $D_{IN1}$ | I | Audio Signal Input Terminal 1 |
| 5 | $O_{BEEP1}$ | O | BEEP Output Terminal 1 |
| 6, 16, 22 | $V_{SS}$ | - | Power GND: $V_{SS}$=0V (Note.2) |
| 7 | $OUT_1$ | O | Output Terminal 1<br>This terminal outputs $D_{IN1}$ terminal input data. |
| 8 | $V_{DDO1}$ | - | Driving Power Supply 1 |
| 9 | $V_{REGO}$ | O | Regulator Output Terminal |
| 10 | $V_{REG}$ | I | Regulator Input Terminal |
| 11 | $V_{CONT}$ | I | Regulator Output Voltage Control Terminal |
| 12 | $V_{REF}$ | O | Reference Voltage Output Terminal |
| 13 | $C_{FB}$ | I | Regulator Output Voltage Sense Terminal |
| 14 | $V_{DDO2}$ | - | Driving Power Supply 2 |
| 15 | $OUT_2$ | O | Output Terminal 2<br>This terminal outputs $D_{IN2}$ terminal input data. |
| 17 | $O_{BEEP2}$ | O | BEEP Output Terminal 2 |
| 18 | NC | - | Non connection |
| 19 | $V_G$ | - | Pre-driver Power supply |
| 20 | $C_H$ | - | + Capacitor Connection Terminal for the charge pump |
| 21 | $C_L$ | - | - Capacitor Connection Terminal for the charge pump |
| 23 | MCK | I | Master Clock Input Terminal<br>The condition of the data input terminal is latched on the rising edge of this signal. |
| 24 | $V_{DD}$ | - | Operation Power Supply |
| 25 | $EN_1$ | I | HP/LINE/BEEP Mode Control Terminal 1 (with pull-down resistor) |
| 26 | $EN_2$ | I | HP/LINE/BEEP Mode Control Terminal 2 (with pull-down resistor) |
| 27 | $EN_{REG}$ | I | Regulator Enable Terminal (with pull-down resistor)<br>H : ON,  L : OFF |
| 28 | $EN_{VG}$ | I | Charging pump Enable Terminal (with pull-down resistor)<br>H : ON,  L : OFF |

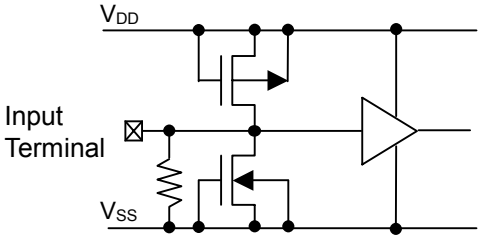
Note.1) 0dBm≅0.775Vrms
Note.2) $V_{SS}$(Terminal No.6,16,22) should be connected at the nearest point to the IC.

## ■ INPUT TERMINAL STRUCTURE

MCK, $D_{IN1}$, $D_{IN2}$, $BEEP_{IN}$, $MODE_B$ Terminal




$EN_1$, $EN_2$, $EN_{REG}$, $EN_{VG}$ Terminal



## ■ FUNCTIONAL DESCRIPTION

(1) Power Supply

$V_{DD}$ : Power supply for input circuit and control logic. Keep the input logic level less than $V_{DD}$.

$V_G$ : Power supply for pre-driver which drives the transistor gates of output drivers.
When ENVG=H, charge pump generates double the voltage of $V_{DD}$, which is supplied to $V_G$ terminal through the inside.
When ENVG=L, charge pump is halted, and $V_G$ terminal accepts the external power supply.

$V_{REG}$ : Power supply for built-in regulator. Apply the required voltage with additional dropout voltage of regulator. By connecting $V_{REGO}$ (regulator output) to $V_{DDO1}$, $V_{DDO2}$ (Driver power supply), the power is provided to the drivers. Furthermore, the regulator output should be supplied to $V_{DDO1}$ and $V_{DDO2}$ by connecting de-coupling capacitor to get highly smoothed power supply.

(2) Regulator Output Voltage Control Terminal ($V_{CONT}$)

$V_{CONT}$ is the control terminal for regulator output voltage. As $V_{REG}$ output voltage is variable from 0V by external DC voltage, driver output level can be used as sound volume.

(3) Regulator Enable Signal ($EN_{REG}$)

The regulator is halted at “L” level, and works at “H” level.

(4) Charging pump Enable Signal ($EN_{VG}$)

The charge pump is halted at “L” level, and works at “H” level.

(5) HP/LINE/BEEP Mode Control Terminal ($EN_1$ / $EN_2$)

Each mode can be selected by a combination setting of $EN_1$ and $EN_2$.
The following table shows each output condition of each mode.

| Mode | Input | | Output | | |
|---|---|---|---|---|---|
| | $EN_1$ | $EN_2$ | HP Amp. | LINE Amp. | BEEP Amp. |
| Standby Mode | L | L | HiZ | HiZ | HiZ |
| LINE Mode | L | H | HiZ | Active | HiZ |
| HP Mode | H | L | Active | HiZ | HiZ |
| BEEP Mode | H | H | HiZ | HiZ | Active |

(6) BEEP Signal Input ($BEEP_{IN}$)

(7) BEEP Signal Output ($O_{BEEP1}$ / $O_{BEEP2}$)

BEEP signal is output in a square wave.

(8) Master Clock (MCK)

Master clock (MCK) synchronizes the audio signal inputs($D_{IN1}$, $D_{IN2}$). The setup time and the hold time should be kept in the AC characteristics because $D_{IN1}$ and $D_{IN2}$ are latched on the rising edge of MCK. During the standby condition, MCK requires “L” level to avoid unnecessary power consumption. In addition, MCK requires jitter-free or fewer jitter because the jitter could lead to poor S/N ratio.

(9) Signal output ($OUT_1$ / $OUT_2$)

$OUT_1$ and $OUT_2$ terminals keep the Hi-z condition if output voltage of $V_{REGO}$ is lower than detection voltage. Output signals are appeared as PWM signals through the use of $V_{DDO1}$ and $V_{DDO2}$ in the $OUT_1$ and $OUT_2$ terminals If the output voltage is over than detection voltage. Output signals will be converted to analog signals via 2nd-order or higher LC filter.

## ■ POWER ON/DOWN SEQUENCE

The pop-noise can be effectively suppressed with the following sequence when power ON and DOWN.

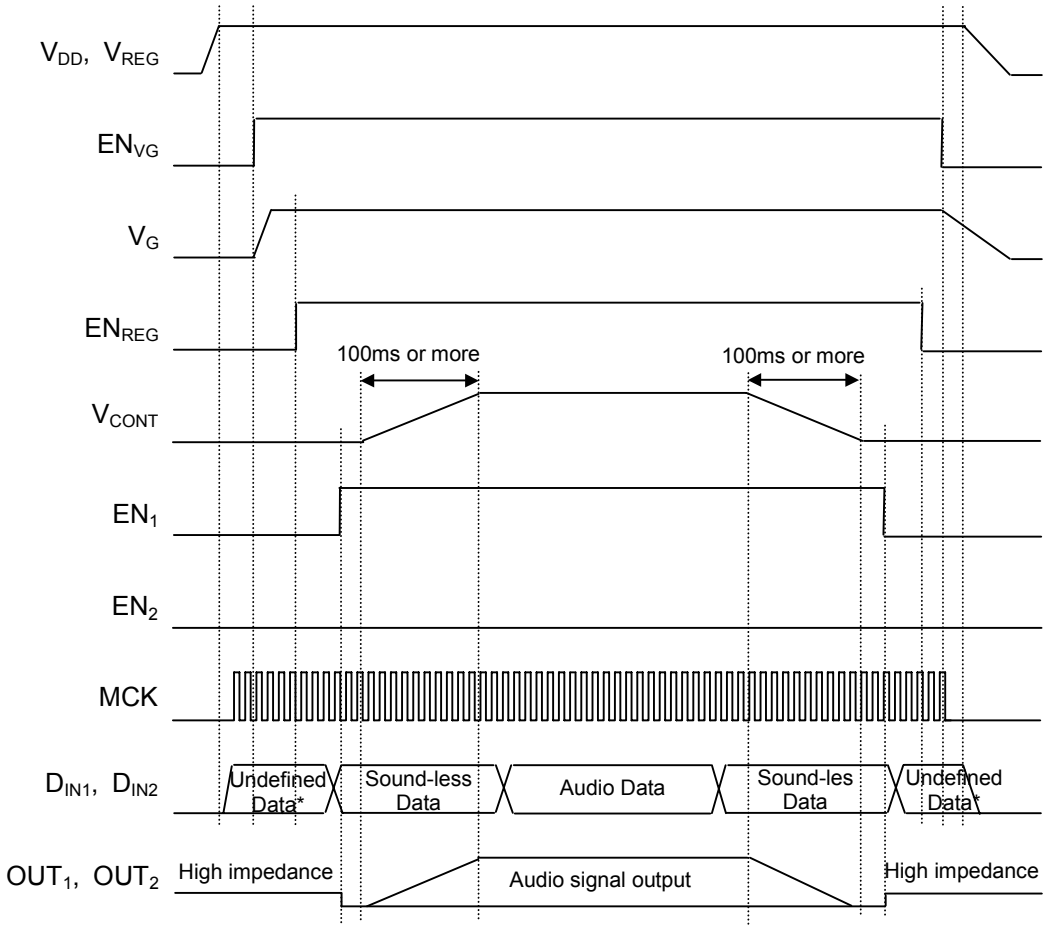
(1) Power ON / Power DOWN Sequence ($EN_{VG}$=H: Using internal $V_G$)

< Power On sequence >

1) Input the MCK after the start-up of $V_{DD}$. After of 100ms delay or more from MCK input, set $EN_{VG}$ at "H" level.
2) Set $EN_{SEG}$ at "H" level after 5ms delay or more.(at 0.1μF for the charge pump and 1μF for the smoothing capacitor)
3) After setting $EN_{REG}$ at "H" level, input audio signals($D_{IN1}$, $D_{IN2}$).
4) Set $EN_1$ at "H" level and $EN_2$ at "L" level after audio signal input. The audio signal input must be "Sound-less data" until $V_{CONT}$ reaches a steady state.
5) $V_{CONT}$ should be applied gradually to the target voltage. If the rising time of the application to the target $V_{CONT}$ voltage is short, it may cause a pop-noise.

< Power Down sequence >

The sequence must be executed in inverse order of the power ON sequence.




* : Do not set $D_{IN1}$ and $D_{IN2}$ at "H" level before the start-up of $V_{DD}$.

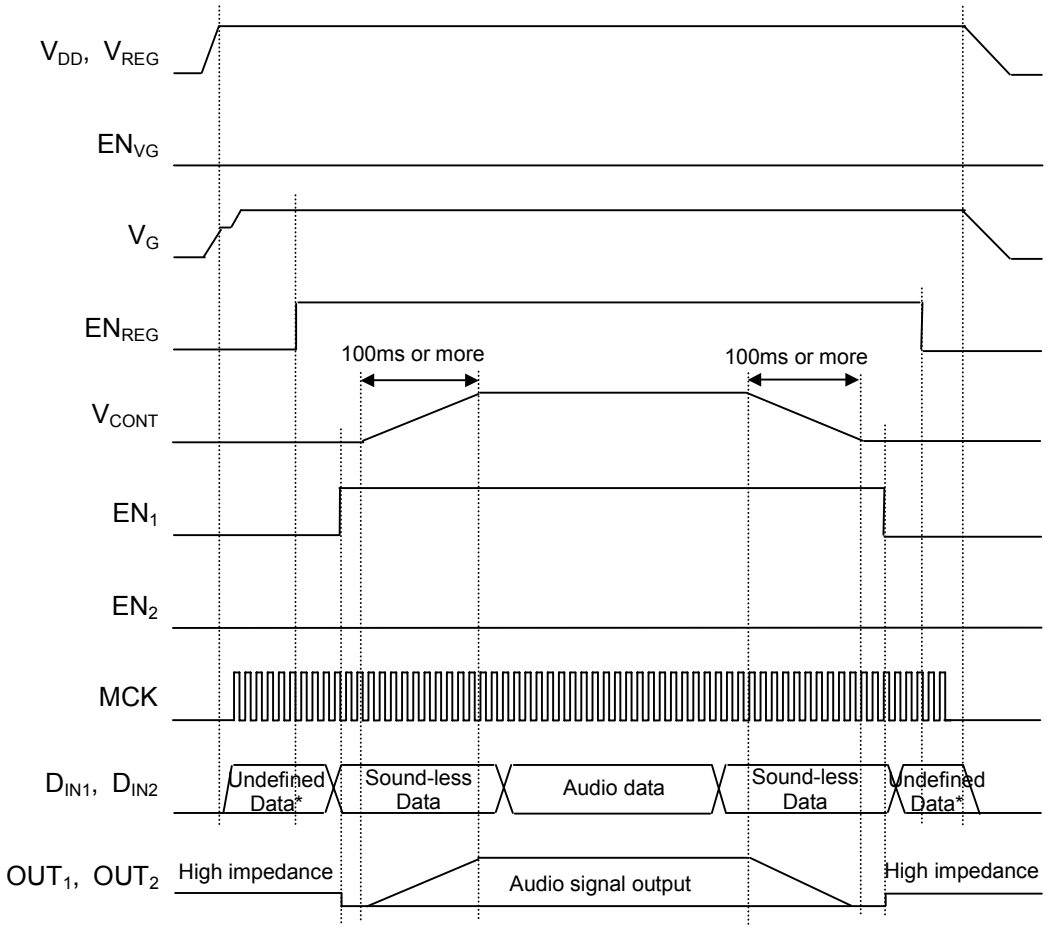
(2)Power ON / Power DOWN Sequence($EN_{VG}$=L, $V_G$: Externally applied)

< Power ON sequence >

1) Input the MCK after the start-up of $V_{DD}$.
   Apply $V_G$ after the start-up $V_{DD}$.(As shown in the following sequence, $V_G$ increases to $V_{DD}$ through a internal protection diode after $V_{DD}$ is turned on.)
2) Set $EN_{REG}$ at "H" level after the start-up of $V_G$.
3) After setting $EN_{REG}$ at "H" level, input audio signals($D_{IN1}$, $D_{IN2}$).
4) Set $EN_1$ at "H" level and $EN_2$ at "L" level after audio signal input. The audio signal input must be "Sound-less data" until $V_{CONT}$ reaches a steady state.
5) $V_{CONT}$ should be applied gradually to the target voltage. If the rising time of the application to the target $V_{CONT}$ voltage is short, it may cause a pop-noise.

< Power DOWN sequence >

The sequence must be executed in inverse order of the power ON sequence.




* : Do not set $D_{IN1}$ and $D_{IN2}$ at "H" level before the start-up of $V_{DD}$.

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.3 ~ +2.75 | V |
| | $V_{REG}$ | -0.3 ~ +5.5 | V |
| | $V_G$ | $V_{DD}$ ~ +6.0 | V |
| Input Voltage | Vin | -0.3 ~ $V_{DD}$+0.3 | V |
| Operating Temperature | Ta | -20 ~ +85 | °C |
| Storage Temperature | Tstg | -40 ~ +125 | °C |
| Power Dissipation | $P_D$ | 640 | mW |

Note.3) The relations of $V_{DDO1}$,$V_{DDO2}$<$V_G$, $V_{REG}$<$V_G$ and $V_{DD}$<$V_G$ must be maintained during operations.
Note.4) All voltage values are specified as $V_{SS}$=$V_{SSO}$=0V.
Note.5) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.
Note.6) De-coupling capacitors for "$V_{DD}$-$V_{SS}$", "$V_{DDO1}$-$V_{SSO}$" and "$V_{DDO2}$-$V_{SS}$" should be connected for stable operation.

## ■ ELECTRICAL CHARACTERISTICS

(1) DC CHARACTERISTICS

($Ta=25°C$, $V_{DD}=2.0V$, $V_{DDO1}=V_{DDO2}=1.7V$, $V_{REG}=2.15V$, $V_{SS}=V_{SSO}=0.0V$, Load Impedance=16Ω, $f_S=44.1kHz$, unless otherwise noted)

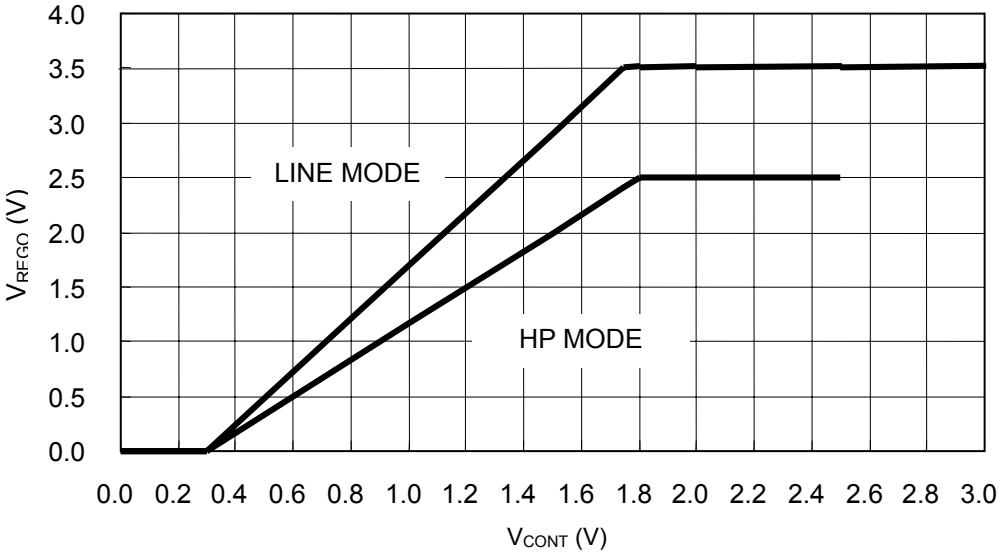
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ Supply Voltage | $V_{DD}$ | | 1.9 | 2.0 | 2.6 | V |
| $V_G$ Supply Voltage | $V_G$ | $V_G$: Externally applied | 4.0 | 5.0 | 5.75 | V |
| HP Driver High side Resistance | $R_{HPH}$ | $OUT_{1,2}=V_{DDO1,2}-0.1V$ | - | 1.2 | 2 | Ω |
| HP Driver Low side Resistance | $R_{HPL}$ | $OUT_{1,2}=0.1V$ | - | 1.2 | 2 | Ω |
| Line Driver High side Resistance | $R_{LINEH}$ | $OUT_{1,2}=V_{DDO1,2}-0.1V$<br>$V_{DDO1,2}=2.75V$ | 7.7 | 11 | 14.3 | Ω |
| Line Driver Low side Resistance | $R_{LINEL}$ | $OUT_{1,2}=0.1V$<br>$V_{DDO1,2}=2.75V$ | 7.7 | 11 | 14.3 | Ω |
| BEEP Output Voltage | $V_{BEEPL}$ | $MODE_B$=L | -50 (2.45) | -48 (3.08) | -46 (3.88) | dBm (mVrms) |
| | $V_{BEEPH}$ | $MODE_B$=H | -41 (6.91) | -39 (8.70) | -37 (10.95) | |
| Power Supply Current At Standby | $I_{ST}$ | Standby Mode<br>Stopping<br>MCK,$D_{IN1}$,$D_{IN2}$,$BEEP_{IN}$<br>$EN_{REG}$=L | - | - | 1 | μA |
| Power Supply Current At Operating (Mute signal input) | $I_{DD1}$ | Using internal $V_G$<br>HP Mode<br>No-load operating,<br>MCK=256fs<br>$D_{IN1}$,$D_{IN2}$=16fs, $EN_{REG}$=H | - | 0.95 | 1.6 | mA |
| | $I_{REG1}$ | | - | 0.70 | 1.2 | |
| | $I_{DD2}$ | $V_G$: Externally applied,<br>HP Mode<br>No-load operating,<br>MCK=256fs,<br>$D_{IN1}$,$D_{IN2}$=16fs,$EN_{REG}$=H<br>$V_G$=5V | - | 0.05 | 0.10 | mA |
| | $I_{REG2}$ | | - | 0.70 | 1.2 | |
| | $I_{G2}$ | | - | 0.75 | 1.2 | |
| Digital Input Voltage | $V_{IH}$ | MCK, $D_{IN1}$, $D_{IN2}$<br>$BEEP_{IN}$, $MODE_B$<br>$EN_1$, $EN_2$, $EN_{REG}$, $EN_{VG}$ | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL}$ | | 0 | - | $0.3V_{DD}$ | V |
| Input Leakage Current | $I_{LK}$ | MCK, $D_{IN1}$, $D_{IN2}$<br>$BEEP_{IN}$, $MODE_B$ | - | - | ±1 | μA |
| Pull-down Resistance | $R_{PD}$ | $EN_1$, $EN_2$, $EN_{REG}$, $EN_{VG}$ | 150 | 300 | 450 | kΩ |

(2) REGULATOR CHARACTERISTICS

(Ta=25°C, $V_{DD}$=2.0V, $V_{DDO1}$=$V_{DDO2}$=1.7V, $V_{REG}$=2.15V, $V_{SS}$=$V_{SSO}$=0.0V, Load Impedance=16Ω, $f_S$=44.1kHz, unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input Voltage | $V_{REGH}$ | HP MODE | 1.9 | 2.15 | 4.0 | V |
| | $V_{REGL}$ | LINE MODE | 3.0 | - | 4.0 | V |
| Output Voltage | $V_{DDOH1}$ | HP MODE<br>$V_{CONT}$=1.5V, $V_{REG}$=2.5V | 1.9 | 2.0 | 2.1 | V |
| | $V_{DDOH2}$ | HP MODE<br>$V_{CONT}$=0.5V, $V_{REG}$=2.5V | 0.23 | 0.33 | 0.43 | V |
| | $V_{DDOL1}$ | LINE MODE<br>$V_{CONT}$=1.5V, $V_{REG}$=3.5V | 2.8 | 2.9 | 3.0 | V |
| | $V_{DDOL2}$ | LINE MODE<br>$V_{CONT}$=0.5V, $V_{REG}$=3.5V | 0.38 | 0.48 | 0.58 | V |
| Output Current | $I_{OUT}$ | | 70 | - | - | mA |
| Sink Current | $I_{SINK}$ | | 60 | - | - | mA |
| Dropout Voltage | $\Delta V_{IO}$ | Iout=70mA<br>$V_{DDO1, 2}$=1.7V | - | - | 0.2 | V |
| Ripple Rejection | RR | Vr=0.1Vrms, Iout=70mA<br>fr=1kHz | 36 | 44 | - | dB |
| Load Regulation Voltage | $V_{LR}$ | $I_{REGO}$=0 ~ 24.3mArms | - | - | 520 | μVrms |
| Residual Voltage | $V_{MIN}$ | $V_{CONT}$=0.1V | - | - | 10 | mV |
| $V_{CONT}$ | $V_{CONT}$ | | 0 | - | $V_{REG}$ | V |

The following figure shows a representative example of $V_{CONT}$ versus $V_{REGO}$.
At $V_{CONT}$=1.5V: $V_{REGO}$=2.0V($V_{REG}$=2.5V) in HP MODE, $V_{REGO}$=2.9V($V_{REG}$=3.5V) in LINE MODE.
At $V_{CONT}$=0.5V: $V_{REGO}$=0.33V($V_{REG}$=2.5V) in HP MODE, $V_{REGO}$=0.48V($V_{REG}$=3.5V) in LINE MODE.



(3) AC CHARACTERISTICS

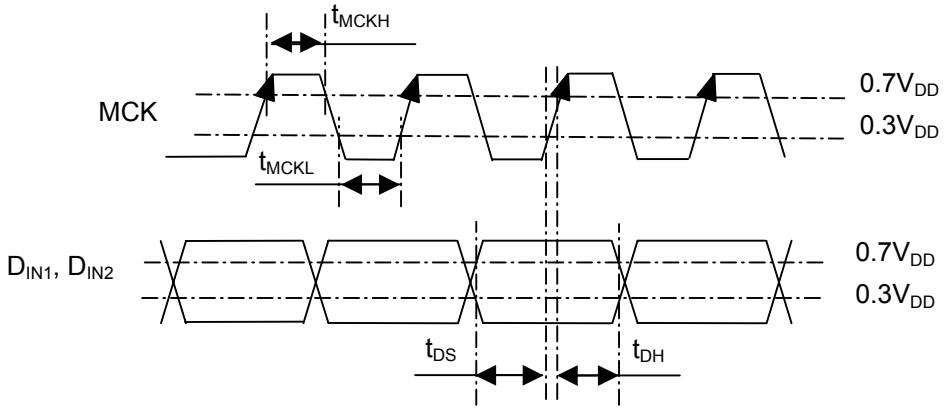
(Ta=25°C, $V_{DD}$=2.0V, $V_{DDO1}$=$V_{DDO2}$=1.7V, $V_{REG}$=2.15V, $V_{SS}$=$V_{SSO}$=0.0V,
Load Impedance=16Ω, $f_S$=44.1kHz, unless otherwise noted)

- Master Clock

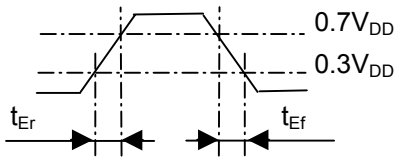
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Frequency | $f_{MCKI}$ | | 8 | - | 50 | MHz |
| Pulse Width (H) | $t_{MCKH}$ | | 8 | - | - | ns |
| Pulse Width (L) | $t_{MCKL}$ | | 8 | - | - | ns |

- Digital Audio Data

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $D_{IN1}$, $D_{IN2}$ Setup Time | $t_{DS}$ | | 5 | - | - | ns |
| $D_{IN1}$, $D_{IN2}$ Hold Time | $t_{DH}$ | | 5 | - | - | ns |
| $EN_1$, $EN_2$, $EN_{REG}$, $EN_{VG}$, $BEEP_{IN}$, $MODE_B$ Rise Time, Fall Time | $t_{Er}$, $t_{Ef}$ | | - | - | 50 | ns |



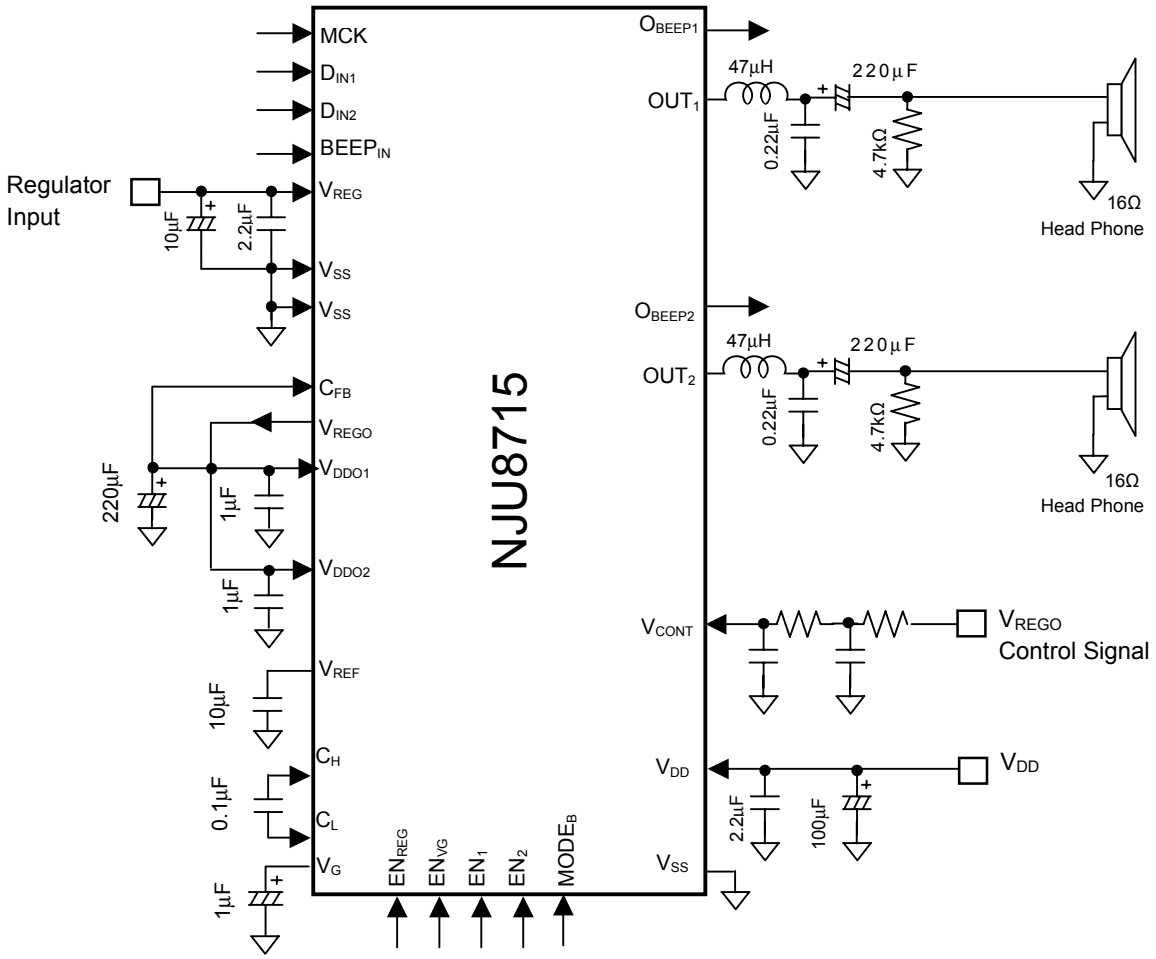

MCK, $D_{IN1}$, $D_{IN2}$ Timing chart



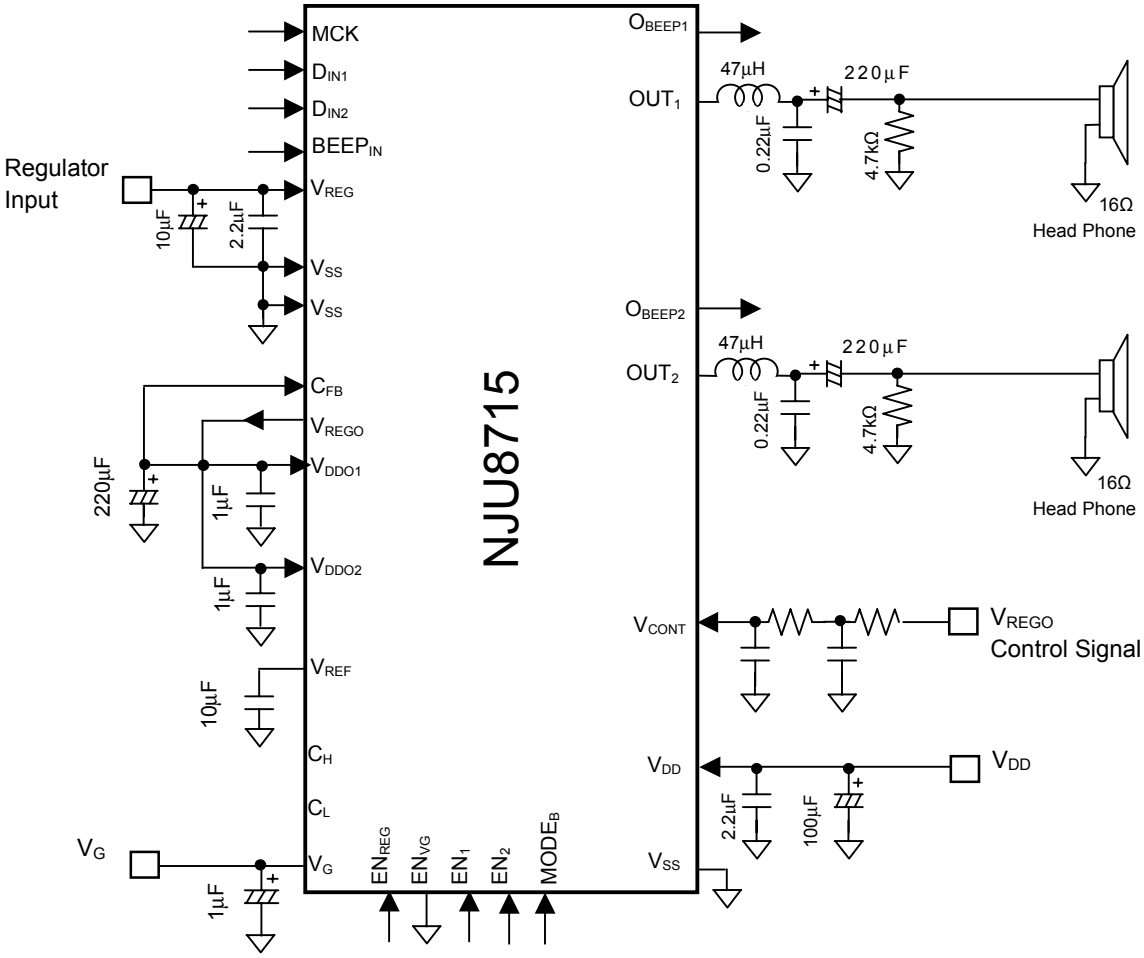

$EN_1$, $EN_2$, $EN_{REG}$, $EN_{VG}$, $BEEP_{IN}$, $MODE_B$ Timing chart

## ■ APPLICATION CIRCUIT

(1) Using Internal $V_G$ ($EN_{VG}$=H)



(2) $V_G$: Externally applied ($EN_{VG}$=L)




Note.7) $C_H$ and $C_L$ pins must be opened when $V_G$ externally applied.

Note.8) De-coupling capacitors must be connected between each power supply pin and GND pin. The capacitor value should be adjusted on the application circuit and the temperature. It may malfunction if capacity value is small.

Note.9) A large-capacitance for the de-coupling capacitors for headphone speaker is recommended to improve a low-frequency characteristics. In addition, a low-ESR(Equivalent series resistance) capacitor is recommened for high power efficiency.

Note.10) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

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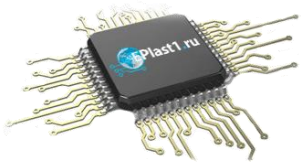
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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