

MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply Voltage Range:**
3.6 V Down to 1.8 V
 - **Ultralow Power Consumption**
 - Active Mode (AM): 180 μ A/MHz
 - Standby Mode (LPM3 WDT Mode, 3 V): 1.1 μ A
 - Off Mode (LPM4 RAM Retention, 3 V): 0.9 μ A
 - Shutdown Mode (LPM4.5, 3 V): 0.25 μ A
 - **Wake-Up From Standby Mode in Less Than 5 μ s**
 - **16-Bit RISC Architecture, Extended Memory, 40-ns Instruction Cycle Time**
 - **Flexible Power Management System**
 - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
 - Supply Voltage Supervision, Monitoring, and Brownout
 - **Unified Clock System**
 - FLL Control Loop for Frequency Stabilization
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - Low-Frequency Trimmed Internal Reference Source (REFO)
 - 32-kHz Crystals (XT1)
 - High-Frequency Crystals up to 25 MHz (XT1)
 - **Hardware Multiplier Supporting 32-Bit Operations**
 - **Three Channel DMA**
 - **Up to Twelve 5-V Tolerant Digital Push/Pull I/Os With Up to 20-mA Drive Strength⁽¹⁾**
 - **16-Bit Timer TD0 With Three Capture/Compare Registers and Support of High-Resolution Mode**
 - **16-Bit Timer TD1 With Three Capture/Compare Registers and Support of High-Resolution Mode**
 - **16-Bit Timer TA0 With Three Capture/Compare Registers**
 - **Universal Serial Communication Interfaces⁽¹⁾**
 - USCI_A0 Supporting
 - Enhanced UART Supporting Auto-Baudrate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 Supporting
 - I²C™
 - Synchronous SPI
 - **10-Bit 200-kSPS Analog-to-Digital (A/D) Converter**
 - Internal Reference
 - Sample-and-Hold
 - Autoscan Feature
 - Up to Eight External Channels, Two Internal Channels, Including Temperature Sensor⁽¹⁾
 - **Up to 16-Channel On-Chip Comparator Including an Ultralow-Power Mode⁽¹⁾**
 - **Serial Onboard Programming, No External Programming Voltage Needed**
 - **Family Members are Summarized in [Table 1](#)**
 - **Available in 40-Pin QFN (RSB) and 38-Pin TSSOP (DA) Packages (See [Table 2](#))**
 - **For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)* ⁽¹⁾**
- (1) Full functionality in the 40-pin QFN package options. For the available features of other packages see [Terminal Functions](#).



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DESCRIPTION

The Texas Instruments MSP430™ family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake up from low-power modes to active mode in less than 5 µs.

The MSP430F51x2 series are microcontroller configurations with two 16-bit high-resolution timers, universal serial communication interfaces (USCI_A0 and USCI_B0), 32-bit hardware multiplier, a high performance 10-bit analog-to-digital (A/D) converter, on-chip comparator, three-channel DMA, 5-V tolerant I/Os, and up to 29 I/O pins.

The MSP430F51x1 series are microcontroller configurations with two 16-bit high-resolution timers, universal serial communication interfaces (USCI_A0 and USCI_B0), 32-bit hardware multiplier, on-chip comparator, three-channel DMA, 5-V tolerant I/Os, and up to 29 I/O pins.

Typical applications for these devices include analog and digital sensor systems, LED lighting, digital power supply, motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

Family members available are summarized in [Table 1](#).

Table 1. Family Members

| Device | Flash (KB) | SRAM (KB) | Timer_A ⁽¹⁾ | Timer_D ⁽²⁾ | USCI | | ADC10_A (Ch) | Comp_B (Ch) | I/O | Package |
|-------------|------------|-----------|------------------------|------------------------|----------------------------|----------------------------------|--------------|-------------|-----|----------|
| | | | | | Channel A: UART, IrDA, SPI | Channel B: SPI, I ² C | | | | |
| MSP430F5172 | 32 | 2 | 3 | 3, 3 | 1 | 1 | 9 ext, 2 int | 16 | 31 | 40 QFN |
| | | | | | | | 8 ext, 2 int | 15 | 29 | 38 TSSOP |
| MSP430F5152 | 16 | 2 | 3 | 3, 3 | 1 | 1 | 9 ext, 2 int | 16 | 31 | 40 QFN |
| | | | | | | | 8 ext, 2 int | 15 | 29 | 38 TSSOP |
| MSP430F5132 | 8 | 1 | 3 | 3, 3 | 1 | 1 | 9 ext, 2 int | 16 | 31 | 40 QFN |
| | | | | | | | 8 ext, 2 int | 15 | 29 | 38 TSSOP |
| MSP430F5171 | 32 | 2 | 3 | 3, 3 | 1 | 1 | - | 16 | 31 | 40 QFN |
| | | | | | | | | 15 | 29 | 38 TSSOP |
| MSP430F5151 | 16 | 2 | 3 | 3, 3 | 1 | 1 | - | 16 | 31 | 40 QFN |
| | | | | | | | | 15 | 29 | 38 TSSOP |
| MSP430F5131 | 8 | 1 | 3 | 3, 3 | 1 | 1 | - | 16 | 31 | 40 QFN |
| | | | | | | | | 15 | 29 | 38 TSSOP |

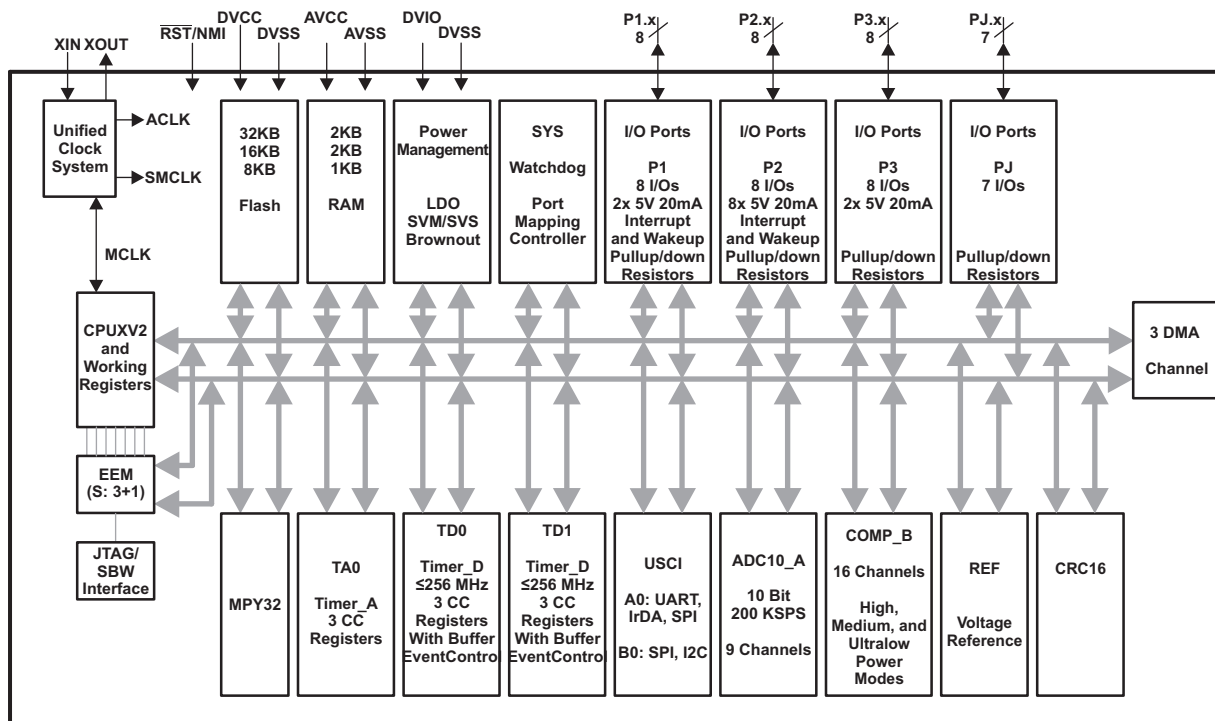
- (1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (2) Each number in the sequence represents an instantiation of Timer_D with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_D, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

Table 2. Ordering Information⁽¹⁾

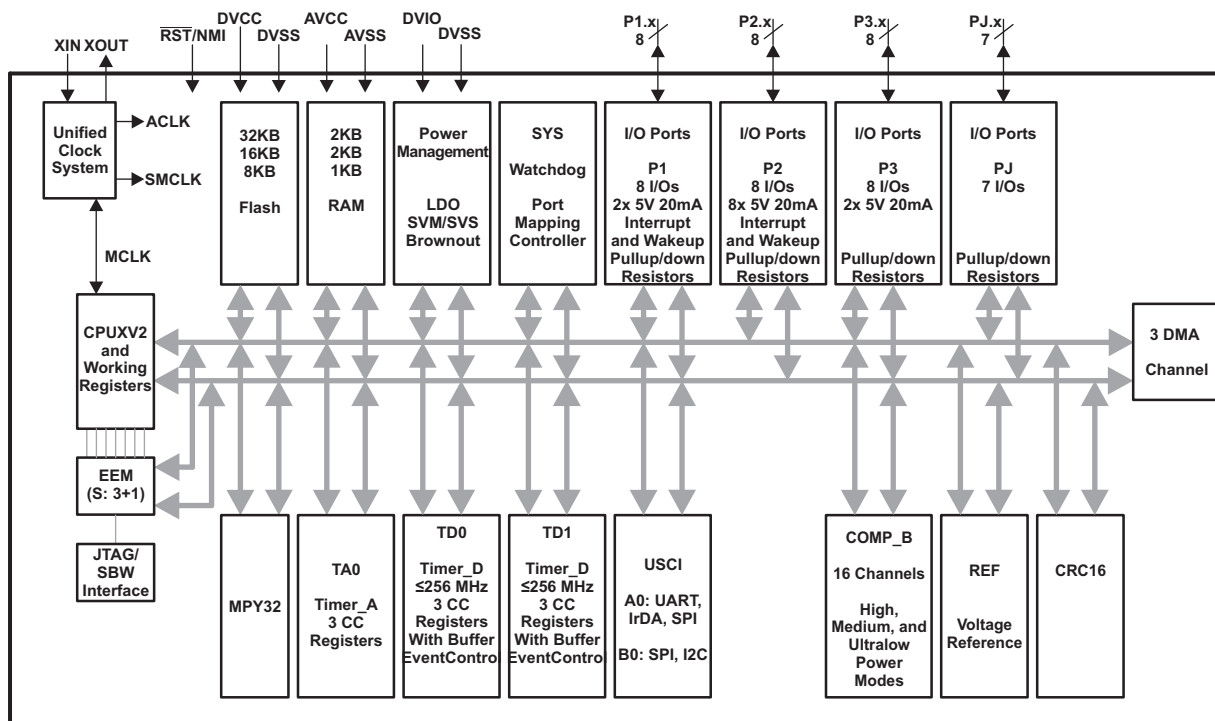
| T _A | PACKAGED DEVICES ⁽²⁾ | |
|----------------|---------------------------------|--------------------------|
| | PLASTIC 38-PIN DA (TSSOP) | PLASTIC 40-PIN RSB (QFN) |
| -40°C to 85°C | MSP430F5132IDA | MSP430F5132IRSB |
| | MSP430F5152IDA | MSP430F5152IRSB |
| | MSP430F5172IDA | MSP430F5172IRSB |
| | MSP430F5131IDA | MSP430F5131IRSB |
| | MSP430F5151IDA | MSP430F5151IRSB |
| | MSP430F5171IDA | MSP430F5171IRSB |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

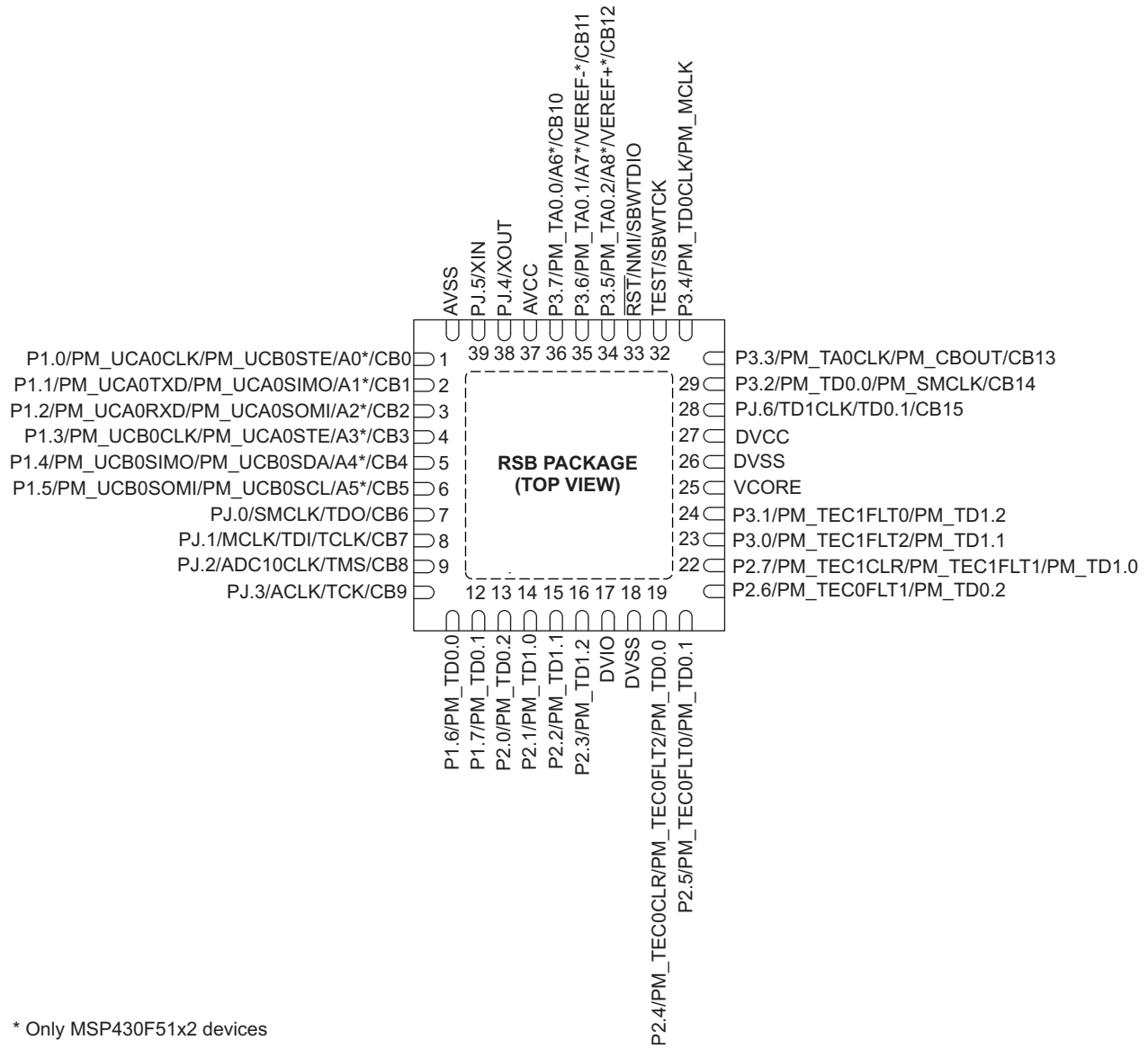
Functional Block Diagram, MSP430F51x2



Functional Block Diagram, MSP430F51x1



Pin Designation, MSP430F51x2IRSB and MSP430F51x1IRSB



* Only MSP430F51x2 devices

Pin Designation, MSP430F51x2IDA and MSP430F51x1IDA

| | | | | |
|-------------------------------------|----|---|----|--------------------------------------|
| AVCC | 1 | ○ | 38 | P3.6/PM_TA0.1/A7*/VEREF-*/CB11 |
| PJ.4/XOUT | 2 | | 37 | P3.5/PM_TA0.2/A8*/VEREF+*/CB12 |
| PJ.5/XIN | 3 | | 36 | RST/NMI/SBWDIO |
| AVSS | 4 | | 35 | TEST/SBWTCK |
| P1.0/PM_UCA0CLK/PM_UCB0STE/A0*/CB0 | 5 | | 34 | P3.3/PM_TA0CLK/PM_CBOUT/CB13 |
| P1.1/PM_UCA0TXD/PM_UCA0SIMO/A1*/CB1 | 6 | | 33 | P3.2/PM_TD0.0/PM_SMCLK/CB14 |
| P1.2/PM_UCA0RXD/PM_UCA0SOMI/A2*/CB2 | 7 | | 32 | PJ.6/TD1CLK/TD0.1/CB15 |
| P1.3/PM_UCB0CLK/PM_UCA0STE/A3*/CB3 | 8 | | 31 | DVCC |
| P1.4/PM_UCB0SIMO/PM_UCB0SDA/A4*/CB4 | 9 | | 30 | DVSS |
| P1.5/PM_UCB0SOMI/PM_UCB0SCL/A5*/CB5 | 10 | | 29 | VCORE |
| PJ.0/SMCLK/TDO/CB6 | 11 | | 28 | P3.1/PM_TEC1FLT0/PM_TD1.2 |
| PJ.1/MCLK/TDI/TCLK/CB7 | 12 | | 27 | P3.0/PM_TEC1FLT2/PM_TD1.1 |
| PJ.2/ADC10CLK/TMS/CB8 | 13 | | 26 | P2.7/PM_TEC1CLR/PM_TEC1FLT1/PM_TD1.0 |
| PJ.3/ACLK/TCK/CB9 | 14 | | 25 | P2.6/PM_TEC0FLT1/PM_TD0.2 |
| P1.6/PM_TD0.0 | 15 | | 24 | P2.5/PM_TEC0FLT0/PM_TD0.1 |
| P1.7/PM_TD0.1 | 16 | | 23 | P2.4/PM_TEC0CLR/PM_TEC0FLT2/PM_TD0.0 |
| P2.0/PM_TD0.2 | 17 | | 22 | DVSS |
| P2.1/PM_TD1.0 | 18 | | 21 | DVIO |
| P2.2/PM_TD1.1 | 19 | | 20 | P2.3/PM_TD1.2 |

**DA PACKAGE
(TOP VIEW)**

* Only MSP430F51x2

Terminal Functions

Table 3. Terminal Functions

| TERMINAL | | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----|----|-----------------------|--|
| NAME | NO. | | | |
| | RSB | DA | | |
| P1.0/ PM_UCA0CLK/ PM_UCB0STE/ A0/ CB0 ⁽²⁾ | 1 | 5 | I/O | General-purpose digital I/O Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode Slave transmit enable – USCI_B0 SPI mode Analog input A0 – 10-bit ADC (see) Comparator_B Input 0 |
| P1.1/ PM_UCA0TXD/ PM_UCA0SIMO/ A1/ CB1 ⁽²⁾ | 2 | 6 | I/O | General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode Analog input A1 – 10-bit ADC ⁽²⁾ Comparator_B Input 1 |
| P1.2/ PM_UCA0RXD/ PM_UCA0SOMI/ A2/ CB2 ⁽²⁾ | 3 | 7 | I/O | General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode Analog input A2 – 10-bit ADC ⁽²⁾ Comparator_B Input 2 |
| P1.3/ PM_UCB0CLK/ PM_UCA0STE/ A3/ CB3 ⁽²⁾ | 4 | 8 | I/O | General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode Analog input A3 – 10-bit ADC ⁽²⁾ Comparator_B Input 3 |
| P1.4/ PM_UCB0SIMO/ PM_UCB0SDA/ A4/ CB4 ⁽²⁾ | 5 | 9 | I/O | General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode Analog input A4 – 10-bit ADC ⁽²⁾ Comparator_B Input 4 |
| P1.5/ PM_UCB0SOMI/ PM_UCB0SCL/ A5/ CB5 ⁽²⁾ | 6 | 10 | I/O | General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode Analog input A5 – 10-bit ADC ⁽²⁾ Comparator_B Input 5 |
| PJ.0/ SMCLK/ TDO/ CB6 | 7 | 11 | I/O | General-purpose digital I/O SMCLK clock output Test data output port Comparator_B Input 6 |
| PJ.1/ MCLK/ TDI/TCLK/ CB7 | 8 | 12 | I/O | General-purpose digital I/O MCLK clock output Test data input or test clock input Comparator_B Input 7 |
| PJ.2/ ADC10CLK/ TMS/ CB8 | 9 | 13 | I/O | General-purpose digital I/O ADC10_A clock output Test mode select Comparator_B Input 8 |
| PJ.3/ ACLK/ TCK/ CB9 | 10 | 14 | I/O | General-purpose digital I/O ACLK output port Test clock Comparator_B Input 9 |
| P1.6/ PM_TD0.0 | 11 | 15 | I/O, DV _{IO} | General-purpose digital I/O TD0 CCR0 compare output/capture input |
| P1.7/ PM_TD0.1 | 12 | 16 | I/O, DV _{IO} | General-purpose digital I/O TD0 CCR1 compare output/capture input |
| P2.0/ PM_TD0.2 | 13 | 17 | I/O, DV _{IO} | General-purpose digital I/O TD0 CCR2 compare output/capture input |

(1) I = input, O = output, N/A = not available on this package offering
(2) The ADC10_A module is available on MSP430F51x2 devices. The secondary pin functions Ax (ADC10_A channel x) available only in MSP430F51x2 devices.

Table 3. Terminal Functions (continued)

| TERMINAL | | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----|----|-----------------------|--|
| NAME | NO. | | | |
| | RSB | DA | | |
| P2.1/ PM_TD1.0 | 14 | 18 | I/O, DV _{IO} | General-purpose digital I/O TD1 CCR0 compare output/capture input |
| P2.2/ PM_TD1.1 | 15 | 19 | I/O, DV _{IO} | General-purpose digital I/O TD1 CCR1 compare output/capture input |
| P2.3/ PM_TD1.2 | 16 | 20 | I/O, DV _{IO} | General-purpose digital I/O TD1 CCR2 compare output/capture input |
| DVIO | 17 | 21 | | 5V tolerant digital I/O power supply |
| DVSS | 18 | 22 | | Digital ground supply |
| P2.4/ PM_TEC0CLR/ PM_TEC0FLT2/ PM_TD0.0 | 19 | 23 | I/O, DV _{IO} | General-purpose digital I/O TD0 external clear input/TD0 fault input channel 2 (controlled by module input enable) TD0 CCR0 compare output |
| P2.5/ PM_TEC0FLT0/ PM_TD0.1 | 20 | 24 | I/O, DV _{IO} | General-purpose digital I/O TD0 fault input channel 0 TD0 CCR1 compare output |
| P2.6/ PM_TEC0FLT1/ PM_TD0.2 | 21 | 25 | I/O, DV _{IO} | General-purpose digital I/O TD0 fault input channel 1 TD0 CCR2 compare output |
| P2.7/ PM_TEC1CLR/ PM_TEC1FLT1/ PM_TD1.0 | 22 | 26 | I/O, DV _{IO} | General-purpose digital I/O TD1 external clear/TD1 fault input channel 1 (controlled by module input enable) TD1 CCR0 compare output |
| P3.0/ PM_TEC1FLT2 / PM_TD1.1 | 23 | 27 | I/O, DV _{IO} | General-purpose digital I/O TD1 fault input channel 2 TD1 CCR1 compare output |
| P3.1/ PM_TEC1FLT0/ PM_TD1.2 | 24 | 28 | I/O, DV _{IO} | General-purpose digital I/O TD1 fault input channel 0 TD1 CCR2 compare output |
| VCORE | 25 | 29 | | Regulated core power supply |
| DVSS | 26 | 30 | | Digital ground supply |
| DVCC | 27 | 31 | | Digital power supply |
| PJ.6/ TD1CLK/ TD0.1/ CB15 | 28 | 32 | I/O | General-purpose digital I/O TD1 clock input TD0 CCR1 compare output Comparator_B Input 15 |
| P3.2/ PM_TD0.0/ PM_SMCLK/ CB14 | 29 | 33 | I/O | General-purpose digital I/O TD0 CCR0 capture input SMCLK output Comparator_B Input 14 |
| P3.3/ PM_TA0CLK/ PM_CBOU/ CB13 | 30 | 34 | I/O | General-purpose digital I/O TA0 clock input Comparator_B output Comparator_B Input 13 |
| P3.4/ PM_TD0CLK/ PM_MCLK | 31 | - | I/O | General-purpose digital I/O TD0 clock input MCLK output |
| TEST/ SBWTCK | 32 | 35 | | Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock |
| RST/ NMI/ SBWDIO | 33 | 36 | | Reset input active low Non-maskable interrupt input Spy-By-Wire data input/output |

Table 3. Terminal Functions (continued)

| TERMINAL | | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----|----|--------------------|---|
| NAME | NO. | | | |
| | RSB | DA | | |
| P3.5/ PM_TA0.2/ A8 ⁽³⁾ VEREF+/ CB12 | 34 | 37 | I/O | General-purpose digital I/O TA0 CCR2 compare output/capture input Analog input A8 – 10-bit ADC ⁽³⁾ Positive terminal for the ADC's reference voltage for an external applied reference voltage Comparator_B Input 12 |
| P3.6/ PM_TA0.1/ A7 ⁽³⁾ / VEREF-/ CB11 | 35 | 38 | I/O | General-purpose digital I/O TA0 CCR1 compare output/capture input Analog input A7 – 10-bit ADC ⁽³⁾ Negative terminal for the ADC's reference voltage for an external applied reference voltage Comparator_B Input 11 |
| P3.7/ PM_TA0.0/ A6 ⁽³⁾ / CB10 | 36 | - | I/O | General-purpose digital I/O TA0 CCR0 compare output/capture input Analog input A6 – 10-bit ADC ⁽³⁾ Comparator_B Input 10 |
| AVCC | 37 | 1 | | Analog power supply |
| PJ.4/ XOUT | 38 | 2 | I/O | General-purpose digital I/O Output terminal of crystal oscillator |
| PJ.5/ XIN | 39 | 3 | I/O | General-purpose digital I/O Input terminal for crystal oscillator |
| AVSS | 40 | 4 | | Analog ground supply |
| QFN pad | - | NA | | Recommended to connect to DVSS externally |

(3) The ADC10_A module is available on MSP430F51x2 devices. The secondary pin functions Ax (ADC10_A channel x) available only in MSP430F51x2 devices.

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. [Table 4](#) shows examples of the three types of instruction formats; [Table 5](#) shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 4. Instruction Word Formats

| FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 5. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|--------------------|------------------|-------------------------------|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV & MEM, & TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect autoincrement | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11 R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and FLL loop control and DCOCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wakeup from $\overline{\text{RST}}$ /NMI, P1, and P2

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|------------------|--------------|-------------|
| System Reset Power-Up External Reset Watchdog Timeout, Key Violation Flash Memory Key Violation | WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)} | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant Memory Access JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾ | (Non)maskable | 0FFFCCh | 62 |
| User NMI NMI Oscillator Fault Flash Memory Access Violation | NMIIFG, OFIFG, ACCVIFG (SYSUNIV) ^{(1) (2)} | (Non)maskable | 0FFFAh | 61 |
| Comp_B | CBIIFG, CBIFG (CBIV) ^{(1) (3)} | Maskable | 0FFF8h | 60 |
| TECO | TECOFLTIFG, TECOEXCLRIFG, TECOAXCLRIFG ^{(1) (3)} | Maskable | 0FFF6h | 59 |
| TD0 | TD0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFF4h | 58 |
| TD0 | TD0CCR1 CCIFG1, ... TD0CCR2 CCIFG2, TD0IFG, TD0HFLIFG, TD0HFHIFG, TD0HLKIFG, TD0HUNLKIFG (TD0IV) ^{(1) (3)} | Maskable | 0FFF2h | 57 |
| Watchdog Timer_A Interval Timer Mode | WDTIFG | Maskable | 0FFF0h | 56 |
| USCI_A0 Receive or Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (3)} | Maskable | 0FFEEh | 55 |
| USCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG, I2C Status Interrupt Flags (UCB0IV) ^{(1) (3)} | Maskable | 0FFECCh | 54 |
| ADC10_A (MSP430F51x2 only) | ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV) ^{(1) (3)} | Maskable | 0FFEAh | 53 |
| TA0 | TA0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFE8h | 52 |
| TA0 | TA0CCR1 CCIFG1 ... TA0CCR2 CCIFG2, TA0IFG (TA0IV) ^{(1) (3)} | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (3)} | Maskable | 0FFE4h | 50 |
| TEC1 | TEC1FLTIFG, TEC1EXCLRIFG, TEC1AXCLRIFG ^{(1) (3)} | Maskable | 0FFE2 | 49 |
| TD1 | TD1CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFE0h | 48 |
| TD1 | TD1CCR1 CCIFG1 ... TD1CCR2 CCIFG2, TD1IFG, TD1HFLIFG, TD1HFHIFG, TD1HLKIFG, TD1HUNLKIFG (TD1IV) ^{(1) (3)} | Maskable | 0FFDEh | 47 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (3)} | Maskable | 0FFDCh | 46 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (3)} | Maskable | 0FFDAh | 45 |
| Reserved | Reserved ⁽⁴⁾ | | 0FFD8h | 44 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Memory Organization

| | | MSP430F5132, MSP430F5131 | MSP430F5152, MSP430F5151 | MSP430F5172, MSP430F5171 |
|---|---------------|----------------------------|----------------------------|----------------------------|
| Memory Main: interrupt vector Main: code memory | Size | 8KB | 16KB | 32KB |
| | Flash | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| | Flash | 00FFFFh to 00E000h | 00FFFFh to 00C000h | 00FFFFh to 008000h |
| RAM | Size | 1KB | 2KB | 2KB |
| | Sector 0 | 001FFFh to 001C00h | 0023FFh to 001C00h | 0023FFh to 001C00h |
| Information memory (Flash) | Size | 512 Byte | 512 Byte | 512 Byte |
| | Info A | 128B 0019FF to 001980h | 128B 0019FF to 001980h | 128B 0019FF to 001980h |
| | Info B | 128B 00197F to 001900h | 128B 00197F to 001900h | 128B 00197F to 001900h |
| | Info C | 128B 0018FF to 001880h | 128B 0018FF to 001880h | 128B 0018FF to 001880h |
| | Info D | 128B 00187F to 001800h | 128B 00187F to 001800h | 128B 00187F to 001800h |
| Bootstrap loader (BSL) memory | Size | 2K | 2KB | 2KB |
| | BSL 3 | 512B 0017FFh to 001600h | 512B 0017FFh to 001600h | 512B 0017FFh to 001600h |
| | BSL 2 | 512B 0015FFh to 001400h | 512B 0015FFh to 001400h | 512B 0015FFh to 001400h |
| | BSL 1 | 512B 0013FFh to 001200h | 512B 0013FFh to 001200h | 512B 0013FFh to 001200h |
| | BSL 0 | 512B 0011FFh to 001000h | 512B 0011FFh to 001000h | 512B 0011FFh to 001000h |
| Peripherals | Size Flash | 4KB 000FFFh to 000000h | 4KB 000FFFh to 000000h | 4KB 000FFFh to 000000h |

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory via the BSL is protected by user-defined password. A bootstrap loader security key is provided to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. For complete description of the features of the BSL and its implementation, see *MSP430 Programming Via the Bootstrap Loader* (SLAU319).

Table 7. BSL Functions

| BSL FUNCTION | DESCRIPTION | |
|------------------|------------------------|-------------------------|
| | 40-PIN QFN RSB PACKAGE | 38-PIN TSSOP DA PACKAGE |
| RST/NMI/SBWT DIO | Entry sequence signal | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal | Entry sequence signal |
| Data transmit | P3.7 | P3.5 |
| Data receive | P3.6 | P3.6 |
| VCC | Power Supply | Power Supply |
| VSS | Ground Supply | Ground Supply |

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n . Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in the [Memory Organization](#) section.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

Digital I/O

There are up to three 8-bit I/O ports implemented. Port PJ contains seven individual I/O pins, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise. P1 and P2 can also be accessed word-wise (PA).
- The input and output voltage levels of the pins supplied by DV_{IO} (see [Table 3](#)) are defined by the voltage supplied by DV_{IO} (up to 5V).

Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to Port P1, Port P2, and Port P3.

Table 8. Port Mapping Mnemonics and Functions

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|--------------------------|-----------------|---|------------------------------|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_UCA0CLK | USCI_A0 clock input/output (direction controlled by USCI) | |
| | PM_UCB0STE | USCI_B0 SPI slave transmit enable (direction controlled by USCI) | |
| 2 | PM_UCA0TXD | USCI_A0 UART TXD (Direction controlled by USCI - output) | |
| | PM_UCA0SIMO | USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| 3 | PM_UCB0SOMI | USCI_B0 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB0SCL | USCI_B0 I2C clock (open drain and direction controlled by USCI) | |
| 4 | PM_UCA0RXD | USCI_A0 UART RXD (Direction controlled by USCI - input) | |
| | PM_UCA0SOMI | USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| 5 | PM_UCB0SIMO | USCI_B0 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB0SDA | USCI_B0 I2C data (open drain and direction controlled by USCI) | |
| 6 | PM_UCB0CLK | USCI_B0 clock input/output (direction controlled by USCI) | |
| | PM_UCA0STE | USCI_A0 SPI slave transmit enable (direction controlled by USCI) | |
| 7 | PM_TD0.0 | TD0 input capture channel 0 | TD0 output compare channel 0 |
| 8 | PM_TD0.1 | TD0 input capture channel 1 | TD0 output compare channel 1 |
| 9 | PM_TD0.2 | TD0 input capture channel 2 | TD0 output compare channel 2 |
| 10 | PM_TD1.0 | TD1 input capture channel 0 | TD1 output compare channel 0 |
| 11 | PM_TD1.1 | TD1 input capture channel 1 | TD1 output compare channel 1 |
| 12 | PM_TD1.2 | TD1 input capture channel 2 | TD1 output compare channel 2 |
| 13 | PM_CLR1TD0.0 | TD0 external clear input | TD0 output compare channel 0 |
| | PM_FLT1_2TD0.0 | TD0 fault input channel 2 | |
| 14 | PM_FLT1_0TD0.1 | TD0 fault input channel 0 | TD0 output compare channel 1 |
| 15 | PM_FLT1_1TD0.2 | TD0 fault input channel 1 | TD0 output compare channel 2 |
| 16 | PM_CLR2TD1.0 | TD1 external clear input (controlled by module input enable) | TD1 output compare channel 0 |
| | PM_FLT2_1TD1.0 | TD1 fault input channel 1 (controlled by module input enable) | |
| 17 | PM_FLT2_2TD1.1 | TD1 fault input channel 2 | TD1 output compare channel 1 |
| 18 | PM_FLT2_0TD1.2 | TD1 fault input channel 0 | TD1 output compare channel 2 |
| 19 | PM_TD0.0SMCLK | TD0 input capture channel 0 | SMCLK output |
| 20 | PM_TA0CLKCBOUT | TA0 input clock | Comparator_B output |
| 21 | PM_TD0CLKMCLK | TD0 input clock | MCLK output |
| 22 | PM_TA0_0 | TA0 input capture channel 0 | TA0 output compare channel 0 |
| 23 | PM_TA0_1 | TA0 input capture channel 1 | TA0 output compare channel 1 |
| 24 | PM_TA0_2 | TA0 input capture channel 2 | TA0 output compare channel 2 |
| 25 | PM_DMAE0SMCLK | DMAE0 input | SMCLK output |
| 26 | PM_DMAE1MCLK | DMAE1 input | MCLK output |
| 27 | PM_DMAE2SVM | DMAE2 input | SVM output |
| 28 | PM_TD0OUTH | TD0 3-state input | ADC10CLK |
| 29 | PM_TD1OUTH | TD1 3-state input | ACLK |
| 30 | Reserved | None | DVSS |
| 31 (0FFh) ⁽¹⁾ | PM_ANALOG | Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

Table 9. Default Mapping

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|--|--------------------------------|---|---|
| P1.0/PM_UCA0CLK/ PM_UCB0STE/A0/CB0 | PM_UCA0CLK PM_UCB0STE | USCI_A0 clock input/output (direction controlled by USCI) | USCI_B0 SPI slave transmit enable (direction controlled by USCI) |
| P1.1/PM_UCA0TXD/ PM_UCA0SIMO/A1/CB1 | PM_UCA0TXD PM_UCA0SIMO | USCI_A0 UART TXD (Direction controlled by USCI - output) | USCI_A0 SPI slave in master out (direction controlled by USCI) |
| P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A2/CB2 | PM_UCA0RXD PM_UCA0SOMI | USCI_A0 UART RXD (Direction controlled by USCI - input) | USCI_A0 SPI slave out master in (direction controlled by USCI) |
| P1.3/PM_UCB0CLK/ PM_UCA0STE/A3/CB3 | PM_UCB0CLK PM_UCA0STE | USCI_B0 clock input/output (direction controlled by USCI) | USCI_A0 SPI slave transmit enable (direction controlled by USCI) |
| P1.4/PM_UCB0SIMO/ PM_UCB0SDA/A4/CB4 | PM_UCB0SIMO PM_UCB0SDA | USCI_B0 SPI slave in master out (direction controlled by USCI) | USCI_B0 I2C data (open drain and direction controlled by USCI) |
| P1.5/PM_UCB0SOMI/ PM_UCB0SCL/A5/CB5 | PM_UCB0SOMI PM_UCB0SCL | USCI_B0 SPI slave out master in (direction controlled by USCI) | USCI_B0 I2C clock (open drain and direction controlled by USCI) |
| P1.6/PM_TD0.0 | PM_TD0.0 | TD0 input capture channel 0 | TD0 output compare channel 0 |
| P1.7/PM_TD0.1 | PM_TD0.1 | TD0 input capture channel 1 | TD0 output compare channel 1 |
| P2.0/PM_TD0.2 | PM_TD0.2 | TD0 input capture channel 2 | TD0 output compare channel 2 |
| P2.1/PM_TD1.0 | PM_TD1.0 | TD1 input capture channel 0 | TD1 output compare channel 0 |
| P2.2/PM_TD1.1 | PM_TD1.1 | TD1 input capture channel 1 | TD1 output compare channel 1 |
| P2.3/PM_TD1.2 | PM_TD1.2 | TD1 input capture channel 2 | TD1 output compare channel 2 |
| P2.4/PM_TEC0CLR/ PM_TEC0FLT2/PM_TD0.0 | PM_CLR1TD0.0 PM_FLT1_2TD0.0 | TD0 external clear input (controlled by module input enable) TD0 fault input channel 2 (controlled by module input enable) | TD0 output compare channel 0 |
| P2.5/PM_TEC0FLT0/PM_TD0.1 | PM_FLT1_0TD0.1 | TD0 fault input channel 0 | TD0 output compare channel 1 |
| P2.6/PM_TEC0FLT1/PM_TD0.2 | PM_FLT1_1TD0.2 | TD0 fault input channel 1 | TD0 output compare channel 2 |
| P2.7/PM_TEC1CLR/ PM_TEC1FLT1/PM_TD1.0 | PM_CLR2TD1.0 PM_FLT2_1TD1.0 | TD1 external clear input (controlled by module input enable) TD1 fault input channel 1 (controlled by module input enable) | TD1 output compare channel 0 |
| P3.0/PM_TEC1FLT2/ PM_TD1.1 | PM_FLT2_2TD1.1 | TD1 fault input channel 2 | TD1 output compare channel 1 |
| P3.1/PM_TEC1FLT0/ PM_TD1.2 | PM_FLT2_0TD1.2 | TD1 fault input channel 0 | TD1 output compare channel 2 |
| P3.2/PM_TD0.0/ PM_SMCLK/CB14 | PM_TD0.0SMCLK | TD0 input capture channel 0 | SMCLK output |
| P3.3/PM_TA0CLK/ PM_CBOUT/CB13 | PM_TA0CLKCBOUT | TA0 input clock | Comparator_B output |
| P3.4/PM_TD0CLK/ PM_MCLK | PM_TD0CLKMCLK | TD0 input clock | MCLK output |
| P3.5/PM_TA0.2/ VEREF+/CB12 | PM_TA3_2 | TA0 input capture channel 0 | TA0 output compare channel 0 |
| P3.6/PM_TA0.1/A7 VEREF-/CB11 | PM_TA3_1 | TA0 input capture channel 1 | TA0 output compare channel 1 |
| P3.7/PM_TA0.0/ A6/CB10 | PM_TA3_0 | TA0 input capture channel 2 | TA0 output compare channel 2 |

Oscillator and System Clock

The clock system (Unified Clock System, UCS) module includes support for a 32-kHz watch crystal oscillator and high-frequency crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal or high-frequency crystal (LFXT1), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations

Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 10. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY | |
|-------------------------------|--------------------------------|--------------|----------------------|----------|--------|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | Highest | |
| | Brownout (BOR) | | 02h | | |
| | RST/NMI (POR) | | 04h | | |
| | DoBOR (BOR) | | 06h | | |
| | LPM5 wakeup (BOR) | | 08h | | |
| | Security violation (BOR) | | 0Ah | | |
| | SVSL (POR) | | 0Ch | | |
| | SVSH (POR) | | 0Eh | | |
| | SVML_OVP (POR) | | 10h | | |
| | SVMH_OVP (POR) | | 12h | | |
| | DoPOR (POR) | | 14h | | |
| | WDT timeout (PUC) | | 16h | | |
| | WDT key violation (PUC) | | 18h | | |
| | KEYV flash key violation (PUC) | | 1Ah | | |
| | Reserved | | 1Ch | | |
| | Peripheral area fetch (PUC) | | 1Eh | | |
| | PMM key violation (PUC) | | 20h | | |
| Reserved | 22h to 3Eh | Lowest | | | |
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | Highest | |
| | SVMLIFG | | 02h | | |
| | SVMHIFG | | 04h | | |
| | DLYLIFG | | 06h | | |
| | DLYHIFG | | 08h | | |
| | VMAIFG | | 0Ah | | |
| | JMBINIFG | | 0Ch | | |
| | JMBOUFIG | | 0Eh | | |
| | VLRIFG | | 10h | | |
| | VLRHIFG | | 12h | | |
| | Reserved | | 14h to 1Eh | | Lowest |
| | SYSUNIV, User NMI | | No interrupt pending | | 019Ah |
| NMIFG | | 02h | | | |
| OFIFG | | 04h | | | |
| ACCVIFG | | 06h | | | |
| Reserved | | 08h to 1Eh | Lowest | | |

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to wake to move data to or from a peripheral.

Table 11. DMA Trigger Assignments ⁽¹⁾

| TRIGGER | CHANNEL | | |
|---------|----------------|----------------|----------------|
| | 0 | 1 | 2 |
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TD0CCR0 CCIFG | TD0CCR0 CCIFG | TD0CCR0 CCIFG |
| 4 | TD0CCR2 CCIFG | TD0CCR2 CCIFG | TD0CCR2 CCIFG |
| 5 | TD1CCR0 CCIFG | TD1CCR0 CCIFG | TD1CCR0 CCIFG |
| 6 | TD1CCR2 CCIFG | TD1CCR2 CCIFG | TD1CCR2 CCIFG |
| 7 | Reserved | Reserved | Reserved |
| 8 | Reserved | Reserved | Reserved |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | Reserved | Reserved | Reserved |
| 12 | Reserved | Reserved | Reserved |
| 13 | Reserved | Reserved | Reserved |
| 14 | Reserved | Reserved | Reserved |
| 15 | Reserved | Reserved | Reserved |
| 16 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 17 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 18 | UCB0RXIFG | UCB0RXIFG | UCB0RXIFG |
| 19 | UCB0TXIFG | UCB0TXIFG | UCB0TXIFG |
| 20 | Reserved | Reserved | Reserved |
| 21 | Reserved | Reserved | Reserved |
| 22 | Reserved | Reserved | Reserved |
| 23 | Reserved | Reserved | Reserved |
| 24 | ADC10IFG0 | ADC10IFG0 | ADC10IFG0 |
| 25 | Reserved | Reserved | Reserved |
| 26 | Reserved | Reserved | Reserved |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two modules, A and B.

The USCI_Ax module provides support for SPI (3 or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bx module provides support for SPI (3 or 4 pin) or I²C.

TA0

TA0 is a 16-bit timer/counter with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. TA0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|-------------------|---------------------|---------------------------|--------------|----------------------|----------------------|-----------------------------------|-----------------------------------|
| RSB (40-PIN QFN) | DA (38-PIN TSSOP) | | | | | | RSB (40-PIN QFN) | DA (38-PIN TSSOP) |
| P3.3 - 30 | P3.3 - 34 | TA0CLK | TACLK | Timer | NA | NA | - | - |
| ACLK (internal) | ACLK | ACLK | ACLK | | | | - | - |
| SMCLK (internal) | SMCLK | SMCLK | SMCLK | | | | - | - |
| P3.3 - 30 | P3.3 - 34 | TA0CLK | $\overline{\text{TACLK}}$ | | | | - | - |
| P3.7 - 36 | - | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | P3.7 - 36 | - |
| - | - | CBOUT | CCI0B | | | | - | - |
| - | - | V _{SS} | GND | | | | - | - |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P3.6 - 35 | - | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | P3.6 - 35 | P3.6 - 38 |
| - | - | ACLK | CCI1B | | | | ADC10_A ⁽¹⁾ (internal) | ADC10_A ⁽¹⁾ (internal) |
| - | - | V _{SS} | GND | | | | ADC10SHSx = 001b | ADC10SHSx = 001b |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P3.5 - 34 | P3.5 - 37 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | P3.5 - 34 | P3.5 - 37 |
| - | - | V _{SS} | CCI2B | | | | - | - |
| - | - | V _{SS} | GND | | | | - | - |
| - | - | V _{CC} | V _{CC} | | | | - | - |

(1) The ADC10_A trigger is available on MSP430F51x2 devices.

TD0

TD0 is a 16-bit timer/counter with three capture/compare registers supporting up to 256-MHz / 4-ns resolution. TD0 can support multiple capture/compares, PWM outputs, and interval timing. TD0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. External fault inputs as well as an external timer counter clear is supported along with interrupt flags from the TEC0 module.

Table 13. TD0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|--------------------------|--------------------------|---------------------|---------------------------|--------------|----------------------|----------------------|---|---|
| RSB (40-PIN QFN) | DA (38-PIN TSSOP) | | | | | | RSB (40-PIN QFN) | DA (38-PIN TSSOP) |
| P3.4 - 31 | - | TD0CLK | TDCLK | Timer | NA | NA | - | - |
| ACLK (internal) | ACLK (internal) | ACLK | ACLK | | | | - | - |
| SMCLK (internal) | SMCLK (internal) | SMCLK | SMCLK | | | | - | - |
| P3.4 - 31 | - | TD0CLK | $\overline{\text{TDCLK}}$ | | | | - | - |
| - | - | - | CLK0 | | | | - | - |
| P2.4 - 19 | P2.4 - 23 | TEC0CLR | TECXCLR | | | | - | - |
| P1.6 - 11 ⁽¹⁾ | P1.6 - 15 ⁽¹⁾ | TD0.0 | CC10A | CCR0 | TD0 | TD0 | P1.6 - 11 ⁽¹⁾ | P1.6 - 15 ⁽¹⁾ |
| P3.2 - 29 | P3.2 - 33 | TD0.0 | CC10B | | | | P2.4 - 19 | P2.4 - 23 |
| - | - | V _{SS} | GND | | | | ADC10_A (internal) ADC10SHSx = 010b ⁽²⁾ | ADC10_A (internal) ADC10SHSx = 010b ⁽²⁾ |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P2.5 - 20 | P2.5 - 24 | TEC0FLT0 | TECXFLT0 | | | | - | - |
| P1.7 - 12 ⁽¹⁾ | P1.7 - 16 ⁽¹⁾ | TD0.1 | CC11A | CCR1 | TD1 | TD1 | P1.7 - 12 ⁽¹⁾ | P1.7 - 16 ⁽¹⁾ |
| CBOU (internal) | CBOU (internal) | TD0.1 | CC11B | | | | PJ.6 - 28 | PJ.6 - 32 |
| - | - | V _{SS} | GND | | | | P2.5 - 20 | P2.5 - 24 |
| - | - | V _{CC} | V _{CC} | | | | ADC10_A (internal) ADC10SHSx = 011b ⁽²⁾ | ADC10_A (internal) ADC10SHSx = 011b ⁽²⁾ |
| P2.6 - 21 | P2.6 - 20 | TEC0FLT1 | TECXFLT1 | | | | - | - |
| P2.0 - 13 ⁽¹⁾ | P2.0 - 17 ⁽¹⁾ | TD0.2 | CC12A | CCR2 | TD2 | TD2 | P2.0 - 13 ⁽¹⁾ | P2.0 - 17 ⁽¹⁾ |
| ACLK (internal) | ACLK (internal) | TD0.2 | CC12B | | | | P2.6 - 21 | P2.6 - 25 |
| - | - | V _{SS} | GND | | | | - | - |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P2.4 - 19 | P2.4 - 23 | TEC0FLT2 | TECXFLT2 | | | | - | - |

(1) Pins P1.6 for TD0.0, P1.7 for TD0.1, and P2.0 for TD0.2 are optimized for matching.
 (2) The ADC10_A trigger is available on MSP430F51x2 devices.

TD1

TD1 is a 16-bit timer/counter with three capture/compare registers supporting up to 256-MHz / 4-ns resolution. TD1 can support multiple capture/compares, PWM outputs, and interval timing. TD1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. External fault inputs as well as a external timer counter clear is supported along with interrupt flags from the TEC0 module.

Table 14. TD1 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|--------------------------|--------------------------|---------------------|---------------------------|--------------|----------------------|----------------------|--------------------------|--------------------------|
| RSB (40-PIN QFN) | DA (38-PIN TSSOP) | | | | | | RSB (40-PIN QFN) | DA (38-PIN TSSOP) |
| PJ.6 - 28 | PJ.6 - 32 | TD1CLK | TDCLK | Timer | NA | NA | - | - |
| ACLK (internal) | ACLK | ACLK | ACLK | | | | - | - |
| SMCLK (internal) | SMCLK | SMCLK | SMCLK | | | | - | - |
| PJ.6 - 28 | PJ.6 - 32 | TD1CLK | $\overline{\text{TDCLK}}$ | | | | - | - |
| - | - | from TD0 (internal) | CLK0 | | | | - | - |
| P2.7 - 22 | P2.7 - 26 | TEC1CLR | TECxCLR | CCR0 | TD0 | TD0 | - | - |
| P2.1 - 14 ⁽¹⁾ | P2.1 - 18 ⁽¹⁾ | TD1.0 | CCI0A | | | | P2.1 - 14 ⁽¹⁾ | P2.1 - 18 ⁽¹⁾ |
| - | - | TD1.0 | CCI0B | | | | P2.7 - 22 | P2.7 - 26 |
| - | - | V _{SS} | GND | | | | - | - |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P3.1 - 24 | P3.1 - 28 | TEC1FLT0 | TECXFLT0 | CCR1 | TD1 | TD1 | - | - |
| P2.2 - 15 ⁽¹⁾ | P2.2 - 19 ⁽¹⁾ | TD1.1 | CCI1A | | | | P2.2 - 15 ⁽¹⁾ | P2.2 - 19 ⁽¹⁾ |
| CBOU (internal) | CBOU (internal) | TD1.1 | CCI1B | | | | P3.0 - 23 | P3.0 - 27 |
| - | - | V _{SS} | GND | | | | - | - |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P2.7 - 22 | P2.7 - 26 | TEC1FLT1 | TECXFLT1 | CCR2 | TD2 | TD2 | - | - |
| P2.3 - 16 ⁽¹⁾ | P2.3 - 20 ⁽¹⁾ | TD1.2 | CCI2A | | | | P2.3 - 16 ⁽¹⁾ | P2.3 - 20 ⁽¹⁾ |
| ACLK (internal) | ACLK (internal) | TD1.2 | CCI2B | | | | P3.1 - 24 | P3.1 - 28 |
| - | - | V _{SS} | GND | | | | - | - |
| - | - | V _{CC} | V _{CC} | | | | - | - |
| P3.0 - 23 | P3.0 - 27 | TEC1FLT2 | TECXFLT2 | | | | - | - |

(1) Pins P2.1 for TD1.0, P2.2 for TD1.1, and P2.3 for TD1.2 are optimized for matching.

Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

ADC10_A (MSP430F51x2 Only)

The ADC10_A module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

REF Voltage Reference

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

Embedded Emulation Module (EEM) (S Version)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

Peripheral File Map
Table 15. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|--------------|----------------------|
| Special Functions (see Table 16) | 0100h | 000h-01Fh |
| PMM (see Table 17) | 0120h | 000h-00Fh |
| Flash Control (see Table 18) | 0140h | 000h-00Fh |
| CRC16 (see Table 19) | 0150h | 000h-007h |
| RAM Control (see Table 20) | 0158h | 000h-001h |
| Watchdog (see Table 21) | 015Ch | 000h-001h |
| UCS (see Table 22) | 0160h | 000h-01Fh |
| SYS (see Table 23) | 0180h | 000h-01Fh |
| Shared Reference (see Table 24) | 01B0h | 000h-001h |
| Port Mapping Control (see Table 25) | 01C0h | 000h-007h |
| Port Mapping Port P1 (see Table 26) | 01C8h | 000h-007h |
| Port Mapping Port P2 (see Table 27) | 01D0h | 000h-007h |
| Port Mapping Port P3 (see Table 28) | 01D8h | 000h-007h |
| Port P1, P2 (see Table 29) | 0200h | 000h-01Fh |
| Port P3 (see Table 30) | 0220h | 000h-01Fh |
| Port PJ (see Table 31) | 0320h | 000h-01Fh |
| TA0 (see Table 32) | 03C0h | 000h-03Fh |
| 32-Bit Hardware Multiplier (see Table 33) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 34) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 35) | 0500h | 010h-00Ah |
| DMA Channel 1 (see Table 36) | 0500h | 020h-00Ah |
| DMA Channel 2 (see Table 37) | 0500h | 030h-00Ah |
| USCI_A0 (see Table 38) | 05C0h | 000h-01Fh |
| USCI_B0 (see Table 38) | 05E0h | 000h-01Fh |
| ADC10_A (see Table 40) (MSP430F51x2 only) | 0740h | 000h-01Fh |
| Comparator_B (see Table 41) | 08C0h | 000h-00Fh |
| TD0 (see Table 42) | 0B00h | 000h-03Fh |
| TEC0 (see Table 44) | 0C00h | 000h-007h |
| TD1 (see Table 43) | 0B40h | 000h-03Fh |
| TEC1 (see Table 45) | 0C20h | 000h-007h |

Table 16. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 17. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|----------|--------|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high side control | SVSMHCTL | 04h |
| SVS low side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM Power Mode 5 control register 0 | PMM5CTL0 | 10h |

Table 18. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

Table 19. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC result | CRC16NIRE | 04h |

Table 20. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

Table 21. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 22. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

Table 23. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|----------|--------|
| System control | SYCTL | 00h |
| Bootstrap loader configuration area | SYBSLC | 02h |
| JTAG mailbox control | SYJMBC | 06h |
| JTAG mailbox input 0 | SYJMBIO | 08h |
| JTAG mailbox input 1 | SYJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYJMBO1 | 0Eh |
| Bus Error vector generator | SYBERRIV | 18h |
| User NMI vector generator | SYUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 24. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

Table 25. Port Mapping Controller (Base Address: 01C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port mapping password register | PMAPPWD | 00h |
| Port mapping control register | PMAPCTL | 02h |

Table 26. Port Mapper for Port P1 (Base Address: 01C8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P1.0 mapping register | P1MAP0 | 00h |
| Port P1.1 mapping register | P1MAP1 | 01h |
| Port P1.2 mapping register | P1MAP2 | 02h |
| Port P1.3 mapping register | P1MAP3 | 03h |
| Port P1.4 mapping register | P1MAP4 | 04h |
| Port P1.5 mapping register | P1MAP5 | 05h |
| Port P1.6 mapping register | P1MAP6 | 06h |
| Port P1.7 mapping register | P1MAP7 | 07h |

Table 27. Port Mapper for Port P2 (Base Address: 01D0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P2.0 mapping register | P2MAP0 | 00h |
| Port P2.1 mapping register | P2MAP2 | 01h |
| Port P2.2 mapping register | P2MAP2 | 02h |
| Port P2.3 mapping register | P2MAP3 | 03h |
| Port P2.4 mapping register | P2MAP4 | 04h |
| Port P2.5 mapping register | P2MAP5 | 05h |
| Port P2.6 mapping register | P2MAP6 | 06h |
| Port P2.7 mapping register | P2MAP7 | 07h |

Table 28. Port Mapper for Port P3 (Base Address: 01D8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P3.0 mapping register | P3MAP0 | 00h |
| Port P3.1 mapping register | P3MAP1 | 01h |
| Port P3.2 mapping register | P3MAP2 | 02h |
| Port P3.3 mapping register | P3MAP3 | 03h |
| Port P3.4 mapping register | P3MAP4 | 04h |
| Port P3.5 mapping register | P3MAP5 | 05h |
| Port P3.6 mapping register | P3MAP6 | 06h |
| Port P3.7 mapping register | P3MAP7 | 07h |

Table 29. Port Registers Port P1, P2 (Base Addresses: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 30. Port Registers P3 (Base Addresses: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |

Table 31. Port Registers PJ (Base Addresses: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |
| Port PJ selection | PJSEL | 0Ah |

Table 32. TA0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA0 control | TAOCTL | 00h |
| Capture/compare control 0 | TAOCTL0 | 02h |
| Capture/compare control 1 | TAOCTL1 | 04h |
| Capture/compare control 2 | TAOCTL2 | 06h |
| TA0 counter register | TAOR | 10h |
| Capture/compare register 0 | TAOCCR0 | 12h |
| Capture/compare register 1 | TAOCCR1 | 14h |
| Capture/compare register 2 | TAOCCR2 | 16h |
| TA0 expansion register 0 | TAOEX0 | 20h |
| TA0 interrupt vector | TAOIV | 2Eh |

Table 33. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

Table 34. DMA General Control (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

Table 35. DMA Channel 0 (Base Address: 0510h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |

Table 36. DMA Channel 1 (Base Address: 0520h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |

Table 37. DMA Channel 2 (Base Address: 0530h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |

Table 38. USCI0_A Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 0 | UCA0CTL0 | 01h |
| USCI control 1 | UCA0CTL1 | 00h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

Table 39. USCI0_B Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 0 | UCB0CTL0 | 00h |
| USCI synchronous control 1 | UCB0CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |
| USCI interrupt vector word | UCB0IV | 1Eh |

Table 40. ADC10_A Registers (MSP430F51x2 Devices Only) (Base Address: 0740h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|------------|--------|
| ADC10_A Control register 0 | ADC10CTL0 | 00h |
| ADC10_A Control register 1 | ADC10CTL1 | 02h |
| ADC10_A Control register 2 | ADC10CTL2 | 04h |
| ADC10_A Window Comparator Low Threshold | ADC10LO | 06h |
| ADC10_A Window Comparator High Threshold | ADC10HI | 08h |
| ADC10_A Memory Control Register 0 | ADC10MCTL0 | 0Ah |
| ADC10_A Conversion Memory Register | ADC10MEM0 | 12h |
| ADC10_A Interrupt Enable | ADC10IE | 1Ah |
| ADC10_A Interrupt Flags | ADC10IGH | 1Ch |
| ADC10_A Interrupt Vector Word | ADC10IV | 1Eh |

Table 41. Comparator_B Registers (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Comparator_B control register 0 | CBCTL0 | 00h |
| Comparator_B control register 1 | CBCTL1 | 02h |
| Comparator_B control register 2 | CBCTL2 | 04h |
| Comparator_B control register 3 | CBCTL3 | 06h |
| Comparator_B interrupt register | CBINT | 0Ch |
| Comparator_B interrupt vector word | CBIV | 0Eh |

Table 42. TD0 Registers (Base Address: 0B00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| TD0 Control 0 | TD0CTL0 | 00h |
| TD0 Control 1 | TD0CTL1 | 02h |
| TD0 Control 2 | TD0CTL2 | 04h |
| TD0 Counter Register | TD0R | 06h |
| Capture/compare control 0 | TD0CCTL0 | 08h |
| Capture/compare register 0 | TD0CCR0 | 0Ah |
| Capture/compare Latch 0 | TD0CL0 | 0Ch |
| Capture/compare control 1 | TD0CCTL1 | 0Eh |
| Capture/compare register 1 | TD0CCR1 | 10h |
| Capture/compare Latch 1 | TD0CL1 | 12h |
| Capture/compare control 2 | TD0CCTL2 | 14h |
| Capture/compare register 2 | TD0CCR2 | 16h |
| Capture/compare Latch 2 | TD0CL2 | 18h |
| TD0 High-Resolution Control 0 | TD0HCTL0 | 38h |
| TD0 High-Resolution Control 1 | TD0HCTL1 | 3Ah |
| TD0 High-Resolution Interrupt | TD0HINT | 3Ch |
| TD0 Interrupt Vector | TD0IV | 3Eh |

Table 43. TD1 Registers (Base Address: 0B40h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| TD1 Control 0 | TD1CTL0 | 00h |
| TD1 Control 1 | TD1CTL1 | 02h |
| TD1 Control 2 | TD1CTL2 | 04h |
| TD1 Counter Register | TD1R | 06h |
| Capture/compare control 0 | TD1CCTL0 | 08h |
| Capture/compare register 0 | TD1CCR0 | 0Ah |
| Capture/compare Latch 0 | TD1CL0 | 0Ch |
| Capture/compare control 1 | TD1CCTL1 | 0Eh |
| Capture/compare register 1 | TD1CCR1 | 10h |
| Capture/compare Latch 1 | TD1CL1 | 12h |
| Capture/compare control 2 | TD1CCTL2 | 14h |
| Capture/compare register 2 | TD1CCR2 | 16h |
| Capture/compare Latch 2 | TD1CL2 | 18h |
| TD1 High-Resolution Control 0 | TD1HCTL0 | 38h |
| TD1 High-Resolution Control 1 | TD1HCTL1 | 3Ah |
| TD1 High-Resolution Interrupt | TD1HINT | 3Ch |
| TD1 Interrupt Vector | TD1IV | 3Eh |

Table 44. TEC0 Registers (Base Address: 0C00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|----------|--------|
| Timer Event Control 0 External Control 0 | TECOCTL0 | 00h |
| Timer Event Control 0 External Control | TECOCTL1 | 02h |
| Timer Event Control 0 External Control | TECOCTL2 | 04h |
| Timer Event Control 0 Status | TECOSTA | 06h |
| Timer Event Control 0 External Interrupt | TECOXINT | 08h |
| Timer Event Control 0 External Interrupt Vector | TECOIV | 0Ah |

Table 45. TEC1 Registers (Base Address: 0C20h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|----------|--------|
| Timer Event Control 1 External Control 0 | TEC1CTL0 | 00h |
| Timer Event Control 1 External Control | TEC1CTL1 | 02h |
| Timer Event Control 1 External Control | TEC1CTL2 | 04h |
| Timer Event Control 1 Status | TEC1STA | 06h |
| Timer Event Control 1 External Interrupt | TEC1XINT | 08h |
| Timer Event Control 1 External Interrupt Vector | TEC1IV | 0Ah |

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------------------|
| Voltage V_{CC} applied at DVCC to DVSS | -0.3 V to 4.1 V |
| Voltage V_{IO} applied at VIO to DVSS | -0.3 V to 6.1 V |
| Voltage applied to any pin (excluding V _{CORE}) ⁽²⁾ | -0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device pin | ±2 mA |
| Storage temperature range, T_{stg} | -55°C to 150°C |
| Maximum operating junction temperature, T_J | 95°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . V_{CORE} is for internal device usage only. No external DC loading or voltage should be applied.

Thermal Packaging Characteristics

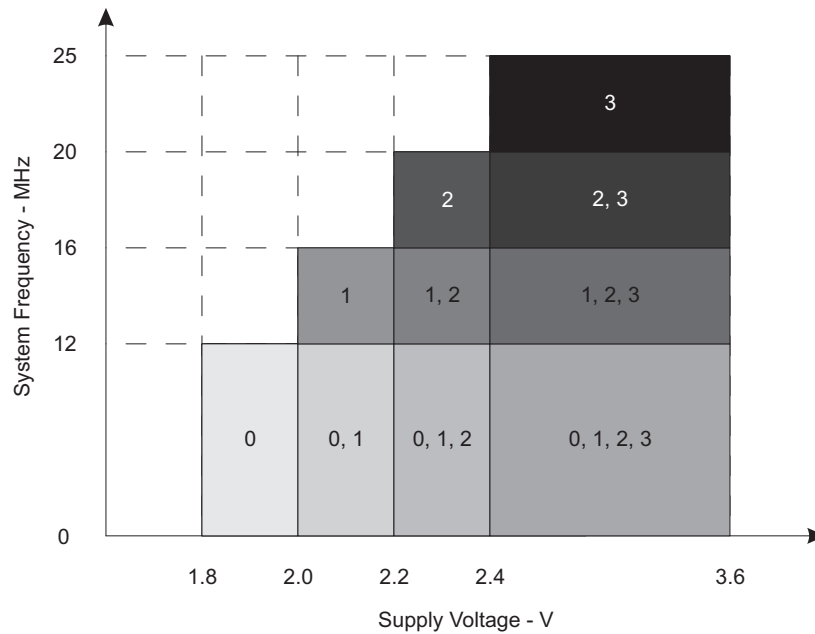
| | | | |
|---|-------------------------|------------|---------|
| θ_{JA} Junction-to-ambient thermal resistance, still air | Low-K board (JESD51-3) | QFN (RSB) | 87°C/W |
| | | TSSOP (DA) | 109°C/W |
| | High-K board (JESD51-7) | QFN (RSB) | 35°C/W |
| | | TSSOP (DA) | 69°C/W |
| θ_{JC} Junction-to-case thermal resistance | | QFN (RSB) | 36°C/W |
| | | TSSOP (DA) | 19°C/W |

Recommended Operating Conditions

Typical values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------------|--|---|--|-----|------|
| V_{CC} | Supply voltage during program execution and flash programming $V(AVCC) = V(DVCC) = V_{CC}^{(1)(2)}$ | PMMCOREVx = 0 | 1.8 | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2.0 | 3.6 | V |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | 3.6 | V |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | 3.6 | V |
| V_{IO} | Supply voltage of pins P1.6, P1.7, P2.0 to P2.7, P3.0, and P3.1 supplied by VIO ⁽³⁾ | 1.8 | 5.5 | V | |
| V_{SS} | Supply voltage $V(AVSS) = V(DVSS) = V_{SS}$ | | 0 | V | |
| T_A | Operating free-air temperature | -40 | | 85 | °C |
| T_J | Operating junction temperature | -40 | | 85 | °C |
| C(VCORE) | Recommended capacitor at VCORE | | 470 | | nF |
| C(DVCC)/ C(VCORE) | Capacitor ratio of DVCC to VCORE | 10 | | | |
| f_{SYSTEM} | Processor frequency (maximum MCLK frequency) ^{(4) (5)} (see Figure 1) | PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition) | 0 | 12 | MHz |
| | | PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V | 0 | 16 | |
| | | PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V | 0 | 20 | |
| | | PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V | 0 | 25 | |
| P_{INT} | Internal power dissipation | | $V_{CC} \times I(DVCC)$ | | W |
| P_{IO} | I/O power dissipation of the I/O pins powered by DVCC | | $(V_{CC} - V_{IOH}) \times I_{IOH} + V_{IOL} \times I_{IOL}$ | | W |
| P_{IO5} | I/O power dissipation of the I/O pins powered by VIO | | $(V_{IO} - V_{IOH5}) \times I_{IOH5} + V_{IOL5} \times I_{IOL5}$ | | W |
| P_{MAX} | Maximum allowed power dissipation, $P_{MAX} > P_{IO} + P_{IO5} + P_{INT}$ | | $(T_J - T_A)/\theta_{JA}$ | | W |

- (1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between V(AVCC) and V(DVCC) can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [PMM, SVS High Side](#) threshold parameters for the exact values and further details.
- (3) It is recommended to power DVCC and AVCC prior to DVIO. At DVCC and AVCC voltages higher than 1.8 V, the maximum difference of 0.3 V between DVIO and DVCC and AVCC can be exceeded.
- (4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
- (5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1. Frequency vs Supply Voltage

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMM CORE V_x | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|-----------------|------------------|----------|----------------|--|------|-------|------|--------|------|--------|-----|--------|------|------|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | 25 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}$ | Flash | 3 V | 0 | 0.24 | 0.27 | 1.48 | 1.60 | - | - | - | - | - | - | mA |
| | | | 1 | 0.26 | - | 1.66 | - | 2.48 | 2.7 | - | - | - | - | |
| | | | 2 | 0.28 | - | 1.83 | - | 2.72 | - | 4.50 | 4.8 | - | - | |
| | | | 3 | 0.28 | - | 1.83 | - | 2.66 | - | 4.40 | - | 5.60 | 6.15 | |
| $I_{AM, RAM}$ | RAM | 3 V | 0 | 0.17 | 0.2 | 0.89 | 0.97 | - | - | - | - | - | - | mA |
| | | | 1 | 0.18 | - | 1.00 | - | 1.49 | 1.62 | - | - | - | - | |
| | | | 2 | 0.20 | - | 1.14 | - | 1.68 | - | 2.75 | 3.0 | - | - | |
| | | | 3 | 0.20 | - | 1.20 | - | 1.78 | - | 2.92 | - | 3.64 | 4.0 | |

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMM CORE V_x | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|--|----------|----------------|-------|------|------|------|------|------|------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0, 1MHz}$ Low-power mode 0 | 2.2 V | 0 | 82 | 90 | 85 | 90 | 87 | 95 | 85 | 100 | μA |
| | 3 V | 3 | 88 | 100 | 85 | 100 | 90 | 104 | 88 | 104 | |
| I_{LPM2} Low-power mode 2 | 2.2 V | 0 | 10 | 12.5 | 10 | 12 | 10 | 12.5 | 12.5 | 13 | μA |
| | 3 V | 3 | 9 | 11.5 | 11 | 13 | 11 | 15 | 12 | 14 | |
| $I_{LPM3, XT1LF}$ Low-power mode 3, crystal mode | 2.2 V | 0 | 1.7 | - | 1.8 | 2.0 | 2.5 | - | 3.5 | 6.0 | μA |
| | 3 V | | 2.0 | - | 2.0 | 2.2 | 3.0 | - | 3.7 | 6.0 | |
| | 2.2 V | 1 | 1.8 | - | 1.9 | - | 2.5 | - | 4.0 | - | |
| | 3 V | | 2.1 | - | 2.2 | - | 2.5 | - | 4.0 | - | |
| | 2.2 V | 2 | 1.8 | - | 2.0 | - | 2.5 | - | 4.2 | - | |
| | 3 V | | 2.0 | - | 2.2 | - | 2.8 | - | 4.2 | - | |
| | 2.2 V | 3 | 1.9 | - | 2.0 | 2.5 | 2.9 | - | 4.8 | 6.5 | |
| | 3 V | | 2.1 | - | 2.2 | 2.5 | 3.0 | - | 5.2 | 7.0 | |
| $I_{LPM3, VLO}$ Low-power mode 3, VLO mode | 2.2 V | 0 | 1.0 | - | 1.0 | 1.25 | 1.6 | - | 3.5 | 4.5 | μA |
| | 3 V | | 1.1 | - | 1.2 | 1.4 | 1.5 | - | 3.6 | 5.0 | |
| | 2.2 V | 1 | 1.0 | - | 1.1 | - | 1.8 | - | 3.0 | - | |
| | 3 V | | 1.3 | - | 1.1 | - | 2.0 | - | 3.2 | - | |
| | 2.2 V | 2 | 1.1 | - | 1.1 | - | 1.8 | - | 3.1 | - | |
| | 3 V | | 1.1 | - | 1.2 | - | 2.0 | - | 3.2 | - | |
| | 2.2 V | 3 | 1.1 | - | 1.1 | 1.4 | 1.9 | - | 3.5 | 5.0 | |
| | 3 V | | 1.1 | - | 1.2 | 1.5 | 2.1 | - | 4.0 | 5.2 | |
| I_{LPM4} Low-power mode 4 | 3 V | 0 | 0.8 | - | 0.9 | 1.3 | 1.4 | - | 3.5 | 4.7 | μA |
| | | 1 | 0.8 | - | 1.0 | - | 1.4 | - | 3.5 | - | |
| | | 2 | 0.8 | - | 1.0 | - | 1.5 | - | 3.6 | - | |
| | | 3 | 0.9 | - | 1.0 | 1.3 | 1.6 | - | 3.6 | 5.0 | |
| $I_{LPM4.5}$ Low-power mode 4.5 | 2.2 V | x | 0.06 | - | 0.20 | 0.26 | 0.33 | - | 0.60 | 0.9 | μA |
| | 3 V | x | 0.07 | - | 0.25 | 0.29 | 0.37 | - | 0.77 | 0.9 | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. DVIO = DVCC = AVCC.

(2) The currents are characterized with a Micro Crystal MS1V-T1K SMD crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

Schmitt-Trigger Inputs – General Purpose I/O (P1.0 to P1.5, P3.2 to P3.7, and PJ.0 to PJ.6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 1.8 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

Schmitt-Trigger Inputs – General Purpose I/O (P1.6 and P1.7, P2.0 to P2.7, and P3.0 and P3.1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{IO} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.20 | | 2.00 | |
| | | | 5 V | 2.10 | | 2.50 | |
| V _{IT-} | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 0.90 | V |
| | | | 3 V | 0.75 | | 1.30 | |
| | | | 5 V | 1.10 | | 1.60 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 1.8 V | 0.27 | | 0.45 | V |
| | | | 3 V | 0.45 | | 0.65 | |
| | | | 5 V | 0.9 | | 1.2 | |
| R _{Pull} | Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

Inputs – Ports P1 and P2⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} or V _{IO} | MIN | MAX | UNIT |
|--------------------|---|------------------------------------|-----|-----|------|
| t _(int) | Port P1.0 to P1.5, External trigger pulse duration to set interrupt flag | 1.8 V to 3.6 V | 20 | | ns |
| | Port P1.6 and P1.7, and P2.0 to P2.7, External trigger pulse duration to set interrupt flag | 1.8 V to 5 V | 25 | | |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|-----------------|-----------------|-----|-----|-----|------|
| I _{lkg(Px.y)} | Port P1.0 to P1.5, P3.0 to P3.7, PJ.0 to PJ.6 | (1) (2) | 1.8 V to 3.6 V | | ±1 | ±50 | nA |
| | Port P1.6 and P1.7, P2.0 to P2.7 | | 1.8 V to 5 V | | ±1 | ±50 | |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Outputs – Ports P1 to P3, PJ (Full Drive Strength, P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|--|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = –3 mA ⁽¹⁾ | 1.8 V | V _{CC} – 0.25 | V _{CC} | V |
| | | I _(OHmax) = –10 mA ⁽²⁾ | | V _{CC} – 0.60 | V _{CC} | |
| | | I _(OHmax) = –5 mA ⁽¹⁾ | 3 V | V _{CC} – 0.25 | V _{CC} | |
| | | I _(OHmax) = –15 mA ⁽²⁾ | | V _{CC} – 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 3 mA ⁽¹⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 10 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 5 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 15 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – Ports P1 to P3 (Full Drive Strength, P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{IO} | MIN | MAX | UNIT |
|------------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH5} | High-level output voltage | I _(OH5max) = –3 mA ⁽¹⁾ | 1.8 V | V _{IO} – 0.25 | V _{CC} | V |
| | | I _(OH5max) = –10 mA ⁽²⁾ | | V _{IO} – 0.60 | V _{CC} | |
| | | I _(OH5max) = –5 mA ⁽¹⁾ | 3 V | V _{IO} – 0.25 | V _{CC} | |
| | | I _(OH5max) = –15 mA ⁽²⁾ | | V _{IO} – 0.60 | V _{CC} | |
| | | I _(OH5max) = –7 mA ⁽¹⁾ | 5 V | V _{IO} – 0.25 | V _{IO} | |
| | | I _(OH5max) = –20 mA ⁽²⁾ | | V _{IO} – 0.60 | V _{IO} | |
| V _{OL5} | Low-level output voltage | I _(OL5max) = 3 mA ⁽¹⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OL5max) = 10 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OL5max) = 5 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OL5max) = 15 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OL5max) = 7 mA ⁽¹⁾ | 5 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OL5max) = 20 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OH5max) and I_(OL5max), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OH5max) and I_(OL5max), for all outputs combined should not exceed ±200 mA to hold the maximum voltage drop specified.

Outputs – Ports P1 to P3, PJ (Reduced Drive Strength, P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6)

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = –1 mA ⁽²⁾ | 1.8 V | V _{CC} – 0.25 | V _{CC} | V |
| | | I _(OHmax) = –3 mA ⁽³⁾ | | V _{CC} – 0.60 | V _{CC} | |
| | | I _(OHmax) = –2 mA ⁽²⁾ | 3 V | V _{CC} – 0.25 | V _{CC} | |
| | | I _(OHmax) = –6 mA ⁽³⁾ | | V _{CC} – 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1 mA ⁽²⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 3 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 2 mA ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 6 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) Selecting reduced drive strength may reduce EMI.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – Ports P1 to P3 (Reduced Drive Strength, P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{IO} | MIN | MAX | UNIT |
|--|---|-----------------|------------------------|------------------------|------|
| V _{OH5} High-level output voltage | I _(OH5max) = -1 mA ⁽²⁾ | 1.8 V | V _{IO} - 0.25 | V _{CC} | V |
| | I _(OH5max) = -3 mA ⁽³⁾ | | V _{IO} - 0.60 | V _{CC} | |
| | I _(OH5max) = -2 mA ⁽²⁾ | 3 V | V _{IO} - 0.25 | V _{CC} | |
| | I _(OH5max) = -6 mA ⁽³⁾ | | V _{IO} - 0.60 | V _{CC} | |
| | I _(OH5max) = -4 mA ⁽²⁾ | 5.0 V | V _{IO} - 0.25 | V _{IO} | |
| | I _(OL5max) = -12 mA ⁽³⁾ | | V _{IO} - 0.60 | V _{IO} | |
| V _{OL5} Low-level output voltage | I _(OL5max) = 1 mA ⁽²⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | I _(OL5max) = 3 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | I _(OL5max) = 2 mA ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | I _(OL5max) = 6 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | I _(OH5max) = 4 mA ⁽²⁾ | 5.0 V | V _{SS} | V _{SS} + 0.25 | |
| | I _(OL5max) = 12 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) Selecting reduced drive strength may reduce EMI.
- (2) The maximum total current, I_(OH5max) and I_(OL5max), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I_(OH5max) and I_(OL5max), for all outputs combined, should not exceed ±200 mA to hold the maximum voltage drop specified.

Output Frequency – Ports P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|--|--|-----|------|
| f _{Px,y} Port output frequency (with load) | PJ.0/SMCLK C _L = 20 pF, R _L = 1 kΩ ^{(1) (2)} | V _{CC} = 1.8 V PMMCOREVx = 0 | 16 | MHz |
| | | V _{CC} = 3 V PMMCOREVx = 3 | 25 | |
| f _{Port_CLK} Clock output frequency | PJ.3/ACLK PJ.0/SMCLK PJ.1/MCLK C _L = 20 pF ⁽²⁾ | V _{CC} = 1.8 V PMMCOREVx = 0 | 16 | MHz |
| | | V _{CC} = 3 V PMMCOREVx = 3 | 25 | |

- (1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Output Frequency – Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|--|---|-----|------|
| f _{Px,y} Port output frequency (with load) | P1.6 port mapper SMCLK from P3.4 C _L = 20 pF, R _L = 1 kΩ ^{(1) (2)} | V _{CC} = 1.8 V, V _{IO} = 1.8 V PMMCOREVx = 0 | 16 | MHz |
| | | V _{CC} = 3 V, V _{IO} = 3 V PMMCOREVx = 3 | 25 | |
| | | V _{CC} = 3 V, V _{IO} = 5 V PMMCOREVx = 3 | 25 | |
| f _{Port_CLK} Clock output frequency | P1.6 port mapper SMCLK from P3.4 C _L = 20 pF ⁽²⁾ | V _{CC} = 1.8 V, V _{IO} = 1.8 V PMMCOREVx = 0 | 16 | MHz |
| | | V _{CC} = 3 V, V _{IO} = 3 V PMMCOREVx = 3 | 25 | |
| | | V _{CC} = 3 V, V _{IO} = 5 V PMMCOREVx = 3 | 25 | |

- (1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0), Ports P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

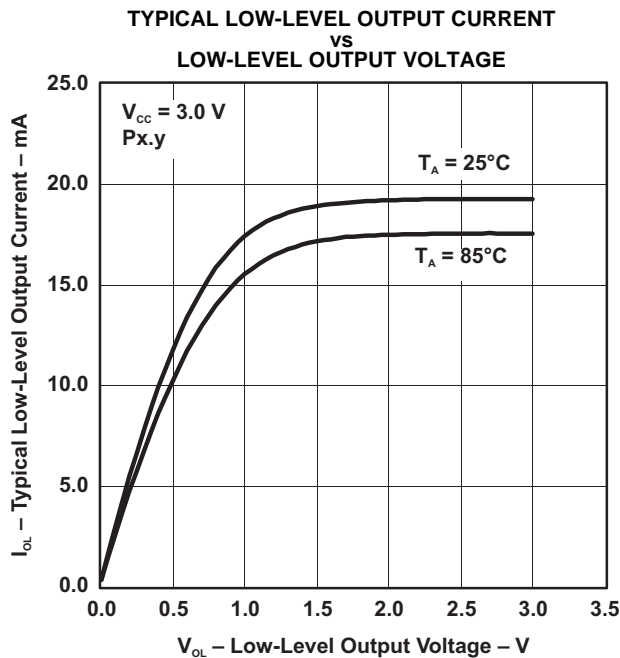


Figure 2.

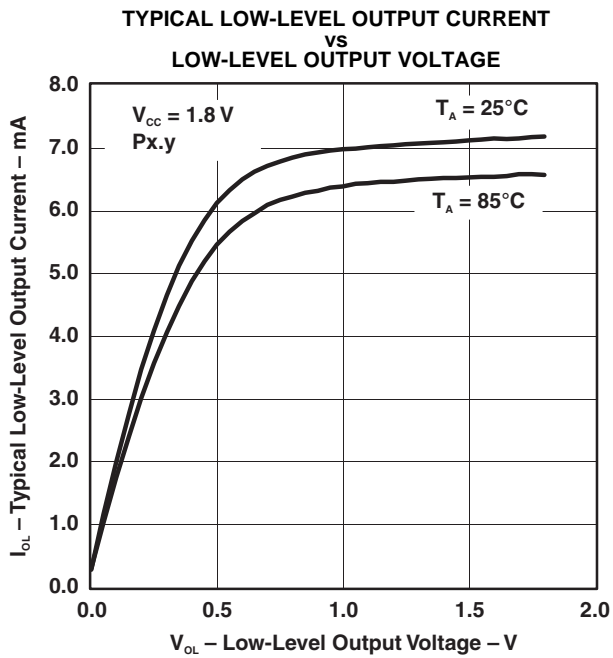


Figure 3.

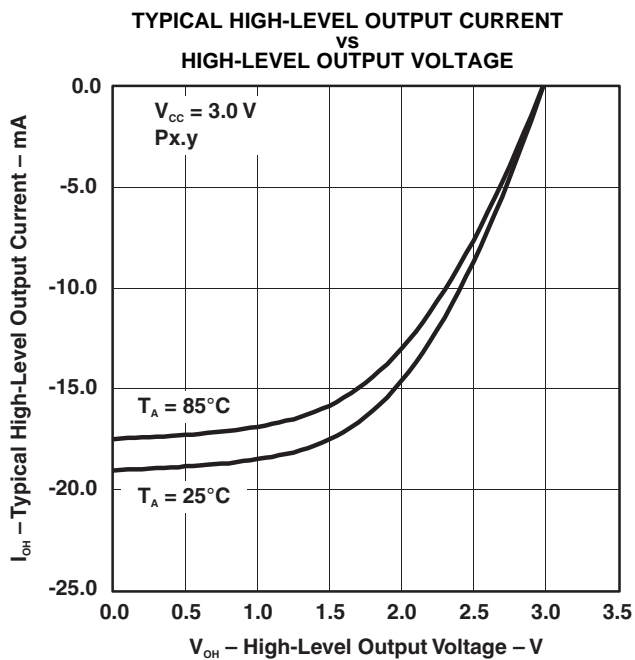


Figure 4.

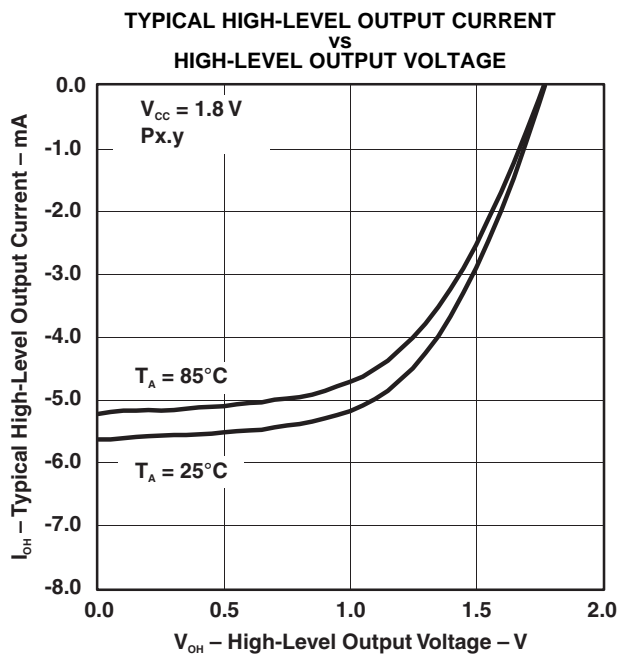


Figure 5.

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1), Ports P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

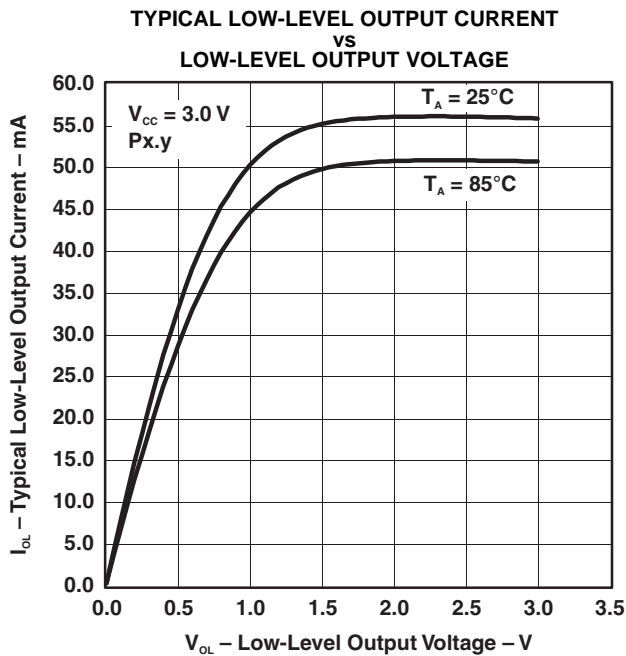


Figure 6.

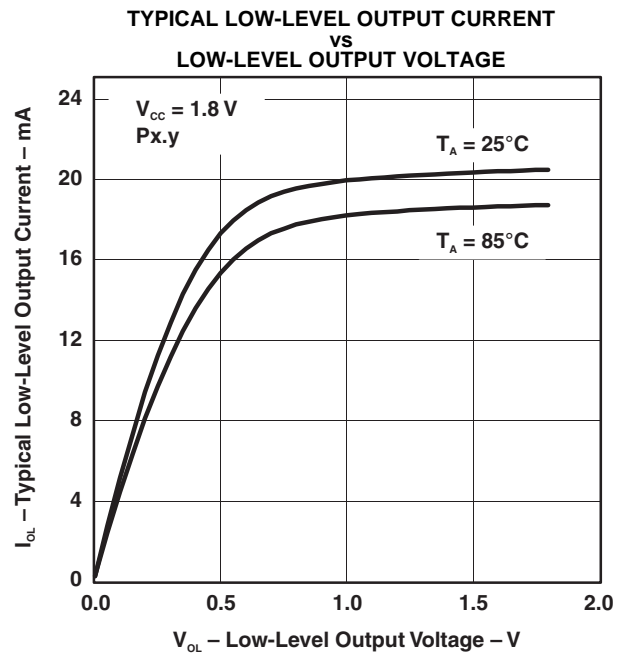


Figure 7.

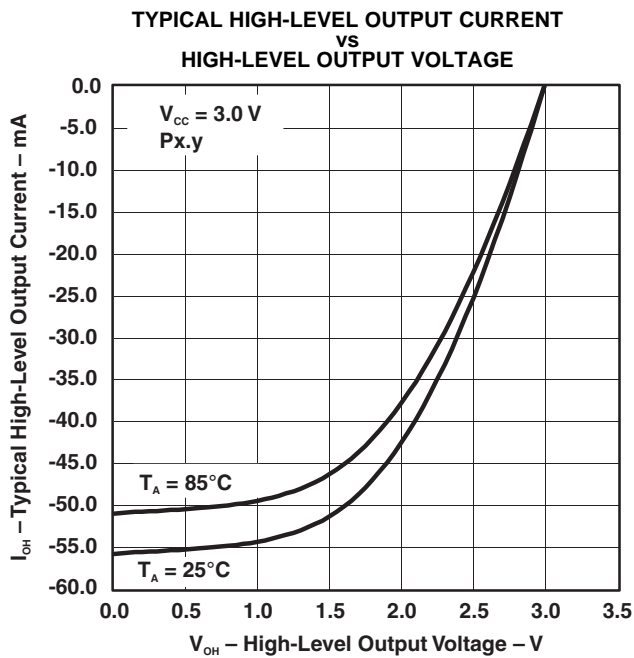


Figure 8.

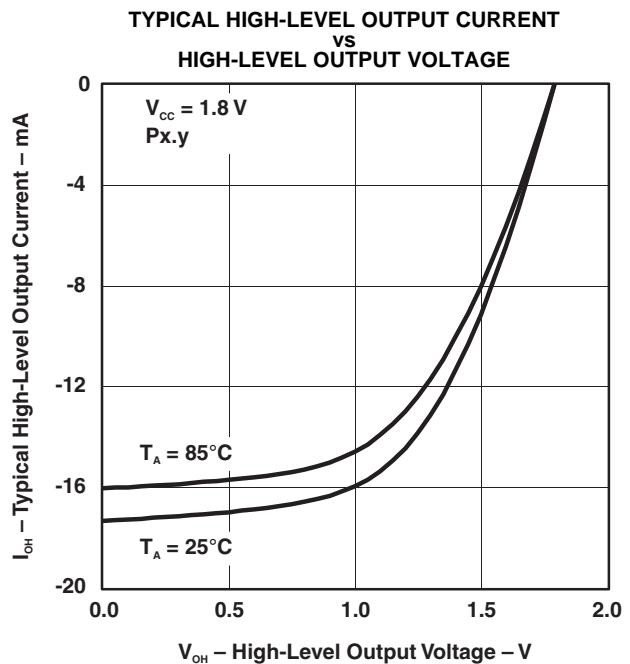


Figure 9.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

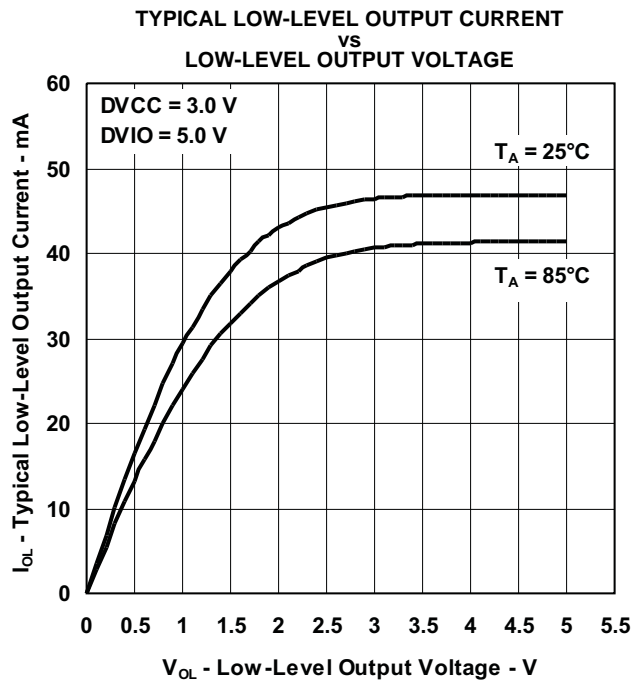


Figure 10.

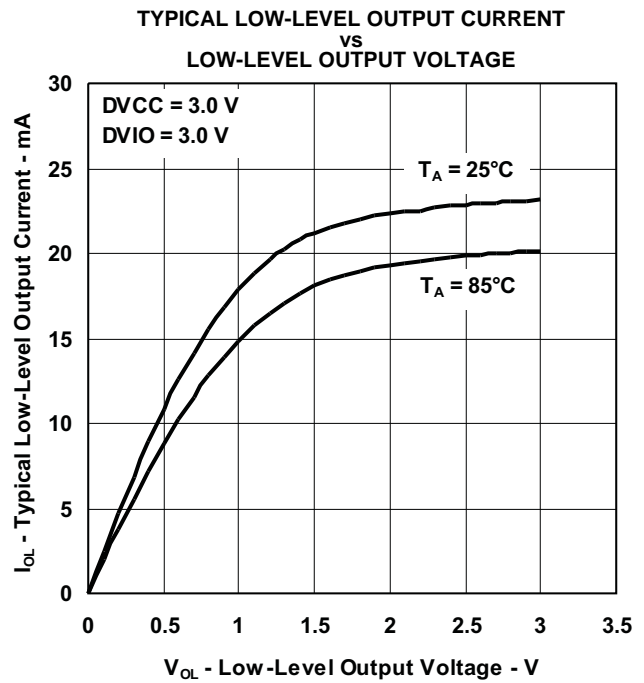


Figure 11.

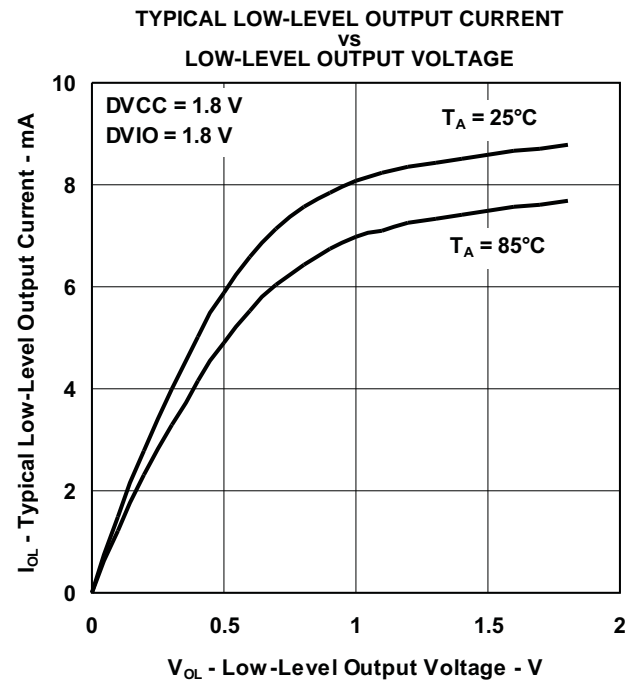


Figure 12.

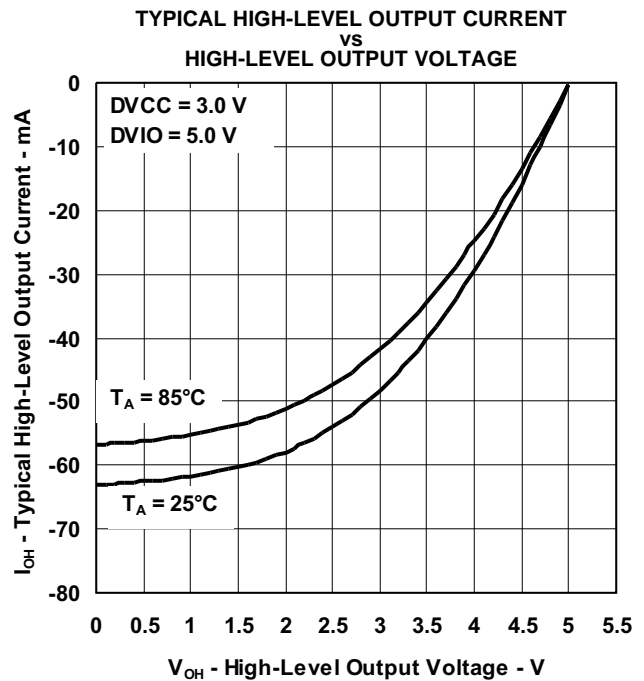


Figure 13.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

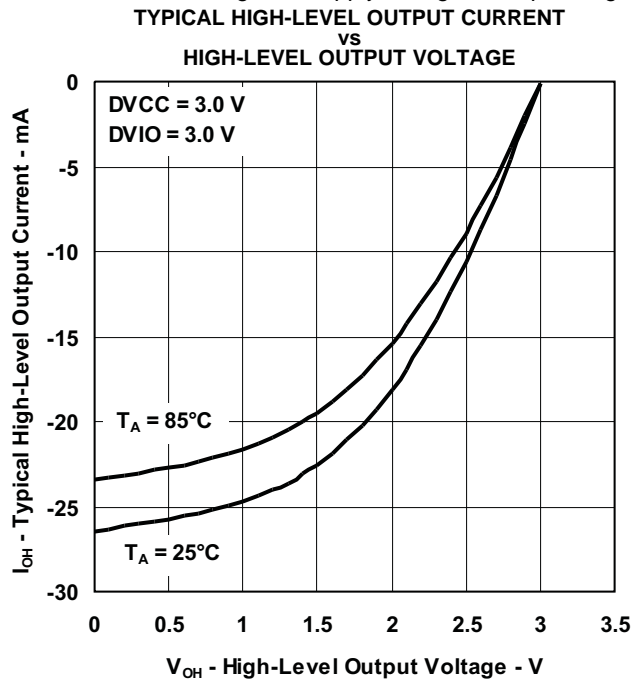


Figure 14.

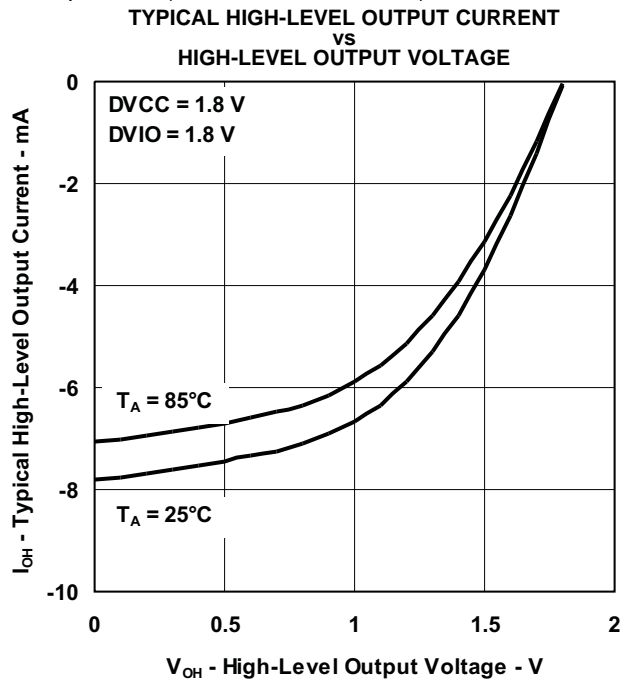


Figure 15.

Typical Characteristics – Outputs, Full Drive Strength ($P_{xDS.y} = 1$), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

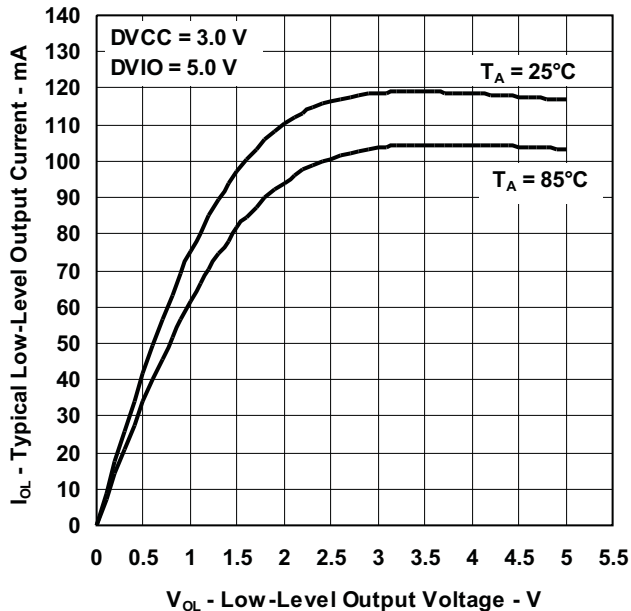


Figure 16.

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

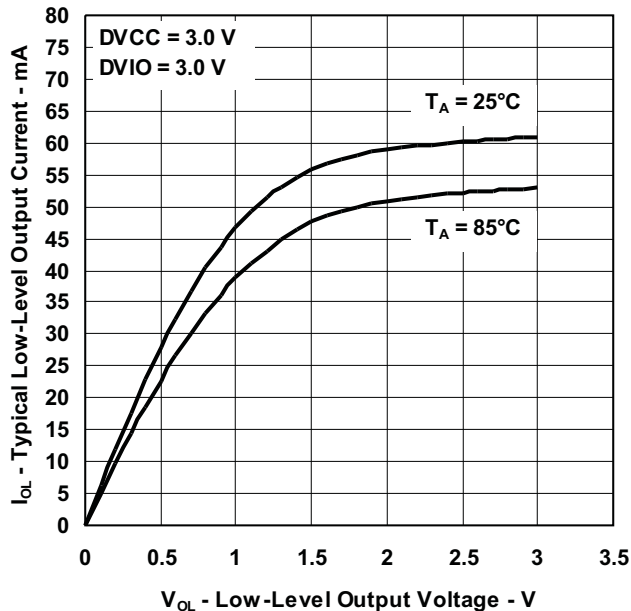


Figure 17.

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

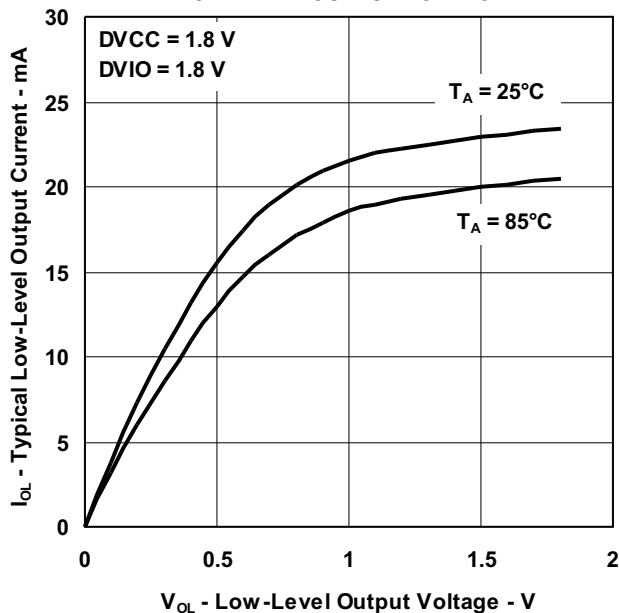


Figure 18.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

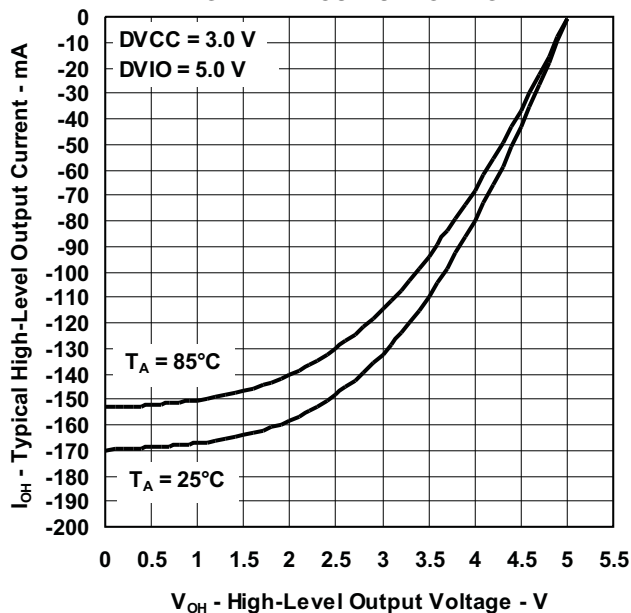


Figure 19.

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

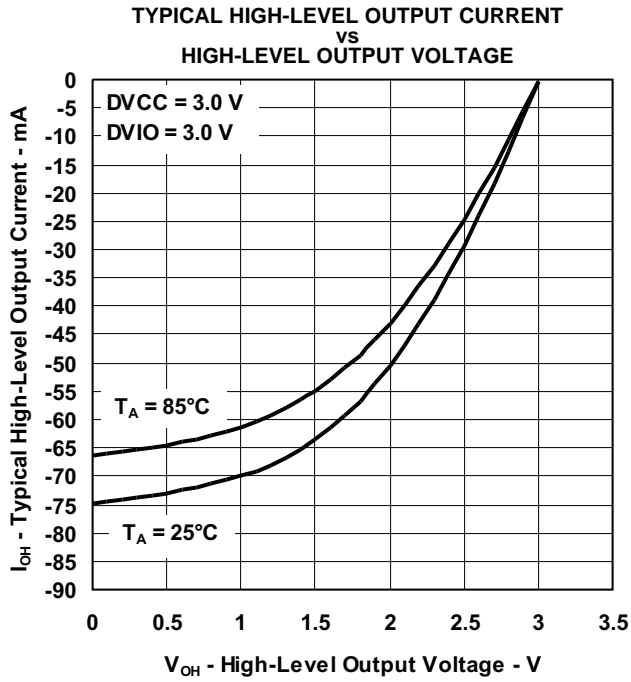


Figure 20.

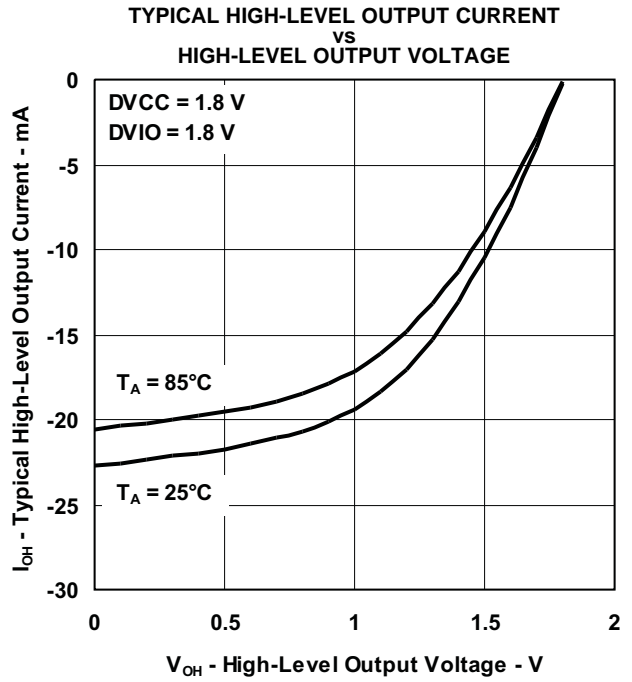


Figure 21.

Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|-----------------|-------|--------|-------|------|
| I _{DVCC,LF} | f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | 3 V | 0.075 | | | μA |
| | f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | 0.170 | | | |
| | f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | 0.290 | | | |
| f _{XT1,LF0} | XTS = 0, XT1BYPASS = 0 | | 32768 | | | Hz |
| f _{XT1,LF,SW} | XTS = 0, XT1BYPASS = 1 | | 10 | 32.768 | 50 | kHz |
| O _{A,LF} | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, f _{XT1,LF} = 32768 Hz, C _{L,eff} = 6 pF | | 210 | | | kΩ |
| | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, f _{XT1,LF} = 32768 Hz, C _{L,eff} = 12 pF | | 300 | | | |
| C _{L,eff} | XTS = 0, XCAP _x = 0 | | 2 | | | pF |
| | XTS = 0, XCAP _x = 1 | | 5.5 | | | |
| | XTS = 0, XCAP _x = 2 | | 8.5 | | | |
| | XTS = 0, XCAP _x = 3 | | 12.0 | | | |
| | Duty cycle, LF mode | | 30 | | 70 | % |
| f _{Fault,LF} | XTS = 0 | | 10 | | 10000 | Hz |
| t _{START,LF} | f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 12 pF | 3 V | 1000 | | | ms |
| | f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF | | 500 | | | |

Crystal Oscillator, XT1, High-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|---|-----------------|-----|-----|-----|------|
| I _{DVCC,HF} | Differential XT1 oscillator crystal current consumption from lowest drive setting, HF mode | f _{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C | 3 V | | 200 | | μA |
| | | f _{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | | | 260 | | |
| | | f _{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | | 325 | | |
| | | f _{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | | 450 | | |
| f _{XT1,HF0} | XT1 oscillator crystal frequency, HF mode 0 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 0 ⁽²⁾ | | 4 | | 8 | MHz |
| f _{XT1,HF1} | XT1 oscillator crystal frequency, HF mode 1 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 1 ⁽²⁾ | | 8 | | 16 | MHz |
| f _{XT1,HF2} | XT1 oscillator crystal frequency, HF mode 2 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 2 ⁽²⁾ | | 16 | | 24 | MHz |
| f _{XT1,HF3} | XT1 oscillator crystal frequency, HF mode 3 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 3 ⁽²⁾ | | 24 | | 32 | MHz |
| f _{XT1,HF,SW} | XT1 oscillator logic-level square-wave input frequency, HF mode | XTS = 1, XT1BYPASS = 1 ⁽³⁾ (2) | | 0.7 | | 32 | MHz |
| O _{AHF} | Oscillation allowance for HF crystals ⁽⁴⁾ | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 0, f _{XT1,HF} = 6 MHz, C _{L,eff} = 15 pF | | | 450 | | kΩ |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 1, f _{XT1,HF} = 12 MHz, C _{L,eff} = 15 pF | | | 320 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 2, f _{XT1,HF} = 20 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 3, f _{XT1,HF} = 32 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| t _{START,HF} | Startup time, HF mode | f _{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF | 3 V | | 0.5 | | ms |
| | | f _{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF | | | 0.3 | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ⁽⁵⁾ (6) | XTS = 1 | | | 1 | | pF |

- (1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
 - (a) Keep the traces between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) Maximum frequency of operation of the entire device cannot be exceeded.
- (3) When XT1BYPASS is set, the VLO, REFO, XT1 circuits are automatically powered down.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

Crystal Oscillator, XT1, High-Frequency Mode⁽¹⁾ (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----------------|-----|-----|-----|------|
| Duty cycle, HF mode | | XTS = 1, Measured at ACLK, f _{XT1,HF2} = 20 MHz | | 40 | 50 | 60 | % |
| f _{Fault,HF} | Oscillator fault frequency, HF mode ⁽⁷⁾ | XTS = 1 ⁽⁸⁾ | | 30 | | 300 | kHz |

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| Duty cycle | | Measured at ACLK | 1.8 V to 3.6 V | 40 | 50 | 60 | % |

(1) Calculated using the box method: (MAX(-40 to 85°C) MIN(-40 to 85°C)) / MIN(85°C (40°C)). The coefficient is negative.

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V 1.8 V). The coefficient is positive.

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5 | % |
| | | T _A = 25°C | 3 V | | | ±1.5 | % |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 1.0 | | %/V |
| Duty cycle | | Measured at ACLK | 1.8 V to 3.6 V | 40 | 50 | 60 | % |
| t _{START} | REFO startup time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

(1) Calculated using the box method: (MAX(-40 to 85°C) MIN(-40 to 85°C)) / MIN(85°C (40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V 1.8 V)

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|----------------------|--|--|------|------|-------|------|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) ⁽¹⁾ | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | 0.20 | MHz | |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) ⁽¹⁾ | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | 1.70 | MHz | |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) ⁽¹⁾ | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | 0.38 | MHz | |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) ⁽¹⁾ | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | 3.45 | MHz | |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) ⁽¹⁾ | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | 0.75 | MHz | |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) ⁽¹⁾ | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | 7.38 | MHz | |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) ⁽¹⁾ | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | 1.51 | MHz | |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) ⁽¹⁾ | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | 14.0 | MHz | |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) ⁽¹⁾ | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | 3.2 | MHz | |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) ⁽¹⁾ | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | 28.2 | MHz | |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) ⁽¹⁾ | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | 6.0 | MHz | |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) ⁽¹⁾ | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | 54.1 | MHz | |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) ⁽¹⁾ | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | 10.7 | MHz | |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) ⁽¹⁾ | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | 88.0 | MHz | |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) ⁽¹⁾ | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | 19.6 | MHz | |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) ⁽¹⁾ | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | 135 | MHz | |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$ | 1.2 | 2.4 | ratio | |
| S_{DCO} | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$ | 1.02 | 1.12 | ratio | |
| | Duty cycle | Measured at SMCLK | 40 | 50 | 60 | % |
| df_{DCO}/dT | DCO frequency temperature drift | $f_{DCO} = 1 \text{ MHz}$, $V_{CORE} = 1.2 \text{ V}/2.0 \text{ V}$ | | 0.1 | | %/°C |
| df_{DCO}/dV_{CORE} | DCO frequency voltage drift | $f_{DCO} = 1 \text{ MHz}$ | | 1.9 | | %/V |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

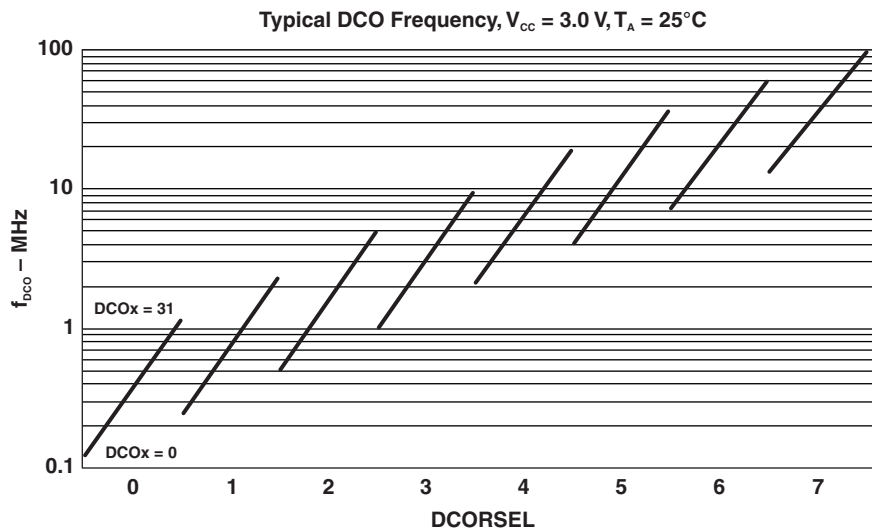


Figure 22. Typical DCO frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|-----------------------------------|------|------|------|------|
| $V_{(DVCC_BOR_IT-)}$ | BOR _H on voltage, DV _{CC} falling level | $dDV_{CC}/dt < 3 \text{ V/s}$ | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | BOR _H off voltage, DV _{CC} rising level | $dDV_{CC}/dt < 3 \text{ V/s}$ | 0.80 | 1.30 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | BOR _H hysteresis | | 40 | | 275 | mV |
| $V_{(VCORE_BOR_IT-)}$ | BOR _L on voltage, V _{CORE} falling level | DV _{CC} = 1.8 V to 3.6 V | 0.69 | | 0.87 | V |
| $V_{(VCORE_BOR_IT+)}$ | BOR _L off voltage, V _{CORE} rising level | DV _{CC} = 1.8 V to 3.6 V | 0.83 | | 1.05 | V |
| $V_{(VCORE_BOR_hys)}$ | BOR _L hysteresis | | 60 | | 200 | mV |
| t_{dBOR} | BOR _L reset release time | | | | 2000 | μs |
| t_{RESET} | Pulse duration required at $\overline{\text{RST/NMI}}$ pin to accept a reset | | 2 | | | μs |

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---|-----|------|-----|------|
| $V_{CORE3(AM)}$ | Core voltage, active mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ mA} \leq I(V_{CORE}) \leq 25 \text{ mA}$ | | 1.90 | | V |
| $V_{CORE2(AM)}$ | Core voltage, active mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ mA} \leq I(V_{CORE}) \leq 21 \text{ mA}$ | | 1.80 | | V |
| $V_{CORE1(AM)}$ | Core voltage, active mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ mA} \leq I(V_{CORE}) \leq 17 \text{ mA}$ | | 1.60 | | V |
| $V_{CORE0(AM)}$ | Core voltage, active mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ mA} \leq I(V_{CORE}) \leq 13 \text{ mA}$ | | 1.40 | | V |
| $V_{CORE3(LPM)}$ | Core voltage, active mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ mA} \leq I(V_{CORE}) \leq 30 \text{ μA}$ | | 1.94 | | V |
| $V_{CORE2(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ μA} \leq I(V_{CORE}) \leq 30 \text{ μA}$ | | 1.84 | | V |
| $V_{CORE1(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ μA} \leq I(V_{CORE}) \leq 30 \text{ μA}$ | | 1.64 | | V |
| $V_{CORE0(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}, 0 \text{ μA} \leq I(V_{CORE}) \leq 30 \text{ μA}$ | | 1.44 | | V |

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---------------------------------------|--|------|------|------|---------------|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC} = 3.6\text{ V}$ | 0 | | | nA |
| | | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 0 | 200 | | | nA |
| | | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 1 | 2 | | | μA |
| $V_{(SVSH_IT-)}$ | SVS _H on voltage level | SVSHE = 1, SVSHRVL = 0 | 1.59 | 1.64 | 1.69 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.79 | 1.84 | 1.91 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.98 | 2.04 | 2.11 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.10 | 2.16 | 2.23 | |
| $V_{(SVSH_IT+)}$ | SVS _H off voltage level | SVSHE = 1, SVSMHRRL = 0 | 1.62 | 1.74 | 1.81 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.88 | 1.94 | 2.01 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.07 | 2.14 | 2.21 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.20 | 2.26 | 2.33 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVSH)}$ | SVS _H propagation delay | SVSHE = 1, $dV_{DVCc}/dt = 10\text{ mV}/\mu\text{s}$, SVSHFP = 1 | 2.5 | | | μs |
| | | SVSHE = 1, $dV_{DVCc}/dt = \pm 1\text{ mV}/\mu\text{s}$, SVSHFP = 0 | 25 | | | |
| $t_{(SVSH)}$ | SVS _H on or off delay time | SVSHE = 0 -> 1 SVSHFP = 1 | 12.5 | | | μs |
| | | SVSHE = 0 -> 1 SVSHFP = 0 | 100 | | | |
| dV_{DVCc}/dt | DV_{CC} rise time | | 0 | 1000 | | V/s |

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|--|------|------|------|------|
| $I_{(SVMH)}$ | SVM _H current consumption | SVMHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0 | | 200 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1 | | 2.0 | | μA |
| $V_{(SVMH)}$ | SVM _H on or off voltage level | SVMHE = 1, SVSMHRRL = 0 | 1.65 | 1.74 | 1.86 | V |
| | | SVMHE = 1, SVSMHRRL = 1 | 1.85 | 1.94 | 2.02 | |
| | | SVMHE = 1, SVSMHRRL = 2 | 2.02 | 2.14 | 2.22 | |
| | | SVMHE = 1, SVSMHRRL = 3 | 2.18 | 2.26 | 2.35 | |
| | | SVMHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVMHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVMHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVMH)}$ | SVM _H propagation delay | SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 2.5 | | μs |
| | | SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 20 | | μs |
| $t_{(SVMH)}$ | SVM _H on or off delay time | SVMHE = 0 -> 1, SVSHFP = 1 | | 12.5 | | μs |
| | | SVMHE = 0 -> 1, SVSHFP = 0 | | 100 | | |

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVSL)}$ | SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 2.0 | | μA |
| $t_{(SVSL)}$ | SVS _L on or off delay time | SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 6 | | μs |
| | | SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 50 | | |
| $t_{pd(SVSL)}$ | SVS _L propagation delay | SVMHE = 0 -> 1, SVSLFP = 1 | | 12.5 | | μs |
| | | SVMHE = 0 -> 1, SVSLFP = 0 | | 100 | | |

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------------------|---|-----|------|-----|------|
| $I_{(SVM_L)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVM_LFP = 0 | | 200 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVM_LFP = 1 | | 2.0 | | μA |
| $t_{pd(SVM_L)}$ | SVM _L propagation delay | SVMLE = 1, dV _{CORE} /dt = 10 mV/μs, SVM_LFP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, dV _{CORE} /dt = 1 mV/μs, SVM_LFP = 0 | | 30 | | |
| $t_{(SVM_L)}$ | SVM _L on or off delay time | SVMLE = 0 -> 1, SVSLFP = 1 | | 12.5 | | μs |
| | | SVMLE = 0 -> 1, SVSLFP = 0 | | 100 | | |

Wake-Up From Low-Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|---|-----------------------------------|-----|-----|------|
| t _{FAST-WAKE-UP} | Wake-up time from LPM2, LPM3, or LPM4 to active mode | PMMCOREV _x = 0 = SVSMLRRL _x = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | f _{MCLK} ≥ 4 MHz | 3 | 6.5 | μs |
| | | | 1 MHz < f _{MCLK} < 4 MHz | 4 | 8.0 | |
| t _{SLOW-WAKE-UP} | Wake-up time from LPM2, LPM3, or LPM4 to active mode | PMMCOREV _x = 0 = SVSMLRRL _x = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 165 | μs |
| t _{WAKE-UP LPM5} | Wake-up time from LPM4.5 to active mode | | | 2 | 3 | ms |
| t _{WAKE-UP-RESET} | Wake-up time from RST or BOR event to active mode | | | 2 | 3 | ms |

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|---|-----------------|-----|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10% | 1.8 V, 3 V | | | 25 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs. Minimum pulse duration required for capture. | 1.8 V, 3 V | 20 | | | ns |

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|---|---|-----------------|-----|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10% | | | | f _{SYSTEM} | MHz |
| f _{max,BITCLK} | Maximum BITCLK clock frequency (equals baud rate in MBaud) ⁽¹⁾ | | | 1 | | | MHz |
| t _r | UART receive deglitch time | | 2.2 V | 50 | 150 | 200 | ns |
| | | | 3 V | 50 | 150 | 200 | |

(1) The DCO wake-up time must be considered in LPM3/4. The wake-up time must be considered in LPMx.5.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 23](#) and [Figure 24](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|-----------------------------|--|-----------------|-----|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | SMCLK, ACLK Duty cycle = 50% ± 10% | | | | f _{SYSTEM} | MHz |
| t _{SU,MI} | SOMI input data setup time | PMMCOREV = 0 | 1.8 V | 55 | | | ns |
| | | | 3 V | 38 | | | |
| | | PMMCOREV = 3 | 2.4 V | 30 | | | |
| | | | 3 V | 25 | | | |
| t _{HD,MI} | SOMI input data hold time | PMMCOREV = 0 | 1.8 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| | | PMMCOREV = 3 | 2.4 V | 0 | | | |
| | | | 3 V | 0 | | | |
| t _{VALID,MO} | SIMO output data valid time | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | | | 20 | ns |
| | | | 3 V | | | 18 | |
| | | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | | | 16 | |
| | | | 3 V | | | 15 | |
| t _{HD,MO} | SIMO output data hold time | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | -10 | | | ns |
| | | | 3 V | -8 | | | |
| | | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | -10 | | | ns |
| | | | 3 V | -8 | | | |

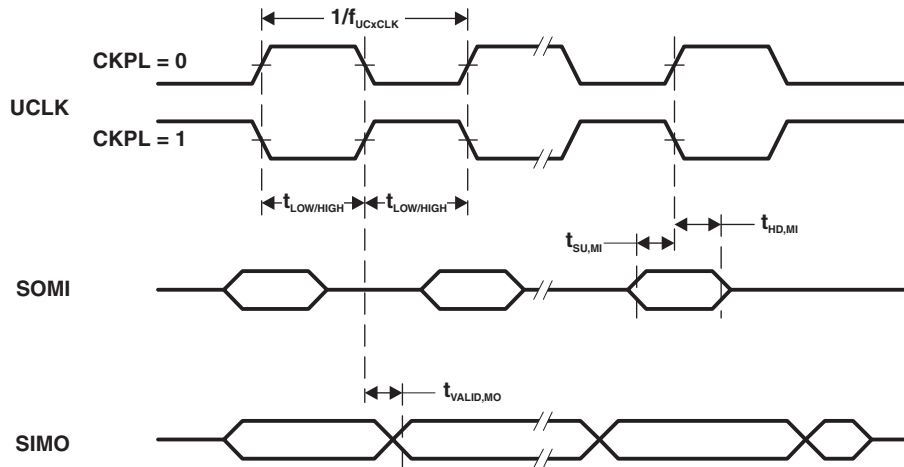


Figure 23. SPI Master Mode, CKPH = 0

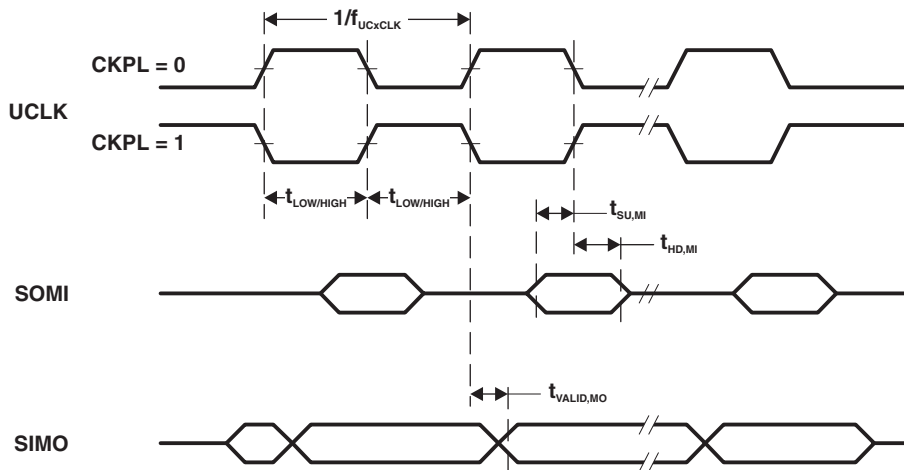


Figure 24. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 25](#) and [Figure 26](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | PMMCOREV = 0 | 1.8 V | 11 | | | ns |
| | | | 3 V | 8 | | | |
| | | PMMCOREV = 3 | 2.4 V | 7 | | | ns |
| | | | 3 V | 6 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE high | PMMCOREV = 0 | 1.8 V | 3 | | | ns |
| | | | 3 V | 3 | | | |
| | | PMMCOREV = 3 | 2.4 V | 3 | | | ns |
| | | | 3 V | 3 | | | |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | PMMCOREV = 0 | 1.8 V | | | 66 | ns |
| | | | 3 V | | | 50 | |
| | | PMMCOREV = 3 | 2.4 V | | | 36 | ns |
| | | | 3 V | | | 30 | |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | PMMCOREV = 0 | 1.8 V | | | 30 | ns |
| | | | 3 V | | | 23 | |
| | | PMMCOREV = 3 | 2.4 V | | | 16 | ns |
| | | | 3 V | | | 13 | |
| t _{SU,SI} | SIMO input data setup time | PMMCOREV = 0 | 1.8 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| | | PMMCOREV = 3 | 2.4 V | 2 | | | ns |
| | | | 3 V | 2 | | | |
| t _{HD,SI} | SIMO input data hold time | PMMCOREV = 0 | 1.8 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| | | PMMCOREV = 3 | 2.4 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| t _{VALID,SO} | SOMI output data valid time | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | | | 76 | ns |
| | | | 3 V | | | 60 | |
| | | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | | | 44 | ns |
| | | | 3 V | | | 40 | |
| t _{HD,SO} | SOMI output data hold time | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 18 | | | ns |
| | | | 3 V | 12 | | | |
| | | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 10 | | | ns |
| | | | 3 V | 8 | | | |

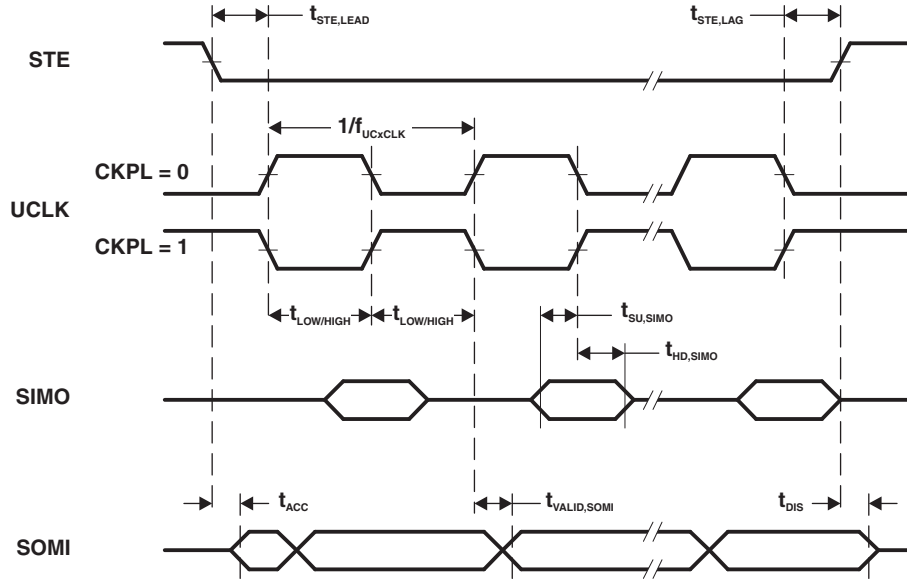


Figure 25. SPI Slave Mode, CKPH = 0

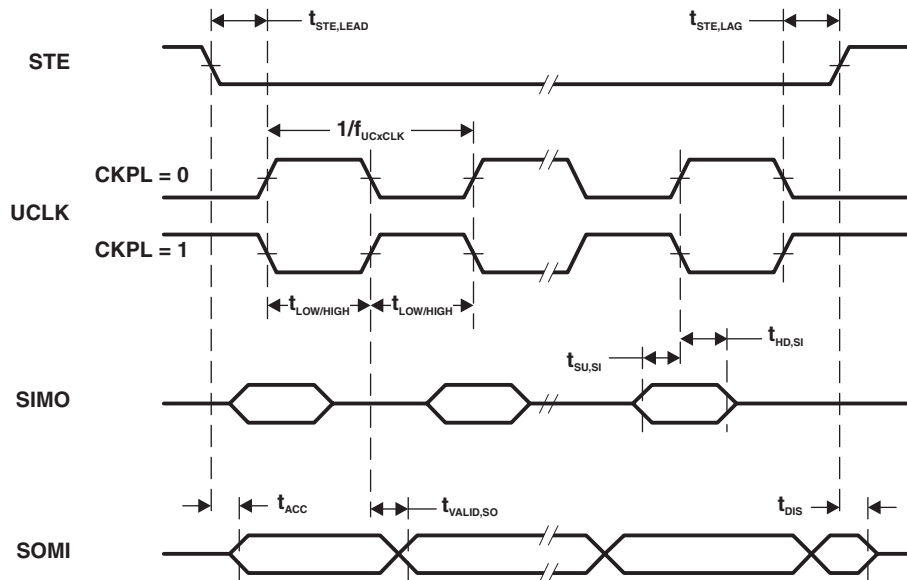


Figure 26. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 27](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|--|------------|------------|---------------------|------|
| f _{USCI} | USCI input clock frequency | | | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | 2.2 V, 3 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.0 0.6 | | μs |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.7 0.6 | | μs |
| t _{HD,DAT} | Data hold time | | 2.2 V, 3 V | 0 | | ns |
| t _{SU,DAT} | Data setup time | | 2.2 V, 3 V | 250 | | ns |
| t _{SU,STO} | Setup time for STOP | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.0 0.6 | | μs |
| t _{SP} | Pulse duration of spikes suppressed by input filter | 2.2 V 3 V | 50 | | 600 | ns |

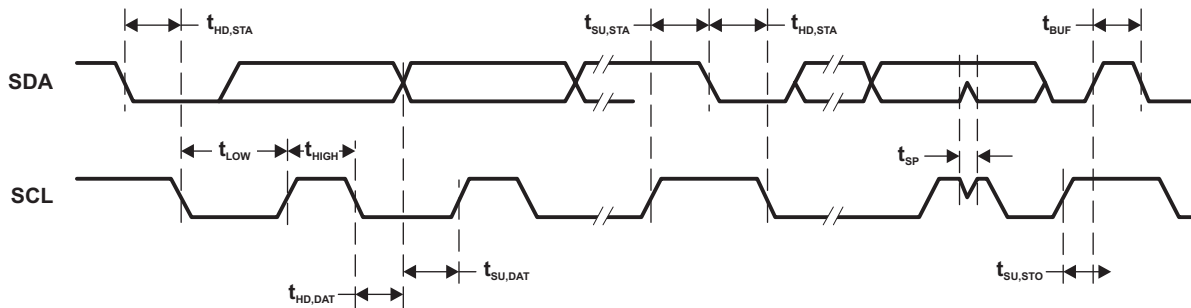


Figure 27. I2C Mode Timing

10-Bit ADC, Power Supply and Input Range Conditions (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 1.8 | | 3.6 | V |
| V _(Ax) | Analog input voltage range ⁽²⁾ | All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals | | 0 | | AV _{CC} | V |
| I _{ADC10_A} | Operating supply current into AV _{CC} terminal, REF module and reference buffer off | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 60 | 90 | μA |
| | | | 3 V | | 75 | 100 | |
| | Operating supply current into AV _{CC} terminal, REF module on, reference buffer on | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 113 | 130 | μA |
| | | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VREF = 2.5 V | 3 V | | 105 | 125 | μA |
| Operating supply current into AV _{CC} terminal, REF module off, reference buffer off | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VREF = 2.5 V | 3 V | | 70 | 95 | μA | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| R _I | Input MUX ON resistance | AV _{CC} > 2.0V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 36 | kΩ |
| | | 1.8V < AV _{CC} < 2.0V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 96 | |

- (1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
 (2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. See ⁰.

10-Bit ADC, Timing Parameters (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|------|-----|-----|------|
| f _{ADC10CLK} | | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADC10OSC} | Internal ADC10_A oscillator ⁽¹⁾ | ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 4.2 | 4.8 | 5.4 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode f _{ADC10OSC} = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | μs |
| | | External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0 | | | (2) | | |
| t _{ADC10ON} | Turn on settling time of the ADC | See ⁽³⁾ | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 96 kΩ, C _I = 3.5 pF ⁽⁴⁾ | 1.8 V | 3 | | | μs |
| | | R _S = 1000 Ω, R _I = 36 kΩ, C _I = 3.5 pF ⁽⁴⁾ | 3 V | 1 | | | μs |

- (1) The ADC10OSC is sourced directly from MODOSC inside the UCS.
 (2) 12 × ADC10DIV × 1/f_{ADC10CLK}
 (3) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.
 (4) Approximately eight Tau (τ) are needed to get an error of less than ±0.5 LSB

10-Bit ADC, Linearity Parameters (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|--|--|-----------------|-----|------|-------|------|
| E _I | Integral linearity error | 1.4 V ≤ (VEREF+ – VREF-)min ≤ 1.6 V | | | | ±1.0 | LSB |
| | | 1.6 V < (VEREF+ – VREF-)min ≤ V _{AVCC} | | | | ±1.0 | |
| E _D | Differential linearity error | (VEREF+ – VREF-)min ≤ (VEREF+ – VREF-), C _{VEREF+} = 20 pF | | | | ±1.0 | LSB |
| E _O | Offset error | (VEREF+ – VREF-)min ≤ (VEREF+ – VREF-), Internal impedance of source R _S < 100 Ω, C _{VEREF+} = 20 pF | | | | ±1.0 | LSB |
| E _G | Gain error, external reference | (VEREF+ – VREF-)min ≤ (VEREF+ – VREF-), C _{VEREF+} = 20 pF | | | | ±1.0 | LSB |
| | Gain error, external reference, buffered | | | | | ±1.5 | |
| | Gain error, internal reference | See (1) | | | | ±1.5% | VREF |
| E _T | Total unadjusted error, external buffered and unbuffered reference | (VEREF+ – VREF-)min ≤ (VEREF+ – VREF-), C _{VEREF+} = 20 pF | | | ±1.0 | ±2.0 | LSB |
| | Total unadjusted error, internal reference | See (1) | | | | ±1.5% | VREF |

(1) Dominated by the absolute voltage of the integrated reference voltage.

REF, External Reference (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|---|-----------------|-----|------|-----------------|------|
| VEREF+ | Positive external reference voltage input | VEREF+ > VREF- (2) | | 1.4 | | V _{CC} | V |
| VEREF- | Negative external reference voltage input | VEREF+ > VREF- (3) | | 0 | | 1.2 | V |
| VEREF+ – VREF- | Differential external reference voltage input | VEREF+ > VREF- (4) | | 1.4 | | V _{CC} | V |
| I _(VEREF+) I _(VEREF-) | Static input current | 1.4 V ≤ VREF+ ≤ V(AVCC), VREF- = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate 200 ksps | 2.2 V, 3 V | | ±8.5 | ±26 | μA |
| | | 1.4 V ≤ VREF+ ≤ V(AVCC), VREF- = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 ksps | 2.2 V, 3 V | | | ±1 | μA |
| C _(VEREF+/-) | Capacitance at VREF+/- terminal | See (5) | | 10 | | | μF |

- The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

REF, Built-In Reference (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------------|---|--------------------------------|------|------|-------|------------|
| V _{REF+} | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | | 2.51 | ±1.5% | V |
| | REFVSEL = {1} for 2.0 V, REFON = 1 | 3 V | | 1.99 | ±1.5% | |
| | REFVSEL = {0} for 1.5 V, REFON = 1 | 2.2 V, 3 V | | 1.5 | ±1.5% | |
| AV _{CC(min)} | REFVSEL = {0} for 1.5 V | | 1.8 | | | V |
| | REFVSEL = {1} for 2.0 V | | 2.3 | | | |
| | REFVSEL = {2} for 2.5 V | | 2.8 | | | |
| I _{REF+} | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | 3 V | | 15.5 | 19 | μA |
| | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V | 3 V | | 18 | 24 | μA |
| | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 21 | 30 | μA |
| TC _{REF+} | REFVSEL = (0, 1, 2), REFON = 1 | | | 30 | 50 | ppm/ °C |
| I _{SENSOR} | REFON = 1, INCH = 0Ah, ADC10ON = 1, T _A = 30°C | 2.2 V | | 150 | 180 | μA |
| | | 3 V | | 150 | 190 | |
| V _{SENSOR} | REFON = 1, INCH = 0Ah, ADC10ON = 1, T _A = 30°C | 2.2 V | | 765 | | mV |
| | | 3 V | | 765 | | |
| V _{MID} | ADC10ON = 1, INCH = 0Bh, V _{MID} is approximately 0.5 × V _{AVCC} | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | 3 V | 1.46 | 1.5 | 1.54 | |
| t _{SENSOR (sample)} | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | 30 | | | μs |
| t _{VMID (sample)} | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | 1 | | | μs |
| PSRR _{DC} | AV _{CC} = AV _{CC (min)} - AV _{CC(max)} , T _A = 25°C, REFVSEL = (0, 1, 2), REFON = 1 | | | 120 | 300 | μV/V |
| PSRR _{AC} | AV _{CC} = AV _{CC (min)} - AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = (0, 1, 2), REFON = 1 | | | 6.4 | | mV/V |
| t _{SETTLE} | AV _{CC} = AV _{CC (min)} - AV _{CC(max)} , REFVSEL = (0, 1, 2), REFON = 0 → 1 | T _A = -40°C to 85°C | | 23 | 125 | μs |
| | | T _A = 25°C | | 23 | 50 | |
| | | T _A = 85°C | | 16 | 25 | |

- (1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
- (2) The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
- (3) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C - (-40°C)).
- (4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
- (5) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
- (6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
- (7) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.
- (8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|------------------------|---|---|-----------------|------|------------------------------------|----------------------------------|------------------------------------|---|
| V _{CC} | Supply voltage | | | 1.8 | | 3.6 | V | |
| I _{AVCC_COMP} | Comparator operating supply current into AVCC, Excludes reference resistor ladder | CBPWRMD = 00, CBON = 1, CBRSx = 00 | 1.8 V | | | 38 | μA | |
| | | | 2.2 V | | 31 | 38 | | |
| | | | 3 V | | 32 | 39 | | |
| | | 2.2 V, 3 V | | 10 | 17 | | | |
| | | CBPWRMD = 10, CBON = 1, CBRSx = 00 | 2.2 V, 3 V | | 0.2 | 0.85 | | |
| V _{REF} | Reference voltage level | CBREFLx = 01, CBREFACC = 0 | ≥1.8 V | | 1.5 | ±1.5% | V | |
| | | CBREFLx = 10, CBREFACC = 0 | ≥2.2 V | | 2.0 | ±1.5% | | |
| | | CBREFLx = 11, CBREFACC = 0 | ≥3.0 V | | 2.5 | ±1.5% | | |
| I _{AVCC_REF} | Quiescent current of resistor ladder into AVCC, Including REF module current | CBREFACC = 0, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | | 10 | 17 | μA | |
| | | CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | | 33 | 40 | μA | |
| V _{IC} | Common mode input range | | | 0 | | V _{CC} -1 | V | |
| V _{OFFSET} | Input offset voltage | CBPWRMD = 00 | | | | ±20 | mV | |
| | | CBPWRMD = 01, 10 | | | | ±10 | mV | |
| C _{IN} | Input capacitance | | | | 5 | | pF | |
| R _{SIN} | Series input resistance | ON - switch closed | | | 3 | 4 | kΩ | |
| | | OFF - switch opened | | 50 | | | MΩ | |
| t _{PD} | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | | 450 | ns | |
| | | CBPWRMD = 01, CBF = 0 | | | | 600 | ns | |
| | | CBPWRMD = 10, CBF = 0 | | | | 50 | μs | |
| t _{PD,filter} | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 00 | | 0.35 | 0.6 | 1.5 | μs | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 01 | | 0.6 | 1.0 | 1.8 | μs | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 10 | | 1.0 | 1.8 | 3.4 | μs | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 11 | | 1.8 | 3.4 | 6.5 | μs | |
| t _{EN_CMP} | Comparator enable time | CBON = 0 to CBON = 1, CBPWRMD = 00, 01 | | | 1 | 2 | μs | |
| | | CBON = 0 to CBON = 1, CBPWRMD = 10 | | | | 1.5 | μs | |
| t _{EN_REF} | Resistor reference enable time | CBON = 0 to CBON = 1 | | | 1.0 | 1.5 | μs | |
| T _{CB_REF} | Temperature coefficient reference of V _{CB_REF} | | | | | 50 | ppm/°C | |
| V _{CB_REF} | Reference voltage for a given tap | V _{IN} = reference into resistor ladder, n = 0 to 31 | | | $\frac{V_{IN} \times (n+0.5)}{32}$ | $\frac{V_{IN} \times (n+1)}{32}$ | $\frac{V_{IN} \times (n+1.5)}{32}$ | V |

Timer_D, Power Supply and Reference Clock Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|---|---------------------------------|-----|-----|------|------|
| DV _{CC} | Digital supply voltage | V _(DVSS) = 0 V | | 1.8 | | 3.6 | V |
| f _{REF,DCO} | Timer_D input reference clock frequency | PMMCOREV _x = 0 | 1.8 V ≤ V _{CC} ≤ 3.6 V | 8 | | 12.0 | MHz |
| | | PMMCOREV _x = 1 | 2.0 V ≤ V _{CC} ≤ 3.6 V | 8 | | 16.0 | |
| | | PMMCOREV _x = 2 | 2.2 V ≤ V _{CC} ≤ 3.6 V | 8 | | 20.0 | |
| | | PMMCOREV _x = 3 | 2.4 V ≤ V _{CC} ≤ 3.6 V | 8 | | 25.5 | |
| I _(64MHz) | I _(DVCC) at 64-MHz Timer_D clock, clock generator only | f _{reference} = 8 MHz, MC _x = 0, TDHREGEN = 1, TDHM _x = 0, TDHCLKCR = 0 | | | 253 | 320 | μA |
| I _(128MHz) | I _(DVCC) at 128-MHz Timer_D clock, clock generator only | f _{reference} = 16 MHz, MC _x = 0, TDHREGEN = 1, TDHM _x = 0, TDHCLKCR = 0 | | | 285 | 360 | μA |
| I _(200MHz) | I _(DVCC) at 200-MHz Timer_D clock, clock generator only | f _{reference} = 25 MHz, MC _x = 0, TDHREGEN = 1, TDHM _x = 0, TDHCLKCR = 1 | | | 280 | 345 | μA |
| I _(256MHz) | I _(DVCC) at 256-MHz Timer_D clock, clock generator only | f _{reference} = 16 MHz, MC _x = 0, TDHREGEN = 1, TDHM _x = 1, TDHCLKCR = 1 | | | 265 | 330 | μA |
| I _(0,16,64) | I _(DVCC) | TDHCLKR _x = 0, TDHCLKSR _x = 16, TDHCLKTRIM = 64 | 2.2 V | | 244 | | μA |
| | | | 3.0 V | | 295 | 325 | |
| I _(1,16,64) | I _(DVCC) | TDHCLKR _x = 1, TDHCLKSR _x = 16, TDHCLKTRIM = 64 | 2.2 V | | 282 | | μA |
| | | | 3.0 V | | 300 | 400 | |
| I _(2,16,64) | I _(DVCC) | TDHCLKR _x = 2, TDHCLKSR _x = 16, TDHCLKTRIM = 64 | 2.2 V | | 358 | | μA |
| | | | 3.0 V | | 414 | 470 | |

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

Timer_D, Local Clock Generator Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------------------|---|-----|-----|-----|------|
| f _{HRCG(0,0,64)} | HRCG frequency (0, 0, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 0, TDHCLKTRIM = 64 | 39 | 56 | 73 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 0, TDHCLKTRIM = 64 | 78 | 112 | 146 | MHz |
| f _{HRCG(0,7,64)} | HRCG frequency (0, 7, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 7, TDHCLKTRIM = 64 | 46 | 66 | 86 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 7, TDHCLKTRIM = 64 | 92 | 132 | 172 | MHz |
| f _{HRCG(0,15,64)} | HRCG frequency (0, 15, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 15, TDHCLKTRIM = 64 | 55 | 78 | 101 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 15, TDHCLKTRIM = 64 | 110 | 156 | 202 | MHz |
| f _{HRCG(0,23,64)} | HRCG frequency (0, 23, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 23, TDHCLKTRIM = 64 | 61 | 87 | 113 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 23, TDHCLKTRIM = 64 | 122 | 174 | 226 | MHz |
| f _{HRCG(0,31,0)} | HRCG frequency (0, 31, 0) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 0 | 36 | 56 | 73 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 0 | 72 | 112 | 146 | MHz |
| f _{HRCG(0,31,64)} | HRCG frequency (0, 31, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 64 | 68 | 98 | 128 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 64 | 136 | 196 | 256 | MHz |
| f _{HRCG(0,31,128)} | HRCG frequency (0, 31, 128) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 128 | 97 | 138 | 180 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 128 | 196 | 176 | 360 | MHz |
| f _{HRCG(1,0,64)} | HRCG frequency (1, 0, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 0, TDHCLKTRIM = 64 | 71 | 101 | 131 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 0, TDHCLKTRIM = 64 | 142 | 202 | 262 | MHz |
| f _{HRCG(1,7,64)} | HRCG frequency (1, 7, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 7, TDHCLKTRIM = 64 | 84 | 120 | 156 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 7, TDHCLKTRIM = 64 | 168 | 240 | 312 | MHz |

Timer_D, Local Clock Generator Frequency (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------------------|---|-----|-----|-----|------|
| f _{HRCG(1,15,64)} | HRCG frequency (1, 15, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 15, TDHCLKTRIM = 64 | 97 | 139 | 182 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 15, TDHCLKTRIM = 64 | 196 | 278 | 364 | MHz |
| f _{HRCG(1,23,64)} | HRCG frequency (1, 23, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 23, TDHCLKTRIM = 64 | 108 | 154 | 200 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 23, TDHCLKTRIM = 64 | 216 | 308 | 400 | MHz |
| f _{HRCG(1,31,0)} | HRCG frequency (1, 31, 0) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 0 | 68 | 97 | 126 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 0 | 136 | 194 | 252 | MHz |
| f _{HRCG(1,31,64)} | HRCG frequency (1, 31, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 64 | 123 | 175 | 227 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 64 | 246 | 350 | 454 | MHz |
| f _{HRCG(1,31,128)} | HRCG frequency (1, 31, 128) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 128 | 169 | 241 | 313 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 128 | 338 | 482 | 616 | MHz |
| f _{HRCG(2,0,64)} | HRCG frequency (2, 0, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 0, TDHCLKTRIM = 64 | 126 | 180 | 234 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 1, TDHCLKSRx = 0, TDHCLKTRIM = 64 | 252 | 360 | 468 | MHz |
| f _{HRCG(2,7,64)} | HRCG frequency (2, 7, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 7, TDHCLKTRIM = 64 | 138 | 208 | 270 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 7, TDHCLKTRIM = 6 | 276 | 416 | 540 | MHz |
| f _{HRCG(2,15,64)} | HRCG frequency (2, 15, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 15, TDHCLKTRIM = 64 | 168 | 240 | 312 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 15, TDHCLKTRIM = 64 | 336 | 480 | 624 | MHz |
| f _{HRCG(2,23,64)} | HRCG frequency (2, 23, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 23, TDHCLKTRIM = 64 | 189 | 270 | 351 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 23, TDHCLKTRIM = 64 | 378 | 540 | 702 | MHz |

Timer_D, Local Clock Generator Frequency (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|-----|-----|-------|------|
| f _{HRCG(2,31,0)} | HRCG frequency (2, 31, 0) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 0 | 119 | 170 | 221 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 0 | 238 | 340 | 442 | MHz |
| f _{HRCG(2,31,64)} | HRCG frequency (2, 31, 64) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, DHCLKSRx = 31, TDHCLKTRIM = 64 | 212 | 303 | 394 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, DHCLKSRx = 31, TDHCLKTRIM = 64 | 424 | 606 | 788 | MHz |
| f _{HRCG(2,31,128)} | HRCG frequency (2, 31, 128) | TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 128 | 290 | 413 | 537 | MHz |
| | | TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 128 | 580 | 826 | 1074 | MHz |
| S _{HRCG,0,SR} | TDHCLKSRx step size in range 0 | S _{HRCGSR} = f _{HRCGSR(HRCGSR+1)} - f _{HRCG(HRCGSR)} | 120 | 185 | 225 | kHz |
| S _{HRCG,1,SR} | TDHCLKSRx step size in range 1 | S _{HRCGSR} = f _{HRCGSR(HRCGSR+1)} - f _{HRCG(HRCGSR)} | 220 | 325 | 395 | kHz |
| S _{HRCG,2,SR} | TDHCLKSRx step size in range 2 | S _{HRCGSR} = f _{HRCGSR(HRCGSR+1)} - f _{HRCG(HRCGSR)} | 400 | 555 | 700 | kHz |
| S _{HRCG,0,TRIM} | 0 >= TDHCLKTRIMx < 16, step size in range 0 | S _{HRCGSR} = f _{HRCGSR(HRCGTRIM+1)} - f _{HRCG(HRCGTRIM)} , TDHCLKSRx = X, Y, Z | 55 | 85 | 120 | kHz |
| | 15 < TDHCLKTRIMx < 49, step size in range 1 | | 40 | 85 | 130 | kHz |
| | 48 < TDHCLKTRIMx < 64, step size in range 2 | | 40 | 85 | 120 | kHz |
| S _{HRCG,1,TRIM} | 0 >= TDHCLKTRIMx < 16, step size in range 0 | S _{HRCGSR} = f _{HRCGSR(HRCGTRIM+1)} - f _{HRCG(HRCGTRIM)} , TDHCLKSRx = X, Y, Z | 90 | 160 | 230 | kHz |
| | 15 < TDHCLKTRIMx < 49, step size in range 1 | | 80 | 160 | 230 | kHz |
| | 48 < TDHCLKTRIMx < 64, step size in range 2 | | 80 | 160 | 230 | kHz |
| S _{HRCG,2,TRIM} | 0 >= TDHCLKTRIMx < 16, step size in range 0 | S _{HRCGSR} = f _{HRCGSR(HRCGTRIM+1)} - f _{HRCG(HRCGTRIM)} , TDHCLKSRx = X, Y, Z | 150 | 230 | 360 | kHz |
| | 15 < TDHCLKTRIMx < 49, step size in range 1 | | 130 | 230 | 350 | kHz |
| | 48 < TDHCLKTRIMx < 32, step size in range 2 | | 100 | 230 | 340 | kHz |
| df _{HRCG/dT} | HRCG frequency temperature drift | f _{HRCG} = 8 MHz, TDHREGEN = 0 | | | ±0.17 | %/°C |
| | | f _{HRCG} = 16 MHz, TDHREGEN = 0 | | | ±0.16 | %/°C |
| | | f _{HRCG} = 25 MHz, TDHREGEN = 0 | | | ±0.16 | %/°C |
| | | f _{HRCG} = 8/16/25 MHz, TDHREGEN = 1 | | 0 | | %/°C |
| df _{HRCG/dV_{CORE}} | HRCG frequency voltage drift | f _{HRCG} = 8/16/25 MHz, TDHREGEN = 0 | 0 | | 5 | %/V |
| | | f _{HRCG} = 8/16/25 MHz, TDHREGEN = 1 | | 0 | | %/V |
| t _{SETTLE} | Settling time | TDHEN = 0 -> 1, TDHFW = 0 | 3 | 5 | 9 | µs |
| | Settling time, fast wake-up | TDHEN = 0 -> 1, TDHFW = 1 | | | 1.5 | µs |

Timer_D, Trimmed Clock Frequencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|---|------|-----|------|------|
| Frequency tolerance during trimming | | | -0.5 | | +0.5 | % |
| $f_{TRIM(64MHz)}$ | TDHMx = 0, TDHREGEN = 0, TDHCLKCR = 0, TDHxCTL1 = TDHxCTL1_64 | $T_A = 25^{\circ}C$, $V_{CC} = 1.8 V$ | 63 | 64 | 65 | MHz |
| $f_{TRIM(128MHz)}$ | TDHMx = 0, TDHREGEN = 0, TDHCLKCR = 1, TDHxCTL1 = TDHxCTL1_128 | $T_A = 25^{\circ}C$, $V_{CC} = 2.0 V$ | 126 | 128 | 130 | MHz |
| $f_{TRIM(200MHz)}$ | TDHMx = 0, TDHREGEN = 0, TDHCLKCR = 1, TDHxCTL1 = TDHxCTL1_200 | $T_A = 25^{\circ}C$, $V_{CC} = 2.4 V$ | 197 | 200 | 203 | MHz |
| $f_{TRIM(256MHz)}$ | TDHMx = 1, TDHREGEN = 0, TDHCLKCR = 1, TDHxCTL1 = TDHxCTL1_256 | $T_A = 25^{\circ}C$, $V_{CC} = 2.2 V$ | 250 | 256 | 262 | MHz |

Timer_D, Frequency Multiplication Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|---|-----|-----|-----|------|
| External frequency tolerance | | | | 0 | | % |
| E(TDHREGEN = 1,64) | $f_{reference} = 8 MHz$, TDHMx = 0, TDHREGEN = 1, TDHCLKCR = 0, TDHCLKRx = 0 | $T_A = 25^{\circ}C$, $V_{CC} = 1.8 V$ | -1 | | +1 | % |
| E(TDHREGEN = 1,128) | $f_{reference} = 16 MHz$, TDHMx = 0, TDHREGEN = 1, TDHCLKCR = 1, TDHCLKRx = 0 | $T_A = 25^{\circ}C$, $V_{CC} = 2.0 V$ | -1 | | +1 | % |
| E(TDHREGEN = 1,200) | $f_{reference} = 25 MHz$, TDHMx = 0, TDHREGEN = 1, TDHCLKCR = 1, TDHCLKRx = 0 | $T_A = 25^{\circ}C$, $V_{CC} = 2.4 V$ | -1 | | +1 | % |
| E(TDHREGEN = 1,256) | $f_{reference} = 16 MHz$, TDHMx = 1, TDHREGEN = 1, TDHCLKCR = 1, TDHCLKRx = 0 | $T_A = 25^{\circ}C$, $V_{CC} = 2.2 V$ | -1 | | +1 | % |

Timer_D, Input Capture and Output Compare Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|--|-----|-----|-----|------|
| $t_{TD,cap}$ | Timer_D input capture timing, minimum pulse duration to trigger input capture event | $f_{MAX} = 262 \text{ MHz}$ | | 4 | | ns |
| $t_{TD0,cap,matching}$ | Timer0_D input capture timing, matching between input capture channels P1.6 to P1.7 and P2.0. | $f_{MAX} = 262 \text{ MHz}$ | | 1 | 2 | LSB |
| | Timer0_D input capture timing, matching between input capture channels. P2.4 to P2.5 and P2.6. | $f_{MAX} = 262 \text{ MHz}$ | | 3 | 4 | LSB |
| $t_{TD1,cap,matching}$ | Timer1_D input capture timing, matching between input capture channels P2.1 to P2.2 and P2.3. | $f_{MAX} = 262 \text{ MHz}$ | | 2 | 3 | LSB |
| | Timer1_D input capture timing, matching between input capture channels. P2.7 to P3.0 and P3.1. | $f_{MAX} = 262 \text{ MHz}$ | | 2 | 4 | LSB |
| $t_{TD01,cap,matching}$ | Timer0_D and Timer1_D input capture timing, matching between input capture channels. Timer0_D is the high-resolution clock generator source. | $f_{MAX} = 262 \text{ MHz}$ | | 4 | 8 | LSB |
| $t_{TD0,comp,matching}$ | Timer0_D output compare timing, matching between output capture compare channels for pins P1.6, P1.7, and P2.0 | Rising edges, $f_{MAX} = 262 \text{ MHz}$ | | | 4 | ns |
| | | Falling edges, $f_{MAX} = 262 \text{ MHz}$ | | | 4 | ns |
| | | Rising and falling edges, $f_{MAX} = 262 \text{ MHz}$ | | | 8 | ns |
| $t_{TD1,comp,matching}$ | Timer1_D output compare timing, matching between output capture compare channels for pins P2.1, P2.2, and P2.3 | Rising edges, $f_{MAX} = 262 \text{ MHz}$ | | | 4 | ns |
| | | Falling edges, $f_{MAX} = 262 \text{ MHz}$ | | | 4 | ns |
| | | Rising and falling edges, $f_{MAX} = 262 \text{ MHz}$ | | | 8 | ns |
| $t_{TD01,comp,matching}$ | Timer0_D and Timer1_D output compare timing, matching between output compare channels. Timer0_D is the high-resolution clock generator source | All edges, $f_{MAX} = 262 \text{ MHz}$ | | | 8 | LSB |

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----------------------|-----------------|-----------------|-----|--------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| I _{PGM} | Supply current from DV _{CC} during program | | | 3 | 5 | mA |
| I _{ERASE} | Supply current from DV _{CC} during erase | | | 2 | 6.5 | mA |
| I _{MERASE} , I _{BANK} | Supply current from DV _{CC} during mass erase or bank erase | | | 2 | 6.5 | mA |
| t _{CPT} | Cumulative program time | See ⁽¹⁾ | | | 16 | ms |
| | Program and erase endurance | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | 100 | | | years |
| t _{Word} | Word or byte program time | See ⁽²⁾ | 64 | | 85 | µs |
| t _{Block, 0} | Block program time for first byte or word | See ⁽²⁾ | 49 | | 65 | µs |
| t _{Block, 1–(N–1)} | Block program time for each additional byte or word, except for last byte or word | See ⁽²⁾ | 37 | | 49 | µs |
| t _{Block, N} | Block program time for last byte or word | See ⁽²⁾ | 55 | | 73 | µs |
| t _{Mass Erase} | Mass erase time | See ⁽²⁾ | 23 | | 32 | ms |
| t _{Seg Erase} | Segment erase time | See ⁽²⁾ | 23 | | 32 | ms |
| f _{MCLK,MGR} | MCLK frequency in marginal read mode (FCLK4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | µs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V, 3 V | | | 1 | µs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| f _{TCK} | TCK input frequency, 4-wire JTAG ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| R _{internal} | Internal pull-down resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the minimum t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.5, Input/Output With Schmitt Trigger

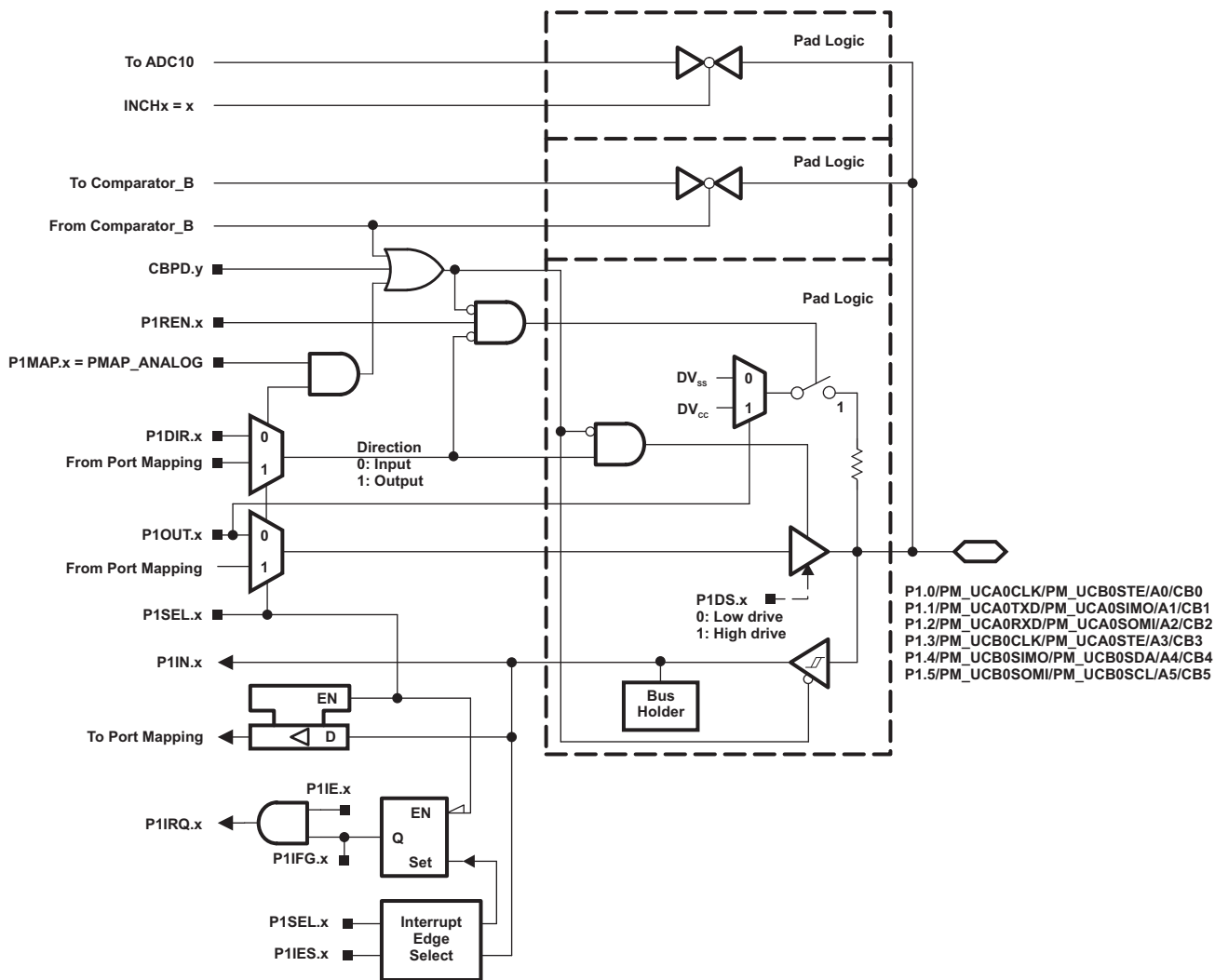


Table 46. Port P1 (P1.0 to P1.5) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|--|---|---|-------------------------------------|---------|-----------------|-----------|
| | | | P1DIR.x | P1SEL.x | P1MAP.x | CBPD.y |
| P1.0/ PM_UCA0CLK/ PM_UCB0STE/ A0/ CB0 | 0 | P1.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA0CLK/UCB0STE ^{(2) (3)} | 0 | 1 | default | 0 |
| | | A0 ⁽⁴⁾ | X | 1 | 31 INCHx = 0 | X |
| | | CB0 | X | X | X | 1 (y = 0) |
| P1.1/ PM_UCA0TXD/ PM_UCA0SIMO/ A1/ CB1 | 1 | P1.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | PM_UCA0TXD/PM_UCA0SIMO ⁽²⁾ | 0 | 1 | default | 0 |
| | | A1 ⁽⁴⁾ | X | 1 | 31 INCHx = 1 | X |
| | | CB1 | X | X | X | 1 (y = 1) |
| P1.2/ PM_UCA0RXD/ PM_UCA0SOMI/ A2/ CB2 | 2 | P1.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | PM_UCA0RXD/PM_UCA0SOMI ⁽²⁾ | 0 | 1 | default | 0 |
| | | A2 ⁽⁴⁾ | X | 1 | 31 INCHx = 2 | X |
| | | CB2 | X | X | X | 1 (y = 2) |
| P1.3/ PM_UCB0CLK/ PM_UCA0STE/ A3/ CB3 | 3 | P1.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0CLK/UCA0STE ⁽²⁾ | 0 | 1 | default | 0 |
| | | A3 ⁽⁴⁾ | X | 1 | 31 INCHx = 3 | X |
| | | CB3 | X | X | X | 1 (y = 3) |
| P1.4/ PM_UCB0SIMO/ PM_UCB0SDA/ A4/ CB4 | 4 | P1.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | PM_UCB0SIMO/PM_UCB0SDA ^{(2) (5)} | 0 | 1 | default | 0 |
| | | A4 ⁽⁴⁾ | X | 1 | 31 INCHx = 4 | X |
| | | CB4 | X | X | X | 1 (y = 4) |
| P1.5/ PM_UCB0SOMI/ PM_UCB0SCL/ A5/ CB5 | 5 | P1.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | PM_UCB0SOMI/PM_UCB0SCL ^{(2) (5)} | 0 | 1 | default | 0 |
| | | A5 ⁽⁴⁾ | X | 1 | 31 INCHx = 5 | X |
| | | CB5 | X | X | X | 1 (y = 5) |

- (1) X = Don't care
- (2) The pin direction is controlled by the USCI module.
- (3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
- (4) MSP430F51x2 device only.
- (5) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P1, P1.6 to P1.7, Input/Output With Schmitt Trigger

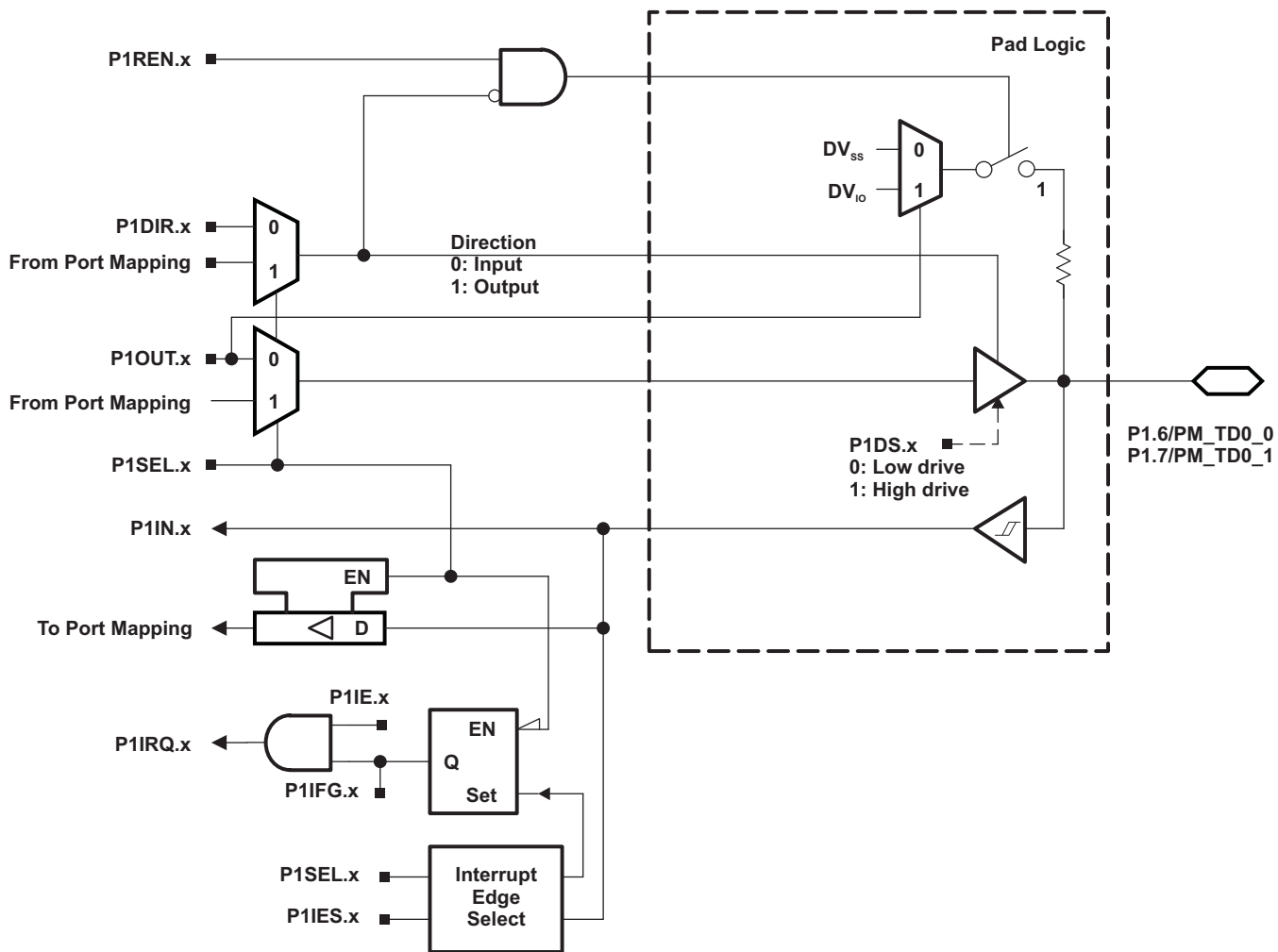


Table 47. Port P1 (P1.6 and P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | |
|-------------------|---|------------|-------------------------------------|---------|---------|
| | | | P1DIR.x | P1SEL.x | P1MAP.x |
| P1.6/ PM_TD0.0 | 6 | P1.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD0.CCI0A | 0 | 1 | default |
| | | TD0.TA0 | 1 | 1 | default |
| P1.7/ PM_TD0.1 | 7 | P1.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD0.CCI1A | 0 | 1 | default |
| | | TD0.TA1 | 1 | 1 | default |

(1) X = Don't care

Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

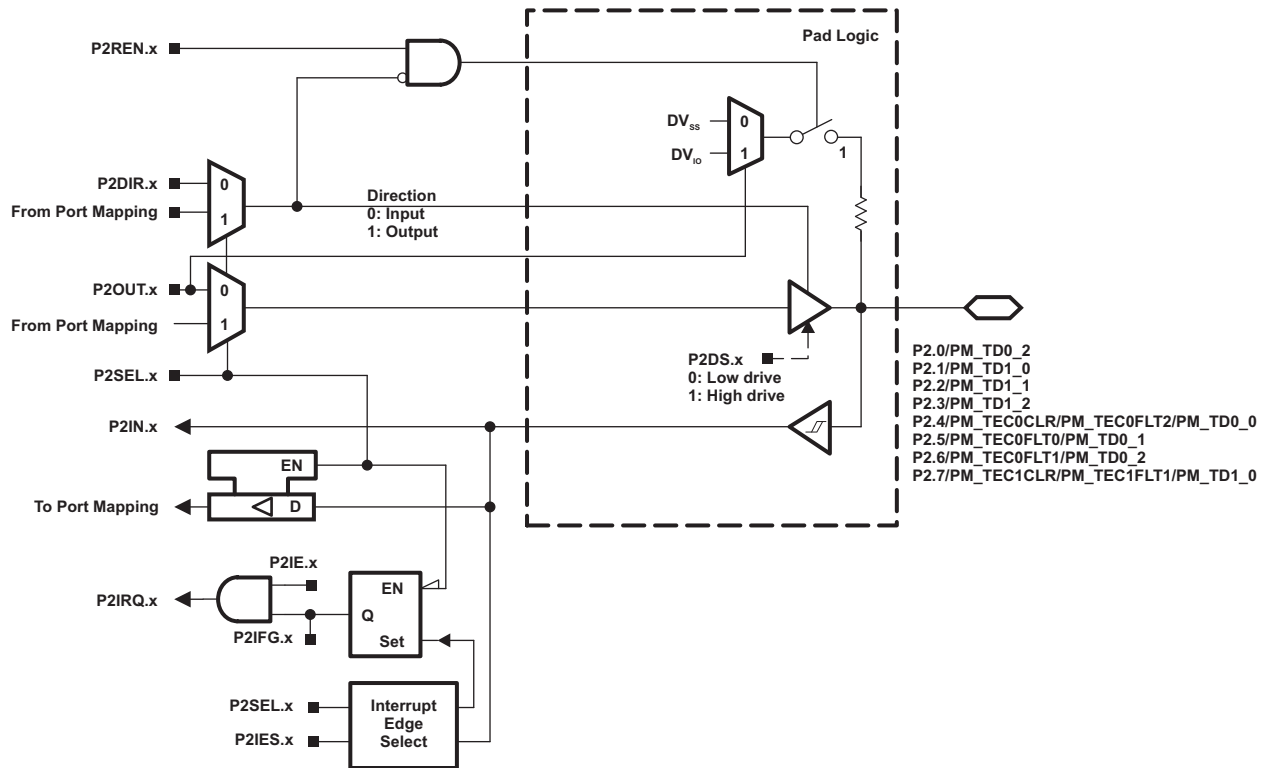


Table 48. Port P2 (P2.0 to P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|--|---|--|----------------------|---------|---------|
| | | | P2DIR.x | P2SEL.x | P2MAP.x |
| P2.0/ PM_TD0.2 | 0 | P2.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD0.CCI2A | 0 | 1 | default |
| | | TD0.TA2 | 1 | 1 | default |
| P2.1/ PM_TD1.0 | 1 | P2.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD1.CCI0A | 0 | 1 | default |
| | | TD1.TA0 | 1 | 1 | default |
| P2.2/ PM_TD1.1 | 2 | P2.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD1.CCI1A | 0 | 1 | default |
| | | TD1.TA1 | 1 | 1 | default |
| P2.3/ PM_TD1.2 | 3 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TD1.CCI2A | 0 | 1 | default |
| | | TD1.TA2 | 1 | 1 | default |
| P2.4/ PM_TEC0CLR/ PM_TEC0FLT2/ PM_TD0.0 | 4 | P2.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD0.TECEXTCLR, controlled by enable signals in the TEC0 module | 0 | 1 | default |
| | | TD0.TECXFLT2, controlled by enable signals in the TEC0 module | 0 | 1 | default |
| | | TD0.TA0 | 1 | 1 | default |
| P2.5/ PM_TEC0FLT0/ PM_TD0.1 | 5 | P2.x (I/O) | I: 0; O: 1 | 0 | x |
| | | TD0.TECXFLT0, controlled by enable signals in the TEC0 module | 0 | 1 | default |
| | | TD0.TA1 | 1 | 1 | default |
| P2.6/ PM_TEC0FLT1/ PM_TD0.2 | 6 | P2.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD0.TECXFLT1, controlled by enable signals in the TEC0 module | 0 | 1 | default |
| | | TD0.TA2 | 1 | 1 | default |
| P2.7/ PM_TEC1CLR/ PM_TEC1FLT1/ PM_TD1.0 | 7 | P2.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD1.TECEXTCLR, controlled by enable signals in the TEC1 module | 0 | 1 | default |
| | | TD1.TECXFLT1, controlled by enable signals in the TEC1 module | 0 | 1 | default |
| | | TD1.TA0 | 1 | 1 | default |

Port P3, P3.0 and P3.1, Input/Output With Schmitt Trigger

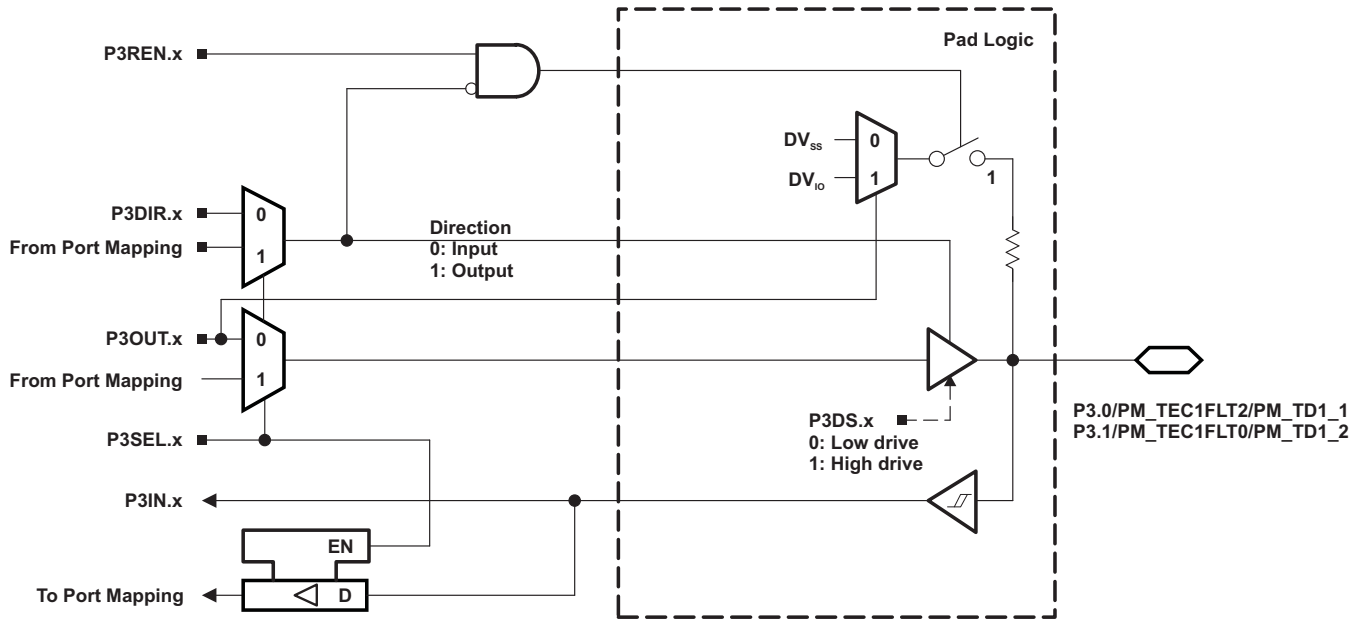


Table 49. Port P3 (P3.0 and P3.1) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|-----------------------------------|---|---|----------------------|---------|---------|
| | | | P3DIR.x | P3SEL.x | P3MAP.x |
| P3.0/ PM_TEC1FLT2/ PM_TD1.1 | 0 | P3.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD1.TECXFLT2, controlled by enable signals in the TEC1 module | 0 | 1 | default |
| | | TD1.TA1 | 1 | 1 | default |
| P3.1/ PM_TEC1FLT0/ PM_TD1.2 | 1 | P3.x (I/O) | I: 0; O: 1 | 0 | X |
| | | TD1.TECXFLT0, controlled by enable signals in the TEC1 module | 0 | 1 | default |
| | | TD1.TA2 | 1 | 1 | default |

Port P3, P3.2 and P3.3, Input/Output With Schmitt Trigger

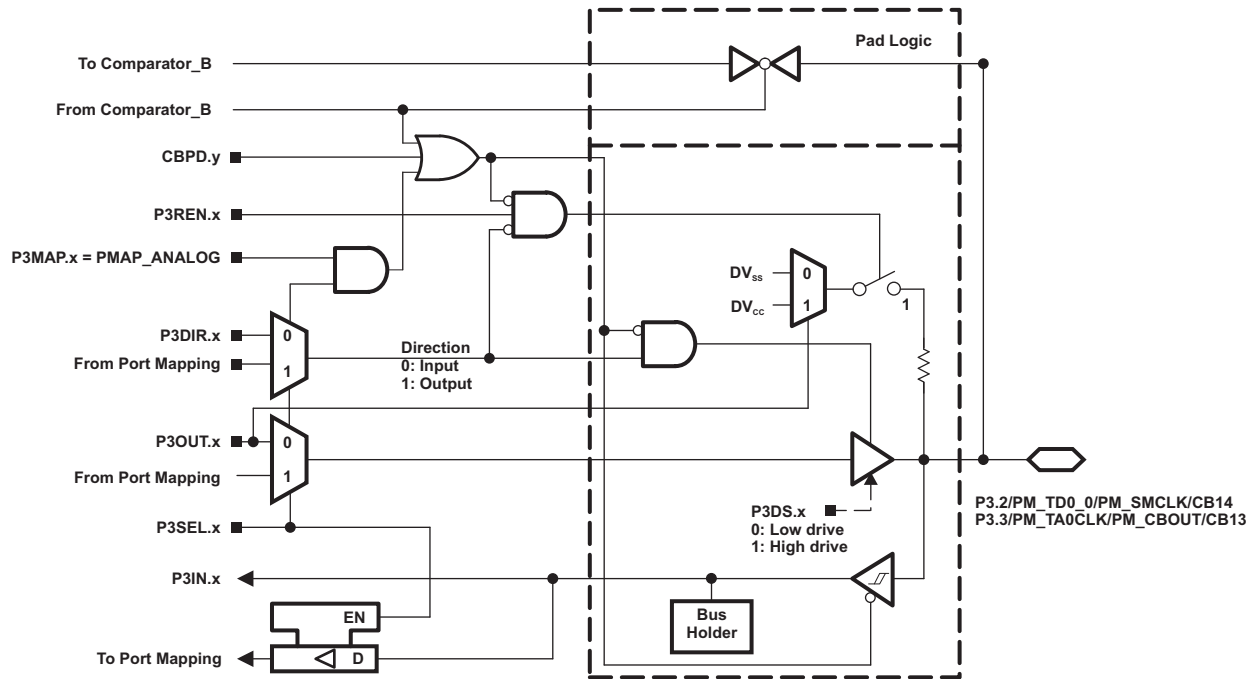


Table 50. Port P3 (P3.2 and P3.3) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|--|---|--------------|-------------------------------------|---------|---------|------------|
| | | | P3DIR.x | P3SEL.x | P3MAP.x | CBPD.y |
| P3.2/ PM_TD0.0/ PM_SMCLK/ CB14 | 2 | P3.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TD0.CCI0A | 0 | 1 | default | 0 |
| | | SMCLK output | 1 | 1 | default | 0 |
| | | CB14 | X | X | X | 1 (y = 14) |
| P3.3/ PM_TA0CLK/ PM_CBOUT/ CB13 | 3 | P3.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA0.TA0CLK | 0 | 1 | default | 0 |
| | | CBOUT | 1 | 1 | default | 0 |
| | | CB13 | X | X | X | 1 (y = 13) |

(1) X = Don't care

Port P3, P3.4, Input/Output With Schmitt Trigger

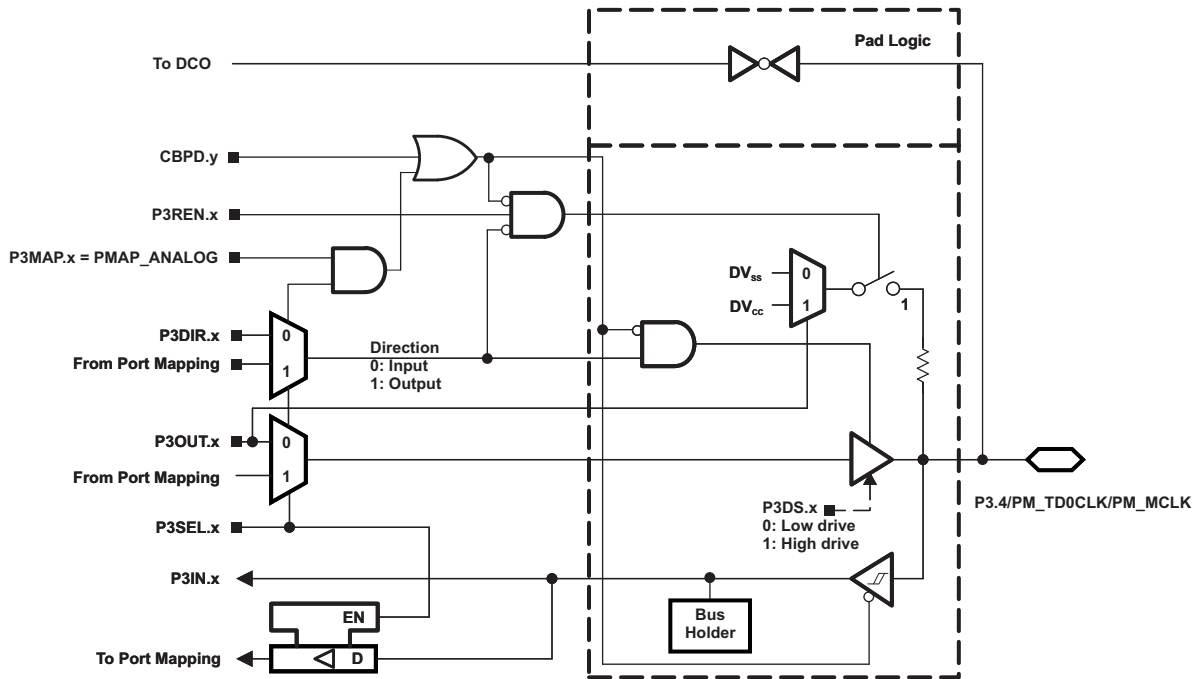


Table 51. Port P3 (P3.4) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|-----------------|---|-----------------|-------------------------------------|---------|---------|---|
| | | | P3DIR.x | P3SEL.x | P3MAP.x | |
| P3.4/ | 4 | P3.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| PM_TD0CLK/ | | TD0 clock input | 0 | 1 | default | 0 |
| PM_MCLK | | MCLK output | 1 | 1 | default | 0 |

(1) X = Don't care

Port P3, P3.5, Input/Output With Schmitt Trigger

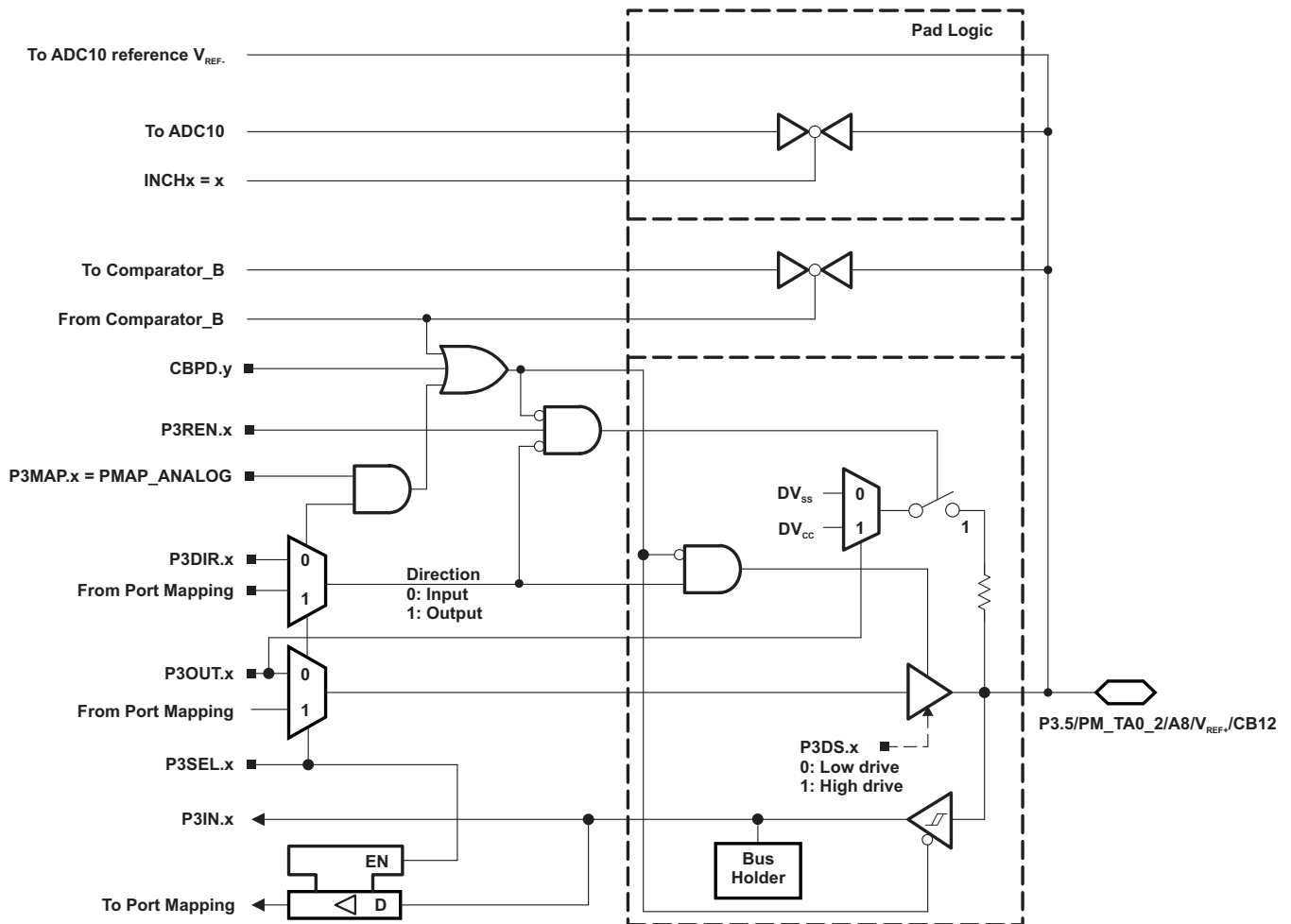


Table 52. Port P3 (P3.5) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|--------------------|---|-----------------------|-------------------------------------|---------|---------|------------|
| | | | P3DIR.x | P3SEL.x | P3MAP.x | CBPD.y |
| P3.5/ PM_TA0.2/ | 5 | P3.x (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA0.CCI2A | 0 | 1 | default | 0 |
| | | TA0.TA2 | 1 | 1 | default | 0 |
| VEREF+/ | | VEREF+ ⁽²⁾ | X | 1 | 31 | X |
| A8/ | | A8 ⁽²⁾ | X | 1 | INCHx=8 | X |
| CB12 | | CB12 | X | X | X | 1 (y = 12) |

(1) X = Don't care

(2) MSP430F51x2 devices only.

Port P3, P3.6, Input/Output With Schmitt Trigger

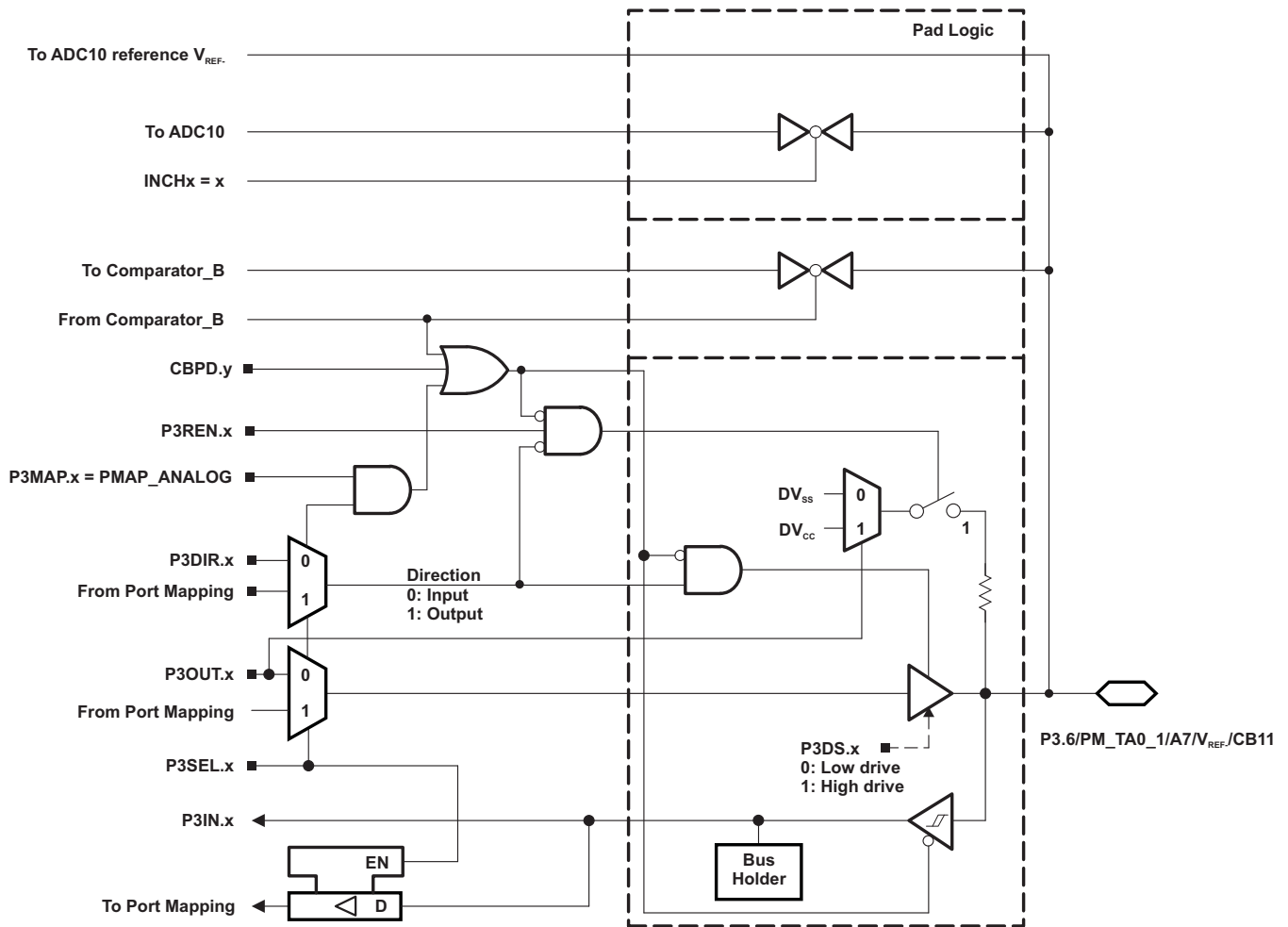


Table 53. Port P3 (P3.6) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|--------------------|---|---------------------------|-------------------------------------|---------|-----------------|------------|
| | | | P3DIR.x | P3SEL.x | P3MAP.x | CBPD.y |
| P3.6/ PM_TA0.1/ | 6 | P3.x (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | X | 0 |
| | | TA0.CCR0 | 0 | 1 | default | 0 |
| | | TA0.TA1 | 1 | 1 | default | 0 |
| VEREF-/ | | VEREF- ⁽³⁾ | X | 1 | 31 | X |
| A7/ | | A7 ⁽³⁾ | X | 1 | 31 INCHx = 7 | X |
| CB11 | | CB11 | X | X | 0 | 1 (y = 11) |

(1) X = Don't care
(2) Default condition.
(3) MSP430F51x2 devices only.

Port P3, P3.7, Input/Output With Schmitt Trigger

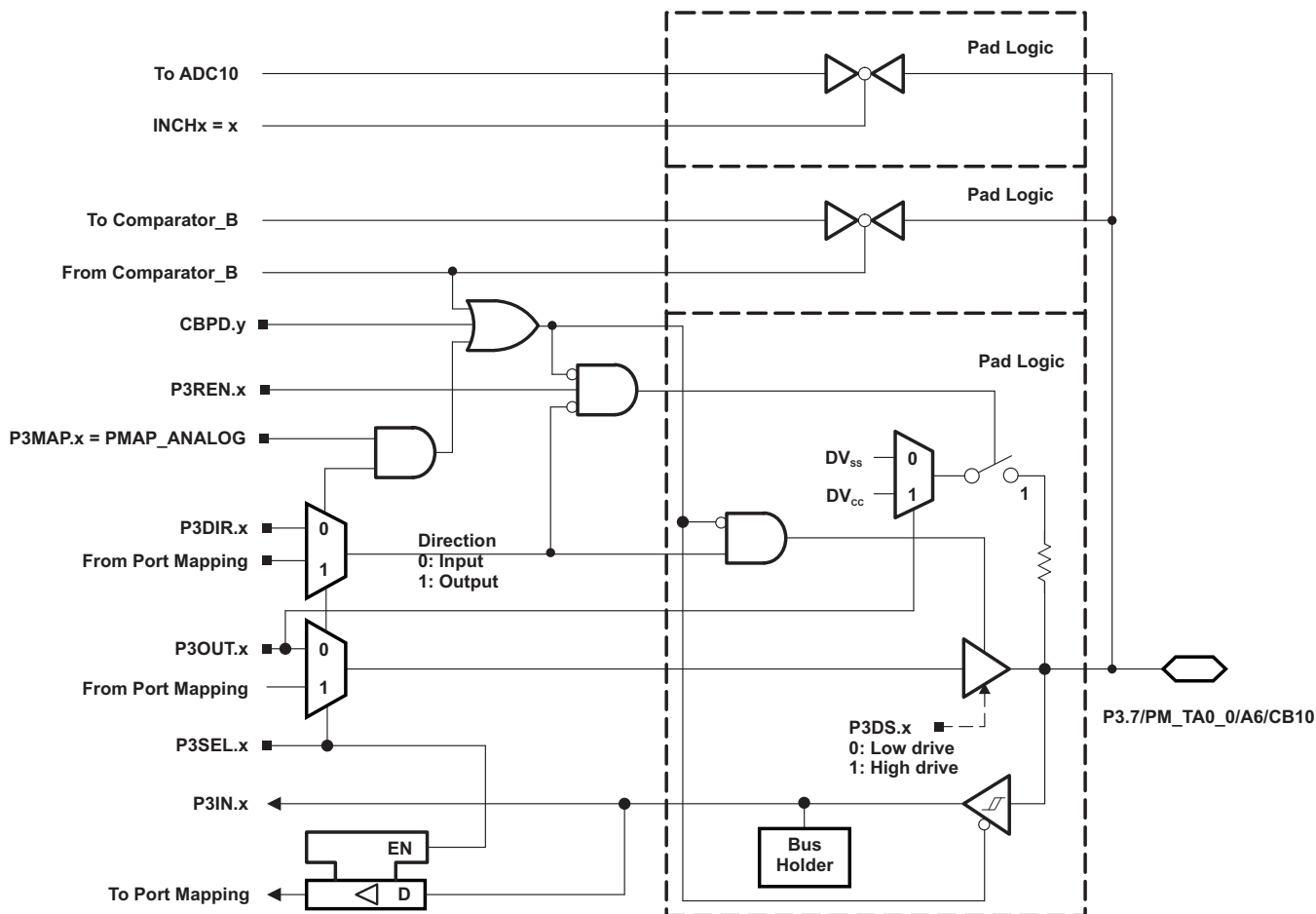


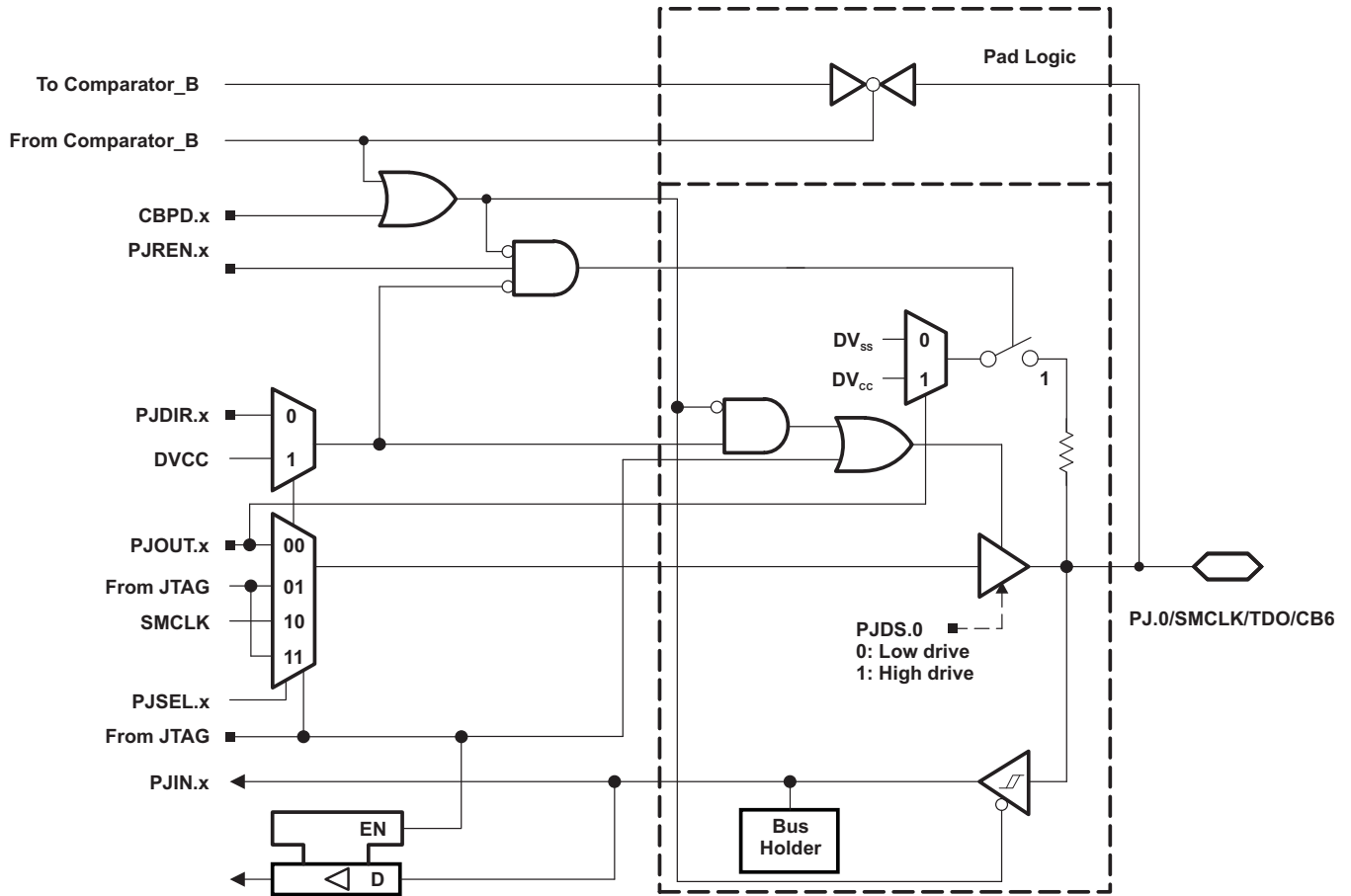
Table 54. Port P3 (P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|--------------------|---|---------------------------|-------------------------------------|---------|-----------------|------------|
| | | | P3DIR.x | P3SEL.2 | P3MAP.x | CBPD.y |
| P3.7/ PM_TA0.0/ | 7 | P3.x (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | X | 0 |
| | | TA0.CCR0 | 0 | 1 | default | 0 |
| | | TA0.TA0 | 1 | 1 | default | 0 |
| A6/ | | A6 ⁽²⁾ | X | 1 | 31 INCHx = 6 | X |
| CB10 | | CB10 | X | X | 0 | 1 (y = 10) |

(1) X = Don't care

(2) MSP430F51x2 devices only.

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

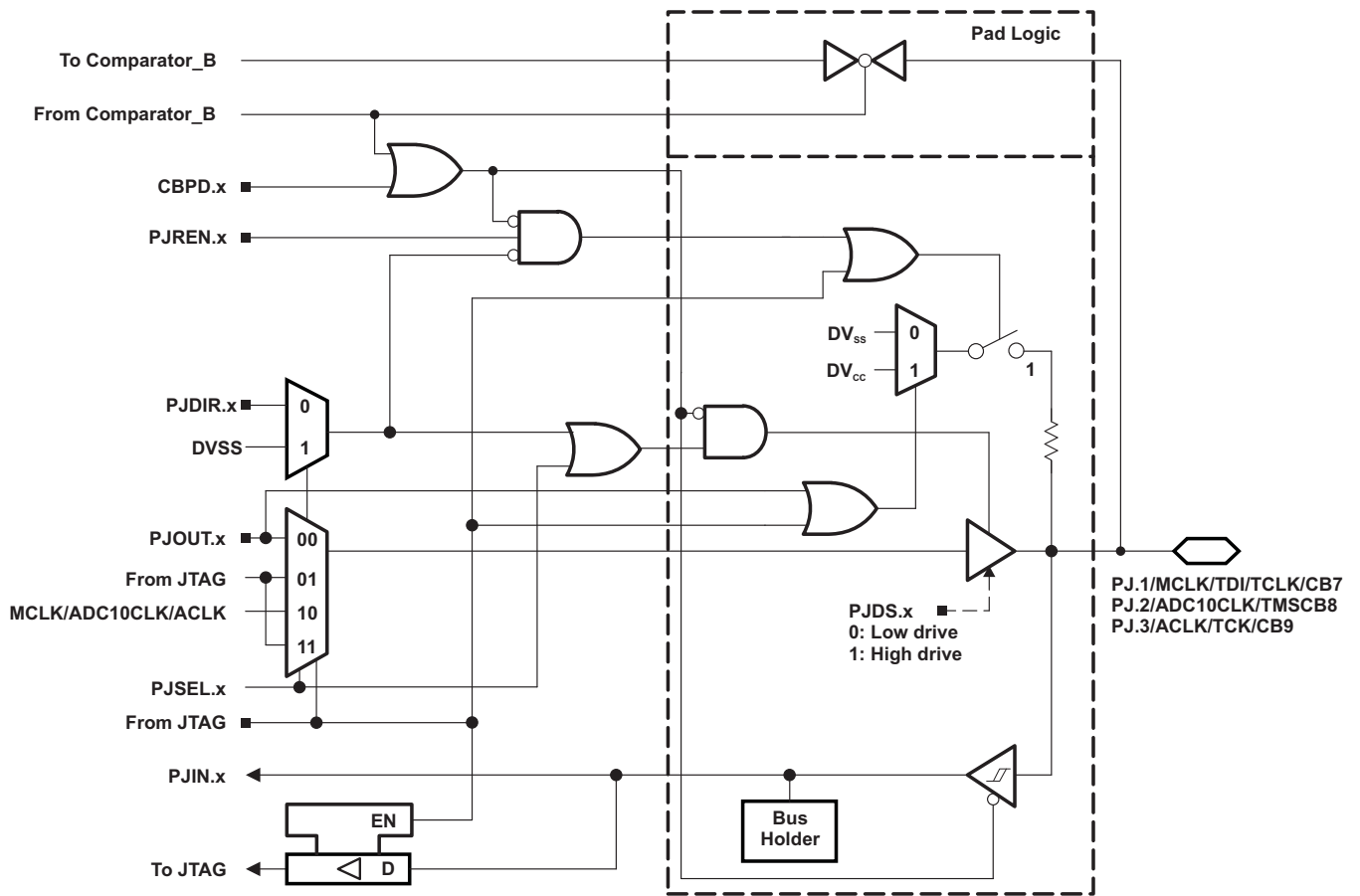
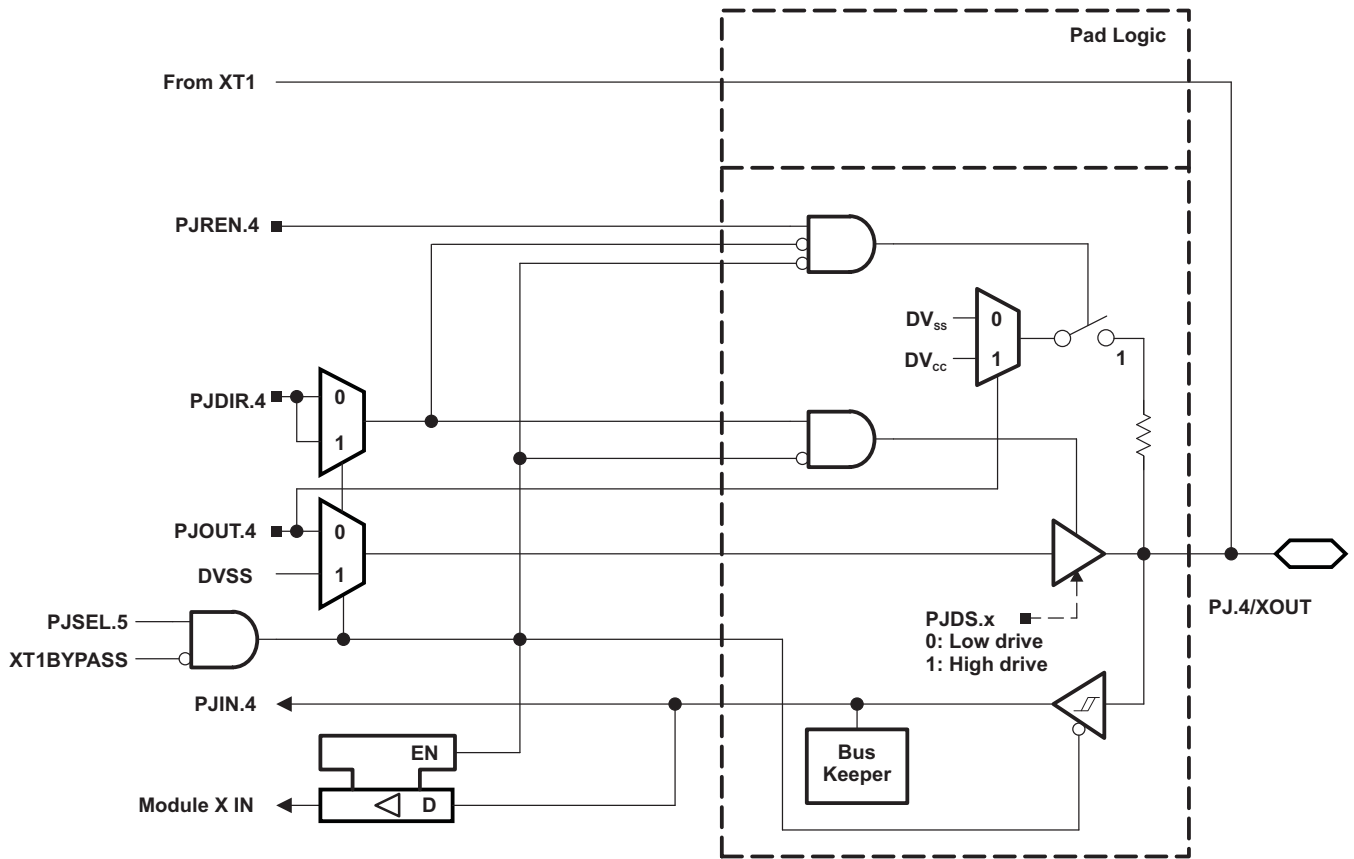


Table 55. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS/ SIGNALS ⁽¹⁾ | | | |
|------------------------------------|---|--------------------------------|--------------------------------------|---------|-----------|-----------|
| | | | PJDIR.x | PJSEL.x | JTAG MODE | CBPD.y |
| PJ.0/ SMCLK/ TDO/ CB6 | 0 | PJ.x (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 | 0 |
| | | SMCLK | 1 | 1 | 0 | 0 |
| | | TDO ⁽³⁾ | X | X | 1 | X |
| | | CB6 | X | X | 0 | 1 (y = 6) |
| PJ.1/ MCLK/ TDI/TCLK/ CB7 | 1 | PJ.x (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 | 0 |
| | | MCLK | 1 | 1 | 0 | 0 |
| | | TDI/TCLK ^{(3) (4)} | X | X | 1 | X |
| | | CB7 | 0 | X | 0 | 1 (y = 7) |
| PJ.2/ ADC10CLK/ TMS/ CB8 | 2 | PJ.x (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 | 0 |
| | | ADC10CLK (See ⁽⁵⁾) | 1 | 1 | 0 | 0 |
| | | TMS ^{(3) (4)} | X | X | 1 | X |
| | | CB8 | X | X | 0 | 1 (y = 8) |
| PJ.3/ ACLK/ TCK/ CB9 | 3 | PJ.x (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 | 0 |
| | | ACLK | 1 | 1 | 0 | 0 |
| | | TCK ^{(3) (4)} | X | X | 1 | X |
| | | CB9 | X | X | 0 | 1 (y = 9) |

- (1) X = Don't care
- (2) Default condition
- (3) The pin direction is controlled by the JTAG module.
- (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.
- (5) MSP430F51x2 device only.

Port PJ.4, Input/Output With Schmitt Trigger



Port PJ.5, Input/Output With Schmitt Trigger

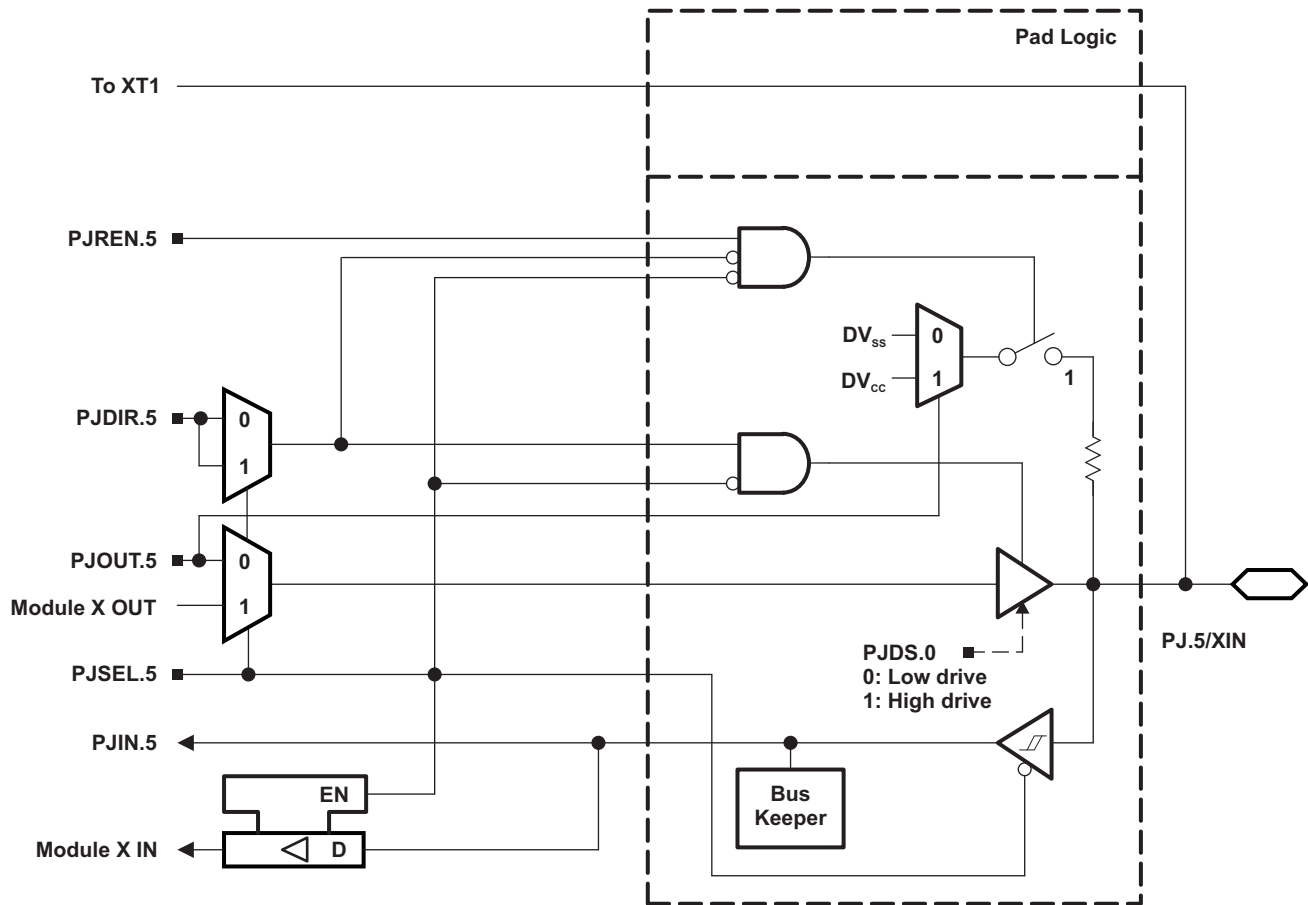


Table 56. Port PJ (PJ.4 and PJ.5) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|-----------------|---|----------------------------------|-------------------------------------|---------|---------|------------|
| | | | PJDIR.x | PJSEL.4 | PJSEL.5 | XT1BYPAS S |
| PJ.4/ | 4 | PJ.x (I/O) | I: 0; O: 1 | X | 0 | x |
| XOUT | | XOUT crystal mode ⁽²⁾ | X | X | 1 | 0 |
| PJ.5/ | 5 | PJ.x (I/O) ⁽³⁾ | I: 0; O: 1 | X | 0 | x |
| XIN | | XIN crystal mode ⁽⁴⁾ | X | X | 1 | 0 |
| | | XIN bypass mode ⁽⁴⁾ | X | X | 1 | 1 |

- (1) X = Don't care
- (2) Setting PJSEL.5 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, PJ.4 can be used as general-purpose I/O.
- (3) Setting PJSEL.5 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, PJ.4 can be used as general-purpose I/O.
- (4) Setting PJSEL.5 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, PJ.5 is configured for crystal mode or bypass mode.

Port PJ.6, Input/Output With Schmitt Trigger

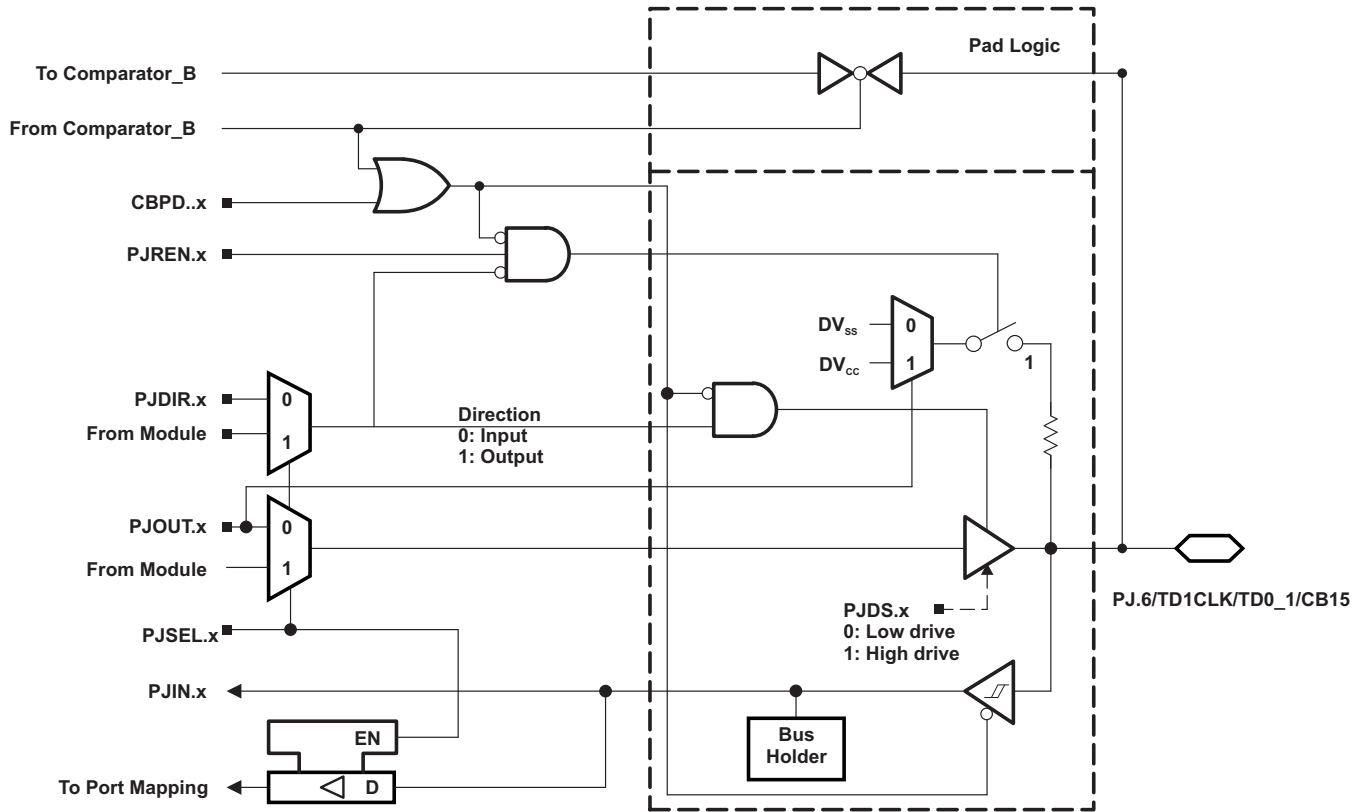


Table 57. Port PJ (PJ.6) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | |
|-----------------|---|-----------------|-------------------------------------|---------|------------|
| | | | PJDIRE.x | PJSEL.x | CBPD.y |
| PJ.6/ | 6 | PJ.x (I/O) | I: 0; O: 1 | 0 | 0 |
| TD1CLK/ | | TD1 clock input | 0 | 1 | 0 |
| TD0.1/ | | TD0.TA1 | 1 | 1 | 0 |
| CB15 | | CB15 | X | X | 1 (y = 15) |

(1) X = Don't care

DEVICE DESCRIPTORS

Table 58 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 58. 'F51x2 Device Descriptor Table⁽¹⁾

| | Description | Address | Size bytes | 'F5172 RSB | 'F5172 DA | 'F5152 RSB | 'F5152 DA | 'F5132 RSB | 'F5132 DA |
|---------------------------------------|---------------------------------------|---------|------------|------------|-----------|------------|-----------|------------|-----------|
| | | | | Value | Value | Value | Value | Value | Value |
| Info Block | Info length | 0x1A00 | 1 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 |
| | CRC length | 0x1A01 | 1 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 |
| | CRC value | 0x1A02 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 0x1A04 | 1 | 0x30 | 0x30 | 0x2C | 0x2C | 0x28 | 0x28 |
| | Device ID | 0x1A05 | 1 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 |
| | Hardware revision | 0x1A06 | 1 | 0x30 | 030 | 0x30 | 0x30 | 0x30 | 0x30 |
| | Firmware revision | 0x1A07 | 1 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 |
| Die Record | Die Record Tag | 0x1A08 | 1 | 0x08 | 08 | 0x08 | 08 | 0x08 | 08 |
| | Die Record length | 0x1A09 | 1 | 0x0A | 0A | 0x0A | 0A | 0x0A | 0A |
| | Lot/Wafer ID | 0x1A0A | 4 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 0x1A0Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 0x1A10 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Test results | 0x1A12 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| ADC10 Calibration | ADC10 Calibration Tag | 0x1A14 | 1 | 0x13 | 0x13 | 0x13 | 0x13 | 0x13 | 0x13 |
| | ADC10 Calibration length | 0x1A15 | 1 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 |
| | ADC Gain Factor | 0x1A16 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC Offset | 0x1A18 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 0x1A1A | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 0x1A1C | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 0x1A1Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 0x1A20 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 0x1A22 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| ADC 2.5-V Reference Temp. Sensor 85°C | 0x1A24 | 2 | per unit | per unit | per unit | per unit | per unit | per unit | |
| REF User Calibration | REF Tag | 0x1A26 | 1 | 0x12 | 0x12 | 0x12 | 0x12 | 0x12 | 0x12 |
| | REF length | 0x1A27 | 1 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 |
| | REF 1.5-V Reference | 0x1A28 | 2 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |
| | REF 2.0-V Reference | 0x1A2A | 2 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |
| | REF 2.5-V Reference | 0x1A2C | 2 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |
| Timer_D0 Calibration | Timer_D Tag | 0x1A2E | 1 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 |
| | Timer_D length | 0x1A2F | 1 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 |
| | Timer_D 64-MHz frequency | 0x1A30 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 128-MHz frequency | 0x1A32 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 200-MHz frequency | 0x1A34 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| Timer_D1 Calibration | Timer_D 256-MHz frequency | 0x1A36 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D Tag | 0x1A38 | 1 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 |
| | Timer_D length | 0x1A39 | 1 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 |
| | Timer_D 64-MHz frequency | 0x1A3A | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 128-MHz frequency | 0x1A3C | 2 | per unit | per unit | per unit | per unit | per unit | per unit |

(1) NA = Not applicable

Table 58. 'F51x2 Device Descriptor Table⁽¹⁾ (continued)

| | Description | Address | Size bytes | 'F5172 RSB | 'F5172 DA | 'F5152 RSB | 'F5152 DA | 'F5132 RSB | 'F5132 DA |
|------------------------------|------------------------------|---------|------------|------------|-----------|------------|-----------|------------|-----------|
| | | | | Value | Value | Value | Value | Value | Value |
| | Timer_D 200-MHz frequency | 0x1A3E | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 256-MHz frequency | 0x1A40 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| Peripheral Descriptor | Peripheral Descriptor Tag | 0x1A42 | 1 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 |
| | Peripheral Descriptor Length | 0x1A43 | 1 | 0x53 | 0x53 | 0x53 | 0x53 | 0x53 | 0x53 |
| | BSL Memory | 0x1A44 | 2 | 0x8A08 | 0x8A08 | 0x8A08 | 0x8A08 | 0x8A08 | 0x8A08 |
| | Information Memory | 0x1A46 | 2 | 0x860C | 0x860C | 0x860C | 0x860C | 0x860C | 0x860C |
| | RAM | 0x1A48 | 2 | 0x2A0E | 0x2A0E | 0x2A0E | 0x2A0E | 0x280E | 0x280E |
| | Main Memory | 0x1A4A | 2 | 0x9240 | 0x9240 | 0x9060 | 0x9060 | 0x8E70 | 0x8E70 |
| | Delimiter | 0x1A4C | 1 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| | Peripheral count | 0x1A4D | 1 | 0x1C | 0x1C | 0x1B | 0x1B | 0x1B | 0x1B |
| | MSP430CPUXV2 | 0x1A4E | 2 | 0x2300 | 0x2300 | 0x2300 | 0x2300 | 0x2300 | 0x2300 |
| | SBW | 0x1A50 | 2 | 0x0F00 | 0x0F00 | 0x0F00 | 0x0F00 | 0x0F00 | 0x0F00 |
| | EEM-S | 0x1A52 | 2 | 0x0300 | 0x0300 | 0x0300 | 0x0300 | 0x0300 | 0x0300 |
| | TI BSL | 0x1A54 | 2 | 0xFC00 | 0xFC00 | 0xFC00 | 0xFC00 | 0xFC00 | 0xFC00 |
| | SFR | 0x1A56 | 2 | 0x4110 | 0x4110 | 0x4110 | 0x4110 | 0x4110 | 0x4110 |
| | PMM | 0x1A58 | 2 | 0x3002 | 0x3002 | 0x3002 | 0x3002 | 0x3002 | 0x3002 |
| | FCTL | 0x1A5A | 2 | 0x3802 | 0x3802 | 0x3802 | 0x3802 | 0x3802 | 0x3802 |
| | CRC16 | 0x1A5C | 2 | 0x3C01 | 0x3C01 | 0x3C01 | 0x3C01 | 0x3C01 | 0x3C01 |
| | CRC16_RB | 0x1A5E | 2 | 0x3D00 | 0x3D00 | 0x3D00 | 0x3D00 | 0x3D00 | 0x3D00 |
| | RAMCTL | 0x1A60 | 2 | 0x4400 | 0x4400 | 0x4400 | 0x4400 | 0x4400 | 0x4400 |
| | WDT_A | 0x1A62 | 2 | 0x4000 | 0x4000 | 0x4000 | 0x4000 | 0x4000 | 0x4000 |
| | UCS | 0x1A64 | 2 | 0x4801 | 0x4801 | 0x4801 | 0x4801 | 0x4801 | 0x4801 |
| | SYS | 0x1A66 | 2 | 0x4202 | 0x4202 | 0x4202 | 0x4202 | 0x4202 | 0x4202 |
| | Shared REF | 0x1A68 | 2 | 0xA003 | 0xA003 | 0xA003 | 0xA003 | 0xA003 | 0xA003 |
| | Port Mapping | 0x1A6A | 2 | 0x1001 | 0x1001 | 0x1001 | 0x1001 | 0x1001 | 0x1001 |
| | Port 1/2 | 0x1A6C | 2 | 0x5104 | 0x5104 | 0x5104 | 0x5104 | 0x5104 | 0x5104 |
| | Port 3/4 | 0x1A6E | 2 | 0x5202 | 0x5202 | 0x5202 | 0x5202 | 0x5202 | 0x5202 |
| | Port J | 0x1A70 | 2 | 0x5F10 | 0x5F10 | 0x5F10 | 0x5F10 | 0x5F10 | 0x5F10 |
| | TA0 | 0x1A72 | 2 | 0x610A | 0x610A | 0x610A | 0x610A | 0x610A | 0x610A |
| | MPY32 | 0x1A74 | 2 | 0x8510 | 0x8510 | 0x8510 | 0x8510 | 0x8510 | 0x8510 |
| | DMA with 3 channels | 0x1A76 | 2 | 0x4704 | 0x4704 | 0x4704 | 0x4704 | 0x4704 | 0x4704 |
| | USCI_A0/B0 | 0x1A78 | 2 | 0x900C | 0x900C | 0x900C | 0x900C | 0x900C | 0x900C |
| | ADC10_A | 0x1A7A | 2 | 0xD318 | 0xD318 | 0xD318 | 0xD318 | 0xD318 | 0xD318 |
| | COMP_B | 0x1A7C | 2 | 0xA818 | 0xA818 | 0x1A919 | 0xA818 | 0x1A919 | 0xA818 |
| | TIMER_D0 | 0x1A7E | 2 | 0xD624 | 0xD624 | 0xD624 | 0xD624 | 0xD624 | 0xD624 |
| | TIMER_D1 | 0x1A80 | 2 | 0x6D04 | 0x6D04 | 0x6D04 | 0x6D04 | 0x6D04 | 0x6D04 |
| | TEC_0 | 0x1A82 | 2 | 0x700C | 0x700C | 0x700C | 0x700C | 0x700C | 0x700C |
| | TEC_1 | 0x1A84 | 2 | 0x7002 | 0x7002 | 0x7002 | 0x7002 | 0x7002 | 0x7002 |
| Interrupts | COMP_B | 0x1A86 | 1 | 0xA8 | 0xA8 | 0xA8 | 0xA8 | 0xA8 | 0xA8 |
| | TEC_0 | 0x1A87 | 1 | 0x6D | 0x6D | 0x6D | 0x6D | 0x6D | 0x6D |
| | TIMER_D0 | 0x1A88 | 1 | 0x62 | 0x62 | 0x62 | 0x62 | 0x62 | 0x62 |
| | TIMER_D0 | 0x1A89 | 1 | 0x63 | 0x63 | 0x63 | 0x63 | 0x63 | 0x63 |
| | WDTIFG | 0x1A8A | 1 | 0x40 | 0x40 | 0x40 | 0x40 | 0x40 | 0x40 |
| | USCI_A0 | 0x1A8B | 1 | 0x90 | 0x90 | 0x90 | 0x90 | 0x90 | 0x90 |
| | USCI_B0 | 0x1A8C | 1 | 0x91 | 0x91 | 0x91 | 0x91 | 0x91 | 0x91 |
| | ADC10_A | 0x1A8D | 1 | 0xD0 | 0xD0 | 0xD0 | 0xD0 | 0xD0 | 0xD0 |
| | TA0.CCIFG0 | 0x1A8E | 1 | 0x60 | 0x60 | 0x60 | 0x60 | 0x60 | 0x60 |
| | TA0.CCIFG1..4 | 0x1A8F | 1 | 0x61 | 0x61 | 0x61 | 0x61 | 0x61 | 0x61 |
| | DMA | 0x1A90 | 1 | 0x46 | 0x46 | 0x46 | 0x46 | 0x46 | 0x46 |

Table 58. 'F51x2 Device Descriptor Table⁽¹⁾ (continued)

| | Description | Address | Size bytes | 'F5172 RSB | 'F5172 DA | 'F5152 RSB | 'F5152 DA | 'F5132 RSB | 'F5132 DA |
|--------------|---------------|-----------------|------------|------------|-----------|------------|-----------|------------|-----------|
| | | | | Value | Value | Value | Value | Value | Value |
| | TEC_1 | 0x1A91 | 1 | 0x6E | 0x6E | 0x6E | 0x6E | 0x6E | 0x6E |
| | TIMER_D1 | 0x1A92 | 1 | 0x64 | 0x64 | 0x64 | 0x64 | 0x64 | 0x64 |
| | TIMER_D1 | 0x1A93 | 1 | 0x65 | 0x65 | 0x65 | 0x65 | 0x65 | 0x65 |
| | Port P1 | 0x1A94 | 1 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 |
| | Port P2 | 0x1A95 | 1 | 0x51 | 0x51 | 0x51 | 0x51 | 0x51 | 0x51 |
| | delimiter | 0x1A96 | 1 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| Empty | Unused Memory | 0x1A97 - 0x1AB9 | | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |

Table 59. 'F51x1 Device Descriptor Table⁽¹⁾

| | Description | Address | Size bytes | 'F5171 RSB | 'F5171 DA | 'F5151 RSB | 'F5151 DA | 'F5131 RSB | 'F5131 DA |
|-----------------------------|---------------------------------------|---------|------------|------------|-----------|------------|-----------|------------|-----------|
| | | | | Value | Value | Value | Value | Value | Value |
| Info Block | Info length | 0x1A00 | 1 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 |
| | CRC length | 0x1A01 | 1 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 |
| | CRC value | 0x1A02 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 0x1A04 | 1 | 0x2E | 0x2E | 0x2A | 0x2A | 0x26 | 0x26 |
| | Device ID | 0x1A05 | 1 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 |
| | Hardware revision | 0x1A06 | 1 | 0x30 | 0x30 | 0x30 | 0x30 | 0x30 | 0x30 |
| | Firmware revision | 0x1A07 | 1 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 |
| Die Record | Die Record Tag | 0x1A08 | 1 | 0x08 | 08 | 0x08 | 08 | 0x08 | 08 |
| | Die Record length | 0x1A09 | 1 | 0x0A | 0A | 0x0A | 0A | 0x0A | 0A |
| | Lot/Wafer ID | 0x1A0A | 4 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 0x1A0Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 0x1A10 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Test results | 0x1A12 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| ADC10 Calibration | ADC10 Calibration Tag | 0x1A14 | 1 | 0x05 | 0x05 | 0x05 | 0x05 | 0x05 | 0x05 |
| | ADC10 Calibration length | 0x1A15 | 1 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 | 0x10 |
| | ADC Gain Factor | 0x1A16 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC Offset | 0x1A18 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 0x1A1A | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 0x1A1C | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 0x1A1Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 0x1A20 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 0x1A22 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 0x1A24 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| REF User Calibration | REF Tag | 0x1A26 | 1 | 0x12 | 0x12 | 0x12 | 0x12 | 0x12 | 0x12 |
| | REF length | 0x1A27 | 1 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 | 0x06 |
| | REF 1.5-V Reference | 0x1A28 | 2 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |
| | REF 2.0-V Reference | 0x1A2A | 2 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |
| | REF 2.5-V Reference | 0x1A2C | 2 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |
| Timer_D0 Calibration | Timer_D Tag | 0x1A2E | 1 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 |

(1) NA = Not applicable

Table 59. 'F51x1 Device Descriptor Table⁽¹⁾ (continued)

| | Description | Address | Size bytes | 'F5171 RSB | 'F5171 DA | 'F5151 RSB | 'F5151 DA | 'F5131 RSB | 'F5131 DA |
|------------------------------|------------------------------|---------|------------|------------|-----------|------------|-----------|------------|-----------|
| | | | | Value | Value | Value | Value | Value | Value |
| | Timer_D length | 0x1A2F | 1 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 |
| | Timer_D 64-MHz frequency | 0x1A30 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 128-MHz frequency | 0x1A32 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 200-MHz frequency | 0x1A34 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 256-MHz frequency | 0x1A36 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| Timer_D1 Calibration | Timer_D Tag | 0x1A38 | 1 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 | 0x15 |
| | Timer_D length | 0x1A39 | 1 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 |
| | Timer_D 64-MHz frequency | 0x1A3A | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 128-MHz frequency | 0x1A3C | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 200-MHz frequency | 0x1A3E | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Timer_D 256-MHz frequency | 0x1A40 | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| Peripheral Descriptor | Peripheral Descriptor Tag | 0x1A42 | 1 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 |
| | Peripheral Descriptor Length | 0x1A43 | 1 | 0x51 | 0x51 | 0x51 | 0x51 | 0x51 | 0x51 |
| | BSL Memory | 0x1A44 | 2 | 0x8A08 | 0x8A08 | 0x8A08 | 0x8A08 | 0x8A08 | 0x8A08 |
| | Information Memory | 0x1A46 | 2 | 0x860C | 0x860C | 0x860C | 0x860C | 0x860C | 0x860C |
| | RAM | 0x1A48 | 2 | 0x2A0E | 0x2A0E | 0x2A0E | 0x2A0E | 0x280E | 0x280E |
| | Main Memory | 0x1A4A | 2 | 0x9240 | 0x9240 | 0x9060 | 0x9060 | 0x8E70 | 0x8E70 |
| | Delimiter | 0x1A4C | 1 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| | Peripheral count | 0x1A4D | 1 | 0x1B | 0x1B | 0x1B | 0x1B | 0x1B | 0x1B |
| | MSP430CPUXV2 | 0x1A4E | 2 | 0x2300 | 0x2300 | 0x2300 | 0x2300 | 0x2300 | 0x2300 |
| | SBW | 0x1A50 | 2 | 0x0F00 | 0x0F00 | 0x0F00 | 0x0F00 | 0x0F00 | 0x0F00 |
| | EEM-S | 0x1A52 | 2 | 0x0300 | 0x0300 | 0x0300 | 0x0300 | 0x0300 | 0x0300 |
| | TI BSL | 0x1A54 | 2 | 0xFC00 | 0xFC00 | 0xFC00 | 0xFC00 | 0xFC00 | 0xFC00 |
| | SFR | 0x1A56 | 2 | 0x4110 | 0x4110 | 0x4110 | 0x4110 | 0x4110 | 0x4110 |
| | PMM | 0x1A58 | 2 | 0x3002 | 0x3002 | 0x3002 | 0x3002 | 0x3002 | 0x3002 |
| | FCTL | 0x1A5A | 2 | 0x3802 | 0x3802 | 0x3802 | 0x3802 | 0x3802 | 0x3802 |
| | CRC16 | 0x1A5C | 2 | 0x3C01 | 0x3C01 | 0x3C01 | 0x3C01 | 0x3C01 | 0x3C01 |
| | CRC16_RB | 0x1A5E | 2 | 0x3D00 | 0x3D00 | 0x3D00 | 0x3D00 | 0x3D00 | 0x3D00 |
| | RAMCTL | 0x1A60 | 2 | 0x4400 | 0x4400 | 0x4400 | 0x4400 | 0x4400 | 0x4400 |
| | WDT_A | 0x1A62 | 2 | 0x4000 | 0x4000 | 0x4000 | 0x4000 | 0x4000 | 0x4000 |
| | UCS | 0x1A64 | 2 | 0x4801 | 0x4801 | 0x4801 | 0x4801 | 0x4801 | 0x4801 |
| | SYS | 0x1A66 | 2 | 0x4202 | 0x4202 | 0x4202 | 0x4202 | 0x4202 | 0x4202 |
| | Shared REF | 0x1A68 | 2 | 0xA003 | 0xA003 | 0xA003 | 0xA003 | 0xA003 | 0xA003 |
| | Port Mapping | 0x1A6A | 2 | 0x1001 | 0x1001 | 0x1001 | 0x1001 | 0x1001 | 0x1001 |
| | Port 1/2 | 0x1A6C | 2 | 0x5104 | 0x5104 | 0x5104 | 0x5104 | 0x5104 | 0x5104 |
| | Port 3/4 | 0x1A6E | 2 | 0x5202 | 0x5202 | 0x5202 | 0x5202 | 0x5202 | 0x5202 |
| | Port J | 0x1A70 | 2 | 0x5F10 | 0x5F10 | 0x5F10 | 0x5F10 | 0x5F10 | 0x5F10 |
| | TA0 | 0x1A72 | 2 | 0x610A | 0x610A | 0x610A | 0x610A | 0x610A | 0x610A |
| | MPY32 | 0x1A74 | 2 | 0x8510 | 0x8510 | 0x8510 | 0x8510 | 0x8510 | 0x8510 |
| | DMA with 3 channels | 0x1A76 | 2 | 0x4704 | 0x4704 | 0x4704 | 0x4704 | 0x4704 | 0x4704 |
| | USCI_A0/B0 | 0x1A78 | 2 | 0x900C | 0x900C | 0x900C | 0x900C | 0x900C | 0x900C |
| | COMP_B | 0x1A7A | 2 | 0xA830 | 0xA830 | 0xA830 | 0xA830 | 0xA830 | 0xA830 |
| | TIMER_D0 | 0x1A7C | 2 | 0xD624 | 0xD624 | 0xD624 | 0xD624 | 0xD624 | 0xD624 |
| | TIMER_D1 | 0x1A7E | 2 | 0x6D04 | 0x6D04 | 0x6D04 | 0x6D04 | 0x6D04 | 0x6D04 |
| | TEC_0 | 0x1A80 | 2 | 0x700C | 0x700C | 0x700C | 0x700C | 0x700C | 0x700C |
| | TEC_1 | 0x1A82 | 2 | 0x7002 | 0x7002 | 0x7002 | 0x7002 | 0x7002 | 0x7002 |
| Interrupts | COMP_B | 0x1A83 | 1 | 0xA8 | 0xA8 | 0xA8 | 0xA8 | 0xA8 | 0xA8 |
| | TEC_0 | 0x1A84 | 1 | 0x6D | 0x6D | 0x6D | 0x6D | 0x6D | 0x6D |

Table 59. 'F51x1 Device Descriptor Table⁽¹⁾ (continued)

| | Description | Address | Size bytes | 'F5171 RSB | 'F5171 DA | 'F5151 RSB | 'F5151 DA | 'F5131 RSB | 'F5131 DA |
|--------------|---------------|--------------------|---------------|---------------|--------------|---------------|--------------|---------------|--------------|
| | | | | Value | Value | Value | Value | Value | Value |
| | TIMER_D0 | 0x1A85 | 1 | 0x62 | 0x62 | 0x62 | 0x62 | 0x62 | 0x62 |
| | TIMER_D0 | 0x1A86 | 1 | 0x63 | 0x63 | 0x63 | 0x63 | 0x63 | 0x63 |
| | WDTIFG | 0x1A87 | 1 | 0x40 | 0x40 | 0x40 | 0x40 | 0x40 | 0x40 |
| | USCI_A0 | 0x1A88 | 1 | 0x90 | 0x90 | 0x90 | 0x90 | 0x90 | 0x90 |
| | USCI_B0 | 0x1A89 | 1 | 0x91 | 0x91 | 0x91 | 0x91 | 0x91 | 0x91 |
| | ADC10_A | 0x1A8A | 1 | 0xD0 | 0xD0 | 0xD0 | 0xD0 | 0xD0 | 0xD0 |
| | TA0.CCIFG0 | 0x1A8B | 1 | 0x60 | 0x60 | 0x60 | 0x60 | 0x60 | 0x60 |
| | TA0.CCIFG1..4 | 0x1A8C | 1 | 0x61 | 0x61 | 0x61 | 0x61 | 0x61 | 0x61 |
| | DMA | 0x1A8D | 1 | 0x46 | 0x46 | 0x46 | 0x46 | 0x46 | 0x46 |
| | TEC_1 | 0x1A8E | 1 | 0x6E | 0x6E | 0x6E | 0x6E | 0x6E | 0x6E |
| | TIMER_D1 | 0x1A8F | 1 | 0x64 | 0x64 | 0x64 | 0x64 | 0x64 | 0x64 |
| | TIMER_D1 | 0x1A90 | 1 | 0x65 | 0x65 | 0x65 | 0x65 | 0x65 | 0x65 |
| | Port P1 | 0x1A91 | 1 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 |
| | Port P2 | 0x1A92 | 1 | 0x51 | 0x51 | 0x51 | 0x51 | 0x51 | 0x51 |
| | delimiter | 0x1A93 | 1 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| Empty | Unused Memory | 0x1A94 - 0x1AB9 | | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |

REVISION HISTORY

| REVISION | COMMENTS |
|----------|--|
| SLAS619 | Product Preview release |
| SLAS619A | Production Data release |
| SLAS619B | Changed Table 7 . |
| SLAS619C | Changed Comparator_B V_{REF} MAX from $\pm 1\%$ to $\pm 1.5\%$ for all test conditions in Comparator_B . |
| SLAS619D | <p>Table 1, Corrected number of I/Os for all entries.</p> <p>Functional Block Diagram, MSP430F51x2 and Functional Block Diagram, MSP430F51x1, Corrected typo on P2 port name.</p> <p>Recommended Operating Conditions, Corrected typo in f_{SYSTEM} V_{CC} conditions on $V_{CORE} = 3$ row.</p> <p>PMM, Brown-Out Reset (BOR), Changed parameter descriptions for $V_{(DVCC_BOR_IT)}$ and $V_{(V_{CORE_BOR_IT})}$.</p> |
| SLAS619E | <p>Table 10, changed "SYSRSTIV, System Reset" interrupt event at offset 1Ch to Reserved.</p> <p>Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current, Changed some typical and maximum current numbers at 85°C.</p> <p>Table 46, Corrected note regarding USCI CLK function taking precedence over USCI STE function.</p> |
| SLAS619F | Removed all occurrences of ROOSC; does not apply to this device. |
| SLAS619G | <p>Recommended Operating Conditions, Added note regarding interaction between minimum V_{CC} and SVSH.</p> <p>Internal Reference, Low-Frequency Oscillator (REFO), Corrected t_{START} UNIT (changed from μA to μs).</p> |
| SLAS619H | <p>Recommended Operating Conditions, Added test conditions for typical characteristics.</p> <p>DCO Frequency, Added note (1).</p> <p>Table 58 and Table 59, Corrected addresses of the Timer_D0 and Timer_D1 device descriptors.</p> |
| SLAS619I | <p>REF, External Reference (MSP430F51x2 Devices Only), Changed note (1) from "12-bit accuracy" to "10-bit accuracy".</p> <p>Comparator_B, Changed description and symbol for T_{CB_REF}.</p> <p>Flash Memory, Changed I_{MERASE}, I_{BANK} values.</p> |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| MSP430F5131IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5131 | Samples |
| MSP430F5131IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5131 | Samples |
| MSP430F5131IRSB | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5131 | Samples |
| MSP430F5131IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5131 | Samples |
| MSP430F5132IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5132 | Samples |
| MSP430F5132IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5132 | Samples |
| MSP430F5132IRHAR | OBSOLETE | VQFN | RHA | 40 | | TBD | Call TI | Call TI | | | |
| MSP430F5132IRHAT | OBSOLETE | VQFN | RHA | 40 | | TBD | Call TI | Call TI | | | |
| MSP430F5132IRSB | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5132 | Samples |
| MSP430F5132IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5132 | Samples |
| MSP430F5151IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5151 | Samples |
| MSP430F5151IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5151 | Samples |
| MSP430F5151IRSB | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5151 | Samples |
| MSP430F5151IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5151 | Samples |
| MSP430F5152IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5152 | Samples |
| MSP430F5152IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5152 | Samples |
| MSP430F5152IRHAR | OBSOLETE | VQFN | RHA | 40 | | TBD | Call TI | Call TI | | | |
| MSP430F5152IRHAT | OBSOLETE | VQFN | RHA | 40 | | TBD | Call TI | Call TI | | | |
| MSP430F5152IRSB | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5152 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| MSP430F5152IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5152 | Samples |
| MSP430F5171IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5171 | Samples |
| MSP430F5171IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5171 | Samples |
| MSP430F5171IRSBR | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5171 | Samples |
| MSP430F5171IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5171 | Samples |
| MSP430F5172IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5172 | Samples |
| MSP430F5172IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430F5172 | Samples |
| MSP430F5172IRSBR | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5172 | Samples |
| MSP430F5172IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | M430 F5172 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

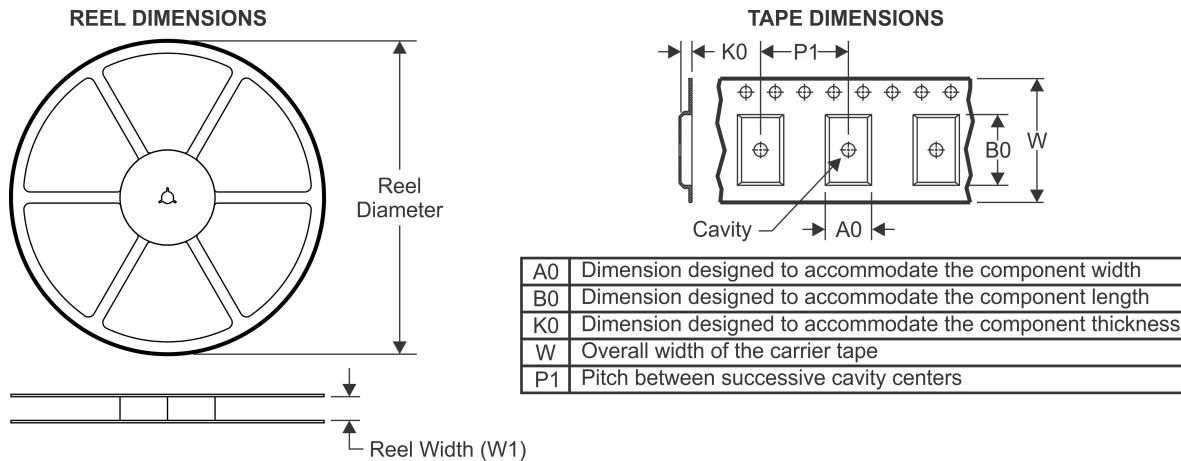
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

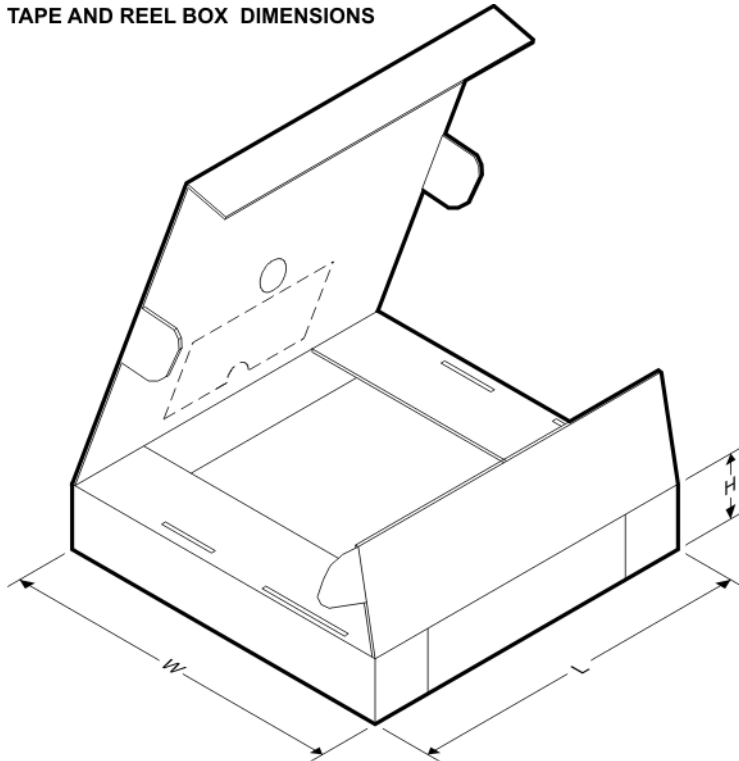
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F5131IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430F5131IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5131IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5132IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430F5132IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5132IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5151IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430F5151IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5151IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5152IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430F5152IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5152IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5171IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430F5171IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5171IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| MSP430F5172IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430F5172IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

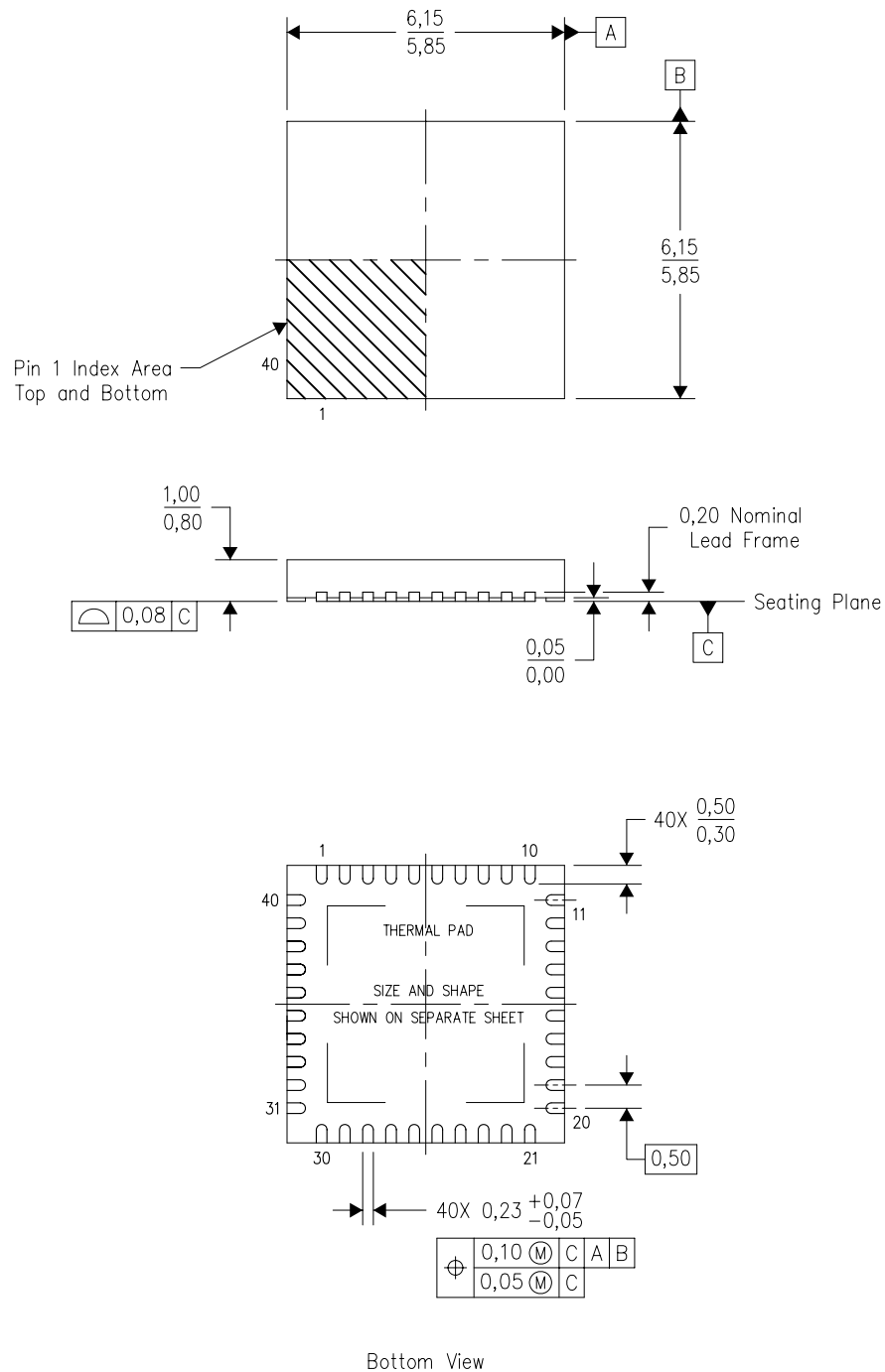
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F5131IDAR | TSSOP | DA | 38 | 2000 | 367.0 | 367.0 | 45.0 |
| MSP430F5131IRSB | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F5131IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5132IDAR | TSSOP | DA | 38 | 2000 | 367.0 | 367.0 | 45.0 |
| MSP430F5132IRSB | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F5132IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5151IDAR | TSSOP | DA | 38 | 2000 | 367.0 | 367.0 | 45.0 |
| MSP430F5151IRSB | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F5151IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5152IDAR | TSSOP | DA | 38 | 2000 | 367.0 | 367.0 | 45.0 |
| MSP430F5152IRSB | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F5152IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5171IDAR | TSSOP | DA | 38 | 2000 | 367.0 | 367.0 | 45.0 |
| MSP430F5171IRSB | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F5171IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5172IDAR | TSSOP | DA | 38 | 2000 | 367.0 | 367.0 | 45.0 |
| MSP430F5172IRSB | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



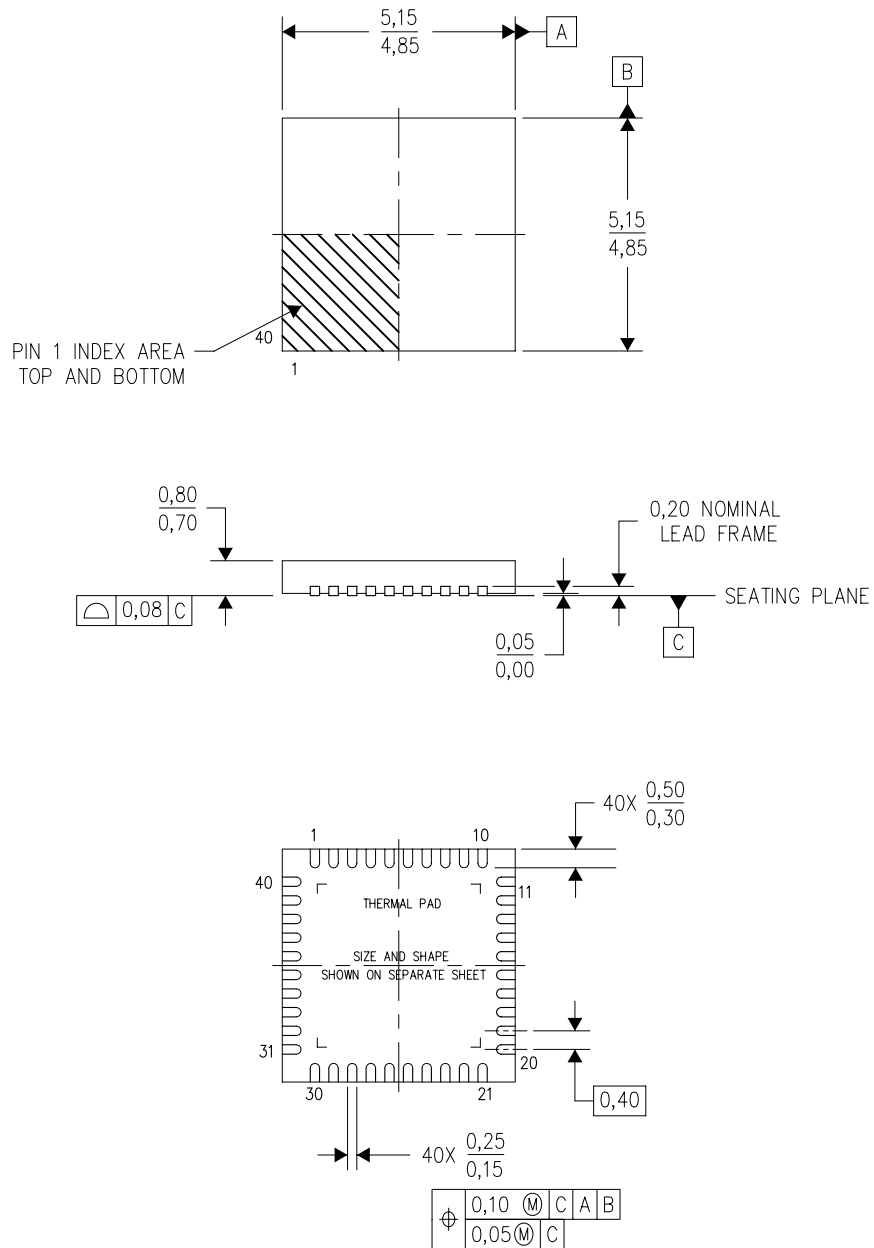
Bottom View

4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Package complies to JEDEC MO-220 variation VJJD-2.

RSB (S-PWQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4207182/C 05/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RSB (S-PWQFN-N40)

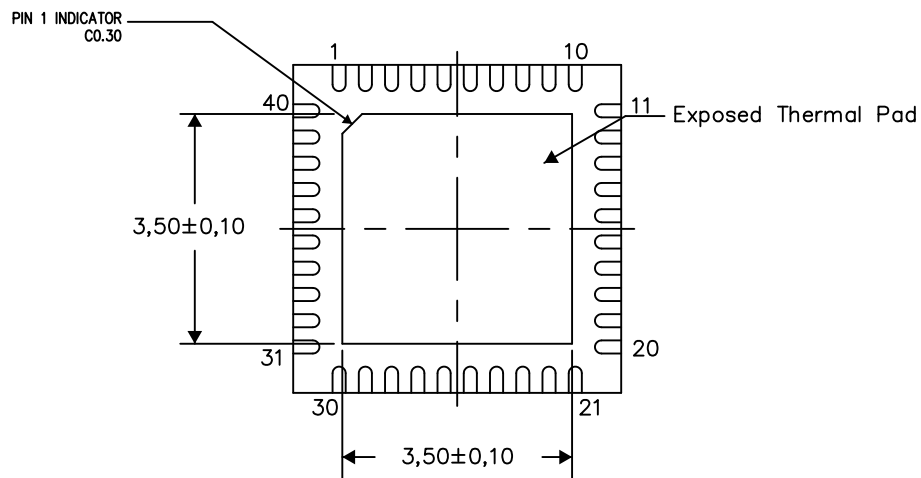
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

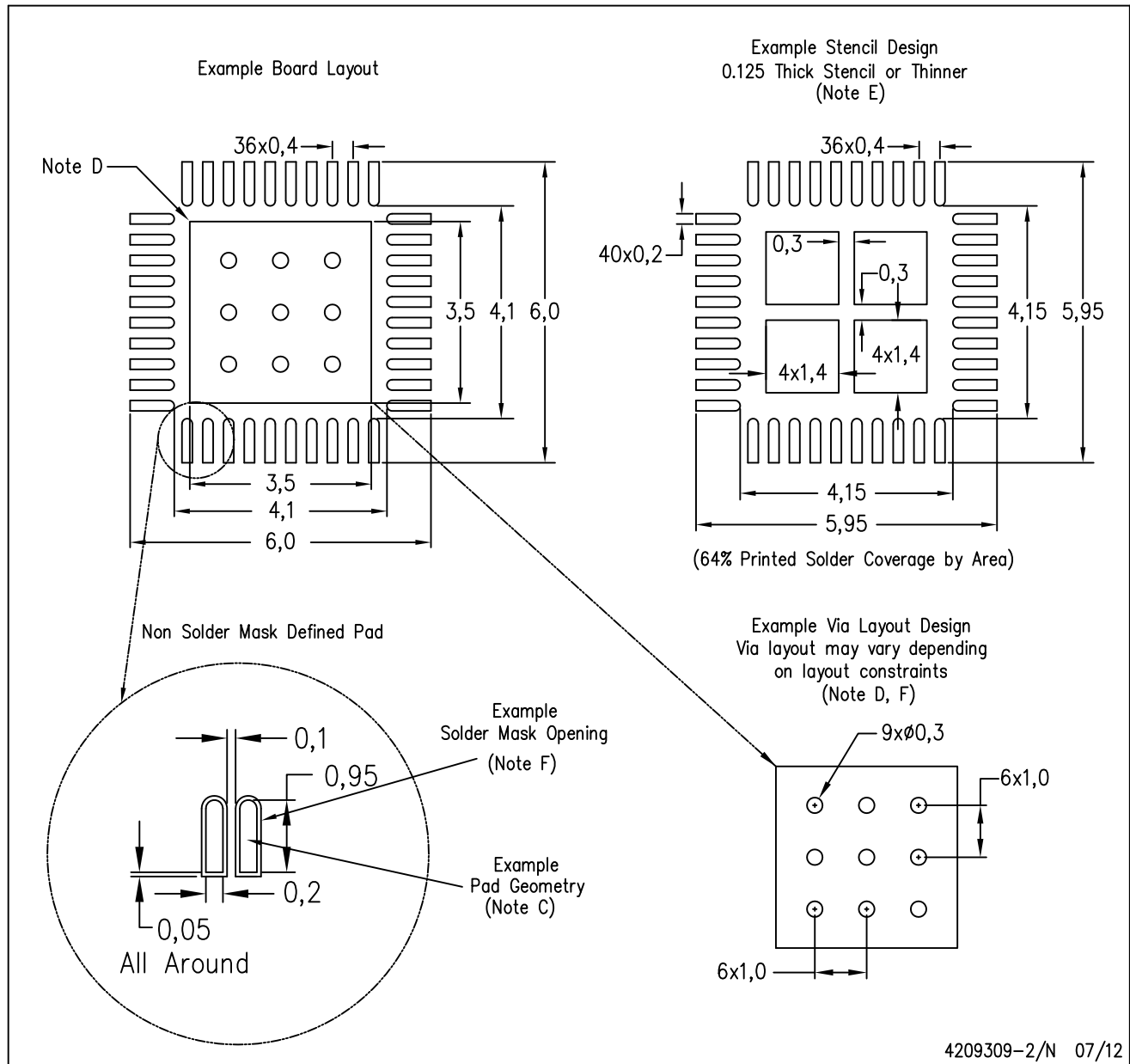
Exposed Thermal Pad Dimensions

4207183-2/P 06/12

NOTE: All linear dimensions are in millimeters

RSB (S-PWQFN-N40)

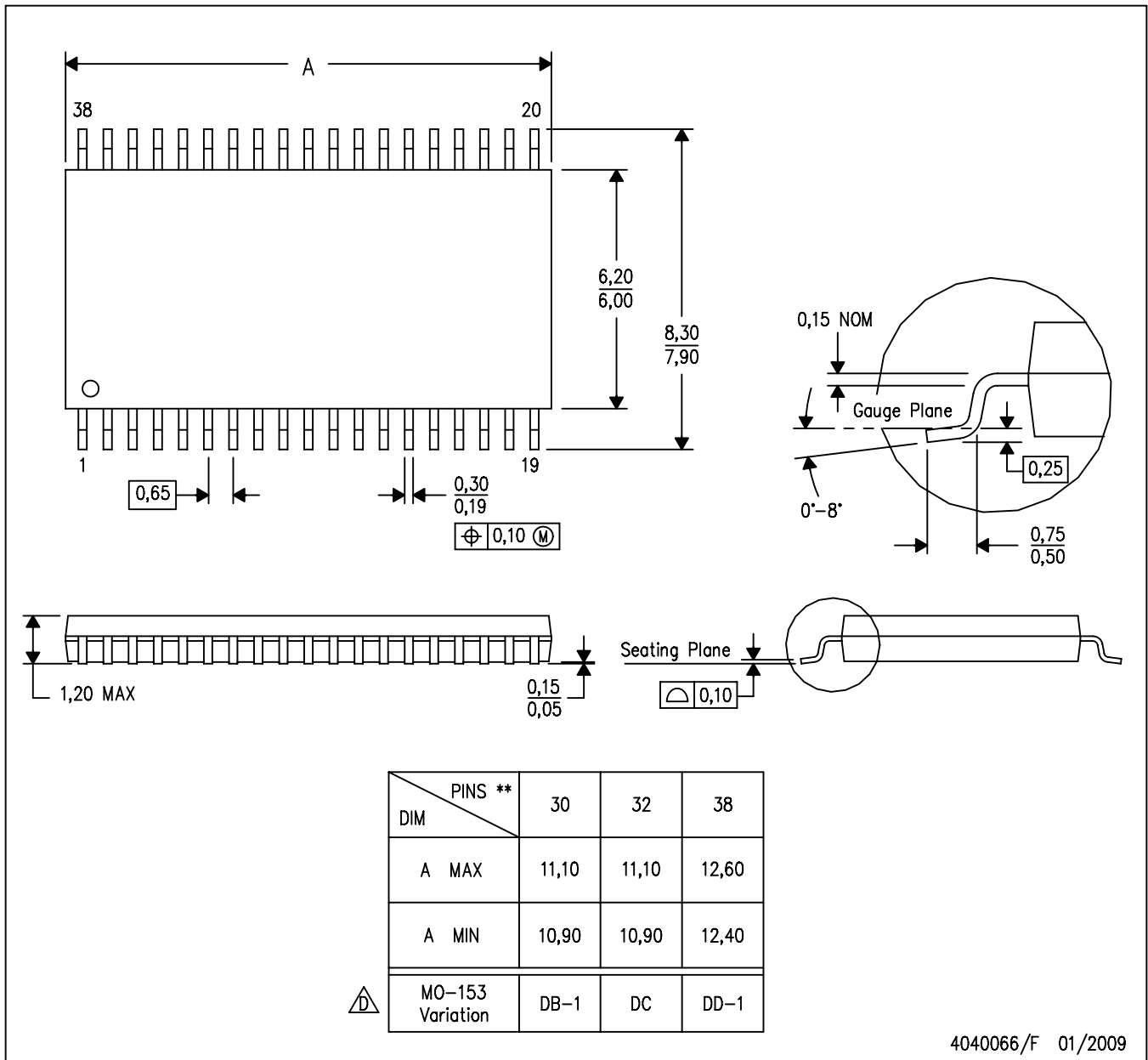
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DA (R-PDSO-G**)
 38 PIN SHOWN

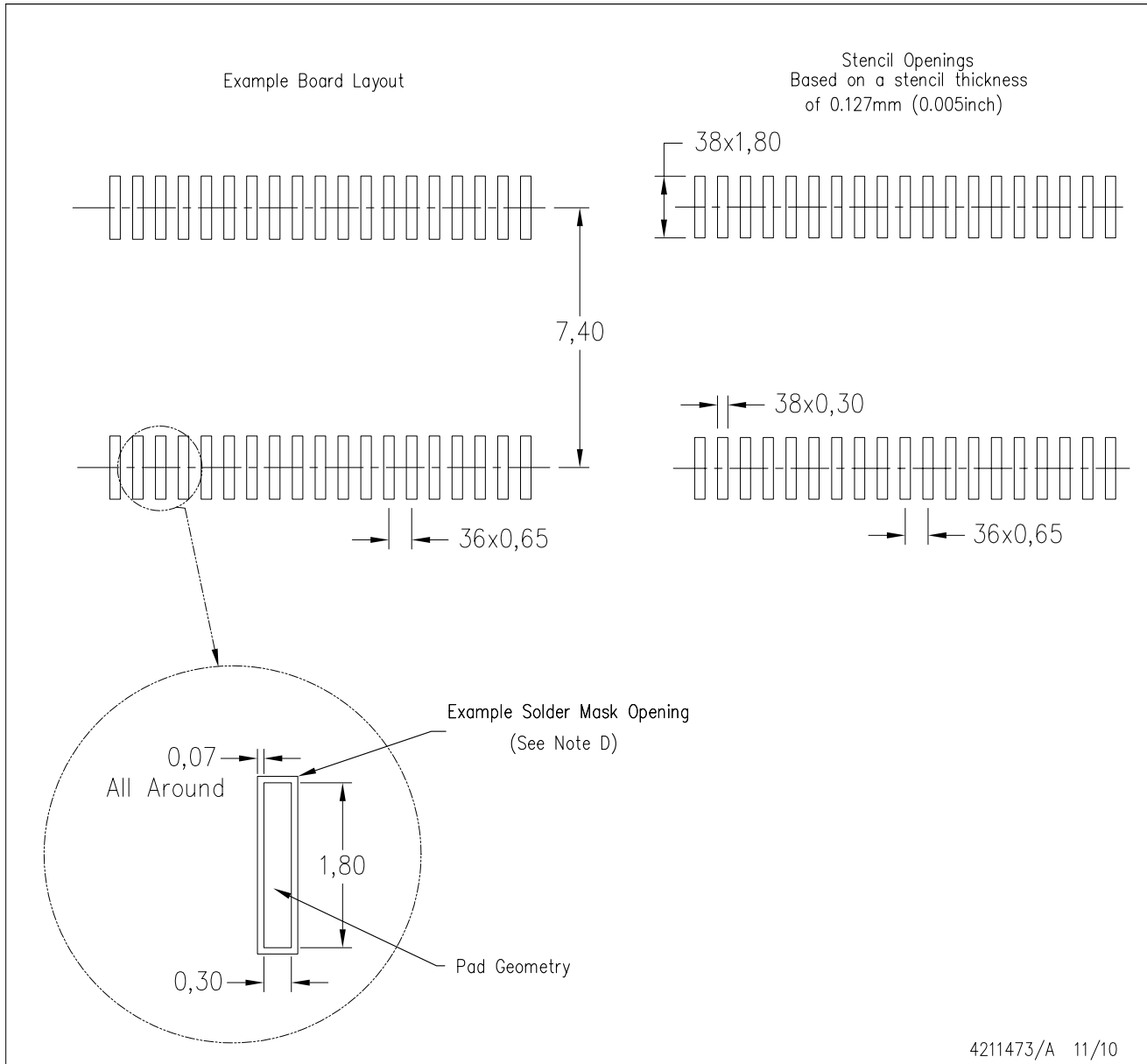
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-153, except 30 pin body length.

DA (R-PDSO-G38)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Contact the board fabrication site for recommended soldermask tolerances.

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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.