

Features

- Spread spectrum for EMI reduction
 - Wide spread % option
 - Center spread: from $\pm 0.125\%$ to $\pm 2\%$, $\pm 0.125\%$ step size
 - Down spread: -0.25% to -4% with -0.25% step size
 - Spread profile option: Triangular, Hershey-kiss
- Programmable rise/fall time for EMI reduction: 8 options, 0.25 to 40 ns
- Any frequency between 1 MHz and 141 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based XO's
- Excellent total frequency stability as low as ± 20 ppm
- Operating temperature from -40°C to 85°C .
- Low power consumption of 4.0 mA typical at 1.8V
- Pin1 modes: Standby, output enable, or spread disable
- Fast startup time of 5 ms
- LVC MOS output
- Industry-standard packages
 - QFN: 2.0×1.6 , 2.5×2.0 , $3.2 \times 2.5 \text{ mm}^2$
 - Contact [SiTime](#) for SOT23-5 ($2.9 \times 2.8 \text{ mm}^2$)
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Surveillance camera
- IP camera
- Industrial motors
- Flat panels
- Multi function printers
- PCI express



Electrical Specifications

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3V supply voltage.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|--------|------|------|------|--------------------|--|
| Frequency Range | | | | | | |
| Output Frequency Range | f | 1 | – | 141 | MHz | |
| Frequency Stability and Aging | | | | | | |
| Frequency Stability | F_stab | -20 | – | +20 | ppm | Inclusive of initial tolerance at 25°C , 1st year aging at 25°C , and variations over operating temperature, rated power supply voltage. Spread = Off. |
| | | -25 | – | +25 | ppm | |
| | | -50 | – | +50 | ppm | |
| Operating Temperature Range | | | | | | |
| Operating Temperature Range | T_use | -20 | – | +70 | $^{\circ}\text{C}$ | Extended Commercial |
| | | -40 | – | +85 | $^{\circ}\text{C}$ | Industrial |
| Supply Voltage and Current Consumption | | | | | | |
| Supply Voltage | Vdd | 1.62 | 1.8 | 1.98 | V | |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.7 | 3.0 | 3.3 | V | |
| | | 2.97 | 3.3 | 3.63 | V | |
| | | 2.25 | – | 3.63 | V | |
| Current Consumption | Idd | – | 5.6 | 6.5 | mA | No load condition, f = 40 MHz, Vdd = 2.5V to 3.3V |
| | | – | 5.0 | 5.5 | mA | No load condition, f = 40 MHz, Vdd = 1.8V |
| OE Disable Current | I_OD | – | 5.0 | 6.5 | mA | f = 40 MHz, Vdd = 2.5V to 3.3V, OE = GND, Output in high-Z state |
| | | – | 4.6 | 5.2 | mA | f = 40 MHz, Vdd = 1.8V, OE = GND, Output in high-Z state |
| Standby Current | I_std | – | 2.1 | 4.3 | μA | $\overline{\text{ST}}$ = GND, Vdd = 2.5V to 3.3V, Output is weakly pulled down |
| | | – | 0.4 | 1.5 | μA | $\overline{\text{ST}}$ = GND, Vdd = 1.8V, Output is weakly pulled down |

Table 1. Electrical Characteristics (continued)

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---------------------------------------|----------|------|------|------|------------|---|
| LVC MOS Output Characteristics | | | | | | |
| Duty Cycle | DC | 45 | – | 55 | % | |
| Rise/Fall Time | Tr, Tf | – | 1 | 2 | ns | Vdd = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%, default derive strength |
| | | – | 1.3 | 2.5 | ns | Vdd = 1.8V, 20% - 80%, default derive strength |
| | | – | – | 2 | ns | Vdd = 2.25V - 3.63V, 20% - 80%, default derive strength |
| Output High Voltage | VOH | 90% | – | – | Vdd | IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V) IOH = -2 mA (Vdd = 1.8V) |
| Output Low Voltage | VOL | – | – | 10% | Vdd | IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V) IOL = 2 mA (Vdd = 1.8V) |
| Input Characteristics | | | | | | |
| Input High Voltage | VIH | 70% | – | – | Vdd | Pin 1, OE or \overline{ST} |
| Input Low Voltage | VIL | – | – | 30% | Vdd | Pin 1, OE or \overline{ST} |
| Input Pull-up Impedance | Z_in | 50 | 87 | 150 | k Ω | Pin 1, OE logic high or logic low, or \overline{ST} logic high |
| | | 2 | – | – | M Ω | Pin 1, \overline{ST} logic low |
| Startup and Resume Timing | | | | | | |
| Startup Time | T_start | – | – | 5 | ms | Measured from the time Vdd reaches its rated minimum value |
| Enable/Disable Time | T_oe | – | – | 180 | ns | f = 40 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles |
| Resume Time | T_resume | – | – | 5 | ms | Measured from the time ST pin crosses 50% threshold |
| Spread Enable Time | T_sde | – | – | 4 | μ s | Measured from the time SD pin crosses 50% threshold |
| Spread Disable Time | T_sdde | – | – | 50 | μ s | Measured from the time SD pin crosses 50% threshold |
| Jitter | | | | | | |
| Cycle-to-cycle jitter | T_ccj | – | 10.5 | 15 | ps | f = 40 MHz, Vdd = 2.5 to 3.3V, Spread = ON(or OFF) |
| | | – | 8.5 | 12 | ps | f = 40 MHz, Vdd = 3.3V, Spread = ON(or OFF) |
| | | – | 12.5 | 22 | ps | f = 40 MHz, Vdd = 1.8V, Spread = ON(or OFF) |

Table 2. Spread Spectrum % ^[1,2]

| Ordering Code | Center Spread (%) | Down Spread (%) |
|---------------|-------------------|-----------------|
| A | ±0.125 | -0.25 |
| B | ±0.250 | -0.50 |
| C | ±0.390 | -0.78 |
| D | ±0.515 | -1.04 |
| E | ±0.640 | -1.29 |
| F | ±0.765 | -1.55 |
| G | ±0.905 | -1.84 |
| H | ±1.030 | -2.10 |
| I | ±1.155 | -2.36 |
| J | ±1.280 | -2.62 |
| K | ±1.420 | -2.91 |
| L | ±1.545 | -3.18 |
| M | ±1.670 | -3.45 |
| N | ±1.795 | -3.71 |
| O | ±1.935 | -4.01 |
| P | ±2.060 | -4.28 |

Table 3. Spread Profile

| Spread Profile |
|----------------|
| Triangular |
| Hershey-kiss |

Notes:

1. In both center spread and down spread modes, modulation rate is employed with a frequency of ~31.25 kHz.
2. Contact [SiTime](http://www.sitime.com) for wider spread options

Table 4. Pin Description

| Pin | Symbol | | Functionality |
|-----|--------------------------------|----------------|---|
| 1 | OE/ \overline{ST} / NC/SD | Output Enable | H ^[3] : specified frequency output L: output is high impedance. Only output driver is disabled. |
| | | Standby | H ^[3] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduced to I _{std} . |
| | | No Connect | Pin1 has no function (Any voltage between 0 and Vdd or Open) |
| | | Spread Disable | H: Spread = ON L: Spread = OFF |
| 2 | GND | Power | Electrical ground |
| 3 | OUT | Output | Oscillator output |
| 4 | VDD | Power | Power supply voltage ^[4] |

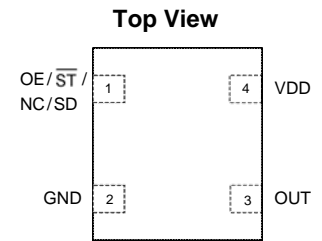


Figure 1. Pin Assignments

Notes:

- 3. In OE or \overline{ST} mode, a pull-up resistor of 10 k Ω or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
- 4. A capacitor of value 0.1 μ F or higher between Vdd and GND is required.

Table 5. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|--|------|------|--------------|
| Storage Temperature | -65 | 150 | $^{\circ}$ C |
| Vdd | -0.5 | 4 | V |
| Electrostatic Discharge | – | 2000 | V |
| Soldering Temperature (follow standard Pb free soldering guidelines) | – | 260 | $^{\circ}$ C |
| Junction Temperature ^[5] | – | 150 | $^{\circ}$ C |

Note:

- 5. Exceeding this temperature for extended period of time may damage the device.

Table 6. Maximum Operating Junction Temperature^[6]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|-------------------------------------|--|
| 70 $^{\circ}$ C | 80 $^{\circ}$ C |
| 85 $^{\circ}$ C | 95 $^{\circ}$ C |

Note:

- 6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 7. Environmental Compliance

| Parameter | Condition/Test Method |
|----------------------------|---------------------------|
| Mechanical Shock | MIL-STD-883F, Method 2002 |
| Mechanical Vibration | MIL-STD-883F, Method 2007 |
| Temperature Cycle | JESD22, Method A104 |
| Solderability | MIL-STD-883F, Method 2003 |
| Moisture Sensitivity Level | MSL1 @ 260 $^{\circ}$ C |

Timing Diagrams

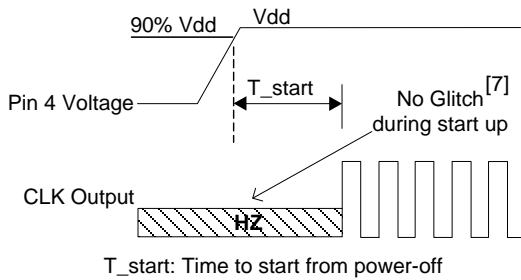


Figure 2. Startup Timing

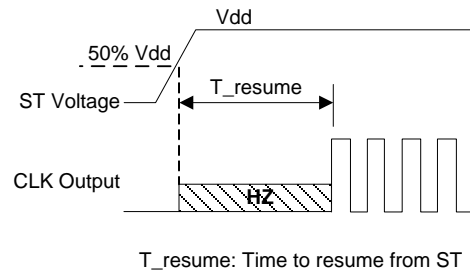


Figure 3. Standby Resume Timing (ST Mode Only)

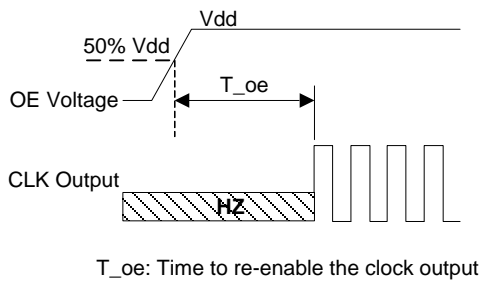


Figure 4. OE Enable Timing (OE Mode Only)

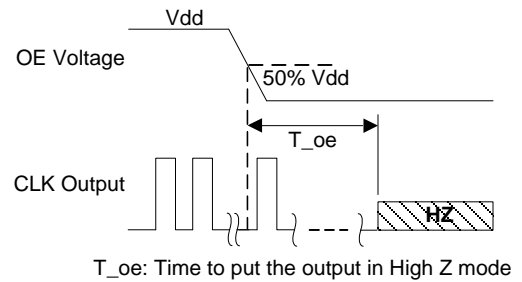


Figure 5. OE Disable Timing (OE Mode Only)

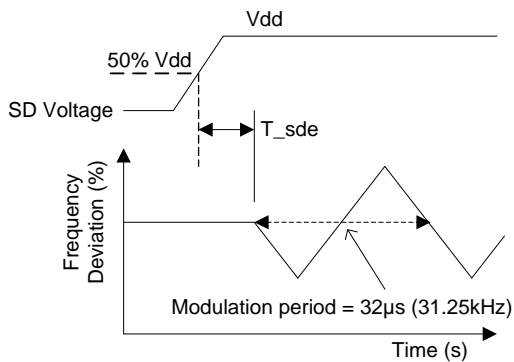


Figure 6. SD Enable Timing (SD Mode Only)

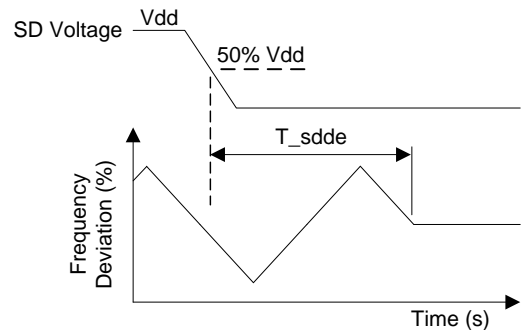


Figure 7. SD Diable Timing (SD Mode Only)

Note:

7. SiT9005 has "no runt" pulses and "no glitch" output during startup or resume.

Programmable Drive Strength

The SiT9005 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section: <http://www.sitime.com/support/application-notes>.

EMI Reduction by Slowing Rise/Fall Time

Figure 8 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

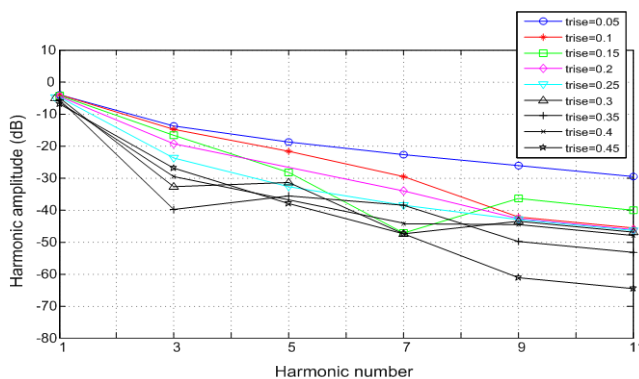


Figure 8. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The SiT9005 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the [Vdd = 1.8V Rise/Fall Times](#) for Specific C_{LOAD} to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT9005 device with default drive strength setting, the typical rise/fall time is 1.1 ns for 15 pF output load. The typical rise/fall time slows down to 2.9 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.9 ns by then increasing the drive strength setting on the SiT9005.

The SiT9005 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the [Vdd = 1.8V Rise/Fall Times](#) for Specific C_{LOAD} to determine the proper drive strength for the desired combination of output load vs. rise/fall time

SiT9005 Drive Strength Selection

Tables Table 1 through Table 12 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT9005 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.3V).
2. Select the capacitive load column that matches the application requirement (15 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables Table 1 through Table 12, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf}_{20/80}}$$

where Trf_{20/80} is the typical rise/fall time at 20% to 80% V_{dd}

Example 1

Calculate f_{MAX} for the following condition:

- V_{dd} = 3.3V (Table 12)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.6ns (rise/fall time part number code = Z)

Part number for the above example:

SiT9005AIZ14-33EB-105.12345



Drive strength code is inserted here. Default setting is “-”

Rise/Fall Time (20% to 80%) vs C_{LOAD} Tables

Table 8. V_{dd} = 1.8V Rise/Fall Times for Specific C_{LOAD}

| Rise/Fall Time Typ (ns) | | | | | |
|------------------------------------|------|-------|-------|-------|-------|
| Drive Strength \ C _{LOAD} | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 6.16 | 11.61 | 22.00 | 31.27 | 39.91 |
| A | 3.19 | 6.35 | 11.00 | 16.01 | 21.52 |
| R | 2.11 | 4.31 | 7.65 | 10.77 | 14.47 |
| B | 1.65 | 3.23 | 5.79 | 8.18 | 11.08 |
| T | 0.93 | 1.91 | 3.32 | 4.66 | 6.48 |
| E | 0.78 | 1.66 | 2.94 | 4.09 | 5.74 |
| U | 0.70 | 1.48 | 2.64 | 3.68 | 5.09 |
| F or "-": default | 0.65 | 1.30 | 2.40 | 3.35 | 4.56 |

Table 9. V_{dd} = 2.5V Rise/Fall Times for Specific C_{LOAD}

| Rise/Fall Time Typ (ns) | | | | | |
|------------------------------------|------|-------|-------|-------|-------|
| Drive Strength \ C _{LOAD} | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 4.13 | 8.25 | 12.82 | 21.45 | 27.79 |
| A | 2.11 | 4.27 | 7.64 | 11.20 | 14.49 |
| R | 1.45 | 2.81 | 5.16 | 7.65 | 9.88 |
| B | 1.09 | 2.20 | 3.88 | 5.86 | 7.57 |
| T | 0.62 | 1.28 | 2.27 | 3.51 | 4.45 |
| E or "-": default | 0.54 | 1.00 | 2.01 | 3.10 | 4.01 |
| U | 0.43 | 0.96 | 1.81 | 2.79 | 3.65 |
| F | 0.34 | 0.88 | 1.64 | 2.54 | 3.32 |

Table 10. V_{dd} = 2.8V Rise/Fall Times for Specific C_{LOAD}

| Rise/Fall Time Typ (ns) | | | | | |
|------------------------------------|------|-------|-------|-------|-------|
| Drive Strength \ C _{LOAD} | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.77 | 7.54 | 12.28 | 19.57 | 25.27 |
| A | 1.94 | 3.90 | 7.03 | 10.24 | 13.34 |
| R | 1.29 | 2.57 | 4.72 | 7.01 | 9.06 |
| B | 0.97 | 2.00 | 3.54 | 5.43 | 6.93 |
| T | 0.55 | 1.12 | 2.08 | 3.22 | 4.08 |
| E or "-": default | 0.44 | 1.00 | 1.83 | 2.82 | 3.67 |
| U | 0.34 | 0.88 | 1.64 | 2.52 | 3.30 |
| F | 0.29 | 0.81 | 1.48 | 2.29 | 2.99 |

Table 11. V_{dd} = 3.0V Rise/Fall Times for Specific C_{LOAD}

| Rise/Fall Time Typ (ns) | | | | | |
|------------------------------------|------|-------|-------|-------|-------|
| Drive Strength \ C _{LOAD} | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.60 | 7.21 | 11.97 | 18.74 | 24.30 |
| A | 1.84 | 3.71 | 6.72 | 9.86 | 12.68 |
| R | 1.22 | 2.46 | 4.54 | 6.76 | 8.62 |
| B | 0.89 | 1.92 | 3.39 | 5.20 | 6.64 |
| T or "-": default | 0.51 | 1.00 | 1.97 | 3.07 | 3.90 |
| E | 0.38 | 0.92 | 1.72 | 2.71 | 3.51 |
| U | 0.30 | 0.83 | 1.55 | 2.40 | 3.13 |
| F | 0.27 | 0.76 | 1.39 | 2.16 | 2.85 |

Table 12. V_{dd} = 3.3V Rise/Fall Times for Specific C_{LOAD}

| Rise/Fall Time Typ (ns) | | | | | |
|------------------------------------|------|-------|-------|-------|-------|
| Drive Strength \ C _{LOAD} | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.39 | 6.88 | 11.63 | 17.56 | 23.59 |
| A | 1.74 | 3.50 | 6.38 | 8.98 | 12.19 |
| R | 1.16 | 2.33 | 4.29 | 6.04 | 8.34 |
| B | 0.81 | 1.82 | 3.22 | 4.52 | 6.33 |
| T or "-": default | 0.46 | 1.00 | 1.86 | 2.60 | 3.84 |
| E | 0.33 | 0.87 | 1.64 | 2.30 | 3.35 |
| U | 0.28 | 0.79 | 1.46 | 2.05 | 2.93 |
| F | 0.25 | 0.72 | 1.31 | 1.83 | 2.61 |

Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) ^[8] | Recommended Land Pattern (Unit: mm) ^[9] |
|---|--|
| <p>2.0 x 1.6 x 0.75 mm</p> | |
| <p>2.5 x 2.0 x 0.75 mm</p> | |
| <p>3.2 x 2.5 x 0.75 mm</p> | |

Notes:

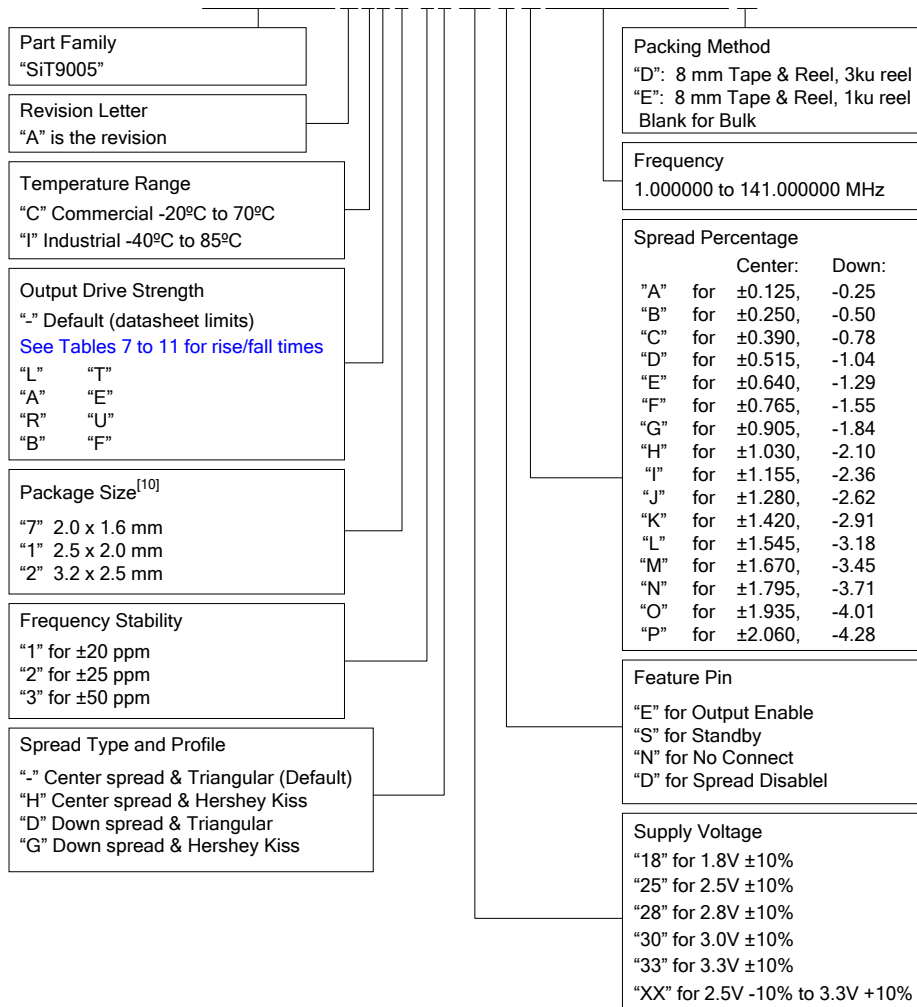
8. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
9. A capacitor of value 0.1 μ F or higher between Vdd and GND is required.

Ordering Information

The Part No. Guide is for reference only.

To customize and build an exact part number, use the SiTime [Part Number Generator](#).

SiT9005AI-71-18EA25.000625D



Note:

10. Contact [SiTime](#) for SOT23 (2.9 x 2.8 mm²) package

Table 13. Revision History

| Revision | Release Date | Change Summary |
|----------|--------------|----------------|
| 1.0 | 09/25/2017 | Final release |

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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