EXAR Powering Connectivity

SP3508

Rugged 3.3V, 20Mbps, 8 Channel Multiprotocol Transceiver with Programmable DCE/DTE and Termination Resistors

FEATURES

- Fast 20Mbps Differential Transmission Rates
- Internal Transceiver Termination Resistors for V.11 & V.35
- Interface Modes:
  - — RS-232 (V.28)
  - — X.21 (V.11)
  - — RS-449/V.36 (V.10 & V.11)
  - — EIA-530 (V.10 & V.11)
  - — EIA-530A (V.10 & V.11)
  - — V.35 (V.35 & V.28)
- Protocols are Software Selectable with 3-Bit Word
- Eight (8) Drivers and Eight (8) Receivers
- Termination Network Disable Option
- Internal Line or Digital Loopback for Diagnostic Testing
- Certified conformance to NET1/NET2 and TBR-1 TBR-2 by TUV Rheinland (TBR2/30451940.001/04)
- Easy Flow-Through Pinout
- +3.3V Only Operation
- Individual Driver and Receiver Enable/Disable Controls
- Operates in either DTE or DCE Mode

Now Available in Lead Free Packaging

Refer to page 9 for pinout

APPLICATIONS

- Router
- Frame Relay
- CSU
- DSU
- PBX
- Secure Communication Terminals

DESCRIPTION

The SP3508 is a monolithic device that supports eight (8) popular serial interface standards for Wide Area Network (WAN) connectivity. The SP3508 is fabricated using a low power BiCMOS process technology, and incorporates a regulated charge pump allowing +3.3V only operation. Exar's patented charge pump provides a regulated output of ±5.5V, which will provide enough voltage for compliant operation in all modes. Eight (8) drivers and eight (8) receivers can be configured via software for any of the above interface modes at any time. The SP3508 requires no additional external components for compliant operation for all of the eight (8) modes of operation other than six capacitors used for the internal charge pump. All necessary termination is integrated within the SP3508 and is switchable when V.35 drivers and V.35 receivers, or when V.11 receivers are used. The SP3508 provides the controls and transceiver availability for operating as either a DTE or DCE.

Additional features with the SP3508 include internal loopback that can be initiated in any of the operating modes by use of the $\overline{\text{LOOPBACK}}$ pin. While in loopback mode, receiver outputs are internally connected to driver inputs creating an internal signal path bypassing the serial communications controller for diagnostic testing. The SP3508 also includes a latch enable pin with the driver and receiver address decoder. The internal V.11 or V.35 termination can be switched off using a control pin (TERM_OFF) for monitoring applications. All eight (8) drivers and receivers in the SP3508 include separate enable pins for added convenience. The SP3508 is ideal for WAN serial ports in networking equipment such as routers, access concentrators, network muxes, DSU/CSU's, networking test equipment, and other access devices.

ABSOLUTE MAXIMUM RATINGS

V_{CC} ....+7V
Input Voltages:
Logic .... -0.3V to (V_{CC}+0.5V)
Drivers....................................... -0.3V to (V_{CC}+0.5V)
Receivers ....±15.5V
Output Voltages:
Logic .... -0.3V to (V_{CC}+0.5V)
Drivers...±12V
Receivers .... -0.3V to (V_{CC}+0.5V)
Storage Temperature...................................-65°C to +150°C
Power Dissipation..1520mW
(derate 19.0mW/°C above +70°C)
Junction Temperature T_J.. +141°C

Package Derating:
$ø_{JA}$ ....36.9 °C/W
$ø_{JC}$ ....6.5 °C/W

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 100-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Exar ships the 100-pin LQFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

ELECTRICAL SPECIFICATIONS

T_A = 0 to 70°C and V_{CC} = 3.3V ± 5% unless otherwise noted. The ♦ denotes the specifications which apply over the full operating temperature range (-40°C to +85°C), unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.		UNITS	CONDITIONS
LOGIC INPUTS						
V_{IL}			0.8	♦	V	
V_{IH}	2.0			♦	V	
LOGIC OUTPUTS						
V_{OL}			0.4	♦	V	I_{OUT} = -3.2mA
V_{OH}	V_{CC} - 0.6	V_{CC} - 0.3		♦	V	I_{OUT} = 1.0mA
V.28 DRIVER DC Parameters (OUTPUTS)						
Open Circuit Voltage			+/-10	♦	V	Per Figure 1
Loaded Voltage	+/-5.0			♦	V	Per Figure 2
Short-Circuit Current			+/-100	♦	mA	Per Figure 4
Power-Off Impedance	300			♦	Ω	Per Figure 5
V.28 DRIVER AC Parameters (Outputs)						V_{CC} = 3.3V for AC parameters
Transition Time			1.5	♦	µs	Per Figure 6, +3V to -3V
Instantaneous Slew Rate			30		V/ µs	Per Figure 3
Propagation Delay: t_{PHL}	0.5	1.0	3.0	♦	µs	
Propagation Delay: t_{PLH}	0.5	1.0	3.0	♦	µs	
Max. Transmission Rate	120	230		♦	kbps	

T_A = 0 to 70°C and V_{CC} = 3.3V ± 5% unless otherwise noted. The ♦ denotes the specifications which apply over the full operating temperature range (-40°C to +85°C), unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.		UNITS	CONDITIONS
V.28 RECEIVER DC Parameters (Inputs)						
Input Impedance	3		7	♦	kΩ	Per Figure 7
Open-Circuit Bias			+2.0	♦	V	Per Figure 8
HIGH Threshold		1.7	3.0	♦	V	
LOW Threshold	0.8	1.2		♦	V	
V.28 RECEIVER AC Parameters						V_{CC} = 3.3V for AC parameters
Propagation Delay: t_{PHL}		100	500		ns	
Propagation Delay: t_{PLH}		100	500		ns	
Max. Transmission Rate	120	230			kbps	
V.10 DRIVER DC Parameters (Outputs)						
Open Circuit Voltage	+/-4.0		+/-6.0	♦	V	Per Figure 9
Test-Terminated Voltage	$0.9V_{CC}$				V	Per Figure 10
Short-Circuit Current			+/-150		mA	Per Figure 11
Power-Off Current			+/-100	♦	µA	Per Figure 12
V.10 DRIVER AC Parameters (Outputs)						V_{CC} = 3.3V for AC parameters
Transition Time			200	♦	ns	Per Figure 13, 10% to 90%
Propagation Delay: t_{PHL}		100	500	♦	ns	
Propagation Delay: t_{PLH}		100	500	♦	ns	
Max. Transmission Rate	120			♦	kbps	
V.10 RECEIVER DC Parameters (Inputs)						
Input Current	-3.25		+3.25		mA	Per Figures 14 and 15
Input Impedance	4			♦	kΩ	
Sensitivity			+/-0.3	♦	V	
V.10 RECEIVER AC Parameters						V_{CC} = 3.3V for AC parameters
Propagation Delay: t_{PHL}		120	250	♦	ns	
Propagation Delay: t_{PLH}		120	250	♦	ns	
Max. Transmission Rate	120			♦	kbps	

T_A = 0 to 70°C and V_{CC} = 3.3V ± 5% unless otherwise noted. The ♦ denotes the specifications which apply over the full operating temperature range (-40°C to +85°C), unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.		UNITS	CONDITIONS
V.11 DRIVER DC Parameters (Outputs)						
Open Circuit Voltage (V_{OC})			+/-6.0	♦	V	Per Figure 16
Test Terminated Voltage	+/-2.0			♦	V	Per Figure 17
	0.5(V_{OC})			♦	V	
Balance			+/-0.4		V	Per Figure 17
Offset			+3.0	♦	V	Per Figure 17
Short-Circuit Current			+/-150	♦	mA	Per Figure 18
Power-Off Current			+/-100	♦	µA	Per Figure 19
V.11 DRIVER AC Parameters (Outputs)						V_{CC} = 3.3V for AC parameters
Transition Time			10	♦	ns	Per Figures 21 and 35, 10% to 90% using C_L = 50pF
Propagation Delay: t_{PHL}		30	85	♦	ns	Per Figures 32 and 35
Propagation Delay: t_{PLH}		30	85	♦	ns	Per Figures 32 and 35
Differential Skew		5	10	♦	ns	Per Figures 32 and 35
Max. Transmission Rate	20			♦	Mbps	
V.11 RECEIVER DC Parameters (Inputs)						
Common Mode Range	-7		+7	♦	V	
Sensitivity			+/-0.2	♦	V	
Input Current	-3.25		+3.25		mA	Per Figures 20 and 22; Power on or off
Current with 100Ω Termination			+/-60		mA	Per Figures 23 and 24
Input Impedance	4			♦	kΩ	
V.11 RECEIVER AC Parameters						V_{CC} = 3.3V for AC parameters using CL = 50pF
Propagation Delay: t_{PHL}		30	85		ns	Per Figures 32 and 37
Propagation Delay: t_{PLH}		30	85		ns	Per Figures 32 and 37
Skew		5	10		ns	Per Figure 32
Max. Transmission Rate	20				Mbps	

T_A = 0 to 70°C and V_{CC} = 3.3V ± 5% unless otherwise noted. The ♦ denotes the specifications which apply over the full operating temperature range (-40°C to +85°C), unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.		UNITS	CONDITIONS
V.35 DRIVER DC Parameters (Outputs)						
Open Circuit Voltage			+/-1.20		V	Per Figure 16
Test Terminated Voltage	+/-0.44		+/-0.66		V	Per Figure 25
Offset			+/-0.6	♦	V	Per Figure 25
Output Overshoot	$-0.2V_{ST}$		$+0.2V_{ST}$	♦	V	Per Figure 25; V_{ST} = Steady State value
Source Impedance	50		150	♦	Ω	Per Figure 26; $Z_S = V_2/V_1 \times 50$
Short-Circuit Impedance	135		165		Ω	Per Figure 27
V.35 DRIVER AC Parameters (Outputs)						V_{CC} = 3.3V for AC parameters
Transition Time			20	♦	ns	
Propagation Delay: t_{PHL}		30	85	♦	ns	Per Figures 32 and 35; C_L = 20pF
Propagation Delay: t_{PLH}		30	85	♦	ns	Per Figures 32 and 35; C_L = 20pF
Differential Skew			5	♦	ns	Per Figures 32 and 35; C_L = 20pF
Max. Transmission Rate	20			♦	Mbps	
V.35 RECEIVER DC Parameters (Inputs)						
Sensitivity		+/-50	+/-200	♦	mV	
Source Impedance	90		110		Ω	Per Figure 29; $Z_S = V_2/V_1 \times 50\Omega$
Short-Circuit Impedance	135		165		Ω	Per Figure 30
V.35 RECEIVER AC Parameters						V_{CC} = 3.3V for AC parameters
Propagation Delay: t_{PHL}		30	85		ns	Per Figures 32 and 37; C_L = 20pF
Propagation Delay: t_{PLH}		30	85		ns	Per Figures 32 and 37; C_L = 20pF
Skew		5	10		ns	Per Figure 32; C_L = 20pF
Max. Transmission Rate	20				Mbps	
TRANSCEIVER LEAKAGE CURRENTS						
Driver Output 3-State Current			200		μA	Per Figure 31; Drivers Disabled
Receiver Output 3-State Current		1	10		μA	D_X = 111

T_A = 0 to 70°C and V_{CC} = 3.3V ± 5% unless otherwise noted. The ♦ denotes the specifications which apply over the full operating temperature range (-40°C to +85°C), unless otherwise specified.

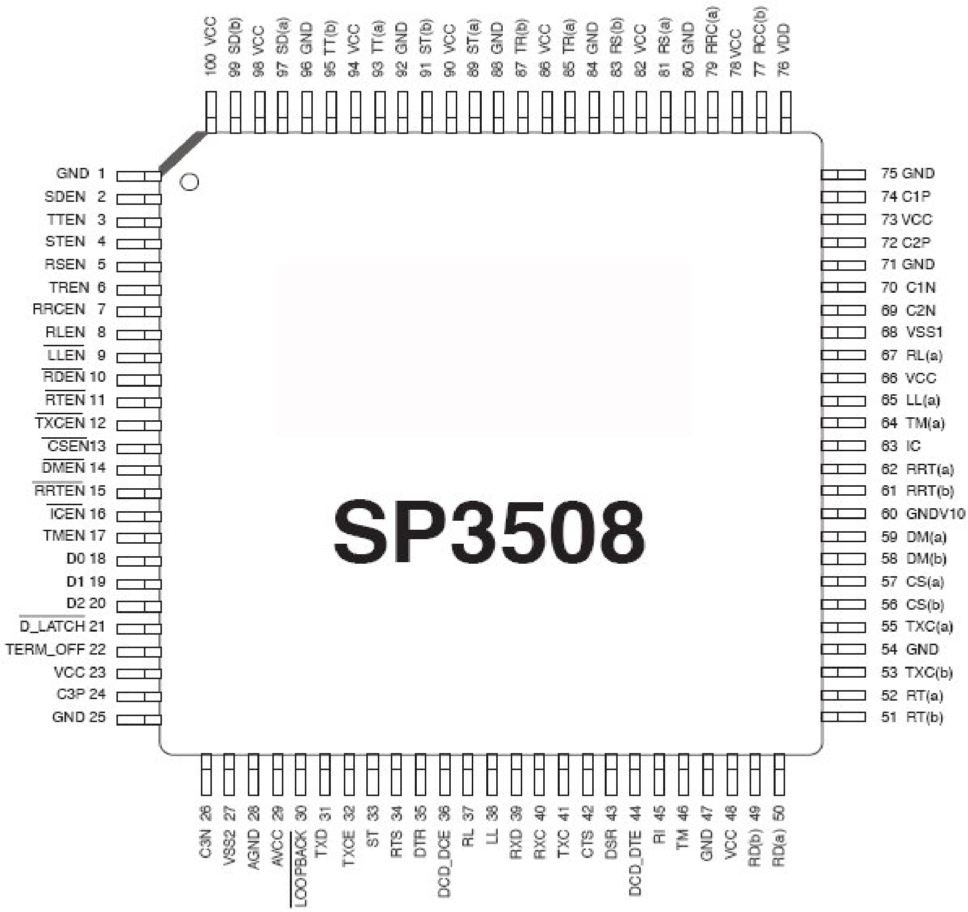
PARAMETER	MIN.	TYP.	MAX.		UNITS	CONDITIONS
POWER REQUIREMENTS						
V_{CC}	3.15	3.3	3.45		V	
I_{CC} (No Mode Selected)		1		♦	µA	All I_{CC} values are with V_{CC} = +3.3V
(V.28 / RS-232)		95		♦	mA	f_{IN} = 230kbps; Drivers active and loaded
(V.11 / RS-422)		230		♦	mA	f_{IN} = 20Mbps; Drivers active and loaded
(EIA-530 & RS-449)		270		♦	mA	f_{IN} = 20Mbps; Drivers active and loaded
(V.35)		170		♦	mA	V.35 @ f_{IN} = 20Mbps, V.28 @ f_{IN} = 230kbps

T_A = 0 to 70°C and V_{CC} = 3.3V ± 5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	Units	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.70	5.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.40	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.40	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.15	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.20	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 100pF, **Fig. 33 & 39**; S_2 closed
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		2.80	10.0	µs	C_L = 100pF, **Fig. 33 & 36**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, **Fig. 33 & 36**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 33 & 36**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 33 & 36**; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		2.60	10.0	µs	C_L = 100pF, **Fig. 33 & 36**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, **Fig. 33 & 36**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 33 & 36**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 15pF, **Fig. 33 & 36**; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.12	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, **Fig. 34 & 37**; S_2 closed

T_A = 0 to 70°C and V_{CC} = +3.3V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, **Fig. 34** & **38**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, **Fig. 34** & **38**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 34** & **38**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 34** & **38**; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, **Fig. 34** & **38**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, **Fig. 34** & **38**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 34** & **38**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, **Fig. 34** & **38**; S_2 closed
TRANSCEIVER TO TRANSCEIVER SKEW					(per Figures 32, 35, 37)
RS-232 Driver		100		ns	[(t_{PHL})Tx1 – (t_{PHL})Txn]
		100		ns	[(t_{PLH})Tx1 – (t_{PLH})Txn]
RS-232 Receiver		20		ns	[(t_{PHL})Rx1 – (t_{PHL})Rxn]
		20		ns	[(t_{PLH})Rx1 – (t_{PLH})Rxn]
RS-422 Driver		2		ns	[(t_{PHL})Tx1 – (t_{PHL})Txn]
		2		ns	[(t_{PLH})Tx1 – (t_{PLH})Txn]
RS-422 Receiver		3		ns	[(t_{PHL})Rx1 – $(t_{PHL:})$Rxn]
		3		ns	[(t_{PLH})Rx1 – (t_{PLH})Rxn]
RS-423 Driver		5		ns	[(t_{PHL})Tx2 – (t_{PHL})Txn]
		5		ns	[(t_{PLH})Tx2 – (t_{PLH})Txn]
RS-423 Receiver		5		ns	[(t_{PHL})Rx2 – (t_{PHL})Rxn]
		5		ns	[(t_{PLH})Rx2 – (t_{PLH})Rxn]
V.35 Driver		4		ns	[(t_{PHL})Tx1 – (t_{PHL})Txn]
		4		ns	[(t_{PLH})Tx1 – (t_{PLH})Txn]
V.35 Receiver		6		ns	[(t_{PHL})Rx1 – (t_{PHL})Rxn]
		6		ns	[(t_{PLH})Rx1 – (t_{PLH})Rxn]


SP3508
GND 1
SDEN 2
TTEN 3
STEN 4
RSEN 5
TREN 6
RRCEN 7
RLEN 8
LLEN 9
RDEN 10
RTEN 11
TXCEN 12
CSEN 13
DMEN 14
RRTEN 15
ICEN 16
TMEN 17
D0 18
D1 19
D2 20
D_LATCH 21
TERM_OFF 22
VCC 23
C3P 24
GND 25
C3N 26
VSS2 27
AGND 28
AVCC 29
LOOPBACK 30
TXD 31
TXCE 32
ST 33
RTS 34
DTR 35
DCD_DCE 36
RL 37
LL 38
RXD 39
RXC 40
TXC 41
CTS 42
DSR 43
DCD_DTE 44
RI 45
TM 46
GND 47
VCC 48
RD(b) 49
RD(a) 50
51 RT(b)
52 RT(a)
53 TXC(b)
54 GND
55 TXC(a)
56 CS(b)
57 CS(a)
58 DM(b)
59 DM(a)
60 GNDV10
61 RRT(b)
62 RRT(a)
63 IC
64 TM(a)
65 LL(a)
66 VCC
67 RL(a)
68 VSS1
69 C2N
70 C1N
71 GND
72 C2P
73 VCC
74 C1P
75 GND
76 VDD
77 RCC(b)
78 VCC
79 RRC(a)
80 GND
81 RS(a)
82 VCC
83 RS(b)
84 GND
85 TR(a)
86 VCC
87 TR(b)
88 GND
89 ST(a)
90 VCC
91 ST(b)
92 GND
93 TT(a)
94 VCC
95 TT(b)
96 GND
97 SD(a)
98 VCC
99 SD(b)
100 VCC

SP3508 Pin Designation		
Pin Number	Pin Name	Description
1	GND	Signal Ground
2	SDEN	TxD Driver Enable Input
3	TTEN	TxCE Driver Enable Input
4	STEN	ST Driver Enabe Input
5	RSEN	RTS Driver Enable Input
6	TREN	DTR Driver Enable Input
7	RRCEN	DCD Driver Enable Input
8	RLEN	RL Driver Enable Input
9	LLEN#	LL Driver Enable Input
10	RDEN#	RxD Receiver Enabe Input
11	RTEN#	RxC Receiver Enable Input
12	TxCEN#	TxC Receiver Enable Input
13	CSEN#	CTS Receiver Enable Input
14	DMEN#	DSR Receiver Enable Input
15	RRTEN#	DCD_{DTE} Receiver Enable Input
16	ICEN#	RI Receiver Enable Input
17	TMEN	TM Receiver Enable Input
18	D0	Mode Select Input
19	D1	Mode Select Input
20	D2	Mode Select Input
21	DLATCH#	Decoder Latch Input
22	TERM_OFF	Termination Disable Input
23	VCC	Power Supply Input
24	C3P	Charge Pump Capacitor
25	GND	Signal Ground

SP3508 Pin Designation		
Pin Number	Pin Name	Description
26	C3N	Charge Pump Capacitor
27	VSS2	Minus VCC
28	AGND	Signal Ground
29	AVCC	Power Supply Input
30	LOOPBACK#	Loopback Mode Enable Input
31	TxD	TxD Driver TTL Input
32	TxCE	TxCE Driver TTL input
33	ST	ST Driver TTL Input
34	RTS	RTS Driver TTL Input
35	DTR	DTR Driver TTL Input
36	DCD_DCE	DCD_{DCE} Driver TTL Input
37	RL	RL Driver TTL Input
38	LL	LL Driver TTL Input
39	RxD	RxD Receiver TTL Output
40	RxC	RxC Receiver TTL Output
41	TxC	TxC Receiver TTL Output
42	CTS	CTS Receiver TTL Output
43	DSR	DSR Receiver TTL Output
44	DCD_DTE	DCD_{DTE} Receiver TTL Output
45	RI	RI Receiver TTL Output
46	TM	TM Receiver TTL Output
47	GND	Signal Ground
48	VCC	Power Supply Input
49	RD(B)	RxD Non-Inverting Input
50	RD(A)	RxD Inverting Input

SP3508 Pin Designation

Pin Number	Pin Name	Description
51	RT(B)	RxC Non-Inverting Input
52	RT(A)	RxC Inverting Input
53	TxC(B)	TxC Non-Inverting Input
54	GND	Signal Ground
55	TxC(A)	TxC Inverting Input
56	CS(B)	CTS Non-Inverting Input
57	CS(A)	CTS Inverting Input
58	DM(B)	DSR Non-Inverting Input
59	DM(A)	DSR Inverting Input
60	GNDV10	V.10 RX Reference Node
61	RRT(B)	DCD_{DTE} Non-Inverting Input
62	RRT(A)	DCD_{DTE} Inverting Input
63	IC	RI Receiver Input
64	TM(A)	TM Receiver Input
65	LL(A)	LL Driver Output
66	VCC	Power Supply Input
67	RL(A)	RL Driver Output
68	VSS1	-2xVCC Charge Pump Output
69	C2N	Charge Pump Capacitor
70	C1N	Charge Pump Capacitor
71	GND	Signal Ground
72	C2P	Charge Pump Capacitor
73	VCC	Power Supply Input
74	C1P	Charge Pump Capacitor
75	GND	Signal Ground

SP3508 Pin Designation

Pin Number	Pin Name	Description
76	VDD	2xVCC Charge Pump Output
77	RRC(B)	DCD_{DCE} Non-Inverting Output
78	VCC	Power Supply Input
79	RRC(A)	DCD_{DCE} Inverting Output
80	GND	Signal Ground
81	RS(A)	RTS Inverting Output
82	VCC	Power Supply Input
83	RS(B)	RTS Non-Inverting Output
84	GND	Signal Ground
85	TR(A)	DTR Inverting Output
86	VCC	Power Supply Input
87	TR(B)	DTR Non-Inverting Output
88	GND	Signal Ground
89	ST(A)	ST Inverting Output
90	VCC	Power Supply Input
91	ST(B)	ST Non-Inverting Output
92	GND	Signal Ground
93	TT(A)	TxCE Inverting Output
94	VCC	Power Supply Input
95	TT(B)	TxCE Non-Inverting Output
96	GND	Signal Ground
97	SD(A)	TxD Inverting Output
98	VCC	Power Supply Input
99	SD(B)	TxD Non-Inverting Output
100	VCC	Power Supply Input

SP3508 Driver Table

Driver Output Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (V.36)	X.21 Mode (V.11)	Shutdown	Suggested Signal
MODE (D0, D1, D2)	001	010	011	100	101	110	111	
T_1OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxD(a)
T_1OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxD(b)
T_2OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxCE(a)
T_2OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxCE(b)
T_3OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DCE(a)
T_3OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DCE(b)
T_4OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	RTS(a)
T_4OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	RTS(b)
T_5OUT(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DTR(a)
T_5OUT(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DTR(b)
T_6OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DCE(a)
T_6OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DCE(b)
T_7OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RL
T_8OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	LL

Table 1. Driver Mode Selection

SP3508 Receiver Table

Receiver Input Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (V.36)	X.21 Mode (V.11)	Shutdown	Suggested Signal
MODE (D0, D1, D2)	001	010	011	100	101	110	111	
R_1IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxD(a)
R_1IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxD(b)
R_2IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxC(a)
R_2IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxC(b)
R_3IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DTE(a)
R_3IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DTE(b)
R_4IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	CTS(a)
R_4IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	CTS(b)
R_5IN(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DSR(a)
R_5IN(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DSR(b)
R_6IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DTE(a)
R_6IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DTE(b)
R_7IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RI
R_8IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	TM

Table 2. Receiver Mode Selection

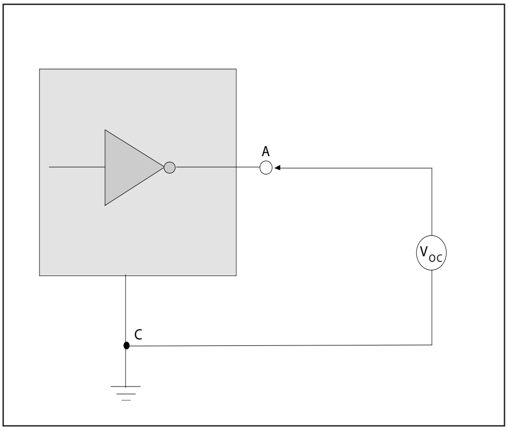


Figure 1. V.28 Driver Output Open Circuit Voltage

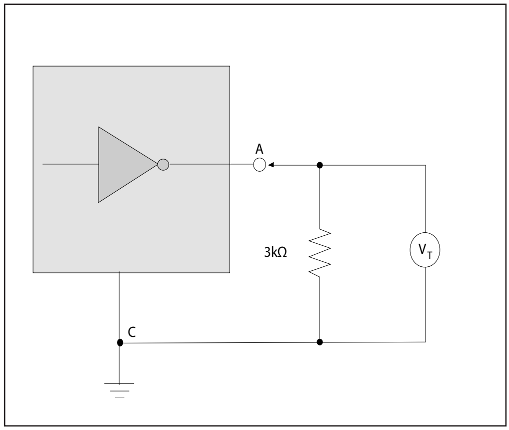


Figure 2. V.28 Driver Output Loaded Voltage

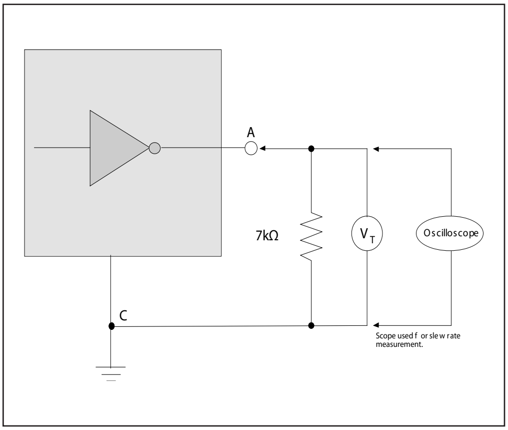


Figure 3. V.28 Driver Output Slew Rate

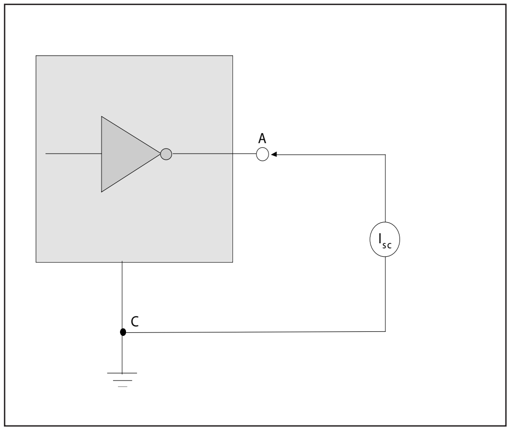


Figure 4. V.28 Driver Output Short-Circuit Current

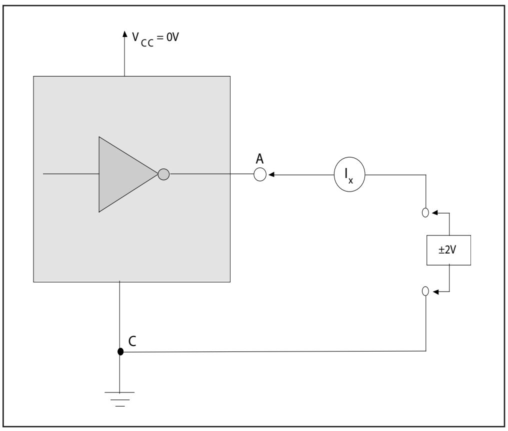


Figure 5. V.28 Driver Output Power-Off Impedance

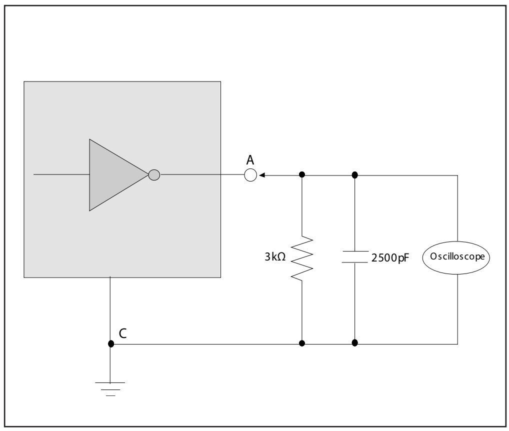


Figure 6. V.28 Driver Output Rise/Fall Times

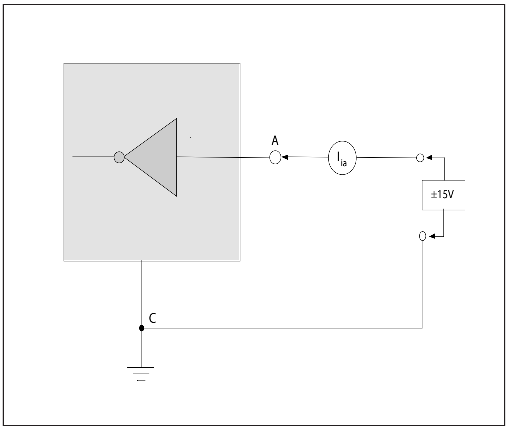


Figure 7. V.28 Receiver Input Impedance

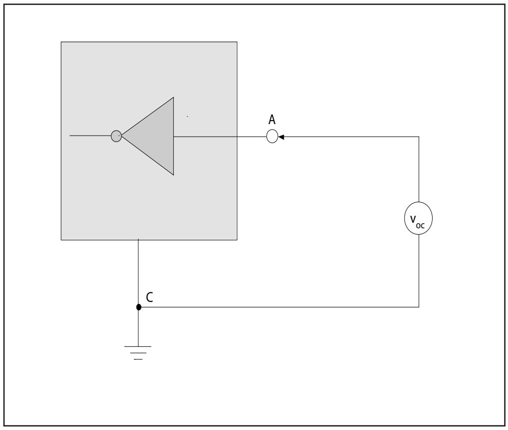


Figure 8. V.28 Receiver Input Open Circuit Bias

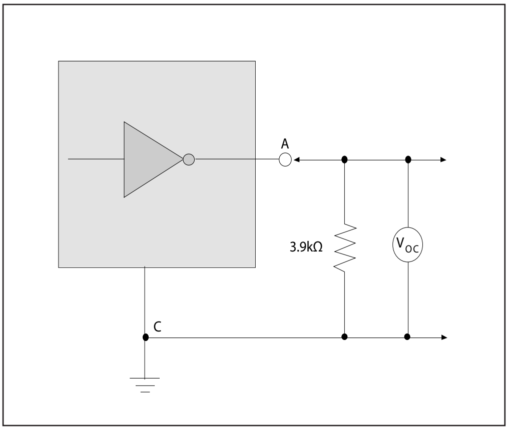


Figure 9. V.10 Driver Output Open-Circuit Voltage

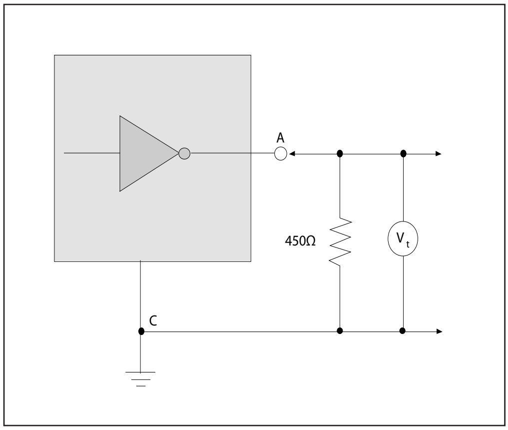


Figure 10. V.10 Driver Output Test Terminated Voltage

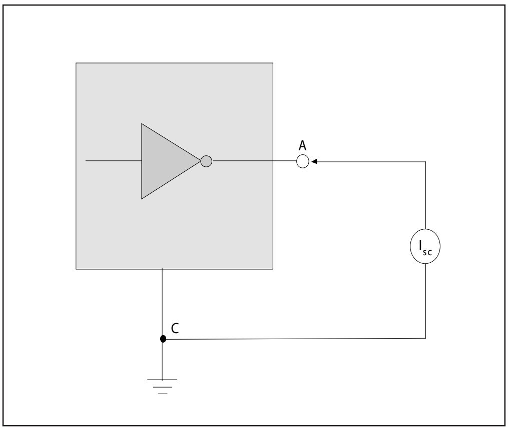


Figure 11. V.10 Driver Output Short-Circuit Current

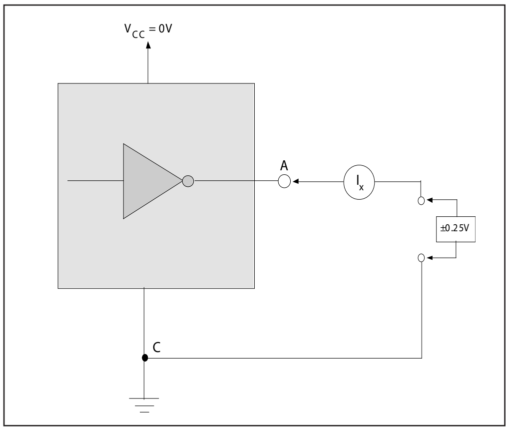


Figure 12. V.10 Driver Output Power-Off Current

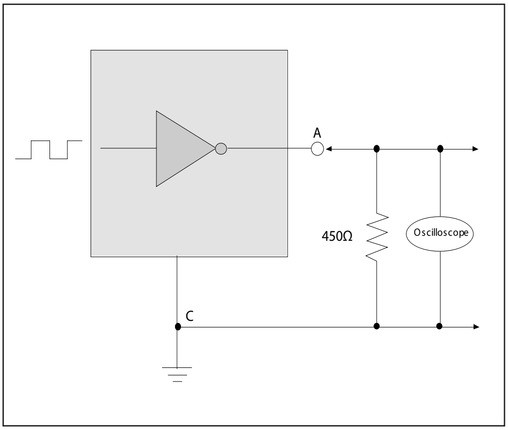


Figure 13. V.10 Driver Output Transition Time

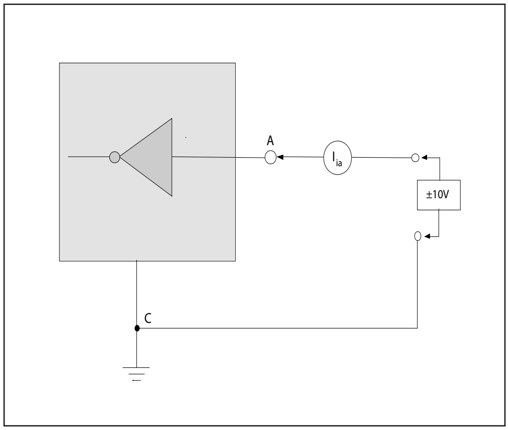


Figure 14. V.10 Receiver Input Current

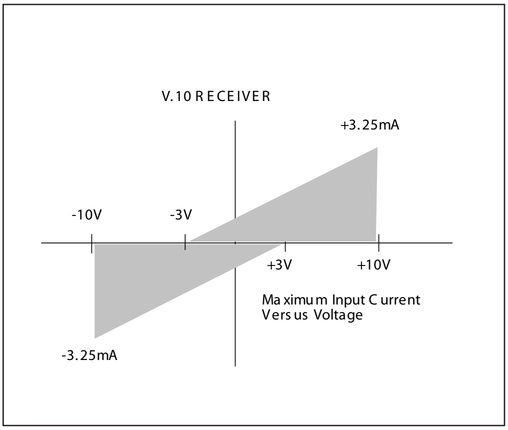


Figure 15. V.10 Receiver Input IV Graph

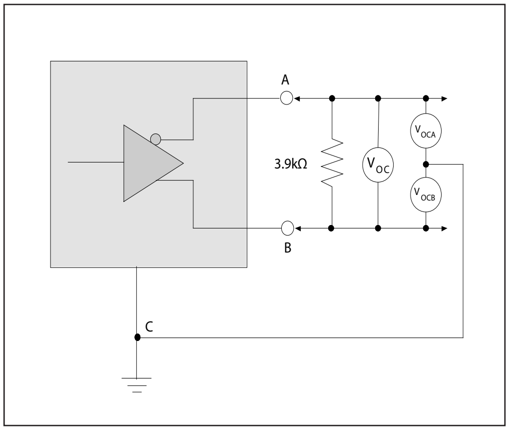


Figure 16. V.11 Driver Output Open-Circuit Voltage

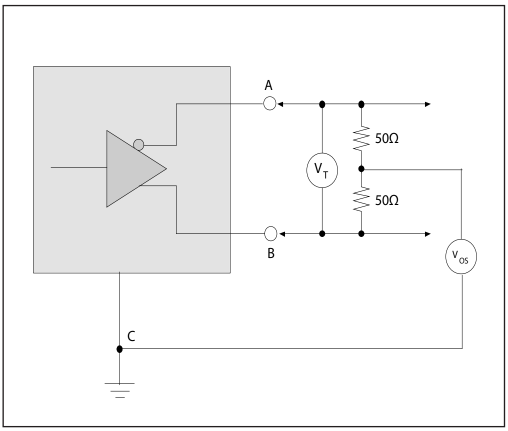


Figure 17. V.11 Driver Output Test Terminated Voltage

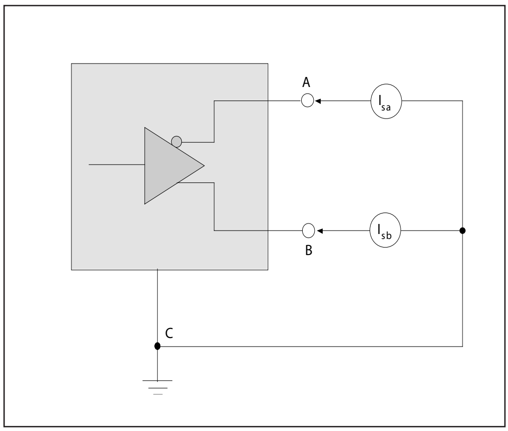


Figure 18. V.11 Driver Output Short-Circuit Current

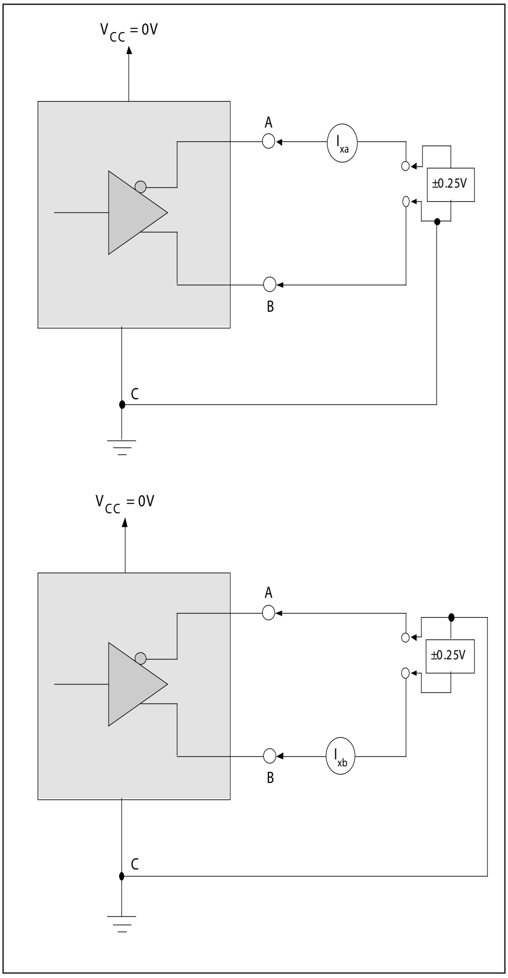


Figure 19. V.11 Driver Output Power-Off Current

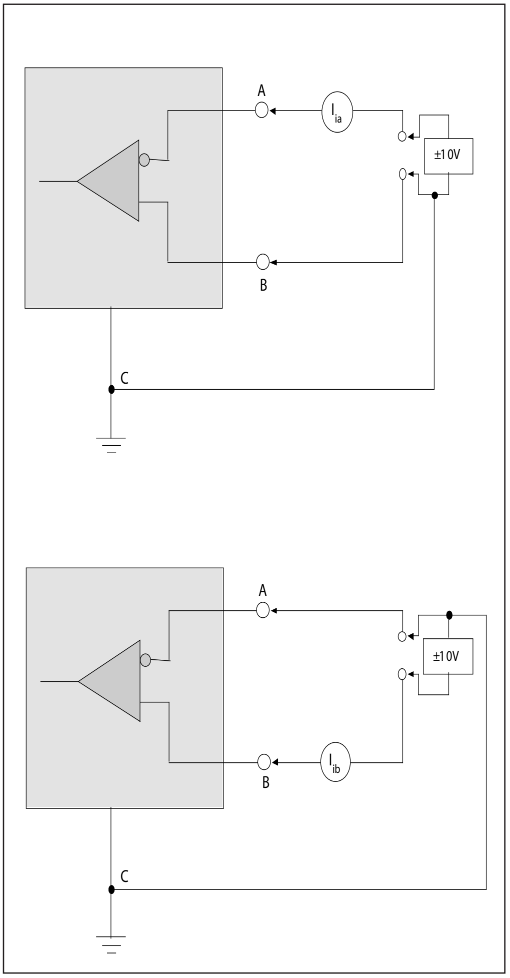


Figure 20. V.11 Receiver Input Current

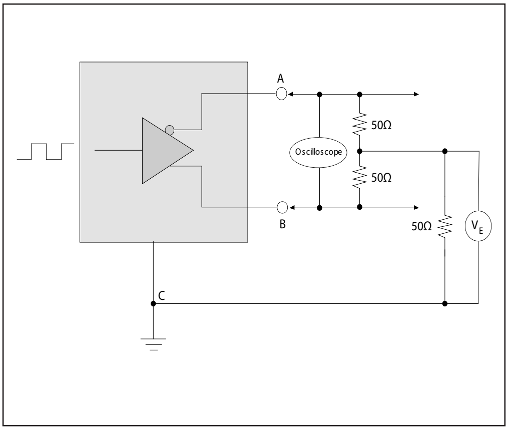


Figure 21. V.11 Driver Output Rise/Fall Time

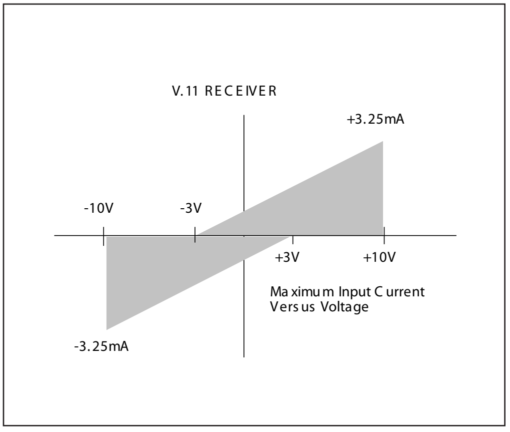


Figure 22. V.11 Receiver Input IV Graph

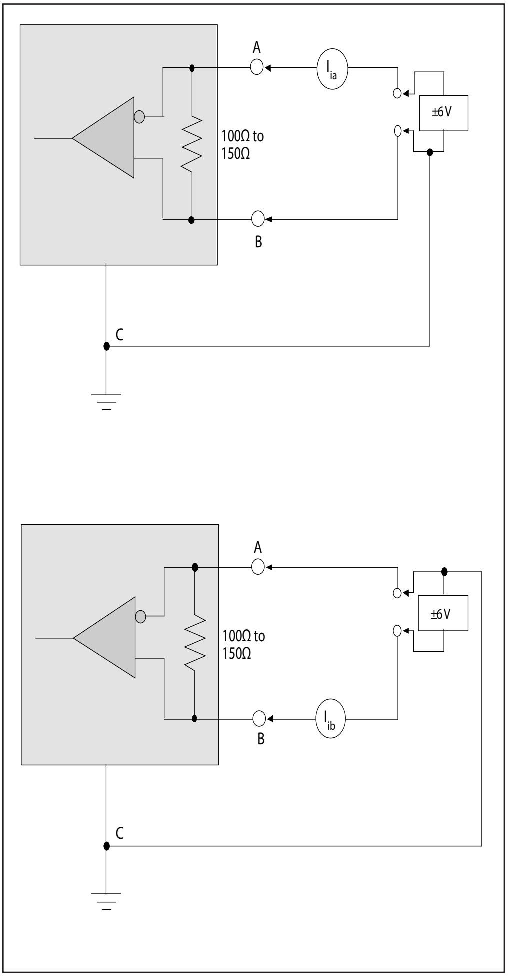


Figure 23. V.11 Receiver Input Current w/ Termination

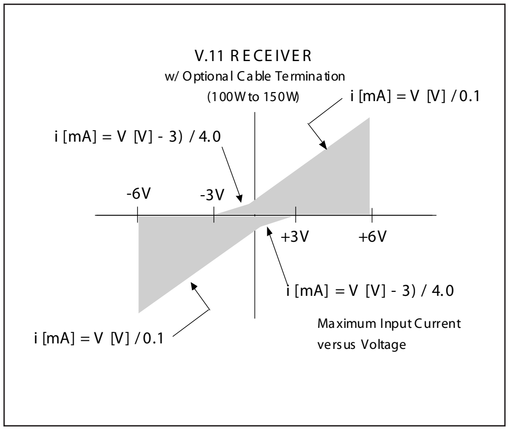


Figure 24. V.11 Receiver Input Graph with Termination

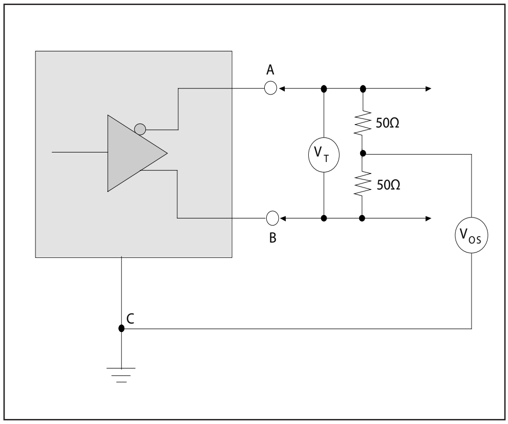


Figure 25. V.35 Driver Output Test Terminated Voltage

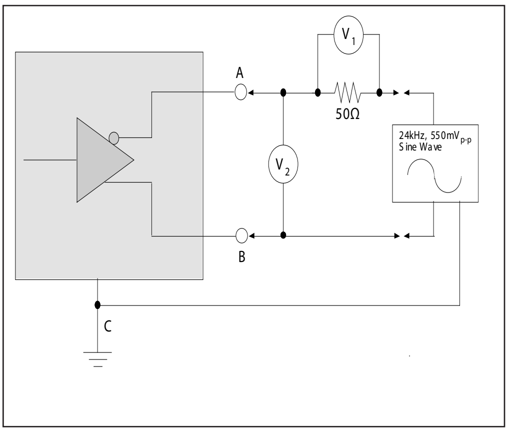


Figure 26. V.35 Driver Output Source Impedance

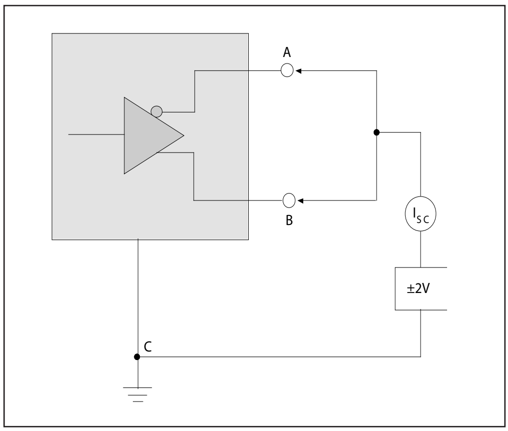


Figure 27. V.35 Driver Output Short-Circuit Impedance

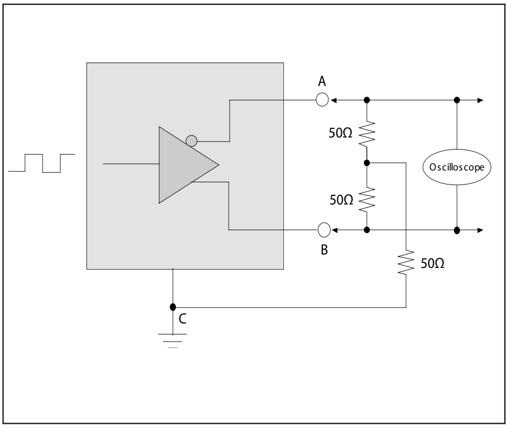


Figure 28. V.35 Driver Output Rise/Fall Time

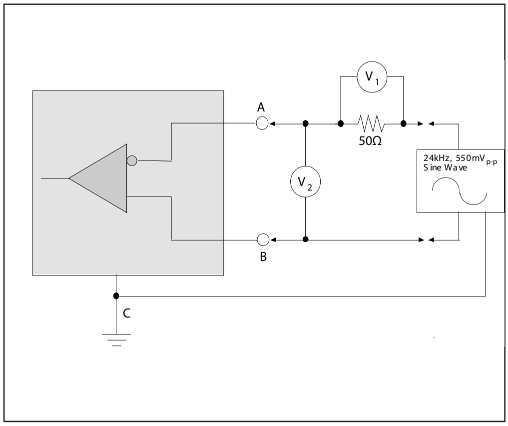


Figure 29. V.35 Receiver Input Source Impedance

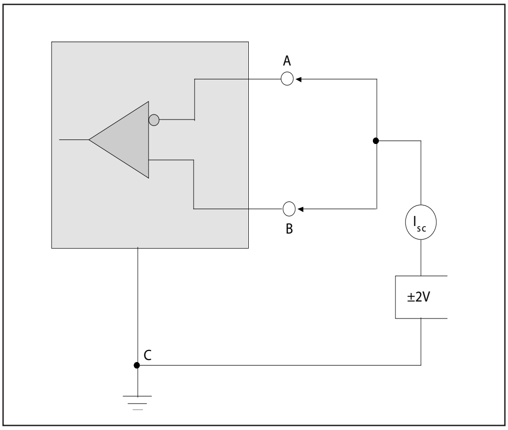


Figure 30. V.35 Receiver Input Short-Circuit Impedance

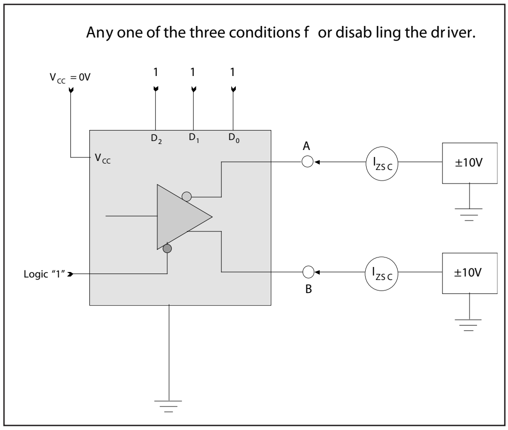


Figure 31. Driver Output Leakage Current Test

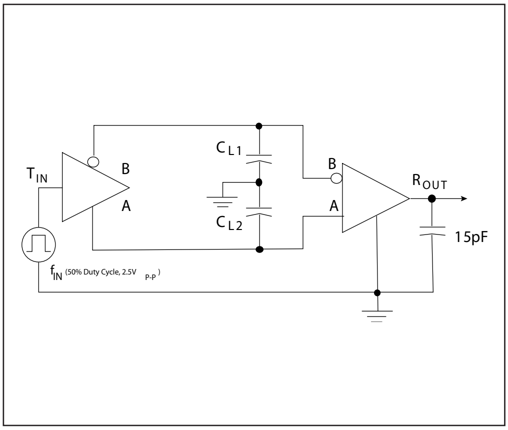


Figure 32. Driver/Receiver Timing Test Circuit

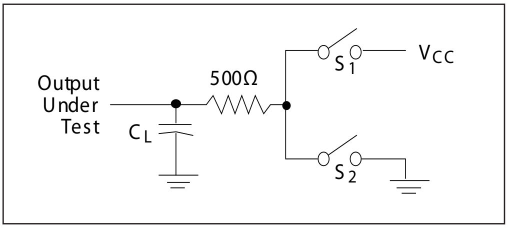


Figure 33. Driver Timing Test Load Circuit

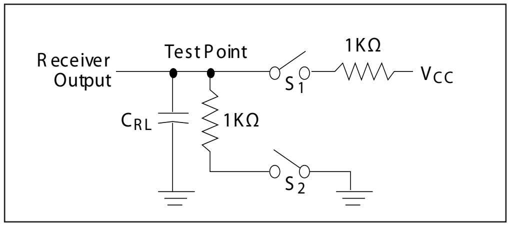


Figure 34. Receiver Timing Test Load Circuit

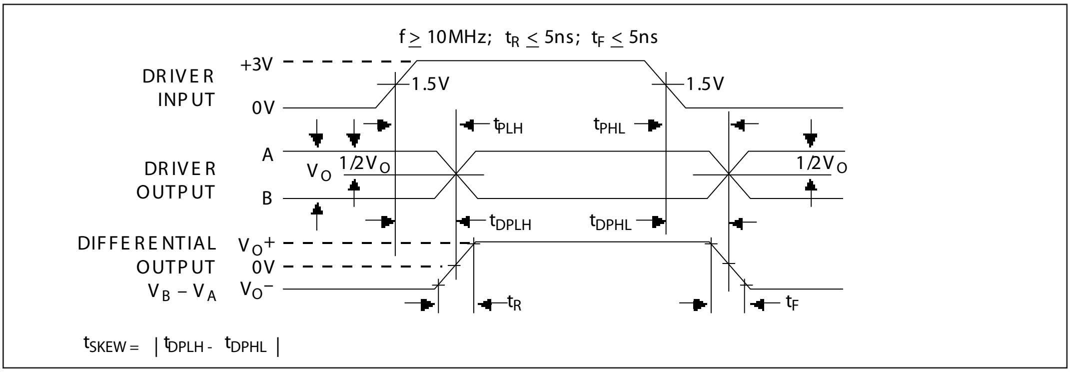


Figure 35. Driver Propagation Delays

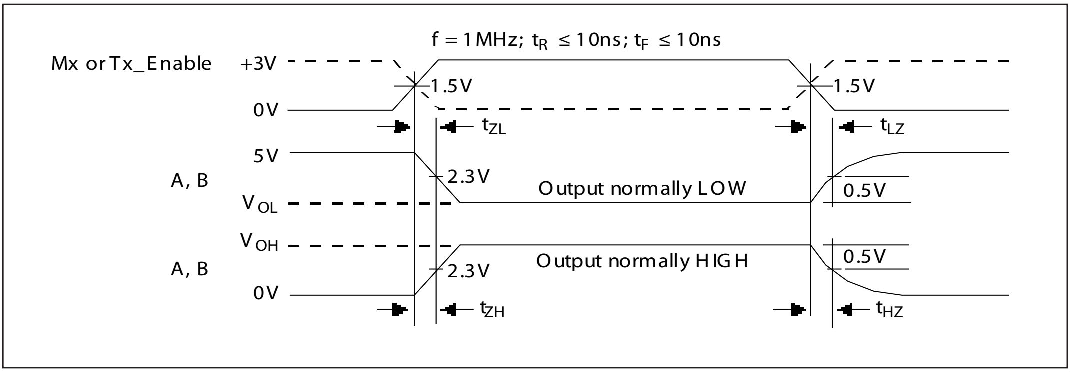


Figure 36. Driver Enable and Disable Times

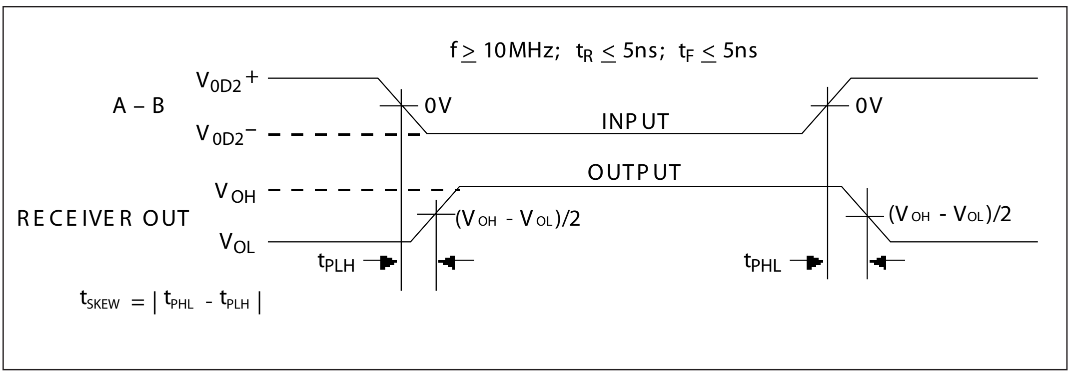


Figure 37. Receiver Propagation Delays

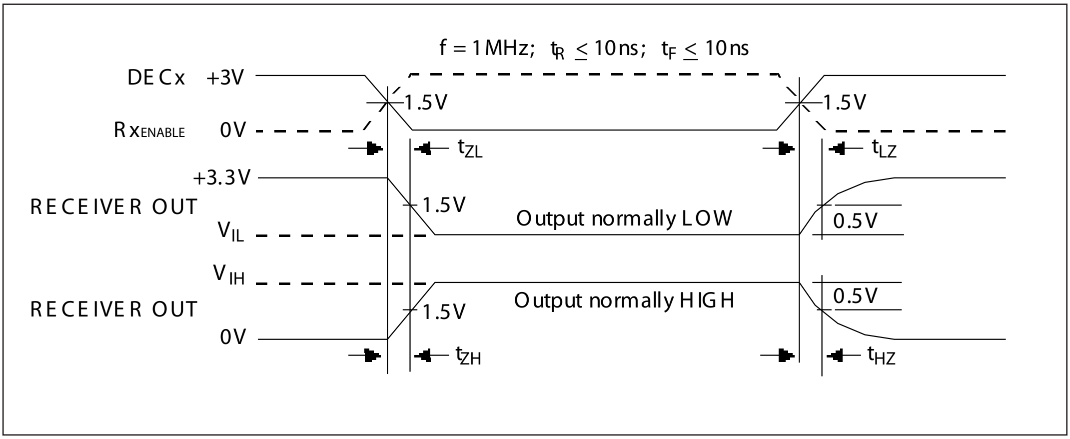


Figure 38. Receiver Enable and Disable Times

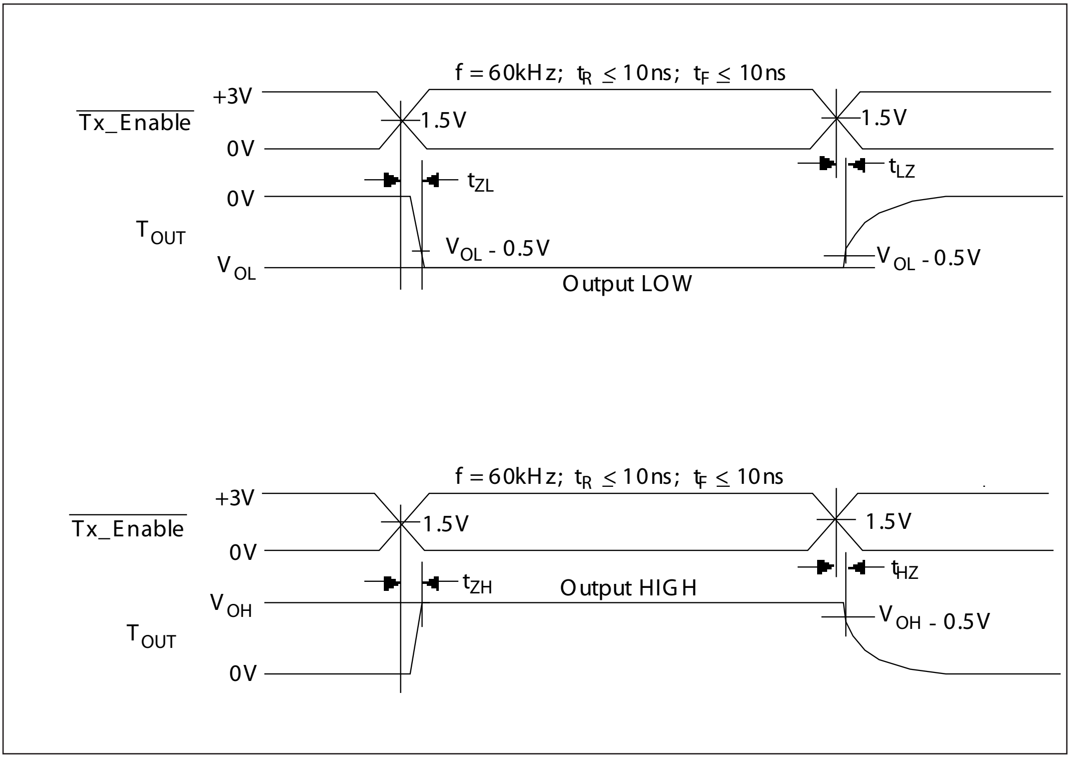


Figure 39. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

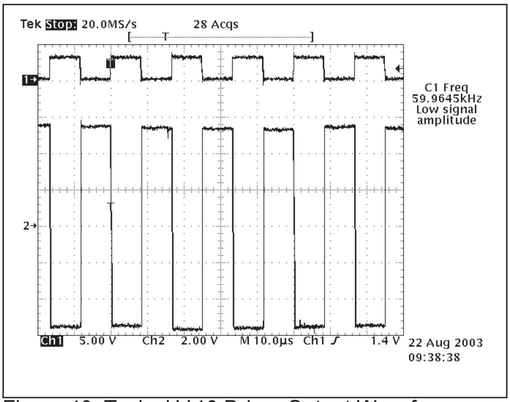


Figure 40. Typical V.10 Driver Output Waveform.

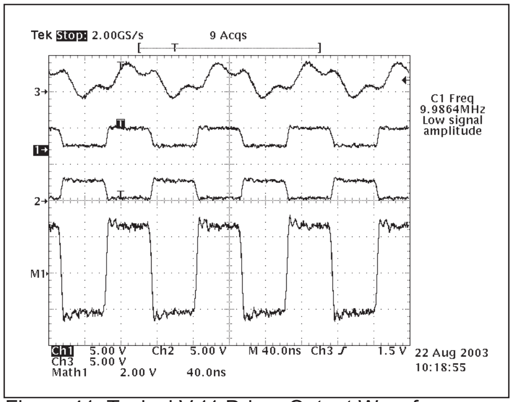


Figure 41. Typical V.11 Driver Output Waveform.

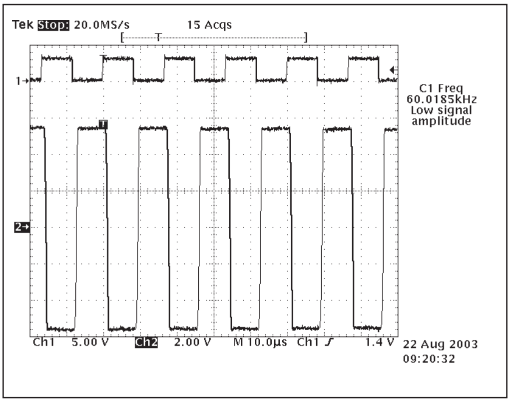


Figure 42. Typical V.28 Driver Output Waveform.

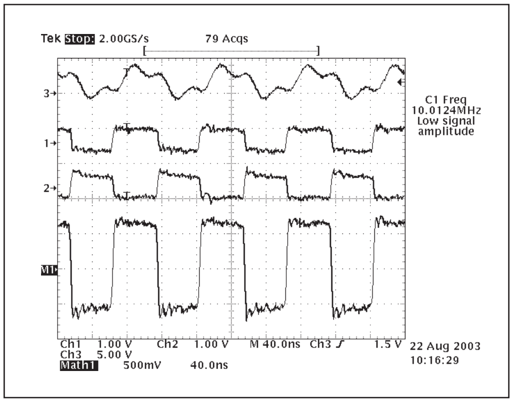


Figure 43. Typical V.35 Driver Output Waveform.

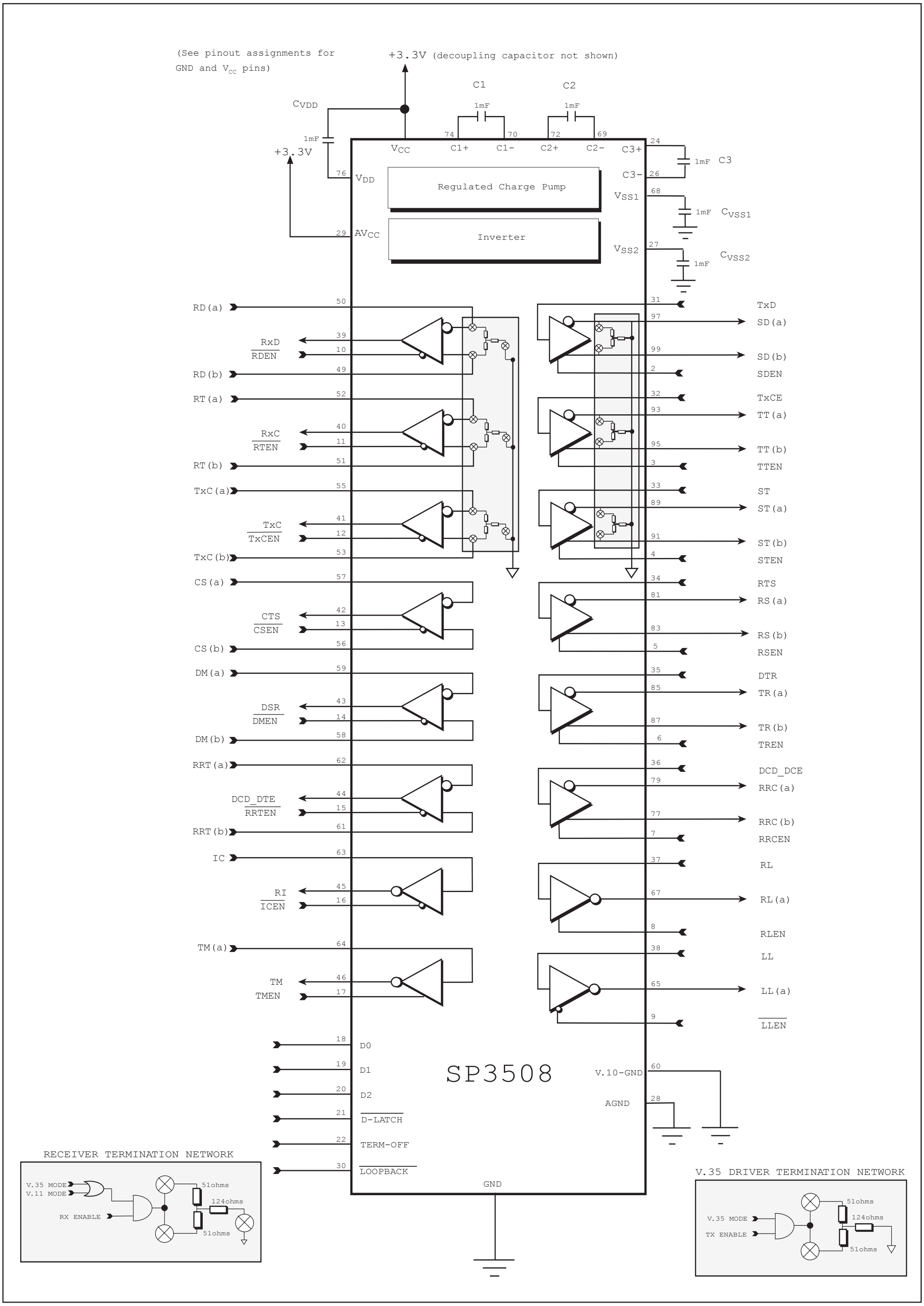


Figure 44. Functional Diagram

The SP3508 contains highly integrated serial transceivers that offer programmability between interface modes through software control. The SP3508 offers the hardware interface modes for RS-232 (V.28), RS-449/V.36 (V.11 and V.10), EIA-530 (V.11 and V.10), EIA-530A (V.11 and V.10), V.35 (V.35 and V.28) and X.21(V.11). The interface mode selection is done via three control pins, which can be latched via microprocessor control.

The SP3508 has eight drivers, eight receivers, and a patented on-board charge pump (5,306,954) that is ideally suited for wide area network connectivity and other multi-protocol applications. Other features include digital and line loopback modes, individual enable/disable control lines for each driver and receiver, fail-safe when inputs are either open or shorted.

THEORY OF OPERATION

The SP3508 device is made up of

1) the drivers
2) the receivers
3) charge pumps
4) DTE/DCE switching algorithm
5) control logic.

Drivers

The SP3508 has eight enhanced independent drivers. Control for the mode selection is done via a three-bit control word into D0, D1, and D2. The drivers are prearranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the required signal levels. The mode of each driver in the different interface modes that can be selected is shown in Table 1.

There are four basic types of driver circuits – ITU-T-V.28 (RS-232), ITU-T-V.10 (RS-423), ITU-T-V.11 (RS-422), and CCITT-V.35.

The V.28 (RS-232) drivers output single-ended signals with a minimum of $\pm$5V (with 3kΩ & 2500pF loading), and can operate over 120kbps. Since the SP3508 uses a charge pump to generate the RS-232 output rails, the driver outputs will never exceed $\pm$10V. The V.28 driver architecture is similar to Sipex's standard line of RS-232 transceivers.

The RS-423 (V.10) drivers are also single-ended signals which produce open circuit V_{OL} and V_{OH} measurements of $\pm$4.0V to $\pm$6.0V. When terminated with a 450Ω load to ground, the driver output will not deviate more than 10% of the open circuit value. This is in compliance of the ITU V.10 specification. The V.10 (RS-423) drivers are used in RS-449/V.36, EIA-530, and EIA-530A modes as Category II signals from each of their corresponding specifications. The V.10 driver can transmit over 120Kbps if necessary.

The third type of drivers are V.11 (RS-422) differential drivers. Due to the nature of differential signaling, the drivers are more immune to noise as opposed to single-ended transmission methods. The advantage is evident over high speeds and long transmission lines. The strength of the driver outputs can produce differential signals that can maintain $\pm$2V differential output levels with a load of 100Ω. The strength allows the SP3508 differential driver to drive over long cable lengths with minimal signal degradation. The V.11 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category I signals which are used for clock and data. Exar's new driver design over its predecessors allow the SP3508 to operate over 20Mbps for differential transmission.

The fourth type of drivers are V.35 differential drivers. There are only three available on the SP3508 for data and clock (TxD, TxCE, and TxC in DCE mode).

These drivers are current sources that drive loop current through a differential pair resulting in a 550mV differential voltage at the receiver. These drivers also incorporate fixed termination networks for each driver in order to set the V_{OH} and V_{OL} depending on load conditions. This termination network is basically a “Y” configuration consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors to GND. Filtering can be done on these pins to reduce common mode noise transmitted over the transmission line by connecting a capacitor to ground.

The drivers also have separate enable pins which simplifies half-duplex configurations for some applications, especially programmable DTE/DCE. The enable pins will either enable or disable the output of the drivers according to the appropriate active logic illustrated on Figure 44. The enable pins have internal pull-up and pull-down devices, depending on the active polarity of the receiver, that enable the driver upon power-on if the enable lines are left floating. During disabled conditions, the driver outputs will be at a high impedance 3-state.

The driver inputs are both TTL or CMOS compatible. All driver inputs have an internal pull-up resistor so that the output will be at a defined state at logic LOW (“0”). Unused driver inputs can be left floating. The internal pull-up resistor value is approximately 500kΩ.

Receivers

The SP3508 has eight enhanced independent receivers. Control for the mode selection is done via a three-bit control word that is the same as the driver control word. Therefore, the modes for the drivers and receivers are identical in the application. Like the drivers, the receivers are prearranged for the specific requirements of the synchronous serial interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the required serial interface protocols of the receivers. Table 1 shows the mode of each receiver in the different interface modes that can be selected. There are two basic types of receiver circuits—ITU-T-V .28 (RS-232) and ITU-T-V.11, (RS-422).

The RS-232 (V.28) receiver is single-ended and accepts RS-232 signals from the RS-232 driver. The RS-232 receiver has an operating input voltage range of $\pm$15V and can receive signals downs to $\pm$3V. The input sensitivity complies with RS-232 and V.28 at $\pm$3V. The input impedance is 3kΩ to 7kΩ in accordance to RS-232 and V.28. The receiver output produces a TTL/CMOS signal with a +2.4V minimum for a logic “1” and a +0.4V maximum for a logic “0”. The RS-232 (V.28) protocol uses these receivers for all data, clock and control signals. They are also used in V.35 mode for control line signals: CTS, DSR, LL, and RL. The RS-232 receivers can operate over 120kbps.

The second type of receiver is a differential type that can be configured internally to support ITU-T-V.10 and CCITT-V.35 depending on its input conditions. This receiver has a typical input impedance of 10kΩ and a differential threshold of less than $\pm$200mV, which complies with the ITU-T-V.11 (RS-422) specifications. V.11 receivers are used in RS-449/V.36, EIA-530, EIA-530A and X.21 as Category I signals for receiving clock, data, and some control line signals not covered by Category II V.10 circuits. The differential V.11 transceiver has improved architecture that allows over 20Mbps transmission rates.

Receivers dedicated for data and clock (RxD, RxC, TxC) incorporate internal termination for V.11. The termination resistor is typically 120Ω connected between the A and B inputs. The termination is essential for minimizing crosstalk and signal reflection over the transmission line . The minimum value is guaranteed to exceed 100Ω, thus complying with the V.11 and RS-422 specifications. This resistor is invoked when the receiver is operating as a V.11 receiver, in modes EIA-530, EIA-530A, RS-449/V.36, and X.21.

The same receivers also incorporate a termination network internally for V.35 applications. For V.35, the receiver input termination is a "Y" termination consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors and GND. The receiver itself is identical to the V.11 receiver.

The differential receivers can be configured to be ITU-T-V.10 single-ended receivers by internally connecting the non-inverting input to ground. This is internally done by default from the decoder. The non-inverting input is rerouted to V10GND and can be grounded separately. The ITU-T-V.10 receivers can operate over 120Kbps and are used in RS-449/V.36, E1A-530, E1A-530A and X.21 modes as Category II signals as indicated by their corresponding specifications. All receivers include an enable/disable line for disabling the receiver output allowing convenient half-duplex configurations. The enable pins will either enable or disable the output of the receivers according to the appropriate active logic illustrated on Figure 44. The receiver's enable lines include an internal pull-up or pull-down device, depending on the active polarity of the receiver, that enables the receiver upon power up if the enable lines are left floating. During disabled conditions, the receiver outputs will be at a high impedance state. If the receiver is disabled any associated termination is also disconnected from the inputs.

All receivers include a fail-safe feature that outputs a logic high when the receiver inputs are open, terminated but open, or shorted together. For single-ended V.28 and V.10 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high ("1") at the receiver outputs. The differential receivers have a proprietary circuit that detect open or shorted inputs and if so, will produce a logic HIGH ("1") at the receiver output.

CHARGE PUMP

SP3508 uses an internal capacitive charge pump to generate Vdd and Vss. The design is a patented (5,306,954) four-phased voltage shifting charge pump converters that converts the input voltage of 3.3V to nominal output voltages of +/-6V (Vdd & Vss1). SP3508 also includes an inverter block that inverts Vcc to -Vcc (Vss2). There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

4-phased doubler pump

Phase 1

-V_{SS1} charge storage -During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to V_{CC}. C1+ is then switched to ground and the charge in C1- is transferred to C2-. Since C2+ is connected to V_{CC}, the voltage potential across capacitor C2 is now 2xV_{CC}.

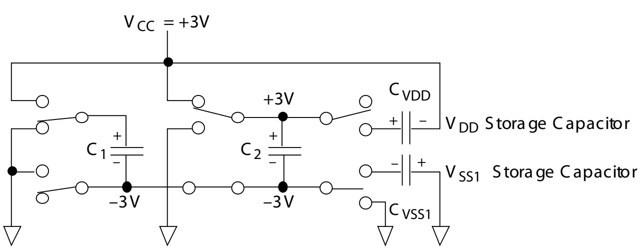


Figure 45. Charge Pump - Phase 1.

Phase 2

-V_{SS1} transfer -Phase two of the clock connects the negative terminal of C2 to the V_{SS1} storage capacitor and the positive terminal of C2 to ground, and transfers the negative generated voltage to C_{VSS1}. This generated voltage is regulated to -5.5V. Simultaneously, the positive side of the capacitor C1 is switched to V_{CC} and the negative side is connected to ground.

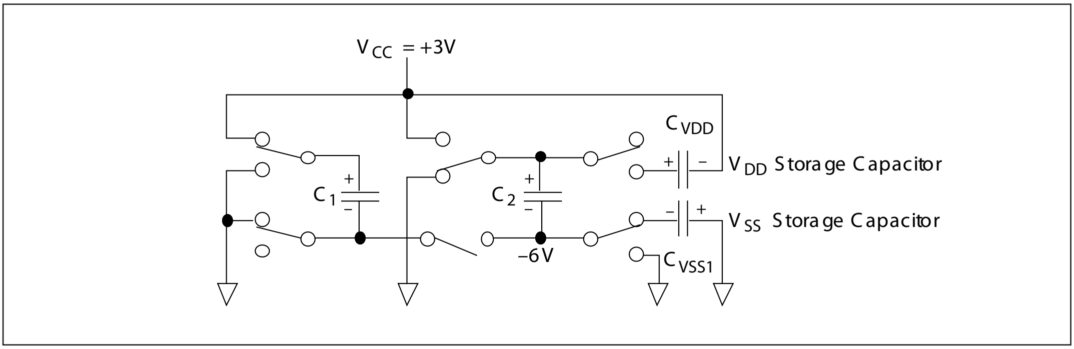


Figure 46. Charge Pump - Phase 2.

Phase 3

-V_{DD} charge storage -The third phase of the clock is identical to the first phase-the charge transferred in C1 produces -V_{CC} in the negative terminal of C1 which is applied to the negative side of the capacitor C2. Since C2+ is at V_{CC}, the voltage potential across C2 is 2xV_{CC}.

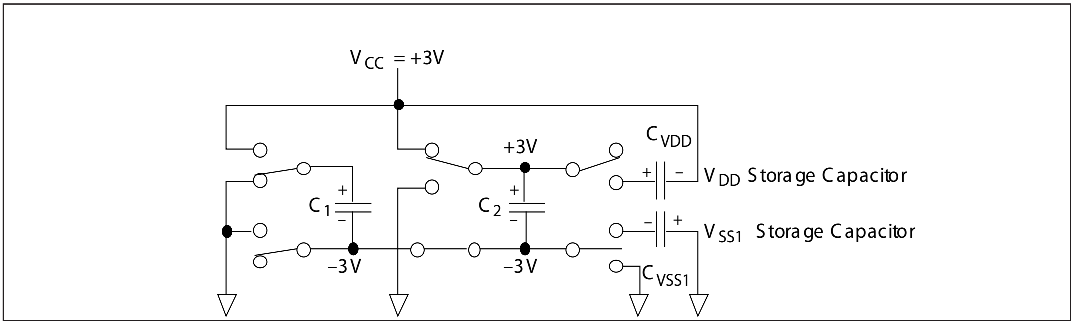


Figure 47.Charge Pump - Phase 3.

Phase 4

-V_{DD} transfer -The fourth phase of the clock connects the negative terminal of C2 to ground, and transfers the generated 5.5V across C2 to C_{VDD}, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At the regulated voltage, the internal oscillator is disabled and simultaneously with this, the positive side of capacitor C1 is switched to V_{CC} and the negative side is connected to ground, and the cycle begins again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present. Since both V+ and V- are separately generated from V_{CC}; in a no-load condition V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design. The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 1µF with a 16V breakdown voltage rating.

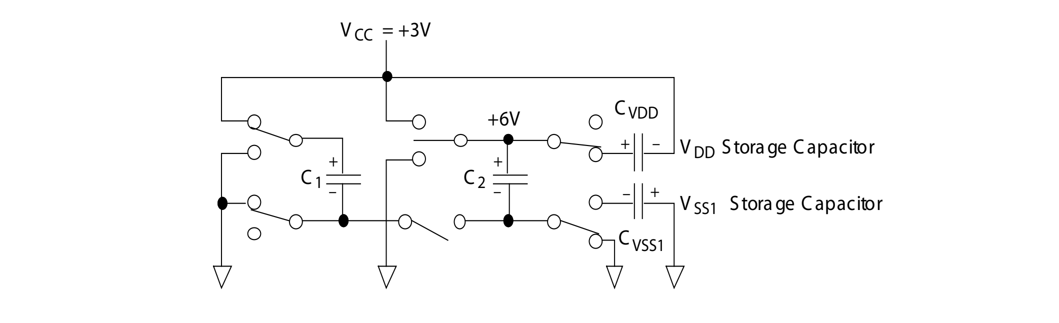


Figure 48. Charge Pump - Phase 4.

2-phased inverter pump

Phase 1

Please refer to figure below: In the first phase of the clock cycle, switches S2 and S4 are opened and S1 and S3 closed. This connects the flying capacitor, C3, from Vin to ground. C3 charge up to the input voltage applied at Vcc.

Phase 2

In the second phase of the clock cycle, switches S2 and S4 are closed and S1 and S3 are opened. This connects the flying capacitor, C3, in parallel with the output capacitor, C_{VSS2}. The Charge stored in C3 is now transferred to C_{VSS2}. Simultaneously, the negative side of C_{VSS2} is connected to V_{SS2} and the positive side is connected to ground. With the voltage across C_{VSS2} smaller than the voltage across C3, the charge flows from C3 to C_{VSS2} until the voltage at the V_{SS2} equals $-V_{CC}$.

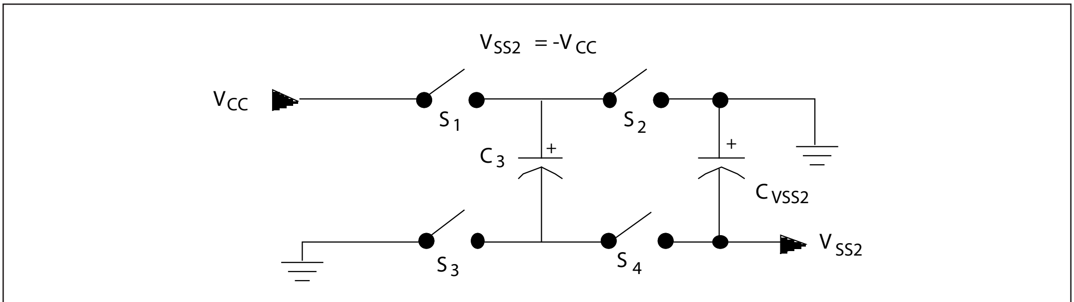


Figure 49. Circuit for an Ideal Voltage Inverter.

SP3508 Multiprotocol Configured as DCE — Recommended Signals and Port Pin Assignments

Interface to System Logic: Pin Number	Pin Mnemonic	Circuit	Interface to Port-Connector: Pin Mnemonic	Pin Number	RS-232 or V.24: Signal Type	Mnemonic	DB-25 Pin(F)	EIA-530: Signal Type	Mnemonic	DB-25 Pin(F)	RS-449: Signal Type	Mnemonic	DB-37 Pin(F)	V.35: Signal Type	Mnemonic	M34 Pin(F)	X.21: Signal Type	Mnemonic	DB-15 Pin(F)
31	TxD	Driver_1	SD(A)	97	V.28	BB	3	V.11	BB(A)	3	V.11	RD(A)	6	V.35	104	R	V.11	R(A)	4
2	SDEN		SD(B)	99				V.11	BB(B)	16	V.11	RD(B)	24	V.35	104	T	V.11	R(B)	11
32	TxCE	Driver_2	TT(A)	93	V.28	DD	17	V.11	DD(A)	17	V.11	RT(A)	8	V.35	115	V	V.11	B(A)	7**
3	TTEN		TT(B)	95				V.11	DD(B)	9	V.11	RT(B)	26	V.35	115	X	V.11	B(B)	14**
33	ST	Driver_3	ST(A)	89	V.28	DB	15	V.11	DB(A)	15	V.11	ST(A)	5	V.35	114	Y	V.11	S(A)	6
4	STEN		ST(B)	91				V.11	DB(B)	12	V.11	ST(B)	23	V.35	114	AA	V.11	S(B)	13
34	RTS	Driver_4	RS(A)	81	V.28	CB	5	V.11	CB(A)	5	V.11	CS(A)	9	V.28	106	D	V.11	I(A)	5
5	RSEN		RS(B)	83				V.11	CB(B)	13	V.11	CS(B)	27				V.11	I(B)	12
35	DTR	Driver_5	TR(A)	85	V.28	CC	6	V.11	CC(A)	6	V.11	DM(A)	11	V.28	107	E			
6	TREN		TR(B)	87				V.11	CC(B)	22	V.11	DM(B)	29						
36	DCD_DCE	Driver_6	RRC(A)	79	V.28	CF	8	V.11	CF(A)	8	V.11	RR(A)	13	V.28	109	F			
7	RRCEN		RRC(B)	77				V.11	CF(B)	10	V.11	RR(B)	31						
37	RL	Driver_7	RL(A)	67	V.28	CE	22							V.28	125	J			
8	RLEN																		
38	LL	Driver_8	LL(A)	65	V.28	TM	25	V.10	TM	25	V.10	TM	18	V.28	142	NN			
9	LLEN#																		
39	RxD	Receiver_1	RD(A)	50	V.28	BA	2	V.11	BA(A)	2	V.11	SD(A)	4	V.35	103	P	V.11	T(A)	2
10	RDEN#		RD(B)	49				V.11	BA(B)	12	V.11	SD(B)	22	V.35	103	S	V.11	T(B)	9
40	RxC	Receiver_2	RT(A)	52	V.28	DA	24	V.11	DA(A)	24	V.11	TT(A)	17	V.35	113	U	V.11	X(A)	7**
11	RTEN#		RT(B)	51				V.11	DA(B)	11	V.11	TT(B)	35	V.35	113	W	V.11	X(B)	14**
41	TxC	Receiver_3	TxC(A)	55															
12	TxCEN#		TxC(B)	53															
42	CTS	Receiver_4	CS(A)	57	V.28	CA	4	V.11	CA(A)	4	V.11	RS(A)	7	V.28	105	C	V.11	C(A)	3
13	CSEN#		CS(B)	56				V.11	CA(B)	19	V.11	RS(B)	25				V.11	C(B)	10
43	DSR	Receiver_5	DM(A)	59	V.28	CD	20	V.11	CD(A)	20	V.11	TR(A)	12	V.28	108	H			
14	DMEN#		DM(B)	58				V.11	CD(B)	23	V.11	TR(B)	30						
44	DCD_DTE	Receiver_6	RRT(A)	62															
15	RRTEN#		RRT(B)	61															
45	RI	Receiver_7	IC	63	V.28	RL	21	V.10	RL	21	V.10	RL	14	V.28	140	N			
16	ICEN#																		
46	TM	Receiver_8	TM(A)	64	V.28	LL	18	V.10	LL	18	V.10	LL	10	V.28	141	L			
17	TMEN																		

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

** X.21 use either B() or X(), not both

DTE CONFIGURATION

SP3508 Multiprotocol Configured as DTE — Recommended Signals and Port Pin Assignments

Interface to System Logic			Interface to Port-Connector		RS-232 or V.24			EIA-530			RS-449			V.35			X.21		
Pin Number	Pin Mnemonic	Circuit	Pin Mnemonic	Pin Number	Signal Type	Mnemonic	DB-25 Pin(M)	Signal Type	Mnemonic	DB-25 Pin(M)	Signal Type	Mnemonic	DB-37 Pin(M)	Signal Type	Mnemonic	M34 Pin(M)	Signal Type	Mnemonic	DB-15 Pin(M)
31	TxD	Driver_1	SD(A)	97	V.28	BA	2	V.11	BA(A)	2	V.11	SD(A)	4	V.35	103	P	V.11	T(A)	2
2	SDEN		SD(B)	99				V.11	BA(B)	12	V.11	SD(B)	22	V.35	103	S	V.11	T(B)	9
32	TxCE	Driver_2	TT(A)	93	V.28	DA	24	V.11	DA(A)	24	V.11	TT(A)	17	V.35	113	U	V.11	X(A)	7**
3	TTEN		TT(B)	95				V.11	DA(B)	11	V.11	TT(B)	35	V.35	113	W	V.11	X(B)	14**
33	ST	Driver_3	ST(A)	89															
4	STEN		ST(B)	91															
34	RTS	Driver_4	RS(A)	81	V.28	CA	4	V.11	CA(A)	4	V.11	RS(A)	7	V.28	105	C	V.11	C(A)	3
5	RSEN		RS(B)	83				V.11	CA(B)	19	V.11	RS(B)	25				V.11	C(B)	10
35	DTR	Driver_5	TR(A)	85	V.28	CD	20	V.11	CD(A)	20	V.11	TR(A)	12	V.28	108	H			
6	TREN		TR(B)	87				V.11	CD(B)	23	V.11	TR(B)	30						
36	DCD_DCE	Driver_6	RRC(A)	79															
7	RRCEN		RRC(B)	77															
37	RL	Driver_7	RL(A)	67	V.28	RL	21	V.10	RL	21	V.10	RL	14	V.28	140	N			
8	RLEN																		
38	LL	Driver_8	LL(A)	65	V.28	LL	18	V.10	LL	18	V.10	LL	10	V.28	141	L			
9	LLEN#																		
39	RxD	Receiver_1	RD(A)	50	V.28	BB	3	V.11	BB(A)	3	V.11	RD(A)	6	V.35	104	R	V.11	R(A)	4
10	RDEN#		RD(B)	49				V.11	BB(B)	16	V.11	RD(B)	24	V.35	104	T	V.11	R(B)	11
40	RxC	Receiver_2	RT(A)	52	V.28	DD	17	V.11	DD(A)	17	V.11	RT(A)	8	V.35	115	V	V.11	B(A)	7**
11	RTEN#		RT(B)	51				V.11	DD(B)	9	V.11	RT(B)	26	V.35	115	X	V.11	B(B)	14**
41	TxC	Receiver_3	TxC(A)	55	V.28	DB	15	V.11	DB(A)	15	V.11	ST(A)	5	V.35	114	Y	V.11	S(A)	6
12	TxCEN#		TxC(B)	53				V.11	DB(B)	12	V.11	ST(B)	23	V.35	114	AA	V.11	S(B)	13
42	CTS	Receiver_4	CS(A)	57	V.28	CB	5	V.11	CB(A)	5	V.11	CS(A)	9	V.28	106	D	V.11	I(A)	5
13	CSEN#		CS(B)	56				V.11	CB(B)	13	V.11	CS(B)	27				V.11	I(B)	12
43	DSR	Receiver_5	DM(A)	59	V.28	CC	6	V.11	CC(A)	6	V.11	DM(A)	11	V.28	107	E			
14	DMEN#		DM(B)	58				V.11	CC(B)	22	V.11	DM(B)	29						
44	DCD_DTE	Receiver_6	RRT(A)	62	V.28	CF	8	V.11	CF(A)	8	V.11	RR(A)	13	V.28	109	F			
15	RRTEN#		RRT(B)	61				V.11	CF(B)	10	V.11	RR(B)	31						
45	RI	Receiver_7	IC	63	V.28	CE	22							V.28	125	J			
16	ICEN#																		
46	TM	Receiver_8	TM(A)	64	V.28	TM	25	V.10	TM	25	V.10	TM	18	V.28	142	NN			
17	TMEN																		

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

** X.21 use either B() or X(), not both

TERM_OFF FUNCTION

The SP3508 contains a TERM_OFF pin that disables all three receiver input termination networks regardless of mode. This allows the device to be used in monitor mode applications typically found in networking test equipment.

The TERM_OFF pin internally contains a pull-down device with an impedance of over 500kΩ, which will default in a "ON" condition during power-up if V.35 receivers enable line and the SHUTDOWN mode from the decoder will disable the termination regardless of TERM_OFF.

LOOPBACK FUNCTION

The SP3508 contains a LOOPBACK pin that invokes a loopback path. This loopback path is illustrated in Figure 50. LOOPBACK has an internal pull-up resistor that defaults to normal mode during power up or if the pin is left floating. During loopback, the driver output and receiver input characteristics will still adhere to its appropriate specifications.

DECODER AND D_LATCH FUNCTION

The SP3508 contains a D_LATCH pin that latches the data into the D0, D1 and D2 decoder inputs. If tied to a logic LOW ("0"), the latch is transparent, allowing the data at the decoder inputs to propagate through and program the SP3508 accordingly. If tied to a logic HIGH ("1"), the latch locks out the data and prevents the mode from changing until this pin is brought to a logic LOW.

There are internal pull-up devices on D0, D1 and D2, which allow the device to be in SHUTDOWN mode ("111") upon power up. However, if the device is powered-up with the D_LATCH at a logic HIGH, the decoder state of the SP3508 will be undefined.

CTR1/CTR2 EUROPEAN COMPLIANCY

As with all of Exar's previous multi-protocol serial transceiver IC's the drivers and receivers have been designed to meet all the requirements to NET1/NET2 and TBR2 in order to meet CTR1/CTR2 compliancy. The SP3508 is also tested in-house at Exar and adheres to all the NET1/2 physical layer testing and the ITU Series V specifications before shipment. Please note that although the SP3508, as with its predecessors, adhere to CRT1/CTR2 compliancy testing, any complex or usual configuration should be double-checked to ensure CTR1/CTR2 compliance. Consult the factory for details.

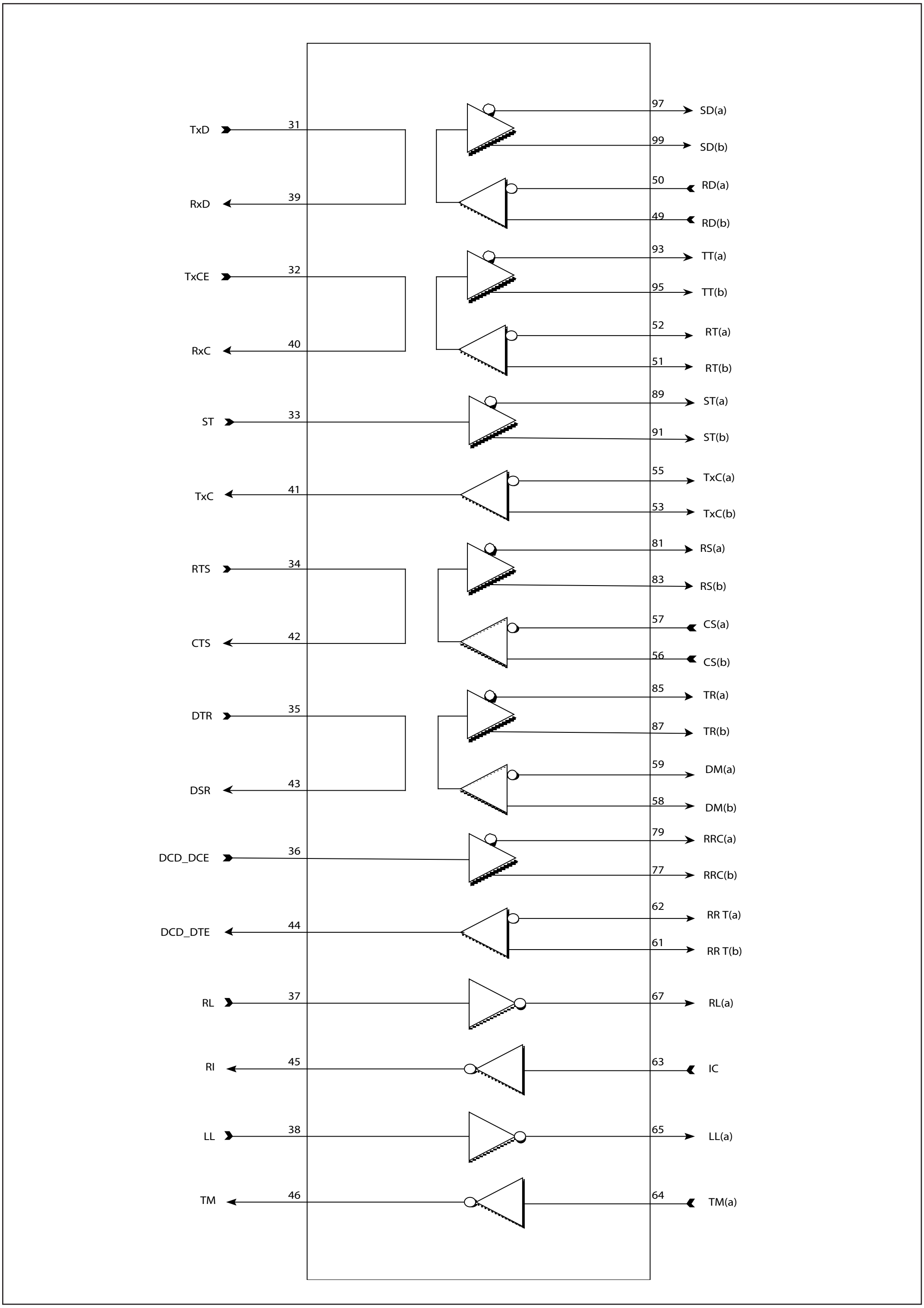


Figure 50. Loopback Path

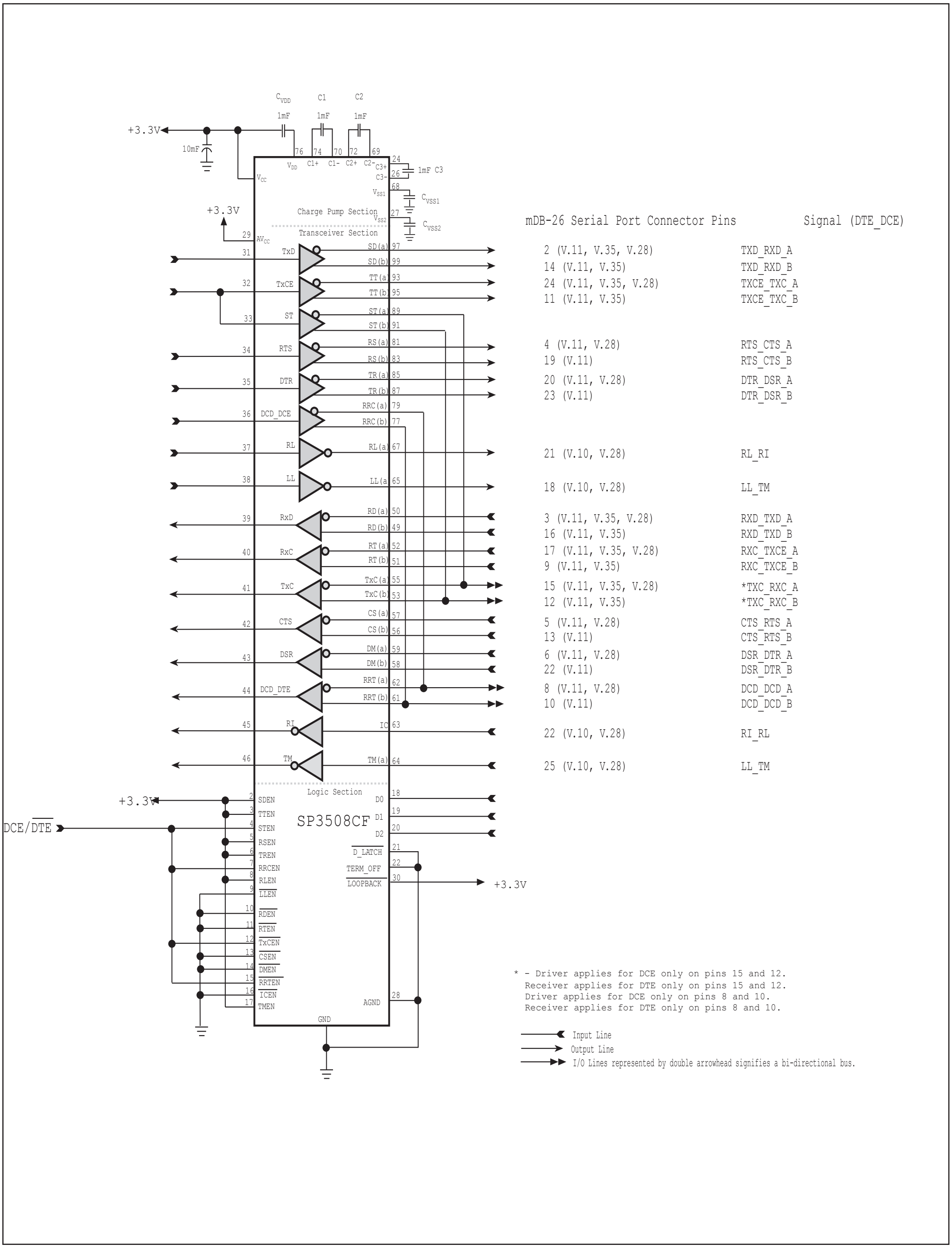
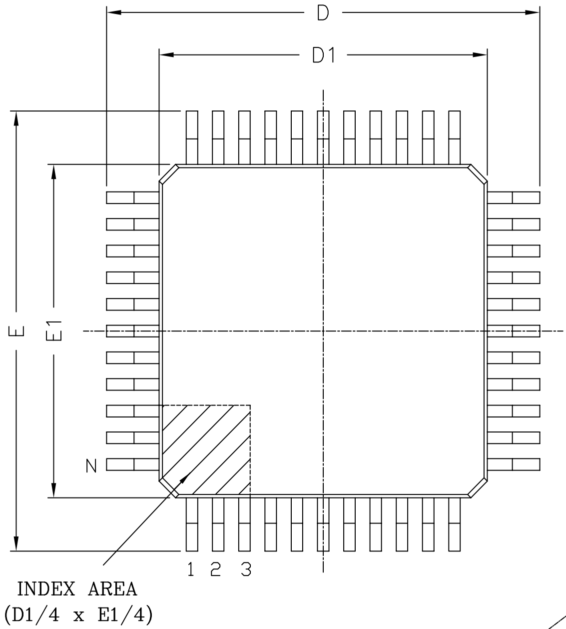
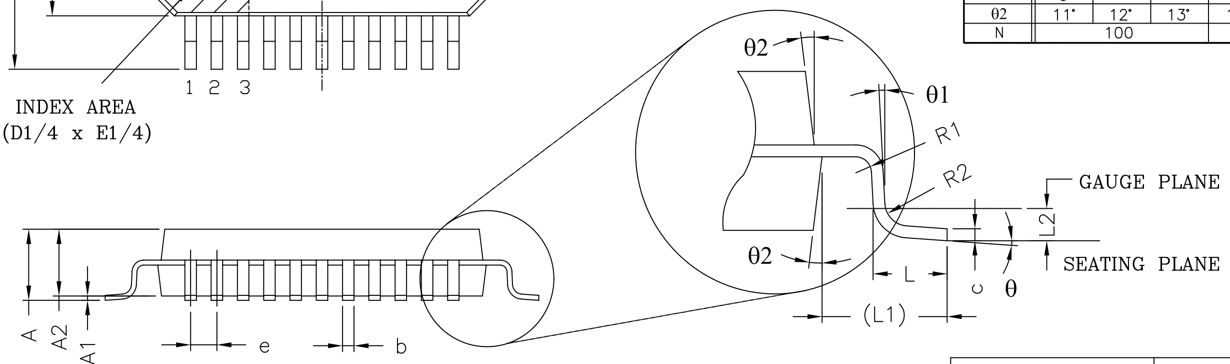


Figure 51. SP3508 Typical Operating Configuration to Serial Port Connector with DCE/DTE programmability

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	05/03/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL





100 Pin LQFP JEDEC MS-026 Variation BED

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	—	0.20	0.004	—	0.008
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
N	100			100		

EXAR Powering Connectivity		EXAR CORPORATION	
		100 PIN LQFP PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 100-PIN LQFP	
By: JL	Date: 11/21/07	Revision: B	Sheet: 1 OF 1

Part Number	Temperature Range	Package Types
SP3508CF-L	0°C to +70°C	100–pin JEDEC LQFP
SP3508EF-L	-40°C to +85°C	100–pin JEDEC LQFP

REVISION HISTORY

Date	Revision	Description
1/12/04	A	Implemented Tracking revision
2/27/04	B	Included Diamond column in spec table inidcating which specs apply over full operating temperature range. Correct typo to Fig. 51 pin 61 and 62.
3/31/04	C	Corrected max dimension for symbol c on LQFP package outline
6/03/04	D	Added table to page 27 and 28
10/12/04	E	Certified conformance to NET1/NET2 and TBR-1/TBR-2 TUV by TUV Rheinland (Test report # TBR2/30451940.001/04)
10/29/04	F	Corrected V.28 Driver Open circuit values, pages 27 and 28 -- both for DCE and DTE that BA(B) should connect to pin 14.
7/17/08	1.0.0	Change Revision format from letter code to number code. Change Logo, footnote and notice statement from Sipex to Exar. Add T_J limits to Absolute Maximum Ratings. Change propagation delay limit specification for V.11 and V.35 Driver/Receiver from 60ns Maximum to 85ns Maximum. Update ordering information to show only RoHS packaging (-L) is available.

Datasheet July 2008

Send your Interface technical inquiry with technical details to: uarttechsupport@exar.com

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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