

PIC18F2450/4450 Data Sheet

24/40/44-Pin High-Performance, 12 MIPS, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

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28/40/44-Pin High-Performance, 12 MIPS, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- · USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports Up to 32 Endpoints (16 bidirectional)
- · 256-Byte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver

Power-Managed Modes:

- · Run: CPU on, Peripherals on
- · Idle: CPU off, Peripherals on
- · Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 5.8 μA Typical
- Sleep mode Currents Down to 0.1 μA Typical
- Timer1 Oscillator: 1.8 μA Typical, 32 kHz, 2V
- Watchdog Timer: 2.1 μA Typical
- · Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High-Precision PLL for USB
- · Two External Clock modes, up to 48 MHz
- · Internal 31 kHz Oscillator
- · Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator Options allow Microcontroller and USB module to Run at Different Clock Speeds
- · Fail-Safe Clock Monitor:
 - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- · High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Three Timer modules (Timer0 to Timer2)
- Capture/Compare/PWM (CCP) module:
- Capture is 16-bit, max. resolution 5.2 ns
- Compare is 16-bit, max. resolution 83.3 ns
- PWM output: PWM resolution is 1 to 10-bit
- · Enhanced USART module:
 - LIN bus support
- 10-Bit, Up to 13-Channel Analog-to-Digital Converter module (A/D):
 - Up to 100 ksps sampling rate
 - Programmable acquisition time

Special Microcontroller Features:

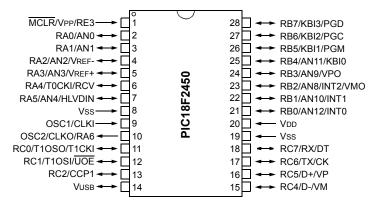
- C Compiler Optimized Architecture with Optional Extended Instruction Set
- Flash Memory Retention: > 40 Years
- · Self-Programmable under Software Control
- · Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- · Programmable Code Protection
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- · In-Circuit Debug (ICD) via Two Pins
- Optional Dedicated ICD/ICSP Port (44-pin TQFP devices only)
- · Wide Operating Voltage Range (2.0V to 5.5V)

	Progra	m Memory	Data					
Device	Flash (bytes)	# Single-Word Instructions	Memory SRAM (bytes)	I/O	10-Bit A/D (ch)	ССР	EUSART	Timers 8/16-Bit
PIC18F2450	16K	8192	768*	23	10	1	1	1/2
PIC18F4450	16K	8192	768*	34	13	1	1	1/2

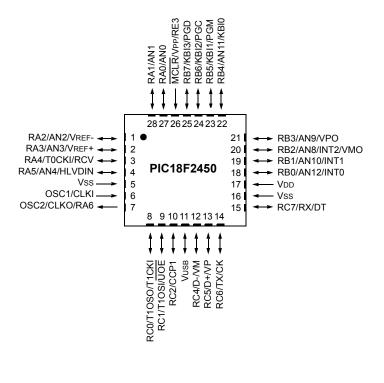
Includes 256 bytes of dual access RAM used by USB module and shared with data memory.

Pin Diagrams

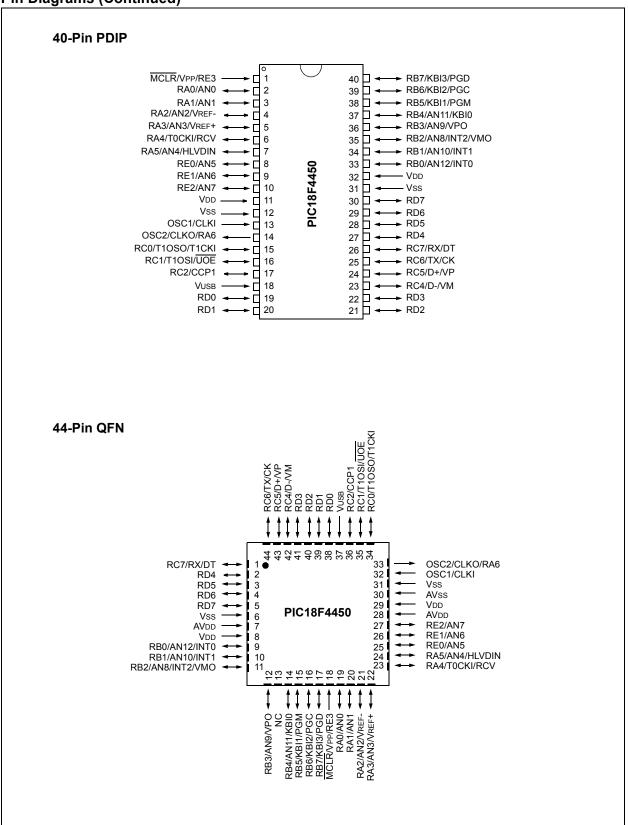
28-Pin SPDIP, SOIC



28-Pin QFN



Pin Diagrams (Continued)



Pin Diagrams (Continued)

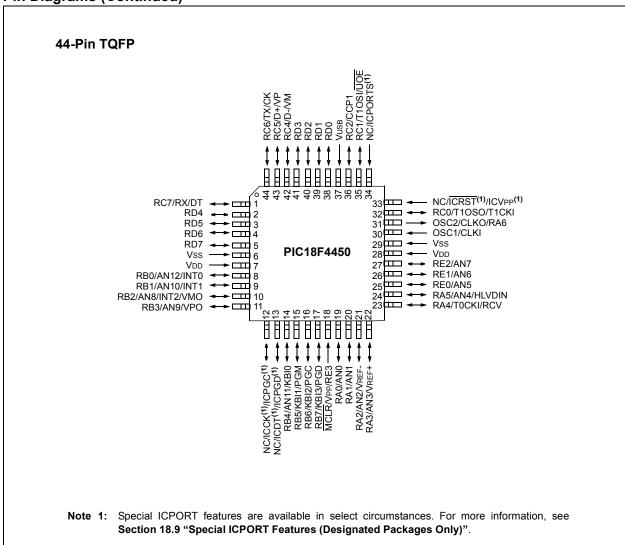


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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

• PIC18F2450 • PIC18F4450

This family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F2450/4450 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2450/4450 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- Alternate Run Modes: By clocking the controller from the Timer1 source or the internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- Multiple Idle Modes: The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- On-the-Fly Mode Switching: The powermanaged modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- Low Consumption in Key Modules: The power requirements for both Timer1 and the Watchdog Timer are minimized. See Section 21.0 "Electrical Characteristics" for values.

1.1.2 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F2450/4450 family incorporate a fully featured Universal Serial Bus communications module that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types. It also incorporates its own on-chip transceiver and 3.3V regulator and supports the use of external transceivers and voltage regulators.

1.1.3 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2450/4450 family offer twelve different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes using crystals or ceramic resonators.
- Four External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- An INTRC source (approximately 31 kHz, stable over temperature and VDD). This option frees an oscillator pin for use as an additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and External Oscillator modes, which allows a wide range of clock speeds from 4 MHz to 48 MHz.
- Asynchronous dual clock operation, allowing the USB module to run from a high-frequency oscillator while the rest of the microcontroller is clocked from an internal low-power oscillator.

The internal oscillator provides a stable reference source that gives the family additional features for robust operation:

- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- Two-Speed Start-up: This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.2 Other Special Features

- Memory Endurance: The Enhanced Flash cells for program memory are rated to last for many thousands of erase/write cycles – up to 100,000.
- Self-Programmability: These devices can write
 to their own program memory spaces under
 internal software control. By using a bootloader
 routine, located in the protected Boot Block at the
 top of program memory, it becomes possible to
 create an application that can update itself in the
 field.
- Extended Instruction Set: The PIC18F2450/ 4450 family introduces an optional extension to the PIC18 instruction set, which adds 8 new instructions and an Indexed Literal Offset Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages such as C.
- Enhanced Addressable USART: This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include Automatic Baud Rate Detection and a 16-bit Baud Rate Generator for improved resolution.
- 10-Bit A/D Converter: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.
- Dedicated ICD/ICSP Port: These devices introduce the use of debugger and programming pins that are not multiplexed with other microcontroller features. Offered as an option in select packages, this feature allows users to develop I/O intensive applications while retaining the ability to program and debug in the circuit.

1.3 Details on Individual Family Members

Devices in the PIC18F2450/4450 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following two ways:

- 1. A/D channels (10 for 28-pin devices, 13 for 40/44-pin devices).
- I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40/44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F2450/4450 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F2450), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF2450), function over an extended VDD range of 2.0V to 5.5V.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2450	PIC18F4450
Operating Frequency	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16384	16384
Program Memory (Instructions)	8192	8192
Data Memory (Bytes)	768	768
Interrupt Sources	13	13
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, D, E
Timers	3	3
Capture/Compare/PWM Modules	1	1
Enhanced USART	1	1
Universal Serial Bus (USB) Module	1	1
10-Bit Analog-to-Digital Module	10 Input Channels	13 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes
Programmable Brown-out Reset	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-Pin SPDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin QFN 44-Pin TQFP

PIC18F2450 (28-PIN) BLOCK DIAGRAM FIGURE 1-1: Data Bus<8> Table Pointer<21> RA0/AN0 Data Latch inc/dec logic 8 8 RA1/AN1 RA2/AN2/VREF-Data Memory RA3/AN3/VREF+ (2 Kbytes) PCLATU PCLATH 21 RA4/T0CKI/RCV 20 Address Latch RA5/AN4/HLVDIN PCU PCH PCL OSC2/CLKO/RA6 Program Counter Data Address<12> 31 Level Stack /12 Address Latch BSR Access FSR0 Program Memory (24/32 Kbytes) STKPTR Bank FSR1 FSR2 Data Latch 12 PORTB RB0/AN12/INT0 inc/dec RB1/AN10/INT1 logic RB2/AN8/INT2/VMO Table Latch RB3/AN9/VPO RB4/AN11/KBI0 Address RB5/KBI1/PGM ROM Latch Instruction Bus <16> Decode RB6/KBI2/PGC RB7/KBI3/PGD IR 8 Instruction State Machine Decode & Control Signals PRODH PRODL PORTC 8 x 8 Multiply RC0/T1OSO/T1CKI RC1/T10SI/UOE OSC1⁽²⁾ Internal RC2/CCP1 Power-up BITOP W Oscillator Timer RC4/D-/VM Block RC5/D+/VP OSC2⁽²⁾ Oscillator RC6/TX/CK INTRC Start-up Time RC7/RX/DT Oscillator T10SI \boxtimes Power-on Reset ALÚ<8> Watchdog T10SO Timer 8 Brown-out Single-Supply MCLR(1) Reset Programming Fail-Safe In-Circuit VDD, VSS Clock Monitor Debugger Band Gap USB Voltage **VUSB** $\boxtimes \blacktriangleleft$ Regulator Reference MCLR/VPP/RE3⁽¹⁾ **BOR** ADC Timer0 Timer2 HLVD Timer1 10-Bit **EUSART** CCP1 **USB Note 1:** RE3 is multiplexed with \overline{MCLR} and is only available when the \overline{MCLR} Resets are disabled. 2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to Section 2.0 "Oscillator Configurations" for additional information.

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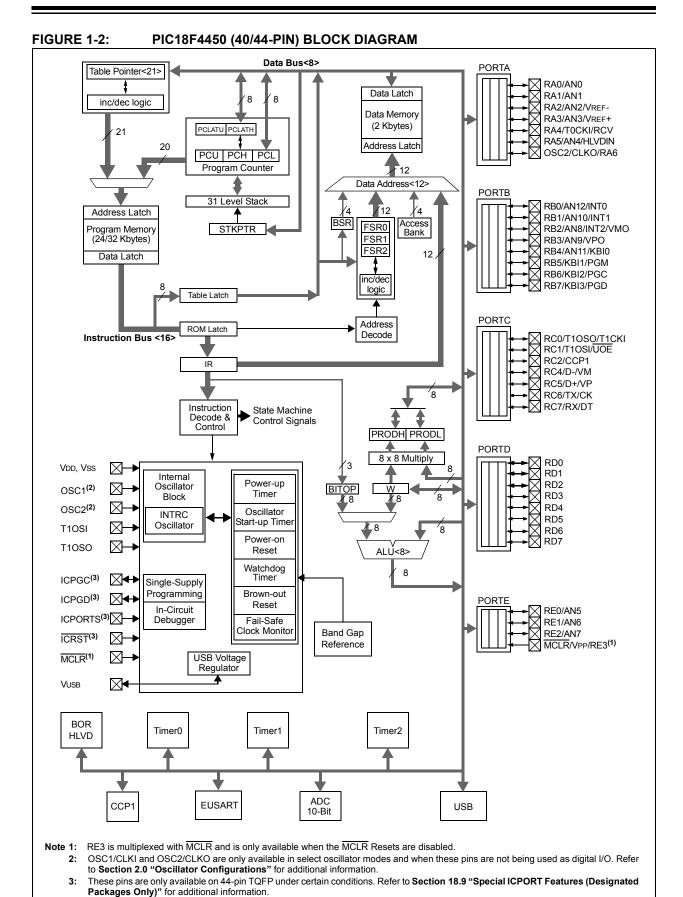


TABLE 1-2: PIC18F2450 PINOUT I/O DESCRIPTIONS

	Pin Nu	mber	Pin	Buffer			
Pin Name	SPDIP, SOIC	QFN	Туре	Туре	Description		
MCLR/VPP/RE3 MCLR	1	26	1	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.		
VPP			Р		Programming voltage input.		
RE3			ı	ST	Digital input.		
OSC1/CLKI OSC1 CLKI	9	6		Analog Analog	' '		
OSC2/CLKO/RA6 OSC2	10	7	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.		
CLKO			0	_	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.		
RA6			I/O	TTL	General purpose I/O pin.		

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels I

O = Output

CMOS = CMOS compatible input or output

I = Input P = Power

TABLE 1-2: PIC18F2450 PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin Number		Pin	Buffer				
Pin Name	SPDIP, SOIC	QFN	Туре	Туре	Description			
					PORTA is a bidirectional I/O port.			
RA0/AN0	2	27						
RA0			I/O	TTL	Digital I/O.			
AN0			I	Analog	Analog input 0.			
RA1/AN1	3	28						
RA1			I/O	TTL	Digital I/O.			
AN1			I	Analog	Analog input 1.			
RA2/AN2/VREF-	4	1						
RA2			I/O	TTL	Digital I/O.			
AN2			I	Analog	Analog input 2.			
VREF-			I	Analog	A/D reference voltage (low) input.			
RA3/AN3/VREF+	5	2						
RA3			I/O	TTL	Digital I/O.			
AN3			- 1	Analog	Analog input 3.			
VREF+			I	Analog	A/D reference voltage (high) input.			
RA4/T0CKI/RCV	6	3						
RA4			I/O	ST	Digital I/O.			
T0CKI			I	ST	Timer0 external clock input.			
RCV			I	TTL	External USB transceiver RCV input.			
RA5/AN4/HLVDIN	7	4						
RA5			I/O	TTL	Digital I/O.			
AN4			I	Analog	Analog input 4.			
HLVDIN			I	Analog	High/Low-Voltage Detect input.			
RA6		_	_		See the OSC2/CLKO/RA6 pin.			

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

O = Output

I = Input

CMOS = CMOS compatible input or output

P = Power

TABLE 1-2: PIC18F2450 PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin Nu	Number Bir Buffer		Buffer					
Pin Name	SPDIP, SOIC	QFN	Pin Type	Туре	Description				
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.				
RB0/AN12/INT0 RB0 AN12 INT0	21	18	I/O I I	TTL Analog ST	Digital I/O. Analog input 12. External interrupt 0.				
RB1/AN10/INT1 RB1 AN10 INT1	22	19	I/O I I	TTL Analog ST	Digital I/O. Analog input 10. External interrupt 1.				
RB2/AN8/INT2/VMO RB2 AN8 INT2 VMO	23	20	I/O 	TTL Analog ST —	Digital I/O. Analog input 8. External interrupt 2. External USB transceiver VMO output.				
RB3/AN9/VPO RB3 AN9 VPO	24	21	I/O I O	TTL Analog	Digital I/O. Analog input 9. External USB transceiver VPO output.				
RB4/AN11/KBI0 RB4 AN11 KBI0	25	22	I/O I I	TTL Analog TTL	Digital I/O. Analog input 11. Interrupt-on-change pin.				
RB5/KBI1/PGM RB5 KBI1 PGM	26	23	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.				
RB6/KBI2/PGC RB6 KBI2 PGC	27	24	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.				
RB7/KBI3/PGD RB7 KBI3 PGD	28	25	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.				

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

O = Output

CMOS = CMOS compatible input or output

I = Input

P = Power

TABLE 1-2: PIC18F2450 PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin Nu	umber B. B. (C.		,	
Pin Name	SPDIP, SOIC	QFN	Pin Type	Buffer Type	Description
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	11	8	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1external clock input.
RC1/T1OSI/UOE RC1 T1OSI UOE	12	9	I/O I O	ST CMOS	Digital I/O. Timer1 oscillator input. External USB transceiver OE output.
RC2/CCP1 RC2 CCP1	13	10	I/O I/O	ST ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output.
RC4/D-/VM RC4 D- VM	15	12	 /O 	TTL — TTL	Digital input. USB differential minus line (input/output). External USB transceiver VM input.
RC5/D+/VP RC5 D+ VP	16	13	 /O O	TTL — TTL	Digital input. USB differential plus line (input/output). External USB transceiver VP input.
RC6/TX/CK RC6 TX CK	17	14	I/O O I/O	ST — ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see RX/DT).
RC7/RX/DT RC7 RX DT	18	15	I/O I I/O	ST ST ST	Digital I/O. EUSART asynchronous receive. EUSART synchronous data (see TX/CK).
RE3	_	_	_	_	See MCLR/VPP/RE3 pin.
Vusb	14	11	Р	_	Internal USB 3.3V voltage regulator. Output, positive supply for internal USB transceiver.
Vss	8, 19	5, 16	Р	_	Ground reference for logic and I/O pins.
VDD	20	17	Р	_	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

O = Output

CMOS = CMOS compatible input or output

I = Input

P = Power

TABLE 1-3: PIC18F4450 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin	Buffer	Description	
Pili Naille	PDIP	QFN	TQFP	Туре	Type	Description
MCLR/VPP/RE3 MCLR	1	18	18	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				Р	 CT	Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI OSC1 CLKI	13	32	30	l I	Analog Analog	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6 OSC2 CLKO	14	33	31	0		Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In select modes, OSC2 pin outputs CLKO which has
RA6				I/O	TTL	1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels
O = Output

= Input = Power

Note 1: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

1

Ρ

TABLE 1-3: PIC18F4450 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pi	Pin Number			Buffer	Description
Pili Naille	PDIP	QFN	TQFP	Type	Type	Description
						PORTA is a bidirectional I/O port.
RA0/AN0 RA0 AN0	2	19	19	I/O I	TTL Analog	Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	20	20	I/O I	TTL Analog	Digital I/O. Analog input 1.
RA2/AN2/VREF- RA2 AN2 VREF-	4	21	21	I/O I I	TTL Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	22	22	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.
RA4/T0CKI/RCV RA4 T0CKI RCV	6	23	23	I/O I I	ST ST TTL	Digital I/O. Timer0 external clock input. External USB transceiver RCV input.
RA5/AN4/HLVDIN RA5 AN4 HLVDIN	7	24	24	I/O I I	TTL Analog Analog	Digital I/O. Analog input 4. High/Low-Voltage Detect input.
RA6	—	_	l —	l —	l —	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

= Input

O = Output P = Power

Note 1: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4450 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pi	n Num	ber	Pin	Buffer	Description
Pin Name	PDIP	QFN	TQFP	Туре	Type	Description
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0 RB0 AN12 INT0	33	9	8	I/O I I	TTL Analog ST	Digital I/O. Analog input 12. External interrupt 0.
RB1/AN10/INT1 RB1 AN10 INT1	34	10	9	I/O I I	TTL Analog ST	Digital I/O. Analog input 10. External interrupt 1.
RB2/AN8/INT2/VMO RB2 AN8 INT2 VMO	35	11	10	I/O I I O	TTL Analog ST —	Digital I/O. Analog input 8. External interrupt 2. External USB transceiver VMO output.
RB3/AN9/VPO RB3 AN9 VPO	36	12	11	I/O I O	TTL Analog —	Digital I/O. Analog input 9. External USB transceiver VPO output.
RB4/AN11/KBI0 RB4 AN11 KBI0	37	14	14	I/O I I	TTL Analog TTL	Digital I/O. Analog input 11. Interrupt-on-change pin.
RB5/KBI1/PGM RB5 KBI1 PGM	38	15	15	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC RB6 KBI2 PGC	39	16	16	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	40	17	17	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

= Input

O = Output

P = Power

Note 1: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4450 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pi	n Num	ber	Pin	Buffer	Description
Pili Naille	PDIP	QFN	TQFP	Туре	Type	Description
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	34	32	1/0	ОТ.	Dirital I/O
RC0 T1OSO				I/O O	ST	Digital I/O. Timer1 oscillator output.
T1CKI				ĭ	ST	Timer 1 oscillator output: Timer1 external clock input.
RC1/T1OSI/UOE	16	35	35	•		The state of the s
RC1	10	33		I/O	ST	Digital I/O.
T1OSI				ı	CMOS	Timer1 oscillator input.
UOE				0	_	External USB transceiver OE output.
RC2/CCP1	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
RC4/D-/VM	23	42	42			Digitalian
RC4 D-				1/0	TTL	Digital input. USB differential minus line (input/output).
VM				1	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			'
RC5				I	TTL	Digital input.
D+				I/O	_	USB differential plus line (input/output).
VP				l	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			D: 11 11 0
RC6 TX				I/O O	ST	Digital I/O. EUSART asynchronous transmit.
CK				1/0	ST	EUSART asynchronous clock (see RX/DT).
RC7/RX/DT	26	1	1		.	
RC7	20	'	'	I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

= Input = Output = Power

Note 1: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4450 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin	Buffer	Description	
Fill Name	PDIP	QFN	TQFP	Type	Type	Description
						PORTD is a bidirectional I/O port.
RD0	19	38	38	I/O	ST	Digital I/O.
RD1	20	39	39	I/O	ST	Digital I/O.
RD2	21	40	40	I/O	ST	Digital I/O.
RD3	22	41	41	I/O	ST	Digital I/O.
RD4	27	2	2	I/O	ST	Digital I/O.
RD5	28	3	3	I/O	ST	Digital I/O.
RD6	29	4	4	I/O	ST	Digital I/O.
RD7	30	5	5	I/O	ST	Digital I/O.

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

= Input

= Output = Power

Note 1: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4450 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin	Buffer	Description	
Pin Name	PDIP	QFN	TQFP	Туре	Type	Description
						PORTE is a bidirectional I/O port.
RE0/AN5 RE0 AN5	8	25	25	I/O I	ST Analog	Digital I/O. Analog input 5.
RE1/AN6 RE1 AN6	9	26	26	I/O I	ST Analog	Digital I/O. Analog input 6.
RE2/AN7 RE2 AN7	10	27	27	I/O I	ST Analog	Digital I/O. Analog input 7.
RE3	_	_	_	_	_	See MCLR/VPP/RE3 pin.
Vss	12, 31	6, 30, 31	6, 29	Р	_	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	Р	_	Positive supply for logic and I/O pins.
Vusb	18	37	37	Р	_	Internal USB 3.3V voltage regulator output. Positive supply for internal USB transceiver.
NC/ICCK/ICPGC ⁽¹⁾ ICCK ICPGC	_		12	I/O I/O	ST ST	No Connect or dedicated ICD/ICSP™ port clock. In-Circuit Debugger clock. ICSP programming clock.
NC/ICDT/ICPGD ⁽¹⁾ ICDT ICPGD			13	I/O I/O	ST ST	No Connect or dedicated ICD/ICSP port clock. In-Circuit Debugger data. ICSP programming data.
NC/ICRST/ICV _{PP} ⁽¹⁾ ICRST ICV _{PP}	_	_	33	I P		No Connect or dedicated ICD/ICSP port Reset. Master Clear (Reset) input. Programming voltage input.
NC/ICPORTS ⁽¹⁾ ICPORTS	_	_	34	Р	_	No Connect or 28-pin device emulation. Enable 28-pin device emulation when connected to Vss.
NC		13	_	_	_	No Connect.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

0 = Output CMOS = CMOS compatible input or output

= Input

Р = Power

Note 1: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

NOTES:

2.0 OSCILLATOR CONFIGURATIONS

2.1 Overview

Devices in the PIC18F2450/4450 family incorporate a different oscillator and microcontroller clock system than the non-USB PIC18F devices. The addition of the USB module, with its unique requirements for a stable clock source, make it necessary to provide a separate clock source that is compliant with both USB low-speed and full-speed specifications.

To accommodate these requirements, PIC18F2450/4450 devices include a new clock branch to provide a 48 MHz clock for full-speed USB operation. Since it is driven from the primary clock source, an additional system of prescalers and postscalers has been added to accommodate a wide range of oscillator frequencies. An overview of the oscillator structure is shown in Figure 2-1.

Other oscillator features used in PIC18 enhanced microcontrollers, such as the internal RC oscillator and clock switching, remain the same. They are discussed later in this chapter.

2.1.1 OSCILLATOR CONTROL

The operation of the oscillator in PIC18F2450/4450 devices is controlled through two Configuration registers and two control registers. Configuration registers, CONFIG1L and CONFIG1H, select the oscillator mode and USB prescaler/postscaler options. As Configuration bits, these are set when the device is programmed and left in that configuration until the device is reprogrammed.

The OSCCON register (Register 2-1) selects the Active Clock mode; it is primarily used in controlling clock switching in power-managed modes. Its use is discussed in **Section 2.4.1 "Oscillator Control Register"**.

2.2 Oscillator Types

PIC18F2450/4450 devices can be operated in twelve distinct oscillator modes. In contrast with the non-USB PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

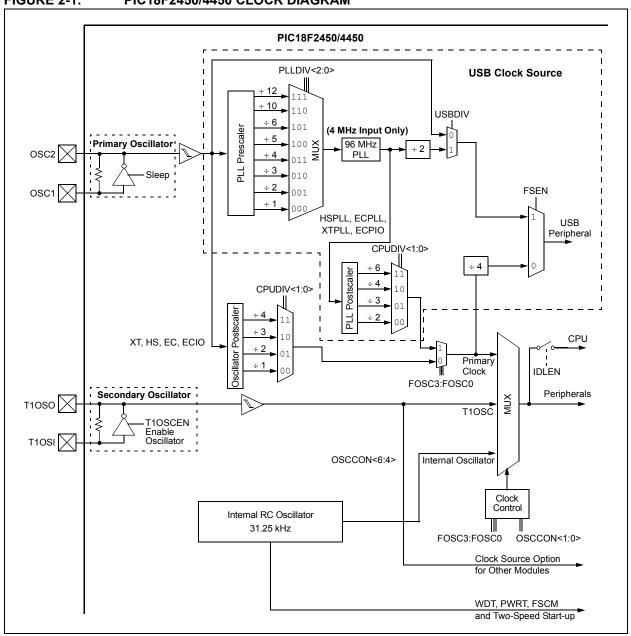
1.	XT	Crystal/Resonator
2.	XTPLL	Crystal/Resonator with PLL Enabled
3.	HS	High-Speed Crystal/Resonator
4.	HSPLL	High-Speed Crystal/Resonator with PLL Enabled
5.	EC	External Clock with Fosc/4 Output
6.	ECIO	External Clock with I/O on RA6
7.	ECPLL	External Clock with PLL Enabled and Fosc/4 Output on RA6
8.	ECPIO	External Clock with PLL Enabled, I/O on RA6
9.	INTHS	Internal Oscillator used as Microcontroller Clock Source, HS Oscillator used as USB Clock Source
10.	INTXT	Internal Oscillator used as Microcontroller Clock Source, XT Oscillator used as USB Clock Source
11.	INTIO	Internal Oscillator used as Microcontroller Clock Source, EC Oscillator used as USB Clock Source, Digital I/O on RA6
12.	INTCKO	Internal Oscillator used as Microcontroller Clock Source, EC Oscillator used as USB Clock Source, Fosc/4 Output on RA6

2.2.1 OSCILLATOR MODES AND USB OPERATION

Because of the unique requirements of the USB module, a different approach to clock operation is necessary. In previous PIC® microcontrollers, all core and peripheral clocks were driven by a single oscillator source; the usual sources were primary, secondary or the internal oscillator. With PIC18F2450/4450 devices, the primary oscillator becomes part of the USB module and cannot be associated to any other clock source. Thus, the USB module must be clocked from the primary clock source; however, the microcontroller core and other peripherals can be separately clocked from the secondary or internal oscillators as before.

Because of the timing requirements imposed by USB, an internal clock of either 6 MHz or 48 MHz is required while the USB module is enabled. Fortunately, the microcontroller and other peripherals are not required to run at this clock speed when using the primary oscillator. There are numerous options to achieve the USB module clock requirement and still provide flexibility for clocking the rest of the device from the primary oscillator source. These are detailed in **Section 2.3** "Oscillator Settings for USB".

FIGURE 2-1: PIC18F2450/4450 CLOCK DIAGRAM



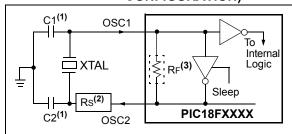
2.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, HSPLL, XT and XTPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-2 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note: Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-2: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, HS OR HSPLL CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2

- 2: A series resistor (Rs) may be required for AT strip cut crystals.
- 3: RF varies with the oscillator mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Typical Capacitor Values Used:						
Mode	Freq	OSC1	OSC2			
XT	4.0 MHz	33 pF	33 pF			
HS	8.0 MHz 16.0 MHz	27 pF 22 pF	27 pF 22 pF			

Capacitor values are for design guidance only.

These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized**.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following Table 2-2 for additional information.

Resonators Used:				
4.0 MHz				
8.0 MHz				
16.0 MHz				

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq		pacitor Values ested:	
	rreq	C1	C2	
XT	4 MHz	27 pF	27 pF	
HS	4 MHz	27 pF	27 pF	
	8 MHz	22 pF	22 pF	
	20 MHz	15 pF	15 pF	

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

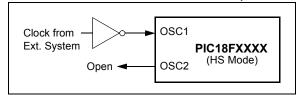
Crystals Used:
4 MHz
8 MHz
20 MHz

- **Note 1:** Higher capacitance increases the stability of oscillator but also increases the start-up time.
 - 2: When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - **4:** Rs may be required to avoid overdriving crystals with low drive level specification.
 - **5:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An internal postscaler allows users to select a clock frequency other than that of the crystal or resonator. Frequency division is determined by the CPUDIV Configuration bits. Users may select a clock frequency of the oscillator frequency, or 1/2, 1/3 or 1/4 of the frequency.

An external clock may also be used when the microcontroller is in HS Oscillator mode. In this case, the OSC2/CLKO pin is left open (Figure 2-3).

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)

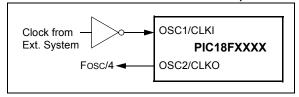


2.2.3 EXTERNAL CLOCK INPUT

The EC, ECIO, ECPLL and ECPIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

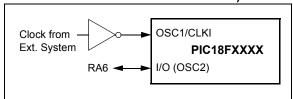
In the EC and ECPLL Oscillator modes, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC AND ECPLL CONFIGURATION)



The ECIO and ECPIO Oscillator modes function like the EC and ECPLL modes, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO AND ECPIO CONFIGURATION)



The internal postscaler for reducing clock frequency in XT and HS modes is also available in EC and ECIO modes.

2.2.4 PLL FREQUENCY MULTIPLIER

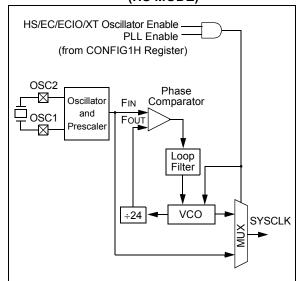
PIC18F2450/4450 devices include a Phase Locked Loop (PLL) circuit. This is provided specifically for USB applications with lower speed oscillators and can also be used as a microcontroller clock source.

The PLL is enabled in HSPLL, XTPLL, ECPLL and ECPIO Oscillator modes. It is designed to produce a fixed 96 MHz reference clock from a fixed 4 MHz input. The output can then be divided and used for both the USB and the microcontroller core clock. Because the PLL has a fixed frequency input and output, there are eight prescaling options to match the oscillator input frequency to the PLL.

There is also a separate postscaler option for deriving the microcontroller clock from the PLL. This allows the USB peripheral and microcontroller to use the same oscillator input and still operate at different clock speeds. In contrast to the postscaler for XT, HS and EC modes, the available options are 1/2, 1/3, 1/4 and 1/6 of the PLL output.

The HSPLL, ECPLL and ECPIO modes make use of the HS mode oscillator for frequencies up to 48 MHz. The prescaler divides the oscillator input by up to 12 to produce the 4 MHz drive for the PLL. The XTPLL mode can only use an input frequency of 4 MHz which drives the PLL directly.

FIGURE 2-6: PLL BLOCK DIAGRAM (HS MODE)



2.2.5 INTERNAL OSCILLATOR

The PIC18F2450/4450 devices include an internal RC oscillator (INTRC) which provides a nominal 31 kHz output. INTRC is enabled if it is selected as the device clock source; it is also enabled automatically when any of the following are enabled:

- · Power-up Timer
- · Fail-Safe Clock Monitor
- · Watchdog Timer
- · Two-Speed Start-up

These features are discussed in greater detail in Section 18.0 "Special Features of the CPU".

2.2.5.1 Internal Oscillator Modes

When the internal oscillator is used as the micro-controller clock source, one of the other oscillator modes (External Clock or External Crystal/Resonator) must be used as the USB clock source. The choice of USB clock source is determined by the particular internal oscillator mode.

There are four distinct modes available:

- 1. INTHS mode: The USB clock is provided by the oscillator in HS mode.
- INTXT mode: The USB clock is provided by the oscillator in XT mode.
- 3. INTCKO mode: The USB clock is provided by an external clock input on OSC1/CLKI; the OSC2/CLKO pin outputs Fosc/4.
- 4. INTIO mode: The USB clock is provided by an external clock input on OSC1/CLKI; the OSC2/CLKO pin functions as a digital I/O (RA6).

Of these four modes, only INTIO mode frees up an additional pin (OSC2/CLKO/RA6) for port I/O use.

2.3 Oscillator Settings for USB

When the PIC18F2450/4450 is used for USB connectivity, it must have either a 6 MHz or 48 MHz clock for USB operation, depending on whether Low-Speed or Full-Speed mode is being used. This may require some forethought in selecting an oscillator frequency and programming the device.

The full range of possible oscillator configurations compatible with USB operation is shown in Table 2-3.

2.3.1 LOW-SPEED OPERATION

The USB clock for Low-Speed mode is derived from the primary oscillator chain and not directly from the PLL. It is divided by 4 to produce the actual 6 MHz clock. Because of this, the microcontroller can only use a clock frequency of 24 MHz when the USB module is active and the controller clock source is one of the primary oscillator modes (XT, HS or EC, with or without the PLL).

This restriction does not apply if the microcontroller clock source is the secondary oscillator or internal oscillator.

2.3.2 RUNNING DIFFERENT USB AND MICROCONTROLLER CLOCKS

The USB module, in either mode, can run asynchronously with respect to the microcontroller core and other peripherals. This means that applications can use the primary oscillator for the USB clock while the microcontroller runs from a separate clock source at a lower speed. If it is necessary to run the entire application from only one clock source, full-speed operation provides a greater selection of microcontroller clock frequencies.

TABLE 2-3: OSCILLATOR CONFIGURATION OPTIONS FOR USB OPERATION

Input Oscillator Frequency	PLL Division (PLLDIV2:PLLDIV0)	Clock Mode (FOSC3:FOSC0)	MCU Clock Division (CPUDIV1:CPUDIV0)	Microcontroller Clock Frequency
			None (00)	48 MHz
40 MI I=	N/A ⁽¹⁾	50 5010	÷2 (01)	24 MHz
48 MHz	N/A(··/	EC, ECIO	÷3 (10)	16 MHz
			÷4 (11)	12 MHz
			None (00)	48 MHz
		FC FCIO	÷2 (01)	24 MHz
		EC, ECIO	÷3 (10)	16 MHz
48 MHz	. 12 /111		÷4 (11)	12 MHz
40 WII 12	÷ 12 (111)		÷2 (00)	48 MHz
		ECPLL, ECPIO	÷3 (01)	32 MHz
		ECFLL, ECFIO	÷4 (10)	24 MHz
			÷6 (11)	16 MHz
			None (00)	40 MHz
		EC, ECIO	÷2 (01)	20 MHz
		EC, ECIO	÷3 (10)	13.33 MHz
40 MH=	.40 /110)		÷4 (11)	10 MHz
40 MHz	÷ 10 (110)		÷2 (00)	48 MHz
		FORL FORM	÷3 (01)	32 MHz
		ECPLL, ECPIO	÷4 (10)	24 MHz
			÷6 (11)	16 MHz
			None (00)	24 MHz
		HS, EC, ECIO	÷2 (01)	12 MHz
		H3, E0, E010	÷3 (10)	8 MHz
24 MHz	÷6 (101)		÷4 (11)	6 MHz
24 WII IZ	÷0 (101)		÷2 (00)	48 MHz
		HSPLL, ECPLL, ECPIO	÷3 (01)	32 MHz
		HISPEL, EGPEL, EGPIO	÷4 (10)	24 MHz
			÷6 (11)	16 MHz
			None (00)	20 MHz
		HS, EC, ECIO	÷2 (01)	10 MHz
		110, 20, 2010	÷3 (10)	6.67 MHz
20 MHz	÷ 5 (100)		÷4 (11)	5 MHz
20 1011 12	.5 (100)		÷2 (00)	48 MHz
		HSPLL, ECPLL, ECPIO	÷3 (01)	32 MHz
		TIOI EE, EOI EE, EOI IO	÷4 (10)	24 MHz
			÷6 (11)	16 MHz
			None (00)	16 MHz
		HS, EC, ECIO	÷2 (01)	8 MHz
		, 23, 20.0	÷3 (10)	5.33 MHz
16 MHz	÷ 4 (011)		÷4 (11)	4 MHz
10 111112	(\ + + /		÷2 (00)	48 MHz
		HSPLL, ECPLL, ECPIO	÷3 (01)	32 MHz
			÷4 (10)	24 MHz
		a exclusively associated wi	÷6 (11)	16 MHz

Legend: All clock frequencies, except 24 MHz, are exclusively associated with full-speed USB operation (USB clock of 48 MHz).

Bold is used to highlight clock selections that are compatible with low-speed USB operation (system clock of 24 MHz,

USB clock of 6 MHz).

Note 1: Only valid when the USBDIV Configuration bit is cleared.

TABLE 2-3: OSCILLATOR CONFIGURATION OPTIONS FOR USB OPERATION (CONTINUED)

Input Oscillator Frequency	PLL Division (PLLDIV2:PLLDIV0)	Clock Mode (FOSC3:FOSC0)	MCU Clock Division (CPUDIV1:CPUDIV0)	Microcontroller Clock Frequency
			None (00)	12 MHz
		HS, EC, ECIO	÷2 (01)	6 MHz
		ПЗ, EG, EGIO	÷3 (10)	4 MHz
12 MHz	.2 (010)		÷4 (11)	3 MHz
12 IVITZ	÷3 (010)		÷2 (00)	48 MHz
		HSPLL, ECPLL, ECPIO	÷3 (01)	32 MHz
		HOPEL, ECPLE, ECPIO	÷4 (10)	24 MHz
			÷6 (11)	16 MHz
		HS, EC, ECIO	None (00)	8 MHz
			÷2 (01)	4 MHz
			÷3 (10)	2.67 MHz
8 MHz	.2 (0.01)		÷4 (11)	2 MHz
O IVITZ	÷2 (001)		÷2 (00)	48 MHz
		HSPLL, ECPLL, ECPIO	÷3 (01)	32 MHz
	l		÷4 (10)	24 MHz
			÷6 (11)	16 MHz
		None (00)	4 MHz	
		XT, HS, EC, ECIO	÷2 (01)	2 MHz
		AI, HO, EU, EUIU	÷3 (10)	1.33 MHz
4 MHz	.1 (000)		÷4 (11)	1 MHz
4 IVI□Z	÷1 (000)		÷2 (00)	48 MHz
		HSPLL, ECPLL, XTPLL,	÷3 (01)	32 MHz
		ECPIO	÷4 (10)	24 MHz
			÷6 (11)	16 MHz

Legend: All clock frequencies, except 24 MHz, are exclusively associated with full-speed USB operation (USB clock of 48 MHz).

Bold is used to highlight clock selections that are compatible with low-speed USB operation (system clock of 24 MHz, USB clock of 6 MHz).

Note 1: Only valid when the USBDIV Configuration bit is cleared.

2.4 Clock Sources and Oscillator Switching

Like previous PIC18 enhanced devices, the PIC18F2450/4450 family includes a feature that allows the device clock source to be switched from the main oscillator to an alternate, low-frequency clock source. PIC18F2450/4450 devices offer two alternate clock sources. When an alternate clock source is enabled, the various power-managed operating modes are available.

Essentially, there are three clock sources for these devices:

- · Primary oscillators
- · Secondary oscillators
- · Internal oscillator

The **primary oscillators** include the External Crystal and Resonator modes, the External Clock modes and the internal oscillator. The particular mode is defined by the FOSC3:FOSC0 Configuration bits. The details of these modes are covered earlier in this chapter.

The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode.

PIC18F2450/4450 devices offer the Timer1 oscillator as a secondary oscillator. This oscillator, in all power-managed modes, is often the time base for functions such as a Real-Time Clock (RTC). Most often, a 32.768 kHz watch crystal is connected between the RC0/T1OSO/T1CKI and RC1/T1OSI/UOE pins. Like the XT and HS Oscillator mode circuits, loading capacitors are also connected from each pin to ground. The Timer1 oscillator is discussed in greater detail in Section 11.3 "Timer1 Oscillator".

In addition to being a primary clock source, the **internal oscillator** is available as a power-managed mode clock source. The INTRC source is also used as the clock source for several special features, such as the WDT and Fail-Safe Clock Monitor.

2.4.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 2-1) controls several aspects of the device clock's operation, both in full-power operation and in power-managed modes.

The System Clock Select bits, SCS1:SCS0, select the clock source. The available clock sources are the primary clock (defined by the FOSC3:FOSC0 Configuration bits), the secondary clock (Timer1 oscillator) and the internal oscillator. The clock source changes immediately, after one or more of the bits is written to, following a brief clock transition interval. The SCS bits are cleared on all forms of Reset.

INTRC always remains the clock source for features such as the Watchdog Timer and the Fail-Safe Clock Monitor.

The OSTS and T1RUN bits indicate which clock source is currently providing the device clock. The OSTS bit indicates that the Oscillator Start-up Timer (OST) has timed out and the primary clock is providing the device clock in primary clock modes. The T1RUN bit (T1CON<6>) indicates when the Timer1 oscillator is providing the device clock in secondary clock modes. In power-managed modes, only one of these three bits will be set at any time. If none of these bits are set, the INTRC is providing the clock or the internal oscillator has just started and is not yet stable.

The IDLEN bit determines if the device goes into Sleep mode, or one of the Idle modes, when the SLEEP instruction is executed.

The use of the flag and control bits in the OSCCON register is discussed in more detail in **Section 3.0** "Power-Managed Modes".

- Note 1: The Timer1 oscillator must be enabled to select the secondary clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 Control register (T1CON<3>). If the Timer1 oscillator is not enabled, then any attempt to select a secondary clock source will be ignored.
 - 2: It is recommended that the Timer1 oscillator be operating and stable prior to switching to it as the clock source; otherwise, a very long delay may occur while the Timer1 oscillator starts.

2.4.2 OSCILLATOR TRANSITIONS

PIC18F2450/4450 devices contain circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in Section 3.1.2 "Entering Power-Managed Modes".

REGISTER 2-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	R ⁽¹⁾	U-0	R/W-0	R/W-0
IDLEN	_	_	_	OSTS	_	SCS1	SCS0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 IDLEN: Idle Enable bit

1 = Device enters Idle mode on SLEEP instruction0 = Device enters Sleep mode on SLEEP instruction

bit 6-4 Unimplemented: Read as '0'

bit 3 OSTS: Oscillator Start-up Time-out Status bit⁽¹⁾

1 = Oscillator Start-up Timer time-out has expired; primary oscillator is running0 = Oscillator Start-up Timer time-out is running; primary oscillator is not ready

bit 2 **Unimplemented:** Read as '0'

bit 1-0 SCS1:SCS0: System Clock Select bits

1x = Internal oscillator 01 = Timer1 oscillator 00 = Primary oscillator

Note 1: Depends on the state of the IESO Configuration bit.

2.5 Effects of Power-Managed Modes on the Various Clock Sources

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. Unless the USB module is enabled, the OSC1 pin (and OSC2 pin if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the Timer1 oscillator is operating and providing the device clock. The Timer1 oscillator may also run in all power-managed modes if required to clock Timer1.

In internal oscillator modes (RC_RUN and RC_IDLE), the internal oscillator provides the device clock source. The 31 kHz INTRC output can be used directly to provide the clock and may be enabled to support various special features regardless of the power-managed mode (see Section 18.2 "Watchdog Timer (WDT)", Section 18.3 "Two-Speed Start-up" and Section 18.4 "Fail-Safe Clock Monitor" for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up).

Regardless of the Run or Idle mode selected, the USB clock source will continue to operate. If the device is operating from a crystal or resonator-based oscillator, that oscillator will continue to clock the USB module. The core and all other modules will switch to the new clock source.

If the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Sleep mode should never be invoked while the USB module is operating and connected. The only exception is when the device has been issued a "Suspend" command over the USB. Once the module has suspended operation and shifted to a low-power state, the microcontroller may be safely put into Sleep mode.

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTRC is required to support WDT operation. The Timer1 oscillator may be operating to support a Real-Time Clock. Other features may be operating that do not require a device clock source (i.e., PSP, INTx pins and others). Peripherals that may add significant current consumption are listed in Section 21.2 "DC Characteristics: Power-Down and Supply Current".

2.6 Power-up Delays

Power-up delays are controlled by two timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 4.5 "Device Reset Timers"**.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up (parameter 33, Table 21-10). It is enabled by clearing (= $^\circ$) the PWRTEN Configuration bit.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the HSPLL Oscillator mode is selected, the device is kept in Reset for an additional 2 ms following the HS mode OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of interval, TCSD (parameter 38, Table 21-10), following POR, while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC or internal oscillator modes are used as the primary clock source.

TABLE 2-4: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

Oscillator Mode	OSC1 Pin	OSC2 Pin
INTCKO	Floating, pulled by external clock	At logic low (clock/4 output)
INTIO	Floating, pulled by external clock	Configured as PORTA, bit 6
ECIO, ECPIO	Floating, pulled by external clock	Configured as PORTA, bit 6
EC	Floating, pulled by external clock	At logic low (clock/4 output)
XT and HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

Note: See Table 4-2 in Section 4.0 "Reset" for time-outs due to Sleep and MCLR Reset.

3.0 POWER-MANAGED MODES

PIC18F2450/4450 devices offer a total of seven operating modes for more efficient power management. These modes provide a variety of options for selective power conservation in applications where resources may be limited (i.e., battery-powered devices).

There are three categories of power-managed modes:

- · Run modes
- · Idle modes
- · Sleep mode

These categories define which portions of the device are clocked and sometimes, what speed. The Run and Idle modes may use any of the three available clock sources (primary, secondary or internal oscillator); the Sleep mode does not use a clock source.

The power-managed modes include several power-saving features offered on previous PIC® microcontrollers. One is the clock switching feature, offered in other PIC18 devices, allowing the controller to use the Timer1 oscillator in place of the primary oscillator. Also included is the Sleep mode, offered by all PIC microcontrollers, where all device clocks are stopped.

3.1 Selecting Power-Managed Modes

Selecting a power-managed mode requires two decisions: if the CPU is to be clocked or not and the selection of a clock source. The IDLEN bit (OSCCON<7>) controls CPU clocking, while the SCS1:SCS0 bits (OSCCON<1:0>) select the clock source. The individual modes, bit settings, clock sources and affected modules are summarized in Table 3-1.

3.1.1 CLOCK SOURCES

The SCS1:SCS0 bits allow the selection of one of three clock sources for power-managed modes. They are:

- The primary clock, as defined by the FOSC3:FOSC0 Configuration bits
- The secondary clock (the Timer1 oscillator)
- The internal oscillator (for RC modes)

3.1.2 ENTERING POWER-MANAGED MODES

Switching from one power-managed mode to another begins by loading the OSCCON register. The SCS1:SCS0 bits select the clock source and determine which Run or Idle mode is to be used. Changing these bits causes an immediate switch to the new clock source, assuming that it is running. The switch may also be subject to clock transition delays. These are discussed in Section 3.1.3 "Clock Transitions and Status Indicators" and subsequent sections.

Entry to the power-managed Idle or Sleep modes is triggered by the execution of a SLEEP instruction. The actual mode that results depends on the status of the IDLEN bit.

Depending on the current mode and the mode being switched to, a change to a power-managed mode does not always require setting all of these bits. Many transitions may be done by changing the oscillator select bits, or changing the IDLEN bit, prior to issuing a SLEEP instruction. If the IDLEN bit is already configured correctly, it may only be necessary to perform a SLEEP instruction to switch to the desired mode.

TABLE 3-1: POWER-MANAGED MODES

	oso	OSCCON Bits		e Clocking	A . !! . ! ! ! ! !		
Mode	IDLEN ⁽¹⁾	SCS1:SCS0	CPU	CPU Peripherals	Available Clock and Oscillator Source		
Sleep	0	N/A	Off	Off	None – all clocks are disabled		
PRI_RUN	N/A	00	Clocked	Clocked	Primary – all oscillator modes. This is the normal full-power execution mode.		
SEC_RUN	N/A	01	Clocked	Clocked	Secondary – Timer1 oscillator		
RC_RUN	N/A	1x	Clocked	Clocked	Internal oscillator ⁽²⁾		
PRI_IDLE	1	00	Off	Clocked	Primary – all oscillator modes		
SEC_IDLE	1	01	Off	Clocked	Secondary – Timer1 oscillator		
RC_IDLE	1	1x	Off	Clocked	Internal oscillator ⁽²⁾		

Note 1: IDLEN reflects its value when the SLEEP instruction is executed.

2: Clock is INTRC source.

3.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Two bits indicate the current clock source and its status. They are:

- OSTS (OSCCON<3>)
- T1RUN (T1CON<6>)

In general, only one of these bits will be set while in a given power-managed mode. When the OSTS bit is set, the primary clock is providing the device clock. When the T1RUN bit is set, the Timer1 oscillator is providing the clock.

Note: Executing a SLEEP instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep mode, or one of the Idle modes, depending on the setting of the IDLEN bit.

3.1.4 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the SLEEP instruction is determined by the setting of the IDLEN bit at the time the instruction is executed. If another SLEEP instruction is executed, the device will enter the power-managed mode specified by IDLEN at that time. If IDLEN has changed, the device will enter the new power-managed mode specified by the new setting.

3.2 Run Modes

In the Run modes, clocks to both the core and peripherals are active. The difference between these modes is the clock source.

3.2.1 PRI_RUN MODE

The PRI_RUN mode is the normal, full-power execution mode of the microcontroller. This is also the default mode upon a device Reset unless Two-Speed Start-up is enabled (see **Section 18.3 "Two-Speed Start-up"** for details). In this mode, the OSTS bit is set.

3.2.2 SEC RUN MODE

The SEC_RUN mode is the compatible mode to the "clock switching" feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high accuracy clock source.

SEC_RUN mode is entered by setting the SCS1:SCS0 bits to '01'. The device clock source is switched to the Timer1 oscillator (see Figure 3-1), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

Note: The Timer1 oscillator should already be running prior to entering SEC_RUN mode. If the T10SCEN bit is not set when the SCS1:SCS0 bits are set to '01', entry to SEC_RUN mode will not occur. If the Timer1 oscillator is enabled but not yet running, device clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation

may result.

On transitions from SEC_RUN mode to PRI_RUN mode, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see

Figure 3-2). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the clock. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run.



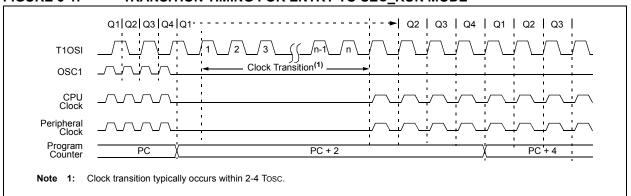
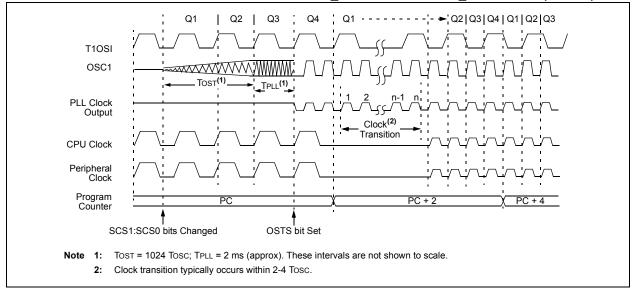


FIGURE 3-2: TRANSITION TIMING FROM SEC_RUN MODE TO PRI_RUN MODE (HSPLL)



PIC18F2450/4450

3.2.3 RC RUN MODE

In RC_RUN mode, the CPU and peripherals are clocked from the internal oscillator; the primary clock is shut down. When using the INTRC source, this mode provides the best power conservation of all the Run modes while still executing code. It works well for user applications which are not highly timing sensitive or do not require high-speed clocks at all times.

If the primary clock source is the internal oscillator (INTRC), there are no distinguishable differences between the PRI_RUN and RC_RUN modes during execution. However, a clock switch delay will occur during entry to and exit from RC_RUN mode. Therefore, if the primary clock source is the internal oscillator, the use of RC_RUN mode is not recommended.

This mode is entered by setting SCS1 to '1'. Although it is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. When the clock source is switched to the INTRC (see Figure 3-3), the primary oscillator is shut down and the OSTS bit is cleared.

On transitions from RC_RUN mode to PRI_RUN mode, the device continues to be clocked from the INTRC while the primary clock is started. When the primary clock becomes ready, a clock switch to the primary clock occurs (see Figure 3-4). When the clock switch is complete, the OSTS bit is set and the primary clock is providing the device clock. The IDLEN and SCS bits are not affected by the switch. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.



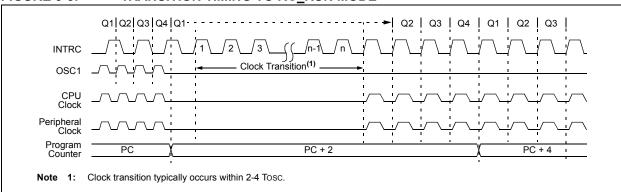
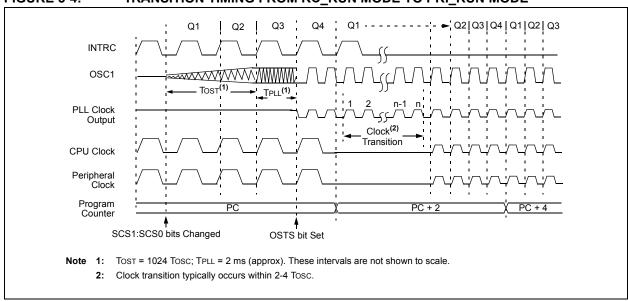


FIGURE 3-4: TRANSITION TIMING FROM RC RUN MODE TO PRI RUN MODE



3.3 Sleep Mode

The power-managed Sleep mode in the PIC18F2450/4450 devices is identical to the legacy Sleep mode offered in all other PIC microcontrollers. It is entered by clearing the IDLEN bit (the default state on device Reset) and executing the SLEEP instruction. This shuts down the selected oscillator (Figure 3-5). All clock source status bits are cleared.

Entering the Sleep mode from any other mode does not require a clock switch. This is because no clocks are needed once the controller has entered Sleep. If the WDT is selected, the INTRC source will continue to operate. If the Timer1 oscillator is enabled, it will also continue to run.

When a wake event occurs in Sleep mode (by interrupt, Reset or WDT time-out), the device will not be clocked until the clock source selected by the SCS1:SCS0 bits becomes ready (see Figure 3-6), or it will be clocked from the internal oscillator if either the Two-Speed Start-up or the Fail-Safe Clock Monitor are enabled (see **Section 18.0 "Special Features of the CPU"**). In either case, the OSTS bit is set when the primary clock is providing the device clocks. The IDLEN and SCS bits are not affected by the wake-up.

3.4 Idle Modes

The Idle modes allow the controller's CPU to be selectively shut down while the peripherals continue to operate. Selecting a particular Idle mode allows users to further manage power consumption.

If the IDLEN bit is set to '1' when a SLEEP instruction is executed, the peripherals will be clocked from the clock source selected using the SCS1:SCS0 bits; however, the CPU will not be clocked. The clock source status bits are not affected. Setting IDLEN and executing a SLEEP instruction provides a quick method of switching from a given Run mode to its corresponding Idle mode.

If the WDT is selected, the INTRC source will continue to operate. If the Timer1 oscillator is enabled, it will also continue to run.

Since the CPU is not executing instructions, the only exits from any of the Idle modes are by interrupt, WDT time-out or a Reset. When a wake event occurs, CPU execution is delayed by an interval of TcsD (parameter 38, Table 21-10) while it becomes ready to execute code. When the CPU begins executing code, it resumes with the same clock source for the current Idle mode. For example, when waking from RC_IDLE mode, the internal oscillator will clock the CPU and peripherals (in other words, RC_RUN mode). The IDLEN and SCS bits are not affected by the wake-up.

While in any Idle mode or Sleep mode, a WDT time-out will result in a WDT wake-up to the Run mode currently specified by the SCS1:SCS0 bits.

FIGURE 3-5: TRANSITION TIMING FOR ENTRY TO SLEEP MODE

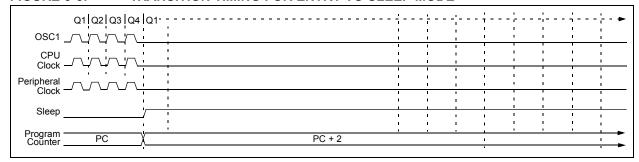
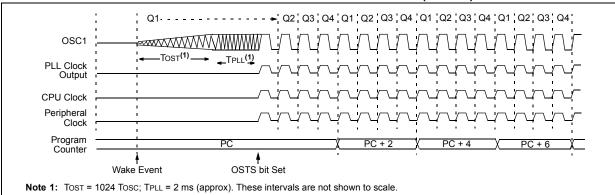


FIGURE 3-6: TRANSITION TIMING FOR WAKE FROM SLEEP (HSPLL)



PIC18F2450/4450

3.4.1 PRI IDLE MODE

This mode is unique among the three low-power Idle modes in that it does not disable the primary device clock. For timing sensitive applications, this allows for the fastest resumption of device operation, with its more accurate primary clock source, since the clock source does not have to "warm up" or transition from another oscillator.

PRI_IDLE mode is entered from PRI_RUN mode by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then clear the SCS bits and execute SLEEP. Although the CPU is disabled, the peripherals continue to be clocked from the primary clock source specified by the FOSC3:FOSC0 Configuration bits. The OSTS bit remains set (see Figure 3-7).

When a wake event occurs, the CPU is clocked from the primary clock source. A delay of interval TCSD is required between the wake event and when code execution starts. This is required to allow the CPU to become ready to execute instructions. After the wake-up, the OSTS bit remains set. The IDLEN and SCS bits are not affected by the wake-up (see Figure 3-8).

3.4.2 SEC IDLE MODE

In SEC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the Timer1 oscillator. This mode is entered from SEC_RUN by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then set SCS1:SCS0 to '01' and execute SLEEP. When the clock source is switched to the Timer1 oscillator, the primary oscillator is shut down, the OSTS bit is cleared and the T1RUN bit is set.

When a wake event occurs, the peripherals continue to be clocked from the Timer1 oscillator. After an interval of TCSD following the wake event, the CPU begins executing code being clocked by the Timer1 oscillator. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run (see Figure 3-8).

Note: The Timer1 oscillator should already be running prior to entering SEC_IDLE mode. If the T1OSCEN bit is not set when the SLEEP instruction is executed, the SLEEP instruction will be ignored and entry to SEC_IDLE mode will not occur. If the Timer1 oscillator is enabled but not yet running, peripheral clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.



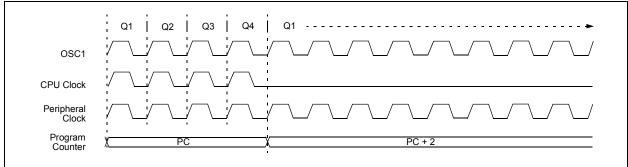
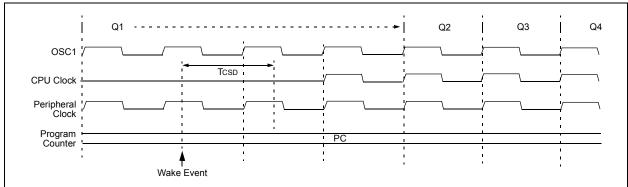


FIGURE 3-8: TRANSITION TIMING FOR WAKE FROM IDLE TO RUN MODE



3.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator, INTRC. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute SLEEP. Although its value is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. When the clock source is switched to the INTRC, the primary oscillator is shut down and the OSTS bit is cleared.

When a wake event occurs, the peripherals continue to be clocked from the INTRC. After a delay of TcsD following the wake event, the CPU begins executing code being clocked by the INTRC. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

3.5 Exiting Idle and Sleep Modes

An exit from Sleep mode or any of the Idle modes is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes (see Section 3.2 "Run Modes", Section 3.3 "Sleep Mode" and Section 3.4 "Idle Modes").

3.5.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode, or the Sleep mode, to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCON or PIE registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see **Section 8.0 "Interrupts"**).

A fixed delay of interval, TCSD, following the wake event, is required when leaving Sleep and Idle modes. This delay is required for the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

3.5.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is in when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see Section 3.2 "Run Modes" and Section 3.3 "Sleep Mode"). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see Section 18.2 "Watchdog Timer (WDT)").

3.5.3 EXIT BY RESET

Normally, the device is held in Reset by the Oscillator Start-up Timer (OST) until the primary clock becomes ready. At that time, the OSTS bit is set and the device begins executing code.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up and the type of oscillator if the new clock source is the primary clock. Exit delays are summarized in Table 3-2.

Code execution can begin before the primary clock becomes ready. If either the Two-Speed Start-up (see Section 18.3 "Two-Speed Start-up") or Fail-Safe Clock Monitor (see Section 18.4 "Fail-Safe Clock Monitor") is enabled, the device may begin execution as soon as the Reset source has cleared. Execution is clocked by the INTRC driven by the internal oscillator. Execution is clocked by the internal oscillator until either the primary clock becomes ready or a power-managed mode is entered before the primary clock becomes ready; the primary clock is then shut down.

3.5.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. There are two cases:

- PRI_IDLE mode, where the primary clock source is not stopped; and
- The primary clock source is not any of the XT or HS modes

In these instances, the primary clock source either does not require an oscillator start-up delay, since it is already running (PRI_IDLE), or normally does not require an oscillator start-up delay (EC and any internal oscillator modes). However, a fixed delay of interval TCSD following the wake event is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

TABLE 3-2: EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Microcontroller	Clock Source	Evit Dalay	Clock Ready Status
Before Wake-up	After Wake-up	Exit Delay	Bit (OSCCON)
	XT, HS		
Primary Device Clock	XTPLL, HSPLL	None	OSTS
(PRI_IDLE mode)	EC	INOTIC	0313
	INTRC ⁽¹⁾		
	XT, HS	Tost ⁽³⁾	
T1OSC or INTRC ⁽¹⁾	XTPLL, HSPLL	Tost + t _{rc} (3)	OSTS
TIOSC OF INTROV	EC	TCSD ⁽²⁾	0313
	INTRC ⁽¹⁾	Tiobst ⁽⁴⁾	
	XT, HS	Tost ⁽³⁾	
INTRC ⁽¹⁾	XTPLL, HSPLL	Tost + t _{rc} (3)	OSTS
INTRO: 7	EC	TCSD ⁽²⁾	0313
	INTRC ⁽¹⁾	None	
	XT, HS	Tost ⁽³⁾	
None	XTPLL, HSPLL	Tost + t _{rc} (3)	OSTS
(Sleep mode)	EC	TCSD ⁽²⁾	0313
	INTRC ⁽¹⁾	Tiobst ⁽⁴⁾	

- Note 1: In this instance, refers specifically to the 31 kHz INTRC clock source.
 - 2: TCSD (parameter 38, Table 21-10) is a required delay when waking from Sleep and all Idle modes and runs concurrently with any other required delays (see **Section 3.4 "Idle Modes"**).
 - 3: Tost is the Oscillator Start-up Timer period (parameter 32, Table 21-10). t_{rc} is the PLL lock time-out (parameter F12, Table 21-7); it is also designated as TPLL.
 - 4: Execution continues during TIOBST (parameter 39, Table 21-10), the INTRC stabilization period.

4.0 RESET

The PIC18F2450/4450 devices differentiate between various kinds of Reset:

- Power-on Reset (POR)
- MCLR Reset during normal operation
- MCLR Reset during power-managed modes
- Watchdog Timer (WDT) Reset (during execution)
- Programmable Brown-out Reset (BOR)
- **RESET Instruction**
- Stack Full Reset
- h) Stack Underflow Reset

This section discusses Resets generated by MCLR. POR and BOR, and covers the operation of the various start-up timers. Stack Reset events are covered in Section 5.1.2.4 "Stack Full and Underflow Resets". WDT Resets are covered in Section 18.2 "Watchdog Timer (WDT)".

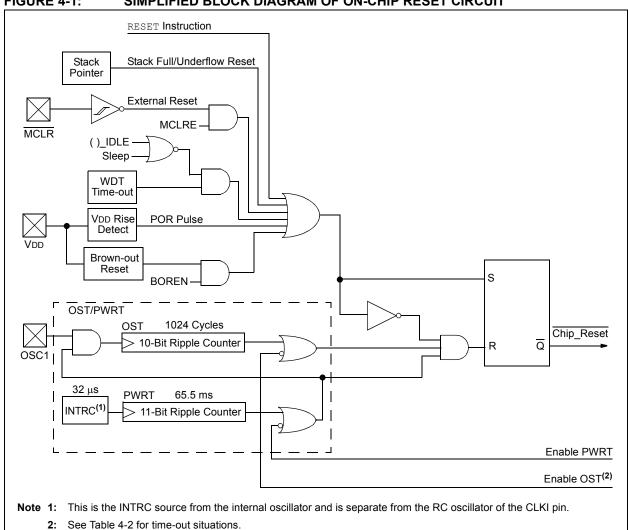
A simplified block diagram of the on-chip Reset circuit is shown in Figure 4-1.

4.1 **RCON Register**

Device Reset events are tracked through the RCON register (Register 4-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in Section 4.6 "Reset State of Registers".

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in Section 8.0 "Interrupts". BOR is covered in Section 4.4 "Brown-out Reset (BOR)".

FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



REGISTER 4-1: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1 ⁽¹⁾	U-0	R/W-1	R-1	R-1	R/W-0 ⁽²⁾	R/W-0
IPEN	SBOREN	_	RI	TO	PD	POR	BOR
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 IPEN: Interrupt Priority Enable bit

1 = Enable priority levels on interrupts

0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6 SBOREN: BOR Software Enable bit (1)

If BOREN1:BOREN0 = 01:

1 = BOR is enabled

0 = BOR is disabled

If BOREN1:BOREN0 = 00, 10 or 11:

Bit is disabled and read as '0'.

bit 5 **Unimplemented:** Read as '0'

bit 4 RI: RESET Instruction Flag bit

1 = The RESET instruction was not executed (set by firmware only)

 ${\tt 0}$ = The RESET instruction was executed causing a device Reset (must be set in software after a

Brown-out Reset occurs)

bit 3 **TO:** Watchdog Time-out Flag bit

1 = Set by power-up, CLRWDT instruction or SLEEP instruction

0 = A WDT time-out occurred

bit 2 PD: Power-Down Detection Flag bit

1 = Set by power-up or by the CLRWDT instruction

0 = Set by execution of the SLEEP instruction

bit 1 **POR:** Power-on Reset Status bit⁽²⁾

1 = A Power-on Reset has not occurred (set by firmware only)

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR**: Brown-out Reset Status bit

1 = A Brown-out Reset has not occurred (set by firmware only)

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: If SBOREN is enabled, its Reset state is '1'; otherwise, it is '0'.

2: The actual Reset value of POR is determined by the type of device Reset. See the notes following this register and Section 4.6 "Reset State of Registers" for additional information.

Note 1: It is recommended that the POR bit be set after a Power-on Reset has been detected so that subsequent Power-on Resets may be detected.

2: Brown-out Reset is said to have occurred when $\overline{\mathsf{BOR}}$ is '0' and $\overline{\mathsf{POR}}$ is '1' (assuming that $\overline{\mathsf{POR}}$ was set to '1' by software immediately after a Power-on Rest).

4.2 Master Clear Reset (MCLR)

The MCLR pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the MCLR Reset path which detects and ignores small pulses.

The MCLR pin is not driven low by any internal Resets, including the WDT.

In PIC18F2450/4450 devices, the MCLR input can be disabled with the MCLRE Configuration bit. When MCLR is disabled, the pin becomes a digital input. See Section 9.5 "PORTE, TRISE and LATE Registers" for more information.

4.3 Power-on Reset (POR)

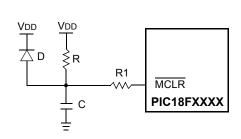
A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the \overline{MCLR} pin through a resistor (1 k Ω to 10 k Ω) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004, **Section269 "DC Characteristics"**). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the POR bit (RCON<1>). The state of the bit is set to '0' whenever a Power-on Reset occurs; it does not change for any other Reset event. POR is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any Power-on Reset.

FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
 - 2: $R < 40 \text{ k}\Omega$ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.
 - 3: $R1 \ge 1$ k Ω will limit any current flowing into \overline{MCLR} from external capacitor C, in the event of \overline{MCLR} /VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

4.4 Brown-out Reset (BOR)

PIC18F2450/4450 devices implement a BOR circuit that provides the user with a number of configuration and power-saving options. The BOR is controlled by the BORV1:BORV0 and BOREN1:BOREN0 Configuration bits. There are a total of four BOR configurations which are summarized in Table 4-1.

The BOR threshold is set by the BORV1:BORV0 bits. If BOR is enabled (any values of BOREN1:BOREN0 except '00'), any drop of VDD below VBOR (parameter D005, **Section 269 "DC Characteristics: Supply Voltage"**) for greater than TBOR (parameter 35, Table 21-10) will reset the device. A Reset may or may not occur if VDD falls below VBOR for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR.

If the Power-up Timer is enabled, it will be invoked after VDD rises above VBOR; it then will keep the chip in Reset for an additional time delay, TPWRT (parameter 33, Table 21-10). If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above VBOR, the Power-up Timer will execute the additional time delay.

BOR and the Power-on Timer (PWRT) are independently configured. Enabling BOR Reset does not automatically enable the PWRT.

4.4.1 SOFTWARE ENABLED BOR

When BOREN1:BOREN0 = 01, the BOR can be enabled or disabled by the user in software. This is done with the control bit, SBOREN (RCON<6>). Setting SBOREN enables the BOR to function as previously described. Clearing SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise, it is read as '0'.

Placing the BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to change BOR configuration. It also allows the user to tailor device power consumption in software by eliminating the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note: Even when BOR is under software control, the BOR Reset voltage level is still set by the BORV1:BORV0 Configuration bits. It cannot be changed in software.

4.4.2 DETECTING BOR

When Brown-out Reset is enabled, the BOR bit always resets to '0' on any Brown-out Reset or Power-on Reset event. This makes it difficult to determine if a Brown-out Reset event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR bit is reset to '1' in software immediately after any Power-on Reset event. IF BOR is '0' while POR is '1', it can be reliably assumed that a Brown-out Reset event has occurred.

4.4.3 DISABLING BOR IN SLEEP MODE

When BOREN1:BOREN0 = 10, the BOR remains under hardware control and operates as previously described. Whenever the device enters Sleep mode, however, the BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

TABLE 4-1: BOR CONFIGURATIONS

BOR Con	Configuration Status of		
BOREN1	BOREN0	SBOREN (RCON<6>)	BOR Operation
0	0	Unavailable	BOR disabled; must be enabled by reprogramming the Configuration bits.
0	1	Available	BOR enabled in software; operation controlled by SBOREN.
1	0	Unavailable	BOR enabled in hardware in Run and Idle modes, disabled during Sleep mode.
1	1	Unavailable	BOR enabled in hardware; must be disabled by reprogramming the Configuration bits.

4.5 Device Reset Timers

PIC18F2450/4450 devices incorporate three separate on-chip timers that help regulate the Power-on Reset process. Their main function is to ensure that the device clock is stable before code is executed. These timers are:

- Power-up Timer (PWRT)
- · Oscillator Start-up Timer (OST)
- · PLL Lock Time-out

4.5.1 POWER-UP TIMER (PWRT)

The Power-up Timer (PWRT) of the PIC18F2450/4450 devices is an 11-bit counter which uses the INTRC source as the clock input. This yields an approximate time interval of 2048 x 32 μ s = 65.6 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC clock and will vary from chip to chip due to temperature and process variation. See DC parameter 33 (Table 21-10) for details.

The PWRT is enabled by clearing the $\overline{\text{PWRTEN}}$ Configuration bit.

4.5.2 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (parameter 33, Table 21-10). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, HS and HSPLL modes and only on Power-on Reset or on exit from most power-managed modes.

4.5.3 PLL LOCK TIME-OUT

With the PLL enabled in its PLL mode, the time-out sequence following a Power-on Reset is slightly different from other oscillator modes. A separate timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL lock time-out (TPLL) is typically 2 ms and follows the oscillator start-up time-out.

4.5.4 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- After the POR condition has cleared, PWRT time-out is invoked (if enabled).
- 2. Then, the OST is activated.

The total time-out will vary based on oscillator configuration and the status of the PWRT. Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7 all depict time-out sequences on power-up, with the Power-up Timer enabled and the device operating in HS Oscillator mode. Figure 4-3 through Figure 4-6 also apply to devices operating in XT mode. For devices in RC mode and with the PWRT disabled, on the other hand, there will be no time-out at all.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, all time-outs will expire. Bringing MCLR high will begin execution immediately (Figure 4-5). This is useful for testing purposes or to synchronize more than one PIC18FXXXX device operating in parallel.

TABLE 4-2: TIME-OUT IN VARIOUS SITUATIONS

Oscillator	Power-up ⁽²⁾ a	Exit from		
Configuration	PWRTEN = 0	PWRTEN = 1	Power-Managed Mode	
HS, XT	66 ms ⁽¹⁾ + 1024 Tosc	1024 Tosc	1024 Tosc	
HSPLL, XTPLL	66 ms ⁽¹⁾ + 1024 Tosc + 2 ms ⁽²⁾	1024 Tosc + 2 ms ⁽²⁾	1024 Tosc + 2 ms ⁽²⁾	
EC, ECIO	66 ms ⁽¹⁾	_	_	
ECPLL, ECPIO	66 ms ⁽¹⁾ + 2 ms ⁽²⁾	2 ms ⁽²⁾	2 ms ⁽²⁾	
INTIO, INTCKO	66 ms ⁽¹⁾	_	_	
INTHS, INTXT	66 ms ⁽¹⁾ + 1024 Tosc	1024 Tosc	1024 Tosc	

Note 1: 66 ms (65.5 ms) is the nominal Power-up Timer (PWRT) delay.

2: 2 ms is the nominal time required for the PLL to lock.

FIGURE 4-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD, VDD RISE < TPWRT)

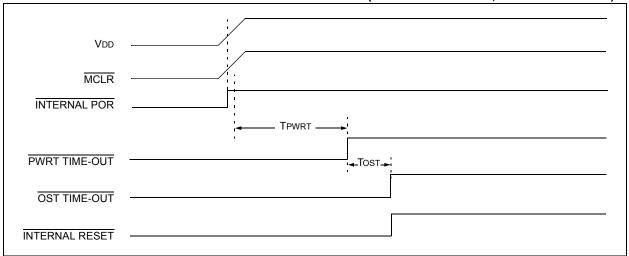


FIGURE 4-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

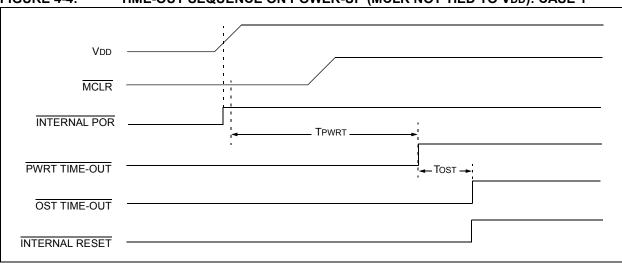
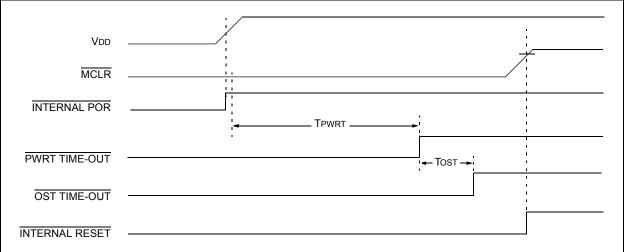
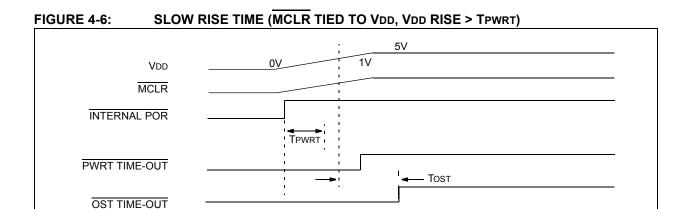
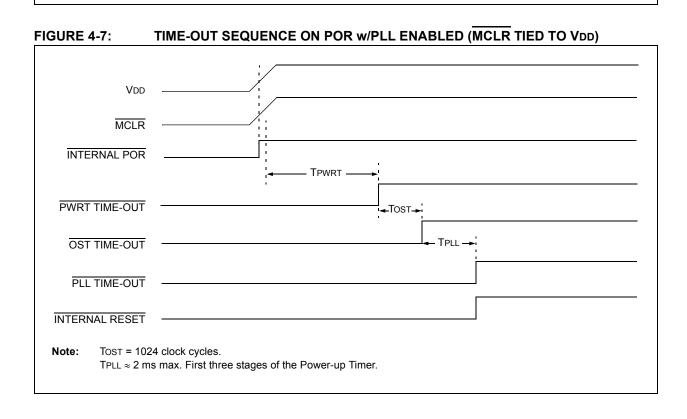


FIGURE 4-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2







INTERNAL RESET

4.6 Reset State of Registers

Most registers are unaffected by a Reset. Their status is unknown on POR and unchanged by all other Resets. The other registers are forced to a "Reset state" depending on the type of Reset that occurred.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, RI, TO, PD,

POR and BOR, are set or cleared differently in different Reset situations as indicated in Table 4-3. These bits are used in software to determine the nature of the Reset.

Table 4-4 describes the Reset states for all of the Special Function Registers. These are categorized by Power-on and Brown-out Resets, Master Clear and WDT Resets and WDT wake-ups.

TABLE 4-3: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program	RCON Register						STKPTR Register	
Condition	Counter	SBOREN	RI	то	PD	POR	BOR	STKFUL	STKUNF
Power-on Reset	0000h	1	1	1	1	0	0	0	0
RESET instruction	0000h	u (2)	0	u	u	u	u	u	u
Brown-out Reset	0000h	ս (2)	1	1	1	u	0	u	u
MCLR Reset during power-managed Run modes	0000h	u (2)	u	1	u	u	u	u	u
MCLR Reset during power-managed Idle modes and Sleep mode	0000h	ս (2)	u	1	0	u	u	u	u
WDT time-out during full-power or power-managed Run modes	0000h	u (2)	u	0	u	u	u	u	u
MCLR Reset during full-power execution	0000h	ս (2)	u	u	u	u	u	u	u
Stack Full Reset (STVREN = 1)	0000h	ս (2)	u	u	u	u	u	1	u
Stack Underflow Reset (STVREN = 1)	0000h	u (2)	u	u	u	u	u	u	1
Stack Underflow Error (not an actual Reset, STVREN = 0)	0000h	u (2)	u	u	u	u	u	u	1
WDT time-out during power-managed Idle or Sleep modes	PC + 2	ս (2)	u	0	0	u	u	u	u
Interrupt exit from power-managed modes	PC + 2 ⁽¹⁾	լ (2)	u	u	0	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bit is set, the PC is loaded with the interrupt vector (008h or 0018h).

2: Reset state is '1' for POR and unchanged for all other Resets when software BOR is enabled (BOREN1:BOREN0 Configuration bits = 01 and SBOREN = 1); otherwise, the Reset state is '0'.

TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	egister Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
TOSU	2450	4450	0 0000	0 0000	0 uuuu (1)
TOSH	2450	4450	0000 0000	0000 0000	uuuu uuuu ⁽¹⁾
TOSL	2450	4450	0000 0000	0000 0000	uuuu uuuu(1)
STKPTR	2450	4450	00-0 0000	uu-0 0000	uu-u uuuu ⁽¹⁾
PCLATU	2450	4450	0 0000	0 0000	u uuuu
PCLATH	2450	4450	0000 0000	0000 0000	uuuu uuuu
PCL	2450	4450	0000 0000	0000 0000	PC + 2 ⁽³⁾
TBLPTRU	2450	4450	00 0000	00 0000	uu uuuu
TBLPTRH	2450	4450	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	2450	4450	0000 0000	0000 0000	uuuu uuuu
TABLAT	2450	4450	0000 0000	0000 0000	uuuu uuuu
PRODH	2450	4450	XXXX XXXX	uuuu uuuu	uuuu uuuu
PRODL	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	2450	4450	0000 000x	0000 000u	uuuu uuuu ⁽²⁾
INTCON2	2450	4450	1111 -1-1	1111 -1-1	uuuu -u-u ⁽²⁾
INTCON3	2450	4450	11-0 0-00	11-0 0-00	uu-u u-uu ⁽²⁾
INDF0	2450	4450	N/A	N/A	N/A
POSTINC0	2450	4450	N/A	N/A	N/A
POSTDEC0	2450	4450	N/A	N/A	N/A
PREINC0	2450	4450	N/A	N/A	N/A
PLUSW0	2450	4450	N/A	N/A	N/A
FSR0H	2450	4450	0000	0000	uuuu
FSR0L	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	2450	4450	N/A	N/A	N/A
POSTINC1	2450	4450	N/A	N/A	N/A
POSTDEC1	2450	4450	N/A	N/A	N/A
PREINC1	2450	4450	N/A	N/A	N/A
PLUSW1	2450	4450	N/A	N/A	N/A
FSR1H	2450	4450	0000	0000	uuuu
FSR1L	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	2450	4450	0000	0000	uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

- **Note 1:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 2: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - **3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - **4:** See Table 4-3 for Reset value for specific condition.
 - **5:** PORTA<6>, LATA<6> and TRISA<6> are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

PIC18F2450/4450

TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable	e Devices	Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt	
INDF2	2450	4450	N/A	N/A	N/A	
POSTINC2	2450	4450	N/A	N/A	N/A	
POSTDEC2	2450	4450	N/A	N/A	N/A	
PREINC2	2450	4450	N/A	N/A	N/A	
PLUSW2	2450	4450	N/A	N/A	N/A	
FSR2H	2450	4450	0000	0000	uuuu	
FSR2L	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu	
STATUS	2450	4450	x xxxx	u uuuu	u uuuu	
TMR0H	2450	4450	0000 0000	0000 0000	uuuu uuuu	
TMR0L	2450	4450	XXXX XXXX	uuuu uuuu	uuuu uuuu	
T0CON	2450	4450	1111 1111	1111 1111	uuuu uuuu	
OSCCON	2450	4450	0 q-00	0 0-q0	u u-qu	
HLVDCON	2450	4450	0-00 0101	0-00 0101	u-uu uuuu	
WDTCON	2450	4450	0	0	u	
RCON ⁽⁴⁾	2450	4450	0q-1 11q0	0q-q qquu	uq-u qquu	
TMR1H	2450	4450	XXXX XXXX	uuuu uuuu	uuuu uuuu	
TMR1L	2450	4450	XXXX XXXX	uuuu uuuu	uuuu uuuu	
T1CON	2450	4450	0000 0000	u0uu uuuu	uuuu uuuu	
TMR2	2450	4450	0000 0000	0000 0000	uuuu uuuu	
PR2	2450	4450	1111 1111	1111 1111	1111 1111	
T2CON	2450	4450	-000 0000	-000 0000	-uuu uuuu	
ADRESH	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu	
ADRESL	2450	4450	XXXX XXXX	uuuu uuuu	uuuu uuuu	
ADCON0	2450	4450	00 0000	00 0000	uu uuuu	
ADCON1	2450	4450	00 qqqq	00 qqqq	uu uuuu	
ADCON2	2450	4450	0-00 0000	0-00 0000	u-uu uuuu	
CCPR1H	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu	
CCPR1L	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu	
CCP1CON	2450	4450	00 0000	00 0000	uu uuuu	
BAUDCON	2450	4450	01-0 0-00	01-0 0-00	uu-u u-uu	
SPBRG	2450	4450	0000 0000	0000 0000	uuuu uuuu	
RCREG	2450	4450	0000 0000	0000 0000	uuuu uuuu	

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', <math>q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

- **Note 1:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 2: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - **3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - 4: See Table 4-3 for Reset value for specific condition.
 - **5:** PORTA<6>, LATA<6> and TRISA<6> are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
TXREG	2450	4450	0000 0000	0000 0000	uuuu uuuu
TXSTA	2450	4450	0000 0010	0000 0010	uuuu uuuu
RCSTA	2450	4450	0000 000x	0000 000x	uuuu uuuu
EECON2	2450	4450	0000 0000	0000 0000	0000 0000
EECON1	2450	4450	-x-0 x00-	-u-0 u00-	-u-0 u00-
IPIR2	2450	4450	1-11	1-11	u-uu
PIR2	2450	4450	0-00	0-00	u-uu (2)
PIE2	2450	4450	0-00	0-00	u-uu
IPR1	2450	4450	-111 -111	-111 -111	-uuu -uuu
PIR1	2450	4450	-000 -000	-000 -000	-uuu -uuu (2)
PIE1	2450	4450	-000 -000	-000 -000	-uuu -uuu
TRISE	2450	4450	111	111	uuu
TRISD	2450	4450	1111 1111	1111 1111	uuuu uuuu
TRISC	2450	4450	11111	11111	uuuuu
TRISB	2450	4450	1111 1111	1111 1111	uuuu uuuu
TRISA ⁽⁵⁾	2450	4450	-111 1111 (5)	-111 1111 (5)	-uuu uuuu(5)
LATE	2450	4450	xxx	uuu	uuu
LATD	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATC	2450	4450	xxxxx	uuuuu	uuuuu
LATB	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATA ⁽⁵⁾	2450	4450	-xxx xxxx(5)	-uuu uuuu(5)	-uuu uuuu(5)
PORTE	2450	4450	x000	x000	uuuu
PORTD	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	2450	4450	xxxx -xxx	uuuu -uuu	uuuu -uuu
PORTB	2450	4450	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA ⁽⁵⁾	2450	4450	-x0x 0000 (5)	-u0u 0000 (5)	-uuu uuuu ⁽⁵⁾
UEP15	2450	4450	0 0000	0 0000	u uuuu
UEP14	2450	4450	0 0000	0 0000	u uuuu
UEP13	2450	4450	0 0000	0 0000	u uuuu
UEP12	2450	4450	0 0000	0 0000	u uuuu
UEP11	2450	4450	0 0000	0 0000	u uuuu
UEP10	2450	4450	0 0000	0 0000	u uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

- **Note 1:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 2: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - **3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - 4: See Table 4-3 for Reset value for specific condition.
 - **5:** PORTA<6>, LATA<6> and TRISA<6> are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

PIC18F2450/4450

TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicabl		Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
UEP9	2450	4450	0 0000	0 0000	u uuuu
UEP8	2450	4450	0 0000	0 0000	u uuuu
UEP7	2450	4450	0 0000	0 0000	u uuuu
UEP6	2450	4450	0 0000	0 0000	u uuuu
UEP5	2450	4450	0 0000	0 0000	u uuuu
UEP4	2450	4450	0 0000	0 0000	u uuuu
UEP3	2450	4450	0 0000	0 0000	u uuuu
UEP2	2450	4450	0 0000	0 0000	u uuuu
UEP1	2450	4450	0 0000	0 0000	u uuuu
UEP0	2450	4450	0 0000	0 0000	u uuuu
UCFG	2450	4450	00-0 0000	00-0 0000	uu-u uuuu
UADDR	2450	4450	-000 0000	-000 0000	-uuu uuuu
UCON	2450	4450	-0x0 000-	-0x0 000-	-uuu uuu-
USTAT	2450	4450	-xxx xxx-	-xxx xxx-	-uuu uuu-
UEIE	2450	4450	00 0000	00 0000	uu uuuu
UEIR	2450	4450	00 0000	00 0000	uu uuuu
UIE	2450	4450	-000 0000	-000 0000	-uuu uuuu
UIR	2450	4450	-000 0000	-000 0000	-uuu uuuu
UFRMH	2450	4450	XXX	xxx	uuu
UFRML	2450	4450	XXXX XXXX	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

- **Note 1:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 2: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - 3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - **4:** See Table 4-3 for Reset value for specific condition.
 - **5:** PORTA<6>, LATA<6> and TRISA<6> are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

5.0 MEMORY ORGANIZATION

There are two types of memory in PIC18F2450/4450 microcontroller devices:

- Program Memory
- · Data RAM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 "Flash Program Memory"**.

5.1 Program Memory Organization

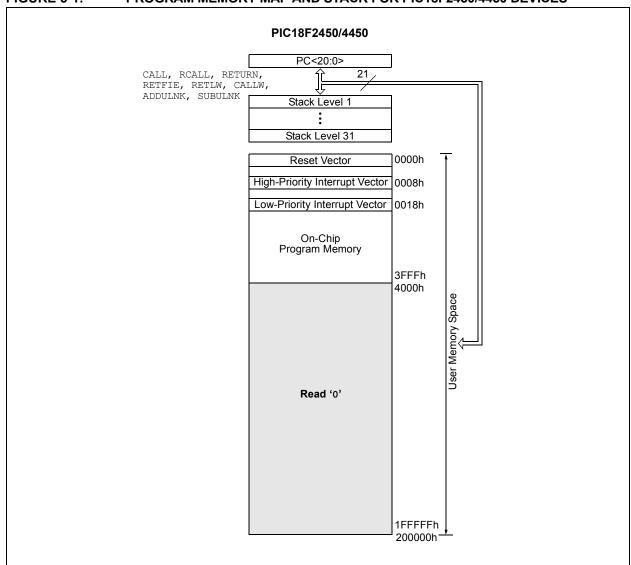
PIC18 microcontrollers implement a 21-bit program counter which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

The PIC18F2450 and PIC18F4450 each have 16 Kbytes of Flash memory and can store up to 8192 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for PIC18F2450 and PIC18F4450 devices are shown in Figure 5-1.

FIGURE 5-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F2450/4450 DEVICES



5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see Section 5.1.4.1 "Computed GOTO").

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

The CALL, RCALL and GOTO program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN. RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack Special Function Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack. The Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack. The contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full, has overflowed or has underflowed.

5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

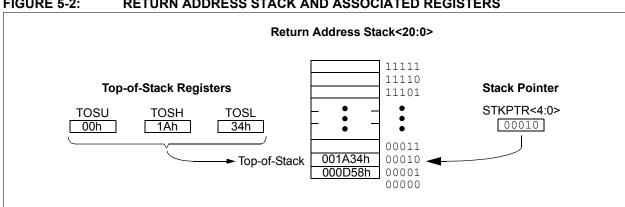


FIGURE 5-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS

5.1.2.2 Return Stack Pointer (STKPTR)

The STKPTR register (Register 5-1) contains the Stack Pointer value, the STKFUL (Stack Full) status bit and the STKUNF (Stack Underflow) status bit. The value of the Stack Pointer can be 0 through 31. The Stack Pointer increments before values are pushed onto the stack and decrements after values are popped off the stack. On Reset, the Stack Pointer value will be zero. The user may read and write the Stack Pointer value. This feature can be used by a Real-Time Operating System (RTOS) for return stack maintenance.

After the PC is pushed onto the stack 31 times (without popping any values off the stack), the STKFUL bit is set. The STKFUL bit is cleared by software or by a POR.

The action that takes place when the stack becomes full depends on the state of the STVREN (Stack Overflow Reset Enable) Configuration bit. (Refer to Section 18.1 "Configuration Bits" for a description of the device Configuration bits.) If STVREN is set (default), the 31st push will push the (PC + 2) value onto the stack, set the STKFUL bit and reset the device. The STKFUL bit will remain set and the Stack Pointer will be set to zero.

If STVREN is cleared, the STKFUL bit will be set on the 31st push and the Stack Pointer will increment to 31. Any additional pushes will not overwrite the 31st push and the STKPTR will remain at 31.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and sets the STKUNF bit, while the Stack Pointer remains at zero. The STKUNF bit will remain set until cleared by software or until a POR occurs.

Note: Returning a value of zero to the PC on an underflow has the effect of vectoring the program to the Reset vector, where the stack conditions can be verified and appropriate actions can be taken. This is not the same as a Reset, as the contents of the SFRs are not affected.

5.1.2.3 PUSH and POP Instructions

Since the Top-of-Stack is readable and writable, the ability to push values onto the stack and pull values off the stack, without disturbing normal program execution, is a desirable feature. The PIC18 instruction set includes two instructions, PUSH and POP, that permit the TOS to be manipulated under software control. TOSU, TOSH and TOSL can be modified to place data or a return address on the stack.

The PUSH instruction places the current PC value onto the stack. This increments the Stack Pointer and loads the current PC value onto the stack.

The POP instruction discards the current TOS by decrementing the Stack Pointer. The previous value pushed onto the stack then becomes the TOS value.

REGISTER 5-1: STKPTR: STACK POINTER REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL ⁽¹⁾	STKUNF ⁽¹⁾	_	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **STKFUL:** Stack Full Flag bit⁽¹⁾

1 = Stack became full or overflowed

0 = Stack has not become full or overflowed

bit 6 STKUNF: Stack Underflow Flag bit⁽¹⁾

1 = Stack underflow occurred0 = Stack underflow did not occur

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SP4:SP0:** Stack Pointer Location bits

Note 1: Bit 7 and bit 6 are cleared by user software or by a POR.

5.1.2.4 Stack Full and Underflow Resets

Device Resets on stack overflow and stack underflow conditions are enabled by setting the STVREN bit in Configuration Register 4L. When STVREN is set, a full or underflow condition will set the appropriate STKFUL or STKUNF bit and then cause a device Reset. When STVREN is cleared, a full or underflow condition will set the appropriate STKFUL or STKUNF bit but not cause a device Reset. The STKFUL or STKUNF bits are cleared by user software or a Power-on Reset.

5.1.3 FAST REGISTER STACK

A Fast Register Stack is provided for the STATUS, WREG and BSR registers to provide a "fast return" option for interrupts. Each stack is only one level deep and is neither readable nor writable. It is loaded with the current value of the corresponding register when the processor vectors for an interrupt. All interrupt sources will push values into the stack registers. The values in the registers are then loaded back into their associated registers if the RETFIE, FAST instruction is used to return from the interrupt.

If both low and high-priority interrupts are enabled, the stack registers cannot be used reliably to return from low-priority interrupts. If a high-priority interrupt occurs while servicing a low-priority interrupt, the stack register values stored by the low-priority interrupt will be overwritten. In these cases, users must save the key registers in software during a low-priority interrupt.

If interrupt priority is not used, all interrupts may use the Fast Register Stack for returns from interrupt. If no interrupts are used, the Fast Register Stack can be used to restore the STATUS, WREG and BSR registers at the end of a subroutine call. To use the Fast Register Stack for a subroutine call, a CALL label, FAST instruction must be executed to save the STATUS, WREG and BSR registers to the Fast Register Stack. A RETURN, FAST instruction is then executed to restore these registers from the Fast Register Stack.

Example 5-1 shows a source code example that uses the Fast Register Stack during a subroutine call and return.

EXAMPLE 5-1: FAST REGISTER STACK CODE EXAMPLE

CALL	SUB1, FAST	;STATUS, WREG, BSR ;SAVED IN FAST REGISTER ;STACK
SUB1	• RETURN, FAST	;RESTORE VALUES SAVED ;IN FAST REGISTER STACK

5.1.4 LOOK-UP TABLES IN PROGRAM MEMORY

There may be programming situations that require the creation of data structures, or look-up tables, in program memory. For PIC18 devices, look-up tables can be implemented in two ways:

- Computed GOTO
- · Table Reads

5.1.4.1 Computed GOTO

A computed GOTO is accomplished by adding an offset to the program counter. An example is shown in Example 5-2.

A look-up table can be formed with an ADDWF PCL instruction and a group of RETLW $\,\mathrm{nn}$ instructions. The W register is loaded with an offset into the table before executing a call to that table. The first instruction of the called routine is the ADDWF PCL instruction. The next instruction executed will be one of the RETLW $\,\mathrm{nn}$ instructions that returns the value ' $\,\mathrm{nn}$ ' to the calling function.

The offset value (in WREG) specifies the number of bytes that the program counter should advance and should be multiples of 2 (LSb = 0).

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

EXAMPLE 5-2: COMPUTED GOTO USING AN OFFSET VALUE

	MOVF	OFFSET,	\overline{W}
	CALL	TABLE	
ORG	nn00h		
TABLE	ADDWF	PCL	
	RETLW	nnh	
	RETLW	nnh	
	RETLW	nnh	
	•		
	•		

5.1.4.2 Table Reads and Table Writes

A better method of storing data in program memory allows two bytes of data to be stored in each instruction location.

Look-up table data may be stored two bytes per program word by using table reads and writes. The Table Pointer (TBLPTR) register specifies the byte address and the Table Latch (TABLAT) register contains the data that is read from or written to program memory. Data is transferred to or from program memory one byte at a time.

Table read and table write operations are discussed further in Section 6.1 "Table Reads and Table Writes".

5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

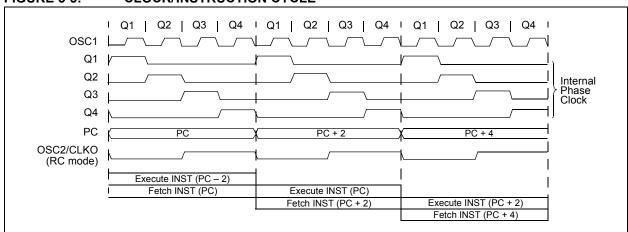
5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).

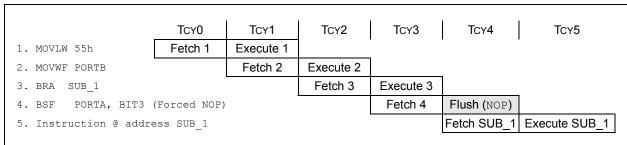
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).





EXAMPLE 5-3: INSTRUCTION PIPELINE FLOW



Note: All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

5.2.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSb = 0). To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSb will always read '0' (see Section 5.1.1 "Program Counter").

Figure 5-4 shows an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 5-4 shows how the instruction, GOTO 0006h, is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. Section 19.0 "Instruction Set Summary" provides further details of the instruction set.

FIGURE 5-4: INSTRUCTIONS IN PROGRAM MEMORY

100KE 5-4.	11101110	0110110	IN PROGRAM	I IVIEIVIOI (I		
				LSB = 1	LSB = 0	Word Address ↓
		Program M				000000h
		Byte Locat	ions \rightarrow			000002h
						000004h
						000006h
	Instruction 1:	MOVLW	055h	0Fh	55h	000008h
	Instruction 2:	GOTO	0006h	EFh	03h	00000Ah
				F0h	00h	00000Ch
	Instruction 3:	MOVFF	123h, 456h	C1h	23h	00000Eh
				F4h	56h	000010h
						000012h
						000014h

5.2.4 TWO-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LSFR. In all cases, the second word of the instructions always has '1111' as its four Most Significant bits; the other 12 bits are literal data, usually a data memory address.

The use of '1111' in the 4 MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence, immediately after the first word, the data in the second word is accessed and

used by the instruction sequence. If the first word is skipped for some reason and the second word is executed by itself, a ${\tt NOP}$ is executed instead. This is necessary for cases when the two-word instruction is preceded by a conditional instruction that changes the PC. Example 5-4 shows how this works.

Note: See Section 5.5 "Program Memory and the Extended Instruction Set" for information on two-word instruction in the extended instruction set.

EXAMPLE 5-4: TWO-WORD INSTRUCTIONS

CASE 1:		
Object Code	Source Code	
0110 0110 0000 0000	TSTFSZ REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF REG1, REG2	; No, skip this word
1111 0100 0101 0110		; Execute this word as a NOP
0010 0100 0000 0000	ADDWF REG3	; continue code
CASE 2:		
Object Code	Source Code	
0110 0110 0000 0000	TSTFSZ REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF REG1, REG2	; Yes, execute this word
1111 0100 0101 0110		; 2nd word of instruction
0010 0100 0000 0000	ADDWF REG3	; continue code

5.3 Data Memory Organization

Note:

The operation of some aspects of data memory are changed when the PIC18 extended instruction set is enabled. See Section 5.6 "Data Memory and the Extended Instruction Set" for more information.

The data memory in PIC18 devices is implemented as static RAM. Each register in the data memory has a 12-bit address, allowing up to 4096 bytes of data memory. The memory space is divided into as many as 16 banks that contain 256 bytes each. PIC18F2450/4450 devices implement three complete banks, for a total of 768 bytes. Figure 5-5 shows the data memory organization for the devices.

The data memory contains Special Function Registers (SFRs) and General Purpose Registers (GPRs). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratchpad operations in the user's application. Any read of an unimplemented location will read as '0's.

The instruction set and architecture allow operations across all banks. The entire data memory may be accessed by Direct, Indirect or Indexed Addressing modes. Addressing modes are discussed later in this subsection.

To ensure that commonly used registers (SFRs and select GPRs) can be accessed in a single cycle, PIC18 devices implement an Access Bank. This is a 256-byte memory space that provides fast access to SFRs and the lower portion of GPR Bank 0 without using the BSR. **Section 5.3.3 "Access Bank"** provides a detailed description of the Access RAM.

5.3.1 USB RAM

Bank 4 of the data memory is actually mapped to special dual port RAM. When the USB module is disabled, the GPRs in these banks are used like any other GPR in the data memory space.

When the USB module is enabled, the memory in this bank is allocated as buffer RAM for USB operation. This area is shared between the microcontroller core and the USB Serial Interface Engine (SIE) and is used to transfer data directly between the two.

It is theoretically possible to use this area of USB RAM that is not allocated as USB buffers for normal scratch-pad memory or other variable storage. In practice, the dynamic nature of buffer allocation makes this risky at best. Bank 4 is also used for USB buffer management when the module is enabled and should not be used for any other purposes during that time.

Additional information on USB RAM and buffer operation is provided in **Section 14.0 "Universal Serial Bus (USB)"**.

5.3.2 BANK SELECT REGISTER (BSR)

Large areas of data memory require an efficient addressing scheme to make rapid access to any address possible. Ideally, this means that an entire address does not need to be provided for each read or write operation. For PIC18 devices, this is accomplished with a RAM banking scheme. This divides the memory space into 16 contiguous banks of 256 bytes. Depending on the instruction, each location can be addressed directly by its full 12-bit address, or an 8-bit low-order address and a 4-bit Bank Pointer.

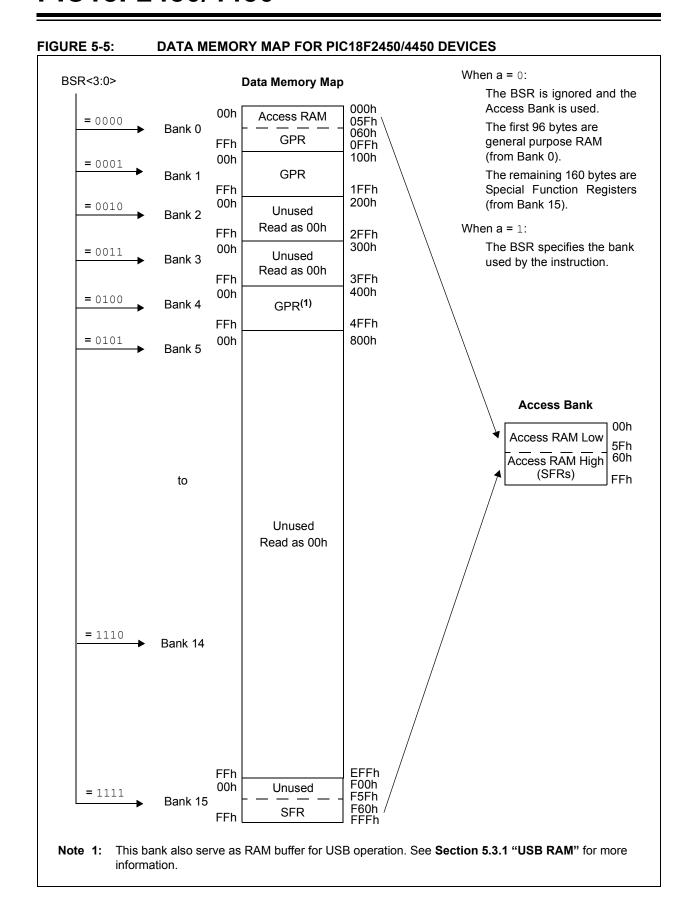
Most instructions in the PIC18 instruction set make use of the Bank Pointer, known as the Bank Select Register (BSR). This SFR holds the 4 Most Significant bits of a location's address; the instruction itself includes the 8 Least Significant bits. Only the four lower bits of the BSR are implemented (BSR3:BSR0). The upper four bits are unused; they will always read '0' and cannot be written to. The BSR can be loaded directly by using the MOVLB instruction.

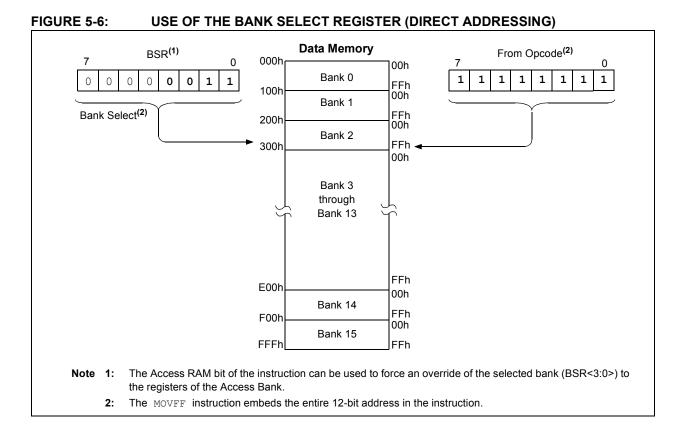
The value of the BSR indicates the bank in data memory. The eight bits in the instruction show the location in the bank and can be thought of as an offset from the bank's lower boundary. The relationship between the BSR's value and the bank division in data memory is shown in Figure 5-6.

Since up to 16 registers may share the same low-order address, the user must always be careful to ensure that the proper bank is selected before performing a data read or write. For example, writing what should be program data to an 8-bit address of F9h, while the BSR is 0Fh, will end up resetting the program counter.

While any bank can be selected, only those banks that are actually implemented can be read or written to. Writes to unimplemented banks are ignored, while reads from unimplemented banks will return '0's. Even so, the STATUS register will still be affected as if the operation was successful. The data memory map in Figure 5-6 indicates which banks are implemented.

In the core PIC18 instruction set, only the <code>MOVFF</code> instruction fully specifies the 12-bit address of the source and target registers. This instruction ignores the BSR completely when it executes. All other instructions include only the low-order address as an operand and must use either the BSR or the Access Bank to locate their target registers.





5.3.3 ACCESS BANK

While the use of the BSR, with an embedded 8-bit address, allows users to address the entire range of data memory, it also means that the user must always ensure that the correct bank is selected. Otherwise, data may be read from or written to the wrong location. This can be disastrous if a GPR is the intended target of an operation but an SFR is written to instead. Verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (00h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Block 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 5-5).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '1', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '0',

however, the instruction is forced to use the Access Bank address map; the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = 1). This is discussed in more detail in Section 5.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode".

5.3.4 GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

5.3.5 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM in the data memory space. SFRs start at the top of data memory and extend downward to occupy the top segment of Bank 15, from F60h to FFFh. A list of these registers is given in Table 5-1 and Table 5-2.

The SFRs can be classified into two sets: those associated with the "core" device functionality (ALU, Resets and interrupts) and those related to the

peripheral functions. The Reset and interrupt registers are described in their respective chapters, while the ALU's STATUS register is described later in this section. Registers related to the operation of a peripheral feature are described in the chapter for that peripheral.

The SFRs are typically distributed among the peripherals whose functions they control. Unused SFR locations are unimplemented and read as '0's.

TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2450/4450 DEVICES

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2 ⁽¹⁾	FBFh	CCPR1H	F9Fh	IPR1	F7Fh	UEP15
FFEh	TOSH	FDEh	POSTINC2 ⁽¹⁾	FBEh	CCPR1L	F9Eh	PIR1	F7Eh	UEP14
FFDh	TOSL	FDDh	POSTDEC2 ⁽¹⁾	FBDh	CCP1CON	F9Dh	PIE1	F7Dh	UEP13
FFCh	STKPTR	FDCh	PREINC2 ⁽¹⁾	FBCh	(2)	F9Ch	(2)	F7Ch	UEP12
FFBh	PCLATU	FDBh	PLUSW2 ⁽¹⁾	FBBh	(2)	F9Bh	(2)	F7Bh	UEP11
FFAh	PCLATH	FDAh	FSR2H	FBAh	(2)	F9Ah	(2)	F7Ah	UEP10
FF9h	PCL	FD9h	FSR2L	FB9h	(2)	F99h	(2)	F79h	UEP9
FF8h	TBLPTRU	FD8h	STATUS	FB8h	BAUDCON	F98h	(2)	F78h	UEP8
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	(2)	F97h	(2)	F77h	UEP7
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	(2)	F96h	TRISE ⁽³⁾	F76h	UEP6
FF5h	TABLAT	FD5h	T0CON	FB5h	(2)	F95h	TRISD ⁽³⁾	F75h	UEP5
FF4h	PRODH	FD4h	(2)	FB4h	(2)	F94h	TRISC	F74h	UEP4
FF3h	PRODL	FD3h	OSCCON	FB3h	(2)	F93h	TRISB	F73h	UEP3
FF2h	INTCON	FD2h	HLVDCON	FB2h	(2)	F92h	TRISA	F72h	UEP2
FF1h	INTCON2	FD1h	WDTCON	FB1h	(2)	F91h	(2)	F71h	UEP1
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	(2)	F70h	UEP0
FEFh	INDF0 ⁽¹⁾	FCFh	TMR1H	FAFh	SPBRG	F8Fh	(2)	F6Fh	UCFG
l.	POSTINC0 ⁽¹⁾	FCEh	TMR1L	FAEh	RCREG	F8Eh	(2)	F6Eh	UADDR
FEDh	POSTDEC0 ⁽¹⁾	FCDh	T1CON	FADh	TXREG	F8Dh	LATE ⁽³⁾	F6Dh	UCON
FECh	PREINC0 ⁽¹⁾	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD ⁽³⁾	F6Ch	USTAT
FEBh	PLUSW0 ⁽¹⁾	FCBh	PR2	FABh	RCSTA	F8Bh	LATC	F6Bh	UEIE
FEAh	FSR0H	FCAh	T2CON	FAAh	(2)	F8Ah	LATB	F6Ah	UEIR
FE9h	FSR0L	FC9h	(2)	FA9h	(2)	F89h	LATA	F69h	UIE
FE8h	WREG	FC8h	(2)	FA8h	(2)	F88h	(2)	F68h	UIR
FE7h	INDF1 ⁽¹⁾	FC7h	(2)	FA7h	EECON2 ⁽¹⁾	F87h	(2)	F67h	UFRMH
l.	POSTINC1 ⁽¹⁾	FC6h	(2)	FA6h	EECON1	F86h	(2)	F66h	UFRML
FE5h	POSTDEC1 ⁽¹⁾	FC5h	(2)	FA5h	(2)	F85h	(2)	F65h	(2)
FE4h	PREINC1 ⁽¹⁾	FC4h	ADRESH	FA4h	(2)	F84h	PORTE	F64h	(2)
FE3h	PLUSW1 ⁽¹⁾	FC3h	ADRESL	FA3h	(2)	F83h	PORTD ⁽³⁾	F63h	(2)
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC	F62h	(2)
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB	F61h	(2)
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA	F60h	(2)

Note 1: Not a physical register.

- 2: Unimplemented registers are read as '0'.
- 3: These registers are implemented only on 40/44-pin devices.

TABLE 5-2: REGISTER FILE SUMMARY (PIC18F2450/4450)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on Page:
TOSU	_	_	_	Top-of-Stack	Upper Byte (T	OS<20:16>)			0 0000	49, 54
TOSH	Top-of-Stack	High Byte (TO	S<15:8>)	•					0000 0000	49, 54
TOSL	Top-of-Stack	Low Byte (TO	S<7:0>)						0000 0000	49, 54
STKPTR	STKFUL	STKUNF	_	SP4	SP3	SP2	SP1	SP0	00-0 0000	49, 55
PCLATU	_	_	_	Holding Regis	ster for PC<20	:16>			0 0000	49, 54
PCLATH	Holding Regis	ster for PC<15	:8>						0000 0000	49, 54
PCL	PC Low Byte	(PC<7:0>)							0000 0000	49, 54
TBLPTRU	— bit 21 ⁽¹⁾ Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)									49, 76
TBLPTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)									49, 76
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)									49, 76
TABLAT	Program Men	nory Table Lat	ch						0000 0000	49, 76
PRODH	Product Regis	ster High Byte							xxxx xxxx	49, 83
PRODL	Product Regis	ster Low Byte							xxxx xxxx	49, 83
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	49, 87
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	_	RBIP	1111 -1-1	49, 88
INTCON3	INT2IP	INT1IP	_	INT2IE	INT1IE	_	INT2IF	INT1IF	11-0 0-00	49, 89
INDF0	Uses contents		ddress data m	nemory – value	<u> </u>	changed (not a	a physical regi	ster)	N/A	49, 68
POSTINC0				nemory – value					N/A	49, 69
POSTDEC0				nemory – value					N/A	49, 69
PREINC0				•	•				N/A	49, 69
PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) – value of FSR0 offset by W								N/A	49, 69
FSR0H	_	_	_	_	Indirect Data	Memory Addre	ess Pointer 0 H	High Byte	0000	49, 68
FSR0L	Indirect Data	Memory Addre	ess Pointer 0 L	ow Byte	•				xxxx xxxx	49, 68
WREG	Working Regi	ster							xxxx xxxx	49,
INDF1	Uses contents	s of FSR1 to a	ddress data m	nemory – value	of FSR1 not	changed (not a	a physical regi	ster)	N/A	49, 68
POSTINC1	Uses contents	s of FSR1 to a	ddress data m	nemory – value	of FSR1 post	-incremented	(not a physica	l register)	N/A	49, 69
POSTDEC1	Uses contents	s of FSR1 to a	ddress data m	nemory – value	of FSR1 post	-decremented	(not a physica	al register)	N/A	49, 69
PREINC1	Uses contents	s of FSR1 to a	ddress data m	nemory – value	of FSR1 pre-	incremented (not a physical	register)	N/A	49, 69
PLUSW1	Uses contents value of FSR		ddress data m	nemory – value	e of FSR1 pre-	incremented (not a physical	register) –	N/A	49, 69
FSR1H	_	_	_	_	Indirect Data	Memory Addre	ess Pointer 1 h	High Byte	0000	49, 68
FSR1L	Indirect Data	Memory Addre	ess Pointer 1 L	ow Byte					xxxx xxxx	49, 68
BSR	_	_	_	_	Bank Select F	Register			0000	49, 59
INDF2	Uses contents	s of FSR2 to a	ddress data m	nemory – value	of FSR2 not	changed (not a	a physical regi	ster)	N/A	50, 68
POSTINC2	Uses contents	s of FSR2 to a	ddress data m	nemory – value	of FSR2 post	-incremented	(not a physica	l register)	N/A	50, 69
POSTDEC2				nemory – value					N/A	50, 69
PREINC2	Uses contents	s of FSR2 to a	ddress data m	nemory – value	of FSR2 pre-	incremented (not a physical	register)	N/A	50, 69
PLUSW2	Uses contents		ddress data m	nemory – value	of FSR2 pre-	incremented (not a physical	register) –	N/A	50, 69
FSR2H	_	_	_	_	Indirect Data	Memory Addre	ess Pointer 2 l	High Byte	0000	50, 68
FSR2L	Indirect Data	Memory Addre	ess Pointer 2 L	ow Byte	•				xxxx xxxx	50, 68
STATUS	_	_	_	N	OV	Z	DC	С	x xxxx	50, 66
TMR0H	Timer0 Regis	ter High Byte							0000 0000	50, 113
TMR0L	Timer0 Regis								xxxx xxxx	50, 113
TOCON	TMR00N	T08BIT	TOCS	T0SE	PSA	T0PS2	T0PS1	T0PS0	1111 1111	50, 111
	l		l	l	alue denends	l	l	l	1	l

 $\textbf{Legend:} \qquad \textbf{x} = \textbf{unknown}, \ \textbf{u} = \textbf{unchanged}, \ \textbf{-= unimplemented}, \ \textbf{q} = \textbf{value depends on condition}. \ \textbf{Shaded cells are unimplemented}, \ \textbf{read as '0'}.$

Note 1: Bit 21 of the TBLPTRU allows access to the device Configuration bits.

- 2: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.
- 3: These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '-'.
- 4: RA6 is configured as a port pin based on various primary oscillator modes. When the port pin is disabled, all of the associated bits read '0'.
- 5: RE3 is only available as a port pin when the MCLRE Configuration bit is clear; otherwise, the bit reads as '0'.
- **6:** RC5 and RC4 are only available as port pins when the USB module is disabled (UCON<3> = 0).

TABLE 5-2: REGISTER FILE SUMMARY (PIC18F2450/4450) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on Page:
OSCCON	IDLEN	_	_	_	OSTS	_	SCS1	SCS0	0 q-00	50, 31
HLVDCON	VDIRMAG	_	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0-00 0101	50, 185
WDTCON	_	_	_	_	_	_	_	SWDTEN	0	50, 204
RCON	IPEN	SBOREN ⁽²⁾	_	RI	TO	PD	POR	BOR	0q-1 11q0	50, 42
TMR1H	Timer1 Regis			I			ı		xxxx xxxx	50, 120
TMR1L	Timer1 Regis	ter Low Byte							xxxx xxxx	50, 120
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	0000 0000	50, 115
TMR2	Timer2 Regis	ter					1		0000 0000	50, 122
PR2	Timer2 Period	d Register							1111 1111	50, 122
T2CON	_	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	50, 121
ADRESH	A/D Result Re	egister High B	yte	I			I		xxxx xxxx	50, 184
ADRESL	A/D Result Re	egister Low By	rte						xxxx xxxx	50, 184
ADCON0	_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	00 0000	50, 175
ADCON1	_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	00 qqqq	50, 176
ADCON2	ADFM	_	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	0-00 0000	50, 177
CCPR1H		pare/PWM Re	l .						xxxx xxxx	50, 124
CCPR1L	†	pare/PWM Re							xxxx xxxx	50, 124
CCP1CON	_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	50, 123,
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	01-0 0-00	51, 156,
SPBRGH	-	ıd Rate Gener	ator Register l						0000 0000	50, 157
SPBRG	1	ıd Rate Gener							0000 0000	50, 157
RCREG	-	ceive Register	J	, , , , ,					0000 0000	50, 165
TXREG	ł	nsmit Register							0000 0000	51, 163
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	51, 154
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	51, 155
EECON2	Data Memory	Control Regis	ster 2 (not a pl	nysical register	.)		ı		0000 0000	51, 74
EECON1	_	CFGS		FREE	WRERR	WREN	WR	_	-x-0 x00-	51, 75
IPR2	OSCFIP	_	USBIP	_	_	HLVDIP	_	_	1-11	51, 95
PIR2	OSCFIF	_	USBIF	_	_	HLVDIF	_	_	0-00	51, 91
PIE2	OSCFIE	_	USBIE	_	_	HLVDIE	_	_	0-00	51, 93
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	-111 -111	51, 94
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	-000 -000	51, 90
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	-000 -000	51, 92
TRISE ⁽³⁾	_	_	_	_	_	TRISE2	TRISE1	TRISE0	111	51, 110
TRISD ⁽³⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	51, 108
TRISC	TRISC7	TRISC6	_	_	_	TRISC2	TRISC1	TRISC0	11111	51, 106
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	51, 103
TRISA	_	TRISA6 ⁽⁴⁾	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	-111 1111	51, 100
LATE ⁽³⁾	_	_	_	_	_	LATE2	LATE1	LATE0	xxx	51, 110
LATD ⁽³⁾	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx xxxx	51, 108
LATC	LATC7	LATC6	_	_	_	LATC2	LATC1	LATC0	xxxxx	51, 106
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx xxxx	51, 103
LATA	_	LATA6 ⁽⁴⁾	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	-xxx xxxx	51, 100
PORTE	_	_	_	_	RE3 ⁽⁵⁾	RE2 ⁽³⁾	RE1 ⁽³⁾	RE0 ⁽³⁾	x000	51, 109
PORTD ⁽³⁾	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	51, 108
<u> </u>	x = unknown,		l		l		L		1	

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

Note 1: Bit 21 of the TBLPTRU allows access to the device Configuration bits.

- 2: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.
- 3: These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '-'.
- RA6 is configured as a port pin based on various primary oscillator modes. When the port pin is disabled, all of the associated bits read '0'.
- 5: RE3 is only available as a port pin when the MCLRE Configuration bit is clear; otherwise, the bit reads as '0'.
- 6: RC5 and RC4 are only available as port pins when the USB module is disabled (UCON<3> = 0).

TABLE 5-2: REGISTER FILE SUMMARY (PIC18F2450/4450) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on Page:
PORTC	RC7	RC6	RC5 ⁽⁶⁾	RC4 ⁽⁶⁾	_	RC2	RC1	RC0	xxxx -xxx	51, 106
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	51, 100
PORTA	_	RA6 ⁽⁴⁾	RA5	RA4	RA3	RA2	RA1	RA0	-x0x 0000	51, 100
UEP15	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	51, 135
UEP14	ı	-	ı	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	51, 135
UEP13	ı	-	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	51, 135
UEP12			-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	51, 135
UEP11	ı	-	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	51, 135
UEP10	ı	-	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	51, 135
UEP9	ı	-	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP8	ı	-	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP7	ı	-	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP6	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP5			-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP4			-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP3	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP2	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP1	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UEP0	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	0 0000	52, 135
UCFG	UTEYE	UOEMON	_	UPUEN	UTRDIS	FSEN	PPB1	PPB0	00-0 0000	52, 132
UADDR	_	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	-000 0000	52, 136
UCON	ı	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	_	-0x0 000-	52, 130
USTAT	-	ENDP3	ENDP2	ENDP1	ENDP0	DIR	PPBI	_	-xxx xxx-	52, 134
UEIE	BTSEE	_	-	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	00 0000	52, 148
UEIR	BTSEF	-	-	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	00 0000	52, 147
UIE	_	SOFIE	STALLIE	IDLEIE	TRNIE	ACTVIE	UERRIE	URSTIE	-000 0000	52, 146
UIR	_	SOFIF	STALLIF	IDLEIF	TRNIF	ACTVIF	UERRIF	URSTIF	-000 0000	52, 144
UFRMH	_		_	_	_	FRM10	FRM9	FRM8	xxx	52, 136
UFRML	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0	xxxx xxxx	52, 136

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

Note 1: Bit 21 of the TBLPTRU allows access to the device Configuration bits.

- 2: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.
- 3: These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '-'.
- 4: RA6 is configured as a port pin based on various primary oscillator modes. When the port pin is disabled, all of the associated bits read '0'.
- 5: RE3 is only available as a port pin when the MCLRE Configuration bit is clear; otherwise, the bit reads as '0'.
- 6: RC5 and RC4 are only available as port pins when the USB module is disabled (UCON<3> = 0).

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5.3.6 STATUS REGISTER

The STATUS register, shown in Register 5-2, contains the arithmetic status of the ALU. As with any other SFR, it can be the operand for any instruction.

If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the results of the instruction are not written; instead, the STATUS register is updated according to the instruction performed. Therefore, the result of an instruction with the STATUS register as its destination may be different than intended. As an example, CLRF STATUS will set the Z bit and leave the remaining Status bits unchanged ('000u u1uu').

It is recommended that only BCF, BSF, SWAPF, MOVFF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions that do not affect Status bits, see the instruction set summaries in Table 19-2 and Table 19-3.

Note: The <u>C</u> and <u>DC</u> bits operate as the Borrow and Digit Borrow bits, respectively, in subtraction.

REGISTER 5-2: STATUS REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_	N	OV	Z	DC ⁽¹⁾	C ⁽²⁾
bit 7							bit 0

e	_	_	-	ᆈ	
е	u	e	п	(1	

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **N:** Negative bit

This bit is used for signed arithmetic (2's complement). It indicates whether the result was negative (ALU MSB = 1).

1 = Result was negative

0 = Result was positive

bit 3 **OV:** Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude which causes the sign bit (bit 7 of the result) to change state.

1 = Overflow occurred for signed arithmetic (in this arithmetic operation)

0 = No overflow occurred

bit 2 Z: Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/Borrow bit⁽¹⁾

For ADDWF, ADDLW, SUBLW and SUBWF instructions:

1 = A carry-out from the 4th low-order bit of the result occurred

0 = No carry-out from the 4th low-order bit of the result

bit 0 C: Carry/Borrow bit⁽²⁾

For ADDWF, ADDLW, SUBLW and SUBWF instructions:

1 = A carry-out from the Most Significant bit of the result occurred

0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For borrow, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either bit 4 or bit 3 of the source register.

2: For borrow, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low-order bit of the source register.

5.4 Data Addressing Modes

Note:

The execution of some instructions in the core PIC18 instruction set are changed when the PIC18 extended instruction set is enabled. See Section 5.6 "Data Memory and the Extended Instruction Set" for more information.

While the program memory can be addressed in only one way – through the program counter – information in the data memory space can be addressed in several ways. For most instructions, the addressing mode is fixed. Other instructions may use up to three modes, depending on which operands are used and whether or not the extended instruction set is enabled.

The addressing modes are:

- Inherent
- Literal
- · Direct
- · Indirect

An additional addressing mode, Indexed Literal Offset, is available when the extended instruction set is enabled (XINST Configuration bit = 1). Its operation is discussed in greater detail in **Section 5.6.1 "Indexed Addressing with Literal Offset"**.

5.4.1 INHERENT AND LITERAL ADDRESSING

Many PIC18 control instructions do not need any argument at all; they either perform an operation that globally affects the device or they operate implicitly on one register. This addressing mode is known as Inherent Addressing. Examples include SLEEP, RESET and DAW.

Other instructions work in a similar way but require an additional explicit argument in the opcode. This is known as Literal Addressing mode because they require some literal value as an argument. Examples include ADDLW and MOVLW, which respectively, add or move a literal value to the W register. Other examples include CALL and GOTO, which include a 20-bit program memory address.

5.4.2 DIRECT ADDRESSING

Direct Addressing mode specifies all or part of the source and/or destination address of the operation within the opcode itself. The options are specified by the arguments accompanying the instruction.

In the core PIC18 instruction set, bit-oriented and byteoriented instructions use some version of Direct Addressing by default. All of these instructions include some 8-bit literal address as their Least Significant Byte. This address specifies either a register address in one of the banks of data RAM (Section 5.3.4 "General Purpose Register File") or a location in the Access Bank (Section 5.3.3 "Access Bank") as the data source for the instruction.

The Access RAM bit 'a' determines how the address is interpreted. When 'a' is '1', the contents of the BSR (Section 5.3.2 "Bank Select Register (BSR)") are used with the address to determine the complete 12-bit address of the register. When 'a' is '0', the address is interpreted as being a register in the Access Bank. Addressing that uses the Access RAM is sometimes also known as Direct Forced Addressing mode.

A few instructions, such as MOVFF, include the entire 12-bit address (either source or destination) in their opcodes. In these cases, the BSR is ignored entirely.

The destination of the operation's results is determined by the destination bit 'd'. When 'd' is '1', the results are stored back in the source register, overwriting its original contents. When 'd' is '0', the results are stored in the W register. Instructions without the 'd' argument have a destination that is implicit in the instruction; their destination is either the target register being operated on or the W register.

5.4.3 INDIRECT ADDRESSING

Indirect Addressing allows the user to access a location in data memory without giving a fixed address in the instruction. This is done by using File Select Registers (FSRs) as pointers to the locations to be read or written to. Since the FSRs are themselves located in RAM as Special Function Registers, they can also be directly manipulated under program control. This makes FSRs very useful in implementing data structures, such as tables and arrays in data memory.

The registers for Indirect Addressing are also implemented with Indirect File Operands (INDFs) that permit automatic manipulation of the pointer value with auto-incrementing, auto-decrementing or offsetting with another value. This allows for efficient code, using loops, such as the example of clearing an entire RAM bank in Example 5-5.

EXAMPLE 5-5: HOW TO CLEAR RAM (BANK 1) USING INDIRECT ADDRESSING

```
LFSR
              FSR0, 100h ;
NEXT
              POSTINCO
                          ; Clear INDF
       CLRF
                          ; register then
                          ; inc pointer
       BTFSS FSR0H, 1
                          ; All done with
                          ; Bank1?
       BRA
              NEXT
                          ; NO, clear next
CONTINUE
                          ; YES, continue
```

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5.4.3.1 FSR Registers and the INDF Operand

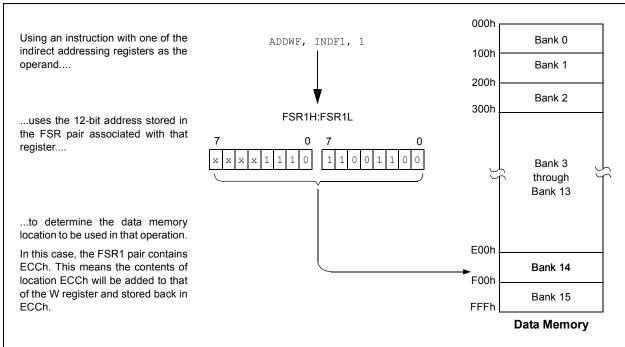
At the core of Indirect Addressing are three sets of registers: FSR0, FSR1 and FSR2. Each represents a pair of 8-bit registers: FSRnH and FSRnL. The four upper bits of the FSRnH register are not used, so each FSR pair holds a 12-bit value. This represents a value that can address the entire range of the data memory in a linear fashion. The FSR register pairs, then, serve as pointers to data memory locations.

Indirect Addressing is accomplished with a set of Indirect File Operands, INDF0 through INDF2. These can be thought of as "virtual" registers; they are

mapped in the SFR space but are not physically implemented. Reading or writing to a particular INDF register actually accesses its corresponding FSR register pair. A read from INDF1, for example, reads the data at the address indicated by FSR1H:FSR1L. Instructions that use the INDF registers as operands actually use the contents of their corresponding FSR as a pointer to the instruction's target. The INDF operand is just a convenient way of using the pointer.

Because Indirect Addressing uses a full 12-bit address, data RAM banking is not necessary. Thus, the current contents of the BSR and the Access RAM bit have no effect on determining the target address.

FIGURE 5-7: INDIRECT ADDRESSING



5.4.3.2 FSR Registers and POSTINC, POSTDEC, PREINC and PLUSW

In addition to the INDF operand, each FSR register pair also has four additional indirect operands. Like INDF, these are "virtual" registers that cannot be indirectly read or written to. Accessing these registers actually accesses the associated FSR register pair, but also performs a specific action on it stored value. They are:

- POSTDEC: accesses the FSR value, then automatically decrements it by '1' afterwards
- POSTINC: accesses the FSR value, then automatically increments it by '1' afterwards
- PREINC: increments the FSR value by '1', then uses it in the operation
- PLUSW: adds the signed value of the W register (range of -127 to 128) to that of the FSR and uses the new value in the operation.

In this context, accessing an INDF register uses the value in the FSR registers without changing them. Similarly, accessing a PLUSW register gives the FSR value offset by that in the W register; neither value is actually changed in the operation. Accessing the other virtual registers changes the value of the FSR registers.

Operations on the FSRs with POSTDEC, POSTINC and PREINC affect the entire register pair; that is, rollovers of the FSRnL register from FFh to 00h carry over to the FSRnH register. On the other hand, results of these operations do not change the value of any flags in the STATUS register (e.g., Z, N, OV, etc.).

The PLUSW register can be used to implement a form of Indexed Addressing in the data memory space. By manipulating the value in the W register, users can reach addresses that are fixed offsets from pointer addresses. In some applications, this can be used to implement some powerful program control structure, such as software stacks, inside of data memory.

5.4.3.3 Operations by FSRs on FSRs

Indirect Addressing operations that target other FSRs or virtual registers represent special cases. For example, using an FSR to point to one of the virtual registers will not result in successful operations. As a specific case, assume that FSR0H:FSR0L contains FE7h, the address of INDF1. Attempts to read the value of INDF1, using INDF0 as an operand, will return 00h. Attempts to write to INDF1, using INDF0 as the operand, will result in a NOP.

On the other hand, using the virtual registers to write to an FSR pair may not occur as planned. In these cases, the value will be written to the FSR pair but without any incrementing or decrementing. Thus, writing to INDF2 or POSTDEC2 will write the same value to the FSR2H:FSR2L.

Since the FSRs are physical registers mapped in the SFR space, they can be manipulated through all direct operations. Users should proceed cautiously when working on these registers, particularly if their code uses Indirect Addressing.

Similarly, operations by Indirect Addressing are generally permitted on all other SFRs. Users should exercise the appropriate caution that they do not inadvertently change settings that might affect the operation of the device.

5.5 Program Memory and the Extended Instruction Set

The operation of program memory is unaffected by the use of the extended instruction set.

Enabling the extended instruction set adds eight additional two-word commands to the existing PIC18 instruction set: ADDFSR, ADDULNK, CALLW, MOVSF, MOVSS, PUSHL, SUBFSR and SUBULNK. These instructions are executed as described in Section 5.2.4 "Two-Word Instructions".

5.6 Data Memory and the Extended Instruction Set

Enabling the PIC18 extended instruction set (XINST Configuration bit = 1) significantly changes certain aspects of data memory and its addressing. Specifically, the use of the Access Bank for many of the core PIC18 instructions is different. This is due to the introduction of a new addressing mode for the data memory space. This mode also alters the behavior of Indirect Addressing using FSR2 and its associated operands.

What does not change is just as important. The size of the data memory space is unchanged, as well as its linear addressing. The SFR map remains the same. Core PIC18 instructions can still operate in both Direct and Indirect Addressing mode; inherent and literal instructions do not change at all. Indirect Addressing with FSR0 and FSR1 also remains unchanged.

5.6.1 INDEXED ADDRESSING WITH LITERAL OFFSET

Enabling the PIC18 extended instruction set changes the behavior of Indirect Addressing using the FSR2 register pair and its associated file operands. Under the proper conditions, instructions that use the Access Bank – that is, most bit-oriented and byte-oriented instructions – can invoke a form of Indexed Addressing using an offset specified in the instruction. This special addressing mode is known as Indexed Addressing with Literal Offset or Indexed Literal Offset mode.

When using the extended instruction set, this addressing mode requires the following:

- The use of the Access Bank is forced ('a' = 0); and
- The file address argument is less than or equal to 5Fh.

Under these conditions, the file address of the instruction is not interpreted as the lower byte of an address (used with the BSR in Direct Addressing), or as an 8-bit address in the Access Bank. Instead, the value is interpreted as an offset value to an Address Pointer specified by FSR2. The offset and the contents of FSR2 are added to obtain the target address of the operation.

5.6.2 INSTRUCTIONS AFFECTED BY INDEXED LITERAL OFFSET MODE

Any of the core PIC18 instructions that can use Direct Addressing are potentially affected by the Indexed Literal Offset Addressing mode. This includes all byte-oriented and bit-oriented instructions, or almost one-half of the standard PIC18 instruction set. Instructions that only use Inherent or Literal Addressing modes are unaffected.

Additionally, byte-oriented and bit-oriented instructions are not affected if they do not use the Access Bank (Access RAM bit is '1') or include a file address of 60h or above. Instructions meeting these criteria will continue to execute as before. A comparison of the different possible addressing modes when the extended instruction set is enabled in shown in Figure 5-8.

Those who desire to use byte-oriented or bit-oriented instructions in the Indexed Literal Offset mode should note the changes to assembler syntax for this mode. This is described in more detail in **Section 19.2.1** "Extended Instruction Syntax".

FIGURE 5-8: COMPARING ADDRESSING OPTIONS FOR BIT-ORIENTED AND BYTE-ORIENTED INSTRUCTIONS (EXTENDED INSTRUCTION SET ENABLED)

EXAMPLE INSTRUCTION: ADDWF, f, d, a (Opcode: 0010 01da fffff fffff)

When a = 0 and $f \ge 60h$:

The instruction executes in Direct Forced mode. 'f' is interpreted as a location in the Access RAM between 060h and 0FFh. This is the same as the SFRs or locations F60h to 0FFh (Bank 15) of data memory.

Locations below 60h are not available in this addressing mode.

When a = 0 and $f \le 5Fh$:

The instruction executes in Indexed Literal Offset mode. 'f' is interpreted as an offset to the address value in FSR2. The two are added together to obtain the address of the target register for the instruction. The address can be anywhere in the data memory space.

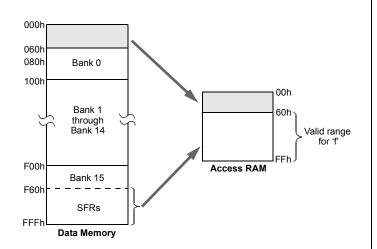
Note that in this mode, the correct syntax is now:

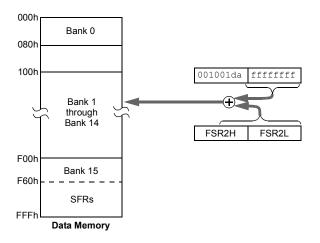
ADDWF [k], d

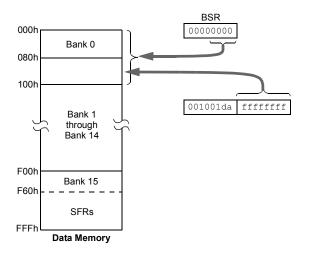
where 'k' is the same as 'f'.

When a = 1 (all values of f):

The instruction executes in Direct mode (also known as Direct Long mode). 'f' is interpreted as a location in one of the 16 banks of the data memory space. The bank is designated by the Bank Select Register (BSR). The address can be in any implemented bank in the data memory space.







5.6.3 MAPPING THE ACCESS BANK IN INDEXED LITERAL OFFSET MODE

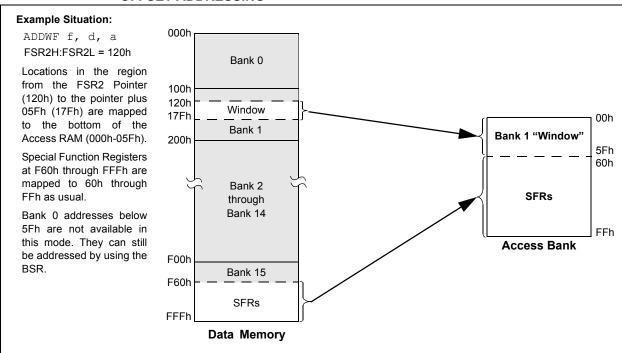
The use of Indexed Literal Offset Addressing mode effectively changes how the lower portion of Access RAM (00h to 5Fh) is mapped. Rather than containing just the contents of the bottom half of Bank 0, this mode maps the contents from Bank 0 and a user-defined "window" that can be located anywhere in the data memory space. The value of FSR2 establishes the lower boundary of the addresses mapped into the window, while the upper boundary is defined by FSR2 plus 95 (5Fh). Addresses in the Access RAM above 5Fh are mapped as previously described (see Section 5.3.3 "Access Bank"). An example of Access Bank remapping in this addressing mode is shown in Figure 5-9.

Remapping of the Access Bank applies *only* to operations using the Indexed Literal Offset mode. Operations that use the BSR (Access RAM bit is '1') will continue to use Direct Addressing as before. Any indirect or indexed operation that explicitly uses any of the indirect file operands (including FSR2) will continue to operate as standard Indirect Addressing. Any instruction that uses the Access Bank, but includes a register address of greater than 05Fh, will use Direct Addressing and the normal Access Bank map.

5.6.4 BSR IN INDEXED LITERAL OFFSET MODE

Although the Access Bank is remapped when the extended instruction set is enabled, the operation of the BSR remains unchanged. Direct Addressing, using the BSR to select the data memory bank, operates in the same manner as previously described.

FIGURE 5-9: REMAPPING THE ACCESS BANK WITH INDEXED LITERAL OFFSET ADDRESSING



6.0 FLASH PROGRAM MEMORY

The Flash program memory is readable, writable and erasable, during normal operation over the entire VDD range.

A read from program memory is executed on one byte at a time. A write to program memory is executed on blocks of 16 bytes at a time. Program memory is erased in blocks of 64 bytes at a time. A Bulk Erase operation may not be issued from user code.

Writing or erasing program memory will cease instruction fetches until the operation is complete. The program memory cannot be accessed during the write or erase, therefore, code cannot execute. An internal programming timer terminates program memory writes and erases.

A value written to program memory does not need to be a valid instruction. Executing a program memory location that forms an invalid instruction results in a NOP.

6.1 **Table Reads and Table Writes**

In order to read and write program memory, there are two operations that allow the processor to move bytes between the program memory space and the data RAM:

- Table Read (TBLRD)
- Table Write (TBLWT)

The program memory space is 16 bits wide, while the data RAM space is 8 bits wide. Table reads and table writes move data between these two memory spaces through an 8-bit register (TABLAT).

Table read operations retrieve data from program memory and place it into the data RAM space. Figure 6-1 shows the operation of a table read with program memory and data RAM.

Table write operations store data from the data memory space into holding registers in program memory. The procedure to write the contents of the holding registers into program memory is detailed in Section 6.5 "Writing to Flash Program Memory". Figure 6-2 shows the operation of a table write with program memory and data RAM.

Table operations work with byte entities. A table block containing data, rather than program instructions, is not required to be word-aligned. Therefore, a table block can start and end at any byte address. If a table write is being used to write executable code into program memory, program instructions will need to be word-aligned.

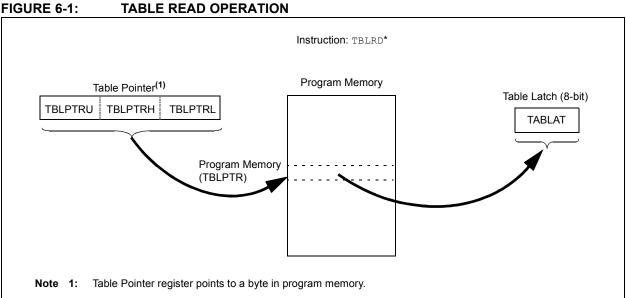
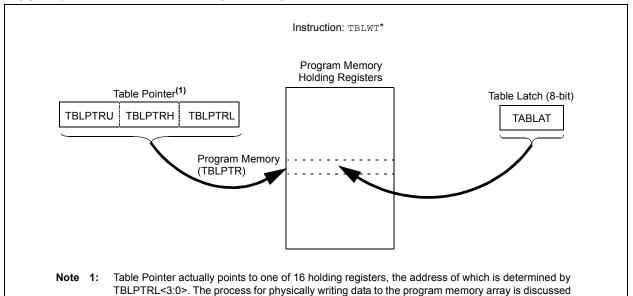


FIGURE 6-2: TABLE WRITE OPERATION



in Section 6.5 "Writing to Flash Program Memory".

6.2 Control Registers

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the:

- EECON1 register
- · EECON2 register
- TABLAT register
- · TBLPTR registers

6.2.1 EECON1 AND EECON2 REGISTERS

The EECON1 register (Register 6-1) is the control register for memory accesses. The EECON2 register is not a physical register; it is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

The CFGS control bit determines if the access will be to the Configuration/Calibration registers or to program memory.

The FREE bit, when set, will allow a program memory erase operation. When FREE is set, the erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WREN bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note: During normal operation, the WRERR is read as '1'. This can indicate that a write operation was prematurely terminated by a Reset or a write operation was attempted improperly.

The WR control bit initiates write operations. The bit cannot be cleared, only set, in software; it is cleared in hardware at the completion of the write operation.

REGISTER 6-1: EECON1: MEMORY CONTROL REGISTER 1

U-0	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	U-0
_	CFGS	_	FREE	WRERR ⁽¹⁾	WREN	WR	_
bit 7							bit 0

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	W = Writable bit U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 Unimplemented: Read as '0'

bit 6 **CFGS:** Flash Program or Configuration Select bit

1 = Access Configuration registers

0 = Access Flash program

bit 5 **Unimplemented:** Read as '0'

bit 4 FREE: Flash Row Erase Enable bit

1 = Erase the program memory row addressed by TBLPTR on the next WR command

(cleared by completion of erase operation)

0 = Perform write-only

bit 3 WRERR: Flash Program Error Flag bit⁽¹⁾

 ${f 1}$ = A write operation is prematurely terminated (any Reset during self-timed programming in normal

operation or an improper write attempt)

0 = The write operation completed

WREN: Flash Program Write Enable bit

1 = Allows write cycles to Flash program

0 = Inhibits write cycles to Flash program

bit 1 WR: Write Control bit

bit 2

1 = Initiates a program memory erase cycle or write cycle

(The operation is self-timed and the bit is cleared by hardware once write is complete.

The WR bit can only be set (not cleared) in software.)

0 = Write cycle complete

bit 0 **Unimplemented:** Read as '0'

Note 1: When a WRERR occurs, the CFGS bit is not cleared. This allows tracing of the error condition.

6.2.2 TABLE LATCH REGISTER (TABLAT)

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch register is used to hold 8-bit data during data transfers between program memory and data RAM.

6.2.3 TABLE POINTER REGISTER (TBLPTR)

The Table Pointer (TBLPTR) register addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low-order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the device ID, the user ID and the Configuration bits.

The Table Pointer, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations are shown in Table 6-1. These operations on the TBLPTR only affect the low-order 21 bits.

6.2.4 TABLE POINTER BOUNDARIES

TBLPTR is used in reads, writes and erases of the Flash program memory.

When a TBLRD is executed, all 22 bits of the TBLPTR determine which byte is read from program memory into TABLAT.

When a TBLWT is executed, the four LSbs of the Table Pointer register (TBLPTR<3:0>) determine which of the 16 program memory holding registers is written to. When the timed write to program memory begins (via the WR bit), the 16 MSbs of the TBLPTR (TBLPTR<21:4>) determine which program memory block of 16 bytes is written to. For more detail, see Section 6.5 "Writing to Flash Program Memory".

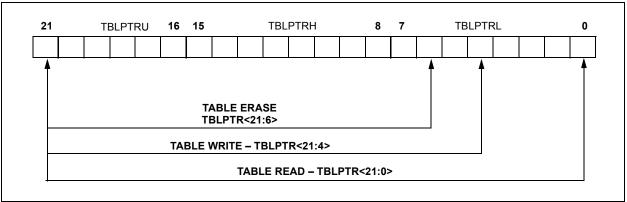
When an erase of program memory is executed, the 16 MSbs of the Table Pointer register (TBLPTR<21:6>) point to the 64-byte block that will be erased. The Least Significant bits (TBLPTR<5:0>) are ignored.

Figure 6-3 describes the relevant boundaries of the TBLPTR based on Flash program memory operations.

TABLE 6-1:	TABLE POINTER	OPERATIONS WITH TBLRD	AND TBLWT INSTRUCTIONS

Example	Operation on Table Pointer
TBLRD* TBLWT*	TBLPTR is not modified
TBLRD*+ TBLWT*+	TBLPTR is incremented after the read/write
TBLRD*- TBLWT*-	TBLPTR is decremented after the read/write
TBLRD+* TBLWT+*	TBLPTR is incremented before the read/write





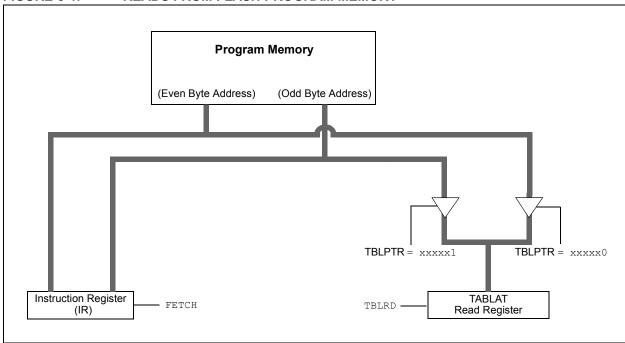
6.3 Reading the Flash Program Memory

The TBLRD instruction is used to retrieve data from program memory and places it into data RAM. Table reads from program memory are performed one byte at a time

TBLPTR points to a byte address in program space. Executing <code>TBLRD</code> places the byte pointed to into TABLAT. In addition, TBLPTR can be modified automatically for the next table read operation.

The internal program memory is typically organized by words. The Least Significant bit of the address selects between the high and low bytes of the word. Figure 6-4 shows the interface between the internal program memory and the TABLAT.

FIGURE 6-4: READS FROM FLASH PROGRAM MEMORY



EXAMPLE 6-1: READING A FLASH PROGRAM MEMORY WORD

	MOVLW MOVWF MOVWF MOVLW MOVWF	CODE_ADDR_UPPER TBLPTRU CODE_ADDR_HIGH TBLPTRH CODE_ADDR_LOW TBLPTRL	; Load TBLPTR with the base ; address of the word
READ_WORD			
	TBLRD*+		; read into TABLAT and increment
	MOVF	TABLAT, W	; get data
	MOVWF	WORD_EVEN	
	TBLRD*+		; read into TABLAT and increment
	MOVF	TABLAT, W	; get data
	MOVF	WORD_ODD	

6.4 Erasing Flash Program Memory

The minimum erase block is 32 words or 64 bytes. Only through the use of an external programmer, or through ICSP control, can larger blocks of program memory be Bulk Erased. Word Erase in the Flash array is not supported.

When initiating an erase sequence from the microcontroller itself, a block of 64 bytes of program memory is erased. The Most Significant 16 bits of the TBLPTR<21:6> point to the block being erased. TBLPTR<5:0> are ignored.

The EECON1 register commands the erase operation. The WREN bit must be set to enable write operations. The FREE bit is set to select an erase operation.

For protection, the write initiate sequence for EECON2 must be used.

A long write is necessary for erasing the internal Flash. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

6.4.1 FLASH PROGRAM MEMORY ERASE SEQUENCE

The sequence of events for erasing a block of internal program memory is:

- Load Table Pointer register with address of row being erased.
- 2. Set the EECON1 register for the erase operation:
 - · clear the CFGS bit to access program memory;
 - · set WREN bit to enable writes;
 - · set FREE bit to enable the erase.
- 3. Disable interrupts.
- 4. Write 55h to EECON2.
- 5. Write 0AAh to EECON2.
- Set the WR bit. This will begin the Row Erase cycle.
- 7. The CPU will stall for duration of the erase (about 2 ms using internal timer).
- 8. Re-enable interrupts.

EXAMPLE 6-2: ERASING A FLASH PROGRAM MEMORY ROW

```
MOVLW CODE ADDR UPPER
                                        ; load TBLPTR with the base
              MOVWF
                     TBLPTRU
                                        ; address of the memory block
              MOVLW CODE ADDR HIGH
              MOVWF
                     TBLPTRH
                     CODE ADDR LOW
              MOVLW
              MOVWF
                     TBLPTRL
   ERASE ROW
                     EECON1, CFGS
              BCF
                                       ; access Flash program memory
              BSF
                     EECON1, WREN
                                       ; enable write to memory
              BSF
                      EECON1, FREE
                                       ; enable Row Erase operation
                      INTCON, GIE
              BCF
                                       ; disable interrupts
Required
              MOVLW 55h
              MOVWF
                      EECON2
                                       ; write 55h
Sequence
              MOVLW
                      0AAh
              MOVWF
                      EECON2
                                        ; write OAAh
              BSF
                      EECON1, WR
                                        ; start erase (CPU stall)
              BSF
                     INTCON, GIE
                                        ; re-enable interrupts
```

6.5 Writing to Flash Program Memory

The minimum programming block is 8 words or 16 bytes. Word or byte programming is not supported.

Table writes are used internally to load the holding registers needed to program the Flash memory. There are 16 holding registers used by the table writes for programming.

Since the Table Latch (TABLAT) is only a single byte, the ${\tt TBLWT}$ instruction may need to be executed 16 times for each programming operation. All of the table write operations will essentially be short writes because only the holding registers are written. At the end of updating the 16 holding registers, the EECON1 register must be written to in order to start the programming operation with a long write.

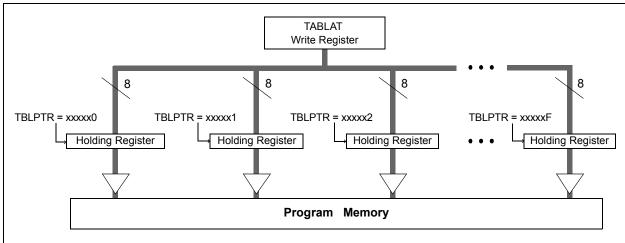
The long write is necessary for programming the internal Flash. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device.

Note:

The default value of the holding registers on device Resets and after write operations is FFh. A write of FFh to a holding register does not modify that byte. This means that individual bytes of program memory may be modified, provided that the change does not attempt to change any bit from a '0' to a '1'. When modifying individual bytes, it is not necessary to load all 16 holding registers before executing a write operation.





6.5.1 FLASH PROGRAM MEMORY WRITE SEQUENCE

The sequence of events for programming an internal program memory location should be:

- Read 64 bytes into RAM.
- 2. Update data values in RAM as necessary.
- Load Table Pointer register with address being erased.
- Execute the Row Erase procedure.
- 5. Load Table Pointer register with address of first byte being written.
- Write 16 bytes into the holding registers with auto-increment.
- 7. Set the EECON1 register for the write operation:
 - · clear the CFGS bit to access program memory;
 - · set WREN to enable byte writes.
- 8. Disable interrupts.
- Write 55h to EECON2.

- 10. Write 0AAh to EECON2.
- 11. Set the WR bit. This will begin the write cycle.
- 12. The CPU will stall for duration of the write (about 2 ms using internal timer).
- 13. Re-enable interrupts.
- 14. Repeat steps 6 through 14 once more to write 64 bytes.
- 15. Verify the memory (table read).

This procedure will require about 8 ms to update one row of 64 bytes of memory. An example of the required code is given in Example 6-3.

Note: Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the 16 bytes in the holding register.

EXAMPLE 6-3: WRITING TO FLASH PROGRAM MEMORY

EXAMPLE 6-3:	VVICION	IG TO FLASH PROGRAM	WEWORT
	MOVLW	D'64'	; number of bytes in erase block
	MOVWF	COUNTER	
	MOVLW	BUFFER_ADDR_HIGH	; point to buffer
	MOVWF	FSR0H	
	MOVLW	BUFFER_ADDR_LOW	
	MOVWF	FSR0L	
	MOVLW	CODE ADDR UPPER	; Load TBLPTR with the base
	MOVWF	TBLPTRU	; address of the memory block
	MOVLW	CODE ADDR HIGH	-
	MOVWF	TBLPTRH	
	MOVLW	CODE ADDR LOW	
	MOVWF	TBLPTRL	
READ BLOCK			
_ `	TBLRD*+		; read into TABLAT, and inc
	MOVF	TABLAT, W	; get data
	MOVWF	POSTINCO	; store data
	DECFSZ	COUNTER	; done?
	BRA	READ BLOCK	; repeat
MODIFY WORD	2141		, 100000
-102111_"01\D	MOVLW	DATA ADDR HIGH	; point to buffer
	MOVWF	FSR0H	,
	MOVLW	DATA ADDR LOW	
	MOVEW	FSR0L	
	MOVWE		; update buffer word
	MOVEW	NEW_DATA_LOW POSTINCO	, apaace parrer word
	MOVWE		
	MOVEW	NEW_DATA_HIGH INDF0	
EDACE DIOCK	MOVWE	INDEO	
ERASE_BLOCK	MOVIT W	CODE YDDD 11DDED	· load TRIDTD with the bace
	MOVIME	CODE_ADDR_UPPER	; load TBLPTR with the base
	MOVWF	TBLPTRU	; address of the memory block
	MOVLW	CODE_ADDR_HIGH	
	MOVWF	TBLPTRH	
	MOVLW	CODE_ADDR_LOW	
	MOVWF	TBLPTRL	Black anna
	BCF	EECON1, CFGS	; access Flash program memory
	BSF	EECON1, WREN	; enable write to memory
	BSF	EECON1, FREE	; enable Row Erase operation
	BCF	INTCON, GIE	; disable interrupts
	MOTITI	E E L	
D	MOVLW	55h	
Required	MOVWF	EECON2	; write 55h
Sequence	MOVLW	0AAh	
	MOVWF	EECON2	; write OAAh
	BSF	EECON1, WR	; start erase (CPU stall)
	BSF	INTCON, GIE	; re-enable interrupts
	TBLRD*-		; dummy read decrement
	MOVLW	BUFFER_ADDR_HIGH	; point to buffer
	MOVWF	FSROH	
	MOVLW	BUFFER_ADDR_LOW	
	MOVWF	FSROL	
	MOVLW	D'4'	
	MOVWF	COUNTER1	
WRITE_BUFFER_E			
	MOVLW	D'16'	; number of bytes in holding register
	MOVWF	COUNTER	
WRITE_BYTE_TO_	_		
	MOVF	POSTINCO, W	; get low byte of buffer data
	MOVWF	TABLAT	; present data to table latch
	TBLWT+*		; write data, perform a short write
			; to internal TBLWT holding register.
	DECFSZ	COUNTER	; loop until buffers are full
Ì	BRA	WRITE_WORD_TO_HREGS	

EXAMPLE 6-3: WRITING TO FLASH PROGRAM MEMORY (CONTINUED)

PROGRAM_MEMORY	Y		
	BCF	EECON1, CFGS	; access Flash program memory
	BSF	EECON1, WREN	; enable write to memory
	BCF	INTCON, GIE	; disable interrupts
	MOVLW	55h	
Required	MOVWF	EECON2	; write 55h
Sequence	MOVLW	0AAh	
	MOVWF	EECON2	; write OAAh
	BSF	EECON1, WR	; start program (CPU stall)
	DECFSZ	COUNTER1	
	BRA	WRITE_BUFFER_BACK	
	BSF	INTCON, GIE	; re-enable interrupts
	BCF	EECON1, WREN	; disable write to memory

6.5.2 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

6.5.3 UNEXPECTED TERMINATION OF WRITE OPERATION

If a write is terminated by an unplanned event, such as loss of power or an unexpected Reset, the memory location just programmed should be verified and reprogrammed if needed. If the write operation is interrupted by a MCLR Reset or a WDT time-out Reset during normal operation, the user can check the WRERR bit and rewrite the location(s) as needed.

6.5.4 PROTECTION AGAINST SPURIOUS WRITES

To protect against spurious writes to Flash program memory, the write initiate sequence must also be followed. See Section 18.0 "Special Features of the CPU" for more detail.

6.6 Flash Program Operation During Code Protection

See Section 18.5 "Program Verification and Code Protection" for details on code protection of Flash program memory.

TABLE 6-2: REGISTERS ASSOCIATED WITH PROGRAM FLASH MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
TBLPTRU			bit 21	Program Me	emory Table F	Pointer Uppe	r Byte (TBLP	TR<20:16>)	49
TBPLTRH	Program M	emory Table	Pointer H	igh Byte (TB	LPTR<15:8	>)			49
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								49
TABLAT	Program M	emory Table	Latch						49
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
EECON2	Data Memo	ry Control F	Register 2 (not a physic	al register)				51
EECON1	_	CFGS	_	FREE	WRERR	WREN	WR	_	51
IPR2	OSCFIP	_	USBIP	_	_	HLVDIP	_	_	51
PIR2	OSCFIF	_	USBIF	_	_	HLVDIF	_	_	51
PIE2	OSCFIE	_	USBIE	_	_	HLVDIE	_	_	51

Legend: — = unimplemented, read as '0'. Shaded cells are not used during Flash access.

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NOTES:

7.0 8 x 8 HARDWARE MULTIPLIER

7.1 Introduction

All PIC18 devices include an 8 x 8 hardware multiplier as part of the ALU. The multiplier performs an unsigned operation and yields a 16-bit result that is stored in the product register pair, PRODH:PRODL. The multiplier's operation does not affect any flags in the STATUS register.

Making multiplication a hardware operation allows it to be completed in a single instruction cycle. This has the advantages of higher computational throughput and reduced code size for multiplication algorithms and allows the PIC18 devices to be used in many applications previously reserved for digital signal processors. A comparison of various hardware and software multiply operations, along with the savings in memory and execution time, is shown in Table 7-1.

7.2 Operation

Example 7-1 shows the instruction sequence for an 8 x 8 unsigned multiplication. Only one instruction is required when one of the arguments is already loaded in the WREG register.

Example 7-2 shows the sequence to do an 8×8 signed multiplication. To account for the sign bits of the arguments, each argument's Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 7-1: 8 x 8 UNSIGNED MULTIPLY ROUTINE

MOVF ARG1, W ;
MULWF ARG2 ; ARG1 * ARG2 ->
; PRODH:PRODL

EXAMPLE 7-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
MOVF
       ARG1, W
                  ; ARG1 * ARG2 ->
MULWE
       ARG2
                  ; PRODH:PRODL
BTFSC
       ARG2, SB
                 ; Test Sign Bit
SUBWF
       PRODH, F ; PRODH = PRODH
                            - ARG1
       ARG2, W
MOVF
BTFSC
       ARG1, SB
                  ; Test Sign Bit
SUBWF
       PRODH, F
                  ; PRODH = PRODH
                            - ARG2
```

TABLE 7-1: PERFORMANCE COMPARISON FOR VARIOUS MULTIPLY OPERATIONS

		Program	Cycles	Time			
Routine	Multiply Method	Memory (Words)	(Max)	@ 40 MHz	@ 10 MHz	@ 4 MHz	
9 v 9 unsigned	Without hardware multiply	13	69	6.9 μs	27.6 μs	69 μs	
8 x 8 unsigned	Hardware multiply	1	1	100 ns	400 ns	1 μs	
0 v 0 signed	Without hardware multiply	33	91	9.1 μs	36.4 μs	91 μs	
8 x 8 signed	Hardware multiply	6	6	600 ns	2.4 μs	6 μs	
16 v 16 upoignod	Without hardware multiply	21	242	24.2 μs	96.8 μs	242 μs	
16 x 16 unsigned	Hardware multiply	28	28	2.8 μs	11.2 μs	28 μs	
16 v 16 signed	Without hardware multiply	52	254	25.4 μs	102.6 μs	254 μs	
16 x 16 signed	Hardware multiply	35	40	4.0 μs	16.0 μs	40 μs	

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Example 7-3 shows the sequence to do a 16 x 16 unsigned multiplication. Equation 7-1 shows the algorithm that is used. The 32-bit result is stored in four registers (RES3:RES0).

EQUATION 7-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

```
RES3:RES0 = ARG1H:ARG1L \bullet ARG2H:ARG2L

= (ARG1H \bullet ARG2H \bullet 2<sup>16</sup>) +

(ARG1H \bullet ARG2L \bullet 2<sup>8</sup>) +

(ARG1L \bullet ARG2H \bullet 2<sup>8</sup>) +

(ARG1L \bullet ARG2L)
```

EXAMPLE 7-3: 16 x 16 UNSIGNED MULTIPLY ROUTINE

```
ARG1L, W
MOVE
       ARG2L
MULWE
                      ; ARG1L * ARG2L->
                      ; PRODH: PRODL
MOVFF
       PRODH, RES1
                      ;
MOVFF
       PRODL, RESO
       ARG1H, W
MOVF
                      ; ARG1H * ARG2H->
MULWF
       ARG2H
                      ; PRODH:PRODL
MOVFF PRODH, RES3
MOVFF PRODL, RES2
       ARG1L, W
MOVF
MULWF
       ARG2H
                      ; ARG1L * ARG2H->
                      ; PRODH: PRODL
       PRODL, W
MOVF
ADDWF RES1, F
                      ; Add cross
                      ; products
MOVF
       PRODH, W
ADDWFC RES2, F
CLRF
       WREG
ADDWFC RES3, F
       ARG1H, W
MOVF
                      ; ARG1H * ARG2L->
MULWF
      ARG2L
                      ; PRODH:PRODL
       PRODL, W
MOVF
ADDWF RES1, F
                     ; Add cross
MOVF
       PRODH, W
                      ; products
ADDWFC RES2, F
CLRF
       WREG
                      ;
ADDWFC RES3, F
                      ;
```

Example 7-4 shows the sequence to do a 16 x 16 signed multiply. Equation 7-2 shows the algorithm used. The 32-bit result is stored in four registers (RES3:RES0). To account for the sign bits of the arguments, the MSb for each argument pair is tested and the appropriate subtractions are done.

EQUATION 7-2: 16 x 16 SIGNED MULTIPLICATION ALGORITHM

```
RES3:RES0=ARG1H:ARG1L • ARG2H:ARG2L
= (ARG1H • ARG2H • 2<sup>16</sup>) +
    (ARG1H • ARG2L • 2<sup>8</sup>) +
    (ARG1L • ARG2H • 2<sup>8</sup>) +
    (ARG1L • ARG2L) +
    (-1 • ARG2H<7> • ARG1H:ARG1L • 2<sup>16</sup>) +
    (-1 • ARG1H<7> • ARG2H:ARG2L • 2<sup>16</sup>)
```

EXAMPLE 7-4: 16 x 16 SIGNED MULTIPLY ROUTINE

```
MOVE
           ARG1L, W
   MULWF
          ARG2L
                        ; ARG1L * ARG2L ->
                       ; PRODH:PRODL
          PRODH, RES1 ;
   MOVFF
   MOVFF
           PRODL, RESO
   MOVF
           ARG1H, W
                       ; ARG1H * ARG2H ->
   MULWF
          ARG2H
                       ; PRODH:PRODL
   MOVFF
          PRODH, RES3 ;
           PRODL, RES2 ;
   MOVF
           ARG1 L. W
          ARG2H
                       ; ARG1L * ARG2H ->
   MULWF
                       ; PRODH:PRODL
   MOVF
           PRODL, W
          RES1, F
   ADDWF
                       ; Add cross
          PRODH, W
                       ; products
   MOVF
   ADDWFC RES2, F
   CLRF
          WREG
   ADDWFC RES3, F
          ARG1H, W
   MOVF
          ARG2L
   MULWF
                       ; ARG1H * ARG2L ->
                       ; PRODH:PRODL
   MOVF
           PRODL, W
          RES1, F
   ADDWF
                       ; Add cross
   MOVF
           PRODH, W
                       ; products
   ADDWFC RES2, F
           WREG
   CLRF
   ADDWFC RES3, F
                      ; ARG2H:ARG2L neg?
   BTFSS
          ARG2H, 7
   BRA
           SIGN ARG1
                       ; no, check ARG1
   MOVF
           ARG1L, W
   SUBWF
          RES2
          ARG1H, W
   MOVF
   SUBWFB RES3
SIGN ARG1
   BTFSS ARG1H, 7
                      ; ARG1H:ARG1L neg?
          CONT_CODE ; no, done
   BRA
   MOVF
          ARG2L, W
                       ;
   SUBWF
          RES2
   MOVF
          ARG2H, W
   SUBWFB RES3
CONT CODE
```

8.0 INTERRUPTS

The PIC18F2450/4450 devices have multiple interrupt sources and an interrupt priority feature that allows each interrupt source to be assigned a high-priority level or a low-priority level. The high-priority interrupt vector is at 000008h and the low-priority interrupt vector is at 000018h. High-priority interrupt events will interrupt any low-priority interrupts that may be in progress.

There are ten registers which are used to control interrupt operation. These registers are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2
- PIE1, PIE2
- · IPR1, IPR2

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/compiler to automatically take care of the placement of these bits within the specified register.

Each interrupt source has three bits to control its operation. The functions of these bits are:

- Flag bit to indicate that an interrupt event occurred
- Enable bit that allows program execution to branch to the interrupt vector address when the flag bit is set
- · Priority bit to select high priority or low priority

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set (high priority). Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared (low priority). When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 000008h or 000018h, depending on the priority bit setting. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC® mid-range microcontrollers. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit which enables/disables all interrupt sources. All interrupts branch to address 000008h in Compatibility mode.

When an interrupt is responded to, the global interrupt enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High-priority interrupt sources can interrupt a low-priority interrupt. Low-priority interrupts are not processed while high-priority interrupts are in progress.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (000008h or 000018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used) which re-enables interrupts.

For external interrupt events, such as the INTx pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding enable bit or the GIE bit.

Note: Do not use the MOVFF instruction to modify any of the interrupt control registers while **any** interrupt is enabled. Doing so may cause erratic microcontroller behavior.

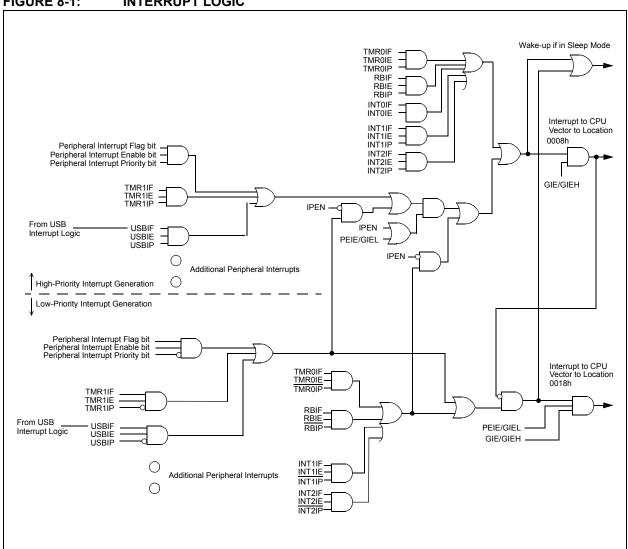
8.1 USB Interrupts

Unlike other peripherals, the USB module is capable of generating a wide range of interrupts for many types of events. These include several types of normal communication and status events and several module level error events.

To handle these events, the USB module is equipped with its own interrupt logic. The logic functions in a manner similar to the microcontroller level interrupt funnel, with each interrupt source having separate flag and enable bits. All events are funneled to a single device level interrupt, USBIF (PIR2<5>). Unlike the device level interrupt logic, the individual USB interrupt events cannot be individually assigned their own priority. This is determined at the device level interrupt funnel for all USB events by the USBIP bit.

For additional details on USB interrupt logic, refer to **Section 14.5 "USB Interrupts"**.

FIGURE 8-1: **INTERRUPT LOGIC**



8.2 INTCON Registers

The INTCON registers are readable and writable registers which contain various enable, priority and flag bits.

Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global interrupt enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF ⁽¹⁾
bit 7							bit 0

Note:

Legend:						
R = Readable bit	W = Writable bit	U = Unimplemented bit,	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 7 **GIE/GIEH:** Global Interrupt Enable bit

When IPEN = 0:

1 = Enables all unmasked interrupts

0 = Disables all interrupts

When IPEN = 1:

1 = Enables all high-priority interrupts

0 = Disables all interrupts

bit 6 PEIE/GIEL: Peripheral Interrupt Enable bit

When IPEN = 0:

1 = Enables all unmasked peripheral interrupts

0 = Disables all peripheral interrupts

When IPEN = 1:

1 = Enables all low-priority peripheral interrupts

0 = Disables all low-priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 overflow interrupt

0 = Disables the TMR0 overflow interrupt

bit 4 INT0IE: INT0 External Interrupt Enable bit

1 = Enables the INT0 external interrupt

0 = Disables the INT0 external interrupt

bit 3 RBIE: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt

0 = Disables the RB port change interrupt

bit 2 TMR0IF: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)

0 = TMR0 register did not overflow

bit 1 INT0IF: INT0 External Interrupt Flag bit

1 = The INT0 external interrupt occurred (must be cleared in software)

0 = The INT0 external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit⁽¹⁾

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)

0 = None of the RB7:RB4 pins have changed state

Note 1: A mismatch condition will continue to set this bit. Reading PORTB and waiting 1 Tcy will end the mismatch condition and allow the bit to be cleared.

REGISTER 8-2: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
RBPU	INTEDG0	INTEDG1	INTEDG2	-	TMR0IP	_	RBIP
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 RBPU: PORTB Pull-up Enable bit

1 = All PORTB pull-ups are disabled

0 = PORTB pull-ups are enabled by individual port latch values

bit 6 INTEDG0: External Interrupt 0 Edge Select bit

1 = Interrupt on rising edge0 = Interrupt on falling edge

bit 5 INTEDG1: External Interrupt 1 Edge Select bit

1 = Interrupt on rising edge0 = Interrupt on falling edge

bit 4 INTEDG2: External Interrupt 2 Edge Select bit

1 = Interrupt on rising edge 0 = Interrupt on falling edge

bit 3 **Unimplemented:** Read as '0'

bit 2 **TMR0IP:** TMR0 Overflow Interrupt Priority bit

1 = High priority0 = Low priority

bit 1 **Unimplemented:** Read as '0'

bit 0 RBIP: RB Port Change Interrupt Priority bit

1 = High priority
0 = Low priority

Note: Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global interrupt enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 8-3: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	_	INT2IE	INT1IE	_	INT2IF	INT1IF
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 INT2IP: INT2 External Interrupt Priority bit

1 = High priority0 = Low priority

bit 6 INT1IP: INT1 External Interrupt Priority bit

1 = High priority0 = Low priority

bit 5 **Unimplemented:** Read as '0'

bit 4 INT2IE: INT2 External Interrupt Enable bit

1 = Enables the INT2 external interrupt0 = Disables the INT2 external interrupt

bit 3 INT1IE: INT1 External Interrupt Enable bit

1 = Enables the INT1 external interrupt0 = Disables the INT1 external interrupt

bit 2 **Unimplemented:** Read as '0'

bit 1 INT2IF: INT2 External Interrupt Flag bit

1 = The INT2 external interrupt occurred (must be cleared in software)

0 = The INT2 external interrupt did not occur

bit 0 INT1IF: INT1 External Interrupt Flag bit

1 = The INT1 external interrupt occurred (must be cleared in software)

0 = The INT1 external interrupt did not occur

Note: Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global interrupt enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

8.3 PIR Registers

The PIR registers contain the individual flag bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Request (Flag) registers (PIR1 and PIR2).

- **Note 1:** Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>).
 - 2: User software should ensure the appropriate interrupt flag bits are cleared prior to enabling an interrupt and after servicing that interrupt.

REGISTER 8-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1

U-0	R/W-0	R-0	R-0	U-0	R/W-0	R/W-0	R/W-0
_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

Lea	е	n	d	:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 ADIF: A/D Converter Interrupt Flag bit

1 = An A/D conversion completed (must be cleared in software)

0 = The A/D conversion is not complete

bit 5 RCIF: EUSART Receive Interrupt Flag bit

1 = The EUSART receive buffer, RCREG, is full (cleared when RCREG is read)

0 = The EUSART receive buffer is empty

bit 4 TXIF: EUSART Transmit Interrupt Flag bit

1 = The EUSART transmit buffer, TXREG, is empty (cleared when TXREG is written)

0 = The EUSART transmit buffer is full

bit 3 Unimplemented: Read as '0'

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode.

bit 1 TMR2IF: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0 TMR1IF: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflowed (must be cleared in software)

0 = TMR1 register did not overflow

REGISTER 8-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0
OSCFIF	_	USBIF	_	_	HLVDIF	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 OSCFIF: Oscillator Fail Interrupt Flag bit

1 = System oscillator failed, clock input has changed to INTRC (must be cleared in software)

0 = System clock operating

bit 6 Unimplemented: Read as '0' bit 5 USBIF: USB Interrupt Flag bit

1 = USB has requested an interrupt (must be cleared in software)

0 = No USB interrupt request

bit 4-3 Unimplemented: Read as '0'

bit 2 **HLVDIF:** High/Low-Voltage Detect Interrupt Flag bit

1 = A high/low-voltage condition occurred0 = No high/low-voltage event has occurred

bit 1-0 Unimplemented: Read as '0'

8.4 PIE Registers

Legend:

R = Readable bit

The PIE registers contain the individual enable bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Enable registers (PIE1 and PIE2). When IPEN = 0, the PEIE bit must be set to enable any of these peripheral interrupts.

REGISTER 8-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

W = Writable bit

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

U = Unimplemented bit, read as '0'

x = Bit is unknown

-n = Value at Po	OR '1' = Bit is set	'0' = Bit is cleared
bit 7	Unimplemented: Read as '0'	
bit 6	ADIE: A/D Converter Interrupt Enable bit	
	1 = Enables the A/D interrupt	
	0 = Disables the A/D interrupt	
bit 5	RCIE: EUSART Receive Interrupt Enable	bit
	1 = Enables the EUSART receive interrup	
	0 = Disables the EUSART receive interrup	ot
bit 4	TXIE: EUSART Transmit Interrupt Enable	bit
	1 = Enables the EUSART transmit interru	pt
	0 = Disables the EUSART transmit interru	ıpt
bit 3	Unimplemented: Read as '0'	
bit 2	CCP1IE: CCP1 Interrupt Enable bit	
	1 = Enables the CCP1 interrupt	
	0 = Disables the CCP1 interrupt	
bit 1	TMR2IE: TMR2 to PR2 Match Interrupt Er	nable bit
	$_{1}$ = Enables the TMR2 to PR2 match inter	•
	0 = Disables the TMR2 to PR2 match inte	rrupt
bit 0	TMR1IE: TMR1 Overflow Interrupt Enable	bit
	$_{1}$ = Enables the TMR1 overflow interrupt	
	0 = Disables the TMR1 overflow interrupt	

REGISTER 8-7: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0
OSCFIE	_	USBIE	_	_	HLVDIE	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 OSCFIE: Oscillator Fail Interrupt Enable bit

1 = Enabled
0 = Disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 USB Interrupt Enable bit

1 = Enabled
0 = Disabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit

1 = Enabled
0 = Disabled

bit 1-0 **Unimplemented:** Read as '0'

8.5 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Priority registers (IPR1 and IPR2). Using the priority bits requires that the Interrupt Priority Enable (IPEN) bit be set.

REGISTER 8-8: IPR1: PERIPHERAL INTERRUPT PRIORITY REGISTER 1

U-0	R/W-1	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	I as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	Unimplemented: Read as '0'
bit 6	ADIP: A/D Converter Interrupt Priority bit
	1 = High priority
	0 = Low priority
bit 5	RCIP: EUSART Receive Interrupt Priority bit
	1 = High priority
	0 = Low priority
bit 4	TXIP: EUSART Transmit Interrupt Priority bit
	1 = High priority
	0 = Low priority
bit 3	Unimplemented: Read as '0'
bit 2	CCP1IP: CCP1 Interrupt Priority bit
	1 = High priority
	0 = Low priority
bit 1	TMR2IP: TMR2 to PR2 Match Interrupt Priority bit
	1 = High priority
	0 = Low priority
bit 0	TMR1IP: TMR1 Overflow Interrupt Priority bit
	1 = High priority
	0 = Low priority

REGISTER 8-9: IPR2: PERIPHERAL INTERRUPT PRIORITY REGISTER 2

R/W-1	U-0	R/W-1	U-0	U-0	R/W-1	U-0	U-0
OSCFIP	_	USBIP	_	_	HLVDIP	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 OSCFIP: Oscillator Fail Interrupt Priority bit

1 = High priority0 = Low priority

bit 6 Unimplemented: Read as '0'

bit 5 USBIP: USB Interrupt Priority bit

1 = High priority0 = Low priority

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **HLVDIP:** High/Low-Voltage Detect Interrupt Priority bit

1 = High priority0 = Low priority

bit 1-0 Unimplemented: Read as '0'

8.6 RCON Register

The RCON register contains flag bits which are used to determine the cause of the last Reset or wake-up from Idle or Sleep modes. RCON also contains the IPEN bit which enables interrupt priorities.

REGISTER 8-10: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1 ⁽¹⁾	U-0	R/W-1	R-1	R-1	R/W-0 ⁽²⁾	R/W-0
IPEN	SBOREN	_	RI	TO	PD	POR	BOR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 7 IPEN: Int	errupt Priority Enable bit		

bit 7	IPEN: Interrupt Priority Enable bit 1 = Enable priority levels on interrupts
	0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)
bit 6	SBOREN: BOR Software Enable bit ⁽¹⁾
	For details of bit operation, see Register 4-1.
bit 5	Unimplemented: Read as '0'
bit 4	RI: RESET Instruction Flag bit
	For details of bit operation, see Register 4-1.
bit 3	TO: Watchdog Time-out Flag bit
	For details of bit operation, see Register 4-1.
bit 2	PD: Power-Down Detection Flag bit
	For details of bit operation, see Register 4-1.
bit 1	POR: Power-on Reset Status bit ⁽²⁾
	For details of bit operation, see Register 4-1.
bit 0	BOR: Brown-out Reset Status bit
	For details of bit operation, see Register 4-1.

- **Note 1:** If SBOREN is enabled, its Reset state is '1'; otherwise, it is '0'. See Register 4-1 for additional information.
 - 2: The actual Reset value of POR is determined by the type of device Reset. See Register 4-1 for additional information.

8.7 INTx Pin Interrupts

External interrupts on the RB0/AN12/INT0, RB1/AN10/INT1and RB2/AN8/INT2/VMO pins are edge-triggered. If the corresponding INTEDGx bit in the INTCON2 register is set (= 1), the interrupt is triggered by a rising edge; if the bit is clear, the trigger is on the falling edge. When a valid edge appears on the RBx/INTx pin, the corresponding flag bit, INTxIF, is set. This interrupt can be disabled by clearing the corresponding enable bit, INTxIE. Flag bit, INTxIF, must be cleared in software in the Interrupt Service Routine before re-enabling the interrupt.

All external interrupts (INT0, INT1 and INT2) can wakeup the processor from the power-managed modes if bit, INTxIE, was set prior to going into the power-managed modes. If the Global Interrupt Enable bit, GIE, is set, the processor will branch to the interrupt vector following wake-up.

Interrupt priority for INT1 and INT2 is determined by the value contained in the interrupt priority bits, INT1IP (INTCON3<6>) and INT2IP (INTCON3<7>). There is no priority bit associated with INT0. It is always a high-priority interrupt source.

8.8 TMR0 Interrupt

In 8-bit mode (which is the default), an overflow in the TMR0 register (FFh \rightarrow 00h) will set flag bit, TMR0IF. In 16-bit mode, an overflow in the TMR0H:TMR0L register pair (FFFFh \rightarrow 0000h) will set TMR0IF. The interrupt can be enabled/disabled by setting/clearing enable bit, TMR0IE (INTCON<5>). Interrupt priority for Timer0 is determined by the value contained in the interrupt priority bit, TMR0IP (INTCON2<2>). See Section 12.0 "Timer2 Module" for further details on the Timer0 module.

8.9 PORTB Interrupt-on-Change

An input change on PORTB<7:4> sets flag bit, RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit, RBIE (INTCON<3>). Interrupt priority for PORTB interrupt-on-change is determined by the value contained in the interrupt priority bit, RBIP (INTCON2<0>).

8.10 Context Saving During Interrupts

During interrupts, the return PC address is saved on the stack. Additionally, the WREG, STATUS and BSR registers are saved on the Fast Return Stack. If a fast return from interrupt is not used (see **Section 5.3** "**Data Memory Organization**"), the user may need to save the WREG, STATUS and BSR registers on entry to the Interrupt Service Routine. Depending on the user's application, other registers may also need to be saved. Example 8-1 saves and restores the WREG, STATUS and BSR registers during an Interrupt Service Routine.

EXAMPLE 8-1: SAVING STATUS. WREG AND BSR REGISTERS IN RAM

```
MOVWF
       W TEMP
                                     ; W TEMP is in virtual bank
MOVFF
       STATUS, STATUS TEMP
                                     ; STATUS TEMP located anywhere
MOVFF
       BSR, BSR_TEMP
                                     ; BSR TMEP located anywhere
:
; USER ISR CODE
MOVEF
       BSR TEMP, BSR
                                     ; Restore BSR
       W TEMP, W
MOVF
                                     ; Restore WREG
       STATUS TEMP, STATUS
MOVEF
                                     ; Restore STATUS
```

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NOTES:

9.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

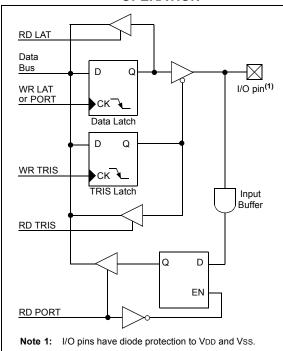
Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Output Latch register)

The Output Latch register (LATA) is useful for readmodify-write operations on the value driven by the I/O pins.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 9-1.

FIGURE 9-1: GENERIC I/O PORT OPERATION



9.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins; writing to it will write to the port latch.

The Output Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA6 pin is multiplexed with the main oscillator pin; it is enabled as an oscillator or I/O pin by the selection of the main oscillator in Configuration Register 1H (see Section 18.1 "Configuration Bits" for details). When not used as a port pin, RA6 and its associated TRIS and LAT bits are read as '0'.

RA4 is also multiplexed with the USB module; it serves as a receiver input from an external USB transceiver. For details on configuration of the USB module, see **Section 14.2 "USB Status and Control"**.

Several PORTA pins are multiplexed with analog inputs. The operation of pins RA5 and RA3:RA0 as A/D Converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note: On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 9-1: INITIALIZING PORTA

CLRF	PORTA	; Initialize PORTA by
		; clearing output
		; data latches
CLRF	LATA	; Alternate method
		; to clear output
		; data latches
MOVLW	0Fh	; Configure A/D
MOVWF	ADCON1	; for digital inputs
MOVLW	0CFh	; Value used to
		; initialize data
		; direction
MOVWF	TRISA	; Set RA<3:0> as inputs
		; RA<5:4> as outputs

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TABLE 9-1: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description				
RA0/AN0	RA0	0	OUT	DIG	LATA<0> data output; not affected by analog input.				
		1	IN	TTL	PORTA<0> data input; disabled when analog input enabled.				
	AN0	1	IN	ANA	A/D input channel 0. Default configuration on POR; does not affect digital output.				
RA1/AN1	RA1	0	OUT	DIG	LATA<1> data output; not affected by analog input.				
		1	IN	TTL	PORTA<1> data input; reads '0' on POR.				
	AN1	1	IN	ANA	A/D input channel 1. Default configuration on POR; does not affect digital output.				
RA2/AN2/	RA2	0	OUT	DIG	LATA<2> data output; not affected by analog input.				
VREF-		1	IN	TTL	PORTA<2> data input. Disabled when analog functions enabled.				
	AN2	1	IN	ANA	A/D input channel 2. Default configuration on POR; not affected by analog output.				
	VREF-	1	IN	ANA	A/D voltage reference low input.				
RA3/AN3/	RA3	0	OUT	DIG	LATA<3> data output; not affected by analog input.				
VREF+		1	IN	TTL	PORTA<3> data input; disabled when analog input enabled.				
	AN3	1	IN	ANA	A/D input channel 3. Default configuration on POR.				
	VREF+	1	IN	ANA	A/D voltage reference high input.				
RA4/T0CKI/	RA4	0	OUT	DIG	LATA<4> data output; not affected by analog input.				
RCV		1	IN	ST	PORTA<4> data input; disabled when analog input enabled.				
	T0CKI	1	IN	ST	Timer0 clock input.				
	RCV	Х	IN	TTL	External USB transceiver RCV input.				
RA5/AN4/	RA5	0	OUT	DIG	LATA<5> data output; not affected by analog input.				
HLVDIN		1	IN	TTL	PORTA<5> data input; disabled when analog input enabled.				
	AN4	1	IN	ANA	A/D input channel 4. Default configuration on POR.				
	HLVDIN	1	IN	ANA	High/Low-Voltage Detect external trip point input.				
OSC2/CLKO/	OSC2	Х	OUT	ANA	Main oscillator feedback output connection (all XT and HS modes).				
RA6	CLKO	Х	OUT	DIG	System cycle clock output (Fosc/4); available in EC, ECPLL and INTCKO modes.				
	RA6	0	OUT	DIG	LATA<6> data output. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.				
		1	IN	TTL	PORTA<6> data input. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.				

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

TABLE 9-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTA	_	RA6 ⁽¹⁾	RA5	RA4	RA3	RA2	RA1	RA0	51
LATA	_	LATA6 ⁽¹⁾	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	51
TRISA		TRISA6 ⁽¹⁾	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	51
ADCON1		_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	50
UCON	_	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	-	52

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTA.

Note 1: RA6 and its associated latch and data direction bits are enabled as I/O pins based on oscillator configuration; otherwise, they are read as '0'.

9.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Output Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Note: On a Power-on Reset, RB4:RB0 are configured as analog inputs by default and read as '0'; RB7:RB5 are configured as digital inputs.

By programming the Configuration bit, PBADEN (CONFIG3H<1>), RB4:RB0 will alternatively be configured as digital inputs

Four of the PORTB pins (RB7:RB4) have an interrupton-change feature. Only pins configured as inputs can cause this interrupt to occur. Any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison. The pins are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

The interrupt-on-change can be used to wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB (except with the MOVFF (ANY), PORTB instruction). This will end the mismatch condition.
- b) Wait one or more instruction cycles.

on POR.

c) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

Pins, RB2 and RB3, are multiplexed with the USB peripheral and serve as the differential signal outputs for an external USB transceiver (TRIS configuration). Refer to **Section 14.2.2.2 "External Transceiver"** for additional information on configuring the USB module for operation with an external transceiver.

EXAMPLE 9-2: INITIALIZING PORTB

CLRF	PORTB	; Initialize PORTB by ; clearing output ; data latches
CLRF	LATB	; Alternate method ; to clear output ; data latches
MOVLW	0Eh	; Set RB<4:0> as
MOVWF	ADCON1	; digital I/O pins
MOMINI M	0CFh	<pre>; (required if config bit ; PBADEN is set) ; Value used to</pre>
MOVIM	UCFII	; initialize data
		; direction
MOVWF	TRISB	; Set RB<3:0> as inputs
		; RB<5:4> as outputs
		; RB<7:6> as inputs

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TABLE 9-3: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description					
RB0/AN12/	RB0	0	OUT	DIG	LATB<0> data output; not affected by analog input.					
INT0		1	IN	TTL	PORTB<0> data input; weak pull-up when RBPU bit is cleared. Disabled when analog input enabled. ⁽¹⁾					
	AN12	1	IN	ANA	A/D input channel 12. ⁽¹⁾					
	INT0	1	IN	ST	External interrupt 0 input.					
RB1/AN10/	RB1	0	OUT	DIG	LATB<1> data output; not affected by analog input.					
INT1		1	IN	TTL	PORTB<1> data input; weak pull-up when RBPU bit is cleared. Disabled when analog input enabled. ⁽¹⁾					
	AN10	1	IN	ANA	A A/D input channel 10. ⁽¹⁾					
	INT1	1	IN	ST	External interrupt 1 input.					
RB2/AN8/	RB2	0	OUT	DIG	LATB<2> data output; not affected by analog input.					
INT2/VMO		1	IN	TTL	PORTB<2> data input; weak pull-up when RBPU bit is cleared. Disabled when analog input enabled. (1)					
	AN8	1	IN	ANA	A/D input channel 8. ⁽¹⁾					
	INT2	1	IN	ST	External interrupt 2 input.					
	VMO	0	OUT	DIG	External USB transceiver VMO data output.					
RB3/AN9/VPO	RB3	0	OUT	DIG	LATB<3> data output; not affected by analog input.					
		1	IN	TTL	PORTB<3> data input; weak pull-up when RBPU bit is cleared. Disabled when analog input enabled. ⁽¹⁾					
	AN9	1	IN	ANA	A/D input channel 9. ⁽¹⁾					
	VPO	0	OUT	DIG	External USB transceiver VPO data output.					
RB4/AN11/	RB4	RB4 0		DIG	LATB<4> data output; not affected by analog input.					
KBI0		1	IN	TTL	PORTB<4> data input; weak pull-up when RBPU bit is cleared. Disabled when analog input enabled. ⁽¹⁾					
	AN11	1	IN	ANA	A/D input channel 11. ⁽¹⁾					
	KBI0	1	IN	TTL	Interrupt-on-pin change.					
RB5/KBI1/	RB5	0	OUT	DIG	LATB<5> data output.					
PGM		1	IN	TTL	PORTB<5> data input; weak pull-up when RBPU bit is cleared.					
	KBI1	1	IN	TTL	Interrupt-on-pin change.					
	PGM	Х	IN	ST	Single-Supply Programming mode entry (ICSP™). Enabled by LVP Configuration bit; all other pin functions disabled.					
RB6/KBI2/	RB6	0	OUT	DIG	LATB<6> data output.					
PGC		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.					
	KBI2	1	IN	TTL	Interrupt-on-pin change.					
	PGC	Х	IN	ST	Serial execution (ICSP) clock input for ICSP and ICD operation. (2)					
RB7/KBI3/	RB7	0	OUT	DIG	LATB<7> data output.					
PGD		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.					
	KBI3	1	IN	TTL	Interrupt-on-pin change.					
	PGD	Х	OUT	DIG	Serial execution data output for ICSP and ICD operation. (2)					
		Х	IN	ST	Serial execution data input for ICSP and ICD operation. (2)					

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input,

 $TTL = TTL \ Buffer \ Input, \ x = Don't \ care \ (TRIS \ bit \ does \ not \ affect \ port \ direction \ or \ is \ overridden \ for \ this \ option)$

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

TABLE 9-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	51
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	51
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	51
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	-	RBIP	49
INTCON3	INT2IP	INT1IP	_	INT2IE	INT1IE	_	INT2IF	INT1IF	49
ADCON1	_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	50
UCON	_	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	_	52

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

9.3 PORTC, TRISC and LATC Registers

PORTC is a 7-bit wide, bidirectional port. The corresponding Data Direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

In PIC18F2450/4450 devices, the RC3 pin is not implemented.

The Output Latch register (LATC) is also memory mapped. Read-modify-write operations on the LATC register read and write the latched output value for PORTC.

PORTC is primarily multiplexed with serial communication modules, including the EUSART and the USB module (Table 9-5). Except for RC4 and RC5, PORTC uses Schmitt Trigger input buffers.

Pins RC4 and RC5 are multiplexed with the USB module. Depending on the configuration of the module, they can serve as the differential data lines for the onchip USB transceiver, or the data inputs from an external USB transceiver. Both RC4 and RC5 have TTL input buffers instead of the Schmitt Trigger buffers on the other pins.

Unlike other PORTC pins, RC4 and RC5 do not have TRISC bits associated with them. As digital ports, they can only function as digital inputs. When configured for USB operation, the data direction is determined by the configuration and status of the USB module at a given time. If an external transceiver is used, RC4 and RC5 always function as inputs from the transceiver. If the on-chip transceiver is used, the data direction is determined by the operation being performed by the module at that time.

When the external transceiver is enabled, RC2 also serves as the output enable control to the transceiver. Additional information on configuring USB options is provided in **Section 14.2.2.2** "External Transceiver".

When enabling peripheral functions on PORTC pins other than RC4 and RC5, care should be taken in defining the TRIS bits. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Note: On a Power-on Reset, these pins, except RC4 and RC5, are configured as digital inputs. To use pins RC4 and RC5 as digital inputs, the USB module must be disabled (UCON<3> = 0) and the on-chip USB transceiver must be disabled (UCFG<3> = 1).

The contents of the TRISC register are affected by peripheral overrides. Reading TRISC always returns the current contents, even though a peripheral device may be overriding one or more of the pins.

EXAMPLE 9-3: INITIALIZING PORTC

```
CLRF
        PORTC
               ; Initialize PORTC by
                ; clearing output
                ; data latches
CLRF
        LATC
                ; Alternate method
                ; to clear output
                ; data latches
       07h
M.TVOM
                ; Value used to
                ; initialize data
                ; direction
MOVWF
       TRISC
               ; RC<5:0> as outputs
                ; RC<7:6> as inputs
```

TABLE 9-5: PORTC I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description		
RC0/T1OSO/	RC0	0	OUT	DIG	LATC<0> data output.		
T1CKI		1	IN	ST	PORTC<0> data input.		
	T10S0	х	OUT	ANA	Timer1 oscillator output; enabled when Timer1 oscillator enabled. Disables digital I/O.		
	T1CKI	1	IN	ST	Timer1 counter input.		
RC1/T1OSI/	RC1	0	OUT	DIG	LATC<1> data output.		
UOE		1	IN	ST	PORTC<1> data input.		
	T10SI	х	IN	ANA	Timer1 oscillator input; enabled when Timer1 oscillator enabled. Disables digital I/O.		
	UOE	0	OUT	DIG	External USB transceiver OE output.		
RC2/CCP1	RC2	0	OUT	DIG	LATC<2> data output.		
		1	IN	ST	PORTC<2> data input.		
	CCP1	0	OUT	DIG	CCP1 Compare and PWM output; takes priority over port data.		
		1	IN	ST	CCP1 Capture input.		
RC4/D-/VM	RC4	(1)	IN	TTL	PORTC<4> data input; disabled when USB module or on-chip transceiver is enabled.		
	D-	(1)	OUT	XCVR	USB bus differential minus line output (internal transceiver).		
		(1)	IN	XCVR	USB bus differential minus line input (internal transceiver).		
	VM	(1)	IN	TTL	External USB transceiver VM input.		
RC5/D+/VP	RC5	(1)	IN	TTL	PORTC<5> data input; disabled when USB module or on-chip transceiver is enabled.		
	D+	(1)	OUT	XCVR	USB bus differential plus line output (internal transceiver).		
		(1)	IN	XCVR	USB bus differential plus line input (internal transceiver).		
	VP	(1)	IN	TTL	External USB transceiver VP input.		
RC6/TX/CK	RC6	0	OUT	DIG	LATC<6> data output.		
		1	IN	ST	PORTC<6> data input.		
	TX	0	OUT	DIG	Asynchronous serial transmit data output (EUSART module); takes priority over port data. User must configure as output.		
	CK	0	OUT	DIG	Synchronous serial clock output (EUSART module); takes priority over port data.		
		1	IN	ST	Synchronous serial clock input (EUSART module).		
RC7/RX/DT	RC7	0	OUT	DIG	LATC<7> data output.		
		1	IN	ST	PORTC<7> data input.		
	RX	1	IN	ST	Asynchronous serial receive data input (EUSART module).		
	DT	1	OUT	DIG	Synchronous serial data output (EUSART module).		
		1	IN	ST	Synchronous serial data input (EUSART module). User must configure as an input.		

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, XCVR = USB Transceiver, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: RC4 and RC5 do not have corresponding TRISC bits. In Port mode, these pins are input only. USB data direction is determined by the USB configuration.

PIC18F2450/4450

TABLE 9-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTC	RC7	RC6	RC5 ⁽¹⁾	RC4 ⁽¹⁾	_	RC2	RC1	RC0	51
LATC	LATC7	LATC6	_	_	_	LATC2	LATC1	LATC0	51
TRISC	TRISC7	TRISC6	_	_	_	TRISC2	TRISC1	TRISC0	51
UCON	_	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	_	52

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTC.

Note 1: RC5 and RC4 are only available as port pins when the USB module is disabled (UCON<3> = 0).

9.4 PORTD, TRISD and LATD Registers

Note: PORTD is only available on 40/44-pin devices.

PORTD is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISD. Setting a TRISD bit (=1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISD bit (=0) will make the corresponding PORTD pin an output (i.e., put the contents of the output latch on the selected pin).

The Output Latch register (LATD) is also memory mapped. Read-modify-write operations on the LATD register read and write the latched output value for PORTD.

All pins on PORTD are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note: On a Power-on Reset, these pins are configured as digital inputs.

EXAMPLE 9-4: INITIALIZING PORTD

CLRF	PORTD	; Initialize PORTD by ; clearing output
CLRF	LATD	; data latches ; Alternate method : to alear output
MOLITE	OCEL	; to clear output ; data latches
MOVLW	0CFh	; initialize data
MOVWF	TRISD	<pre>; direction ; Set RD<3:0> as inputs ; RD<5:4> as outputs ; RD<7:6> as inputs</pre>

TABLE 9-7: PORTD I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RD0	RD0	0	OUT	DIG	LATD<0> data output.
		1	IN	ST	PORTD<0> data input.
RD1	RD1	0	OUT	DIG	LATD<1> data output.
		1	IN	ST	PORTD<1> data input.
RD2	RD2	0	OUT	DIG	LATD<2> data output.
		1	IN	ST	PORTD<2> data input.
RD3	RD3	0	OUT	DIG	LATD<3> data output.
		1	IN	ST	PORTD<3> data input.
RD4	RD4	0	OUT	DIG	LATD<4> data output.
		1	IN	ST	PORTD<4> data input.
RD5	RD5	0	OUT	DIG	LATD<5> data output
		1	IN	ST	PORTD<5> data input
RD6	RD6	0	OUT	DIG	LATD<6> data output.
		1	IN	ST	PORTD<6> data input.
RD7	RD7	0	OUT	DIG	LATD<7> data output.
		1	IN	ST	PORTD<7> data input.

Legend: OUT = Output, IN = Input, DIG = Digital Output, ST = Schmitt Buffer Input

TABLE 9-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTD ⁽¹⁾	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	51
LATD ⁽¹⁾	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	51
TRISD ⁽¹⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	51

Note 1: These registers and/or bits are unimplemented on 28-pin devices.

9.5 PORTE, TRISE and LATE Registers

Depending on the particular PIC18F2450/4450 device selected, PORTE is implemented in two different ways.

For 40/44-pin devices, PORTE is a 4-bit wide port. Three pins (RE0/AN5, RE1/AN6 and RE2/AN7) are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers. When selected as an analog input, these pins will read as '0's.

The corresponding Data Direction register is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., put the contents of the output latch on the selected pin).

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset, RE2:RE0 are configured as analog inputs.

The Output Latch register (LATE) is also memory mapped. Read-modify-write operations on the LATE register read and write the latched output value for PORTE.

The fourth pin of PORTE (MCLR/VPP/RE3) is an input only pin. Its operation is controlled by the MCLRE Configuration bit. When selected as a port pin (MCLRE = 0), it

functions as a digital input only pin; as such, it does not have TRIS or LAT bits associated with its operation. Otherwise, it functions as the device's Master Clear input. In either configuration, RE3 also functions as the programming voltage input during programming.

Note: On a Power-on Reset, RE3 is enabled as a digital input only if Master Clear functionality is disabled.

EXAMPLE 9-5: INITIALIZING PORTE

CLRF	PORTE	; Initialize PORTE by
		; clearing output
		; data latches
CLRF	LATE	; Alternate method
		; to clear output
		; data latches
MOVLW	0Ah	; Configure A/D
MOVWF	ADCON1	; for digital inputs
MOVLW	03h	; Value used to
		; initialize data
		; direction
MOVWF	TRISC	; Set RE<0> as inputs
		; RE<1> as inputs
		; RE<2> as outputs

9.5.1 PORTE IN 28-PIN DEVICES

For 28-pin devices, PORTE is only available when Master Clear functionality is disabled (MCLRE = 0). In these cases, PORTE is a single bit, input only port comprised of RE3 only. The pin operates as previously described.

REGISTER 9-1: PORTE REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/W-0	R/W-0
_	_	_	_	RE3 ^(1,2)	RE2 ⁽³⁾	RE1 ⁽³⁾	RE0 ⁽³⁾
bit 7							bit 0

 Legend:
 R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'

 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RE3:RE0:** PORTE Data Input bits^(1,2,3)

- **Note 1:** implemented only when Master Clear functionality is disabled (MCLRE Configuration bit = 0); otherwise, read as '0'.
 - **2:** RE3 is the only PORTE bit implemented on both 28-pin and 40/44-pin devices. All other bits are implemented only when PORTE is implemented (i.e., 40/44-pin devices).
 - 3: Unimplemented in 28-pin devices; read as '0'.

TABLE 9-9: PORTE I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RE0/AN5	RE0	0	OUT	DIG	LATE<0> data output; not affected by analog input.
		1	IN	ST	PORTE<0> data input; disabled when analog input enabled.
	AN5	1	IN	ANA	A/D input channel 5; default configuration on POR.
RE1/AN6	RE1	0	OUT	DIG	LATE<1> data output; not affected by analog input.
		1	IN	ST	PORTE<1> data input; disabled when analog input enabled.
	AN6	1	IN	ANA	A/D input channel 6; default configuration on POR.
RE2/AN7	RE2	0	OUT	DIG	LATE<2> data output; not affected by analog input.
		1	IN	ST	PORTE<2> data input; disabled when analog input enabled.
	AN7	1	IN	ANA	A/D input channel 7; default configuration on POR.
MCLR/VPP/ RE3	MCLR	(1)	IN	ST	External Master Clear input; enabled when MCLRE Configuration bit is set.
	VPP	(1)	IN	ANA	High-voltage detection, used for ICSP™ mode entry detection. Always available regardless of pin mode.
	RE3	(1)	IN	ST	PORTE<3> data input; enabled when MCLRE Configuration bit is clear.

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input.
 Note 1: RE3 does not have a corresponding TRISE<3> bit. This pin is always an input regardless of mode.

TABLE 9-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTE	_	_	_	_	RE3 ^(1,2)	RE2 ⁽³⁾	RE1 ⁽³⁾	RE0 ⁽³⁾	51
LATE ⁽³⁾	_	_	_	_	_	LATE2	LATE1	LATE0	51
TRISE ⁽³⁾	_	_	_	_	_	TRISE2	TRISE1	TRISE0	51
ADCON1	_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	50

Legend: — = unimplemented, read as '0'

Note 1: Implemented only when Master Clear functionality is disabled (MCLRE Configuration bit = 0); otherwise, read as '0'.

- **2:** RE3 is the only PORTE bit implemented on both 28-pin and 40/44-pin devices. All other bits are implemented only when PORTE is implemented (i.e., 40/44-pin devices).
- 3: These registers and/or bits are unimplemented on 28-pin devices.

10.0 TIMERO MODULE

The Timer0 module incorporates the following features:

- Software selectable operation as a timer or counter in both 8-bit or 16-bit modes
- · Readable and writable registers
- Dedicated 8-bit, software programmable prescaler
- · Selectable clock source (internal or external)
- · Edge select for external clock
- · Interrupt on overflow

bit 7

The T0CON register (Register 10-1) controls all aspects of the module's operation, including the prescale selection. It is both readable and writable.

A simplified block diagram of the Timer0 module in 8-bit mode is shown in Figure 10-1. Figure 10-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

REGISTER 10-1: TOCON: TIMERO CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR00N	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

	1 = Enables Timer0	
	0 = Stops Timer0	
bit 6	T08BIT: Timer0 8-Bit/16-Bit Control bit	

TMR0ON: Timer0 On/Off Control bit

1 - TimerO 8-Bit/16-Bit Control bit

1 = Timer0 is configured as an 8-bit timer/counter 0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit

1 = TImer0 prescaler is not assigned. Timer0 clock input bypasses prescaler.

 $\ensuremath{\textsc{0}}$ = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits

111 = 1:256 Prescale value 110 = 1:128 Prescale value 101 = 1:64 Prescale value 100 = 1:32 Prescale value 011 = 1:16 Prescale value 010 = 1:8 Prescale value 001 = 1:4 Prescale value 000 = 1:2 Prescale value

10.1 Timer0 Operation

Timer0 can operate as either a timer or a counter; the mode is selected by clearing the ToCS bit (T0CON<5>). In Timer mode, the module increments on every clock by default unless a different prescaler value is selected (see **Section 10.3 "Prescaler"**). If the TMR0 register is written to, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

The Counter mode is selected by setting the T0CS bit (= 1). In Counter mode, Timer0 increments either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (T0CON<4>); clearing this bit selects the rising edge. Restrictions on the external clock input are discussed below.

An external clock source can be used to drive Timer0; however, it must meet certain requirements to ensure that the external clock can be synchronized with the

internal phase clock (Tosc). There is a delay between synchronization and the onset of incrementing the timer/counter.

10.2 Timer0 Reads and Writes in 16-Bit Mode

TMR0H is not the actual high byte of Timer0 in 16-bit mode; it is actually a buffered version of the real high byte of Timer0, which is not directly readable nor writable (refer to Figure 10-2). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte were valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

FIGURE 10-1: TIMER0 BLOCK DIAGRAM (8-BIT MODE)

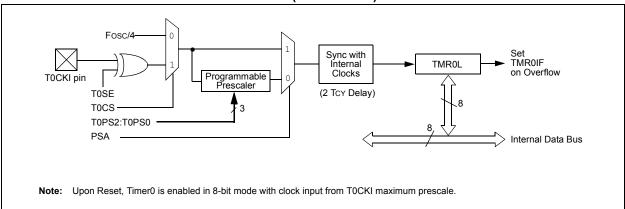
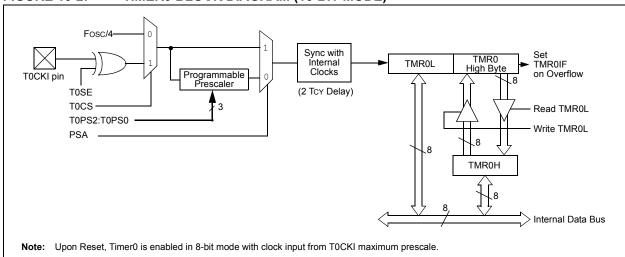


FIGURE 10-2: TIMER0 BLOCK DIAGRAM (16-BIT MODE)



10.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable; its value is set by the PSA and T0PS2:T0PS0 bits (T0CON<3:0>) which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When it is assigned, prescale values from 1:2 through 1:256, in power-of-2 increments, are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF $\tt TMR0$, MOVWF $\tt TMR0$, BSF $\tt TMR0$, etc.) clear the prescaler count.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count but will not change the prescaler assignment.

10.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed "on-the-fly" during program execution.

10.4 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit (INTCON<5>). Before reenabling the interrupt, the TMR0IF bit must be cleared in software by the Interrupt Service Routine.

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

TABLE 10-1: REGISTERS ASSOCIATED WITH TIMERO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
TMR0L Timer0 Register Low Byte									
TMR0H	Timer0 Reg	ister High By	/te						50
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
T0CON	TMR00N	TMROON TO8BIT TOCS TOSE PSA TOPS2 TOPS1 TOPS0							
TRISA	_	TRISA6 ⁽¹⁾	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	51

Legend: — = unimplemented locations, read as '0'. Shaded cells are not used by Timer0.

Note 1: RA6 is configured as a port pin based on various primary oscillator modes. When the port pin is disabled, all of the associated bits read '0'.

NOTES:

11.0 TIMER1 MODULE

The Timer1 timer/counter module incorporates these features:

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR1H and TMR1L)
- Selectable clock source (internal or external) with device clock or Timer1 oscillator internal options
- Interrupt on overflow

Legend:

R = Readable bit

- · Module Reset on CCP Special Event Trigger
- Device clock status flag (T1RUN)

A simplified block diagram of the Timer1 module is shown in Figure 11-1. A block diagram of the module's operation in Read/Write mode is shown in Figure 11-2.

The module incorporates its own low-power oscillator to provide an additional clocking option. The Timer1 oscillator can also be used as a low-power clock source for the microcontroller in power-managed operation.

Timer1 can also be used to provide Real-Time Clock (RTC) functionality to applications with only a minimal addition of external components and code overhead.

Timer1 is controlled through the T1CON Control register (Register 11-1). It also contains the Timer1 Oscillator Enable bit (T1OSCEN). Timer1 can be enabled or disabled by setting or clearing control bit, TMR1ON (T1CON<0>).

REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N
bit 7							bit 0

-n = Value at POR	'1' = Bit is set	

'1' = Bit is set 0' = Bit is cleared 0' = Bit is unknown

U = Unimplemented bit, read as '0'

bit 7 RD16: 16-Bit Read/Write Mode Enable bit

1 = Enables register read/write of Timer1 in one 16-bit operation0 = Enables register read/write of Timer1 in two 8-bit operations

bit 6 T1RUN: Timer1 System Clock Status bit

1 = Device clock is derived from Timer1 oscillator0 = Device clock is derived from another source

bit 5-4 T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits

W = Writable bit

11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value

bit 3 T10SCEN: Timer1 Oscillator Enable bit

1 = Timer1 oscillator is enabled 0 = Timer1 oscillator is shut off

The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 T1SYNC: Timer1 External Clock Input Synchronization Select bit

When TMR1CS = 1:

1 = Do not synchronize external clock input0 = Synchronize external clock input

When TMR1CS = 0:

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 TMR1CS: Timer1 Clock Source Select bit

1 = External clock from RC0/T1OSO/T1CKI pin (on the rising edge)

0 = Internal clock (Fosc/4)

bit 0 **TMR1ON:** Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

11.1 Timer1 Operation

Timer1 can operate in one of these modes:

- Timer
- · Synchronous Counter
- · Asynchronous Counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>). When TMR1CS is cleared (= 0), Timer1 increments on every internal instruction

cycle (Fosc/4). When the bit is set, Timer1 increments on every rising edge of the Timer1 external clock input or the Timer1 oscillator, if enabled.

When Timer1 is enabled, the RC1/T1OSI/UOE and RC0/T1OSO/T1CKI pins become inputs. This means the values of TRISC<1:0> are ignored and the pins are read as '0'.

FIGURE 11-1: TIMER1 BLOCK DIAGRAM

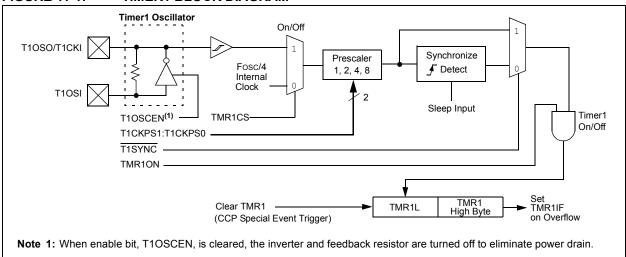
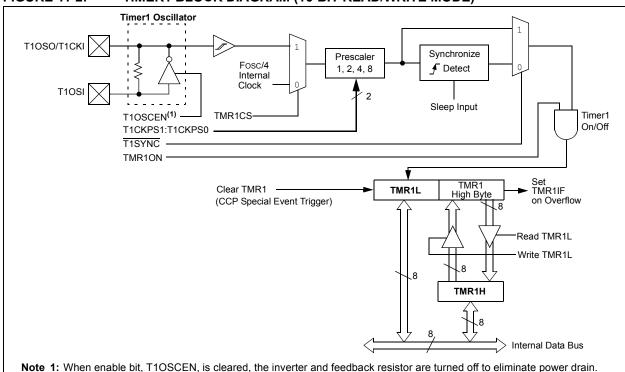


FIGURE 11-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



11.2 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 11-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 high byte buffer. This provides the user with the ability to accurately read all 16 bits of Timer1 without having to determine whether a read of the high byte, followed by a read of the low byte, has become invalid due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H Buffer register. The Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 High Byte Buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

11.3 Timer1 Oscillator

An on-chip crystal oscillator circuit is incorporated between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting the Timer1 Oscillator Enable bit, T1OSCEN (T1CON<3>). The oscillator is a low-power circuit rated for 32 kHz crystals. It will continue to run during all power-managed modes. The circuit for a typical LP oscillator is shown in Figure 11-3. Table 11-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

FIGURE 11-3: EXTERNAL

COMPONENTS FOR THE

TIMER1 LP OSCILLATOR

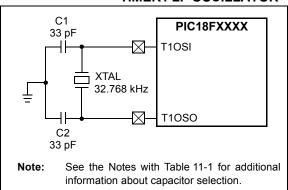


TABLE 11-1: CAPACITOR SELECTION FOR THETIMEROSCILLATOR^(2,3,4)

Osc Type	Freq	C1	C2	
LP	32 kHz	27 pF ⁽¹⁾	27 pF ⁽¹⁾	

- **Note 1:** Microchip suggests these values as a starting point in validating the oscillator circuit.
 - Higher capacitance increases the stability of the oscillator but also increases the start-up time.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - **4:** Capacitor values are for design guidance only.

11.3.1 USING TIMER1 AS A CLOCK SOURCE

The Timer1 oscillator is also available as a clock source in power-managed modes. By setting the clock select bits, SCS1:SCS0 (OSCCON<1:0>), to '01', the device switches to SEC_RUN mode. Both the CPU and peripherals are clocked from the Timer1 oscillator. If the IDLEN bit (OSCCON<7>) is cleared and a SLEEP instruction is executed, the device enters SEC_IDLE mode. Additional details are available in **Section 3.0** "Power-Managed Modes".

Whenever the Timer1 oscillator is providing the clock source, the Timer1 system clock status flag, T1RUN (T1CON<6>), is set. This can be used to determine the controller's current clocking mode. It can also indicate the clock source being currently used by the Fail-Safe Clock Monitor. If the Clock Monitor is enabled and the Timer1 oscillator fails while providing the clock, polling the T1RUN bit will indicate whether the clock is being provided by the Timer1 oscillator or another source.

11.3.2 LOW-POWER TIMER1 OPTION

The Timer1 oscillator can operate at two distinct levels of power consumption based on device configuration. When the LPT1OSC Configuration bit is set, the Timer1 oscillator operates in a low-power mode. When LPT1OSC is not set, Timer1 operates at a higher power level. Power consumption for a particular mode is relatively constant, regardless of the device's operating mode. The default Timer1 configuration is the higher power mode.

As the Low-Power Timer1 mode tends to be more sensitive to interference, high noise environments may cause some oscillator instability. The low-power option is, therefore, best suited for low noise applications where power conservation is an important design consideration.

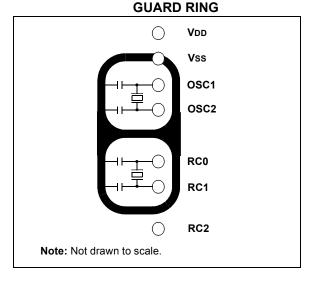
11.3.3 TIMER1 OSCILLATOR LAYOUT CONSIDERATIONS

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 11-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than Vss or VDD.

If a high-speed circuit must be located near the oscillator (such as the CCP1 pin in Output Compare or PWM mode, or the primary oscillator using the OSC2 pin), a grounded guard ring around the oscillator circuit, as shown in Figure 11-4, may be helpful when used on a single-sided PCB or in addition to a ground plane.

FIGURE 11-4: OSCILLATOR CIRCUIT WITH GROUNDED



11.4 Timer1 Interrupt

The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The Timer1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled or disabled by setting or clearing the Timer1 Interrupt Enable bit, TMR1IE (PIE1<0>).

11.5 Resetting Timer1 Using the CCP Special Event Trigger

If the CCP module is configured in Compare mode to generate a Special Event Trigger (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1. The trigger from CCP1 will also start an A/D conversion if the A/D module is enabled (see Section 13.3.4 "Special Event Trigger" for more information).

The module must be configured as either a timer or a synchronous counter to take advantage of this feature. When used this way, the CCPRH:CCPRL register pair effectively becomes a period register for Timer1.

If Timer1 is running in Asynchronous Counter mode, this Reset operation may not work.

In the event that a write to Timer1 coincides with a Special Event Trigger, the write operation will take precedence.

Note: The Special Event Triggers from the CCP1 module will not set the TMR1IF interrupt flag bit (PIR1<0>).

11.6 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in **Section 11.3 "Timer1 Oscillator"**) gives users the option to include RTC functionality to their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

The application code routine, RTCisr, shown in Example 11-1, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow triggers the interrupt and calls the routine which increments the seconds counter by one. Additional counters for minutes and hours are incremented as the previous counter overflows.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it. The simplest method is to set the MSb of TMR1H with a BSF instruction. Note that the TMR1L register is never preloaded or altered; doing so may introduce cumulative error over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (PIE1<0> = 1) as shown in the routine, RTCinit. The Timer1 oscillator must also be enabled and running at all times.

11.7 Considerations in Asynchronous Counter Mode

Following a Timer1 interrupt and an update to the TMR1 registers, the Timer1 module uses a falling edge on its clock source to trigger the next register update on the rising edge. If the update is completed after the clock input has fallen, the next rising edge will not be counted.

If the application can reliably update TMR1 before the timer input goes low, no additional action is needed. Otherwise, an adjusted update can be performed

following a later Timer1 increment. This can be done by monitoring TMR1L within the interrupt routine until it increments, and then updating the TMR1H:TMR1L register pair while the clock is low, or one-half of the period of the clock source. Assuming that Timer1 is being used as a Real-Time Clock, the clock source is a 32.768 kHz crystal oscillator. In this case, one-half period of the clock is 15.25 μs .

The Real-Time Clock application code in Example 11-1 shows a typical ISR for Timer1, as well as the optional code required if the update cannot be done reliably within the required interval.

EXAMPLE 11-1: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

```
RTCinit
          MOVLW
                   80h
                                  ; Preload TMR1 register pair
          MOVWF
                TMR1H
                                 ; for 1 second overflow
          CLRF
                 TMR1L
                b'00001111'; Configure for external clock,
          W.TVOM
          MOVWF T1CON
                                 ; Asynchronous operation, external oscillator
          CLRF
                  secs
                                 ; Initialize timekeeping registers
                  mins
          CLRF
          MOVIW
                  .12
                 hours
          MOVWF
          BSF
                  PIE1, TMR1IE
                                 ; Enable Timer1 interrupt
          RETURN
RTCisr
                                  ; Insert the next 4 lines of code when TMR1
                                  ; cannot be reliably updated before clock pulse goes low
                                 ; wait for TMR1L to become clear
          BTFSC
                  TMR1L,0
                   $-2
                                 ; (may already be clear)
          BTFSS
                  TMR1L,0
                                 ; wait for TMR1L to become set
                                  ; TMR1 has just incremented
                  $-2
          BRA
                                 ; If TMR1 update can be completed before clock pulse goes low
                                 ; Start ISR here
                 TMR1H, 7
                                 ; Preload for 1 sec overflow
          BSF
          BCF
                  PIR1, TMR1IF ; Clear interrupt flag
                 secs, F
          INCF
                                 ; Increment seconds
                  .59
                                 ; 60 seconds elapsed?
          MOVLW
          CPFSGT
                  secs
          RETURN
                                 ; No, done
          CLRF
                  secs
                                  ; Clear seconds
          INCF
                 mins, F
                                 ; Increment minutes
                  .59
                                  ; 60 minutes elapsed?
          MOVLW
          CPFSGT
                 mins
          RETURN
                                 ; No, done
          CLRF mins
                                 ; clear minutes
          INCE
                 hours, F
                                 ; Increment hours
          MOVLW
                  .23
                                  ; 24 hours elapsed?
          CPFSGT
                  hours
          RETURN
                                  ; No, done
          CLRF
                  hours
                                  ; Reset hours
                                  ; Done
          RETURN
```

TABLE 11-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
TMR1L	Timer1 Register Low Byte									
TMR1H	Tlmer1 Register High Byte									
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

12.0 TIMER2 MODULE

The Timer2 module timer incorporates the following features:

- 8-Bit Timer and Period Registers (TMR2 and PR2, respectively)
- · Readable and Writable (both registers)
- Software Programmable Prescaler (1:1, 1:4 and 1:16)
- Software Programmable Postscaler (1:1 through 1:16)
- · Interrupt on TMR2 to PR2 Match

The module is controlled through the T2CON register (Register 12-1) which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 12-1.

12.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (Fosc/4). A 2-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options. These are selected by the prescaler control bits, T2CKPS1:T2CKPS0 (T2CON<1:0>). The value of TMR2 is compared to that of the period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see Section 12.2 "Timer2 Interrupt").

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- · a write to the TMR2 register
- · a write to the T2CON register
- any device Reset (Power-on Reset, MCLR Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 T2OUTPS3:T2OUTPS0: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale 0001 = 1:2 Postscale

•

1111 = 1:16 Postscale

bit 2 TMR2ON: Timer2 On bit

1 = Timer2 is on 0 = Timer2 is off

bit 1-0 T2CKPS1:T2CKPS0: Timer2 Clock Prescale Select bits

00 = Prescaler is 1 01 = Prescaler is 4 1x = Prescaler is 16

12.2 Timer2 Interrupt

Timer2 also can generate an optional device interrupt. The Timer2 output signal (TMR2 to PR2 match) provides the input for the 4-bit output counter/ postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF (PIR1<1>). The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE (PIE1<1>).

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, T2OUTPS3:T2OUTPS0 (T2CON<6:3>).

12.3 TMR2 Output

The unscaled output of TMR2 is available primarily to the CCP module, where it is used as a time base for operations in PWM mode.

FIGURE 12-1: TIMER2 BLOCK DIAGRAM

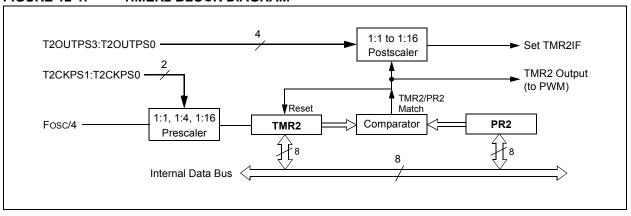


TABLE 12-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	-	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE		CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP		CCP1IP	TMR2IP	TMR1IP	51	
TMR2	Timer2 Register									
T2CON	_	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	50	
PR2	Timer2 Peri	iod Register	•			•			50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

13.0 CAPTURE/COMPARE/PWM (CCP) MODULE

PIC18F2450/4450 devices have one CCP (Capture/Compare/PWM) module. The module contains a 16-bit register, which can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register.

REGISTER 13-1: CCP1CON: CAPTURE/COMPARE/PWM CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 DC1B1:DC1B0: PWM Duty Cycle for CCP Module bits

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPR1L.

bit 3-0 CCP1M3:CCP1M0: CCP Module Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCP module)

0001 = Reserved

0010 = Compare mode: toggle output on match (CCP1IF bit is set)

0011 = Reserved

0100 = Capture mode: every falling edge

0101 = Capture mode: every rising edge

0110 = Capture mode: every 4th rising edge

0111 = Capture mode: every 16th rising edge

1000 = Compare mode: initialize CCP1 pin low; on compare match, force CCP1 pin high (CCP1IF bit is set)

1001 = Compare mode: initialize CCP1 pin high; on compare match, force CCP1 pin low (CCP1IF bit is set)

1010 = Compare mode: generate software interrupt on compare match (CCP1IF bit is set, CCP1 pin reflects I/O state)

1011 = Compare mode: trigger special event, reset timer and start A/D conversion on CCP1 match (CCP1IF bit is set)

11xx = PWM mode

13.1 CCP Module Configuration

The Capture/Compare/PWM module is associated with a control register (generically, CCP1CON) and a data register (CCPR1). The data register, in turn, is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). All registers are both readable and writable.

13.1.1 CCP MODULE AND TIMER RESOURCES

The CCP module utilizes Timer1 or Timer2, depending on the mode selected. Timer1 is available to the module in Capture or Compare modes, while Timer2 is available for modules in PWM mode.

TABLE 13-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

In Timer1 in Asynchronous Counter mode, the capture operation will not work.

13.2 Capture Mode

In Capture mode, the CCPR1H:CCPR1L register pair captures the 16-bit value of the TMR1 register when an event occurs on the corresponding CCP1 pin. An event is defined as one of the following:

- · every falling edge
- · every rising edge
- · every 4th rising edge
- · every 16th rising edge

The event is selected by the mode select bits, CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit, CCP1IF, is set; it must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new captured value.

13.2.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the corresponding TRIS direction bit.

Note: If RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

13.2.2 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit clear to avoid false interrupts. The interrupt flag bit, CCP1IF, should also be cleared following any such change in operating mode.

13.2.3 CCP PRESCALER

There are four prescaler settings in Capture mode. They are specified as part of the operating mode selected by the mode select bits (CCP1M3:CCP1M0). Whenever the CCP module is turned off or Capture mode is disabled, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 13-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 13-1: CHANGING BETWEEN
CAPTURE PRESCALERS
(CCP1 SHOWN)

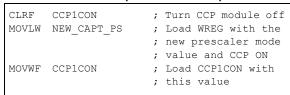
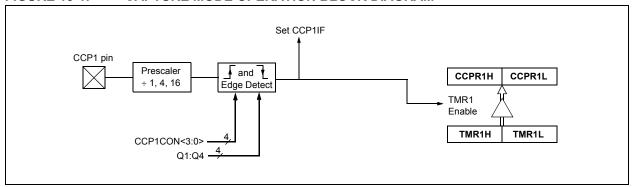


FIGURE 13-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



13.3 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 pin can be:

- · driven high
- · driven low
- toggled (high-to-low or low-to-high)
- remain unchanged (that is, reflects the state of the I/O latch)

The action on the pin is based on the value of the mode select bits (CCP1M3:CCP1M0). At the same time, the interrupt flag bit, CCP1IF, is set.

13.3.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the appropriate TRIS bit.

Note: Clearing the CCP1CON register will force the RC2 compare output latch to the default low level.

13.3.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode, or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

13.3.3 SOFTWARE INTERRUPT MODE

When the Generate Software Interrupt mode is chosen (CCP1M3:CCP1M0 = 1010), the CCP1 pin is not affected. Only a CCP interrupt is generated, if enabled, and the CCP1IE bit is set.

13.3.4 SPECIAL EVENT TRIGGER

The CCP module is equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCP1M3:CCP1M0 = 1011).

For the CCP module, the Special Event Trigger resets the Timer1 register pair. This allows the CCPR1 registers to serve as a programmable period register for the Timer1.

The Special Event Trigger for CCP1 can also start an A/D conversion. In order to do this, the A/D Converter must already be enabled.

FIGURE 13-2: COMPARE MODE OPERATION BLOCK DIAGRAM

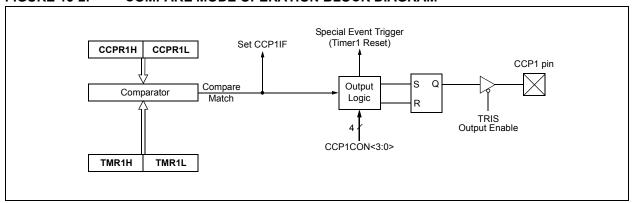


TABLE 13-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
RCON	IPEN	SBOREN ⁽¹⁾	_	RI	TO	PD	POR	BOR	50	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
TRISC	TRISC7	TRISC6		_	_	TRISC2	TRISC1	TRISC0	51	
TMR1L	Timer1 Reg	gister Low By	⁄te						50	
TMR1H	Timer1 Reg	gister High B	yte						50	
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	50	
CCPR1L	Capture/Compare/PWM Register 1 Low Byte									
CCPR1H	Capture/Compare/PWM Register 1 High Byte									
CCP1CON	_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used by capture/compare and Timer1.

Note 1: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.

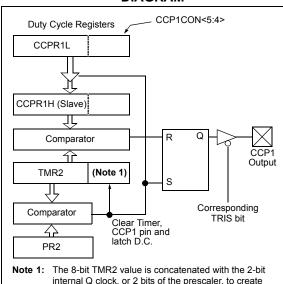
13.4 PWM Mode

In Pulse-Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output.

Figure 13-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 13.4.3** "**Setup for PWM Operation**".

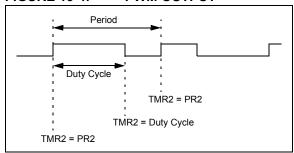
FIGURE 13-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 13-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 13-4: PWM OUTPUT

the 10-bit time base.



13.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

EQUATION 13-1:

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- · TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscalers (see Section 12.0 "Timer2 Module") are not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

13.4.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> bits contain the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. Equation 13-2 is used to calculate the PWM duty cycle in time:

EQUATION 13-2:

PWM Duty Cycle = (CCPR1L:CCP1CON<5:4>) • Tosc • (TMR2 Prescale Value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation:

EQUATION 13-3:

$$PWM Resolution (max) = \frac{\log(\frac{FOSC}{FPWM})}{\log(2)} bits$$

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

13.4.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- 3. Make the CCP1 pin an output by clearing the appropriate TRIS bit.
- 4. Set the TMR2 prescale value, then enable Timer2 by writing to T2CON.
- 5. Configure the CCP module for PWM operation.

TABLE 13-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	10	10	10	8	7	6.58

TABLE 13-4: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
RCON	IPEN	SBOREN ⁽¹⁾	_	RI	TO	PD	POR	BOR	50	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP		CCP1IP	TMR2IP	TMR1IP	51	
TRISC	TRISC7	TRISC6	_	_		TRISC2	TRISC1	TRISC0	51	
TMR2	Timer2 Reg	jister							50	
PR2	Timer2 Per	iod Register							50	
T2CON	_	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	50	
CCPR1L	Capture/Compare/PWM Register 1 Low Byte									
CCPR1H	Capture/Compare/PWM Register 1 High Byte									
CCP1CON	_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PWM or Timer2.

Note 1: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.

14.0 UNIVERSAL SERIAL BUS (USB)

This section describes the details of the USB peripheral. Because of the very specific nature of the module, knowledge of USB is expected. Some high-level USB information is provided in **Section 14.9 "Overview of USB"** only for application design reference. Designers are encouraged to refer to the official specification published by the USB Implementers Forum (USB-IF) for the latest information. USB Specification Revision 2.0 is the most current specification at the time of publication of this document.

14.1 Overview of the USB Peripheral

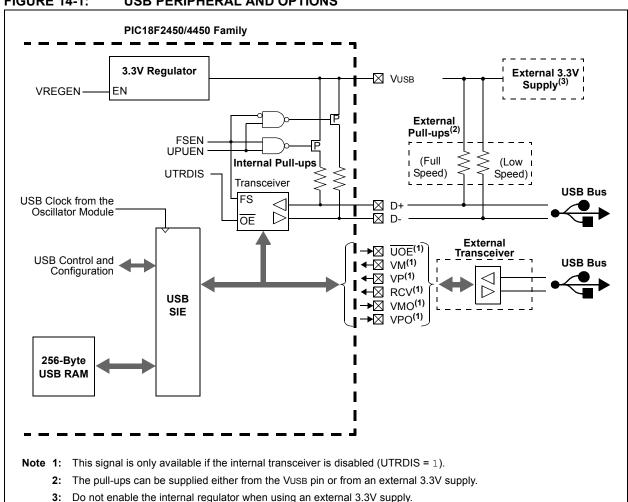
The PIC18F2450/4450 device family contains a full-speed and low-speed, compatible USB Serial Interface Engine (SIE) that allows fast communication between

any USB host and the PIC[®] microcontroller. The SIE can be interfaced directly to the USB, utilizing the internal transceiver, or it can be connected through an external transceiver. An internal 3.3V regulator is also available to power the internal transceiver in 5V applications.

Some special hardware features have been included to improve performance. Dual port memory in the device's data memory space (USB RAM) has been supplied to share direct memory access between the microcontroller core and the SIE. Buffer descriptors are also provided, allowing users to freely program endpoint memory usage within the USB RAM space.

Figure 14-1 presents a general overview of the USB peripheral and its features.

FIGURE 14-1: USB PERIPHERAL AND OPTIONS



14.2 USB Status and Control

The operation of the USB module is configured and managed through three control registers. In addition, a total of 22 registers are used to manage the actual USB transactions. The registers are:

- · USB Control register (UCON)
- USB Configuration register (UCFG)
- · USB Transfer Status register (USTAT)
- · USB Device Address register (UADDR)
- Frame Number registers (UFRMH:UFRML)
- Endpoint Enable registers 0 through 15 (UEPn)

14.2.1 USB CONTROL REGISTER (UCON)

The USB Control register (Register 14-1) contains bits needed to control the module behavior during transfers. The register contains bits that control the following:

- · Main USB Peripheral Enable
- · Ping-Pong Buffer Pointer Reset
- · Control of the Suspend Mode
- · Packet Transfer Disable

In addition, the USB Control register contains a status bit, SE0 (UCON<5>), which is used to indicate the occurrence of a single-ended zero on the bus. When the USB module is enabled, this bit should be monitored to determine whether the differential data lines have come out of a single-ended zero condition. This helps to differentiate the initial power-up state from the USB Reset signal.

The overall operation of the USB module is controlled by the USBEN bit (UCON<3>). Setting this bit activates the module and resets all of the PPBI bits in the Buffer Descriptor Table to '0'. This bit also activates the onchip voltage regulator, if enabled. Thus, this bit can be used as a soft attach/detach to the USB. Although all status and control bits are ignored when this bit is clear, the module needs to be fully preconfigured prior to setting this bit.

REGISTER 14-1: UCON: USB CONTROL REGISTER

U-0	R/W-0	R-x	R/C-0	R/W-0	R/W-0	R/W-0	U-0
_	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	_
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 Unimplemented: Read as '	
	γ,
	.)

bit 6 **PPBRST:** Ping-Pong Buffers Reset bit

1 = Reset all Ping-Pong Buffer Pointers to the EVEN Buffer Descriptor (BD) banks

0 = Ping-Pong Buffer Pointers not being reset

bit 5 SE0: Live Single-Ended Zero Flag bit

1 = Single-ended zero active on the USB bus

0 = No single-ended zero detected

bit 4 **PKTDIS:** Packet Transfer Disable bit

1 = SIE token and packet processing disabled, automatically set when a SETUP token is received

0 = SIE token and packet processing enabled

bit 3 USBEN: USB Module Enable bit

1 = USB module and supporting circuitry enabled (device attached)0 = USB module and supporting circuitry disabled (device detached)

bit 2 RESUME: Resume Signaling Enable bit

1 = Resume signaling activated

0 = Resume signaling disabled

bit 1 SUSPND: Suspend USB bit

1 = USB module and supporting circuitry in Power Conserve mode, SIE clock inactive

0 = USB module and supporting circuitry in normal operation, SIE clock clocked at the configured rate

bit 0 **Unimplemented**: Read as '0'

The PPBRST bit (UCON<6>) controls the Reset status when Double-Buffering mode (ping-pong buffering) is used. When the PPBRST bit is set, all Ping-Pong Buffer Pointers are set to the EVEN buffers. PPBRST has to be cleared by firmware. This bit is ignored in buffering modes not using ping-pong buffering.

The PKTDIS bit (UCON<4>) is a flag indicating that the SIE has disabled packet transmission and reception. This bit is set by the SIE when a SETUP token is received to allow setup processing. This bit cannot be set by the microcontroller, only cleared; clearing it allows the SIE to continue transmission and/or reception. Any pending events within the Buffer Descriptor Table will still be available, indicated within the USTAT register's FIFO buffer.

The RESUME bit (UCON<2>) allows the peripheral to perform a remote wake-up by executing Resume signaling. To generate a valid remote wake-up, firmware must set RESUME for 10 ms and then clear the bit. For more information on Resume signaling, see Sections 7.1.7.5, 11.4.4 and 11.9 in the USB 2.0 Specification.

The SUSPND bit (UCON<1>) places the module and supporting circuitry (i.e., voltage regulator) in a low-power mode. The input clock to the SIE is also disabled. This bit should be set by the software in response to an IDLEIF interrupt. It should be reset by the microcontroller firmware after an ACTVIF interrupt is observed. When this bit is active, the device remains attached to the bus but the transceiver outputs remain Idle. The voltage on the VUSB pin may vary depending on the value of this bit. Setting this bit before a IDLEIF request will result in unpredictable bus behavior.

Note: While in Suspend mode, a typical bus powered USB device is limited to 500 μ A of current. This is the complete current drawn by the PIC microcontroller and its supporting circuitry. Care should be taken to assure minimum current draw when the device enters Suspend mode.

14.2.2 USB CONFIGURATION REGISTER (UCFG)

Prior to communicating over USB, the module's associated internal and/or external hardware must be configured. Most of the configuration is performed with the UCFG register (Register 14-2). The separate USB voltage regulator (see **Section 14.2.2.8 "Internal Regulator"**) is controlled through the Configuration registers.

The UFCG register contains most of the bits that control the system level behavior of the USB module. These include:

- · Bus Speed (full speed versus low speed)
- · On-Chip Transceiver Enable
- · Ping-Pong Buffer Usage

The UCFG register also contains two bits which aid in module testing, debugging and USB certifications. These bits control output enable state monitoring and eye pattern generation.

Note: The USB speed, transceiver and pull-up should only be configured during the module setup phase. It is not recommended to switch these settings while the module is enabled.

14.2.2.1 Internal Transceiver

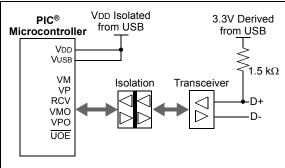
The USB peripheral has a built-in, USB 2.0, full-speed and low-speed compliant transceiver, internally connected to the SIE. This feature is useful for low-cost, single chip applications. The UTRDIS bit (UCFG<3>) controls the transceiver; it is enabled by default (UTRDIS = 0). The FSEN bit (UCFG<2>) controls the transceiver speed; setting the bit enables full-speed operation. The on-chip USB pull-up resistors are controlled by the UPUEN bit (UCFG<4>). They can only be selected when the on-chip transceiver is enabled.

The USB specification requires 3.3V operation for communications; however, the rest of the chip may be running at a higher voltage. Thus, the transceiver is supplied power from a separate source, VUSB.

14.2.2.2 External Transceiver

This module provides support for use with an off-chip transceiver. The off-chip transceiver is intended for applications where physical conditions dictate the location of the transceiver to be away from the SIE. For example, applications that require isolation from the USB could use an external transceiver through some isolation to the microcontroller's SIE (Figure 14-2). External transceiver operation is enabled by setting the UTRDIS bit.

FIGURE 14-2: TYPICAL EXTERNAL TRANSCEIVER WITH ISOLATION



Note: The above setting shows a simplified schematic for a full-speed configuration using an external transceiver with isolation.

REGISTER 14-2: UCFG: USB CONFIGURATION REGISTER

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UTEYE	UOEMON ⁽¹⁾	_	UPUEN ^(2,3)	UTRDIS ⁽²⁾	FSEN ⁽²⁾	PPB1	PPB0
bit 7			•				bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 UTEYE: USB Eye Pattern Test Enable bit

1 = Eye pattern test enabled0 = Eye pattern test disabled

bit 6 **UOEMON:** USB \overline{OE} Monitor Enable bit⁽¹⁾

1 = UOE signal active; it indicates intervals during which the D+/D- lines are driving

 $0 = \overline{\mathsf{UOE}}$ signal inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **UPUEN:** USB On-Chip Pull-up Enable bit^(2,3)

1 = On-chip pull-up enabled (pull-up on D+ with FSEN = 1 or D- with FSEN = 0)

0 = On-chip pull-up disabled

bit 3 UTRDIS: On-Chip Transceiver Disable bit⁽²⁾

1 = On-chip transceiver disabled; digital transceiver interface enabled

0 = On-chip transceiver active

bit 2 **FSEN:** Full-Speed Enable bit⁽²⁾

1 = Full-speed device: controls transceiver edge rates; requires input clock at 48 MHz

0 = Low-speed device: controls transceiver edge rates; requires input clock at 6 MHz

bit 1-0 **PPB1:PPB0:** Ping-Pong Buffers Configuration bits

11 = Enabled for all endpoints except Endpoint 0

10 = EVEN/ODD ping-pong buffers enabled for all endpoints

01 = EVEN/ODD ping-pong buffer enabled for OUT Endpoint 0

00 = EVEN/ODD ping-pong buffers disabled

Note 1: If UTRDIS is set, the UOE signal will be active independent of the UOEMON bit setting.

2: The UPUEN, UTRDIS and FSEN bits should never be changed while the USB module is enabled. These values must be preconfigured prior to enabling the module.

3: This bit is only valid when the on-chip transceiver is active (UTRDIS = 0); otherwise, it is ignored.

There are 6 signals from the module to communicate with and control an external transceiver:

- · VM: Input from the single-ended D- line
- VP: Input from the single-ended D+ line
- RCV: Input from the differential receiver
- VMO: Output to the differential line driver
- · VPO: Output to the differential line driver
- UOE: Output enable

The VPO and VMO signals are outputs from the SIE to the external transceiver. The RCV signal is the output from the external transceiver to the SIE; it represents the differential signals from the serial bus translated into a single pulse train. The VM and VP signals are used to report conditions on the serial bus to the SIE that can't be captured with the RCV signal. The combinations of states of these signals and their interpretation are listed in Table 14-1 and Table 14-2.

TABLE 14-1: DIFFERENTIAL OUTPUTS TO TRANSCEIVER

VPO	VMO	Bus State
0	0	Single-Ended Zero
0	1	Differential '0'
1	0	Differential '1'
1	1	Illegal Condition

TABLE 14-2: SINGLE-ENDED INPUTS FROM TRANSCEIVER

VP	VM	Bus State				
0	0	Single-Ended Zero				
0	1	Low Speed				
1	0	High Speed				
1	1	Error				

The UOE signal toggles the state of the external transceiver. This line is pulled low by the device to enable the transmission of data from the SIE to an external device.

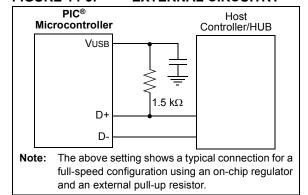
14.2.2.3 Internal Pull-up Resistors

The PIC18F2450/4450 devices have built-in pull-up resistors designed to meet the requirements for low-speed and full-speed USB. The UPUEN bit (UCFG<4>) enables the internal pull-ups. Figure 14-1 shows the pull-ups and their control.

14.2.2.4 Pull-up Resistors

The PIC18F2450/4450 devices require an external pull-up resistor to meet the requirements for low-speed and full-speed USB. Either an external 3.3V supply or the VUSB pin may be used to pull up D+ or D-. The pull-up resistor must be 1.5 k Ω (±5%) as required by the USB specifications. Figure 14-3 shows an example with the VUSB pin.

FIGURE 14-3: EXTERNAL CIRCUITRY



14.2.2.5 Ping-Pong Buffer Configuration

The usage of ping-pong buffers is configured using the PPB1:PPB0 bits. Refer to **Section 14.4.4 "Ping-Pong Buffering"** for a complete explanation of the ping-pong buffers.

14.2.2.6 USB Output Enable Monitor

The USB $\overline{\text{OE}}$ monitor provides indication as to whether the SIE is listening to the bus or actively driving the bus. This is enabled by default when using an external transceiver or when UCFG<6> = 1.

The USB $\overline{\text{OE}}$ monitoring is useful for initial system debugging, as well as scope triggering during eye pattern generation tests.

14.2.2.7 Eve Pattern Test Enable

An automatic eye pattern test can be generated by the module when the UCFG<7> bit is set. The eye pattern output will be observable based on module settings, meaning that the user is first responsible for configuring the SIE clock settings, pull-up resistor and Transceiver mode. In addition, the module has to be enabled.

Once UTEYE is set, the module emulates a switch from a receive to transmit state and will start transmitting a J-K-J-K bit sequence (K-J-K-J for full speed). The sequence will be repeated indefinitely while the Eye Pattern Test mode is enabled.

Note that this bit should never be set while the module is connected to an actual USB system. This test mode is intended for board verification to aid with USB certification tests. It is intended to show a system developer the noise integrity of the USB signals which can be affected by board traces, impedance mismatches and proximity to other system components. It does not properly test the transition from a receive to a transmit state. Although the eye pattern is not meant to replace the more complex USB certification test, it should aid during first order system debugging.

14.2.2.8 Internal Regulator

The PIC18F2450/4450 devices have a built-in 3.3V regulator to provide power to the internal transceiver and provide a source for the external pull-ups. An external 220 nF (±20%) capacitor is required for stability.

Note: The drive from VUSB is sufficient to only drive an external pull-up in addition to the internal transceiver.

The regulator is disabled by default and can be enabled through the VREGEN Configuration bit. When enabled, the voltage is visible on pin Vusb. When the regulator is disabled, a 3.3V source must be provided through the Vusb pin for the internal transceiver. If the internal transceiver is disabled, Vusb is not used.

- **Note 1:** Do not enable the internal regulator if an external regulator is connected to VUSB.
 - 2: VDD must be greater than or equal to VUSB at all times, even with the regulator disabled.

14.2.3 USB STATUS REGISTER (USTAT)

The USB Status register reports the transaction status within the SIE. When the SIE issues a USB transfer complete interrupt, USTAT should be read to determine the status of the transfer. USTAT contains the transfer endpoint number, direction and Ping-Pong Buffer Pointer value (if used).

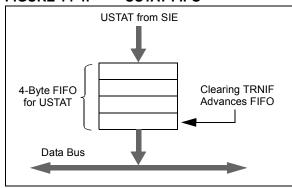
Note: The data in the USB Status register is valid only when the TRNIF interrupt flag is asserted.

The USTAT register is actually a read window into a four-byte status FIFO, maintained by the SIE. It allows the microcontroller to process one transfer while the SIE processes additional endpoints (Figure 14-4). When the SIE completes using a buffer for reading or writing data, it updates the USTAT register. If another USB transfer is performed before a transaction complete interrupt is serviced, the SIE will store the status of the next transfer into the status FIFO.

Clearing the transfer complete flag bit, TRNIF, causes the SIE to advance the FIFO. If the next data in the FIFO holding register is valid, the SIE will reassert the interrupt within 6 Tcy of clearing TRNIF. If no additional data is present, TRNIF will remain clear; USTAT data will no longer be reliable.

Note: If an endpoint request is received while the USTAT FIFO is full, the SIE will automatically issue a NAK back to the host.

FIGURE 14-4: USTAT FIFO



REGISTER 14-3: USTAT: USB STATUS REGISTER

U-0	R-x	R-x	R-x	R-x	R-x	R-x	U-0
_	ENDP3	ENDP2	ENDP1	ENDP0	DIR	PPBI ⁽¹⁾	_
bit 7			•			•	bit 0

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **ENDP3:ENDP0:** Encoded Number of Last Endpoint Activity bits

(represents the number of the BDT updated by the last USB transfer)

1111 = Endpoint 15 1110 = Endpoint 14

. . . .

0001 = Endpoint 1 0000 = Endpoint 0

bit 2 DIR: Last BD Direction Indicator bit

1 = The last transaction was an IN token

0 = The last transaction was an OUT or SETUP token

bit 1 **PPBI:** Ping-Pong BD Pointer Indicator bit⁽¹⁾

1 = The last transaction was to the ODD BD bank 0 = The last transaction was to the EVEN BD bank

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is only valid for endpoints with available EVEN and ODD BD registers.

14.2.4 **USB ENDPOINT CONTROL**

Each of the 16 possible bidirectional endpoints has its own independent control register, UEPn (where 'n' represents the endpoint number). Each register has an identical complement of control bits. The prototype is shown in Register 14-4.

The EPHSHK bit (UEPn<4>) controls handshaking for the endpoint; setting this bit enables USB handshaking. Typically, this bit is always set except when using isochronous endpoints.

The EPCONDIS bit (UEPn<3>) is used to enable or disable USB control operations (SETUP) through the endpoint. Clearing this bit enables SETUP transactions. Note that the corresponding EPINEN and EPOUTEN bits must be set to enable IN and OUT

transactions. For Endpoint 0, this bit should always be cleared since the USB specifications identify Endpoint 0 as the default control endpoint.

The EPOUTEN bit (UEPn<2>) is used to enable or disable USB OUT transactions from the host. Setting this bit enables OUT transactions. Similarly, the EPINEN bit (UEPn<1>) enables or disables USB IN transactions from the host.

The EPSTALL bit (UEPn<0>) is used to indicate a STALL condition for the endpoint. If a STALL is issued on a particular endpoint, the EPSTALL bit for that endpoint pair will be set by the SIE. This bit remains set until it is cleared through firmware, or until the SIE is reset.

REGISTER 14-4: UEPn: USB ENDPOINT n CONTROL REGISTER (UEP0 THROUGH UEP15)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL ⁽¹⁾
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-5	Unimplemented: Read as '0'
bit 4	EPHSHK: Endpoint Handshake Enable bit
	1 = Endpoint handshake enabled
	0 = Endpoint handshake disabled (typically used for isochronous endpoints)
bit 3	EPCONDIS: Bidirectional Endpoint Control bit
	If EPOUTEN = 1 and EPINEN = 1:
	1 = Disable Endpoint n from control transfers; only IN and OUT transfers allowed
	0 = Enable Endpoint n for control (SETUP) transfers; IN and OUT transfers also a

s also allowed **EPOUTEN:** Endpoint Output Enable bit

bit 2 1 = Endpoint n output enabled

0 = Endpoint n output disabled

bit 1 **EPINEN:** Endpoint Input Enable bit

> 1 = Endpoint n input enabled 0 = Endpoint n input disabled

bit 0 **EPSTALL:** Endpoint Stall Indicator bit

1 = Endpoint n has issued one or more STALL packets

0 = Endpoint n has not issued any STALL packets

14.2.5 USB ADDRESS REGISTER (UADDR)

The USB Address register contains the unique USB address that the peripheral will decode when active. UADDR is reset to 00h when a USB Reset is received, indicated by URSTIF, or when a Reset is received from the microcontroller. The USB address must be written by the microcontroller during the USB setup phase (enumeration) as part of the Microchip USB firmware support.

14.2.6 USB FRAME NUMBER REGISTERS (UFRMH:UFRML)

The Frame Number registers contain the 11-bit frame number. The low-order byte is contained in UFRML, while the three high-order bits are contained in UFRMH. The register pair is updated with the current frame number whenever a SOF token is received. For the microcontroller, these registers are read-only. The Frame Number register is primarily used for isochronous transfers.

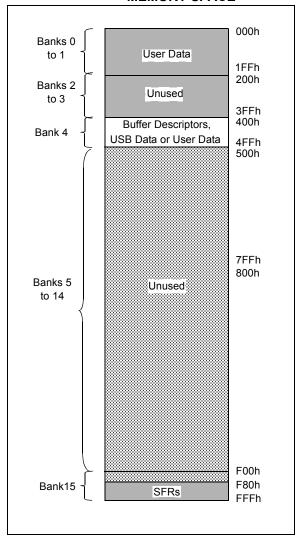
14.3 **USB RAM**

USB data moves between the microcontroller core and the SIE through a memory space known as the USB RAM. This is a special dual port memory that is mapped into the normal data memory space in Bank 4 (400h to 4FFh) for a total of 256 bytes (Figure 14-5).

Some portion of Bank 4 (400h through 4FFh) is used specifically for endpoint buffer control, while the remaining portion is available for USB data. Depending on the type of buffering being used, all but 8 bytes of Bank 4 may also be available for use as USB buffer space.

Although USB RAM is available to the microcontroller as data memory, the sections that are being accessed by the SIE should not be accessed by the microcontroller. A semaphore mechanism is used to determine the access to a particular buffer at any given time. This is discussed in **Section 14.4.1.1 "Buffer Ownership"**.

FIGURE 14-5: IMPLEMENTATION OF USB RAM IN DATA MEMORY SPACE



14.4 Buffer Descriptors and the Buffer Descriptor Table

The registers in Bank 4 are used specifically for endpoint buffer control in a structure known as the Buffer Descriptor Table (BDT). This provides a flexible method for users to construct and control endpoint buffers of various lengths and configuration.

The BDT is composed of Buffer Descriptors (BD) which are used to define and control the actual buffers in the USB RAM space. Each BD, in turn, consists of four registers, where n represents one of the 64 possible BDs (range of 0 to 63):

BDnSTAT: BD Status register
BDnCNT: BD Byte Count register
BDnADRL: BD Address Low register
BDnADRH: BD Address High register

BDs always occur as a four-byte block in the sequence, BDnSTAT:BDnCNT:BDnADRL:BDnADRH. The address of BDnSTAT is always an offset of (4n-1) (in hexadecimal) from 400h, with n being the buffer descriptor number.

Depending on the buffering configuration used (**Section 14.4.4 "Ping-Pong Buffering"**), there are up to 32, 33 or 64 sets of buffer descriptors. At a minimum, the BDT must be at least 8 bytes long. This is because the USB specification mandates that every device must have Endpoint 0 with both input and output for initial setup. Depending on the endpoint and buffering configuration, the BDT can be as long as 256 bytes.

Although they can be thought of as Special Function Registers, the Buffer Descriptor Status and Address registers are not hardware mapped, as conventional microcontroller SFRs in Bank 15 are. If the endpoint corresponding to a particular BD is not enabled, its registers are not used. Instead of appearing as unimplemented addresses, however, they appear as available RAM. Only when an endpoint is enabled by setting the UEPn<1> bit does the memory at those addresses become functional as BD registers. As with any address in the data memory space, the BD registers have an indeterminate value on any device Reset.

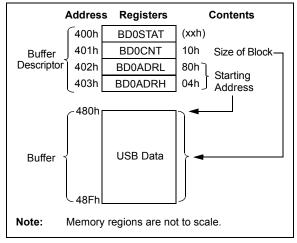
A total of 256 bytes of address space in Bank 4 is available for BDT and USB data RAM. In Ping-Pong Buffer mode, all the 16 bidirectional endpoints can not be implemented where BDT itself can be as long as 256 bytes. In the majority of USB applications, few endpoints are required to be implemented. Hence, a small portion of the 256 bytes will be used for BDT and the rest can be used for USB data.

An example of a BD for a 16-byte buffer, starting at 480h, is shown in Figure 14-6. A particular set of BD registers is only valid if the corresponding endpoint has been enabled using the UEPn register. All BD registers are available in USB RAM. The BD for each endpoint should be set up prior to enabling the endpoint.

14.4.1 BD STATUS AND CONFIGURATION

Buffer descriptors not only define the size of an endpoint buffer, but also determine its configuration and control. Most of the configuration is done with the BD Status register, BDnSTAT. Each BD has its own unique and correspondingly numbered BDnSTAT register.

FIGURE 14-6: EXAMPLE OF A BUFFER DESCRIPTOR



Unlike other control registers, the bit configuration for the BDnSTAT register is context sensitive. There are two distinct configurations, depending on whether the microcontroller or the USB module is modifying the BD and buffer at a particular time. Only three bit definitions are shared between the two.

14.4.1.1 Buffer Ownership

Because the buffers and their BDs are shared between the CPU and the USB module, a simple semaphore mechanism is used to distinguish which is allowed to update the BD and associated buffers in memory.

This is done by using the UOWN bit (BDnSTAT<7>) as a semaphore to distinguish which is allowed to update the BD and associated buffers in memory. UOWN is the only bit that is shared between the two configurations of BDnSTAT.

When UOWN is clear, the BD entry is "owned" by the microcontroller core. When the UOWN bit is set, the BD entry and the buffer memory are "owned" by the USB peripheral. The core should not modify the BD or its corresponding data buffer during this time. Note that the microcontroller core can still read BDnSTAT while the SIE owns the buffer and vice versa.

The buffer descriptors have a different meaning based on the source of the register update. Prior to placing ownership with the USB peripheral, the user can configure the basic operation of the peripheral through the BDnSTAT bits. During this time, the byte count and buffer location registers can also be set.

When UOWN is set, the user can no longer depend on the values that were written to the BDs. From this point, the SIE updates the BDs as necessary, overwriting the original BD values. The BDnSTAT register is updated by the SIE with the token PID and the transfer count, BDnCNT, is updated.

The BDnSTAT byte of the BDT should always be the last byte updated when preparing to arm an endpoint. The SIE will clear the UOWN bit when a transaction has completed. The only exception to this is when KEN is enabled and/or BSTALL is enabled.

No hardware mechanism exists to block access when the UOWN bit is set. Thus, unexpected behavior can occur if the microcontroller attempts to modify memory when the SIE owns it. Similarly, reading such memory may produce inaccurate data until the USB peripheral returns ownership to the microcontroller.

14.4.1.2 BDnSTAT Register (CPU Mode)

When UOWN = 0, the microcontroller core owns the BD. At this point, the other seven bits of the register take on control functions.

The Data Toggle Sync Enable bit, DTSEN (BDnSTAT<3>), controls data toggle parity checking. Setting DTSEN enables data toggle synchronization by the SIE. When enabled, it checks the data packet's parity against the value of DTS (BDnSTAT<6>). If a packet arrives with an incorrect synchronization, the data will essentially be ignored. It will not be written to

the USB RAM and the USB transfer complete interrupt flag will not be set. The SIE will send an ACK token back to the host to Acknowledge receipt, however. The effects of the DTSEN bit on the SIE are summarized in Table 14-3.

The Buffer Stall bit, BSTALL (BDnSTAT<2>), provides support for control transfers, usually one-time stalls on Endpoint 0. It also provides support for the SET_FEATURE/CLEAR_FEATURE commands specified in Chapter 9 of the USB specification; typically, continuous STALLs to any endpoint other than the default control endpoint.

The BSTALL bit enables buffer stalls. Setting BSTALL causes the SIE to return a STALL token to the host if a received token would use the BD in that location. The EPSTALL bit in the corresponding UEPn control register is set and a STALL interrupt is generated when a STALL is issued to the host. The UOWN bit remains set and the BDs are not changed unless a SETUP token is received. In this case, the STALL condition is cleared and the ownership of the BD is returned to the microcontroller core.

The BD9:BD8 bits (BDnSTAT<1:0>) store the two most significant digits of the SIE byte count; the lower 8 digits are stored in the corresponding BDnCNT register. See Section 14.4.2 "BD Byte Count" for more information.

TABLE 14-3: EFFECT OF DTSEN BIT ON ODD/EVEN (DATA0/DATA1) PACKET RECEPTION

OUT Packet	ket BDnSTAT Settings		ī	Device Response after Receiving Packet				
from Host	DTSEN	DTS	Handshake	UOWN	TRNIF	BDnSTAT and USTAT Status		
DATA0	1	0	ACK	0	1	Updated		
DATA1	1	0	ACK	1	0	Not Updated		
DATA1	1	1	ACK	0	1	Updated		
DATA0	1	1	ACK	1	0	Not Updated		
Either	0	X	ACK	0	1	Updated		
Either, with error	Х	Х	NAK	1	0	Not Updated		

Legend: x = don't care

REGISTER 14-5: BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER (BD0STAT THROUGH BD63STAT), CPU MODE (DATA IS WRITTEN TO THE SIDE)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
UOWN ⁽¹⁾	DTS ⁽²⁾	(3)	(3)	DTSEN	BSTALL	BC9	BC8
bit 7		•		•			bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **UOWN:** USB Own bit⁽¹⁾

0 = The microcontroller core owns the BD and its corresponding buffer

bit 6 **DTS:** Data Toggle Synchronization bit⁽²⁾

1 = Data 1 packet 0 = Data 0 packet

bit 5-4 **Reserved:** These bits should always be programmed to '0'(3)

bit 3 DTSEN: Data Toggle Synchronization Enable bit

1 = Data toggle synchronization is enabled; data packets with incorrect Sync value will be ignored except for a SETUP transaction, which is accepted even if the data toggle bits do not match.

0 = No data toggle synchronization is performed

bit 2 BSTALL: Buffer Stall Enable bit

1 = Buffer stall enabled; STALL handshake issued if a token is received that would use the BD in the given location (UOWN bit remains set, BD value is unchanged)

0 = Buffer stall disabled

bit 1-0 BC9:BC8: Byte Count 9 and 8 bits

The byte count bits represent the number of bytes that will be transmitted for an IN token or received during an OUT token. Together with BC<7:0>, the valid byte counts are 0-1023.

Note 1: This bit must be initialized by the user to the desired value prior to enabling the USB module.

2: This bit is ignored unless DTSEN = 1.

3: If these bits are set, USB communication may not work. Hence, these bits should always be maintained as '0'.

14.4.1.3 BDnSTAT Register (SIE Mode)

When the BD and its buffer are owned by the SIE, most of the bits in BDnSTAT take on a different meaning. The configuration is shown in Register 14-6. Once UOWN is set, any data or control settings previously written there by the user will be overwritten with data from the SIE.

The BDnSTAT register is updated by the SIE with the token Packet Identifier (PID) which is stored in BDnSTAT<5:3>. The transfer count in the corresponding BDnCNT register is updated. Values that overflow the 8-bit register carry over to the two most significant digits of the count, stored in BDnSTAT<1:0>.

14.4.2 BD BYTE COUNT

The byte count represents the total number of bytes that will be transmitted during an IN transfer. After an IN transfer, the SIE will return the number of bytes sent to the host.

For an OUT transfer, the byte count represents the maximum number of bytes that can be received and stored in USB RAM. After an OUT transfer, the SIE will return the actual number of bytes received. If the number of bytes received exceeds the corresponding

byte count, the data packet will be rejected and a NAK handshake will be generated. When this happens, the byte count will not be updated.

The 10-bit byte count is distributed over two registers. The lower 8 bits of the count reside in the BDnCNT register. The upper two bits reside in BDnSTAT<1:0>. This represents a valid byte range of 0 to 1023.

14.4.3 BD ADDRESS VALIDATION

The BD Address register pair contains the starting RAM address location for the corresponding endpoint buffer. For an endpoint starting location to be valid, it must fall in the range of the USB RAM, 400h to 4FFh. No mechanism is available in hardware to validate the BD address.

If the value of the BD address does not point to an address in the USB RAM, or if it points to an address within another endpoint's buffer, data is likely to be lost or overwritten. Similarly, overlapping a receive buffer (OUT endpoint) with a BD location in use can yield unexpected results. When developing USB applications, the user may want to consider the inclusion of software-based address validation in their code.

REGISTER 14-6: BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER (BD0STAT THROUGH BD63STAT), SIE MODE (DATA RETURNED BY THE SIDE TO THE MICROCONTROLLER)

R/W-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
UOWN	_	PID3	PID2	PID1	PID0	BC9	BC8
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 UOWN: USB Own bit

1 = The SIE owns the BD and its corresponding buffer

bit 6 Reserved: Not written by the SIE bit 5-2 PID3:PID0: Packet Identifier bits

The received token PID value of the last transfer (IN, OUT or SETUP transactions only).

bit 1-0 BC9:BC8: Byte Count 9 and 8 bits

These bits are updated by the SIE to reflect the actual number of bytes received on an OUT transfer

and the actual number of bytes transmitted on an IN transfer.

14.4.4 PING-PONG BUFFERING

An endpoint is defined to have a ping-pong buffer when it has two sets of BD entries: one set for an EVEN transfer and one set for an ODD transfer. This allows the CPU to process one BD while the SIE is processing the other BD. Double-buffering BDs in this way allows for maximum throughput to/from the USB.

The USB module supports three modes of operation:

- · No ping-pong support
- Ping-pong buffer support for OUT Endpoint 0 only
- · Ping-pong buffer support for all endpoints

The ping-pong buffer settings are configured using the PPB1:PPB0 bits in the UCFG register.

The USB module keeps track of the Ping-Pong Pointer individually for each endpoint. All pointers are initially reset to the EVEN BD when the module is enabled. After the completion of a transaction (UOWN cleared

by the SIE), the pointer is toggled to the ODD BD. After the completion of the next transaction, the pointer is toggled back to the EVEN BD and so on.

The EVEN/ODD status of the last transaction is stored in the PPBI bit of the USTAT register. The user can reset all Ping-Pong Pointers to EVEN using the PPBRST bit.

Figure 14-7 shows the three different modes of operation and how USB RAM is filled with the BDs.

BDs have a fixed relationship to a particular endpoint, depending on the buffering configuration. The mapping of BDs to endpoints is detailed in Table 14-4. This relationship also means that gaps may occur in the BDT if endpoints are not enabled contiguously. This theoretically means that the BDs for disabled endpoints could be used as buffer space. In practice, users should avoid using such spaces in the BDT unless a method of validating BD addresses is implemented.

PPB1:PPB0 = 10 PPB1:PPB0 = 01 PPB1:PPB0 = 00 Ping-Pong Buffers on All EPs Ping-Pong Buffer on EP0 OUT No Ping-Pong Buffers 400h 400h 400h EP0 OUT EVEN EP0 OUT EP0 OUT EVEN Descriptor Descriptor Descriptor EP0 OUT ODD EP0 IN EP0 OUT ODD Descriptor Descriptor Descriptor EP0 IN EVEN EP1 OUT EP0 IN Descriptor Descriptor Descriptor EP1 IN EP0 IN ODD EP1 OUT Descriptor Descriptor Descriptor **EP1 OUT EVEN** FP1 IN Descriptor Descriptor FP1 OUT ODD EP15 IN Descriptor Descriptor 47Fh **EP1 IN EVEN** Descriptor EP15 IN Descriptor 483h EP1 IN ODD Descriptor Available as Available Data RAM Data RAM EP15 IN ODD Descriptor 4FFh Maximum Memory Used: 256 bytes Maximum Memory Used: 128 bytes Maximum Memory Used: 132 bytes Maximum BDs: 32 (BD0 to BD31) Maximum BDs: 64 (BD0 to BD63) Maximum BDs: 33 (BD0 to BD32) Note: Memory area not shown to scale.

FIGURE 14-7: BUFFER DESCRIPTOR TABLE MAPPING FOR BUFFERING MODES

TABLE 14-4: ASSIGNMENT OF BUFFER DESCRIPTORS FOR THE DIFFERENT BUFFERING MODES

Endpoint	BDs Assigned to Endpoint									
	Mode 0 (No Ping-Pong)			de 1 on EP0 OUT)	Mode 2 (Ping-Pong on all EPs)					
	Out	ln	Out	ln	Out	In				
0	0	1	0 (E), 1 (O)	2	0 (E), 1 (O)	2 (E), 3 (O)				
1	2	3	3	4	4 (E), 5 (O)	6 (E), 7 (O)				
2	4	5	5	6	8 (E), 9 (O)	10 (E), 11 (O)				
3	6	7	7	8	12 (E), 13 (O)	14 (E), 15 (O)				
4	8	9	9	10	16 (E), 17 (O)	18 (E), 19 (O)				
5	10	11	11	12	20 (E), 21 (O)	22 (E), 23 (O)				
6	12	13	13	14	24 (E), 25 (O)	26 (E), 27 (O)				
7	14	15	15	16	28 (E), 29 (O)	30 (E), 31 (O)				
8	16	17	17	18	32 (E), 33 (O)	34 (E), 35 (O)				
9	18	19	19	20	36 (E), 37 (O)	38 (E), 39 (O)				
10	20	21	21	22	40 (E), 41 (O)	42 (E), 43 (O)				
11	22	23	23	24	44 (E), 45 (O)	46 (E), 47 (O)				
12	24	25	25	26	48 (E), 49 (O)	50 (E), 51 (O)				
13	26	27	27	28	52 (E), 53 (O)	54 (E), 55 (O)				
14	28	29	29	30	56 (E), 57 (O)	58 (E), 59 (O)				
15	30	31	31	32	60 (E), 61 (O)	62 (E), 63 (O)				

Legend: (E) = EVEN transaction buffer, (O) = ODD transaction buffer

TABLE 14-5: SUMMARY OF USB BUFFER DESCRIPTOR TABLE REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
BDnSTAT ⁽¹⁾	UOWN	DTS ⁽⁴⁾	PID3 ⁽²⁾	PID2 ⁽²⁾	PID1 ⁽²⁾ DTSEN ⁽³⁾	PID0 ⁽²⁾ BSTALL ⁽³⁾	BC9	BC8			
BDnCNT ⁽¹⁾	Byte Count										
BDnADRL ⁽¹⁾	Buffer Address Low										
BDnADRH ⁽¹⁾	Buffer Address High										

- **Note 1:** For buffer descriptor registers, n may have a value of 0 to 63. For the sake of brevity, all 64 registers are shown as one generic prototype. All registers have indeterminate Reset values (xxxx xxxx).
 - 2: Bits 5 through 2 of the BDnSTAT register are used by the SIE to return PID3:PID0 values once the register is turned over to the SIE (UOWN bit is set). Once the registers have been under SIE control, the values written for DTSEN and BSTALL are no longer valid.
 - **3:** Prior to turning the buffer descriptor over to the SIE (UOWN bit is cleared), bits 3 and 2 of the BDnSTAT register are used to configure the DTSEN and BSTALL settings.
 - **4:** This bit is ignored unless DTSEN = 1.

14.5 USB Interrupts

The USB module can generate multiple interrupt conditions. To accommodate all of these interrupt sources, the module is provided with its own interrupt logic structure, similar to that of the microcontroller. USB interrupts are enabled with one set of control registers and trapped with a separate set of flag registers. All sources are funneled into a single USB interrupt request, USBIF (PIR2<5>), in the microcontroller's interrupt logic.

Figure 14-8 shows the interrupt logic for the USB module. There are two layers of interrupt registers in the USB module. The top level consists of overall USB status interrupts; these are enabled and flagged in the UIE and UIR registers, respectively. The second level consists of USB error conditions, which are enabled and flagged in the UEIR and UEIE registers. An interrupt condition in any of these triggers a USB Error Interrupt Flag (UERRIF) in the top level.

Interrupts may be used to trap routine events in a USB transaction. Figure 14-9 shows some common events within a USB frame and their corresponding interrupts.

FIGURE 14-8: USB INTERRUPT LOGIC FUNNEL

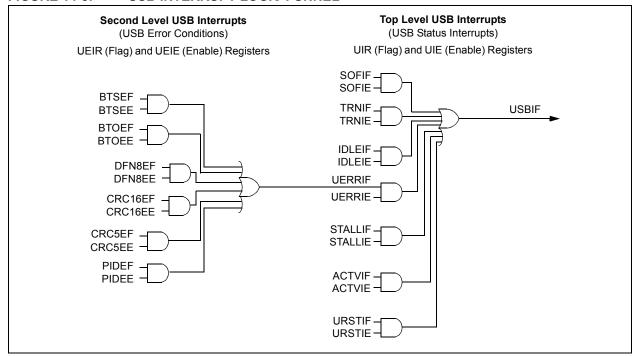
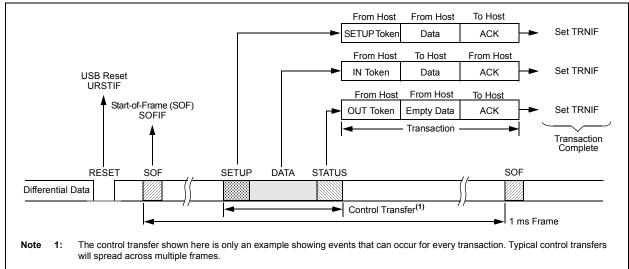


FIGURE 14-9: EXAMPLE OF A USB TRANSACTION AND INTERRUPT EVENTS



14.5.1 USB INTERRUPT STATUS REGISTER (UIR)

The USB Interrupt Status register (Register 14-7) contains the flag bits for each of the USB status interrupt sources. Each of these sources has a corresponding interrupt enable bit in the UIE register. All of the USB status flags are ORed together to generate the USBIF interrupt flag for the microcontroller's interrupt funnel.

Once an interrupt bit has been set by the SIE, it must be cleared by software by writing a '0'. The flag bits can also be set in software which can aid in firmware debugging.

When the USB module is in the Low-Power Suspend mode (UCON<1> = 1), the SIE does not get clocked. When in this state, the SIE cannot process packets, and therefore, cannot detect new interrupt conditions other than the Activity Detect Interrupt, Flag ACTVIF. The ACTVIF bit is typically used by USB firmware to detect when the microcontroller should bring the USB module out of the Low-Power Suspend mode (UCON<1> = 0).

x = Bit is unknown

REGISTER 14-7: UIR: USB INTERRUPT STATUS REGISTER

W = Writable bit

'1' = Bit is set

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0
_	SOFIF	STALLIF	IDLEIF ⁽¹⁾	TRNIF ⁽²⁾	ACTVIF ⁽³⁾	UERRIF ⁽⁴⁾	URSTIF
bit 7							bit 0

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

bit 7	Unimplemented: Poad as '0'
	Unimplemented: Read as '0'
bit 6	SOFIF: Start-of-Frame Token Interrupt bit
	1 = A Start-of-Frame token received by the SIE
	0 = No Start-of-Frame token received by the SIE
bit 5	STALLIF: A STALL Handshake Interrupt bit
	1 = A STALL handshake was sent by the SIE
	0 = A STALL handshake has not been sent
bit 4	IDLEIF: Idle Detect Interrupt bit ⁽¹⁾
	1 = Idle condition detected (constant Idle state of 3 ms or more)
	0 = No Idle condition detected
bit 3	TRNIF: Transaction Complete Interrupt bit ⁽²⁾
	1 = Processing of pending transaction is complete; read USTAT register for endpoint information
	0 = Processing of pending transaction is not complete or no transaction is pending
bit 2	ACTVIF: Bus Activity Detect Interrupt bit ⁽³⁾
	1 = Activity on the D+/D- lines was detected
	0 = No activity detected on the D+/D- lines
bit 1	UERRIF: USB Error Condition Interrupt bit ⁽⁴⁾
	1 = An unmasked error condition has occurred
	0 = No unmasked error condition has occurred.
bit 0	URSTIF: USB Reset Interrupt bit
	1 = Valid USB Reset occurred; 00h is loaded into UADDR register
	0 = No USB Reset has occurred

- **Note 1:** Once an Idle state is detected, the user may want to place the USB module in Suspend mode.
 - 2: Clearing this bit will cause the USTAT FIFO to advance (valid only for IN, OUT and SETUP tokens).
 - 3: This bit is typically unmasked only following the detection of a UIDLE interrupt event.
 - **4:** Only error conditions enabled through the UEIE register will set this bit. This bit is a status bit only and cannot be set or cleared by the user.

Legend:

R = Readable bit

-n = Value at POR

14.5.1.1 Bus Activity Detect Interrupt Bit (ACTVIF)

The ACTVIF bit cannot be cleared immediately after the USB module wakes up from Suspend or while the USB module is suspended. A few clock cycles are required to synchronize the internal hardware state machine before the ACTVIF bit can be cleared by firmware. Clearing the ACTVIF bit before the internal hardware is synchronized may not have an effect on the value of ACTVIF. Additionally, if the USB module uses the clock from the 96 MHz PLL source, then after clearing the SUSPND bit, the USB module may not be immediately operational while waiting for the 96 MHz PLL to lock. The application code should clear the ACTVIF bit as shown in Example 14-1.

Only one ACTVIF interrupt is generated when resuming from the USB bus Idle condition. If user firmware clears the ACTVIF bit, the bit will not immediately become set again, even when there is continuous bus traffic. Bus traffic must cease long enough to generate another IDLEIF condition before another ACTVIF interrupt can be generated.

EXAMPLE 14-1: CLEARING ACTVIF BIT (UIR<2>)

Assembly: BCF UCON, SUSPND LOOP: BTFSS UIR, ACTVIF BRA DONE BCF UIR, ACTVIF BRA LOOP DONE C: UCONDits.SUSPND = 0; while (UIRbits.ACTVIF) {UIRbits.ACTVIF = 0};

14.5.2 **USB INTERRUPT ENABLE** REGISTER (UIE)

Legend:

R = Readable bit

The USB Interrupt Enable register (Register 14-8) contains the enable bits for the USB status interrupt sources. Setting any of these bits will enable the respective interrupt source in the UIR register.

The values in this register only affect the propagation of an interrupt condition to the microcontroller's interrupt logic. The flag bits are still set by their interrupt conditions, allowing them to be polled and serviced without actually generating an interrupt.

x = Bit is unknown

U = Unimplemented bit, read as '0'

REGISTER 14-8: UIE: USB INTERRUPT ENABLE REGISTER

W = Writable bit

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	SOFIE	STALLIE	IDLEIE	TRNIE	ACTVIE	UERRIE	URSTIE
bit 7							bit 0

-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
bit 7 Un	implemented: Read as '0'	
bit 6 SO	FIE: Start-of-Frame Token Interrupt E	nable bit
	Start-of-Frame token interrupt enable Start-of-Frame token interrupt disable	
bit 5 ST	ALLIE: STALL Handshake Interrupt E	nable bit
	STALL interrupt enabled	
0 =	STALL interrupt disabled	
bit 4 IDI	.EIE: Idle Detect Interrupt Enable bit	
	Idle detect interrupt enabled Idle detect interrupt disabled	
bit 3 TR	NIE: Transaction Complete Interrupt E	nable bit
	Transaction interrupt enabled Transaction interrupt disabled	
bit 2 AC	TVIE: Bus Activity Detect Interrupt En	able bit
1 =	Bus activity detect interrupt enabled	
0 =	Bus activity detect interrupt disabled	
bit 1 UE	RRIE: USB Error Interrupt Enable bit	
	USB error interrupt enabled	
	USB error interrupt disabled	
bit 0 UR	STIE: USB Reset Interrupt Enable bit	
	USB Reset interrupt enabled	
0 =	USB Reset interrupt disabled	

14.5.3 USB ERROR INTERRUPT STATUS REGISTER (UEIR)

The USB Error Interrupt Status register (Register 14-9) contains the flag bits for each of the error sources within the USB peripheral. Each of these sources is controlled by a corresponding interrupt enable bit in the UEIE register. All of the USB error flags are ORed together to generate the USB Error Interrupt Flag (UERRIF) at the top level of the interrupt logic.

Each error bit is set as soon as the error condition is detected. Thus, the interrupt will typically not correspond with the end of a token being processed.

Once an interrupt bit has been set by the SIE, it must be cleared by software by writing a '0'.

REGISTER 14-9: UEIR: USB ERROR INTERRUPT STATUS REGISTER

R/C-0	U-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
BTSEF	_	_	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF
bit 7							bit 0

Legend:							
R = Read	able bit	C = Clearable bit	U = Unimplemented bit, read as '0'				
-n = Value	n = Value at POR '1' = Bit is set		'0' = Bit is cleared	x = Bit is unknown			
=		D" 0' " E					
bit 7	BTSEF:	Bit Stuff Error Flag bit					
	1 = A bit	stuff error has been detecte	d				
	0 = No b	oit stuff error					

bit 6-5 **Unimplemented:** Read as '0'

bit 4 BTOEF: Bus Turnaround Time-out Error Flag bit

1 = Bus turnaround time-out has occurred (more than 16 bit times of Idle from previous EOP elapsed)

0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit

1 = The data field was not an integral number of bytes0 = The data field was an integral number of bytes

bit 2 CRC16EF: CRC16 Failure Flag bit

1 = The CRC16 failed0 = The CRC16 passed

bit 1 CRC5EF: CRC5 Host Error Flag bit

1 = The token packet was rejected due to a CRC5 error

0 = The token packet was acceptedPIDEF: PID Check Failure Flag bit

1 = PID check failed 0 = PID check passed

bit 0

14.5.4 USB ERROR INTERRUPT ENABLE REGISTER (UEIE)

The USB Error Interrupt Enable register (Register 14-10) contains the enable bits for each of the USB error interrupt sources. Setting any of these bits will enable the respective error interrupt source in the UEIR register to propagate into the UERR bit at the top level of the interrupt logic.

Legend:

R = Readable bit

As with the UIE register, the enable bits only affect the propagation of an interrupt condition to the microcontroller's interrupt logic. The flag bits are still set by their interrupt conditions, allowing them to be polled and serviced without actually generating an interrupt.

x = Bit is unknown

REGISTER 14-10: UEIE: USB ERROR INTERRUPT ENABLE REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BTSEE	_	_	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE
bit 7							bit 0

U = Unimplemented bit, read as '0'

-n = Value at P	POR	'1' = Bit is set	'0' = Bit is cleared
bit 7	BTSEE: Bit St	uff Error Interrupt Enable bit	
	1 = Bit stuff en	ror interrupt enabled	
	0 = Bit stuff en	ror interrupt disabled	
bit 6-5	Unimplement	ed: Read as '0'	
bit 4	BTOEE: Bus 7	Turnaround Time-out Error I	nterrupt Enable bit
	1 = Bus turnar	ound time-out error interrup	t enabled
	0 = Bus turnar	ound time-out error interrup	t disabled
bit 3	DFN8EE: Data	a Field Size Error Interrupt E	nable bit
	1 = Data field	size error interrupt enabled	
	0 = Data field	size error interrupt disabled	
bit 2	CRC16EE: CF	RC16 Failure Interrupt Enabl	le bit
	1 = CRC16 fai	lure interrupt enabled	
	0 = CRC16 fai	lure interrupt disabled	
bit 1	CRC5EE: CRC	C5 Host Error Interrupt Enat	ole bit
	1 = CRC5 hos	t error interrupt enabled	
	0 = CRC5 hos	t error interrupt disabled	
bit 0	PIDEE: PID CI	heck Failure Interrupt Enabl	e bit
	1 = PID check	failure interrupt enabled	
	0 = PID check	failure interrupt disabled	

W = Writable bit

14.6 USB Power Modes

Many USB applications will likely have several different sets of power requirements and configuration. The most common power modes encountered are Bus Power Only, Self-Power Only and Dual Power with Self-Power Dominance. The most common cases are presented here.

14.6.1 BUS POWER ONLY

In Bus Power Only mode, all power for the application is drawn from the USB (Figure 14-10). This is effectively the simplest power method for the device.

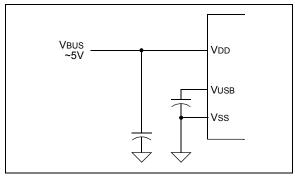
In order to meet the inrush current requirements of the USB 2.0 specifications, the total effective capacitance appearing across VBUS and ground must be no more than 10 μ F; otherwise, some kind of inrush limiting is required. For more details, see Section 7.2.4 of the USB 2.0 specification.

According to the USB 2.0 specification, all USB devices must also support a Low-Power Suspend mode. In the USB Suspend mode, devices must consume no more than 500 A (or 2.5 mA for high-powered devices that are capable of remote wake-up) from the 5V VBUS line of the USB cable.

The host signals the USB device to enter the Suspend mode by stopping all USB traffic to that device for more than 3 ms. This condition will set the IDLEIF bit in the UIR register.

During the USB Suspend mode, the D+ or D- pull-up resistor must remain active, which will consume some of the allowed suspend current: 500A/2.5 mA budget.

FIGURE 14-10: BUS POWER ONLY



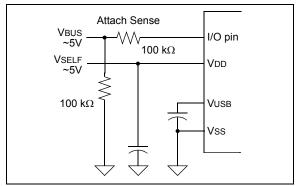
14.6.2 SELF-POWER ONLY

In Self-Power Only mode, the USB application provides its own power, with very little power being pulled from the USB. Figure 14-11 shows an example. Note that an attach indication is added to show when the USB has been connected and the host is actively powering VBUS.

In order to meet compliance specifications, the USB module (and the D+ or D- pull-up resistor) should not be enabled until the host actively drives VBUS high. One of the I/O pins may be used for this purpose.

The application should never source any current onto the 5V VBUS pin of the USB cable.

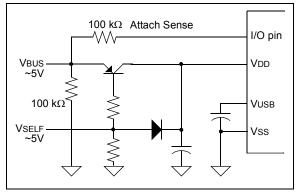
FIGURE 14-11: SELF-POWER ONLY



14.6.3 DUAL POWER WITH SELF-POWER DOMINANCE

Some applications may require a dual power option. This allows the application to use internal power primarily, but switch to power from the USB when no internal power is available. Figure 14-12 shows a simple Dual Power with Self-Power Dominance example, which automatically switches between Self-Power Only and USB Bus Power Only modes.

FIGURE 14-12: DUAL POWER EXAMPLE



Dual power devices must also meet all of the special requirements for inrush current and Suspend mode current, and must not enable the USB module until VBUS is driven high. For descriptions of those requirements, see Section 14.6.1 "Bus Power Only" and Section 14.6.2 "Self-Power Only". Additionally, dual power devices must never source current onto the 5V VUSB pin of the USB cable.

Note: Users should keep in mind the limits for devices drawing power from the USB. According to USB Specification 2.0, this cannot exceed 100 mA per low-power device or 500 mA per high-power device.

14.7 Oscillator

The USB module has specific clock requirements. For full-speed operation, the clock source must be 48 MHz. Even so, the microcontroller core and other peripherals are not required to run at that clock speed or even from the same clock source. Available clocking options are described in detail in **Section 2.3 "Oscillator Settings for USB"**.

14.8 USB Firmware and Drivers

Microchip provides a number of application-specific resources, such as USB firmware and driver support. Refer to www.microchip.com for the latest firmware and driver support.

TABLE 14-6: REGISTERS ASSOCIATED WITH USB MODULE OPERATION(1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Details on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
IPR2	OSCFIP	_	USBIP	_	_	HLVDIP	_	_	51
PIR2	OSCFIF	_	USBIF	_	_	HLVDIF	_	_	51
PIE2	OSCFIE	_	USBIE	_	_	HLVDIE	_	_	51
UCON	_	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	_	52
UCFG	UTEYE	UOEMON	_	UPUEN	UTRDIS	FSEN	PPB1	PPB0	52
USTAT	_	ENDP3	ENDP2	ENDP1	ENDP0	DIR	PPBI	_	52
UADDR	_	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	52
UFRML	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0	52
UFRMH	_	_	_	_	_	FRM10	FRM9	FRM8	52
UIR	_	SOFIF	STALLIF	IDLEIF	TRNIF	ACTVIF	UERRIF	URSTIF	52
UIE	_	SOFIE	STALLIE	IDLEIE	TRNIE	ACTVIE	UERRIE	URSTIE	52
UEIR	BTSEF	_	_	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	52
UEIE	BTSEE	_	_	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	52
UEP0	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP1	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP2	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP3	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP4	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP5	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP6	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP7	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP8	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP9	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	52
UEP10	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	51
UEP11	_	_	-	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	51
UEP12	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	51
UEP13	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	51
UEP14	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	51
UEP15	_	_	_	EPHSHK	EPCONDIS	EPOUTEN	EPINEN	EPSTALL	51

Legend:

— = unimplemented, read as '0'. Shaded cells are not used by the USB module.

Note 1: This table includes only those hardware mapped SFRs located in Bank 15 of the data memory space. The Buffer Descriptor registers, which are mapped into Bank 4 and are not true SFRs, are listed separately in Table 14-5.

14.9 Overview of USB

This section presents some of the basic USB concepts and useful information necessary to design a USB device. Although much information is provided in this section, there is a plethora of information provided within the USB specifications and class specifications. Thus, the reader is encouraged to refer to the USB specifications for more information (www.usb.org). If you are very familiar with the details of USB, then this section serves as a basic, high-level refresher of USB.

14.9.1 LAYERED FRAMEWORK

USB device functionality is structured into a layered framework graphically shown in Figure 14-13. Each level is associated with a functional level within the device. The highest layer, other than the device, is the configuration. A device may have multiple configurations. For example, a particular device may have multiple power requirements based on Self-Power Only or Bus Power Only modes.

For each configuration, there may be multiple interfaces. Each interface could support a particular mode of that configuration.

Below the interface is the endpoint(s). Data is directly moved at this level. There can be as many as 16 bidirectional endpoints. Endpoint 0 is always a control endpoint and by default, when the device is on the bus, Endpoint 0 must be available to configure the device.

14.9.2 FRAMES

Information communicated on the bus is grouped into 1 ms time slots, referred to as frames. Each frame can contain many transactions to various devices and endpoints. Figure 14-9 shows an example of a transaction within a frame.

14.9.3 TRANSFERS

There are four transfer types defined in the USB specification.

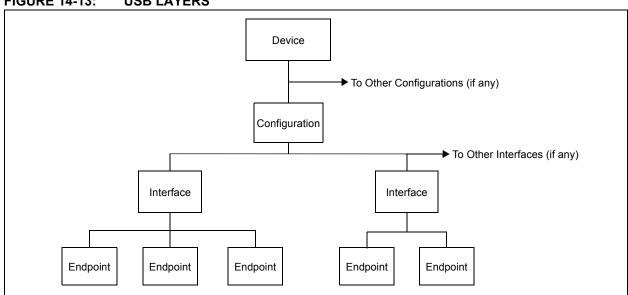
- Isochronous: This type provides a transfer method for large amounts of data (up to 1023 bytes) with timely delivery ensured; however, the data integrity is not ensured. This is good for streaming applications where small data loss is not critical, such as audio.
- Bulk: This type of transfer method allows for large amounts of data to be transferred with ensured data integrity; however, the delivery timeliness is not ensured.
- Interrupt: This type of transfer provides for ensured timely delivery for small blocks of data; plus data integrity is ensured.
- Control: This type provides for device setup control.

While full-speed devices support all transfer types, low-speed devices are limited to interrupt and control transfers only.

14.9.4 POWER

Power is available from the Universal Serial Bus. The USB specification defines the bus power requirements. Devices may either be self-powered or bus powered. Self-powered devices draw power from an external source, while bus powered devices use power supplied from the bus.





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The USB specification limits the power taken from the bus. Each device is ensured 100 mA at approximately 5V (one-unit load). Additional power may be requested, up to a maximum of 500 mA. Note that power above a one-unit load is a request and the host or hub is not obligated to provide the extra current. Thus, a device capable of consuming more than a one-unit load must be able to maintain a low-power configuration of a one-unit load or less, if necessary.

The USB specification also defines a Suspend mode. In this situation, current must be limited to 500 $\mu\text{A},$ averaged over 1 second. A device must enter a Suspend state after 3 ms of inactivity (i.e., no SOF tokens for 3 ms). A device entering Suspend mode must drop current consumption within 10 ms after Suspend mode. Likewise, when signaling a wake-up, the device must signal a wake-up within 10 ms of drawing current above the Suspend limit.

14.9.5 ENUMERATION

When the device is initially attached to the bus, the host enters an enumeration process in an attempt to identify the device. Essentially, the host interrogates the device, gathering information such as power consumption, data rates and sizes, protocol and other descriptive information; descriptors contain this information. A typical enumeration process would be as follows:

- USB Reset: Reset the device. Thus, the device is not configured and does not have an address (address 0).
- 2. Get Device Descriptor: The host requests a small portion of the device descriptor.
- 3. USB Reset: Reset the device again.
- 4. Set Address: The host assigns an address to the device.
- Get Device Descriptor: The host retrieves the device descriptor, gathering info such as manufacturer, type of device, maximum control packet size.
- Get configuration descriptors.
- 7. Get any other descriptors.
- 8. Set a configuration.

The exact enumeration process depends on the host.

14.9.6 DESCRIPTORS

There are eight different standard descriptor types of which five are most important for this device.

14.9.6.1 Device Descriptor

The device descriptor provides general information, such as manufacturer, product number, serial number, the class of the device and the number of configurations. There is only one device descriptor.

14.9.6.2 Configuration Descriptor

The configuration descriptor provides information on the power requirements of the device and how many different interfaces are supported when in this configuration. There may be more than one configuration for a device (i.e., low-power and high-power configurations).

14.9.6.3 Interface Descriptor

The interface descriptor details the number of endpoints used in this interface, as well as the class of the interface. There may be more than one interface for a configuration.

14.9.6.4 Endpoint Descriptor

The endpoint descriptor identifies the transfer type (Section 14.9.3 "Transfers") and direction, as well as some other specifics for the endpoint. There may be many endpoints in a device and endpoints may be shared in different configurations.

14.9.6.5 String Descriptor

Many of the previous descriptors reference one or more string descriptors. String descriptors provide human readable information about the layer (Section 14.9.1 "Layered Framework") they describe. Often these strings show up in the host to help the user identify the device. String descriptors are generally optional to save memory and are encoded in a unicode format.

14.9.7 BUS SPEED

Each USB device must indicate its bus presence and speed to the host. This is accomplished through a 1.5 k Ω resistor which is connected to the bus at the time of the attachment event.

Depending on the speed of the device, the resistor either pulls up the D+ or D- line to 3.3V. For a low-speed device, the pull-up resistor is connected to the D- line. For a full-speed device, the pull-up resistor is connected to the D+ line.

14.9.8 CLASS SPECIFICATIONS AND DRIVERS

USB specifications include class specifications which operating system vendors optionally support. Examples of classes include Audio, Mass Storage, Communications and Human Interface (HID). In most cases, a driver is required at the host side to 'talk' to the USB device. In custom applications, a driver may need to be developed. Fortunately, drivers are available for most common host systems for the most common classes of devices. Thus, these drivers can be reused.

15.0 ENHANCED UNIVERSAL SYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI.) The USART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers. It can also be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs and so on.

The Enhanced Universal Synchronous Receiver Transmitter (EUSART) module implements additional features, including Automatic Baud Rate Detection (ABD) and calibration, automatic wake-up on Sync Break reception and 12-bit Break character transmit. These features make it ideally suited for use in Local Interconnect Network bus (LIN bus) systems.

The EUSART can be configured in the following modes:

- · Asynchronous (full-duplex) with:
 - Auto-wake-up on character reception
 - Auto-baud calibration
 - 12-bit Break character transmission
- Synchronous Master (half-duplex) with selectable clock polarity
- Synchronous Slave (half-duplex) with selectable clock polarity

The pins of the Enhanced USART are multiplexed with PORTC. In order to configure RC6/TX/CK and RC7/RX/DT as an EUSART:

- bit SPEN (RCSTA<7>) must be set (= 1)
- bit TRISC<7> must be set (= 1)
- bit TRISC<6> must be cleared (= 0) for Asynchronous and Synchronous Master modes or set (= 1) for Synchronous Slave mode

Note: The EUSART control will automatically reconfigure the pin from input to output as needed.

The operation of the Enhanced USART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- · Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These are detailed on the following pages in Register 15-1, Register 15-2 and Register 15-3, respectively.

REGISTER 15-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN ⁽¹⁾	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 CSRC: Clock Source Select bit

Asynchronous mode:

Don't care.

Synchronous mode:

1 = Master mode (clock generated internally from BRG)

0 = Slave mode (clock from external source)

bit 6 TX9: 9-Bit Transmit Enable bit

1 = Selects 9-bit transmission0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit⁽¹⁾

1 = Transmit enabled0 = Transmit disabled

bit 4 SYNC: EUSART Mode Select bit

1 = Synchronous mode0 = Asynchronous mode

bit 3 SENDB: Send Break Character bit

Asynchronous mode:

1 = Send Sync Break on next transmission (cleared by hardware upon completion)

0 = Sync Break transmission completed

Synchronous mode:

Don't care.

bit 2 BRGH: High Baud Rate Select bit

Asynchronous mode:

1 = High speed

0 = Low speed

Synchronous mode:

Unused in this mode.

bit 1 TRMT: Transmit Shift Register Status bit

1 = TSR empty 0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data

Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode with the exception that SREN has no effect in Synchronous Slave mode.

REGISTER 15-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 SPEN: Serial Port Enable bit

1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)

0 = Serial port disabled (held in Reset)

bit 6 **RX9:** 9-Bit Receive Enable bit

1 = Selects 9-bit reception 0 = Selects 8-bit reception

bit 5 SREN: Single Receive Enable bit

Asynchronous mode:

Don't care.

Synchronous mode – Master:

1 = Enables single receive

0 = Disables single receive

This bit is cleared after reception is complete.

Synchronous mode - Slave:

Don't care.

bit 4 CREN: Continuous Receive Enable bit

Asynchronous mode:

1 = Enables receiver

0 = Disables receiver

Synchronous mode:

1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)

0 = Disables continuous receive

bit 3 ADDEN: Address Detect Enable bit

Asynchronous mode 9-bit (RX9 = 1):

1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set

0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit

Asynchronous mode 8-bit (RX9 = 0):

Don't care.

bit 2 FERR: Framing Error bit

1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)

0 = No framing error

bit 1 **OERR:** Overrun Error bit

1 = Overrun error (can be cleared by clearing bit CREN)

0 = No overrun error

bit 0 **RX9D**: 9th bit of Received Data

This can be address/data bit or a parity bit and must be calculated by user firmware.

REGISTER 15-3: BAUDCON: BAUD RATE CONTROL REGISTER

R/W-0	R-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 ABDOVF: Auto-Baud Acquisition Rollover Status bit

1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)

0 = No BRG rollover has occurred

bit 6 RCIDL: Receive Operation Idle Status bit

1 = Receive operation is Idle0 = Receive operation is active

bit 5 **Unimplemented:** Read as '0'

bit 4 SCKP: Synchronous Clock Polarity Select bit

Asynchronous mode: Unused in this mode. Synchronous mode:

1 = Idle state for clock (CK) is a high level 0 = Idle state for clock (CK) is a low level

bit 3 BRG16: 16-Bit Baud Rate Register Enable bit

1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG

0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode), SPBRGH value ignored

bit 2 Unimplemented: Read as '0' bit 1 WUE: Wake-up Enable bit

Asynchronous mode:

1 = EUSART will continue to sample the RX pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge

0 = RX pin not monitored or rising edge detected

Synchronous mode: Unused in this mode.

bit 0 ABDEN: Auto-Baud Detect Enable bit

Asynchronous mode:

1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.

0 = Baud rate measurement disabled or completed

Synchronous mode:

Unused in this mode.

15.1 Baud Rate Generator (BRG)

The BRG is a dedicated, 8-bit or 16-bit generator that supports both the Asynchronous and Synchronous modes of the EUSART. By default, the BRG operates in 8-bit mode. Setting the BRG16 bit (BAUDCON<3>) selects 16-bit mode.

The SPBRGH:SPBRG register pair controls the period of a free-running timer. In Asynchronous mode, bits BRGH (TXSTA<2>) and BRG16 (BAUDCON<3>) also control the baud rate. In Synchronous mode, BRGH is ignored. Table 15-1 shows the formula for computation of the baud rate for different EUSART modes which only apply in Master mode (internally generated clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRGH:SPBRG registers can be calculated using the formulas in Table 15-1. From this, the error in baud rate can be determined. An example calculation is shown in Example 15-1. Typical baud rates and error values for the various Asynchronous modes are shown in Table 15-2. It may be advantageous to use

the high baud rate (BRGH = 1) or the 16-bit BRG to reduce the baud rate error, or achieve a slow baud rate for a fast oscillator frequency.

Writing a new value to the SPBRGH:SPBRG registers causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

15.1.1 OPERATION IN POWER-MANAGED MODES

The device clock is used to generate the desired baud rate. When one of the power-managed modes is entered, the new clock source may be operating at a different frequency. This may require an adjustment to the value in the SPBRG register pair.

15.1.2 SAMPLING

The data on the RX pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

TABLE 15-1: BAUD RATE FORMULAS

C	onfiguration B	its	DDC/EUCADT Mode	Baud Rate Formula		
SYNC	BRG16	BRGH	BRG/EUSART Mode	Baud Rate Formula		
0	0	0	8-Bit/Asynchronous	Fosc/[64 (n + 1)]		
0	0	1	8-Bit/Asynchronous	F000/[16 (n + 1)]		
0	1	0	16-Bit/Asynchronous	Fosc/[16 (n + 1)]		
0	1	1	16-Bit/Asynchronous			
1	0	х	8-Bit/Synchronous	Fosc/[4 (n + 1)]		
1	1	Х	16-Bit/Synchronous			

Legend: x = Don't care, n = Value of SPBRGH:SPBRG register pair

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EXAMPLE 15-1: CALCULATING BAUD RATE ERROR

For a device with Fosc of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

Desired Baud Rate = Fosc/(64 ([SPBRGH:SPBRG] + 1)

Solving for SPBRGH:SPBRG:

X = ((Fosc/Desired Baud Rate)/64) - 1

= ((16000000/9600)/64) - 1

= [25.042] = 25

Calculated Baud Rate = 16000000/(64(25+1))

= 9615

Error = (Calculated Baud Rate – Desired Baud Rate)/Desired Baud Rate

= (9615 - 9600)/9600 = 0.16%

TABLE 15-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51
SPBRGH	EUSART Baud Rate Generator Register High Byte								50
SPBRG	EUSART B	aud Rate C	Senerator R	egister Low	Byte				50

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the BRG.

TABLE 15-3: BAUD RATES FOR ASYNCHRONOUS MODES

					SYNC	= 0, BRGH	I = 0, BRG	316 = 0					
BAUD RATE	Fosc	= 40.000) MHz	Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fos	Fosc = 8.000 MHz		
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
0.3	_	_	_	_	_	_	_	_	_	_	_	_	
1.2	_	_	_	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103	
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51	
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12	
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	_	_	_	
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	_	_	_	
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	_	_	_	

		SYNC = 0, BRGH = 0, BRG16 = 0												
BAUD RATE	Fos	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz							
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)					
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51					
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12					
2.4	2.404	0.16	25	2.403	-0.16	12	_	_	_					
9.6	8.929	-6.99	6	_	_	_	_	_	_					
19.2	20.833	8.51	2	_	_	_	_	_	_					
57.6	62.500	8.51	0	_	_	_	_	_	_					
115.2	62.500	-45.75	0	_	_	_	_	_	_					

					SYNC	= 0, BRGH	l = 1, BRG	16 = 0				
BAUD RATE	Fosc	= 40.000) MHz	Fosc = 20.000 MHz			Fosc	= 10.000) MHz	Fosc = 8.000 MHz		
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	_	_	_	_	_	_	_	_	_	_	_	_
1.2	_	_	_	_	_	_	_	_	_	_	_	_
2.4	_	_	_	_	_	_	2.441	1.73	255	2.403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	_	_	_

			s	YNC = 0, E	BRGH = 1	, BRG16 =	0			
BAUD	Fosc	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz			
RATE (K)	Actual Rate (K)		SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
0.3	_	_	_	1	_	_	0.300	-0.16	207	
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51	
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25	
9.6	9.615	0.16	25	9.615	-0.16	12	_	_	_	
19.2	19.231	0.16	12	_	_	_	_	_	_	
57.6	62.500	8.51	3	_	_	_	_	_	_	
115.2	125.000	8.51	1	-	_	_	_	_	_	

TABLE 15-3: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

					SYNC	= 0, BRGH	l = 0, BRG	16 = 1				
BAUD RATE	Fosc	= 40.000) MHz	Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)									
0.3	0.300	0.00	8332	0.300	0.02	4165	0.300	0.02	2082	0.300	-0.04	1665
1.2	1.200	0.02	2082	1.200	-0.03	1041	1.200	-0.03	520	1.201	-0.16	415
2.4	2.402	0.06	1040	2.399	-0.03	520	2.404	0.16	259	2.403	-0.16	207
9.6	9.615	0.16	259	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4		_	_

		SYNC = 0, BRGH = 0, BRG16 = 1												
BAUD	Fosc	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz							
RATE (K)	Actual % Rate Error (K) 0.300 0.04		SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)					
0.3	0.300	0.04	832	0.300	-0.16	415	0.300	-0.16	207					
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51					
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25					
9.6	9.615	0.16	25	9.615	-0.16	12	_	_	_					
19.2	19.231	0.16	12	_	_	_	_	_	_					
57.6	62.500	8.51	3	_	_	_	_	_	_					
115.2	125.000	8.51	1	_	_	_	_	_	_					

				SYNC = 0,	, BRGH =	= 1, BRG16	= 1 or SY	NC = 1,	BRG16 = 1	•	•	
BAUD	Fosc	= 40.000) MHz	Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
RATE (K)) Actual Rate (K) E		SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.00	33332	0.300	0.00	16665	0.300	0.00	8332	0.300	-0.01	6665
1.2	1.200	0.00	8332	1.200	0.02	4165	1.200	0.02	2082	1.200	-0.04	1665
2.4	2.400	0.02	4165	2.400	0.02	2082	2.402	0.06	1040	2.400	-0.04	832
9.6	9.606	0.06	1040	9.596	-0.03	520	9.615	0.16	259	9.615	-0.16	207
19.2	19.193	-0.03	520	19.231	0.16	259	19.231	0.16	129	19.230	-0.16	103
57.6	57.803	0.35	172	57.471	-0.22	86	58.140	0.94	42	57.142	0.79	34
115.2	114.943	-0.22	86	116.279	0.94	42	113.636	-1.36	21	117.647	-2.12	16

		SYN	IC = 0, BR	3H = 1, BF	RG16 = 1	or SYNC =	1, BRG1	6 = 1		
BAUD RATE	Fos	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz			
(K)	Actual Rate (K)	% SPBRG value (decimal) 0.01 3332		Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
0.3	0.300	0.01	3332	0.300	-0.04	1665	0.300	-0.04	832	
1.2	1.200	0.04	832	1.201	-0.16	415	1.201	-0.16	207	
2.4	2.404	0.16	415	2.403	-0.16	207	2.403	-0.16	103	
9.6	9.615	0.16	103	9.615	-0.16	51	9.615	-0.16	25	
19.2	19.231	0.16	51	19.230	-0.16	25	19.230	-0.16	12	
57.6	58.824	2.12	16	55.555	3.55	8	_	_	_	
115.2	111.111	-3.55	8	_	_	_	_	_	_	

15.1.3 AUTO-BAUD RATE DETECT

The Enhanced USART module supports the automatic detection and calibration of baud rate. This feature is active only in Asynchronous mode and while the WUE bit is clear.

The automatic baud rate measurement sequence (Figure 15-1) begins whenever a Start bit is received and the ABDEN bit is set. The calculation is self-averaging.

In the Auto-Baud Rate Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. In ABD mode, the internal Baud Rate Generator is used as a counter to time the bit period of the incoming serial byte stream.

Once the ABDEN bit is set, the state machine will clear the BRG and look for a Start bit. The Auto-Baud Rate Detection must receive a byte with the value 55h (ASCII "U", which is also the LIN bus Sync character) in order to calculate the proper bit rate. The measurement is taken over both a low and a high bit time in order to minimize any effects caused by asymmetry of the incoming signal. After a Start bit, the SPBRG begins counting up, using the preselected clock source on the first rising edge of RX. After eight bits on the RX pin, or the fifth rising edge, an accumulated value totalling the proper BRG period is left in the SPBRGH:SPBRG register pair. Once the 5th edge is seen (this should correspond to the Stop bit), the ABDEN bit is automatically cleared.

If a rollover of the BRG occurs (an overflow from FFFFh to 0000h), the event is trapped by the ABDOVF status bit (BAUDCON<7>). It is set in hardware by BRG rollovers and can be set or cleared by the user in software. ABD mode remains active after rollover events and the ABDEN bit remains set (Figure 15-2).

While calibrating the baud rate period, the BRG registers are clocked at 1/8th the preconfigured clock rate. Note that the BRG clock will be configured by the BRG16 and BRGH bits. Independent of the BRG16 bit setting, both the SPBRG and SPBRGH will be used as a 16-bit counter. This allows the user to verify that no carry occurred for 8-bit modes by checking for 00h in the SPBRGH register. Refer to Table 15-4 for counter clock rates to the BRG.

While the ABD sequence takes place, the EUSART state machine is held in Idle. The RCIF interrupt is set once the fifth rising edge on RX is detected. The value in the RCREG needs to be read to clear the RCIF interrupt. The contents of RCREG should be discarded.

- **Note 1:** If the WUE bit is set with the ABDEN bit, Auto-Baud Rate Detection will occur on the byte *following* the Break character.
 - 2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible due to bit error rates. Overall system timing and communication baud rates must be taken into consideration when using the Auto-Baud Rate Detection feature.

TABLE 15-4: BRG COUNTER CLOCK RATES

BRG16	BRGH	BRG Counter Clock
0	0	Fosc/512
0	1	Fosc/128
1	0	Fosc/128
1	1	Fosc/32

Note: During the ABD sequence, SPBRG and SPBRGH are both used as a 16-bit counter, independent of the BRG16 setting.

15.1.3.1 ABD and EUSART Transmission

Since the BRG clock is reversed during ABD acquisition, the EUSART transmitter cannot be used during ABD. This means that whenever the ABDEN bit is set, TXREG cannot be written to. Users should also ensure that ABDEN does not become set during a transmit sequence. Failing to do this may result in unpredictable EUSART operation.

FIGURE 15-1: AUTOMATIC BAUD RATE CALCULATION

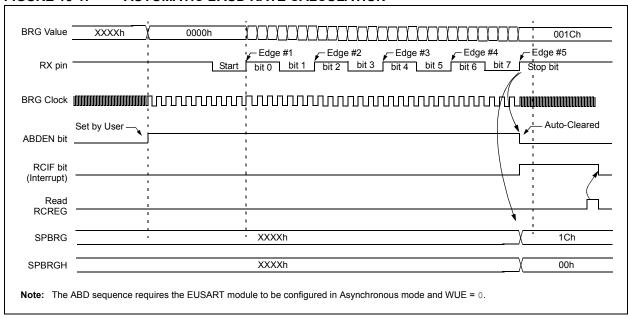
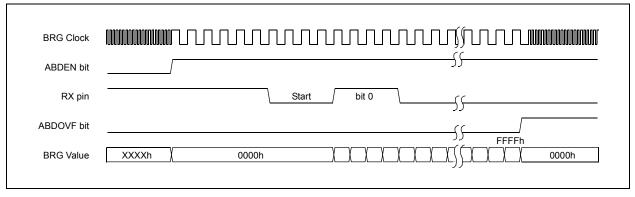


FIGURE 15-2: BRG OVERFLOW SEQUENCE



15.2 EUSART Asynchronous Mode

The Asynchronous mode of operation is selected by clearing the SYNC bit (TXSTA<4>). In this mode, the EUSART uses the standard Non-Return-to-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is eight bits. An on-chip dedicated 8-bit/16-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate depending on the BRGH and BRG16 bits (TXSTA<2> and BAUDCON<3>). Parity is not supported by the hardware but can be implemented in software and stored as the ninth data bit.

When operating in Asynchronous mode, the EUSART module consists of the following important elements:

- · Baud Rate Generator
- · Sampling Circuit
- · Asynchronous Transmitter
- · Asynchronous Receiver
- · Auto-Wake-up on Sync Break Character
- · 12-Bit Break Character Transmit
- · Auto-Baud Rate Detection

15.2.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 15-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one TcY), the TXREG register is empty and the TXIF flag bit (PIR1<4>) is set. This interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXIE (PIE1<4>). TXIF will be set regardless of the state of TXIE; it cannot be cleared in software. TXIF is also not cleared immediately upon loading TXREG but becomes valid in the second instruction cycle following the load instruction. Polling TXIF immediately following a load of TXREG will return invalid results.

While TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty.

- **Note 1:** The TSR register is not mapped in data memory so it is not available to the user.
 - **2:** Flag bit, TXIF, is set when enable bit, TXEN, is set.

To set up an Asynchronous Transmission:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
- 3. If interrupts are desired, set enable bit, TXIE.
- 4. If 9-bit transmission is desired, set transmit bit, TX9. Can be used as address/data bit.
- Enable the transmission by setting bit, TXEN, which will also set bit, TXIF.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- 7. Load data to the TXREG register (starts transmission).
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are

FIGURE 15-3: EUSART TRANSMIT BLOCK DIAGRAM

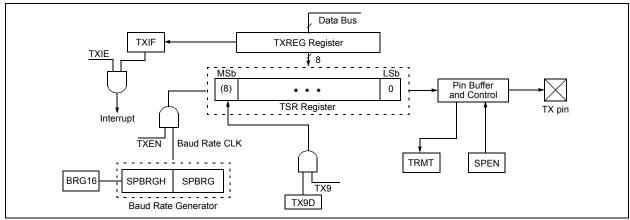


FIGURE 15-4: ASYNCHRONOUS TRANSMISSION

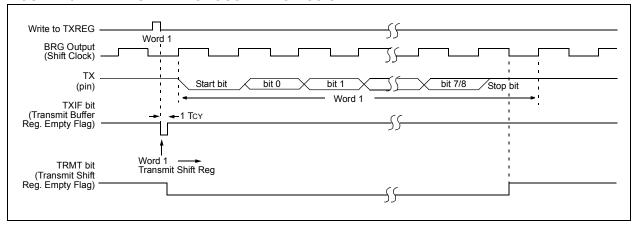


FIGURE 15-5: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)

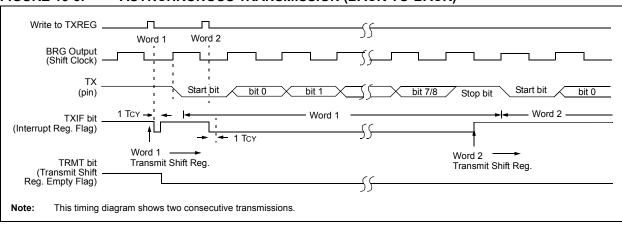


TABLE 15-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51	
TXREG	EUSART T	ransmit Reg	jister						51	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51	
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51	
SPBRGH	EUSART B	EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART B	aud Rate G	enerator Re	gister Low I	Byte				50	

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

15.2.2 EUSART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 15-6. The data is received on the RX pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc. This mode would typically be used in RS-232 systems.

To set up an Asynchronous Reception:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
- 3. If interrupts are desired, set enable bit, RCIE.
- 4. If 9-bit reception is desired, set bit, RX9.
- 5. Enable the reception by setting bit, CREN.
- Flag bit, RCIF, will be set when reception is complete and an interrupt will be generated if enable bit, RCIE, was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing enable bit, CREN.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

15.2.3 SETTING UP 9-BIT MODE WITH ADDRESS DETECT

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- 3. If interrupts are required, set the RCEN bit and select the desired priority level with the RCIP bit.
- 4. Set the RX9 bit to enable 9-bit reception.
- 5. Set the ADDEN bit to enable address detect.
- 6. Enable reception by setting the CREN bit.
- The RCIF bit will be set when reception is complete. The interrupt will be Acknowledged if the RCIE and GIE bits are set.
- 8. Read the RCSTA register to determine if any error occurred during reception, as well as read bit 9 of data (if applicable).
- Read RCREG to determine if the device is being addressed.
- 10. If any error occurred, clear the CREN bit.
- If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and interrupt the CPU.



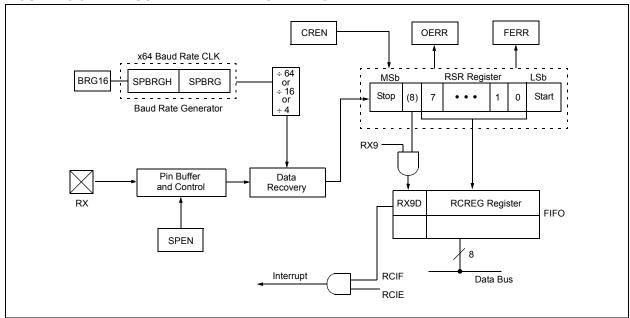


FIGURE 15-7: ASYNCHRONOUS RECEPTION

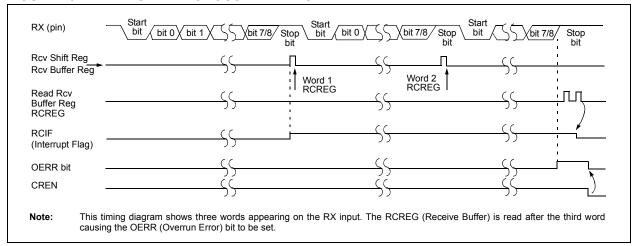


TABLE 15-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:		
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49		
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51		
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51		
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51		
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51		
RCREG	EUSART R	Receive Regi	ster						50		
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51		
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51		
SPBRGH	BRGH EUSART Baud Rate Generator Register High Byte										
SPBRG	EUSART B	Baud Rate G	enerator Re	gister Low	Byte				50		

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

15.2.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

During Sleep mode, all clocks to the EUSART are suspended. Therefore, the Baud Rate Generator is inactive and proper byte reception cannot be performed. The auto-wake-up feature allows the controller to wake-up due to activity on the RX/DT line while the EUSART is operating in Asynchronous mode.

The auto-wake-up feature is enabled by setting the WUE bit (BAUDCON<1>). Once set, the typical receive sequence on RX/DT is disabled and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a Wake-up Signal character for the LIN protocol.)

Following a wake-up event, the module generates an RCIF interrupt. The interrupt is generated synchronously to the Q clocks in normal operating modes (Figure 15-8) and asynchronously if the device is in Sleep mode (Figure 15-9). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared once a low-to-high transition is observed on the RX line following the wake-up event. At this point, the EUSART module is in Idle mode and returns to normal operation. This signals to the user that the Sync Break event is over.

15.2.4.1 Special Considerations Using Auto-Wake-up

Since auto-wake-up functions by sensing rising edge transitions on RX/DT, information with any state changes before the Stop bit may signal a false End-of-Character

(EOC) and cause data or framing errors. To work properly, therefore, the initial character in the transmission must be all '0's. This can be 00h (8 bits) for standard RS-232 devices or 000h (12 bits) for LIN bus.

Oscillator start-up time must also be considered, especially in applications using oscillators with longer start-up intervals (i.e., XT or HS mode). The Sync Break (or Wake-up Signal) character must be of sufficient length and be followed by a sufficient interval to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

15.2.4.2 Special Considerations Using the WUE Bit

The timing of WUE and RCIF events may cause some confusion when it comes to determining the validity of received data. As noted, setting the WUE bit places the EUSART in an Idle mode. The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared after this when a rising edge is seen on RX/DT. The interrupt condition is then cleared by reading the RCREG register. Ordinarily, the data in RCREG will be dummy data and should be discarded.

The fact that the WUE bit has been cleared (or is still set) and the RCIF flag is set should not be used as an indicator of the integrity of the data in RCREG. Users should consider implementing a parallel method in firmware to verify received data integrity.

To assure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

FIGURE 15-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING NORMAL OPERATION

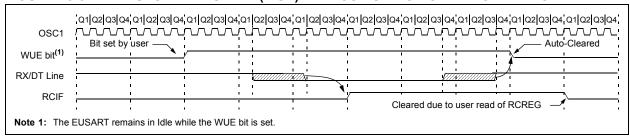
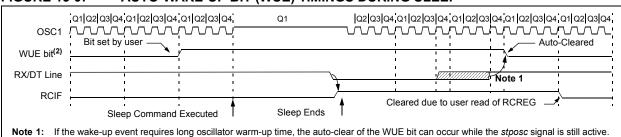


FIGURE 15-9: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP



This sequence should not depend on the presence of Q clocks.

2: The EUSART remains in Idle while the WUE bit is set.

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15.2.5 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. The Break character transmit consists of a Start bit, followed by twelve '0' bits and a Stop bit. The Frame Break character is sent whenever the SENDB and TXEN bits (TXSTA<3> and TXSTA<5>) are set while the Transmit Shift Register is loaded with data. Note that the value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

Note that the data value written to the TXREG for the Break character is ignored. The write simply serves the purpose of initiating the proper sequence.

The TRMT bit indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 15-10 for the timing of the Break character sequence.

15.2.5.1 Break and Sync Transmit Sequence

The following sequence will send a message frame header made up of a Break, followed by an Auto-Baud Sync byte. This sequence is typical of a LIN bus master.

- 1. Configure the EUSART for the desired mode.
- Set the TXEN and SENDB bits to set up the Break character.

- 3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
- 4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
- After the Break has been sent, the SENDB bit is reset by hardware. The Sync character now transmits in the preconfigured mode.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

15.2.6 RECEIVING A BREAK CHARACTER

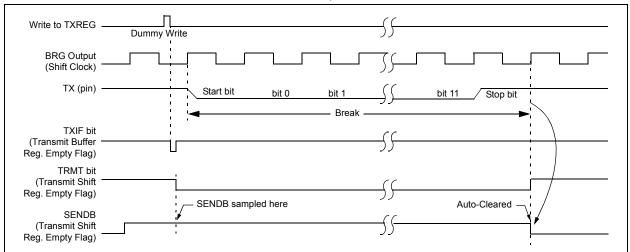
The Enhanced USART module can receive a Break character in two ways.

The first method forces configuration of the baud rate at a frequency of 9/13 the typical speed. This allows for the Stop bit transition to be at the correct sampling location (13 bits for Break versus Start bit and eight data bits for typical data).

The second method uses the auto-wake-up feature described in **Section 15.2.4** "Auto-Wake-up on Sync Break Character". By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Rate Detect feature. For both methods, the user can set the ABD bit once the TXIF interrupt is observed.





15.3 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTA<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTA<4>). In addition, enable bit, SPEN (RCSTA<7>), is set in order to configure the TX and RX pins to CK (clock) and DT (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CK line. Clock polarity is selected with the SCKP bit (BAUDCON<4>). Setting SCKP sets the Idle state on CK as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

15.3.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 15-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG register is empty and the TXIF flag bit (PIR1<4>) is set. The interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXIE (PIE1<4>). TXIF is set regardless of the state of enable bit, TXIE; it cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

While flag bit, TXIF, indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit so the user must poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

To set up a Synchronous Master Transmission:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
- 3. If interrupts are desired, set enable bit, TXIE.
- 4. If 9-bit transmission is desired, set bit, TX9.
- 5. Enable the transmission by setting bit, TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- 7. Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.



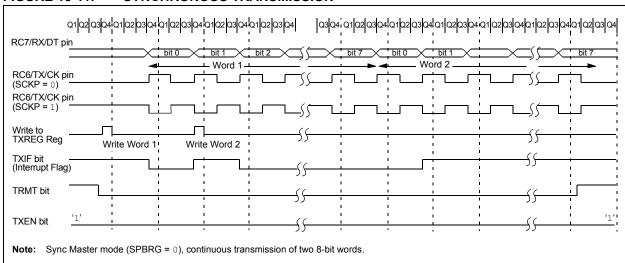


FIGURE 15-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

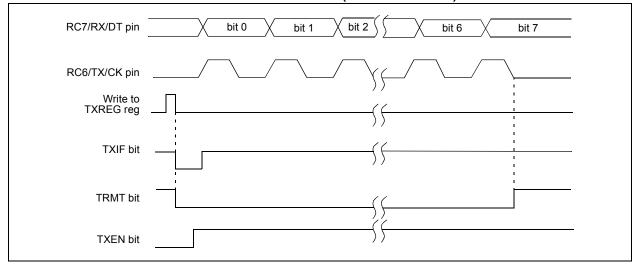


TABLE 15-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	_	ADIF	RCIF	TXIF	1	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51	
TXREG	EUSART T	ransmit Reg	ister						51	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51	
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51	
SPBRGH	SPBRGH EUSART Baud Rate Generator Register High Byte									
SPBRG	EUSART E	Baud Rate G	enerator Re	gister Low	Byte				50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

15.3.2 EUSART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either the Single Receive Enable bit, SREN (RCSTA<5>), or the Continuous Receive Enable bit, CREN (RCSTA<4>). Data is sampled on the RX pin on the falling edge of the clock.

If enable bit, SREN, is set, only a single word is received. If enable bit, CREN, is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.

- 3. Ensure bits, CREN and SREN, are clear.
- 4. If interrupts are desired, set enable bit, RCIE.
- 5. If 9-bit reception is desired, set bit, RX9.
- 6. If a single reception is required, set bit, SREN. For continuous reception, set bit, CREN.
- Interrupt flag bit, RCIF, will be set when reception is complete and an interrupt will be generated if the enable bit, RCIE, was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing bit, CREN.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set

FIGURE 15-13: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)

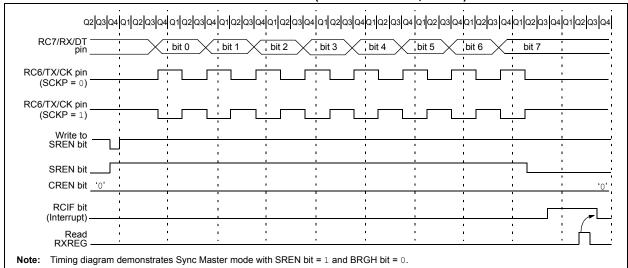


TABLE 15-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51	
RCREG	EUSART R	eceive Registe	r						50	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51	
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51	
SPBRGH EUSART Baud Rate Generator Register High Byte										
SPBRG	EUSART B	aud Rate Gene	rator Regist	er Low Byte			•		50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

15.4 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTA<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

15.4.1 EUSART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep mode.

If two words are written to the TXREG register and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in the TXREG register.
- c) Flag bit, TXIF, will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit, TXIF, will now be set.
- e) If enable bit, TXIE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- 2. Clear bits, CREN and SREN.
- 3. If interrupts are desired, set enable bit, TXIE.
- 4. If 9-bit transmission is desired, set bit, TX9.
- Enable the transmission by setting enable bit, TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 15-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51	
TXREG	EUSART T	ransmit Regi	ister						51	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51	
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51	
SPBRGH EUSART Baud Rate Generator Register High Byte										
SPBRG	EUSART E	Baud Rate Ge	enerator Re	gister Low E	Byte	•	•		50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

15.4.2 EUSART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep or any Idle mode and bit, SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting the CREN bit prior to entering Sleep or any Idle mode, then a word may be received while in this low-power mode. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the chip from the low-power mode. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- 2. If interrupts are desired, set enable bit, RCIE.
- 3. If 9-bit reception is desired, set bit, RX9.
- 4. To enable reception, set enable bit, CREN.
- Flag bit RCIF will be set when reception is complete. An interrupt will be generated if enable bit, RCIE, was set.
- 6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit, CREN.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 15-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49	
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51	
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51	
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51	
RCREG	EUSART F	Receive Regi	ster						50	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51	
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	51	
SPBRGH	SPBRGH EUSART Baud Rate Generator Register High Byte									
SPBRG	EUSART E	Baud Rate G	enerator Re	gister Low I	Byte			•	50	

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception.

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NOTES:

16.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 16-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 16-2, configures the functions of the port pins. The ADCON2 register, shown in Register 16-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 16-1: ADCON0: A/D CONTROL REGISTER 0

U0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 CHS3:CHS0: Analog Channel Select bits

0000 = Channel 0 (AN0)

0001 = Channel 1 (AN1)

0010 = Channel 2 (AN2)

0011 = Channel 3 (AN3)

0100 = Channel 4 (AN4)

0101 = Channel 5 (AN5)(1,2)

0110 = Channel 6 (AN6)^(1,2)

0111 = Channel 7 (AN7)(1,2)

1000 = Channel 8 (AN8)

1001 = Channel 9 (AN9)

1010 = Channel 10 (AN10)

1011 = Channel 11 (AN11)

1100 = Channel 12 (AN12

1101 = Unimplemented⁽²⁾

1110 = Unimplemented(2)

1111 = Unimplemented⁽²⁾

bit 1 GO/DONE: A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 ADON: A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.

2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 16-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W ⁽¹⁾	R/W ⁽¹⁾	R/W ⁽¹⁾
_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 VCFG1: Voltage Reference Configuration bit (VREF- source)

1 = VREF- (AN2)

0 **= V**ss

bit 4 **VCFG0:** Voltage Reference Configuration bit (VREF+ source)

1 = VREF+ (AN3)

0 = VDD

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

				J									
PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7 ⁽²⁾	AN6 ⁽²⁾	AN5 ⁽²⁾	AN4	AN3	AN2	AN1	AN0
0000(1)	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0001	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0010	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0011	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0100	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0101	D	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
0110	D	D	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α
0111(1)	D	D	D	D	D	Α	Α	Α	Α	Α	Α	Α	Α
1000	D	D	D	D	D	D	Α	Α	Α	Α	Α	Α	Α
1001	D	D	D	D	D	D	D	Α	Α	Α	Α	Α	Α
1010	D	D	D	D	D	D	D	D	Α	Α	Α	Α	Α
1011	D	D	D	D	D	D	D	D	D	Α	Α	Α	Α
1100	D	D	D	D	D	D	D	D	D	D	Α	Α	Α
1101	D	D	D	D	D	D	D	D	D	D	D	Α	Α
1110	D	D	D	D	D	D	D	D	D	D	D	D	Α
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are available only on 40/44-pin devices.

D = Digital I/O

REGISTER 16-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	_	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 ADFM: A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 Unimplemented: Read as '0'

bit 5-3 ACQT2:ACQT0: A/D Acquisition Time Select bits

111 **= 20 T**AD

110 = **16 T**AD

101 **= 12 T**AD

100 **= 8 T**AD

011 **= 6 TAD**

010 **= 4 TAD**

001 **= 2 T**AD

000 = 0 TAD⁽¹⁾

bit 2-0 ADCS2:ADCS0: A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)(1)

110 = Fosc/64

101 = Fosc/16

100 = Fosc/4

011 = FRC (clock derived from A/D RC oscillator)(1)

010 = Fosc/32

001 = Fosc/8

000 = Fosc/2

Note 1: If the A/D FRC clock source is selected, a delay of one Tcy (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

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The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss) or the voltage level on the RA3/AN3/ VREF+ and RA2/AN2/VREF- pins.

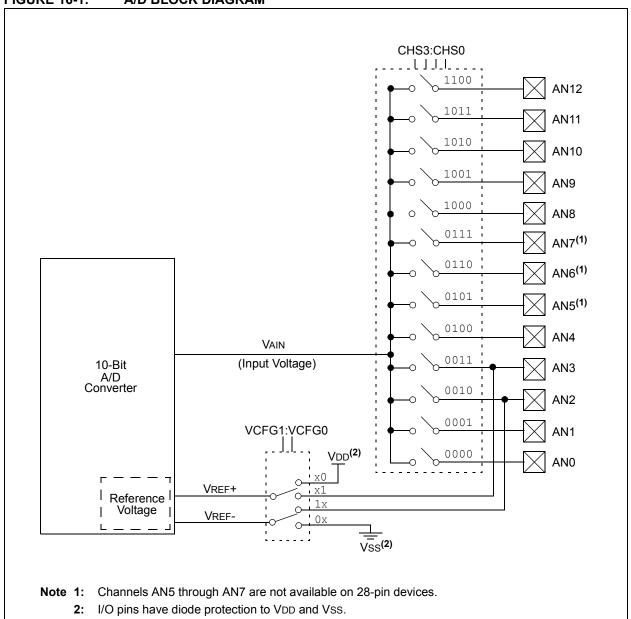
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 16-1.

FIGURE 16-1: A/D BLOCK DIAGRAM



The value in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 16.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

- 1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - · Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
- 2. Configure A/D interrupt (if desired):
 - · Clear ADIF bit
 - · Set ADIE bit
 - · Set GIE bit
- 3. Wait the required acquisition time (if required).
- 4. Start conversion:
 - Set GO/DONE bit (ADCON0 register)

- 5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared OR
 - · Waiting for the A/D interrupt
- 6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
- For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 3 TAD is required before the next acquisition starts.



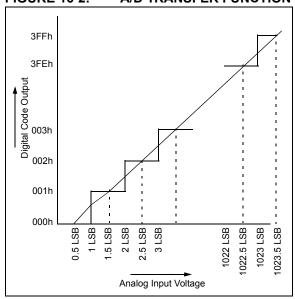
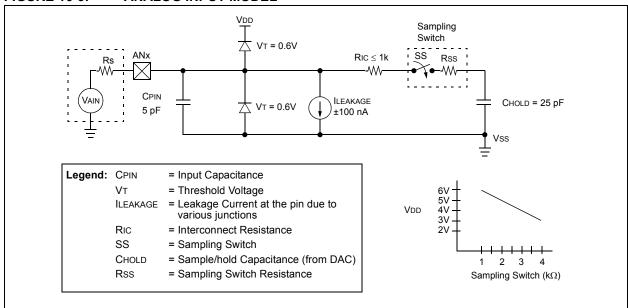


FIGURE 16-3: ANALOG INPUT MODEL



16.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (Chold) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 16-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor Chold. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 2.5 k Ω . After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note: When the conversion is started, the

holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 16-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 16-3 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following application system assumptions:

CHOLD = 25 pF Rs = 2.5 kΩ Conversion Error \leq 1/2 LSb

VDD = $5V \rightarrow Rss = 2 \text{ k}\Omega$ Temperature = 85°C (system max.)

EQUATION 16-1: ACQUISITION TIME

```
TACQ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient
= TAMP + TC + TCOFF
```

EQUATION 16-2: A/D MINIMUM CHARGING TIME

```
VHOLD = (VREF - (VREF/2048)) \cdot (1 - e^{(-TC/CHOLD(RIC + RSS + RS))})

or

TC = -(CHOLD)(RIC + RSS + RS) \ln(1/2048)
```

EQUATION 16-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

```
TACQ
                     TAMP + TC + TCOFF
TAMP
                     0.2 \, \mu s
TCOFF
                     (Temp - 25^{\circ}C)(0.02 \mu s/^{\circ}C)
                     (85^{\circ}C - 25^{\circ}C)(0.02 \,\mu\text{s}/^{\circ}C)
                     1.2 us
Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 ms.
TC
                     -(CHOLD)(RIC + RSS + RS) ln(1/2047) \mu s
                     -(25 \text{ pF}) (1 \text{ k}\Omega + 2 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0004883) \,\mu\text{s}
                     1.05 \mu s
                     0.2 \mu s + 1 \mu s + 1.2 \mu s
TACO
                     2.4 \mu s
```

16.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>) which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

16.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 Tosc
- 4 Tosc
- 8 Tosc
- 16 Tosc
- 32 Tosc
- 64 Tosc
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD (see parameter 130 in Table 21-18 for more information).

Table 16-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 16-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock S	ource (TAD)	Maximum Device Frequency				
Operation	ADCS2:ADCS0	PIC18FX450	PIC18LFX450 ⁽⁴⁾			
2 Tosc	000	2.86 MHz	1.43 MHz			
4 Tosc	100	5.71 MHz	2.86 MHz			
8 Tosc	001	11.43 MHz	5.72 MHz			
16 Tosc	101	22.86 MHz	11.43 MHz			
32 Tosc	010	45.71 MHz	22.86 MHz			
64 Tosc	110	48.0 MHz	45.71 MHz			
RC ⁽³⁾	x11	1.00 MHz ⁽¹⁾	1.00 MHz ⁽²⁾			

- **Note 1:** The RC source has a typical TAD time of 1.2 μ s.
 - 2: The RC source has a typical TAD time of 2.5 μ s.
 - 3: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or the A/D accuracy may be out of specification.
 - 4: Low-power devices only.

16.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT2:ACQT0 and ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used in that mode. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in the Sleep mode requires the A/D FRC clock to be selected. If bits ACQT2:ACQT0 are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

16.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

- Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert as analog inputs. Analog levels on a digitally configured input will be accurately converted.
 - 2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.
 - **3:** The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG0 bits in ADCON1 are reset.

16.6 A/D Conversions

Figure 16-4 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 16-5 shows the operation of the A/D Converter after the GO/DONE bit has been set, the ACQT2:ACQT0 bits are set to '010' and selecting a 4 TAD acquisition time before the conversion starts.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

16.7 Discharge

The discharge phase is used to initialize the value of the capacitor array. The array is discharged before every sample. This feature helps to optimize the unitygain amplifier as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measurement values.

FIGURE 16-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)

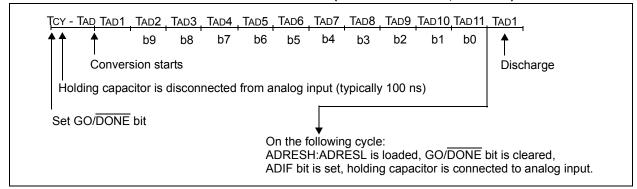
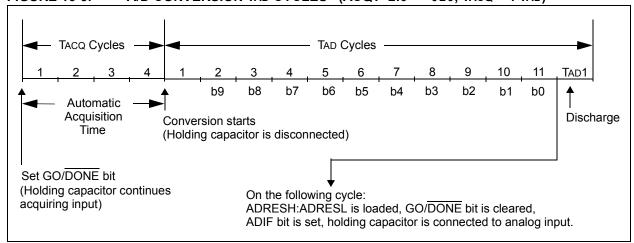


FIGURE 16-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



16.8 Use of the CCP1 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP1 module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead

(moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 counter.

TABLE 16-2: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	_	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	51
PIE1	_	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	51
IPR1	_	ADIP	RCIP	TXIP	_	CCP1IP	TMR2IP	TMR1IP	51
PIR2	OSCFIF	_	USBIF	_	_	HLVDIF	_	_	51
PIE2	OSCFIE	_	USBIE	_	_	HLVDIE	_	_	51
IPR2	OSCFIP	_	USBIP	_	_	HLVDIP	_	_	51
ADRESH	A/D Result	Register Hig	ıh Byte						50
ADRESL	A/D Result	Register Lov	w Byte						50
ADCON0	_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	50
ADCON1	_	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	50
ADCON2	ADFM	_	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	50
PORTA	_	RA6 ⁽²⁾	RA5	RA4	RA3	RA2	RA1	RA0	51
TRISA	_	TRISA6 ⁽²⁾	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	51
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	51
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	51
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	51
PORTE	_	_	_	_	RE3 ^(1,3)	RE2 ⁽⁴⁾	RE1 ⁽⁴⁾	RE0 ⁽⁴⁾	51
TRISE ⁽⁴⁾	_	_	_	_	_	TRISE2 ⁽⁴⁾	TRISE1 ⁽⁴⁾	TRISE0 ⁽⁴⁾	51
LATE ⁽⁴⁾	_	_	_	_	_	LATE2 ⁽⁴⁾	LATE1 ⁽⁴⁾	LATE0 ⁽⁴⁾	51

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: Implemented only when Master Clear functionality is disabled (MCLRE Configuration bit = 0).

- 2: RA6 and its associated latch and data direction bits are enabled as I/O pins based on oscillator configuration; otherwise, they are read as '0'.
- 3: RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.
- 4: These registers and/or bits are not implemented on 28-pin devices.

17.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

PIC18F2450/4450 devices have a High/Low-Voltage Detect module (HLVD). This is a programmable circuit that allows the user to specify both a device voltage trip point and the direction of change from that point. If the device experiences an excursion past the trip point in that direction, an interrupt flag is set. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

High/Low-Voltage Detect Control register (Register 17-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control which minimizes the current consumption for the device.

The block diagram for the HLVD module is shown in Figure 17-1.

REGISTER 17-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
VDIRMAG	_	IRVST	HLVDEN	HLVDL3 ⁽¹⁾	HLVDL2 ⁽¹⁾	HLVDL1 ⁽¹⁾	HLVDL0 ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 VDIRMAG: Voltage Direction Magnitude Select bit

1 = Event occurs when voltage equals or exceeds trip point (HLVDL3:HLDVL0)

0 = Event occurs when voltage equals or falls below trip point (HLVDL3:HLVDL0)

bit 6 Unimplemented: Read as '0'

bit 5 IRVST: Internal Reference Voltage Stable Flag bit

> 1 = Indicates that the voltage detect logic will generate the interrupt flag at the specified voltage trip point

0 = Indicates that the voltage detect logic will not generate the interrupt flag at the specified voltage trip point and the LVD interrupt should not be enabled

bit 4 HLVDEN: High/Low-Voltage Detect Power Enable bit

1 = HIVD enabled

0 = HLVD disabled

bit 3-0 **HLVDL3:HLVDL0:** Voltage Detection Limit bits⁽¹⁾

1111 = Reserved

1110 = Maximum setting

0000 = Minimum setting

Note 1: See Table 21-4 in Section 21.0 "Electrical Characteristics" for specifications.

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The module is enabled by setting the HLVDEN bit. Each time that the HLVD module is enabled, the circuitry requires some time to stabilize. The IRVST bit is a read-only bit and is used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and IRVST is set.

The VDIRMAG bit determines the overall operation of the module. When VDIRMAG is cleared, the module monitors for drops in VDD below a predetermined set point. When the bit is set, the module monitors for rises in VDD above the set point.

17.1 Operation

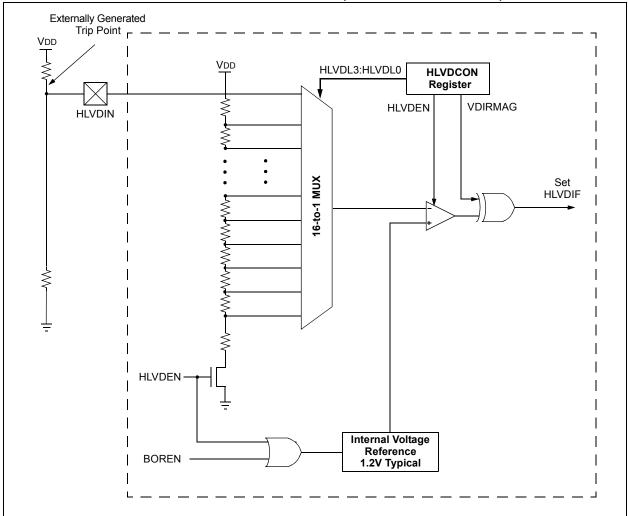
When the HLVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a high or low-voltage

event, depending on the configuration of the module. When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any one of 16 values. The trip point is selected by programming the HLVDL3:HLVDL0 bits (HLVDCON<3:0>).

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits, HLVDL3:HLVDL0, are set to '1111'. In this state, the comparator input is multiplexed from the external input pin, HLVDIN. This gives users flexibility because it allows them to configure the High/Low-Voltage Detect interrupt to occur at any voltage in the valid operating range.

FIGURE 17-1: HLVD MODULE BLOCK DIAGRAM (WITH EXTERNAL INPUT)



17.2 HLVD Setup

The following steps are needed to set up the HLVD module:

- Disable the module by clearing the HLVDEN bit (HLVDCON<4>).
- 2. Write the value to the HLVDL3:HLVDL0 bits that selects the desired HLVD trip point.
- Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
- Enable the HLVD module by setting the HLVDEN bit.
- 5. Clear the HLVD Interrupt Flag, HLVDIF (PIR2<2>), which may have been set from a previous interrupt.
- Enable the HLVD interrupt, if interrupts are desired, by setting the HLVDIE and GIE/GIEH bits (PIE2<2> and INTCON<7>). An interrupt will not be generated until the IRVST bit is set.

17.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and will consume static current. The total current consumption, when enabled, is specified in electrical specification parameter D022 (Section 270 "DC Characteristics").

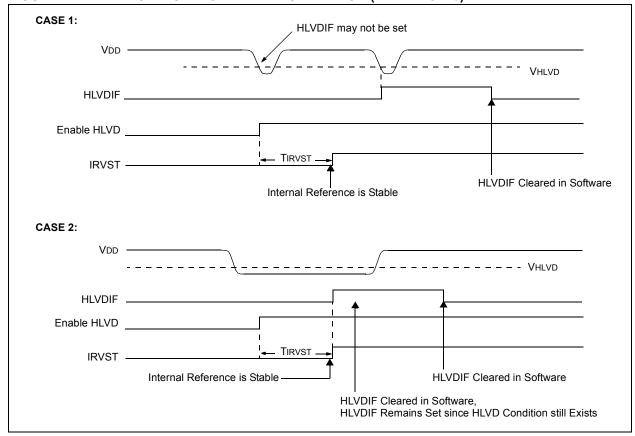
Depending on the application, the HLVD module does not need to be operating constantly. To decrease the current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After doing the check, the HLVD module may be disabled.

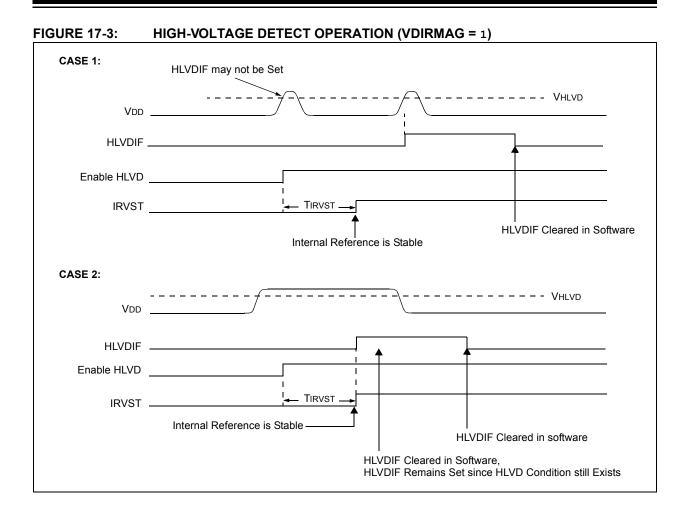
17.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification parameter D420 (see Table 21-4 in **Section 21.0 "Electrical Characteristics"**), may be used by other internal circuitry, such as the Programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification parameter 36 (Table 21-10).

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval. Refer to Figure 17-2 or Figure 17-3.

FIGURE 17-2: LOW-VOLTAGE DETECT OPERATION (VDIRMAG = 0)



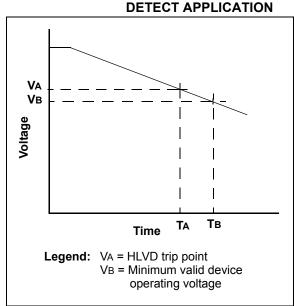


17.5 Applications

In many applications, the ability to detect a drop below or rise above a particular threshold is desirable. For example, the HLVD module could be periodically enabled to detect Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a high-voltage detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 17-4 shows a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage, VA, the HLVD logic generates an interrupt at time, TA. The interrupt could cause the execution of an ISR, which would allow the application to perform "house-keeping tasks" and perform a controlled shutdown before the device voltage exits the valid operating range at TB. The HLVD, thus, would give the application a time window, represented by the difference between TA and TB, to safely exit.

FIGURE 17-4: TYPICAL
HIGH/LOW-VOLTAGE
DETECT APPLICATION



17.6 Operation During Sleep

When enabled, the HLVD circuitry continues to operate during Sleep. If the device voltage crosses the trip point, the HLVDIF bit will be set and the device will wake-up from Sleep. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

17.7 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.

TABLE 17-1: REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
HLVDCON	VDIRMAG	_	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	50
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR2	OSCFIF	_	USBIF	_	_	HLVDIF	_	_	51
PIE2	OSCFIE	_	USBIE	_	_	HLVDIE	_	_	51
IPR2	OSCFIP	_	USBIP	_	_	HLVDIP	_	_	51

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the HLVD module.

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NOTES:

18.0 SPECIAL FEATURES OF THE CPU

PIC18F2450/4450 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These are:

- · Oscillator Selection
- · Resets:
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- · Fail-Safe Clock Monitor (FSCM)
- · Two-Speed Start-up
- · Code Protection
- · ID Locations
- In-Circuit Serial Programming (ICSP)

The oscillator can be configured for the application depending on frequency, power, accuracy and cost. All of the options are discussed in detail in **Section 2.0** "Oscillator Configurations".

A complete discussion of device Resets and interrupts is available in previous sections of this data sheet.

In addition to their Power-up and Oscillator Start-up Timers provided for Resets, PIC18F2450/4450 devices have a Watchdog Timer, which is either permanently enabled via the Configuration bits or software controlled (if configured as disabled).

The inclusion of an internal RC oscillator also provides the additional benefits of a Fail-Safe Clock Monitor (FSCM) and Two-Speed Start-up. FSCM provides for background monitoring of the peripheral clock and automatic switchover in the event of its failure. Two-Speed Start-up enables code to be executed almost immediately on start-up, while the primary clock source completes its start-up delays.

All of these features are enabled and configured by setting the appropriate Configuration register bits.

18.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped starting at program memory location 300000h.

The user will note that address 300000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h-3FFFFFh), which can only be accessed using table reads and table writes.

Programming the Configuration registers is done in a manner similar to programming the Flash memory. The WR bit in the EECON1 register starts a self-timed write to the Configuration register. In normal operation mode, a TBLWT instruction, with the TBLPTR pointing to the Configuration register, sets up the address and the data for the Configuration register write. Setting the WR bit starts a long write to the Configuration register. The Configuration registers are written a byte at a time. To write or erase a configuration cell, a TBLWT instruction can write a '1' or a '0' into the cell. For additional details on Flash programming, refer to Section 6.5 "Writing to Flash Program Memory".

TABLE 18-1: CONFIGURATION BITS AND DEVICE IDs

File	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	_	_	USBDIV	CPUDIV1	CPUDIV0	PLLDIV2	PLLDIV1	PLLDIV0	00 0111
300001h	CONFIG1H	IESO	FCMEN	_	1	FOSC3	FOSC2	FOSC1	FOSC0	00 0111
300002h	CONFIG2L	_	_	VREGEN	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	01 1111
300003h	CONFIG2H	_	_	_	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	1 1111
300005h	CONFIG3H	MCLRE	_	_	_	_	LPT10SC	PBADEN	_	101-
300006h	CONFIG4L	DEBUG	XINST	ICPRT ⁽²⁾	-	BBSIZ	LVP	1	STVREN	100- 01-1
300008h	CONFIG5L	_	_	_	_	_	_	CP1	CP0	11
300009h	CONFIG5H	_	СРВ	_	_	_	_	_	_	-1
30000Ah	CONFIG6L	_	_	_	_	_	_	WRT1	WRT0	11
30000Bh	CONFIG6H		WRTB	WRTC	1	-	_	1	-	-11
30000Ch	CONFIG7L	_	_	_	_	_	_	EBTR1	EBTR0	11
30000Dh	CONFIG7H	_	EBTRB	_	_	_	_	_	_	-1
3FFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	XXXX XXXX(1)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0001 0010(1)

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: See Register 18-13 and Register 18-14 for device ID values. DEVID registers are read-only and cannot be programmed by the user.

^{2:} Available only on PIC18F4450 devices in 44-pin TQFP packages. Always leave this bit clear in all other devices.

REGISTER 18-1: CONFIG1L: CONFIGURATION REGISTER 1 LOW (BYTE ADDRESS 300000h)

U-0	U-0	R/P-0	R/P-0	R/P-0	R/P-1	R/P-1	R/P-1
_	_	USBDIV	CPUDIV1	CPUDIV0	PLLDIV2	PLLDIV1	PLLDIV0
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-6 **Unimplemented:** Read as '0'

bit 5 USBDIV: USB Clock Selection bit (used in Full-Speed USB mode only; UCFG:FSEN = 1)

1 = USB clock source comes from the 96 MHz PLL divided by 2

0 = USB clock source comes directly from the primary oscillator block with no postscale

bit 4-3 CPUDIV1:CPUDIV0: System Clock Postscaler Selection bits

For XT, HS, EC and ECIO Oscillator modes:

11 = Primary oscillator divided by 4 to derive system clock

10 = Primary oscillator divided by 3 to derive system clock

01 = Primary oscillator divided by 2 to derive system clock

00 = Primary oscillator used directly for system clock (no postscaler)

For XTPLL, HSPLL, ECPLL and ECPIO Oscillator modes:

11 = 96 MHz PLL divided by 6 to derive system clock

10 = 96 MHz PLL divided by 4 to derive system clock

01 = 96 MHz PLL divided by 3 to derive system clock

00 = 96 MHz PLL divided by 2 to derive system clock

bit 2-0 PLLDIV2:PLLDIV0: PLL Prescaler Selection bits

111 = Divide by 12 (48 MHz oscillator input)

110 = Divide by 10 (40 MHz oscillator input)

101 = Divide by 6 (24 MHz oscillator input)

100 = Divide by 5 (20 MHz oscillator input)

011 = Divide by 4 (16 MHz oscillator input)

010 = Divide by 3 (12 MHz oscillator input)

001 = Divide by 2 (8 MHz oscillator input)

000 = No prescale (4 MHz oscillator input drives PLL directly)

REGISTER 18-2: CONFIG1H: CONFIGURATION REGISTER 1 HIGH (BYTE ADDRESS 300001h)

R/P-0	R/P-0	U-0	U-0	R/P-0	R/P-1	R/P-1	R/P-1
IESO	FCMEN	_	_	FOSC3 ⁽¹⁾	FOSC2 ⁽¹⁾	FOSC1 ⁽¹⁾	FOSC0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 IESO: Internal/External Oscillator Switchover bit

1 = Oscillator Switchover mode enabled0 = Oscillator Switchover mode disabled

bit 6 FCMEN: Fail-Safe Clock Monitor Enable bit

1 = Fail-Safe Clock Monitor enabled0 = Fail-Safe Clock Monitor disabled

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **FOSC3:FOSC0:** Oscillator Selection bits⁽¹⁾

111x = HS oscillator, PLL enabled (HSPLL)

110x = HS oscillator (HS)

1011 = Internal oscillator, HS oscillator used by USB (INTHS)

1010 = Internal oscillator, XT used by USB (INTXT)

1001 = Internal oscillator, CLKO function on RA6, EC used by USB (INTCKO)

1000 = Internal oscillator, port function on RA6, EC used by USB (INTIO)

0111 = EC oscillator, PLL enabled, CLKO function on RA6 (ECPLL)

0110 = EC oscillator, PLL enabled, port function on RA6 (ECPIO)

0101 = EC oscillator, CLKO function on RA6 (EC)

0100 = EC oscillator, port function on RA6 (ECIO)

001x = XT oscillator, PLL enabled (XTPLL)

000x = XT oscillator (XT)

Note 1: The microcontroller and USB module both use the selected oscillator as their clock source in XT, HS and EC modes. The USB module uses the indicated XT, HS or EC oscillator as its clock source whenever the microcontroller uses the internal oscillator.

REGISTER 18-3: CONFIG2L: CONFIGURATION REGISTER 2 LOW (BYTE ADDRESS 300002h)

U-0	U-0	R/P-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
_	_	VREGEN	BORV1 ⁽¹⁾	BORV0 ⁽¹⁾	BOREN1 ⁽²⁾	BORENO ⁽²⁾	PWRTEN ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-6 Unimplemented: Read as '0'

bit 5 **VREGEN:** USB Internal Voltage Regulator Enable bit

1 = USB voltage regulator enabled0 = USB voltage regulator disabled

bit 4-3 **BORV1:BORV0:** Brown-out Reset Voltage bits⁽¹⁾

11 = Minimum setting

.

00 = Maximum setting

bit 2-1 BOREN1:BOREN0: Brown-out Reset Enable bits⁽²⁾

11 = Brown-out Reset enabled in hardware only (SBOREN is disabled)

10 = Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)

01 = Brown-out Reset enabled and controlled by software (SBOREN is enabled)

00 = Brown-out Reset disabled in hardware and software

bit 0 **PWRTEN**: Power-up Timer Enable bit⁽²⁾

1 = PWRT disabled

0 = PWRT enabled

Note 1: See Section 21.0 "Electrical Characteristics" for the specifications.

2: The Power-up Timer is decoupled from Brown-out Reset, allowing these features to be independently controlled.

REGISTER 18-4: CONFIG2H: CONFIGURATION REGISTER 2 HIGH (BYTE ADDRESS 300003h)

U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
_	_	_	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 WDTPS3:WDTPS0: Watchdog Timer Postscale Select bits

1111 = 1:32,768

1110 = 1:16,384

1101 = 1:8,192

1100 = 1:4,096

1011 = 1:2,048

1010 = 1:1,024

1001 = 1:512

1000 = 1:256

0111 = 1:128

0110 = 1:64

0101 = 1:32

0100 = 1:16

0011 = 1:8

0010 = 1:4

0001 = 1:2

0000 = 1:1

bit 0 WDTEN: Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled (control is placed on the SWDTEN bit)

REGISTER 18-5: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	U-0
MCLRE	_	_	_	_	LPT1OSC	PBADEN	_
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 MCLRE: MCLR Pin Enable bit

1 = $\overline{\text{MCLR}}$ pin enabled, RA5 input pin disabled 0 = RA5 input pin enabled, $\overline{\text{MCLR}}$ pin disabled

bit 6-3 Unimplemented: Read as '0'

bit 2 LPT10SC: Low-Power Timer1 Oscillator Enable bit

1 = Timer1 configured for low-power operation0 = Timer1 configured for higher power operation

bit 1 PBADEN: PORTB A/D Enable bit

(Affects ADCON1 Reset state. ADCON1 controls PORTB<4:0> pin configuration.)

1 = PORTB<4:0> pins are configured as analog input channels on Reset

0 = PORTB<4:0> pins are configured as digital I/O on Reset

bit 0 Unimplemented: Read as '0'

REGISTER 18-6: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/P-1	R/P-0	R/P-0	U-0	R/P-0	R/P-1	U-0	R/P-1
DEBUG	XINST	ICPRT ⁽¹⁾	_	BBSIZ	LVP	_	STVREN
bit 7							bit 0

 Legend:

 R = Readable bit
 P = Programmable bit
 U = Unimplemented bit, read as '0'

 -n = Value when device is unprogrammed
 u = Unchanged from programmed state

bit 7 **DEBUG:** Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug bit 6 XINST: Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode) bit 5 ICPRT: Dedicated In-Circuit Debug/Programming Port (ICPORT) Enable bit (1) 1 = ICPORT enabled 0 = ICPORT disabled Unimplemented: Read as '0' bit 4 bit 3 BBSIZ: Boot Block Size Select bit 1 = 2 kW boot block size 0 = 1 kW boot block size bit 2 LVP: Single-Supply ICSP™ Enable bit 1 = Single-Supply ICSP enabled 0 = Single-Supply ICSP disabled bit 1 Unimplemented: Read as '0' bit 0 STVREN: Stack Full/Underflow Reset Enable bit 1 = Stack full/underflow will cause Reset 0 = Stack full/underflow will not cause Reset

Note 1: Available only on PIC18F4450 devices in 44-pin TQFP packages. Always leave this bit clear in all other devices.

REGISTER 18-7: CONFIG5L: CONFIGURATION REGISTER 5 LOW (BYTE ADDRESS 300008h)

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
_	_	_	_	_	_	CP1	CP0
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-2 **Unimplemented:** Read as '0' bit 1 **CP1:** Code Protection bit

1 = Block 1 (002000-003FFFh) is not code-protected 0 = Block 1 (002000-003FFFh) is code-protected

bit 0 **CP0:** Code Protection bit

1 = Block 0 (000800-001FFFh) or (001000-001FFFh) is not code-protected 0 = Block 0 (000800-001FFFh) or (001000-001FFFh) is code-protected

REGISTER 18-8: CONFIG5H: CONFIGURATION REGISTER 5 HIGH (BYTE ADDRESS 300009h)

U-0	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
_	CPB	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 **Unimplemented:** Read as '0'

bit 6 CPB: Boot Block Code Protection bit

1 = Boot block (000000-0007FFh) or (000000-000FFFh) is not code-protected 0 = Boot block (000000-0007FFh) or (000000-000FFFh) is code-protected

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 18-9: CONFIG6L: CONFIGURATION REGISTER 6 LOW (BYTE ADDRESS 30000Ah)

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
_		_	_	_	_	WRT1	WRT0
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-2 **Unimplemented:** Read as '0' bit 1 **WRT1:** Write Protection bit

1 = Block 1 (002000-003FFFh) is not write-protected 0 = Block 1 (002000-003FFFh) is write-protected

bit 0 WRT0: Write Protection bit

1 = Block 0 (000800-001FFFh) or (001000-001FFFh) is not write-protected 0 = Block 0 (000800-001FFFh) or (001000-001FFFh) is write-protected

REGISTER 18-10: CONFIG6H: CONFIGURATION REGISTER 6 HIGH (BYTE ADDRESS 30000Bh)

U-0	R/C-1	R-1	U-0	U-0	U-0	U-0	U-0
_	WRTB	WRTC ⁽¹⁾	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 **Unimplemented:** Read as '0'

bit 6 WRTB: Boot Block Write Protection bit

 $\tt 1$ = Boot block (000000-0007FFh) or (000000-000FFFh) is not write-protected $\tt 0$ = Boot block (000000-0007FFh) or (000000-000FFFh) is write-protected

bit 5 WRTC: Configuration Register Write Protection bit⁽¹⁾

1 = Configuration registers (300000-3000FFh) are not write-protected 0 = Configuration registers (300000-3000FFh) are write-protected

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is read-only in normal execution mode; it can be written only in Program mode.

REGISTER 18-11: CONFIG7L: CONFIGURATION REGISTER 7 LOW (BYTE ADDRESS 30000Ch)

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
_	_	_	_	_	_	EBTR1	EBTR0
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **EBTR1:** Table Read Protection bit

1 = Block 1 (002000-003FFFh) is not protected from table reads executed in other blocks 0 = Block 1 (002000-003FFFh) is protected from table reads executed in other blocks

bit 0 **EBTR0**: Table Read Protection bit

1 = Block 0 (000800-001FFFh) or (001000-001FFFh) is not protected from table reads executed in other blocks

0 = Block 0 (000800-001FFFh) or (001000-001FFFh) is protected from table reads executed in other blocks

REGISTER 18-12: CONFIG7H: CONFIGURATION REGISTER 7 HIGH (BYTE ADDRESS 30000Dh)

U-0	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
_	EBTRB	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7 Unimplemented: Read as '0'

bit 6 EBTRB: Boot Block Table Read Protection bit

1 = Boot block (000000-0007FFh) or (000000-000FFFh) is not protected from table reads executed in other blocks

0 = Boot block (000000-0007FFh) or (000000-000FFFh) is protected from table reads executed in other blocks

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 18-13: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2450/4450 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:

R = Read-only bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-5 **DEV2:DEV0:** Device ID bits

001 = PIC18F2450 000 = PIC18F4450

bit 4-0 **REV4:REV0:** Revision ID bits

These bits are used to indicate the device revision.

REGISTER 18-14: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2450/4450 DEVICES

R	R	R	R	R	R	R	R
DEV10 ⁽¹⁾	DEV9 ⁽¹⁾	DEV8 ⁽¹⁾	DEV7 ⁽¹⁾	DEV6 ⁽¹⁾	DEV5 ⁽¹⁾	DEV4 ⁽¹⁾	DEV3 ⁽¹⁾
bit 7							bit 0

Legend:

R = Read-only bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed u = Unchanged from programmed state

bit 7-0 **DEV10:DEV3:** Device ID bits⁽¹⁾

These bits are used with the DEV2:DEV0 bits in the DEVID1 register to identify the part number.

0010 0100 = PIC18F2450/4450 devices

Note 1: These values for DEV10:DEV3 may be shared with other devices. The specific device is always identified by using the entire DEV10:DEV0 bit sequence.

18.2 Watchdog Timer (WDT)

For PIC18F2450/4450 devices, the WDT is driven by the INTRC source. When the WDT is enabled, the clock source is also enabled. The nominal WDT period is 4 ms and has the same stability as the INTRC oscillator.

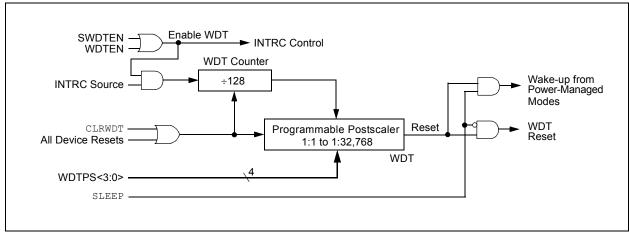
The 4 ms period of the WDT is multiplied by a 16-bit postscaler. Any output of the WDT postscaler is selected by a multiplexer, controlled by bits in Configuration Register 2H. Available periods range from 4 ms to 131.072 seconds (2.18 minutes). The WDT and postscaler are cleared when any of the following events occur: a SLEEP or CLRWDT instruction is executed or a clock failure has occurred.

- **Note 1:** The CLRWDT and SLEEP instructions clear the WDT and postscaler counts when executed.
 - **2:** When a CLRWDT instruction is executed, the postscaler count will be cleared.

18.2.1 CONTROL REGISTER

Register 18-15 shows the WDTCON register. This is a readable and writable register which contains a control bit that allows software to override the WDT enable Configuration bit, but only if the Configuration bit has disabled the WDT.

FIGURE 18-1: WDT BLOCK DIAGRAM



REGISTER 18-15: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	_	_	_	_	_	SWDTEN ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit⁽¹⁾

1 = Watchdog Timer is on0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bit, WDTEN, is enabled.

TABLE 18-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
RCON	IPEN	SBOREN ⁽¹⁾	_	RI	TO	PD	POR	BOR	50
WDTCON	_	_	_	_	_	_	_	SWDTEN	50

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

Note 1: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.

18.3 Two-Speed Start-up

The Two-Speed Start-up feature helps to minimize the latency period, from oscillator start-up to code execution, by allowing the microcontroller to use the INTRC oscillator as a clock source until the primary clock source is available. It is enabled by setting the IESO Configuration bit.

Two-Speed Start-up should be enabled only if the primary oscillator mode is XT, HS, XTPLL or HSPLL (Crystal-Based modes). Other sources do not require an Oscillator Start-up Timer delay; for these, Two-Speed Start-up should be disabled.

When enabled, Resets and wake-ups from Sleep mode cause the device to configure itself to run from the internal oscillator as the clock source, following the time-out of the Power-up Timer after a Power-on Reset is enabled. This allows almost immediate code execution while the primary oscillator starts and the OST is running. Once the OST times out, the device automatically switches to PRI_RUN mode.

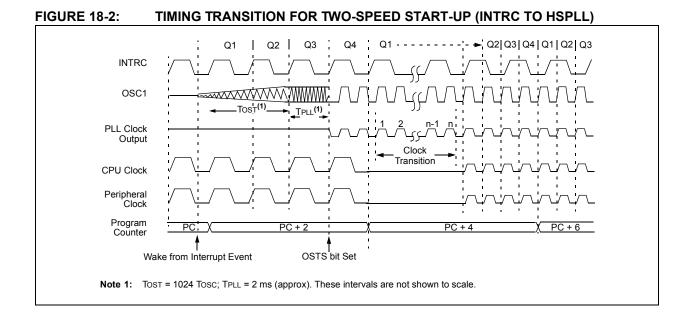
Because the OSCCON register is cleared on Reset events, the INTRC clock is used directly at its base frequency.

In all other power-managed modes, Two-Speed Start-up is not used. The device will be clocked by the currently selected clock source until the primary clock source becomes available. The setting of the IESO bit is ignored.

18.3.1 SPECIAL CONSIDERATIONS FOR USING TWO-SPEED START-UP

While using the INTRC oscillator in Two-Speed Start-up, the device still obeys the normal command sequences for entering power-managed modes, including serial SLEEP instructions (refer to **Section 3.1.4 "Multiple Sleep Commands"**). In practice, this means that user code can change the SCS1:SCS0 bit settings or issue SLEEP instructions before the OST times out. This would allow an application to briefly wake-up, perform routine "housekeeping" tasks and return to Sleep before the device starts to operate from the primary oscillator.

User code can also check if the primary clock source is currently providing the device clocking by checking the status of the OSTS bit (OSCCON<3>). If the bit is set, the primary oscillator is providing the clock. Otherwise, the internal oscillator is providing the clock during wake-up from Reset or Sleep mode.



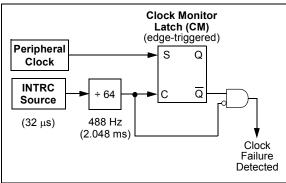
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18.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the microcontroller to continue operation in the event of an external oscillator failure by automatically switching the device clock to the internal oscillator. The FSCM function is enabled by setting the FCMEN Configuration bit.

When FSCM is enabled, the INTRC oscillator runs at all times to monitor clocks to peripherals and provide a backup clock in the event of a clock failure. Clock monitoring (shown in Figure 18-3) is accomplished by creating a sample clock signal, which is the INTRC output divided by 64. This allows ample time between FSCM sample clocks for a peripheral clock edge to occur. The peripheral device clock and the sample clock are presented as inputs to the Clock Monitor latch (CM). The CM is set on the falling edge of the device clock source, but cleared on the rising edge of the sample clock.

FIGURE 18-3: FSCM BLOCK DIAGRAM



Clock failure is tested for on the falling edge of the sample clock. If a sample clock falling edge occurs while CM is still set, a clock failure has been detected (Figure 18-4). This causes the following:

- the FSCM generates an oscillator fail interrupt by setting bit, OSCFIF (PIR2<7>);
- the device clock source is switched to the internal oscillator (OSCCON is not updated to show the current clock source – this is the fail-safe condition); and
- · the WDT is reset.

The FSCM will detect failures of the primary or secondary clock sources only. If the internal oscillator fails, no failure would be detected, nor would any action be possible.

18.4.1 FSCM AND THE WATCHDOG TIMER

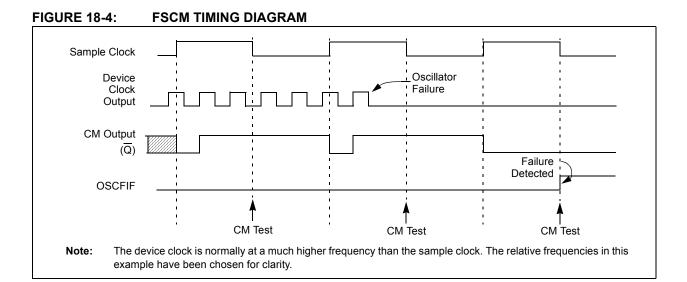
Both the FSCM and the WDT are clocked by the INTRC oscillator. Since the WDT operates with a separate divider and counter, disabling the WDT has no effect on the operation of the INTRC oscillator when the FSCM is enabled.

If the WDT is enabled with a small prescale value, a decrease in clock speed allows a WDT time-out to occur and a subsequent device Reset. For this reason, Fail-Safe Clock Monitor events also reset the WDT and postscaler, allowing it to start timing from when execution speed was changed and decreasing the likelihood of an erroneous time-out.

18.4.2 EXITING FAIL-SAFE OPERATION

The fail-safe condition is terminated by either a device Reset or by entering a power-managed mode. On Reset, the controller starts the primary clock source specified in Configuration Register 1H (with any start-up delays that are required for the oscillator mode, such as OST or PLL timer). The INTRC provides the device clock until the primary clock source becomes ready (similar to a Two-Speed Start-up). The clock source is then switched to the primary clock (indicated by the OSTS bit in the OSCCON register becoming set). The Fail-Safe Clock Monitor then resumes monitoring the peripheral clock.

The primary clock source may never become ready during start-up. In this case, operation is clocked by the INTRC. The OSCCON register will remain in its Reset state until a power-managed mode is entered.



18.4.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexer selects the clock source selected by the OSCCON register. Fail-Safe Clock Monitoring of the powermanaged clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTRC. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, subsequent interrupts while in Idle mode will cause the CPU to begin executing instructions while being clocked by the INTRC source.

18.4.4 POR OR WAKE-UP FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is either EC or INTRC, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, HSPLL or XT), the situation is somewhat different. Since the oscillator may require a start-up time

considerably longer than the FCSM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator is automatically configured as the device clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on POR or wake from Sleep will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

As noted in **Section 18.3.1 "Special Considerations for Using Two-Speed Start-up"**, it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new power-managed mode is selected, the primary clock is disabled.

18.5 Program Verification and Code Protection

The overall structure of the code protection on the PIC18 Flash devices differs significantly from other PIC® microcontrollers.

The user program memory is divided into three blocks. One of these is a boot block of 1 or 2 Kbytes. The remainder of the memory is divided into two blocks on binary boundaries.

Each of the three blocks has three code protection bits associated with them. They are:

- Code-Protect bit (CPx)
- Write-Protect bit (WRTx)
- · External Block Table Read bit (EBTRx)

Figure 18-5 shows the program memory organization for 24 and 32-Kbyte devices and the specific code protection bit associated with each block. The actual locations of the bits are summarized in Table 18-3.

FIGURE 18-5: CODE-PROTECTED PROGRAM MEMORY FOR PIC18F2450/4450

MEMORY SIZE/DEVICE		Block Code Protection
16 Kbytes (PIC18F2450/4450)	Address Range	Controlled By:
Boot Block	000000h 0007FFh 000FFFh	CPB, WRTB, EBTRB
Block 0	001000h 001FFFh	CP0, WRT0, EBTR0
Block 1	002000h 003FFFh	CP1, WRT1, EBTR1
Unimplemented Read '0's		
Unimplemented Read '0's		
Unimplemented Read '0's		(Unimplemented Memory Space)
	1FFFFFh	

TABLE 18-3: SUMMARY OF CODE PROTECTION REGISTERS

File	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
300008h	CONFIG5L	_	_	_	_	_	_	CP1	CP0
300009h	CONFIG5H	_	СРВ	_	_	_	_	_	_
30000Ah	CONFIG6L	_	_	_	_	_	_	WRT1	WRT0
30000Bh	CONFIG6H	_	WRTB	WRTC	_	_	_	_	_
30000Ch	CONFIG7L	_	_	_	_	_	_	EBTR1	EBTR0
30000Dh	CONFIG7H	_	EBTRB	_	_	_	_	_	_

Legend: Shaded cells are unimplemented.

18.5.1 PROGRAM MEMORY CODE PROTECTION

The program memory may be read to or written from any location using the table read and table write instructions. The device ID may be read with table reads. The Configuration registers may be read and written with the table read and table write instructions.

In normal execution mode, the CPx bits have no direct effect. CPx bits inhibit external reads and writes. A block of user memory may be protected from table writes if the WRTx Configuration bit is '0'. The EBTRx bits control table reads. For a block of user memory with the EBTRx bit set to '0', a table read instruction that executes from within that block is allowed to read.

A table read instruction that executes from a location outside of that block is not allowed to read and will result in reading '0's. Figure 18-6 through Figure 18-8 illustrate table write and table read protection.

Note: Code protection bits may only be written to a '0' from a '1' state. It is not possible to write a '1' to a bit in the '0' state. Code protection bits are only set to '1' by a full Chip Erase or Block Erase function. The full Chip Erase and Block Erase functions can only be initiated via ICSP operation or an external programmer.

FIGURE 18-6: TABLE WRITE (WRTx) DISALLOWED

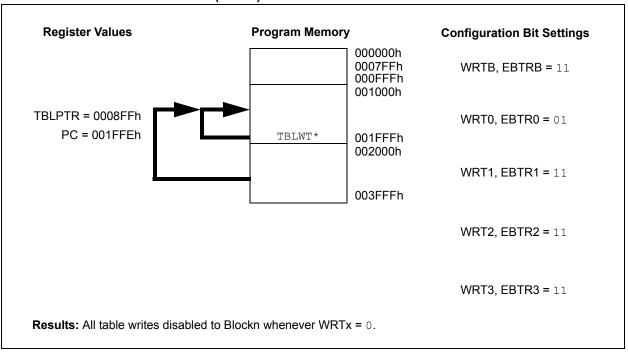


FIGURE 18-7: EXTERNAL BLOCK TABLE READ (EBTRx) DISALLOWED

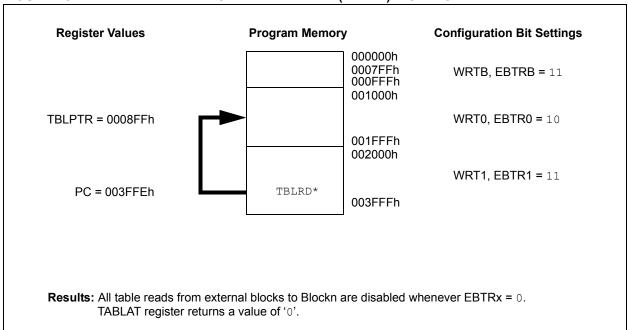
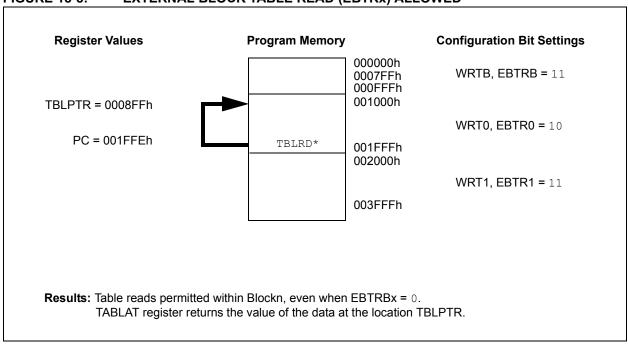


FIGURE 18-8: EXTERNAL BLOCK TABLE READ (EBTRx) ALLOWED



18.5.2 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In normal execution mode, the WRTC bit is readable only. WRTC can only be written via ICSP operation or an external programmer.

18.6 ID Locations

Eight memory locations (200000h-200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are both readable and writable during normal execution through the TBLRD and TBLWT instructions or during program/verify. The ID locations can be read when the device is code-protected.

18.7 In-Circuit Serial Programming

PIC18F2450/4450 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

18.8 In-Circuit Debugger

When the DEBUG Configuration bit is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® IDE. When the microcontroller has this feature enabled, some resources are not available for general use. Table 18-4 shows which resources are required by the background debugger.

TABLE 18-4: DEBUGGER RESOURCES

I/O pins:	RB6, RB7
Stack:	2 levels
Program Memory:	512 bytes
Data Memory:	10 bytes

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP/RE3, VDD, Vss, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

18.9 Special ICPORT Features (Designated Packages Only)

Under specific circumstances, the No Connect (NC) pins of PIC18F4450 devices in 44-pin TQFP packages can provide additional functionality. These features are controlled by device Configuration bits and are available only in this package type and pin count.

18.9.1 DEDICATED ICD/ICSP PORT

The 44-pin TQFP devices can use NC pins to provide an alternate port for In-Circuit Debugging (ICD) and In-Circuit Serial Programming (ICSP). These pins are collectively known as the dedicated ICSP/ICD port, since they are not shared with any other function of the device.

When implemented, the dedicated port activates three NC pins to provide an alternate device Reset, data and clock ports. None of these ports overlap with standard I/O pins, making the I/O pins available to the user's application.

The dedicated ICSP/ICD port is enabled by setting the ICPRT Configuration bit. The port functions the same way as the legacy ICSP/ICD port on RB6/RB7. Table 18-5 identifies the functionally equivalent pins for ICSP and ICD purposes.

TABLE 18-5: EQUIVALENT PINS FOR LEGACY AND DEDICATED ICD/ICSP™ PORTS

Pin Name		Pin	
Legacy Port	Dedicated Port	Type	Pin Function
MCLR/VPP/ RE3	NC/ICRST/ ICVPP	Р	Device Reset and Programming Enable
RB6/KBI2/ PGC	NC/ICCK/ ICPGC	I	Serial Clock
RB7/KBI3/ PGD	NC/ICDT/ ICPGD	I/O	Serial Data

Legend: I = Input, O = Output, P = Power

PIC18F2450/4450

Even when the dedicated port is enabled, the ICSP and ICD functions remain available through the legacy port. When VIHH is seen on the MCLR/VPP/RE3 pin, the state of the ICRST/ICVPP pin is ignored.

- **Note 1:** The ICPRT Configuration bit can only be programmed through the default ICSP port.
 - 2: The ICPRT Configuration bit must be maintained clear for all 28-pin and 40-pin devices; otherwise, unexpected operation may occur.

18.9.2 28-PIN EMULATION

PIC18F4450 devices in 44-pin TQFP packages also have the ability to change their configuration under external control for debugging purposes. This allows the device to behave as if it were a PIC18F2450/4450 28-pin device.

This 28-pin Configuration mode is controlled through a single pin, NC/ICPORTS. Connecting this pin to Vss forces the device to function as a 28-pin device. Features normally associated with the 40/44-pin devices are disabled, along with their corresponding control registers and bits. On the other hand, connecting the pin to VDD forces the device to function in its default configuration.

The configuration option is only available when background debugging and the dedicated ICD/ICSP port are both enabled (DEBUG Configuration bit is clear and ICPRT Configuration bit is set). When disabled, NC/ICPORTS is a No Connect pin.

18.10 Single-Supply ICSP Programming

The LVP Configuration bit enables Single-Supply ICSP Programming (formerly known as *Low-Voltage ICSP Programming* or *LVP*). When Single-Supply Programming is enabled, the microcontroller can be programmed without requiring high voltage being applied to the MCLR/VPP/RE3 pin, but the RB5/KB11/PGM pin is then dedicated to controlling Program mode entry and is not available as a general purpose I/O pin.

While programming using <u>Single-Supply Programming</u>, VDD is applied to the $\overline{MCLR/VPP/RE3}$ pin as in normal execution mode. To enter Programming mode, VDD is applied to the PGM pin.

- **Note 1:** High-Voltage Programming is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR pin.
 - 2: While in Low-Voltage ICSP Programming mode, the RB5 pin can no longer be used as a general purpose I/O pin and should be held low during normal operation.
 - **3:** When using Low-Voltage ICSP Programming (LVP) and the pull-ups on PORTB are enabled, bit 5 in the TRISB register must be cleared to disable the pull-up on RB5 and ensure the proper operation of the device.
 - **4:** If the device Master Clear is disabled, verify that either of the following is done to ensure proper entry into ICSP mode:
 - a) Disable Low-Voltage Programming (CONFIG4L<2> = 0); or
 - b) Make certain that RB5/KBI1/PGM is held low during entry into ICSP.

If Single-Supply ICSP Programming mode will not be used, the LVP bit can be cleared. RB5/KBI1/PGM then becomes available as the digital I/O pin, RB5. The LVP bit may be set or cleared only when using standard high-voltage programming (VIHH applied to the MCLR/VPP/RE3 pin). Once LVP has been disabled, only the standard high-voltage programming is available and must be used to program the device.

Memory that is not code-protected can be erased using either a Block Erase, or erased row by row, then written at any specified VDD. If code-protected memory is to be erased, a Block Erase is required. If a Block Erase is to be performed when using Low-Voltage Programming, the device must be supplied with VDD of 4.5V to 5.5V.

19.0 INSTRUCTION SET SUMMARY

PIC18F2450/4450 devices incorporate the standard set of 75 PIC18 core instructions, as well as an extended set of eight new instructions for the optimization of code that is recursive or that utilizes a software stack. The extended set is discussed later in this section.

19.1 Standard Instruction Set

The standard PIC18 instruction set adds many enhancements to the previous PIC MCU instruction sets, while maintaining an easy migration from these PIC MCU instruction sets. Most instructions are a single program memory word (16 bits) but there are four instructions that require two program memory locations.

Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- Byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- · Control operations

The PIC18 instruction set summary in Table 19-2 lists byte-oriented, bit-oriented, literal and control operations. Table 19-1 shows the opcode field descriptions.

Most byte-oriented instructions have three operands:

- 1. The file register (specified by 'f')
- 2. The destination of the result (specified by 'd')
- 3. The accessed memory (specified by 'a')

The file register designator, 'f', specifies which file register is to be used by the instruction. The destination designator, 'd', specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the WREG register. If 'd' is '1', the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

- 1. The file register (specified by 'f')
- The bit in the file register (specified by 'b')
- 3. The accessed memory (specified by 'a')

The bit field designator 'b' selects the number of the bit affected by the operation, while the file register designator, 'f', represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a file register (specified by 'k')
- The desired FSR register to load the literal value into (specified by 'f')
- No operand required (specified by '—')

The **control** instructions may use some of the following operands:

- A program memory address (specified by 'n')
- The mode of the CALL or RETURN instructions (specified by 's')
- The mode of the table read and table write instructions (specified by 'm')
- No operand required (specified by '—')

All instructions are a single word, except for four double-word instructions. These instructions were made double-word to contain the required information in 32 bits. In the second word, the 4 MSbs are '1's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs . If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs . Two-word branch instructions (if true) would take 3 μs .

Figure 19-1 shows the general formats that the instructions can have. All examples use the convention 'nnh' to represent a hexadecimal number.

The instruction set summary, shown in Table 19-2, lists the standard instructions recognized by the Microchip MPASM™ Assembler.

Section 19.1.1 "Standard Instruction Set" provides a description of each instruction.

PIC18F2450/4450

TABLE 19-1: OPCODE FIELD DESCRIPTIONS

Field	Description
a	RAM access bit
	a = 0: RAM location in Access RAM (BSR register is ignored)
	a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7).
BSR	Bank Select Register. Used to select the current RAM bank.
C, DC, Z, OV, N	ALU Status bits: Carry, Digit Carry, Zero, Overflow, Negative.
d	Destination select bit
	d = 0: store result in WREG d = 1: store result in file register f
dest	Destination: either the WREG register or the specified register file location.
f	8-bit register file address (00h to FFh) or 2-bit FSR designator (0h to 3h).
f _s	12-bit register file address (000h to FFFh). This is the source address.
f _d	12-bit register file address (000h to FFFh). This is the destination address.
GIE	Global Interrupt Enable bit.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value).
label	Label name.
	The mode of the TBLPTR register for the table read and table write instructions.
mm	Only used with table read and table write instructions:
*	No change to register (such as TBLPTR with table reads and writes)
*+	Post-Increment register (such as TBLPTR with table reads and writes)
*-	Post-Decrement register (such as TBLPTR with table reads and writes)
+*	Pre-Increment register (such as TBLPTR with table reads and writes)
n	The relative address (2's complement number) for relative branch instructions or the direct address for
11	Call/Branch and Return instructions.
PC	Program Counter.
PCL	Program Counter Low Byte.
PCH	Program Counter High Byte.
PCLATH	Program Counter High Byte Latch.
PCLATU	Program Counter Upper Byte Latch.
PD	Power-Down bit.
PRODH	Product of Multiply High Byte.
PRODL	Product of Multiply Low Byte.
S	Fast Call/Return mode select bit
	s = 0: do not update into/from shadow registers
	s = 1: certain registers loaded into/from shadow registers (Fast mode)
TBLPTR	21-bit Table Pointer (points to a program memory location).
TABLAT	8-bit Table Latch.
TO	Time-out bit.
TOS	Top-of-Stack.
u	Unused or unchanged.
WDT	Watchdog Timer.
WREG	Working register (accumulator).
х	Don't care ('0' or '1'). The assembler will generate code with $x = 0$. It is the recommended form of use for
	compatibility with all Microchip software tools.
Z _S	7-bit offset value for indirect addressing of register files (source).
z _d	7-bit offset value for indirect addressing of register files (destination).
{ }	Optional argument.
[text]	Indicates an indexed address.
(text)	The contents of text.
[expr] <n></n>	Specifies bit n of the register indicated by the pointer, expr.
\rightarrow	Assigned to.
< >	Register bit field.
€	In the set of.
_	

FIGURE 19-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations **Example Instruction** ADDWF MYREG, W, B OPCODE f (FILE #) d а d = 0 for result destination to be WREG register d = 1 for result destination to be file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address Byte to Byte move operations (2-word) 12 11 OPCODE f (Source FILE #) MOVFF MYREG1, MYREG2 15 12 11 0 1111 f (Destination FILE #) f = 12-bit file register address Bit-oriented file register operations 9 8 7 12 11 OPCODE b (BIT#) a f (FILE #) BSF MYREG, bit, B b = 3-bit position of bit in file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address Literal operations 15 8 7 0 OPCODE k (literal) MOVLW 7Fh k = 8-bit immediate value **Control** operations CALL, GOTO and Branch operations 15 8 7 0 n<7:0> (literal) GOTO Label OPCODE 15 12 11 1111 n<19:8> (literal) n = 20-bit immediate value 15 CALL MYFUNC **OPCODE** n<7:0> (literal) 15 12 11 0 n<19:8> (literal) 1111 S = Fast bit 15 0 11 10 OPCODE n<10:0> (literal) BRA MYFUNC 15 8 7 BC MYFUNC **OPCODE** n<7:0> (literal)

TABLE 19-2: PIC18FXXXX INSTRUCTION SET

Mnemonic,		Description	Cycles	16-	Bit Instr	uction W	/ord	Status	Notes
Opera	nds	Description	Cycles	MSb LSb		Affected	Notes		
BYTE-ORII	ENTED (PERATIONS							
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1, 2
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1, 2
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1,2
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	2
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1, 2
CPFSEQ	f, a	Compare f with WREG, Skip =	1 (2 or 3)	0110	001a	ffff	ffff	None	4
CPFSGT	f, a	Compare f with WREG, Skip >	1 (2 or 3)	0110	010a	ffff	ffff	None	4
CPFSLT	f, a	Compare f with WREG, Skip <	1 (2 or 3)	0110	000a	ffff	ffff	None	1, 2
DECF	f, d, a	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None	1, 2, 3, 4
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100	11da	ffff	ffff	None	1, 2
INCF	f, d, a	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None	4
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100	10da	ffff	ffff	None	1, 2
IORWF	f, d, a	Inclusive OR WREG with f	1 ` ′	0001	00da	ffff	ffff	Z, N	1, 2
MOVF	f, d, a	Move f	1	0101	00da	ffff	ffff	Z, N	1
MOVFF	f_s , f_d	Move f _s (source) to 1st word	2	1100	ffff	ffff	ffff	None	
	3. u	f _d (destination) 2nd word		1111	ffff	ffff	ffff		
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None	
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	1, 2
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N	,
RLCF	f, d, a	Rotate Left f through Carry	1	0011	01da	ffff	ffff	C, Z, N	1, 2
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff	ffff	Z, N	,
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	Ć, Z, N	
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff	Z, N	
SETF	f, a	Set f	1	0110	100a	ffff	ffff	None	1, 2
SUBFWB	f, d, a	Subtract f from WREG with	1	0101	01da	ffff	ffff	C, DC, Z, OV, N	,
		Borrow							
SUBWF	f, d, a	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N	1, 2
SUBWFB	f, d, a	Subtract WREG from f with	1	0101	10da	ffff	ffff	C, DC, Z, OV, N	
	, -,	Borrow						, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
SWAPF	f, d, a	Swap Nibbles in f	1	0011	10da	ffff	ffff	None	4
TSTFSZ	f, a	Test f, Skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None	1, 2
XORWF	f, d, a	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N	

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as an input and is driven low by an external device, the data will be written back with a '0'.

^{2:} If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

^{3:} If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

^{4:} Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

TABLE 19-2: PIC18FXXXX INSTRUCTION SET (CONTINUED)

Mnemo	onic,	Description	Cycles	16-Bit Instruction Word		Status	Notes		
Opera	nds	Description	Cycles	MSb			LSb	Affected	Notes
BIT-ORIEN	ITED OP	ERATIONS							
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, d, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2
CONTROL	OPERA	TIONS	•						
ВС	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	1 (2)	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	n, s	Call Subroutine 1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
CLRWDT	_	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	_	Decimal Adjust Wreg	1	0000	0000	0000	0111	С	
GOTO	n	Go To Address 1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
NOP	_	No Operation	1	0000	0000	0000	0000	None	
NOP	_	No Operation	1	1111	XXXX	XXXX	XXXX	None	4
POP	_	Pop Top of Return Stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	_	Push Top of Return Stack (TOS)		0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software Device Reset	1	0000	0000	1111	1111	All	
RETFIE	S	Return from Interrupt Enable	2	0000	0000	0001	000s	GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with Literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	s	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	_	Go into Standby mode	1	0000	0000	0000	0011	TO, PD	

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as an input and is driven low by an external device, the data will be written back with a '0'.

^{2:} If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

^{3:} If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

^{4:} Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

TABLE 19-2: PIC18FXXXX INSTRUCTION SET (CONTINUED)

Mnemonic,		Description	Cycles	16-	Bit Inst	ruction	Word	Status	Notes
Oper	ands	Description	Cycles	MSb LSb		Affected	Notes		
LITERAL	OPERATI	ONS							
ADDLW	k	Add Literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND Literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR Literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f, k	Move Literal (12-bit) 2nd word	2	1110	1110	00ff	kkkk	None	
		to FSR(f) 1st word		1111	0000	kkkk	kkkk		
MOVLB	k	Move Literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW	k	Move Literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW	k	Multiply Literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW	k	Return with Literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW	k	Subtract WREG from Literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR Literal with	1	0000	1010	kkkk	kkkk	Z, N	
		WREG							
DATA ME	MORY ↔	PROGRAM MEMORY OPERATI	ONS						
TBLRD*		Table Read	2	0000	0000	0000	1000	None	
TBLRD*+		Table Read with Post-Increment		0000	0000	0000	1001	None	
TBLRD*-		Table Read with Post-Decrement		0000	0000	0000	1010	None	
TBLRD+*		Table Read with Pre-Increment		0000	0000	0000	1011	None	
TBLWT*		Table Write	2	0000	0000	0000	1100	None	
TBLWT*+		Table Write with Post-Increment		0000	0000	0000	1101	None	
TBLWT*-		Table Write with Post-Decrement		0000	0000	0000	1110	None	
TBLWT+*		Table Write with Pre-Increment		0000	0000	0000	1111	None	

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as an input and is driven low by an external device, the data will be written back with a '0'.

- 2: If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.
- 3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

19.1.1 STANDARD INSTRUCTION SET

ADD	LW	ADD Litera	al to W					
Synta	ax:	ADDLW	k					
Oper	ands:	$0 \le k \le 255$	$0 \leq k \leq 255$					
Oper	ation:	$(W) + k \rightarrow V$	$(W) + k \rightarrow W$					
Statu	s Affected:	N, OV, C, E	C, Z					
Enco	ding:	0000	1111	kkkk	kkkk			
Desc	ription:	The conten 8-bit literal W.						
Word	ls:	1	1					
Cycle	es:	1	1					
QC	ycle Activity:							
	Q1	Q2	Q3	1	Q4			
	Decode	Read	Proce	ss Wr	ite to W			
		literal 'k'	Data	a .				

Example: ADDLW 15h

 $\begin{array}{rcl} \text{Before Instruction} & & \\ W & = & 10\text{h} \\ \text{After Instruction} & & \\ W & = & 25\text{h} \end{array}$

ADD	WF	ADD W to	f					
Synta	ax:	ADDWF	ADDWF f {,d {,a}}					
Oper	ands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$	d ∈ [0,1]					
Oper	ation:	$(W) + (f) \rightarrow$	dest					
Statu	s Affected:	N, OV, C, E)C, Z					
Enco	ding:	0010	01da	fff	f	ffff		
Desc	ription:	Add W to register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.						
Word	ls:	1	1					
Cycle	es:	1	1					
QC	ycle Activity:							
	Q1	Q2 Q3 Q4						
	Decode	Read register 'f'	Proce Data			rite to stination		

Example: ADDWF REG, 0, 0

Before Instruction

W = 17h REG = 0C2h

After Instruction

W = 0D9hREG = 0C2h

Note: All PIC18 instructions may take an optional label argument, preceding the instruction mnemonic, for use in symbolic addressing. If a label is used, the instruction format then becomes: {label} instruction argument(s).

ADDWFC ADD W and Carry bit to f

Syntax: **ADDWFC** f {,d {,a}} Operands: $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$

Operation: $(W) + (f) + (C) \rightarrow dest$ N, OV, C, DC, Z Status Affected:

Encoding: 0010 ffff ffff

Description: Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

> GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and

Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: ADDWFC REG, 0, 1

50h

Before Instruction

Carry bit = REG W 02h 4Dh After Instruction Carry bit = 02h REG W

ANDLW AND Literal with W

Syntax: ANDLW Operands: $0 \le k \le 255$ Operation: (W) .AND. $k \rightarrow W$

Status Affected: N, Z

Encoding: 0000 1011 kkkk kkkk

The contents of W are ANDed with the Description: 8-bit literal 'k'. The result is placed in W.

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to W
	'k'	Data	

Example: 05Fh ANDLW

> Before Instruction A3h W

After Instruction

W 03h **ANDWF** AND W with f Syntax: ANDWF $f \{ d \{ a \} \}$ Operands: $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$ Operation: (W) .AND. (f) \rightarrow dest Status Affected: N, Z Encoding: 0001 01da ffff ffff Description: The contents of W are ANDed with

register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).

If 'a' is '0', the Access Bank is selected.

If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: ANDWF REG, 0, 0

Before Instruction

W = 17h REG = C2hAfter Instruction

W = 02hREG = C2h

BC	Branch if Carry
----	-----------------

Syntax: BC n

Operands: $-128 \le n \le 127$ Operation: if Carry bit is '1', $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0010 nnnn nnnn

Description: If the Carry bit is '1', then the program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have

incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a

two-cycle instruction.

Words: 1
Cycles: 1(2)

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE BC 5

Before Instruction

PC = address (HERE)

After Instruction

If Carry = 1; PC = ac

PC = address (HERE + 12)
If Carry = 0;

PC = address (HERE + 2)

BCF	Bit Clear	f		
Syntax:	BCF f, b	o {,a}		
Operands:	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$	5		
Operation:	$0 \rightarrow f < b >$			
Status Affected:	None			
Encoding:	1001	bbba	ffff	ffff
Description:	Bit 'b' in re	0	s cleared.	aalaatad

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and **Bit-Oriented Instructions in Indexed** Literal Offset Mode" for details.

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: FLAG_REG, 7, 0 BCF

Before Instruction FLAG_REG = C7h After Instruction FLAG_REG = 47h

BN	Branch if	Negative		
Syntax:	BN n			
Operands:	-128 ≤ n ≤	127		
Operation:	if Negative bit is '1', (PC) + 2 + 2n → PC			
Status Affected:	None			
Encoding:	1110	0110	nnnn	nnnn
Description:	If the Nega		,	he

The 2's complement number '2n' is added to the PC. Since the PC will have

incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a

two-cycle instruction.

Words: 1 Cycles: 1(2)

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE Jump

Before Instruction

PC address (HERE)

After Instruction

If Negative PC 1;

address (Jump)

0; address (HERE + 2)

BNC Branch if Not Carry Syntax: BNC n Operands: $\text{-}128 \leq n \leq 127$ Operation: if Carry bit is '0', $(PC) + 2 + 2n \rightarrow PC$ Status Affected: None Encoding: 1110 0011 nnnn nnnn Description: If the Carry bit is '0', then the program

will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next

instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1 1(2) Cycles:

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE BNC Jump

Before Instruction

PC address (HERE)

After Instruction

If Carry PC 0.

= address (Jump) If Carry PC

address (HERE + 2)

BNN Branch if Not Negative

Syntax: BNN n Operands: $\text{-}128 \leq n \leq 127$ Operation: if Negative bit is '0',

Status Affected: None

Encoding: 1110 0111 nnnn nnnn

If the Negative bit is '0', then the Description:

program will branch.

 $(PC) + 2 + 2n \rightarrow PC$

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next

instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

1(2) Cycles:

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	ʻn'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE BNN Jump

Before Instruction

PC address (HERE)

After Instruction

If Negative PC 0.

= address (Jump) If Negative PC =

address (HERE + 2)

BNOV	Branch if Not Overflow	
Syntax:	BNOV n	
Operands:	$-128 \le n \le 127$	
Operation:	if Overflow bit is '0', (PC) + 2 + 2n \rightarrow PC	
Status Affected:	None	
Encoding:	1110 0101 nnnn nnnn	
Description:	If the Overflow bit is '0', then the program will branch. The 2's complement number '2n' is	

added to the PC. Since the PC will have incremented to fetch the next

instruction, the new address will be PC + 2 + 2n. This instruction is then a

two-cycle instruction.

Words: 1 Cycles: 1(2)

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE BNOV Jump

Before Instruction

PC address (HERE)

After Instruction

If Overflow 0:

address (Jump) PC

If Overflow PC

1; address (HERE + 2)

BNZ **Branch if Not Zero**

Syntax: BNZ n

Operands: $\text{-}128 \leq n \leq 127$ Operation: if Zero bit is '0',

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Description:

Encoding: 1110 0001 nnnn nnnn

> If the Zero bit is '0', then the program will branch.

> > The 2's complement number '2n' is added to the PC. Since the PC will have

incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a

two-cycle instruction.

Words: 1 Cycles: 1(2)

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	ʻn'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE BNZ Jump

Before Instruction

PC address (HERE)

After Instruction

If Zero 0;

address (Jump)

If Zero PC 1; address (HERE + 2) BRA Unconditional Branch

Syntax: BRA n

Operands: $-1024 \le n \le 1023$ Operation: $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1101 Onnn nnnn nnnn

Description: Add the 2's complement number '2n' to

the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a

two-cycle instruction.

Words: 1
Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	ʻn'	Data	
No	No	No	No
operation	operation	operation	operation

Example: HERE BRA Jump

Before Instruction

PC = address (HERE)

After Instruction

PC = address (Jump)

BSF	Bit Set f
Syntax:	BSF f, b {,a}
Operands:	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$
Operation:	$1 \rightarrow f < b >$
Status Affected:	None
Encoding:	1000 bbba ffff ffff
Description	Dit 'h' in register 'f' is set

Description: Bit 'b' in register 'f' is set.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

1

Cycles: 1

Q Cycle Activity:

Words:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: BSF FLAG_REG, 7, 1

Before Instruction

FLAG_REG = 0Ah After Instruction FLAG_REG = 8Ah

BTFS	С	Bit Test File	, Skip if Clear	,	BTF	ss	Bit Test File	, Skip if Set	
Synta	x:	BTFSC f, b	{,a}		Synta	ax:	BTFSS f, b	{,a}	
Opera	ands:	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$			Oper	ands:	$0 \le f \le 255$ $0 \le b < 7$ $a \in [0,1]$		
Opera	ation:	skip if (f)	= 0		Oper	ation:	skip if (f)	= 1	
Status	Affected:	None			Statu	s Affected:	None		
Encod	ding:	1011	bbba ff	ff ffff	Enco	ding:	1010	bbba ff:	ff ffff
Description: If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.		Desc	ription:	instruction is the next instruction and a NOP is this a two-cy If 'a' is '0', the 'a' is '1', the GPR bank (of If 'a' is '0' an set is enable in Indexed L mode where See Section Bit-Oriented	gister 'f' is '1', t skipped. If bit ruction fetched uction executio executed instruction. e Access Bank BSR is used to default). d the extended d, this instructi iteral Offset Ad ever f ≤ 95 (5Fh 19.2.3 "Byte- d Instructions et Mode" for de	'b' is '1', then during the n is discarded ead, making is selected. If select the distriction on operates dressing n). Oriented and in Indexed			
Words	s:	1			Word	ls:	1		
Cycles	s:		cles if skip and 2-word instruc		Cycle	es:		cles if skip and	
Q Cy	cle Activity:	•			QC	ycle Activity:	·		
	Q1	Q2	Q3	Q4		Q1	Q2	Q3	Q4
	Decode	Read	Process	No		Decode	Read	Process	No
		register 'f'	Data	operation			register 'f'	Data	operation
lf skip		00	00	04	lf sk	•	00	00	0.4
Г	Q1 No	Q2 No	Q3 No	Q4 No		Q1 No	Q2 No	Q3 No	Q4 No
	operation	operation	operation	operation		operation	operation	operation	operation
If skip	p and followed	by 2-word ins			If skip and followed by 2-word instruction:				
	Q1	Q2	Q3	Q4		Q1	Q2	Q3	Q4
	No	No	No	No		No	No	No	No
-	operation	operation	operation	operation		operation	operation	operation	operation
	No	No	No	No		No	No	No	No
L	operation	operation	operation	operation		operation	operation	operation	operation
	<u>ple:</u> Before Instruct PC After Instructio	FALSE : TRUE : ion = add	ress (HERE)	, 1, 0		nple: Before Instruct PC After Instructio	FALSE : TRUE : tion = add	ress (HERE)	, 1, 0
	If FLAG< PC If FLAG< PC	1> = 0; = add 1> = 1;	ress (FALSE)			If FLAG< PC If FLAG< PC	1> = 0; = add 1> = 1;	ress (FALSE)	

BTG Bit Toggle f Syntax: BTG f, b {,a} Operands: $0 \le f \le 255$ $0 \le b < 7$ $a \in [0,1]$ $(\overline{f < b >}) \rightarrow f < b >$ Operation: Status Affected: None Encoding: 0111 bbba ffff ffff Bit 'b' in data memory location 'f' is Description:

inverted.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and **Bit-Oriented Instructions in Indexed** Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: BTG PORTC, 4, 0

Before Instruction:

PORTC = 0111 0101 [75h]

After Instruction:

PORTC = 0110 0101 [65h]

BOV	Branch if Overflow

Syntax: BOV n Operands: $\text{-}128 \leq n \leq 127$ Operation: if Overflow bit is '1',

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0100 nnnn nnnn

Description: If the Overflow bit is '1', then the

program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next

instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	ʻn'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example: HERE BOV Jump

Before Instruction

PC address (HERE)

After Instruction

If Overflow 1:

PC = address (Jump) If Overflow PC =

address (HERE + 2)

BZ	Branch if Zero			
Syntax:	BZ n			
Operands:	$-128 \le n \le 127$			
Operation:	if Zero bit is '1', (PC) + 2 + 2n \rightarrow PC			
Status Affected:	None			
Encoding:	1110 0000 nnnn nnnn			
Description:	If the Zero bit is '1', then the program will branch. The 2's complement number '2n' is added to the BC. Since the BC will have			

added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a

two-cycle instruction.

Words: Cycles: 1(2)

Q Cycle Activity: If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	ʻn'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	ʻn'	Data	operation

Example:	HERE	BZ	Jump
Before Instru	uction		

After Instruction

PC

If Zero

PC address (Jump) If Zero PC

address (HERE + 2)

address (HERE)

CALL	Subroutine Call			
Syntax:	CALL k {	CALL k {,s}		
Operands:	$0 \le k \le 10$ $s \in [0,1]$	48575		
Operation:	$(PC) + 4 \rightarrow TOS,$ $k \rightarrow PC < 20:1>;$ if $s = 1,$ $(W) \rightarrow WS,$ $(STATUS) \rightarrow STATUSS,$ $(BSR) \rightarrow BSRS$			
Status Affected:	None			
Encoding: 1st word (k<7:0>) 2nd word(k<19:8>)	1110	110s	k ₇ kkk	kkkk ₀

2nd word(k<19:8>) Description:

1111 k ₁₉ kkk kk	kk kk	kk。
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	.1.1. 1.1.1	1_1_
1110 110s k ₇ 1	kkk kk	kko

Subroutine call of entire 2-Mbyte memory range. First, return address (PC + 4) is pushed onto the return stack. If 's' = 1, the W, STATUS and

registers are also pushed into their respective shadow registers, WS, STATUSS and BSRS. If 's' = 0, no update occurs (default). Then, the 20-bit value 'k' is loaded into PC<20:1>.

CALL is a two-cycle instruction.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Push PC to	Read literal
	'k'<7:0>,	stack	'k'<19:8>,
			Write to PC
No	No	No	No
operation	operation	operation	operation

Example: HERE CALL THERE, 1

Before Instruction

PC address (HERE)

After Instruction

PC address (THERE) TOS address (HERE + 4)

WS **BSRS BSR** STATUSS = **STATUS**

CLRF Clear f Syntax: CLRF f {,a} Operands: $0 \le f \le 255$ $a \in \left[0,1\right]$ $000h \rightarrow f$, Operation: $1 \rightarrow Z$ Status Affected: Ζ Encoding: 0110 101a ffff ffff Description: Clears the contents of the specified

register.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and **Bit-Oriented Instructions in Indexed** Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

_	Q1	Q2	Q3	Q4
	Decode	Read	Process	Write
		register 'f'	Data	register 'f'

Example: FLAG_REG,1 CLRF

Before Instruction

FLAG REG 5Ah After Instruction FLAG_REG 00h

CLRWDT	Clear Watchdog Timer				
Syntax:	CLRWDT				
Operands:	None				
Operation:	000h → WDT, 000h → WDT postscaler, 1 → \overline{TO} , 1 → \overline{PD}				
Status Affected:	TO, PD				
Encoding:	0000 0000 0000 0100				
Description:	CLRWDT instruction resets the				

Watchdog Timer. It also resets the postscaler of the WDT. Status bits, $\overline{\text{TO}}$

and \overline{PD} , are set.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	No
	operation	Data	operation

Example: CLRWDT

Before Instruction

WDT Counter ?

After Instruction

WDT Counter 00h WDT Postscaler 0 TO PD

COMF	Compleme	nt f		
Syntax:	COMF f	(,d {,a}}		
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$			
Operation:	$(\bar{f}) \rightarrow dest$			
Status Affected:	N, Z			
Encoding:	0001	11da	ffff	ffff
Description:	The content complement stored in W stored back If 'a' is '0', till f'a' is '1', till GPR bank (If 'a' is '0' a set is enable in Indexed I mode when Section 19 Bit-Oriente Literal Offs	ted. If 'd' is . If 'd' is in regist the Acces the BSR i (default). the exit of the exit	' is '0', the rector 'f' (defines Bank is sused to the struction of the second of the	e result is sult is sult is sult. selected. select the estruction operates essing See ed and Indexed
Words:	1			
Cycles:	1			
Q Cycle Activity	:			
Q1	Q2	Q3	}	Q4
Q I				

Example:	C	OMF	REG,	Ο,	0
Before Instru	ıction				
REG	=	13h			
After Instruc	tion				
REG	=	13h			
١٨/		ECh.			

CPF	SEQ	Compare f	with W, Skip	if f = W		
Synta	ax:	CPFSEQ	f {,a}			
Oper	ands:	$0 \le f \le 255$				
		a ∈ [0,1]				
Oper	ation:	(f) - (W),				
		skip if (f) = (W) (unsigned comparison)				
Statu	s Affected:	None	,			
	oding:	0110	001a ffi	f ffff		
	cription:		the contents of			
2000	mpuon.		o the contents			
			an unsigned s			
			en the fetched			
			iliu a NOP is ex			
		instruction.		,		
			he Access Bar			
		If 'a' is '1', t GPR bank	he BSR is use	d to select the		
			nd the extende	ed instruction		
		set is enabl	ed, this instruc	ction operates		
			Literal Offset A			
			ever f ≤ 95 (5l . 2.3 "Byte-Or i			
			ed Instruction			
		Literal Offs	set Mode" for	details.		
Word	ds:	1				
Cycle	es:	1(2)				
			ycles if skip an			
0.0		Бу	a 2-word instru	iction.		
QC	ycle Activity: Q1	Q2	Q3	Q4		
	Decode	Read	Process	No No		
	200000	register 'f'	Data	operation		
If sk	ip:					
	Q1	Q2	Q3	Q4		
	No operation	No operation	No operation	No operation		
lf sk	ip and follower	•		operation		
	Q1	Q2	Q3	Q4		
	No	No	No	No		
	operation	operation	operation	operation		
	No	No	No	No		
	operation	operation	operation	operation		
Exan	nple:	HERE	CPFSEQ REG	, 0		
		NEQUAL	:			
	Doforo Instruc	EQUAL	:			
	Before Instruct PC Addre		RE			
	W	= ?				
	REG	= ?				

After Instruction
If REG
PC
If REG
PC

W; Address (EQUAL) W; Address (NEQUAL)

Compare f with W, Skip if f < W

CPFSLT f {,a}

 $0 \le f \le 255$ $a \in [0,1]$

CPFSLT

Syntax:

Operands:

	Compare f	with W, Skip	11 1 / W		
Syntax:	CPFSGT	f {,a}			
Operands:	$0 \leq f \leq 255$				
	a ∈ [0,1]				
Operation:	(f) - (W),				
		skip if (f) > (W) (unsigned comparison)			
Status Affected:	None	ompanson)			
_		010 55	55 5555		
Encoding: Description:	0110	010a ff	ff ffff f data memory		
	performing an unsigned subtraction. If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.				
	1				
Words:					
Words: Cycles:	1(2)	alaa Malda	d fallace d		
	Note: 3 cy	cles if skip an			
Cycles:	Note: 3 cy	cles if skip an 2-word instru			
Cycles: Q Cycle Activity:	Note: 3 cy by a	•	ction.		
Cycles:	Note: 3 cy	2-word instru			
Cycles: Q Cycle Activity: Q1	Note: 3 cy by a	2-word instru	ction. Q4		
Cycles: Q Cycle Activity: Q1	Note: 3 cy by a Q2 Read	2-word instru Q3 Process	Q4 No		
Cycles: Q Cycle Activity: Q1 Decode If skip: Q1	Note: 3 cy by a Q2 Read register 'f'	Q3 Process Data Q3	Q4 No operation Q4		
Cycles: Q Cycle Activity: Q1 Decode If skip:	Note: 3 cy by a Q2 Read register 'f'	Q3 Process Data	Q4 No operation		

Q4

No

operation

No

operation

Q3

No

operation

operation

Address (HERE) ?

Address (GREATER) Address (NGREATER)

CPFSGT REG, 0

Oper	ation:	(f) – (W), skip if (f) < (W) (unsigned comparison)			
Statu	s Affected:	None			
Enco	ding:	0110	000a fff	ff ffff	
Description: Compares the contents of data mend location 'f' to the contents of W by performing an unsigned subtraction. If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected if 'a' is '1', the BSR is used to select the GPR bank (default).				of W by ubtraction. ss than the stched a NOP is this a	
Word	ls:	1			
Cycles: 1(2) Note: 3 cycles if skip and followed by a 2-word instruction.					
Q C	ycle Activity:				
	Q1	Q2	Q3	Q4	
	Decode	Read register 'f'	Process Data	No operation	
lf sk	ip:		l .		
	Q1	Q2	Q3	Q4	
	No	No	No	No	
	operation	operation	operation	operation	
If sk	ip and followed	d by 2-word in	struction:		
1	Q1	Q2	Q3	Q4	
	No	No	No	No	
	operation	operation	operation	operation	
	No	No	No	No	
ļ	operation	operation	operation	operation	
Exam	nple:	NLESS	CPFSLT REG, :	1	
	Before Instruc	tion			
	PC W		dress (HERE))	

Address (LESS)

Address (NLESS)

After Instruction

If REG PC

If REG PC

≥ **=**

Q1

No

operation

No

operation

Before Instruction

PC W

After Instruction

If REG PC If REG PC

Example:

Q2

No

operation

No

operation

NGREATER

GREATER

HERE

DAW	Decimal Adjust W Register			
Syntax:	DAW			
Operands:	None			
Operation:	If [W<3:0> > 9] or [DC = 1] then, (W<3:0>) + 6 \rightarrow W<3:0>; else, (W<3:0>) \rightarrow W<3:0>			
	If [W<7:4> + DC > 9] or [C = 1] then, (W<7:4>) + 6 + DC \rightarrow W<7:4>; else, (W<7:4>) + DC \rightarrow W<7:4>			
Status Affected: C				
Encoding:	0000	0000	0000	0111
Description:	DAW adjusts resulting fro variables (e and produce result.	m the ear ach in pac	lier addition	on of two format)
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3		Q4
Decode	Read	Proces		Write

Example 1:	DAW		
Before Instr	uction		
W	=	A5h	
С	=	0	
DC	=	0	
After Instruc	ction		
W	=	05h	
С	=	1	
DC	=	0	
Example 2:			
Before Instr	uction		
W	=	CEh	
С	=	0	
DC	=	0	
After Instruc	ction		
W	=	34h	
С	=	1	
C DC	=	1	

DECF	Decremen	t f			
Syntax:	DECF f{,	d {,a}}			
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$				
Operation:	$(f) - 1 \rightarrow d$	est			
Status Affected:	C, DC, N, 0	OV, Z			
Encoding:	0000	01da	ffff	ffff	
Description:	result is storesult is storesult is storesult is stored (default). If 'a' is '0', if 'a' is '0' a set is enabin Indexed mode when Section 15 Bit-Oriento Literal Offi	Decrement register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'			
Words:	1				
Cycles:	1				
Q Cycle Activity:					
Q Cycle Activity: Q1	Q2	Q3	3	Q4	

DECFSZ	Decremen	t f, Skip if 0		DCF	SNZ	Decremen	t f, Skip if Not	0
Syntax:	DECFSZ	f {,d {,a}}		Synta	ax:	DCFSNZ	f {,d {,a}}	
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$			Oper	ands:	$0 \le f \le 255$ d $\in [0,1]$ a $\in [0,1]$		
Operation:	(f) $-1 \rightarrow de$ skip if result			Oper	ation:	(f) $-1 \rightarrow d$ skip if resu	•	
Status Affected:	None			Statu	s Affected:	None		
Encoding:	0010	11da ff	ff ffff	Enco	ding:	0100	11da ffi	f ffff
Description:	decremente placed in W placed back If the result which is alr and a NOP it a two-cyc If 'a' is '0', t If 'a' is '1', t GPR bank If 'a' is '0' a set is enabl in Indexed mode wher Section 19 Bit-Oriente	the instruction. The Access Base BSR is use (default). Individual the extended, this instruction of $f \le 95$ (5 the extended of the extended	the result is he result is he result is default). It instruction, is discarded stead, making on the selected of the select the ded instruction ction operates addressing of h. See riented and is in Indexed	Desc	The contents of register 'f' are decremented. If 'd' is '0', the result placed in W. If 'd' is '1', the result in placed back in register 'f' (default). If the result is not '0', the next instruction, which is already fetched discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is '0', the Access Bank is select if 'a' is '1', the BSR is used to select GPR bank (default). If 'a' is '0' and the extended instruction open in Indexed Literal Offset Addressin mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Indexed Instructions in Indexed Instruction Instructions in Indexed Instruction Instruct		the result is a result is default). next dy fetched, is executed eycle ak is selected. d to select the ed instruction operates addressing Fh). See iented and s in Indexed	
Words:	1					Literal Off	set Mode" for	details.
Cycles:	1(2)			Word	ls:	1		
	•	cles if skip ar 2-word instri		Cycle	es:		cycles if skip a	
Q Cycle Activity: Q1	Q2	Q3	Q4	QC	ycle Activity:	Бу	a 2-word insti	uction.
Decode	Read	Process	Write to		Q1	Q2	Q3	Q4
	register 'f'	Data	destination		Decode	Read	Process	Write to
If skip:			•	lf sk	in:	register 'f'	Data	destination
Q1	Q2 No	Q3 No	Q4 No	11 51	ιρ. Q1	Q2	Q3	Q4
No operation	operation	operation	operation		No	No	No	No
If skip and follow	<u> </u>		1 - 1		operation	operation	operation	operation
Q1	Q2	Q3	Q4	If sk	ip and followe	d by 2-word in	struction:	
No	No	No	No		Q1	Q2	Q3	Q4
operation	operation	operation	operation		No	No	No	No
No	No	No	No		operation	operation	operation	operation
operation	operation	operation	operation		No operation	No operation	No operation	No operation
Example:	HERE CONTINUE	DECFSZ GOTO	CNT, 1, 1 LOOP	<u>Exan</u>		HERE ZERO	DCFSNZ TEM	1P, 1, 0
Before Instr	uction						:	
PC After Instruc CNT If CNT	tion = CNT - 1 = 0;		7.)		Before Instruc TEMP After Instruction TEMP	= on =	? TEMP – 1,	
If CNT	C = Address $\neq 0;$	S (CONTINUE	≦)		If TEMP PC	=	0; Address (:	ZERO)
		S (HERE + 2	2)		If TEMP PC	≠ =	0; Address (1	

GOTO	Unconditional Branch			
Syntax:	GOTO k			
Operands:	$0 \leq k \leq 1048575$			
Operation:	$k \rightarrow PC < 20:1 >$			
Status Affected:	None			
Encoding: 1st word (k<7:0>) 2nd word(k<19:8>)	1110 1111 k ₇ kkk kkkk ₀ 1111 k ₁₉ kkk kkkk kkkk ₈			
Description:	GOTO allows an unconditional branch			

anywhere within the entire 2-Mbyte memory range. The 20-bit value 'k' is loaded into PC<20:1>. GOTO is always a two-cycle instruction.

Words: 2 Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	No operation	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: GOTO THERE

After Instruction

PC = Address (THERE)

INCF	:	Increment	f			
Synta	ax:	INCF f {,c	d {,a}}			
Oper	ands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$				
Oper	ation:	$(f) + 1 \rightarrow de$	(f) + 1 \rightarrow dest			
Statu	s Affected:	C, DC, N,	C, DC, N, OV, Z			
Enco	ding:	0010 10da ffff ffff				
Desc	ription:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.				
Word	ls:	1				
Cycle	es:	1				
Q C	ycle Activity:					
	Q1	Q2	Q3		Q4	
	Decode	Read register 'f'	Proce Data		Write to destination	1

Example:	II	NCF	CNT,	1,	0
Before Instru CNT Z C DC After Instruct	= = = =	FFh 0 ? ?			
CNT Z C	= = =	00h 1 1			

INCFSZ	Increment	f, Skip if 0		INFS	NZ	Increment	f, Skip if No	ot 0	
Syntax:	INCFSZ f	{,d {,a}}		Synta	ax:	INFSNZ	f {,d {,a}}		
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$			Oper	ands:	$0 \le f \le 255$ d $\in [0,1]$ a $\in [0,1]$			
Operation:	(f) + 1 \rightarrow description (f) skip if results	•		·	ation:	(f) + 1 \rightarrow d skip if resu			
Status Affected:	None				s Affected:	None			
Encoding:	0011	11da ff	ff ffff		ding:	0100		fff	ffff
Description:	incremente placed in W placed back If the result which is alr and a NOP it a two-cyc If 'a' is '0', t If 'a' is '1', t GPR bank If 'a' is '0' a set is enable in Indexed mode wher Section 19 Bit-Oriente	the instruction. The Access Base BSR is use (default). The extend led, this instructional Diffset ℓ never f \leq 95 (5 1.2.3 "Byte-Or	the result is ne result is . (default) to instruction, is discarded stead, making which is selected. It is selected to select the led instruction ction operates Addressing Fh). See riented and is in Indexed	Desc	ription:	incremented placed in V placed back if the result instruction, discarded a instead, mainstruction. If 'a' is '0', If 'a' is '0', GPR bank If 'a' is '0' a set is enable in Indexed mode when Section 18 Bit-Oriented	the Access E the BSR is u	the rether entered the rether the enext entered to execute exe	esult is sult is sult is sult is sult. etched, is sted selected. select the estruction operates essing See ed and Indexed
Words:	1			Word	ls:	1			
Cycles:		cles if skip an 2-word instru		Cycle	es:		cycles if skip / a 2-word in		
Q Cycle Activity:				QC	ycle Activity:				
Q1	Q2	Q3	Q4	•	Q1	Q2	Q3		Q4
Decode	Read register 'f'	Process Data	Write to destination		Decode	Read register 'f'	Process Data		Vrite to stination
If skip:	, ,	JI.		lf sk	ip:	1 3			
Q1	Q2	Q3	Q4	_	Q1	Q2	Q3		Q4
No	No	No	No		No	No	No		No
operation	operation	operation	operation		operation	operation	operation	op	peration
If skip and followe			04	lf sk	•	d by 2-word ir			0.4
Q1 No	Q2 No	Q3 No	Q4 No	1	Q1	Q2	Q3		Q4
operation	operation	operation	operation		No operation	No operation	No operation	or	No peration
No	No	No	No		No	No	No		No
operation	operation	operation	operation		operation	operation	operation	op	peration
Example:	NZERO	INCFSZ CI :	NT, 1, 0	<u>Exan</u>	nple:	HERE ZERO NZERO	INFSNZ R	EG, 1	., 0

Before Instruction

After Instruction

REG If REG PC If REG PC Address (HERE)

Address (NZERO)

0; Address (ZERO)

REG + 1

PC

Before Instruction PC =

After Instruction

CNT If CNT PC If CNT PC Address (HERE)

0; Address (NZERO)

CNT + 1 0; Address (ZERO)

IORLW	Inclusive OR Literal with W
IORLW	iliciusive OK Literal With W

Status Affected: N, Z

Encoding: 0000 1001 kkkk kkkk

Description: The contents of W are ORed with the

8-bit literal 'k'. The result is placed in W.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4	
Decode	Read	Process	Write to W	
	literal 'k'	Data		

Example: IORLW 35h

Before Instruction

W = 9Ah

After Instruction

W = BFh

Syntax: IORWF $f \{d, d, a\}$ Operands: $0 \le f \le 255$

 $d\in [0,1] \\ a\in [0,1]$

Operation: (W) .OR. (f) \rightarrow dest

Status Affected: N, Z

Encoding: 0001 00da ffff ffff

Description: Inclusive OR W with register 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'

(default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: IORWF RESULT, 0, 1

Before Instruction

RESULT = 13hW = 91h

After Instruction

RESULT = 13h W = 93h **LFSR** Load FSR

Syntax: LFSR f, k Operands:

 $0 \le f \le 2$ $0 \le k \le 4095$

Operation: $k \rightarrow FSRf$

Status Affected: None

 $k_{11}kkk$ Encoding: 1110 1110 00ff 1111 0000 k₇kkk kkkk

Description: The 12-bit literal 'k' is loaded into the

File Select Register pointed to by 'f'.

2 Words: Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write
	'k' MSB	Data	literal 'k' MSB
			to FSRfH
Decode	Read literal	Process	Write literal 'k'
	'k' LSB	Data	to FSRfL

Example: LFSR 2, 3ABh

After Instruction

FSR2H FSR2L 03h ABh

MOVF	Move f
Syntax:	MOVF f {,d {,a}}
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$
Operation:	$f \to dest$
Status Affected:	N, Z
Encoding:	0101 00da ffff ffff
Description:	The contents of register 'f' are moved to

a destination dependent upon the status of 'd'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). Location 'f' can be anywhere in the

256-byte bank.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

If 'a' is '0' and the extended instruction

GPR bank (default).

set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and **Bit-Oriented Instructions in Indexed**

Literal Offset Mode" for details.

Words: Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write W
	register 'f'	Data	

Example: MOVF REG, 0, 0

Before Instruction

REG W 22h FFh

After Instruction

REG 22h W 22h

MOVFF	Move f to f		
Syntax:	MOVFF f _s ,f _d		
Operands:	$0 \le f_s \le 4095$ $0 \le f_d \le 4095$		
Operation:	$(f_s) \rightarrow f_d$		
Status Affected:	None		
Encoding: 1st word (source) 2nd word (destin.)	1100 ffff ffff ffff _s 1111 ffff ffff ffff _d		
Description:	The contents of source register 'f _s ' are		

The contents of source register ' f_s ' are moved to destination register ' f_d '. Location of source ' f_s ' can be anywhere in the 4096-byte data space (000h to FFFh) and location of destination ' f_d ' can also be anywhere from 000h to FFFh.

Either source or destination can be W (a useful special situation).

MOVFF is particularly useful for

transferring a data memory location to a peripheral register (such as the transmit

buffer or an I/O port).

The ${\tt MOVFF}$ instruction cannot use the PCL, TOSU, TOSH or TOSL as the

destination register.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f' (src)	Process Data	No operation
Decode	No operation No dummy read	No operation	Write register 'f' (dest)

Example: MOVFF REG1, REG2

Before Instruction

 $\begin{array}{lll} \mathsf{REG1} & = & 33\mathsf{h} \\ \mathsf{REG2} & = & 11\mathsf{h} \end{array}$

After Instruction

 $\begin{array}{ccc} \mathsf{REG1} & = & 33\mathsf{h} \\ \mathsf{REG2} & = & 33\mathsf{h} \end{array}$

MOV	LB	Move Literal to Low Nibble in BSR				
Synta	ax:	MOVLW k				
Oper	ands:	$0 \le k \le 255$	5			
Oper	ation:	$k \to BSR$				
Statu	s Affected:	None				
Enco	ding:	0000	0000 0001 kkkk kkkk			
Description:		The 8-bit li Bank Sele of BSR<7: regardless	ct Registe 4> always	er (BSR) s remair). The value	
Word	ls:	1				
Cycle	es:	1				
Q Cycle Activity:						
	Q1	Q2	Q3	3	Q4	
	Decode	Read	Proce		Vrite literal	
		literal 'k'	Data	a	'k' to BSR	

Example: MOVLB 5

Before Instruction

BSR Register = 02h

After Instruction

BSR Register = 05h

Description: The 8-bit literal 'k' is loaded into W.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to W
	literal 'k'	Data	

Example: MOVLW 5Ah

After Instruction

W = 5Ah

MOVWF	Move W to f		
Syntax:	MOVWF f {,a}		
Operands:	$0 \le f \le 255$ a $\in [0,1]$		
Operation:	$(W) \rightarrow f$		
Status Affected:	None		
Encoding:	0110 111a ffff f	fff	
Description:	Move data from W to register 'f'. Location 'f' can be anywhere in the		

256-byte bank.

If 'a' is '0', the Access Bank is selected.

If 'a' is '1', the BSR is used to select the

GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed

Literal Offset Mode" for details.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: MOVWF REG, 0

Before Instruction

W = 4Fh REG = FFh

After Instruction

W = 4Fh REG = 4Fh

MULLW	Multiply Literal with W			
Syntax:	MULLW	k		
Operands:	$0 \le k \le 25$	5		
Operation:	(W) $x k \rightarrow$	PRODH:	PRODL	
Status Affected:	None			
Encoding:	0000	1101	kkkk	kkkk
Description:	An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged. None of the Status flags are affected. Note that neither Overflow nor Carry is possible in this operation. A zero result is possible but not detected.			

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	literal 'k'	Data	registers
			PRODH:
			PRODL

Example: MULLW 0C4h

Before Instruction

E2h ? ? W PRODH **PRODL** After Instruction

> E2h PRODH ADh PRODL 08h

MULWF	Multiply W with f			
Syntax:	MULWF	f {,a}		
Operands:	$0 \le f \le 255$ a $\in [0,1]$			
Operation:	(W) $x (f) \rightarrow PRODH:PRODL$			
Status Affected:	None			
Encoding:	0000	001a	ffff	ffff
Description:	An unsigned multiplication is carried			

out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged.

None of the Status flags are affected. Note that neither Overflow nor Carry is possible in this operation. A zero result is possible but not detected. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 19.2.3** "Byte-Oriented and Bit-Oriented

Instructions in Indexed Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	registers
			PRODH:
			PRODL

Example: MULWF REG, 1 Before Instruction C4h B5h PRODH PRODL After Instruction C4h REG B5h PRODH

PRODL

=

8Ah

94h

NEGF Negate f NEGF f {,a} Syntax: Operands: $0 \leq f \leq 255$ $a \in [0,1]$ $(\overline{f}) + 1 \rightarrow f$ Operation: N, OV, C, DC, Z Status Affected: Encoding: 0110 110a ffff ffff Description: Location 'f' is negated using two's complement. The result is placed in the

data memory location 'f'. If 'a' is '0', the Access Bank is selected.

If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and **Bit-Oriented Instructions in Indexed** Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: NEGF REG, 1

Before Instruction

REG 0011 1010 [3Ah]

After Instruction

REG 1100 0110 [C6h]

NOP		No Opera	tion			
Synta	ax:	NOP				
Oper	ands:	None				
Oper	ation:	No operation				
Statu	s Affected:	d: None				
Enco	ding:	0000	0000	000	0 (0000
		1111	XXXX	XXX	XX	XXXX
Desc	ription:	No operati	on.			
Word	ls:	1				
Cycle	es:	1				
QC	ycle Activity:					
	Q1	Q2	Q:	3		Q4
	Decode	No	No			No
		operation	opera	tion	op	eration

Example:

None.

POP		Pop Top of Return Stack				
Synta	ax:	POP	POP			
Oper	ands:	None	None			
Oper	ation:	$(TOS) \rightarrow b$	it bucket			
Statu	s Affected:	None				
Enco	ding:	0000 0000 0000 0110			0110	
Desc	ription:	The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack. This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.				
Word	ls:	1				
Cycle	es:	1				
QC	ycle Activity:					
	Q1	Q2	Q3	3		Q4
	Decode	No	Pop T			No
		operation	valu	е	ор	eration

Example: POP GOTO

Before Instruction

TOS = 0031A2h Stack (1 level down) = 014332h

NEW

After Instruction

TOS = 014332h PC = NEW

PUS	Н	Push Top of Return Stack				
Synta	ax:	PUSH				
Oper	ands:	None	None			
Oper	ation:	$(PC + 2) \rightarrow TOS$				
Statu	s Affected:	None				
Enco	ding:	0000	0000	000	0	0101
Description: The PC + 2 is pushed onto the top the return stack. The previous TOS value is pushed down on the stack. This instruction allows implementing software stack by modifying TOS at then pushing it onto the return stack.				TOS stack. enting a OS and		
Word	ls:	1				
Cycle	es:	1				
QC	ycle Activity:					
	Q1	Q2	Q3	}		Q4
	Decode	Push PC + 2	No			No
		onto return	onerat	ion I	Λn	eration

onto return operation operation

Example:

PUSH

Onto return operation operation

Before Instruction

TOS = 345Ah PC = 0124h

After Instruction

PC = 0126h TOS = 0126h Stack (1 level down) = 345Ah **RCALL Relative Call** Syntax: RCALL n Operands: $\text{-}1024 \leq n \leq 1023$ Operation: (PC) + 2 \rightarrow TOS, $(PC) + 2 + 2n \rightarrow PC$ Status Affected: None Encoding: 1101 1nnn nnnn nnnn Description: Subroutine call with a jump up to 1K

from the current location. First, return address (PC + 2) is pushed onto the stack. Then, add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a

two-cycle instruction.

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process Data	Write to PC
	Push PC to stack		
No operation	No operation	No operation	No operation

Example: HERE RCALL Jump

Before Instruction

PC = Address (HERE)

After Instruction

PC = Address (Jump) TOS = Address (HERE + 2)

RESET	Reset			
Syntax:	RESET			
Operands:	None			
Operation:	Reset all registers and flags that are affected by a MCLR Reset.			
Status Affected:	All			
Encoding:	0000	0000	1111	1111
Description:	This instruction provides a way to execute a MCLR Reset in software.			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3	3	Q4

Example: RESET

After Instruction

Decode

Registers = Reset Value Flags* = Reset Value

Start

Reset

No

operation

No

operation

RETFIE	Return from Interrupt			
Syntax:	RETFIE +	(s)		
Operands:	$s \in \left[0,1\right]$			
Operation:	$(TOS) \rightarrow PC$, 1 → GIE/GIEH or PEIE/GIEL; if s = 1, $(WS) \rightarrow W$, $(STATUSS) \rightarrow STATUS$, $(BSRS) \rightarrow BSR$, PCLATU, PCLATH are unchanged			
Status Affected:	GIE/GIEH	, PEIE/GI	EL.	
Encoding:	0000	0000	0001	000s
Description:	Return from interrupt. Stack is popped and Top-of-Stack (TOS) is loaded into the PC. Interrupts are enabled by setting either the high or low-priority global interrupt enable bit. If 's' = 1, the			

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	No	Pop PC from
	operation	operation	stack
			Set GIEH or
			GIEL
No	No	No	No
operation	operation	operation	operation

contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers, W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default).

Example: RETFIE 1

After Interrupt

RETLW	Return Literal to W			
Syntax:	RETLW I	(
Operands:	$0 \leq k \leq 255$			
Operation:	$k \rightarrow W$, (TOS) \rightarrow PC, PCLATU, PCLATH are unchanged			
Status Affected:	None			
Encoding:	0000	1100	kkkk	kkkk
Description:	W is loaded with the 8-bit literal 'k'. The program counter is loaded from the top			

unchanged.
Words: 1
Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Pop PC from
	literal 'k'	Data	stack, Write
			to W
No	No	No	No
operation	operation	operation	operation

of the stack (the return address). The high address latch (PCLATH) remains

Example:

```
CALL TABLE ; W contains table
               ; offset value
               ; W now has
                ; table value
TABLE
   ADDWF PCL ; W = offset
   RETLW k0
               ; Begin table
   RETLW k1
   RETLW kn
               ; End of table
   Before Instruction
       W
    After Instruction
       W
                   value of kn
```

RETURN	Return from Subroutine			
Syntax:	RETURN	{s}		
Operands:	$s \in \left[0,1\right]$			
Operation:	(TOS) → PC; if s = 1, (WS) → W, (STATUSS) → STATUS, (BSRS) → BSR, PCLATU, PCLATH are unchanged			
Status Affected:	None			
Encoding:	0000	0000	0001	001s
Description:	Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's'= 1, the contents of the shadow			

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	Pop PC
	operation	Data	from stack
No	No	No	No
operation	operation	operation	operation

occurs (default).

registers WS, STATUSS and BSRS are loaded into their corresponding registers, W, STATUS and BSR. If 's' = 0, no update of these registers

Example: RETURN

After Instruction: PC = TOS

RLCF	Rotate Lef	t f through	Carry		
Syntax:	RLCF f	{,d {,a}}			
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$	$d \in [0,1]$			
Operation:	$(f<7>) \rightarrow C$	$(f) \rightarrow dest,$ $(f<7>) \rightarrow C,$ $(C) \rightarrow dest<0>$			
Status Affected:	C, N, Z				
Encoding:	0011	01da f	fff ffff		
Description:	one bit to the flag. If 'd' is 'W. If 'd' is 'W. If 'd' is 'in register' If 'a' is '0', selected. If select the 'G' is 'e' a set is enable operates in Addressing f ≤ 95 (5Fh "Byte-Orie"	the left through the left through the result of (default). The Access Is a like the Access Is a like the Access Is a like the external led, this instance where the led and Bins in Indexed and Bins in Indexed in Indexed and Bins in Indexed in	alt is placed in a stored back Bank is BSR is used to lefault). Indeed instruction ruction ruction eral Offset never on 19.2.3 t-Oriented d Literal Offset		
Words:	1				
Cycles:	1				
Q Cycle Activity:					
Q1	Q2	Q3	Q4		
Decode	Read register 'f'	Process Data	Write to destination		
Example:	RI.CF	REG. O	. 0		

Example: RLCF REG, 0, 0

Before Instruction

REG = 1110 0110

C = 0

After Instruction

REG = 1110 0110 W = 1100 1100 C = 1

RLNCF	Rotate Le	ft f (No Carry)	RRCF	Rotate Rig	ht f through	Carry
Syntax:	RLNCF	f {,d {,a}}		Syntax:	RRCF f{	,d {,a}}	
Operands:	$0 \le f \le 255$ d $\in [0,1]$ a $\in [0,1]$;		Operands:	$0 \le f \le 255$ d $\in [0,1]$ a $\in [0,1]$		
Operation:	$ (f < n >) \rightarrow 0 $ $ (f < 7 >) \rightarrow 0 $	lest <n +="" 1="">, lest<0></n>		Operation:	$(f<0>) \rightarrow C$	•	
Status Affected:	N, Z			Otatua Affaatada	$(C) \rightarrow dest$	I<1>	
Encoding:	0100	01da ff	ff ffff	Status Affected:	C, N, Z	1	<u> </u>
Description:		nts of register		Encoding:	0011	00da ff	fff ffff
	is placed in stored back If 'a' is '0', If 'a' is '1', GPR bank If 'a' is '0' a set is enabl in Indexed mode whe Section 19 Bit-Orient	n W. If 'd' is '1 the Access Ba the BSR is use (default). and the extend bled, this instru Literal Offset never f ≤ 95 (\$ 9.2.3 "Byte-O	default). Ink is selected. I	Description:	one bit to the flag. If 'd' is '1', register 'f' If 'a' is '0', If 'a' is '1', GPR bank If 'a' is '0' at set is enable in Indexed mode whe Section 19 Bit-Orient Literal Off	the result is pl (default). the Access Ba the BSR is use (default). and the extend pled, this instru. Literal Offset never f ≤ 95 (§ 3.2.3 "Byte-O ed Instruction set Mode" for	gh the Carry is placed in W. laced back in ank is selected. ed to select the ded instruction action operates Addressing 5Fh). See riented and ns in Indexed r details.
Words:	1				C	→ registe	er f
Cycles:	1			Words:	1		
Q Cycle Activity:					•		
Q1	Q2	Q3	Q4	Cycles:	1		
Decode	Read	Process	Write to	Q Cycle Activity			
	register 'f'	Data	destination	Q1	Q2	Q3	Q4
Example:	RLNCF	REG, 1,	0	Decode	Read register 'f'	Process Data	Write to destination
Before Instru	ction						
REG	= 1010 1	1011		Example:	RRCF	REG, 0,	0
After Instruct				Before Instr	ruction		
REG	= 0101 (0111		REG C After Instruc REG	= 1110 = 0 ction = 1110		
				W	= 0111		

RRNCF Rotate Right f (No Carry) Syntax: RRNCF f {, d {,a}} Operands: $0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$ Operation: $(f < n >) \rightarrow dest < n - 1 >$ (f<0>) → dest<7> Status Affected: N. Z Encoding: 0100 00da ffff ffff Description: The contents of register 'f' are rotated

one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See

Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.



Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example 1: RRNCF REG, 1, 0

Before Instruction

REG = 1101 0111

After Instruction

REG = 1110 1011

Example 2: RRNCF REG, 0, 0

Before Instruction

W = ? REG = 1101 0111

After Instruction

W = 1110 1011 REG = 1101 0111

SETF	Set f			
Syntax:	SETF f{	,a}		
Operands:	$0 \le f \le 255$ $a \in [0,1]$;		
Operation:	$FFh \to f$			
Status Affected:	None			
Encoding:	0110	100a	ffff	ffff
5			.c. 1	

Description: The contents of the specified register

are set to FFh.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: SETF REG, 1

Before Instruction

REG = 5Ah After Instruction REG = FFh

SLEEP	Enter Sle	ep Mode			
Syntax:	SLEEP				
Operands:	None				
Operation:					
Status Affected:	$\overline{TO}, \overline{PD}$				
Encoding:	0000	0000	0000	0011	
Description:	The Power-Down status bit (PD) is cleared. The Time-out status bit (TO)				

is set. Watchdog Timer and its postscaler are cleared.

The processor is put into Sleep mode

with the oscillator stopped.

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	Go to
	operation	Data	Sleep

Example: SLEEP Before Instruction <u>TO</u> = PD = After Instruction TO =

† If WDT causes wake-up, this bit is cleared.

SUB	FWB	Sı	ubtract 1	from W	with	Bor	row
Synta	ax:	S	UBFWB	f {,d {,a	a}}		
Oper	ands:	d	≤ f ≤ 255 ∈ [0,1] ∈ [0,1]	i			
Oper	ation:	(V	/) – (f) –	$(\overline{C}) \rightarrow de$	est		
Statu	s Affected:	N,	OV, C,	DC, Z			
Enco	ding:		0101	01da	fff	f	ffff
Desc	ription:	(bo mo in req If ' se to If ' se op Ac f ≤ "B	Subtract register 'f' and Carry flag (borrow) from W (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.				
Word	ls:	1	000 101	dotano.			
Cycle	es:	1					
•	ycle Activity:						
	Q1	(Q2	Q3			Q4
	Decode		ead ster 'f'	Proces Data			/rite to stination
Exan	nple 1:	SU	JBFWB	REG,	1, 0		
	Before Instruction REG W C After Instruction REG W C Z	= = on = = = =	3 2 1 FF 2 0				
Evan	N aplo 2:	=	, -	sult is ne	J	9	
⊏xan	<u>nple 2:</u> Before Instruc		JBFWB	REG,	U, U		
	REG W C After Instruction	= = =	2 5 1				
	REG W C	= = =	2 3 1				

; result is positive

; result is zero

REG, 1, 0

SUBFWB

1 2 0

0 2 1

Example 3:

Before Instruction REG

W

After Instruction

REG =

W =

C =

Z =

N =

Cycles: 1 result is stored in result is stored in result is stored by the company of the company	ffff ffff register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
Status Affected: N, OV, C, DC, Z Encoding: $0000 1000 kkkk kkkk$ Description W is subtracted from the 8-bit literal 'k'. The result is placed in W. Words: 1 Cycles: 1 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read Process Write to W literal 'k' Data	register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
Status Affected: N, OV, C, DC, Z Encoding: $0000 1000 kkkk kkkk$ Description W is subtracted from the 8-bit literal 'k'. The result is placed in W. Words: 1 Cycles: 1 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read Process Write to W literal 'k' Data	register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
Encoding: Description W is subtracted from the 8-bit literal 'k'. The result is placed in W. Words: 1 Cycles: Q1 Q2 Q3 Q4 Decode Read Iteral 'k' Data Status Affected: N, OV, C, DC, Z Description: Subtract W from a complement meth result is stored by (default). If 'a' is '0', the Access elected. If 'a' is 'to select the GPR	register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
Description W is subtracted from the 8-bit literal 'k'. The result is placed in W. Words: 1 Cycles: Q1 Q2 Q3 Q4 Decode Read Process Write to W literal 'k' Data Status Affected: N, OV, C, DC, Z 0101 11da Complement meth result is stored in result is stored in result is stored by (default). If 'a' is '0', the Accesselect the GPR	register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
Words: 1 Cycles: 1 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read Process Uniteral 'k' Data Data	register 'f' (2's nod). If 'd' is '0', the W. If 'd' is '1', the
Cycles: 1 complement metrices result is stored in result is stored in result is stored by complement metrices. The complement metrices result is stored in result is stored by complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices are complement metrices. The complement metrices are complement metrices are complement metrices are complement metrices. The complement metrices are c	nod). If 'd' is '0', the W. If 'd' is '1', the
Cycles: 1 result is stored in result is stored in result is stored by Cycle Activity: Q1 Q2 Q3 Q4 (default). Decode Read Process Write to W selected. If 'a' is '0', the Act selected. If 'a' is '0 is to select the GPR	W. If 'd' is '1', the
Q1 Q2 Q3 Q4 Decode Read Process Write to W selected. If 'a' is '0', the Acc selected. If 'a' is '0' to select the GPR	ack in register 'f'
Decode Read Process Write to W selected. If 'a' is '0', the Act selected. If 'a' is '0', the Act selected of the Act selected	
Decode Read Process Write to W selected. If 'a' is ' literal 'k' Data to select the GPR	acca Donk io
IO Select the GPM	1', the BSR is used
Example 1: SIDIM 02b If a is 0 and the	
set is enabled, thi	
Before Instruction operates in Index W = 01h	
C = ? Addressing mode	
After Instruction $f \le 95$ (5Fh). See $W = 01h$ "Byte-Oriented a	
C = 1 ; result is positive Instructions in In	dexed Literal Offset
Z = 0 $N = 0$ Mode" for details.	
Example 2: SUBLW 02h Words: 1	
Before Instruction Cycles: 1	
W = 02h Q Cycle Activity:	
After Instruction Q1 Q2 C	Q3 Q4
W = 00h C = 1 ; result is zero Decode Read Proc	
Z = 1	L.
N = 0 <u>Example 1:</u> SUBWF REG, Example 3: SUBLW 02h Before Instruction	1, 0
REG = 3	
W = 03h $C = ?$	
C = ? After Instruction After Instruction REG = 1	
W = FFh : (2's complement) $W = 2$	
C = 0 ; result is negative C = 1 ; result is Z = 0	positive
$N = 1 \qquad \qquad \overline{N} = 0$	
Example 2: SUBWF REG,	0, 0
Before Instruction REG = 2 W = 2	
W = 2 C = ?	
After Instruction	
REG = 2 W = 0	
C = 1 ; result is	zero
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	
Example 3: SUBWF REG,	1, 0
Before Instruction	
REG = 1 W = 2	
C = ? After Instruction	
REG = FFh ;(2's com	plement)
W = 2 $C = 0$; result is	negative
Z = 0	
N = 1	

SUBWFB	Subtract W	I from f with B	orrow	SWAPF
Syntax:	SUBWFB	f {,d {,a}}		Syntax:
Operands:	$0 \le f \le 255$			Operands:
	d ∈ [0,1] a ∈ [0,1]			
Operation:	(f) - (W) - (W)	$\overline{(C)} \rightarrow \text{dest}$		Onenation
Status Affected:	N, OV, C, D			Operation:
Encoding:	0101	10da fff	f ffff	Status Affect
Description:	Subtract W	and the Carry	flag (borrow)	Encoding:
	_	er 'f' (2's comple 'd' is '0', the re		Description:
	,	s '1', the result is		·
	in register "			
		he Access Ban he BSR is used		
	GPR bank		10 00.000 11.0	
		nd the extende		
		led, this instruct Literal Offset A		
	mode when	never $f \le 95$ (5F)	h). See	
		.2.3 "Byte-Oried Instructions		
		set Mode" for o		
Words:	1			NA/ a mala a
Cycles:	1			Words:
Q Cycle Activity:			_	Cycles:
Q1 Decode	Q2 Read	Q3 Process	Q4 Write to	Q Cycle Act Q
Decode	register 'f'	Data	destination	Deco
Example 1:	SUBWFB	REG, 1, 0		
Before Instruc REG		(0001 100	.1.\	
W	= 0Dh	(0001 100 (0000 110		Example:
C After Instruction	= 1			Before RE
REG	= 0Ch	(0000 101		After In:
W C	= 0Dh = 1	(0000 110	1)	RE
Z N	= 0 = 0	; result is po	sitive	
Example 2:	SUBWFB	REG, 0, 0		
Before Instruc				
REG W	= 1Bh = 1Ah	(0001 101 (0001 101		
С				
	= 0			
After Instruction	on = 1Bh	(0001 101	1)	
After Instruction	on	(0001 101	1)	
After Instruction REG W C Z	on = 1Bh = 00h = 1 = 1	(0001 101 ; result is ze		
After Instruction REG W C Z N	on = 1Bh = 00h = 1 = 1 = 0	; result is ze		
After Instruction REG W C Z N Example 3:	on = 1Bh = 00h = 1 = 1 = 0 SUBWFB	; result is ze	ro	
After Instruction REG W C Z N Example 3: Before Instruc	on = 1Bh = 00h = 1 = 1 = 0 SUBWFB	; result is ze	ro 1)	
After Instruction REG W C Z N N Example 3: Before Instruction REG W C	on = 1Bh = 00h = 1 = 1 = 0 SUBWFB etion = 03h = 0Eh = 1	; result is ze	ro 1)	
After Instruction REG W C Z N N Example 3: Before Instruction REG W	on = 1Bh = 00h = 1 = 1 = 0 SUBWFB etion = 03h = 0Eh = 1	; result is ze	1) 1)	
After Instruction REG W C Z N Example 3: Before Instruction REG W C After Instruction	on	; result is ze REG, 1, 0 (0000 001 (0000 110 (1111 010 ; [2's comp]	1) 1) 1)	
After Instruction REG W C Z N N Example 3: Before Instruction REG W C C After Instruction	DON	; result is ze REG, 1, 0 (0000 001 (0000 110 (1111 010	1) 1) 1)	

SWAPF	Swap f			
Syntax:	•	{,d {,a}}		
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	(, , (, ,))		
Operation:	$(f<3:0>) \rightarrow dest<7:4>,$ $(f<7:4>) \rightarrow dest<3:0>$			
Status Affected:	None			
Encoding:	0011	10da	ffff	ffff
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3	1	Q4
Decode	Read register 'f'	Proce Data		Vrite to stination
Evample:	SMADE I	DEC 1	0	

Example: SWAPF REG, 1, 0

Before Instruction

REG = 53h

After Instruction

REG = 35h

TBLRD	Table Read				
Syntax:	TBLRD (*; *+; *-; +*)				
Operands:	None				
Operation:	if TBLRD *, (Prog Mem (TBLPTR)) → TABLAT, TBLPTR – No Change; if TBLRD *+, (Prog Mem (TBLPTR)) → TABLAT, (TBLPTR) + 1 → TBLPTR; if TBLRD *-, (Prog Mem (TBLPTR)) → TABLAT, (TBLPTR) – 1 → TBLPTR; if TBLRD +*, (TBLPTR) + 1 → TBLPTR, (Prog Mem (TBLPTR)) → TABLAT				
Status Affected:	None				
Encoding:	0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*	
Description:	This instruction is used to read the contents of Program Memory (P.M.). To address the				

TBLRD	Table Read (Continued)		
Example 1:	TBLRD *+	;	
Before Instructi TABLAT TBLPTR MEMORY After Instructior TABLAT TBLPTR	(00A356h)	= = = = =	00/100011
Example 2:	TBLRD +*	;	
Before Instructi TABLAT TBLPTR MEMORY MEMORY After Instruction	(01A357h) (01A358h)	= = =	12h
TABLAT TBLPTR		=	34h 01A358h

program memory, a pointer called Table

Pointer (TBLPTR) is used.

The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range.

TBLPTR<0> = 0: Least Significant Byte of Program Memory Word
TBLPTR<0> = 1: Most Significant Byte of Program Memory Word The TBLRD instruction can modify the value

of TBLPTR as follows:

· no change

· post-increment

post-decrement

pre-increment

Words: Cycles: 2 Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	No	No
	operation	operation	operation
No operation	No operation (Read Program Memory)	No operation	No operation (Write TABLAT)

TBLWT	Table Writ	te			
Syntax:	TBLWT (*	; *+; *-; +*))		
Operands:	None				
Operation:	if TBLWT*, (TABLAT) → Holding Register, TBLPTR – No Change; if TBLWT*+, (TABLAT) → Holding Register, (TBLPTR) + 1 → TBLPTR; if TBLWT*-, (TABLAT) → Holding Register, (TBLPTR) – 1 → TBLPTR; if TBLWT+*, (TBLPTR) + 1 → TBLPTR, (TBLPTR) + 1 → TBLPTR, (TABLAT) → Holding Register				
Status Affected:	None				
Encoding:	0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*	
Description:	This instruction uses the 3 LSBs of TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to Section 6.0 "Flash Program Memory" for additional details on programming Flash memory.) The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range. The LSb of the TBLPTR selects which byte of the program memory location to access. TBLPTR<0> = 0: Least Significant Byte of Program Memory Word TBLPTR<0> = 1: Most Significant Byte of Program Memory Word The TBLWT instruction can modify the value of TBLPTR as follows: • no change • post-increment • post-decrement				
Manda.	• pre-incr	ement			
Words: Cycles:	1				
,	4				
Q Cycle Activity:	Q1	02	Q3	04	
	Decode	Q2 No operation	No operation	Q4 No operation	
	.		.		

Q1	Q2	Q3	Q4
Decode	No	No	No
	operation	operation	operation
No	No	No	No
operation	operation	operation	operation
	(Read		(Write to
	TABLAT)		Holding
			Register)

TBLWT	Table Write (Conti	nued)	
Example 1:	TBLWT *+;			
Before Instru	uction			
	R NG REGISTER	=	55h 00A356h	
(00A3	,	=	FFh	
	tions (table write		,	
TABLA TBLPT HOLDI		=	55h 00A357h	
(00A3		=	55h	
Example 2:	TBLWT +*;			
Before Instru	uction			
TABLA	T	=	34h	
TBLPT	• •	=	01389Ah	
(0138	NG REGISTER 9Ah) NG REGISTER	=	FFh	
(01389	9Bh)	=	FFh	
After Instruc	tion (table write	compl	etion)	
TABLA		=	34h	
TBLPT	R NG REGISTER	=	01389Bh	
(01389		=	FFh	
(01389	9Bh)	=	34h	

TSTFSZ Test f, Skip if 0

Syntax: TSTFSZ $f\{,a\}$ Operands: $0 \le f \le 255$ $a \in [0,1]$

Operation: skip if f = 0

Status Affected: None

Encoding: $0110 \ 011a \ ffff \ ffff$ Description: If 'f' = 0, the next instruction fetched

during the current instruction execution is discarded and a NoP is executed, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default). If 'a' is '0' and the extended instruction

set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed

Literal Offset Mode" for details.

Words: 1 Cycles: 1(2)

Note: 3 cycles if skip and followed

by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4	
Decode	Read	Process	No	
	register 'f'	Data	operation	

If skip:

Q1 Q2		Q3	Q4		
No	No	No	No		
operation	operation	operation	operation		

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No No n operation		No
operation			operation
No	No	No	No
operation	operation operation		operation

Example: HERE TSTFSZ CNT, 1

NZERO : ZERO :

Before Instruction

PC = Address (HERE)

After Instruction

If CNT = 00h,

PC = Address (ZERO)
If CNT ≠ 00h,
PC = Address (NZERO)

XORLW	Exclusive	Exclusive OR Literal with W				
Syntax:	XORLW	k				
Operands:	$0 \le k \le 25$	5				
Operation:	(W) .XOR	(W) .XOR. $k \rightarrow W$				
Status Affected:	N, Z	N, Z				
Encoding:	0000	1010	kkkk	kkkk		
Description:	The conte the 8-bit lift in W.					
Words:	1					
Cycles:	1	1				
Q Cycle Activity:						
Q1	Q2	Q3		Q4		
Decode	Read	Proces	ss W	rite to W		

Example: XORLW 0AFh

literal 'k'

Data

Before Instruction
W =

W = B5h After Instruction

W = 1Ah

XORWF Exclusive OR W with f

Syntax: XORWF $f \{ d \}$

 $\begin{array}{ll} \text{Operands:} & 0 \leq f \leq 255 \\ & d \in [0,1] \end{array}$

 $d \in [0,1]$ $a \in [0,1]$

Operation: (W) .XOR. (f) \rightarrow dest

Status Affected: N, Z

Encoding: 0001 10da ffff ffff

Description: Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored

in W. If 'd' is '1', the result is stored back in the register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the

GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 19.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed

Literal Offset Mode" for details.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: XORWF REG, 1, 0

Before Instruction

REG = AFh W = B5h

After Instruction

REG = 1Ah W = B5h

19.2 Extended Instruction Set

In addition to the standard 75 instructions of the PIC18 instruction set, PIC18F2450/4450 devices also provide an optional extension to the core CPU functionality. The added features include eight additional instructions that augment indirect and indexed addressing operations and the implementation of Indexed Literal Offset Addressing mode for many of the standard PIC18 instructions.

The additional features of the extended instruction set are disabled by default. To enable them, users must set the XINST Configuration bit.

The instructions in the extended set can all be classified as literal operations, which either manipulate the File Select Registers, or use them for Indexed Addressing. Two of the instructions, ${\tt ADDFSR}$ and ${\tt SUBFSR}$, each have an additional special instantiation for using FSR2. These versions (${\tt ADDULNK}$ and ${\tt SUBULNK}$) allow for automatic return after execution.

The extended instructions are specifically implemented to optimize re-entrant program code (that is, code that is recursive or that uses a software stack) written in high-level languages, particularly C. Among other things, they allow users working in high-level languages to perform certain operations on data structures more efficiently. These include:

- Dynamic allocation and deallocation of software stack space when entering and leaving subroutines
- · Function Pointer invocation
- · Software Stack Pointer manipulation
- Manipulation of variables located in a software stack

A summary of the instructions in the extended instruction set is provided in Table 19-3. Detailed descriptions are provided in **Section 19.2.2 "Extended Instruction Set"**. The opcode field descriptions in Table 19-1 (page 214) apply to both the standard and extended PIC18 instruction sets.

Note:

The instruction set extension and the Indexed Literal Offset Addressing mode were designed for optimizing applications written in C; the user may likely never use these instructions directly in assembler. The syntax for these commands is provided as a reference for users who may be reviewing code that has been generated by a compiler.

19.2.1 EXTENDED INSTRUCTION SYNTAX

Most of the extended instructions use indexed arguments, using one of the File Select Registers and some offset to specify a source or destination register. When an argument for an instruction serves as part of Indexed Addressing, it is enclosed in square brackets ("[]"). This is done to indicate that the argument is used as an index or offset. The MPASM™ Assembler will flag an error if it determines that an index or offset value is not bracketed.

When the extended instruction set is enabled, brackets are also used to indicate index arguments in byte-oriented and bit-oriented instructions. This is in addition to other changes in their syntax. For more details, see Section 19.2.3.1 "Extended Instruction Syntax with Standard PIC18 Commands".

Note: In the past, square brackets have been used to denote optional arguments in the PIC18 and earlier instruction sets. In this text and going forward, optional arguments are denoted by braces ("{ }").

TABLE 19-3: EXTENSIONS TO THE PIC18 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word			Status	
		Description	Cycles	MSb			LSb	Affected
ADDFSR	f, k	Add Literal to FSR	1	1110	1000	ffkk	kkkk	None
ADDULNK	k	Add Literal to FSR2 and Return	2	1110	1000	11kk	kkkk	None
CALLW		Call Subroutine using WREG	2	0000	0000	0001	0100	None
MOVSF	z_s , f_d	Move z _s (source) to 1st word	2	1110	1011	0zzz	ZZZZ	None
		f _d (destination) 2nd word		1111	ffff	ffff	ffff	
MOVSS	z_s, z_d	Move z _s (source) to 1st word	2	1110	1011	1zzz	ZZZZ	None
		z _d (destination) 2nd word		1111	XXXX	XZZZ	ZZZZ	
PUSHL	k	Store Literal at FSR2,	1	1110	1010	kkkk	kkkk	None
		Decrement FSR2						
SUBFSR	f, k	Subtract Literal from FSR	1	1110	1001	ffkk	kkkk	None
SUBULNK	k	Subtract Literal from FSR2 and	2	1110	1001	11kk	kkkk	None
		Return						

19.2.2 EXTENDED INSTRUCTION SET

ADDFSR	Add Lite	ral to FSF	₹	
Syntax:	ADDFSR	f, k		
Operands:	$0 \le k \le 63$ $f \in [0, 1,$			
Operation:	$FSR(f) + k \rightarrow FSR(f)$			
Status Affected:	None			
Encoding:	1110	1000	ffkk	kkkk
Description:	The 6-bit literal 'k' is added to the contents of the FSR specified by 'f'.			
Words:	1			

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	literal 'k'	Data	FSR

Example: ADDFSR 2, 23h

Before Instruction

FSR2 = 03FFh

After Instruction

FSR2 = 0422h

ADDULNK	Add Literal to FSR2 and Return			
Syntax:	ADDULN	K k		
Operands:	$0 \le k \le 63$	3		
Operation:	FSR2 + k	$A \rightarrow FSR2$,	
	$(TOS) \rightarrow$	PC		
Status Affected:	None			
Encoding:	1110	1000	11kk	kkkk
Description:	contents executed TOS. The instri execute; the secor This may case of the	be though ne ADDFSI 3 (binary	A RETURN g the PC es two cyc performed ht of as a r instruction	is then with the cles to during special on,
Words:	1			

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	literal 'k'	Data	FSR
No	No	No	No
Operation	Operation	Operation	Operation

Example: ADDULNK 23h

Before Instruction

FSR2 = 03FFh PC = 0100h

After Instruction

FSR2 = 0422hPC = (TOS)

Note: All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction syntax then becomes: {label} instruction argument(s).

CALLW Subroutine Call Using WREG

Syntax: **CALLW**

Operands: None

 $(PC + 2) \rightarrow TOS$, Operation: $(W) \rightarrow PCL$

 $(PCLATH) \rightarrow PCH,$ (PCLATU) → PCU

Status Affected: None

Encoding: 0000

Description First, the return address (PC + 2) is

> pushed onto the return stack. Next, the contents of W are written to PCL; the existing value is discarded. Then the contents of PCLATH and PCLATU are

0001

0100

0000

latched into PCH and PCU, respectively. The second cycle is executed as a NOP instruction while the new next instruction is fetched. Unlike CALL, there is no option to

update W, STATUS or BSR.

Words: 1 2 Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Push PC to	No
	WREG	stack	operation
No	No	No	No
operation	operation	operation	operation

Example: HERE CALLW

Before Instruction

PC address (HERE)

PCLATH = 10h PCLATU W 00h 06h

After Instruction

001006h PC

TOS address (HERE + 2)

PCLATH = 10h PCLATU = 00h06h

MOVSF Move Indexed to f

 $\overline{\text{MOVSF}}$ [z_s], f_d Syntax: $0 \le z_s \le 127$ Operands: $0 \leq f_d \leq 4095$

 $((FSR2) + z_s) \rightarrow f_d$ Operation:

Status Affected: None

Encoding: 1st word (source)

1110 2nd word (destin.) 1111

ffff ffff $ffff_d$ Description: The contents of the source register are

1011

moved to destination register 'f_d'. The actual address of the source register is determined by adding the 7-bit literal offset 'zs' in the first word to the value of FSR2. The address of the destination register is specified by the 12-bit literal 'f_d' in the second word. Both addresses can be anywhere in the 4096-byte data

0zzz

ZZZZs

space (000h to FFFh).

The MOVSF instruction cannot use the PCL, TOSU, TOSH or TOSL as the

destination register.

If the resultant source address points to an indirect addressing register, the

value returned will be 00h.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1 Q2 Q3 Q4 Decode Determine Determine Read source addr source addr source reg Decode Write No No operation operation register 'f' (dest) No dummy read

Example: [05h], REG2 MOVSF

Before Instruction

80h FSR2 = Contents of 85h 33h REG2 11h

After Instruction

FSR2 80h Contents 33h of 85h RFG2 33h

MOVSS Move Indexed to Indexed

Syntax: MOVSS $[z_s], [z_d]$ $0 \le z_s \le 127$ Operands: $0 \le z_d \le 127$

Operation: $((FSR2) + z_s) \rightarrow ((FSR2) + z_d)$

Status Affected: None

Encoding: 1st word (source) 2nd word (dest.)

Description

1110	1011	1zzz	ZZZZs
1111	XXXX	XZZZ	zzzzd

The contents of the source register are moved to the destination register. The addresses of the source and destination registers are determined by adding the 7-bit literal offsets 'z_s' or 'z_d',

respectively, to the value of FSR2. Both registers can be located anywhere in the 4096-byte data memory space

(000h to FFFh).

The MOVSS instruction cannot use the PCL, TOSU, TOSH or TOSL as the

destination register.

If the resultant source address points to an indirect addressing register, the value returned will be 00h. If the resultant destination address points to an indirect addressing register, the instruction will execute as a NOP.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Determine	Determine	Read
	source addr	source addr	source reg
Decode	Determine	Determine	Write
	dest addr	dest addr	to dest reg

Example: MOVSS [05h], [06h]

Before Instruction

FSR2 80h Contents of 85h 33h Contents of 86h 11h After Instruction

FSR2

80h Contents of 85h 33h Contents of 86h 33h

PUSHL	Store Literal at FSR2, Decrement FSR2
-------	---------------------------------------

Syntax: PUSHL k Operands: $0 \le k \le 255$ Operation: $k \rightarrow (FSR2),$

FSR2 - 1→ FSR2

Status Affected: None

Description:

Encoding: 1111 1010 kkkk kkkk

> memory address specified by FSR2. FSR2 is decremented by '1' after the operation. This instruction allows users to push values

The 8-bit literal 'k' is written to the data

onto a software stack.

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process	Write to
		data	destination

Example: PUSHL 08h

Before Instruction

FSR2H:FSR2L 01ECh Memory (01ECh)

After Instruction

FSR2H:FSR2L 01EBh Memory (01ECh) 08h

Subtract Literal from FSR2 and Return

SUBFSR Subtract Literal from FSR
Syntax: SUBFSR f, k

 $\begin{tabular}{lll} Syntax: & SUBFSR f, k \\ Operands: & 0 \le k \le 63 \end{tabular}$

 $f\in \left[\ 0,\,1,\,2\ \right]$

 $\mbox{ Operation: } \mbox{ FSRf}-\mbox{ k} \rightarrow \mbox{ FSRf}$

Status Affected: None

Encoding: 1110 1001 ffkk kkkk

Description: The 6-bit literal 'k' is subtracted from

the contents of the FSR specified by

'f'. Words: 1 Cycles: 1

Q Cycle Activity:

 Q1
 Q2
 Q3
 Q4

 Decode
 Read register 'f'
 Process Data
 Write to destination

Example: SUBFSR 2, 23h

Before Instruction

FSR2 = 03FFh

After Instruction

FSR2 = 03DCh

Syntax: SUBULNK k Operands: $0 \le k \le 63$

 $Operation: \qquad FSR2-k \rightarrow FSR2,$

 $(TOS) \rightarrow PC$

Status Affected: None

SUBULNK

Description:

Encoding: 1110 1001 11kk kkkk

contents of the FSR2. A RETURN is then executed by loading the PC with the TOS. The instruction takes two cycles to

The 6-bit literal 'k' is subtracted from the

execute; a NOP is performed during the

second cycle.

This may be thought of as a special case of the $\verb"SUBFSR"$ instruction, where f = 3 (binary

'11'); it operates only on FSR2.

Words: 1
Cycles: 2
Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination
No	No	No	No
Operation	Operation	Operation	Operation

Example: SUBULNK 23h

Before Instruction

FSR2 = 03FFh PC = 0100h

After Instruction

FSR2 = 03DChPC = (TOS)

19.2.3 BYTE-ORIENTED AND BIT-ORIENTED INSTRUCTIONS IN INDEXED LITERAL OFFSET MODE

Note: Enabling the PIC18 instruction set extension may cause legacy applications to behave erratically or fail entirely.

In addition to eight new commands in the extended set, enabling the extended instruction set also enables Indexed Literal Offset Addressing mode (Section 5.6.1 "Indexed Addressing with Literal Offset"). This has a significant impact on the way that many commands of the standard PIC18 instruction set are interpreted.

When the extended set is disabled, addresses embedded in opcodes are treated as literal memory locations: either as a location in the Access Bank ('a' = 0) or in a GPR bank designated by the BSR ('a' = 1). When the extended instruction set is enabled and 'a' = 0, however, a file register argument of 5Fh or less is interpreted as an offset from the pointer value in FSR2 and not as a literal address. For practical purposes, this means that all instructions that use the Access RAM bit as an argument – that is, all byteoriented and bit-oriented instructions, or almost half of the core PIC18 instructions – may behave differently when the extended instruction set is enabled.

When the content of FSR2 is 00h, the boundaries of the Access RAM are essentially remapped to their original values. This may be useful in creating backward compatible code. If this technique is used, it may be necessary to save the value of FSR2 and restore it when moving back and forth between C and assembly routines in order to preserve the Stack Pointer. Users must also keep in mind the syntax requirements of the extended instruction set (see Section 19.2.3.1 "Extended Instruction Syntax with Standard PIC18 Commands").

Although the Indexed Literal Offset Addressing mode can be very useful for dynamic stack and pointer manipulation, it can also be very annoying if a simple arithmetic operation is carried out on the wrong register. Users who are accustomed to the PIC18 programming must keep in mind that, when the extended instruction set is enabled, register addresses of 5Fh or less are used for Indexed Literal Offset Addressing.

Representative examples of typical byte-oriented and bit-oriented instructions in the Indexed Literal Offset Addressing mode are provided on the following page to show how execution is affected. The operand conditions shown in the examples are applicable to all instructions of these types.

19.2.3.1 Extended Instruction Syntax with Standard PIC18 Commands

When the extended instruction set is enabled, the file register argument, 'f', in the standard byte-oriented and bit-oriented commands is replaced with the literal offset value, 'k'. As already noted, this occurs only when 'f' is less than or equal to 5Fh. When an offset value is used, it must be indicated by square brackets ("[]"). As with the extended instructions, the use of brackets indicates to the compiler that the value is to be interpreted as an index or an offset. Omitting the brackets, or using a value greater than 5Fh within brackets, will generate an error in the MPASM Assembler.

If the index argument is properly bracketed for Indexed Literal Offset Addressing mode, the Access RAM argument is never specified; it will automatically be assumed to be '0'. This is in contrast to standard operation (extended instruction set disabled) when 'a' is set on the basis of the target address. Declaring the Access RAM bit in this mode will also generate an error in the MPASM Assembler.

The destination argument, 'd', functions as before.

In the latest versions of the MPASM assembler, language support for the extended instruction set must be explicitly invoked. This is done with either the command line option, /y, or the PE directive in the source listing.

19.2.4 CONSIDERATIONS WHEN ENABLING THE EXTENDED INSTRUCTION SET

It is important to note that the extensions to the instruction set may not be beneficial to all users. In particular, users who are not writing code that uses a software stack may not benefit from using the extensions to the instruction set.

Additionally, the Indexed Literal Offset Addressing mode may create issues with legacy applications written to the PIC18 assembler. This is because instructions in the legacy code may attempt to address registers in the Access Bank below 5Fh. Since these addresses are interpreted as literal offsets to FSR2 when the instruction set extension is enabled, the application may read or write to the wrong data addresses.

When porting an application to the PIC18F2450/4450, it is very important to consider the type of code. A large, re-entrant application that is written in 'C' and would benefit from efficient compilation will do well when using the instruction set extensions. Legacy applications that heavily use the Access Bank will most likely not benefit from using the extended instruction set.

ADDWF ADD W to Indexed (Indexed Literal Offset mode)

Syntax: ADDWF [k] {,d}

Operation: $(W) + ((FSR2) + k) \rightarrow dest$

Status Affected: N, OV, C, DC, Z

Encoding: 0010 01d0 kkkk kkkk

Description: The contents of W are added to the contents of the register indicated by

FSR2, offset by the value 'k'.

If 'd' is '0', the result is stored in W. If 'd'

is '1', the result is stored back in

register 'f' (default).

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process	Write to
		Data	destination

Example: ADDWF [OFST],0

Before Instruction

W = 17h OFST = 2Ch FSR2 = 0A00h Contents of 0A2Ch = 20h

After Instruction

W = 37h Contents of 0A2Ch = 20h BSF Bit Set Indexed

(Indexed Literal Offset mode)

Syntax: BSF [k], b

Operands: $0 \le f \le 95$ $0 \le b \le 7$

Operation: $1 \rightarrow ((FSR2) + k) < b >$

Status Affected: None

Encoding: 1000 bbb0 kkkk kkkk

Description: Bit 'b' of the register indicated by FSR2,

offset by the value 'k', is set.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example:
BSF [FLAG_OFST], 7

Before Instruction

FLAG_OFST = 0Ah FSR2 = 0A00h Contents of 0A0Ah = 55h

After Instruction

Contents of 0A0Ah = D5h

SETF Set Indexed

(Indexed Literal Offset mode)

Syntax: SETF [k] Operands: $0 \le k \le 95$

Operation: FFh \rightarrow ((FSR2) + k)

Status Affected: None

Encoding: 0110 1000 kkkk kkkk

Description: The contents of the register indicated by FSR2, offset by 'k', are set to FFh.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4	
Decode	Read 'k'	Process	Write	
		Data	register	

Example: SETF [OFST]

Before Instruction

OFST = 2Ch FSR2 = 0A00h Contents of 0A2Ch = 00h

After Instruction

Contents of 0A2Ch = FFh

19.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB® IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set of the PIC18F2450/4450 family of devices. This includes the MPLAB C18 C compiler, MPASM Assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '0', disabling the extended instruction set and Indexed Literal Offset Addressing mode. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option, or dialog box within the environment, that allows the user to configure the language tool and its settings for the project
- · A command line option
- · A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.

20.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- · Integrated Development Environment
 - MPLAB® IDE Software
- · Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C18 and MPLAB C30 C Compilers
 - MPLINK™ Object Linker/ MPLIB™ Object Librarian
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB REAL ICE™ In-Circuit Emulator
- · In-Circuit Debugger
 - MPLAB ICD 2
- · Device Programmers
 - PICSTART® Plus Development Programmer
 - MPLAB PM3 Device Programmer
 - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

20.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- · A multiple project manager
- Customizable data windows with direct edit of contents
- · High-level source code debugging
- Visual device initializer for easy register initialization
- · Mouse over variable inspection
- Drag and drop variables from source to watch windows
- · Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - Source files (assembly or C)
 - Mixed assembly and C
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

20.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

20.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

20.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

20.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire dsPIC30F instruction set
- · Support for fixed-point and floating-point data
- · Command line interface
- · Rich directive set
- · Flexible macro language
- · MPLAB IDE compatibility

20.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

20.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

20.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

20.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers costeffective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

20.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

20.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

20.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

20.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, Keeloq® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

21.0 ELECTRICAL CHARACTERISTICS

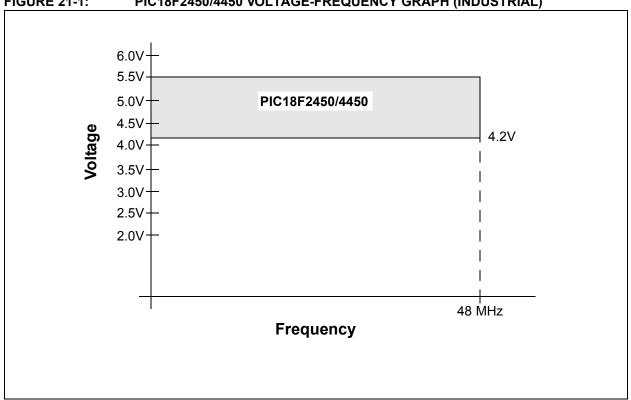
Absolute Maximum Ratings^(†)

Ambient temperature under bias	40°C to +85°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, loκ (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

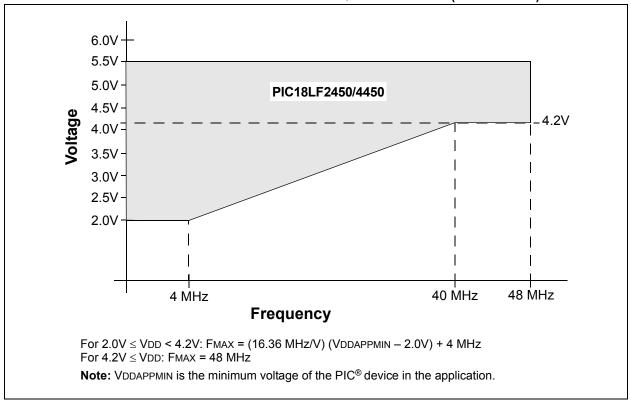
- **Note 1:** Power dissipation is calculated as follows: Pdis = VDD x {IDD Σ IOH} + Σ {(VDD VOH) x IOH} + Σ (VOL x IOL)
 - 2: Voltage spikes below Vss at the $\overline{MCLR}/VPP/RE3$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{MCLR}/VPP/RE3$ pin, rather than pulling this pin directly to Vss.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 21-1: PIC18F2450/4450 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)







21.1 DC Characteristics: Supply Voltage

Supply Voltage PIC18F2450/4450 (Industrial) PIC18LF2450/4450 (Industrial)

PIC18LF2450/4450 (Industrial) PIC18F2450/4450 (Industrial)				Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial							
D001	VDD	Supply Voltage	2.0	_	5.5	V	EC, HS, XT and Internal Oscillator modes				
			3.0	_	5.5	V	HSPLL, XTPLL, ECPIO and ECPLL Oscillator modes				
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5	_	_	V					
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	_	_	0.7	V	See Section 4.3 "Power-on Reset (POR)" for details				
D004	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	_	_	V/ms	See Section 4.3 "Power-on Reset (POR)" for details				
D005	VBOR	Brown-out Reset Voltage		•							
		BORV1:BORV0 = 11	2.00	2.11	2.22	V					
		BORV1:BORV0 = 10	2.65	2.79	2.93	V					
		BORV1:BORV0 = 01	4.11	4.33	4.55	V					
		BORV1:BORV0 = 00	4.36	4.59	4.82	V					

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

21.2 DC Characteristics: Power-Down and Supply Current PIC18F2450/4450 (Industrial)

PIC18LF2450/4450 (Industrial)

PIC18LF2 (Indust		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial										
	PIC18F2450/4450 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial								
Param No.	Device	Тур	Max	Units	Conditio	ns						
	Power-Down Current (IPD)	(1)										
	PIC18LF2450/4450	0.1	0.95	μА	-40°C	.,						
		0.1	1.0	μΑ	+25°C	V _{DD} = 2.0V (Sleep mode)						
		0.1	5.0	μА	+85°C	(Sieep mode)						
	PIC18LF2450/4450	0.1	1.4	μА	-40°C	.,						
		0.1	2.0	μА	+25°C	V _{DD} = 3.0V (Sleep mode)						
		1.5	8.0	μА	+85°C	(Sieep mode)						
	All devices	0.1	19	μА	-40°C							
		0.1	2.0	μА	+25°C	V _{DD} = 5.0V (Sleep mode)						
		2.5	15	μА	+85°C	(Sieep mode)						

Legend: Shading of rows is to assist in readability of the table.

- Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
 - 2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current PIC18F2450/4450 (Industrial) PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2 (Indust		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
PIC18F24 (Indust		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial								
Param No.	Device	Тур	Max	Units		Conditio	ns			
	Supply Current (IDD) ⁽²⁾									
	PIC18LF2450/4450	10	32	μА	-40°C					
		10	30	μΑ	+25°C	VDD = 2.0V				
		12	29	μА	+85°C					
	PIC18LF2450/4450	35	63	μА	-40°C		Fosc = 31 kHz			
		30	60	μΑ	+25°C	VDD = 3.0V	(RC_RUN mode,			
		25	57	μА	+85°C		INTRC source)			
	All devices	95	168	μА	-40°C					
		75	160	μА	+25°C	VDD = 5.0V				
		65	152	μА	+85°C					
	PIC18LF2450/4450	2.3	8	μΑ	-40°C					
		2.5	8	μΑ	+25°C	VDD = 2.0V				
		3.3	11	μΑ	+85°C					
	PIC18LF2450/4450	3.3	11	μА	-40°C		Fosc = 31 kHz			
		3.6	11	μΑ	+25°C	VDD = 3.0V	(RC_IDLE mode,			
		4.0	15	μА	+85°C		INTRC source)			
	All devices	6.5	16	μΑ	-40°C					
		7.0	16	μΑ	+25°C	VDD = 5.0V				
		9.0	36	μΑ	+85°C					

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current

PIC18F2450/4450 (Industrial)

PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2 (Indust	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial										
PIC18F24 (Indust		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial									
Param No.	Device	Тур	Max	Units		Conditions					
	Supply Current (IDD) ⁽²⁾										
	PIC18LF2450/4450	200	500	μΑ	-40°C						
		200	500	μΑ	+25°C	VDD = 2.0V					
		200	500	μΑ	+85°C						
	PIC18LF2450/4450	500	650	μΑ	-40°C		Fosc = 1 MHz				
		400	650	μΑ	+25°C	VDD = 3.0V	(PRI_RUN,				
		360	650	μА	+85°C		EC oscillator)				
	All devices	1.0	1.6	mA	-40°C						
		0.9	1.5	mA	+25°C	VDD = 5.0V	l				
		8.0	1.4	mA	+85°C						
	PIC18LF2450/4450	0.53	2.0	mA	-40°C						
		0.53	2.0	mA	+25°C	VDD = 2.0V					
		0.55	2.0	mA	+85°C	1					
	PIC18LF2450/4450	1.0	3.0	mA	-40°C		Fosc = 4 MHz				
		0.9	3.0	mA	+25°C	VDD = 3.0V	(PRI_RUN,				
		0.9	3.0	mA	+85°C		EC oscillator)				
	All devices	2.0	6.0	mA	-40°C						
		1.9	6.0	mA	+25°C	VDD = 5.0V					
		1.8	6.0	mA	+85°C						
	All devices	11.0	35	mA	-40°C						
		11.0	35	mA	+25°C	VDD = 4.2V	F				
		11.3	35	mA	+85°C		Fosc = 40 MHz (PRI_RUN ,				
	All devices	14.0	40	mA	-40°C		EC oscillator)				
		14.0	40	mA	+25°C	VDD = 5.0V					
		14.5	40	mA	+85°C						
	All devices	20	40	mA	-40°C						
		20	40	mA	+25°C	VDD = 4.2V	F 40.141				
		20	40	mA	+85°C		Fosc = 48 MHz (PRI_RUN ,				
	All devices	25	50	mA	-40°C		EC oscillator)				
		25	50	mA	+25°C	VDD = 5.0V	20 000				
		25	50	mA	+85°C						

Legend: Shading of rows is to assist in readability of the table.

- Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
 - 2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current PIC18F2450/4450 (Industrial) PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2 (Indus	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial									
PIC18F24 (Indus		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	Device	Тур	Max	Units		Condition	ıs			
	Supply Current (IDD) ⁽²⁾									
	PIC18LF2450/4450	50	130	μА	-40°C					
		50	120	μΑ	+25°C	VDD = 2.0V				
		50	115	μА	+85°C					
	PIC18LF2450/4450	75	270	μΑ	-40°C		Fosc = 1 MHz			
		80	250	μΑ	+25°C	VDD = 3.0V	(PRI_IDLE mode,			
		80	240	μА	+85°C		EC oscillator)			
	All devices	150	480	μА	-40°C					
		150	450	μА	+25°C	VDD = 5.0V				
		150	430	μА	+85°C					
	PIC18LF2450/4450	190	475	μА	-40°C					
		195	450	μА	+25°C	VDD = 2.0V	Fosc = 4 MHz (PRI_IDLE mode, EC oscillator)			
		200	430	μА	+85°C					
	PIC18LF2450/4450	295	900	μА	-40°C					
		300	850	μА	+25°C	VDD = 3.0V				
		310	810	μА	+85°C					
	All devices	560	1.5	mA	-40°C					
		570	1.4	mA	+25°C	VDD = 5.0V				
		580	1.3	mA	+85°C					
	All devices	4.4	16	mA	-40°C					
		4.5	16	mA	+25°C	VDD = 4.2V	F000 - 40 MIL			
		4.6	16	mA	+85°C		Fosc = 40 MHz (PRI_IDLE mode,			
	All devices	5.5	18	mA	-40°C	_	EC oscillator)			
		5.6	18	mA	+25°C	VDD = 5.0V	,			
		5.8	18	mA	+85°C					
	All devices	8.0	18	mA	-40°C	_				
		8.1	18	mA	+25°C	VDD = 4.2V	F000 - 40 MU-			
		8.2	18	mA	+85°C		Fosc = 48 MHz (PRI_IDLE mode,			
	All devices	9.8	21	mA	-40°C	_	EC oscillator)			
		10.0	21	mA	+25°C	VDD = 5.0V	· · ·			
		10.5	21	mA	+85°C					

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current

PIC18F2450/4450 (Industrial)

PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2 (Indus		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for industrial									
PIC18F24 (Indus			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial								
Param No.	Device	Тур	Max	Units		Conditio	ns				
	Supply Current (IDD) ⁽²⁾										
	PIC18LF2450/4450	13	40	μА	-40°C						
		15	40	μА	+25°C	VDD = 2.0V					
		17	40	μΑ	+85°C						
	PIC18LF2450/4450	40	76	μΑ	-40°C		Fosc = 32 kHz ⁽³⁾				
		32	70	μА	+25°C	VDD = 3.0V	(SEC_RUN mode,				
		25	67	μА	+85°C		Timer1 as clock)				
	All devices	100	150	μΑ	-40°C						
		80	150	μА	+25°C	VDD = 5.0V					
		70	150	μА	+85°C						
	PIC18LF2450/4450	5.6	12	μА	-40°C						
		7.0	12	μА	+25°C	VDD = 2.0V					
		8.3	12	μΑ	+85°C						
	PIC18LF2450/4450	6.5	15	μА	-40°C		Fosc = 32 kHz ⁽³⁾				
		8.0	15	μА	+25°C	VDD = 3.0V	(SEC_IDLE mode,				
		9.5	15	μΑ	+85°C		Timer1 as clock)				
	All devices	8.7	25	μА	-40°C						
		10.2	25	μА	+25°C	VDD = 5.0V					
		13.0	36	μА	+85°C						

Legend: Shading of rows is to assist in readability of the table.

- Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
 - 2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current PIC18F2450/4450 (Industrial) PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2 (Indust	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial												
	PIC18F2450/4450 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial									
Param No.	Device	Тур	Max	Units		Conditio	ns						
D022	Module Differential Currer	nts (∆lw	DT, ∆lbo	or, ∆ILV	D, \triangle IOSCB, \triangle IAD)								
$(\Delta IWDT)$	Watchdog Timer	1.3	3.8	μΑ	-40°C								
		1.5	3.8	μΑ	+25°C	VDD = 2.0V							
		2.3	3.8	μΑ	+85°C								
		1.8	4.6	μΑ	-40°C								
		2.0	4.6	μΑ	+25°C	VDD = 3.0V							
		3.0	4.6	μΑ	+85°C								
		3.3	10	μΑ	-40°C								
		3.6	10	μΑ	+25°C	VDD = 5.0V							
		3.9	10	μΑ	+85°C								
D022A	Brown-out Reset ⁽⁴⁾	40	52	μΑ	-40°C to +85°C	VDD = 3.0V							
(∆lbor)		45	63	μΑ	-40°C to +85°C								
		0	2	μА	-40°C to +85°C	VDD = 5.0V	Sleep mode, BOREN1:BOREN0 = 10						
D022B	High/Low-Voltage	22	47	μΑ	-40°C to +85°C	VDD = 2.0V							
(∆llvd)	Detect ⁽⁴⁾	25	58	μА	-40°C to +85°C	VDD = 3.0V							
		29	69	μΑ	-40°C to +85°C	VDD = 5.0V							
D025	Timer1 Oscillator	1.5	4.5	μΑ	-40°C								
(∆loscb)		1.2	4.5	μΑ	+25°C	VDD = 2.0V	32 kHz on Timer1 ⁽³⁾						
		1.6	4.5	μΑ	+85°C								
		1.7	6.0	μΑ	-40°C								
		1.8	6.0	μΑ	+25°C	VDD = 3.0V	32 kHz on Timer1 ⁽³⁾						
		2.0	6.0	μΑ	+85°C								
		1.4	8.0	μΑ	-40°C								
		1.5	8.0	μΑ	+25°C	VDD = 5.0V	32 kHz on Timer1 ⁽³⁾						
		1.9	8.0	μΑ	+85°C								
D026	A/D Converter	0.2	2.0	μΑ	-40°C to +85°C	VDD = 2.0V							
(∆lad)		0.2	2.0	μΑ	-40°C to +85°C	VDD = 3.0V	A/D on, not converting						
		0.2	2.0	μΑ	-40°C to +85°C	VDD = 5.0V							

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or Vss;

MCLR = VDD; WDT enabled/disabled as specified.

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current

PIC18F2450/4450 (Industrial)

PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2 (Indust			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial							
PIC18F24 (Indust	******	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial								
Param No.	Device	Тур	Max	Units	Conditions					
	USB and Related Module	Differer	tial Cu	rrents (ΔIUSBX, ΔIPLL, ΔΙ	JREG)				
Δ lusbx	USB Module	0.0	14.5	mA	+25°C	VDD = 3.3V				
	with On-Chip Transceiver	12.4	20	mA	+25°C	VDD = 5.0V				
$\Delta IPLL$	96 MHz PLL		3.0	mA	+25°C	VDD = 3.3V				
	(Oscillator Module)	1.2	4.8	mA	+25°C	VDD = 5.0V				
Δlureg	USB Internal Voltage Regulator	80	125	μА	+25°C	V _{DD} = 5.0V	USB Idle, UCON <suspnd> = 1</suspnd>			

Legend: Shading of rows is to assist in readability of the table.

- Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
 - 2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.2 DC Characteristics: Power-Down and Supply Current PIC18F2450/4450 (Industrial)

PIC18LF2450/4450 (Industrial) (Continued)

PIC18LF2		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for industrial							
PIC18F24		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for industrial							
Param No.	Device	Тур	Max	Units	Conditions				
ITUSB	Total USB Run Currents (I	TUSB) ⁽²⁾							
	Primary Run with USB		65	mA	-40°C	VDD = 5.0V	EC+PLL 4 MHz input,		
	Module, PLL and USB Voltage Regulator	23	65	mA	+25°C	VDD = 5.0V	48 MHz PRI_RUN,		
		29	65	mA	+85°C	VDD = 5.0V	USB module enabled in Full-Speed mode, USB VREG enabled, no bus traffic		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or Vss and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- 3: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- **4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

21.3 DC Characteristics: PIC18F2450/4450 (Industrial) PIC18LF2450/4450 (Industrial)

DC CHA	ARACTE	RISTICS				(unless otherwise stated) ∆ ≤ +85°C for industrial
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
	VIL	Input Low Voltage				
		I/O Ports (except RC4/RC5 in USB mode):				
D030		with TTL Buffer	Vss	0.15 VDD	V	VDD < 4.5V
D030A			_	0.8	V	$4.5V \leq V \text{DD} \leq 5.5V$
D032		MCLR	Vss	0.2 Vdd	V	
D032A		OSC1 and T1OSI	Vss	0.3 VDD	V	XT, HS, HSPLL modes ⁽¹⁾
D033		OSC1	Vss	0.2 VDD	V	EC mode ⁽¹⁾
	VIH	Input High Voltage I/O Ports (except RC4/RC5 in USB mode):				
D040		with TTL Buffer	0.25 VDD + 0.8V	VDD	V	VDD < 4.5V
D040A			2.0	VDD	V	$4.5V \leq VDD \leq 5.5V$
D042		MCLR	0.8 VDD	VDD	V	
D042A		OSC1 and T1OSI	0.7 VDD	VDD	V	XT, HS, HSPLL modes ⁽¹⁾
D043		OSC1	0.8 VDD	Vdd	V	EC mode ⁽¹⁾
	lıL	Input Leakage Current ^(2,3)				
D060		I/O Ports (except D+ and D-)	_	±200	nA	VDD = 5V
			_	±50	nA	VDD = 3V
D061		MCLR	_	±1	μΑ	$Vss \leq V \texttt{PIN} \leq V \texttt{DD}$
D063		OSC1	_	±1	μΑ	$Vss \leq VPIN \leq VDD$
	IPU	Weak Pull-up Current				
D070	IPURB	PORTB Weak Pull-up Current	50	400	μΑ	VDD = 5V, VPIN = VSS

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® microcontroller be driven with an external clock while in RC mode.

^{2:} The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{3:} Negative current is defined as current sourced by the pin.

^{4:} Parameter is characterized but not tested.

21.3 DC Characteristics: PIC18F2450/4450 (Industrial) PIC18LF2450/4450 (Industrial) (Continued)

			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial				
Param No.	Sym	Characteristic	Min	Max	Units	Conditions	
	Vol	Output Low Voltage					
D080		I/O Ports (except RC4/RC5 in USB mode)	_	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C	
D083		OSC2/CLKO (EC, ECIO modes)	_	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C	
	Vон	Output High Voltage ⁽³⁾					
D090		I/O Ports (except RC4/RC5 in USB mode)	VDD - 0.7	_	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C	
D092		OSC2/CLKO (EC, ECIO, ECPIO modes)	VDD - 0.7	_	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C	
		Capacitive Loading Specs on Output Pins					
D100 ⁽⁴⁾	Cosc2	OSC2 pin	_	15	pF	In XT and HS modes when external clock is used to drive OSC1	
D101	Сю	All I/O pins and OSC2 (in RC mode)	_	50	pF	To meet the AC Timing Specifications	

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® microcontroller be driven with an external clock while in RC mode.

- **3:** Negative current is defined as current sourced by the pin.
- 4: Parameter is characterized but not tested.

^{2:} The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

TABLE 21-1: MEMORY PROGRAMMING REQUIREMENTS

			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for industrial					
Param No.	Sym Characteristic		Characteristic Min Typ† Max l		Units	Conditions		
		Internal Program Memory Programming Specifications ⁽¹⁾						
D110	VIHH	Voltage on MCLR/VPP/RE3 pin	9.00	_	13.25	V	(Note 2)	
D113	IDDP	Supply Current during Programming	_	_	10	mA		
		Program Flash Memory						
D130	EР	Cell Endurance	10K	100K	_	E/W	-40°C to +85°C	
D131	VPR	VDD for Read	VMIN	_	5.5	V	VMIN = Minimum operating voltage	
D132	VIE	VDD for Block Erase	4.5	_	5.5	V	Using ICSP™ port	
D132A	Viw	VDD for Externally Timed Erase or Write	3.0	_	5.5	V	Using ICSP port	
D132B	VPEW	VDD for Self-Timed Write	VMIN	_	5.5	V	VMIN = Minimum operating voltage	
D133	TIE	ICSP™ Block Erase Cycle Time	_	4	_	ms	VDD > 4.5V	
D133A	Tıw	ICSP Erase or Write Cycle Time (externally timed)	1	_	_	ms	VDD > 4.5V	
D133A	Tıw	Self-Timed Write Cycle Time	_	2	_	ms		
D134	TRETD	Characteristic Retention	40	100	_	Year	Provided no other specifications are violated	

[†] Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

^{2:} Required only if Single-Supply Programming is disabled.

TABLE 21-2: USB MODULE SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated).									
Param No.	Sym	Characteristic	Min	Тур	Max	Units	Comments		
D313	Vusb	USB Voltage	3.0	_	3.6	V	Voltage on bus must be in this range for proper USB operation		
D314	II∟	Input Leakage on D+ or D- pin	_	_	±1	μА	Vss ≤ VPIN ≤ VDD; pin at high-impedance		
D315	VILUSB	Input Low Voltage for USB Buffer	_	_	0.8	V	For VusB range		
D316	VIHUSB	Input High Voltage for USB Buffer	2.0	_	_	V	For VusB range		
D317	VCRS	Crossover Voltage	1.3		2.0	V	Voltage range for D+ and D- crossover to occur		
D318	VDIFS	Differential Input Sensitivity	_	_	0.2	V	The difference between D+ and D- must exceed this value while VCM is met		
D319	Vсм	Differential Common Mode Range	0.8	_	2.5	V			
D320	Zout	Driver Output Impedance	28	_	44	Ω			
D321	Vol	Voltage Output Low	0.0		0.3	V	1.5 k Ω load connected to 3.6V		
D322	Vон	Voltage Output High	2.8		3.6	V	15 k Ω load connected to ground		

TABLE 21-3: USB INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated).								
Param No.	Sym Characteristics Min Lyn Max Linits Comments							
D323	VUSBANA	Regulator Output Voltage	3.0	_	3.6	V	$V_{DD} > 4.0V^{(1)}$	
D324	Cusb	External Filter Capacitor Value	220	470	_	nF	Low ESR	

Note 1: If device VDD is less than 4.0V, the internal USB voltage regulator should be disabled and an external 3.0-3.6V supply should be provided on VUSB.

FIGURE 21-3: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

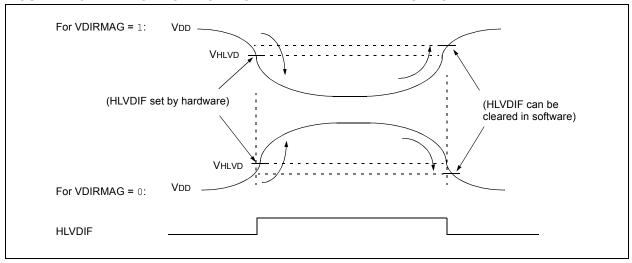


TABLE 21-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial									
Param No.	Sym	Characteristic			Тур	Max	Units	Conditions	
D420		HLVD Voltage on VDD	HLVDL<3:0> = 0000	2.06	2.17	2.28	V		
		Transition High-to-Low	HLVDL<3:0> = 0001	2.12	2.23	2.34	V		
			HLVDL<3:0> = 0010	2.24	2.36	2.48	V		
			HLVDL<3:0> = 0011	2.32	2.44	2.56	V		
			HLVDL<3:0> = 0100	2.47	2.60	2.73	V		
			HLVDL<3:0> = 0101	2.65	2.79	2.93	V		
			HLVDL<3:0> = 0110	2.74	2.89	3.04	V		
			HLVDL<3:0> = 0111	2.96	3.12	3.28	V		
			HLVDL<3:0> = 1000	3.22	3.39	3.56	V		
			HLVDL<3:0> = 1001	3.37	3.55	3.73	V		
			HLVDL<3:0> = 1010	3.52	3.71	3.90	V		
			HLVDL<3:0> = 1011	3.70	3.90	4.10	V		
			HLVDL<3:0> = 1100	3.90	4.11	4.32	V		
			HLVDL<3:0> = 1101	4.11	4.33	4.55	V		
			HLVDL<3:0> = 1110	4.36	4.59	4.82	V		

21.4 AC (Timing) Characteristics

21.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

- 1. TppS2ppS
- 2. TppS

T				_
F	Frequency	Т	Time	
Lowercase	e letters (pp) and their meanings:			
рр				
		mc	MCLR	
СС	CCP1	osc	OSC1	
ck	CLKO	wr	WR	
dt	Data in	t0	T0CKI	
io	I/O port	t1	T1CKI	
:Uppercas	e Letters and their meanings			
S				
F	Fall	Р	Period	
Н	High	R	Rise	
I	Invalid (High-Impedance)	V	Valid	
L	Low	Z	High-Impedance	
		High	High	
		Low	Low	

21.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 21-5 apply to all timing specifications unless otherwise noted. Figure 21-4 specifies the load conditions for the timing specifications.

Because of space limitations, the generic terms "PIC18FXXXX" and "PIC18LFXXXX" are used throughout this section to refer to the PIC18F2450/4450 and PIC18LF2450/4450 families of devices specifically and only those devices.

TABLE 21-5: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

Standard Operating Conditions (unless otherwise stated)

Note:

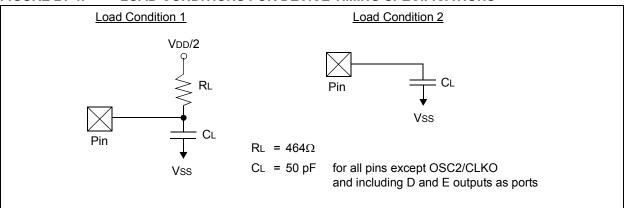
Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial

AC CHARACTERISTICS Operating voltage VDD range as described in DC spec Section 21.1 and

Section 21.3.

LF parts operate for industrial temperatures only.

FIGURE 21-4: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



21.4.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 21-5: EXTERNAL CLOCK TIMING (ALL MODES EXCEPT PLL)

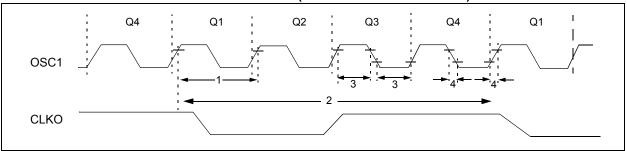


TABLE 21-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	Fosc	External CLKI Frequency(1)	DC	48	MHz	EC, ECIO Oscillator modes
		Oscillator Frequency ⁽¹⁾	0.2	1	MHz	XT, XTPLL Oscillator modes
			4	25	MHz	HS Oscillator mode
			4	25	MHz	HSPLL Oscillator mode
1	Tosc	External CLKI Period ⁽¹⁾	20.8	_	ns	EC, ECIO Oscillator modes
		Oscillator Period ⁽¹⁾	1,000	5,000	ns	XT Oscillator mode
			40	250	ns	HS Oscillator mode
			40	250	ns	HSPLL Oscillator mode
2	Tcy	Instruction Cycle Time ⁽¹⁾	83.3	_	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1)	30	_	ns	XT Oscillator mode
	TosH	High or Low Time	10	_	ns	HS Oscillator mode
4	TosR,	External Clock in (OSC1)	_	20	ns	XT Oscillator mode
	TosF	Rise or Fall Time	-	7.5	ns	HS Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

TABLE 21-7: PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 5.5V)

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
F10	Fosc	Oscillator Frequency Range	4	_	48	MHz	
F11	Fsys	On-Chip VCO System Frequency	_	96	_	MHz	
F12	t _{rc}	PLL Start-up Time (lock time)	_	_	2	ms	
F13	Δ CLK	CLKO Stability (jitter)	-0.25	_	+0.25	%	

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 21-8: AC CHARACTERISTICS: INTERNAL RC ACCURACY
PIC18F2450/4450 (INDUSTRIAL)
PIC18LF2450/4450 (INDUSTRIAL)

PIC18LF2450/4450 (Industrial) Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
PIC18F2450/4450 (Industrial) Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	Device	Min	Тур	Max	Units	Conditions		
	INTRC Accuracy @ Freq = 31 kHz ⁽¹⁾							
	PIC18LF2450/4450	26.562	_	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V	
	PIC18F2450/4450	26.562	_	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: INTRC frequency after calibration.

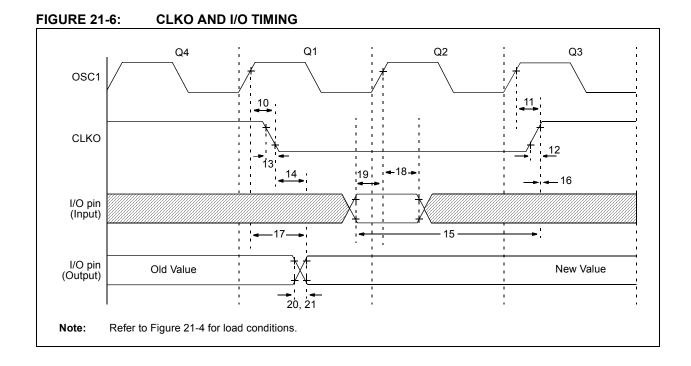


TABLE 21-9: CLKO AND I/O TIMING REQUIREMENTS

Param No.	Symbol	Characteri	stic	Min	Тур	Max	Units	Conditions
10	TosH2ckL	OSC1 ↑ to CLKO ↓		_	75	200	ns	(Note 1)
11	TosH2ckH	OSC1 ↑ to CLKO ↑		_	75	200	ns	(Note 1)
12	TckR	CLKO Rise Time		_	35	100	ns	(Note 1)
13	TckF	CLKO Fall Time	CLKO Fall Time		35	100	ns	(Note 1)
14	TckL2ioV	LKO ↓ to Port Out Valid		_	_	0.5 Tcy + 20	ns	(Note 1)
15	TioV2ckH	Port In Valid before CLKC	ort In Valid before CLKO ↑		_	_	ns	(Note 1)
16	TckH2ioI	Port In Hold after CLKO 1		0	_	_	ns	(Note 1)
17	TosH2ioV	OSC1 ↑ (Q1 cycle) to Po	OSC1 ↑ (Q1 cycle) to Port Out Valid		50	150	ns	
18	TosH2iol	OSC1 ↑ (Q2 cycle) to	PIC18FXXXX	100	_	_	ns	
18A		Port Input Invalid (I/O in hold time)	PIC18 LF XXXX	200	_	_	ns	VDD = 2.0V
19	TioV2osH	Port Input Valid to OSC1 ↑ time)	(I/O in setup	0	_	_	ns	
20	TioR	Port Output Rise Time	PIC18FXXXX	_	10	25	ns	
20A			PIC18 LF XXXX	_	_	60	ns	VDD = 2.0V
21	TioF	Port Output Fall Time	PIC18FXXXX	_	10	25	ns	
21A			PIC18 LF XXXX	_	_	60	ns	VDD = 2.0V
22†	TINP	INTx Pin High or Low Time		Tcy	_	_	ns	
23†	TRBP	RB7:RB4 Change Interru Time	pt High or Low	Tcy		_	ns	

[†] These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode, where CLKO output is 4 x Tosc.

FIGURE 21-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

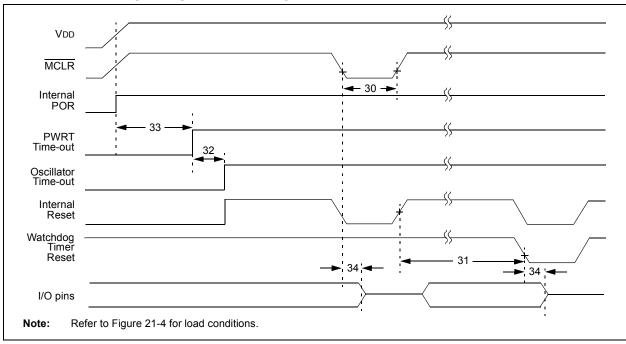


FIGURE 21-8: BROWN-OUT RESET TIMING

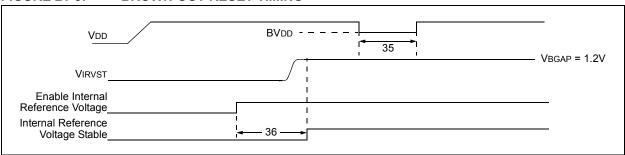


TABLE 21-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	_	_	μS	
31	TWDT	Watchdog Timer Time-out Period (no postscaler)	_	4.00	4.6	ms	
32	Tost	Oscillator Start-up Timer Period	1024 Tosc	_	1024 Tosc	_	Tosc = OSC1 period
33	TPWRT	Power-up Timer Period	_	65.5	75	ms	
34	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	_	2	_	μS	
35	TBOR	Brown-out Reset Pulse Width	200	_	_	μS	V _{DD} ≤ B _{VDD} (see D005)
36	TIRVST	Time for Internal Reference Voltage to become Stable	_	20	50	μS	
37	TLVD	Low-Voltage Detect Pulse Width	200	_	_	μS	$VDD \le VLVD$
38	TCSD	CPU Start-up Time	5	_	10	μS	
39	TIOBST	Time for INTRC to Stabilize	_	1	_	ms	

T0CKI T10S0/T1CKI TMR0 or -TMR1_ Refer to Figure 21-4 for load conditions. Note:

FIGURE 21-9: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

TABLE 21-11: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol		Characteristic		Min	Max	Units	Conditions
40	Tt0H	T0CKI High P	ulse Width	No prescaler	0.5 Tcy + 20	_	ns	
				With prescaler	10	_	ns	
41	Tt0L	T0CKI Low Pu	ılse Width	No prescaler	0.5 Tcy + 20	_	ns	
					10	_	ns	
42	Tt0P	T0CKI Period	OCKI Period N		Tcy + 10	_	ns	
				With prescaler	Greater of: 20 ns or (Tcy + 40)/N	_	ns	N = prescale value (1, 2, 4,, 256)
45	Tt1H	T1CKI High	Synchronous, no	o prescaler	0.5 Tcy + 20	_	ns	
		Time	Synchronous,	PIC18FXXXX	10	_	ns	
			with prescaler	PIC18 LF XXXX	25	_	ns	VDD = 2.0V
			Asynchronous	PIC18FXXXX	30	_	ns	
				PIC18 LF XXXX	50	_	ns	VDD = 2.0V
46	Tt1L	T1CKI Low	Synchronous, no	o prescaler	0.5 Tcy + 5	_	ns	
		Time	Synchronous,	PIC18FXXXX	10	_	ns	
			with prescaler	PIC18 LF XXXX	25	_	ns	VDD = 2.0V
			Asynchronous	PIC18FXXXX	30	_	ns	
				PIC18 LF XXXX	50	_	ns	VDD = 2.0V
47	Tt1P	T1CKI Input Period	Synchronous		Greater of: 20 ns or (Tcy + 40)/N	_	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		60	_	ns	
	Ft1	T1CKI Oscillat	tor Input Frequency Range		DC	50	kHz	
48	Tcke2tmrl	Delay from Ex Increment	ternal T1CKI Cloc	k Edge to Timer	2 Tosc	7 Tosc	_	

FIGURE 21-10: CAPTURE/COMPARE/PWM TIMINGS (CCP MODULE)

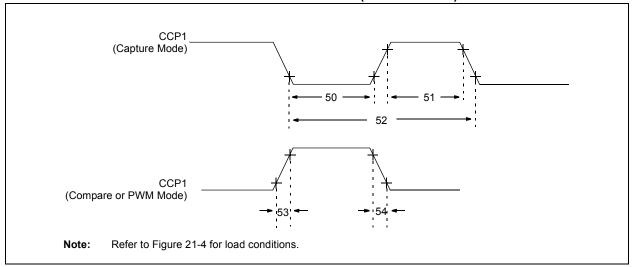


TABLE 21-12: CAPTURE/COMPARE/PWM REQUIREMENTS

Param No.	Symbol	С	Characteristic		Min	Max	Units	Conditions
50	TccL	CCP1 Input			0.5 Tcy + 20	_	ns	
			With	PIC18FXXXX	10	_	ns	
		prescaler	PIC18 LF XXXX	20	_	ns	VDD = 2.0V	
51	TccH	CCP1 Input No prescaler		er	0.5 Tcy + 20	_	ns	
	High Time	With	PIC18FXXXX	10	_	ns		
			prescaler	PIC18 LF XXXX	20	_	ns	VDD = 2.0V
52	TccP	CCP1 Input Perio	od		3 Tcy + 40 N	_	ns	N = prescale value (1, 4 or 16)
53	TccR	CCP1 Output Fa	II Time	PIC18FXXXX	_	25	ns	
				PIC18 LF XXXX	_	45	ns	VDD = 2.0V
54	TccF CCP1 Output Fall Time		PIC18FXXXX	_	25	ns		
				PIC18 LF XXXX	_	45	ns	VDD = 2.0V

FIGURE 21-11: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

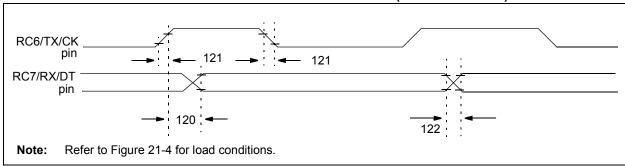


TABLE 21-13: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock High to Data Out Valid	PIC18 F XXXX		40	ns	
			PIC18 LF XXXX	_	100	ns	VDD = 2.0V
121	Tckrf	Clock Out Rise Time and Fall Time	PIC18FXXXX	_	20	ns	
	(Master mode)		PIC18 LF XXXX	_	50	ns	VDD = 2.0V
122	Tdtrf	Data Out Rise Time and Fall Time	PIC18FXXXX	_	20	ns	
			PIC18 LF XXXX	_	50	ns	VDD = 2.0V

FIGURE 21-12: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

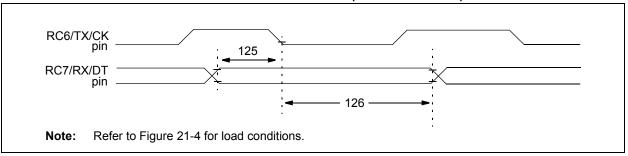


TABLE 21-14: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
125	TDTV2CKL	SYNC RCV (MASTER & SLAVE) Data Hold before CK ↓ (DT hold time)	10	_	ns	
126	TCKL2DTL	Data Hold after CK ↓ (DT hold time)	15	_	ns	

FIGURE 21-13: USB SIGNAL TIMING

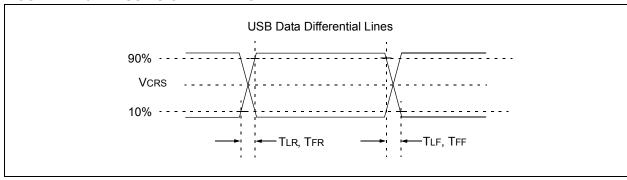


TABLE 21-15: USB LOW-SPEED TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
	TLR	Transition Rise Time	75	_	300	ns	CL = 200 to 600 pF
	TLF	Transition Fall Time	75		300	ns	CL = 200 to 600 pF
	TLRFM	Rise/Fall Time Matching	80	_	125	%	

TABLE 21-16: USB FULL-SPEED REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
	TFR	Transition Rise Time	4	_	20	ns	CL = 50 pF
	TFF	Transition Fall Time	4	_	20	ns	CL = 50 pF
	TFRFM	Rise/Fall Time Matching	90		111.1	%	

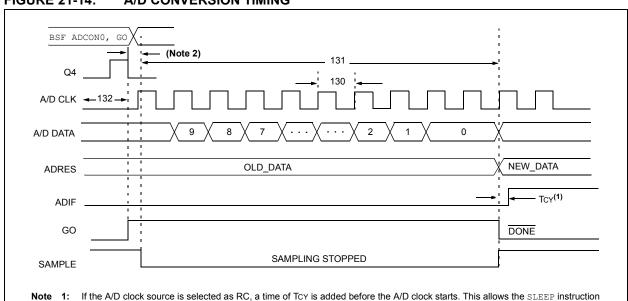
TABLE 21-17: A/D CONVERTER CHARACTERISTICS: PIC18F2450/4450 (INDUSTRIAL) PIC18LF2450/4450 (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
A01	NR	Resolution	_	_	10	bit	$\Delta VREF \ge 3.0V$
A03	EIL	Integral Linearity Error	_		<±1	LSb	ΔV REF $\geq 3.0V$
A04	EDL	Differential Linearity Error	_		<±1	LSb	ΔV REF $\geq 3.0V$
A06	Eoff	Offset Error	_	_	< <u>+2</u>	LSb	$\Delta VREF \ge 3.0V$
A07	Egn	Gain Error	_		<±1	LSb	ΔV REF $\geq 3.0V$
A10	_	Monotonicity	Gı	uarantee	d ⁽¹⁾	_	$Vss \leq Vain \leq Vref$
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	1.8 3			V V	V _{DD} < 3.0V V _{DD} ≥ 3.0V
A21	VREFH	Reference Voltage High	Vss		VREFH	V	
A22	VREFL	Reference Voltage Low	Vss - 0.3V	_	VDD - 3.0V	V	
A25	VAIN	Analog Input Voltage	VREFL	_	VREFH	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	_	_	2.5	kΩ	
A50	IREF	VREF Input Current ⁽²⁾		_	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from RA2/AN2/VREF- pin or VSS, whichever is selected as the VREFL source.

FIGURE 21-14: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

2: This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.

TABLE 21-18: A/D CONVERSION REQUIREMENTS

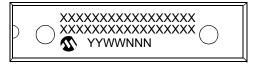
Param No.	Symbol	Charact	eristic	Min	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC18FXXXX	0.7	25 ⁽¹⁾	μS	Tosc based, VREF ≥ 3.0V
			PIC18 LF XXXX	1.4	25 ⁽¹⁾	μS	V _{DD} = 2.0V, Tosc based, V _{REF} full range
			PIC18FXXXX	2.0	6.0	μS	A/D RC mode
			PIC18 LF XXXX	3.0	9.0	μS	V _{DD} = 2.0V, A/D RC mode
131	TCNV	Conversion Time (not including acquisiti	on time) ⁽²⁾	11	12	TAD	
132	TACQ	Acquisition Time ⁽³⁾		15	_	μS	-40°C to +85°C
				10	_	μS	0°C ≤ to ≤ +85°C
135	Tswc	Switching Time from C	onvert → Sample	_	(Note 4)		
137	TDIS	Discharge Time	_	0.2	_	μS	

- Note 1: The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.
 - 2: ADRES registers may be read on the following TcY cycle.
 - 3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to Vss or Vss to VDD). The source impedance (Rs) on the input channels is 50Ω .
 - 4: On the following cycle of the device clock.

22.0 PACKAGING INFORMATION

22.1 Package Marking Information

28-Lead SPDIP (Skinny DIP)



Example



28-Lead SOIC



Example



28-Lead QFN



Example



Legend: XX...X Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

(e3) Pb-free JEDEC designator for Matte Tin (Sn)

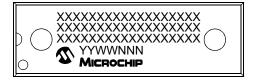
This package is Pb-free. The Pb-free JEDEC designator (e3)

can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

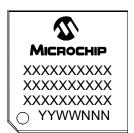
40-Lead PDIP



Example



44-Lead TQFP



Example



44-Lead QFN



Example

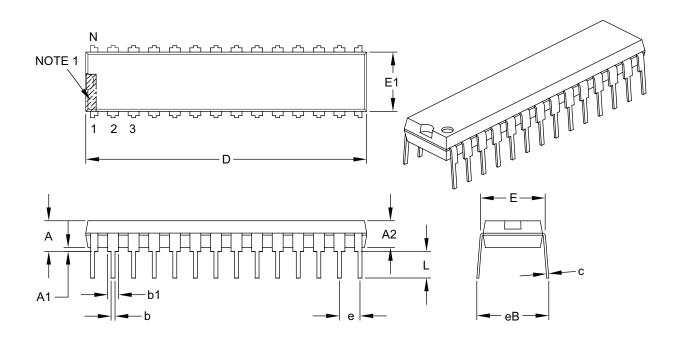


22.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		
Dimens	sion Limits	MIN	NOM	MAX	
Number of Pins	N		28		
Pitch	е		.100 BSC		
Top to Seating Plane	Α	200			
Molded Package Thickness	A2	.120	.135	.150	
Base to Seating Plane	A1	.015	-	_	
Shoulder to Shoulder Width	Е	.290	.310	.335	
Molded Package Width	E1	.240	.285	.295	
Overall Length	D	1.345	1.365	1.400	
Tip to Seating Plane	L	.110	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.040	.050	.070	
Lower Lead Width	b	.014 .018 .022			
Overall Row Spacing §	eB	_	_	.430	

Notes:

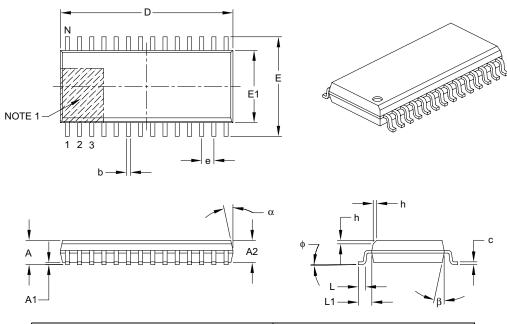
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3	
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N		28		
Pitch	е		1.27 BSC		
Overall Height	Α	2.65			
Molded Package Thickness	A2	2.05	_	_	
Standoff §	A1	0.10	_	0.30	
Overall Width	E	10.30 BSC			
Molded Package Width	E1		7.50 BSC		
Overall Length	D		17.90 BSC		
Chamfer (optional)	h	0.25	-	0.75	
Foot Length	L	0.40	_	1.27	
Footprint	L1		1.40 REF		
Foot Angle Top	ф	0°	_	8°	
Lead Thickness	С	0.18	_	0.33	
Lead Width	b	0.31 – 0.51			
Mold Draft Angle Top	α	5° – 15°			
Mold Draft Angle Bottom	β	5°	_	15°	

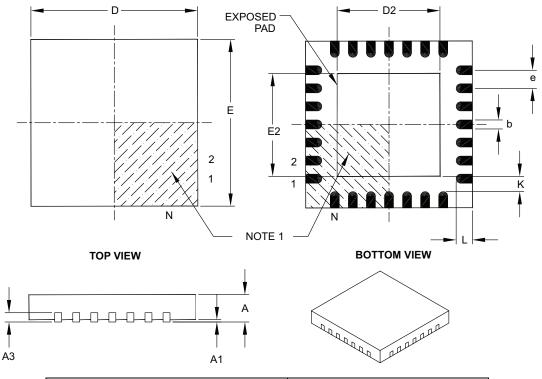
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	6
Dimens	ion Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	е		0.65 BSC	
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	Е		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

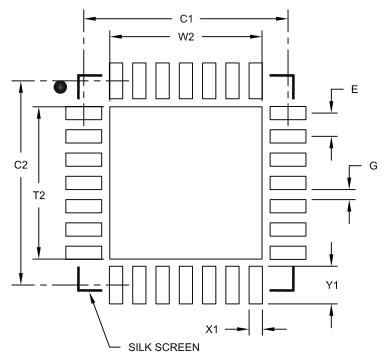
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units			MILLIM	ETERS
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

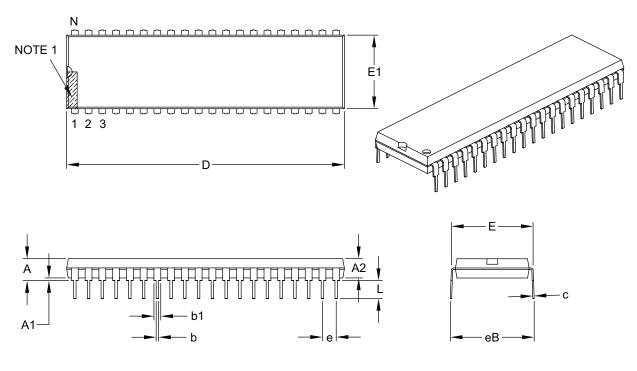
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

40-Lead Plastic Dual In-Line (P) - 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		40	
Pitch	е		.100 BSC	
Top to Seating Plane	A	_	_	.250
Molded Package Thickness	A2	.125	_	.195
Base to Seating Plane	A1	.015	_	_
Shoulder to Shoulder Width	E	.590	_	.625
Molded Package Width	E1	.485	_	.580
Overall Length	D	1.980	_	2.095
Tip to Seating Plane	L	.115	_	.200
Lead Thickness	С	.008	_	.015
Upper Lead Width	b1	.030	_	.070
Lower Lead Width	b	.014	_	.023
Overall Row Spacing §	eB	_	_	.700

Notes:

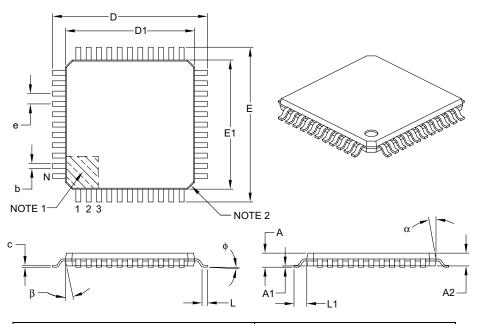
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3
Dime	nsion Limits	MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	е		0.80 BSC	
Overall Height	Α	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	_	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ф	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	С	0.09	_	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

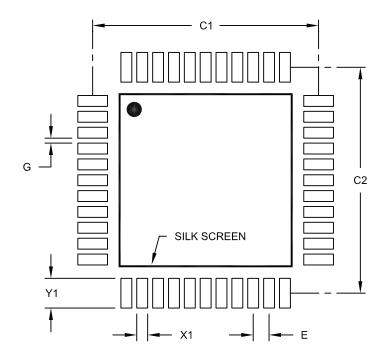
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1 mm Body, 2.00 mm [TQFP]

ote: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIM	ETERS	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

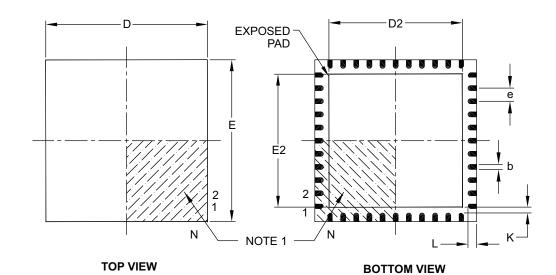
1. Dimensioning and tolerancing per ASME Y14.5M

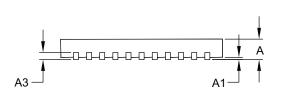
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

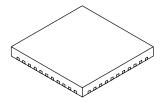
Microchip Technology Drawing No. C04-2076A

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Units		MILLIMETERS	3
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		44	
Pitch	е		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

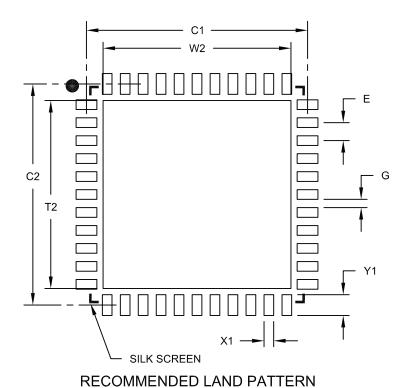
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units **MILLIMETERS** MIN NOM **Dimension Limits** MAX Contact Pitch Е 0.65 BSC Optional Center Pad Width W2 6.80 Optional Center Pad Length 6.80 T2 Contact Pad Spacing C1 8.00 Contact Pad Spacing C2 8.00 Contact Pad Width (X44) 0.35 Χ1 Contact Pad Length (X44) 0.80 Υ1 0.25 Distance Between Pads G

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2006)

Original data sheet for PIC18F2450/4450 devices.

Revision B (January 2007)

Example 11-1 and Figure 14-1 have been updated, Section 14.5.1.1 "Bus Activity Detect Interrupt Bit (ACTVIF)" and Section 14.2.2.3 "Internal Pull-up Resistors" have been added, the Electrical Specifications in Section 21.0 "Electrical Characteristics" have been updated, the package diagrams in Section 22.2 "Package Details" have been updated and there have been minor corrections to the data sheet text.

Revision C (August 2007)

The Electrical Specifications in Section 21.2 "DC Characteristics: Power-Down and Supply Current" have been updated and the package diagrams in Section 22.2 "Package Details" have been updated.

Revision D (March 2008)

Minor edits to Section 14.0 "Universal Serial Bus (USB)", Section 16.0 "10-Bit Analog-to-Digital Converter (A/D) Module", Section 18.0 "Special Features of the CPU" and Section 21.0 "Electrical Characteristics".

APPENDIX B: DEVICE

DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F2450	PIC18F4450
Program Memory (Bytes)	16384	16384
Program Memory (Instructions)	8192	8192
Interrupt Sources	13	13
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, D, E
Capture/Compare/PWM Modules	1	1
10-Bit Analog-to-Digital Module	10 Input Channels	13 Input Channels
Packages	28-Pin SPDIP 28-Pin SOIC 28-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the Mid-Range MCU devices (i.e., PIC16CXXX) and the Enhanced devices (i.e., PIC18FXXX) is provided in AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442". The changes discussed, while device specific, are generally applicable to all Mid-Range to Enhanced device migrations.

This Application Note is available as Literature Number DS00716.

APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the High-End MCU devices (i.e., PIC17CXXX) and the Enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration"*. This Application Note is available as Literature Number DS00726.

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PRODUCT IDENTIFICATION SYSTEM

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PART NO. Device	X <u>/XX</u> XXX Temperature Package Pattern Range	Examples: a) PIC18LF4450-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301. b) PIC18LF2450-I/SO = Industrial temp., SOIC
Device	PIC18F2450 ⁽¹⁾ , PIC18F4450 ⁽¹⁾ , PIC18F2450T ⁽²⁾ , PIC18F4450T ⁽²⁾ ; VDD range 4.2V to 5.5V PIC18LF2450 ⁽¹⁾ , PIC18LF4450 ⁽¹⁾ , PIC18LF2450T ⁽²⁾ , PIC18LF4450T ⁽²⁾ ; VDD range 2.0V to 5.5V	package, Extended VDD limits. c) PIC18F4450-I/P = Industrial temp., PDIP package, normal VDD limits.
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny Plastic DIP P = PDIP ML = QFN	Note 1: F = Standard Voltage Range LF = Wide Voltage Range 2: T = in tape and reel TQFP packages only.
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	



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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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