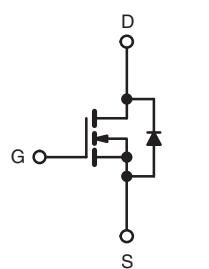
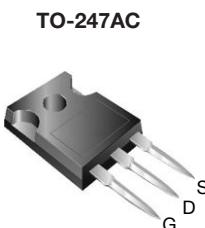


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	600
R _{DSON} (Ω)	V _{GS} = 10 V 0.27
Q _g (Max.) (nC)	150
Q _{gs} (nC)	46
Q _{gd} (nC)	64
Configuration	Single



N-Channel MOSFET



FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simple Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION

Package	TO-247AC		
Lead (Pb)-free	IRFP21N60LPbF SiHFP21N60L-E3		
SnPb	IRFP21N60L SiHFP21N60L		

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D
		T _C = 100 °C	21
Pulsed Drain Current ^a	I _{DM}	13	A
Linear Derating Factor		84	
Single Pulse Avalanche Energy ^b	E _{AS}	2.6	W/°C
Repetitive Avalanche Current ^a	I _{AR}	420	mJ
Repetitive Avalanche Energy ^a	E _{AR}	21	A
Maximum Power Dissipation	P _D	33	mJ
Peak Diode Recovery dV/dt ^c	dV/dt	330	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	Ibf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 1.9 mH, R_g = 25 Ω, I_{AS} = 21 A, dV/dt = 11 V/ns (see fig. 12a).
- I_{SD} ≤ 21 A, dI/dt ≤ 530 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.38	

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

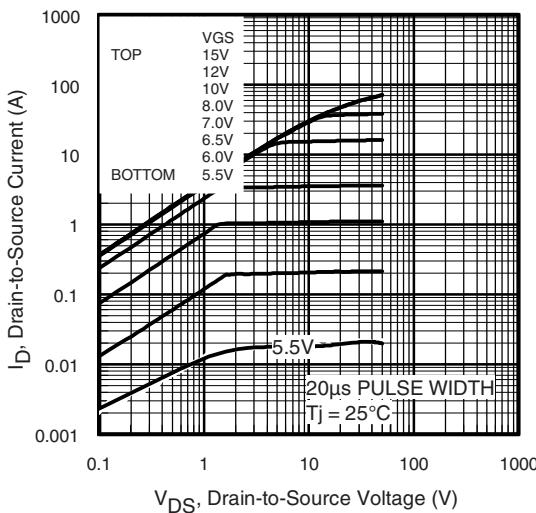
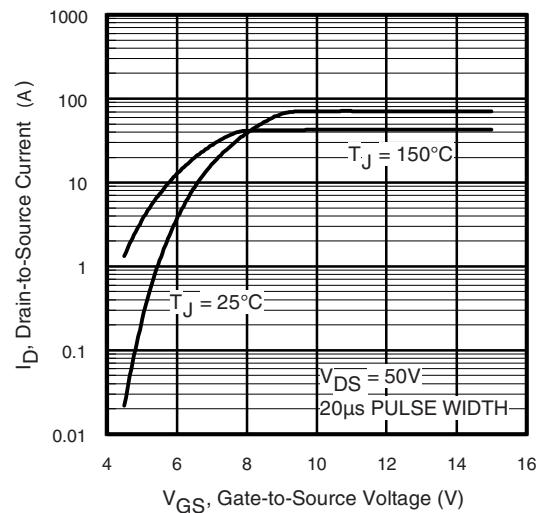
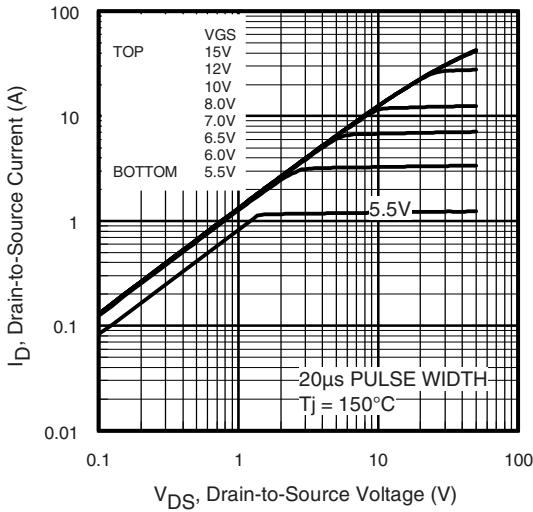
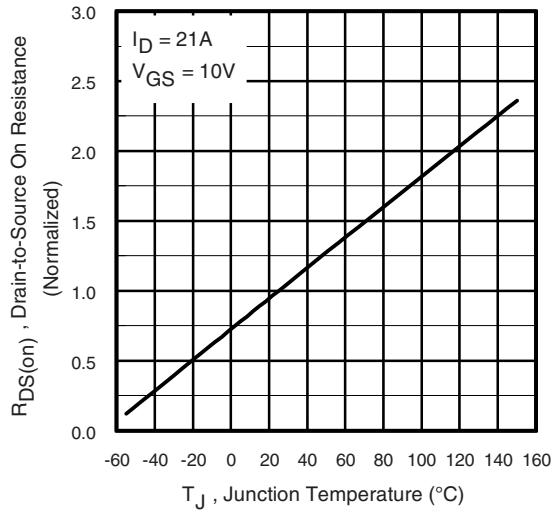
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$	$I_D = 250 \mu\text{A}$	600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	420	-	mV/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		3.0	-	5.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	50	μA	
		$V_{DS} = 480 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$		-	-	2.0	mA	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 13 \text{ A}^b$	-	0.27	0.32	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 13 \text{ A}$		11	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	4000	-	pF	
Output Capacitance	C_{oss}			-	340	-		
Reverse Transfer Capacitance	C_{rss}			-	29	-		
Effective Output Capacitance	$C_{oss} \text{ eff.}$	$V_{GS} = 0 \text{ V}$, $V_{DS} = 0 \text{ V to } 480 \text{ V}^c$		-	170	-		
Effective Output Capacitance (Energy Related)	$C_{oss} \text{ eff. (ER)}$			-	130	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 21 \text{ A}$, $V_{DS} = 480 \text{ V}$ see fig. 7 and 15 ^b	-	-	150	nC	
Gate-Source Charge	Q_{gs}			-	-	46		
Gate-Drain Charge	Q_{gd}			-	-	64		
Gate Resistance	R_g	$f = 1 \text{ MHz}$, open drain		-	0.63	-	Ω	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300 \text{ V}$, $I_D = 21 \text{ A}$, $R_g = 1.3 \Omega$, $V_{GS} = 10 \text{ V}$, see fig. 11a and 11b ^b		-	20	-	ns	
Rise Time	t_r			-	58	-		
Turn-Off Delay Time	$t_{d(off)}$			-	33	-		
Fall Time	t_f			-	10	-		

Drain-Source Body Diode Characteristics

Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	84	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 21 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = 21 \text{ A}$		-	160	240	ns
		$T_J = 125^\circ\text{C}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	400	610	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25^\circ\text{C}$, $I_F = 21 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	480	730	nC
		$T_J = 125^\circ\text{C}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	1540	2310	
Reverse Recovery Time	I_{RRM}	$T_J = 25^\circ\text{C}$		-	5.3	7.9	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 C_{oss} eff. (ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

IRFP21N60L, SiHFP21N60L

Vishay Siliconix

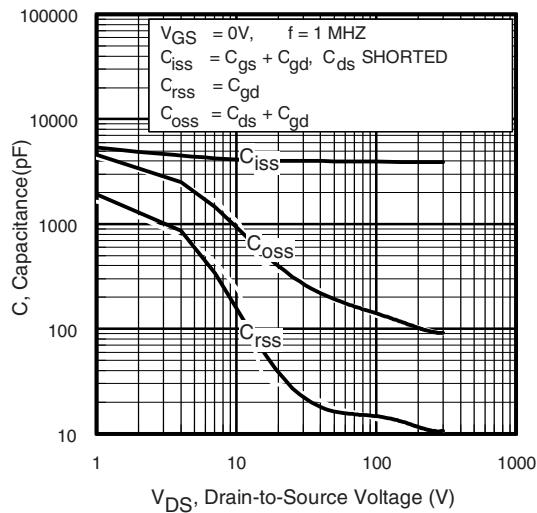


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

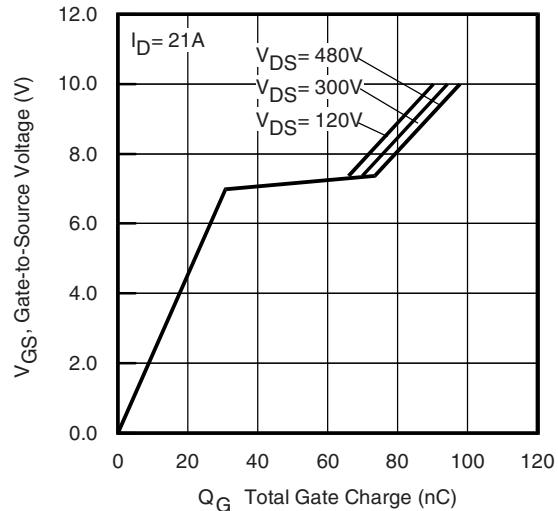


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

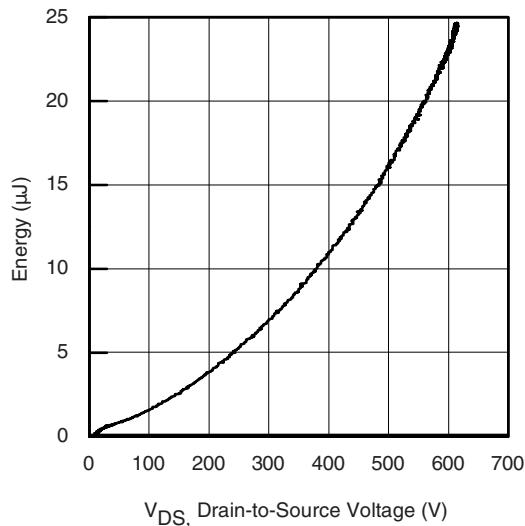


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

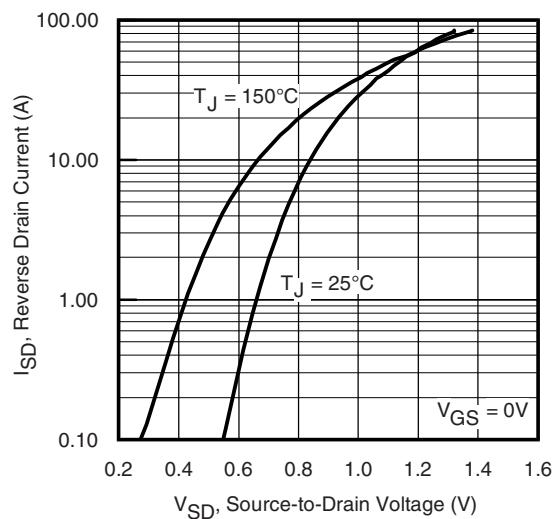
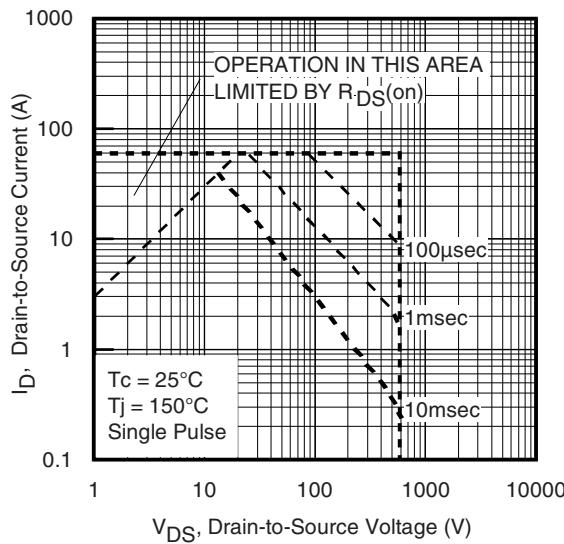
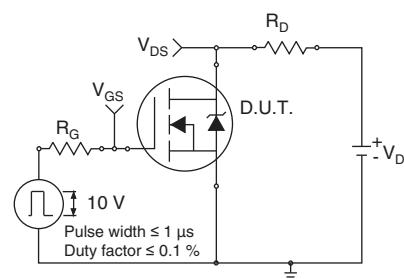
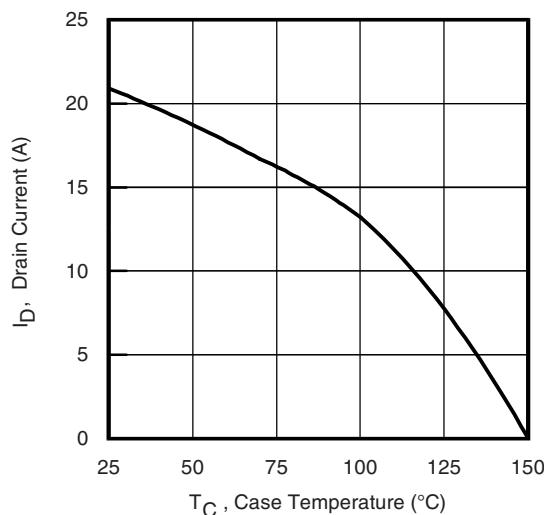
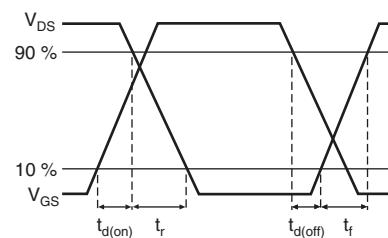
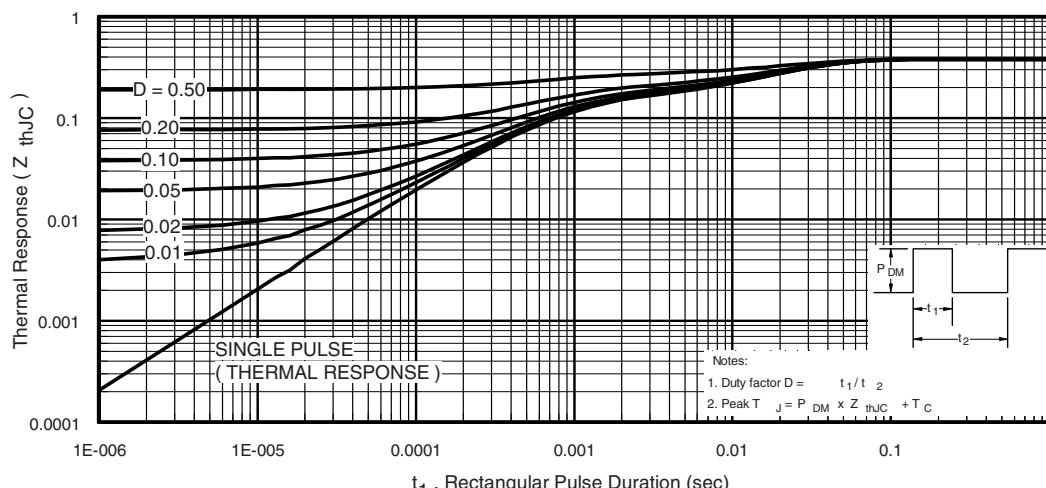


Fig. 8 - Typical Source-Drain Diode Forward Voltage


Fig. 9 - Maximum Safe Operating Area

Fig. 11a - Switching Time Test Circuit

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 11b - Switching Time Waveforms

Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFP21N60L, SiHFP21N60L

Vishay Siliconix

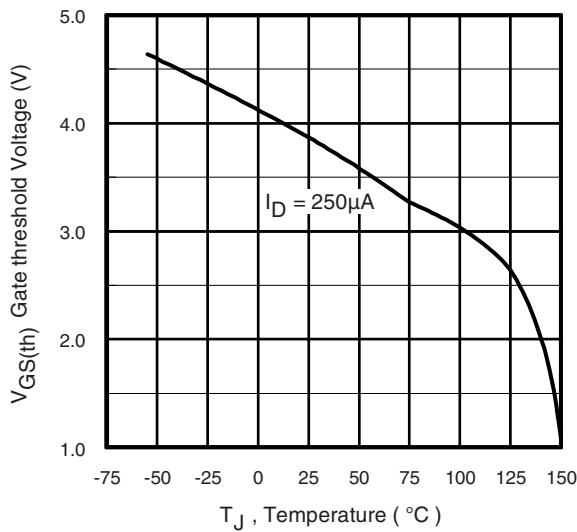


Fig. 13 - Threshold Voltage vs. Temperature

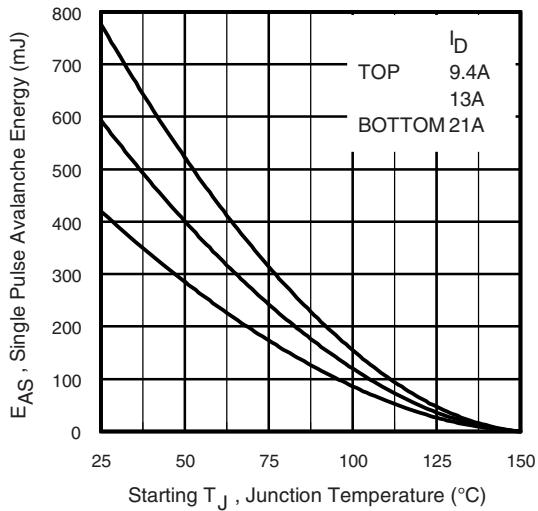


Fig. 14a - Maximum Avalanche Energy vs. Drain Current

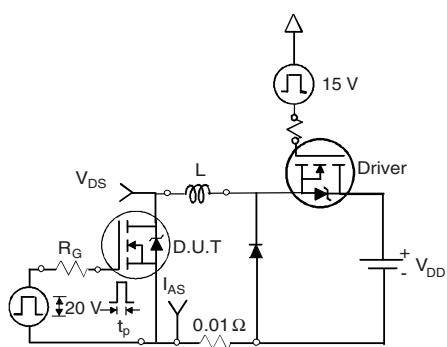


Fig. 14b - Unclamped Inductive Test Circuit

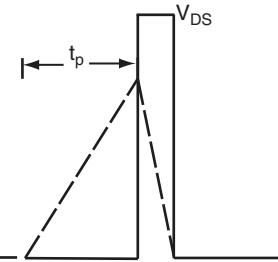


Fig. 14c - Unclamped Inductive Waveforms

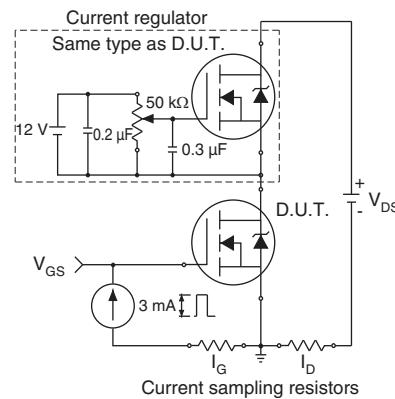


Fig. 15a - Gate Charge Test Circuit

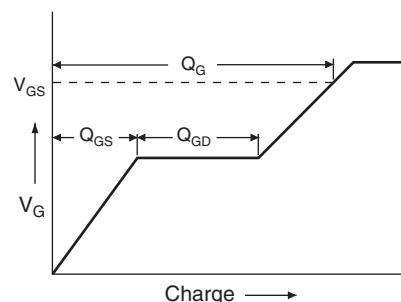
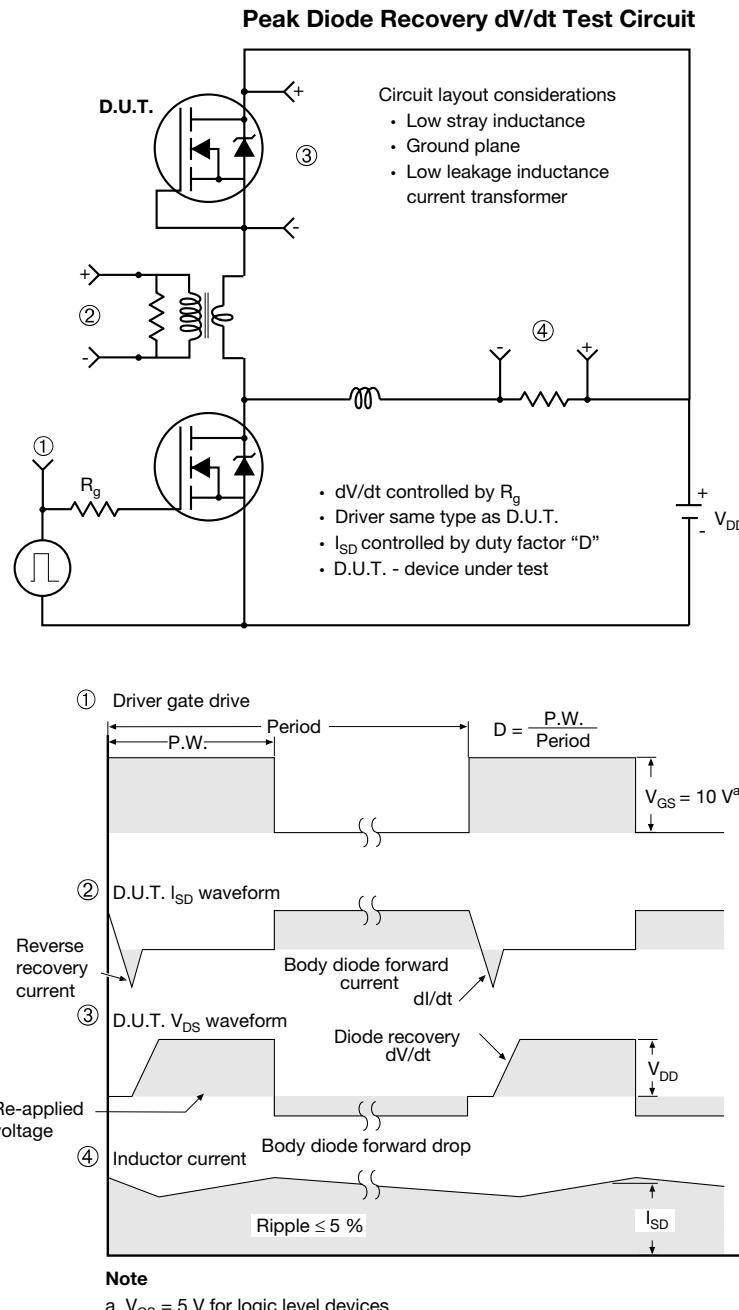
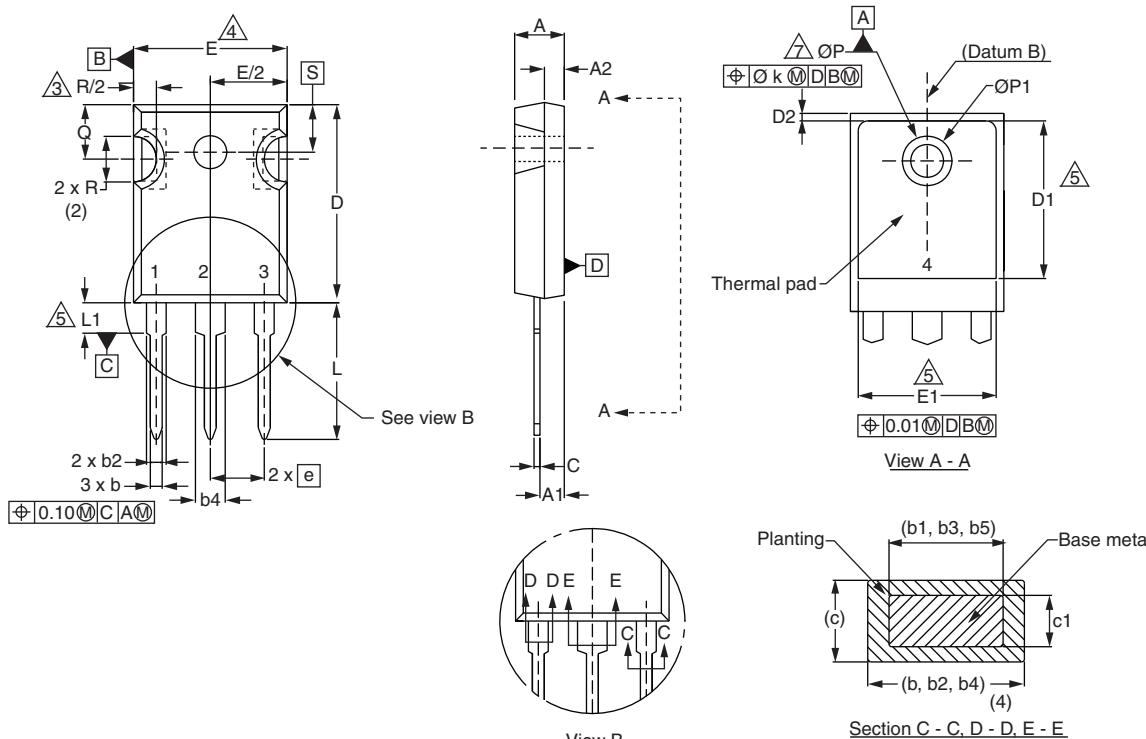


Fig. 15b - Basic Gate Charge Waveform


Fig. 16 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91206.

TO-247AC (High Voltage)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

ECN: X13-0045-Rev. C, 18-Mar-13
 DWG: 5971

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Contour of slot optional.
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- Thermal pad contour optional with dimensions D1 and E1.
- Lead finish uncontrolled in L1.
- Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- Xian and Mingxin actually photo.





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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помошь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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