

CMOS Analog Switches

DESCRIPTION

The DG300B, DG303B family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

Designed on the Vishay Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

Featuring low power consumption (3.5 mW typ.) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V- rail to 0 V.

FEATURES

- Analog signal range: ± 15 V
- Fast switching - t_{ON} : 150 ns
- Low on-resistance - $R_{DS(on)}$: 30 Ω
- Single supply operation
- Latch-up proof
- CMOS compatible



RoHS*
COMPLIANT

BENEFITS

- Full rail-to-rail analog signal range
- Low signal error
- Low power dissipation

APPLICATIONS

- Low level switching circuits
- Programmable gain amplifiers
- Portable and battery powered systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

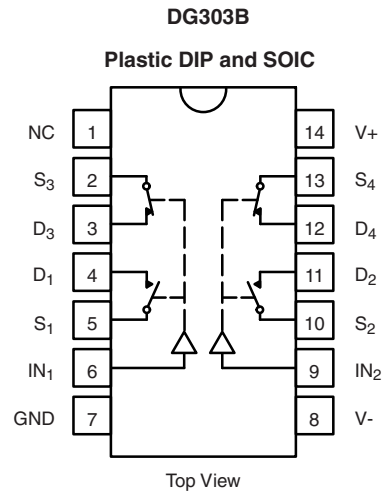
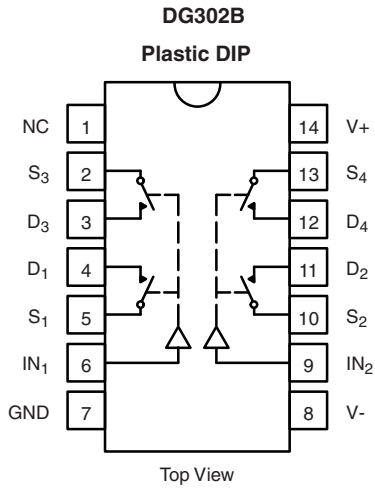
Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

TRUTH TABLE		
Logic	SW ₁	SW ₂
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

TRUTH TABLE		
Logic	SW ₁ , SW ₂	SW ₃ , SW ₄
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

ORDERING INFORMATION			
Temp. Range	Standard Package	Standard Part Number	Lead (Pb)-free Part Number
- 40 °C to 85 °C	14-Pin Plastic DIP	DG300BDJ	DG300BDJ-E3
		DG301BDJ	DG301BDJ-E3
		DG302BDJ	DG302BDJ-E3
		DG303BDJ	DG303BDJ-E3
	14-SOIC	DG303BDY	DG303BDY-T1 DG303BDY-E3 DG303BDY-T1-E3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)			
Parameter	Limit	Unit	
Voltages Referenced V_+ to V_-	44	V	
GND	25		
Digital Inputs ^a , V_S , V_D	$(V_-) - 2$ to $(V_+) + 2$ or 30 mA, whichever occurs first		
Current (Any Terminal)	30	mA	
Continuous Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)	100		
Storage Temperature	- 65 to 150	$^\circ\text{C}$	
Power Dissipation (Package) ^b	14-Pin PlasticDIP ^c	470	mW
	SOIC-14 ^d	600	

Notes:

- a. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.5 mW/ $^\circ\text{C}$ above 25 $^\circ\text{C}$
- d. Derate 7.6 mW/ $^\circ\text{C}$ above 75 $^\circ\text{C}$.

SCHEMATIC DIAGRAM (Typical Channel)

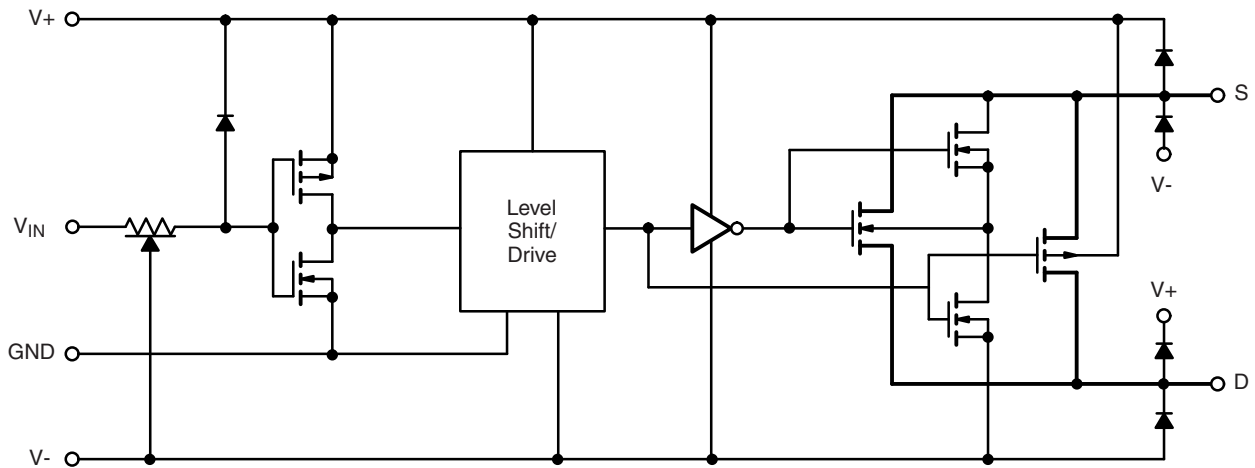


Figure 1.

SPECIFICATIONS ^a							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = -15 V V _{IN} = 0.8 V or V _{IN} = 4 V ^f	Temp. ^b	Limits -40 °C to 85 °C			Unit
				Min. ^d	Typ. ^c	Max. ^d	
Analog Switch							
Analog Signal Range ^e	V _{ANALOG}		Full	-15		15	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = ±10 V, I _S = -10 mA	Room Full		30	50 75	Ω
Source Off Leakage Current	I _{S(off)}	V _S = ±14 V, V _D = ±14 V	Room Hot	-5 -100	±0.1	5 100	nA
Drain Off Leakage Current	I _{D(off)}		Room Hot	-5 -100	±0.1	5 100	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ±14 V	Room Hot	-5 -100	±0.1	5 100	
Digital Control							
Input Current with Input Voltage High	I _{INH}	V _{IN} = 5 V	Room Full	-1	-0.001		μA
		V _{IN} = 15 V	Room Full		0.001	1	
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0 V	Room Full	-1	-0.001		
Dynamic Characteristics							
Turn-On Time	t _{ON}	see figure 2	Room			150	ns
Turn-Off Time	t _{OFF}		Room			130	
Break-Before-Make Time	t _{OPEN}	DG301B, DG303B Only figure 3	Room			50	
Charge Injection	Q	C _L = 1 nF, R _{gen} = 0 Ω, V _{gen} = 0 V figure 4	Room			8	pC
Source Off Capacitance	C _{S(off)}	V _S , V _D = 0 V, f = 1 MHz	Room			14	pF
Drain Off Capacitance	C _{D(off)}		Room			14	
Channel-On Capacitance	C _{D(on)}		Room			40	
Input Capacitance	C _{in}	f = 1 MHz	V _{IN} = 0 V	Room		6	
			V _{IN} = 15 V	Room		7	
Off Isolation	OIRR	V _{IN} = 0 V, R _L = 1 kΩ	Room			62	dB
Crosstalk (Channel-to-Channel)	X _{TALK}	V _S = 1 V _{rms} , f = 500 kHz	Room			74	
Power Supplies							
Positive Supply Current	I ₊	V _{IN} = 4 V (one input) all others = 0 V	Room Full			0.23 1	mA
Negative Supply Current	I ₋		Room Full	-100	-0.001		
Positive Supply Current	I ₊	V _{IN} = 0.8 V (all inputs)	Room Full			0.001 100	μA
Negative Supply Current	I ₋		Room Full	-100	-0.001		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



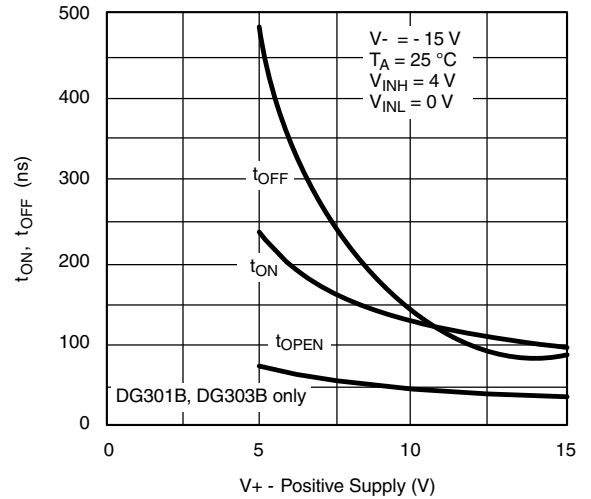
$R_{DS(on)}$ vs. V_D and Power Supply



$R_{DS(on)}$ vs. V_D and Temperature



$R_{DS(on)}$ vs. V_D and Power Supply Voltage



Switching Time and Break-Before-Make Time vs. Positive Supply Voltage



Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Positive Supply Voltage

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Supply Current vs. Temperature



Off Isolation and Crosstalk vs. Frequency



Supply Currents vs. Switching Frequency



Leakage vs. Temperature



Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature

TEST CIRCUITS



Figure 2. Switching Time



Figure 3. Break-Before-Make SPDT (DG301B, DG303B)

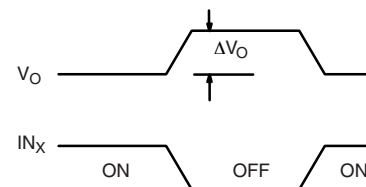


Figure 4. Charge Injection

APPLICATIONS HINTS^a

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Voltage (V)	V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V)	V _S or V _D Analog Voltage Range (V)
15	- 15	0	4/0.8	- 15 to 15
20	- 20	0	4/0.8	- 20 to 20
15	0	0	4/0.8	0 to 15

Notes:

a. Application hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

The DG300B series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are:

- 1) Increased R_{DS(on)}.
- 2) Slower switching speed. The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V. (See Input Switching Threshold vs. Positive Supply Voltage Curve.)

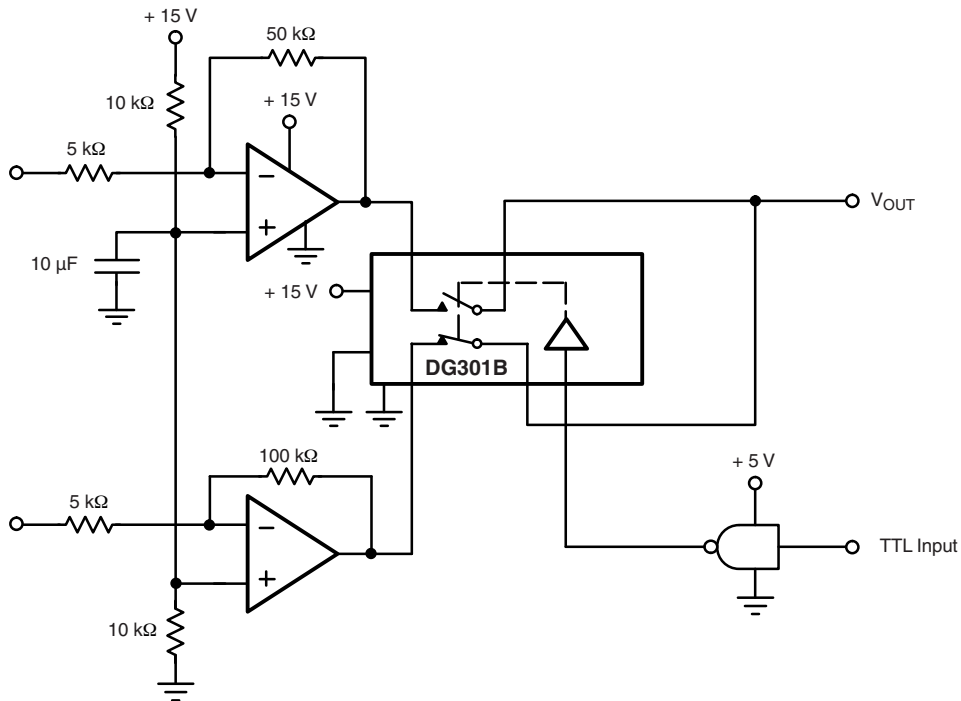


Figure 5. Single Supply Op. Amp. Switching

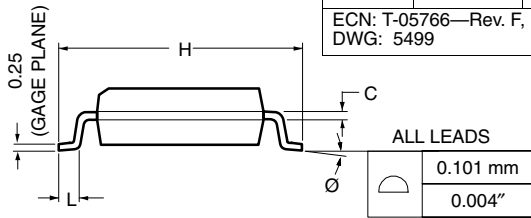
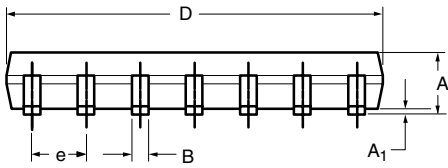
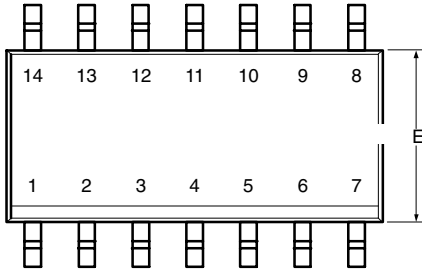
APPLICATIONS



Figure 6. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

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SOIC (NARROW): 14-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	8.55	8.75	0.336	0.344
E	3.8	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: T-05766—Rev. F, 19-Sep-05
DWG: 5499



Notice

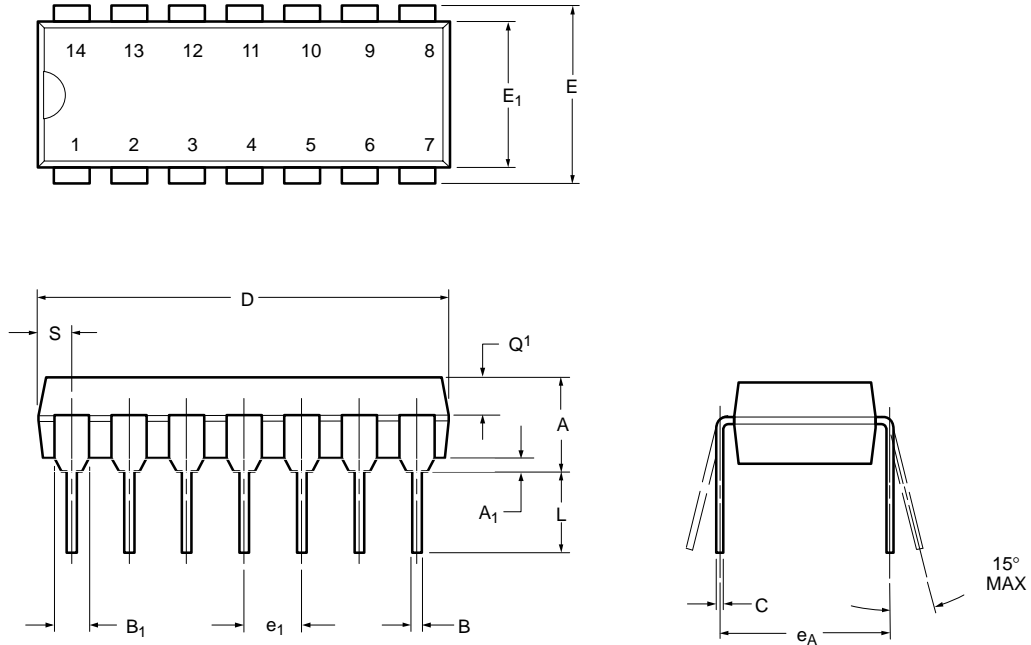
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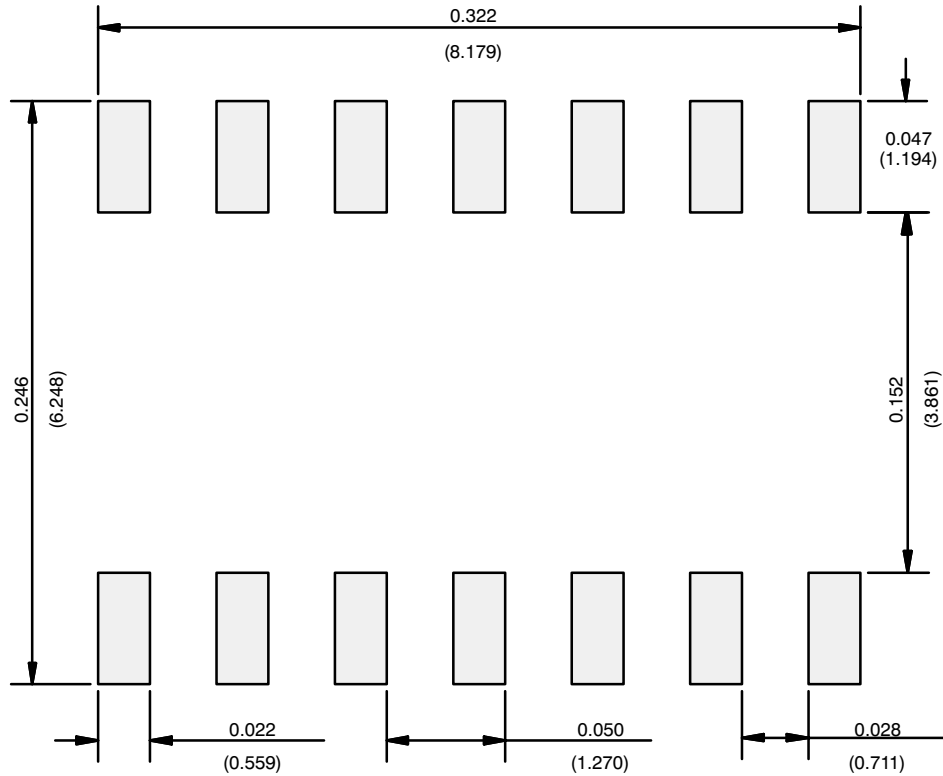
PDIP: 14-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	17.27	19.30	0.680	0.760
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	1.02	2.03	0.040	0.080

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5481

RECOMMENDED MINIMUM PADS FOR SO-14



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.