

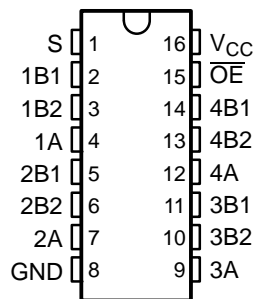
## FEATURES

- High-Bandwidth Data Path (up to 500 MHz <sup>(1)</sup>)
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance ( $r_{on}$ ) Characteristics Over Operating Range ( $r_{on} = 4\ \Omega$  Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V  $V_{CC}$
  - 0- to 3.3-V Switching With 2.5-V  $V_{CC}$
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 3.5\text{ pF}$  Typ)
- Fast Switching Frequency ( $f_{OE} = 20\text{ MHz Max}$ )

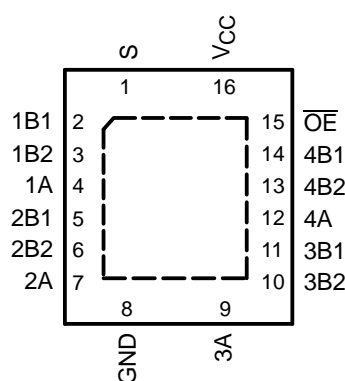
(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 0.7\text{ mA Typ}$ )
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

DBQ, DGV, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CB3Q3257RGYR	BU257
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3Q3257DBQR	BU257
	TSSOP – PW	Tape and reel	SN74CB3Q3257PWR	BU257
	TVSOP – DGV	Tape and reel	SN74CB3Q3257DGVR	BU257

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SN74CB3Q3257**  
**4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER**  
**2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH**

SCDS135A–SEPTEMBER 2003–REVISED MARCH 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The SN74CB3Q3257 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3257 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer with a single output-enable ( $\overline{OE}$ ) input. The select (S) input controls the data path of the multiplexer/demultiplexer. When  $\overline{OE}$  is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

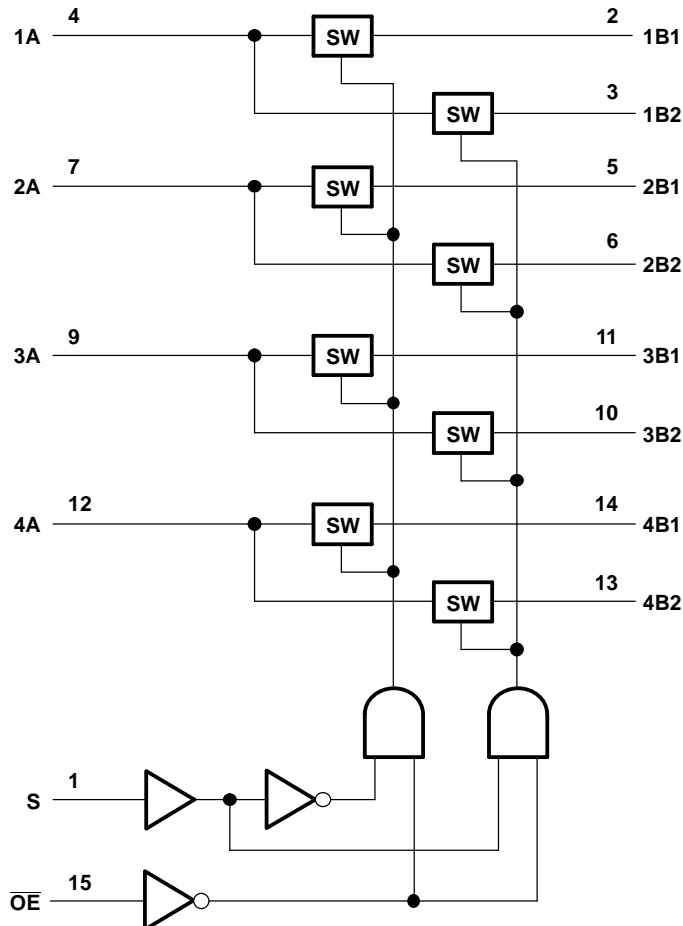
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

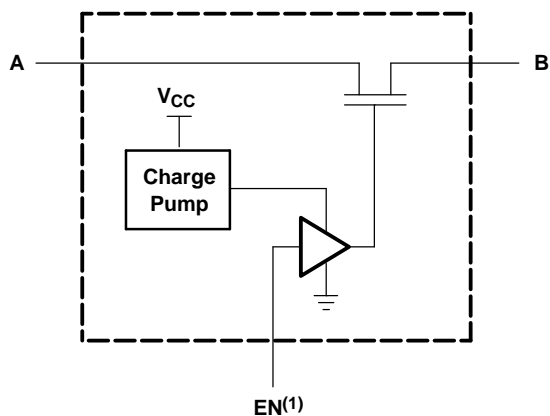
**FUNCTION TABLE**

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

### LOGIC DIAGRAM (POSITIVE LOGIC)



### SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

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## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	4.6	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	−0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	−0.5	7	V
$I_{IK}$	Control input clamp current	$V_{IN} < 0$		−50 mA
$I_{I/O}$	I/O port clamp current	$V_{I/O} < 0$		−50 mA
$I_{IO}$	ON-state switch current	±64		mA
	Continuous current through $V_{CC}$ or GND	±100		mA
$\theta_{JA}$	Package thermal impedance	D package <sup>(5)</sup>		73
		DB package <sup>(5)</sup>		82
		DBQ package <sup>(5)</sup>		90
		DGV package <sup>(5)</sup>		120
		PW package <sup>(5)</sup>		108
		RGY package <sup>(6)</sup>		39
$T_{stg}$	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.
- (6) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8
$V_{I/O}$	Data input/output voltage	0	5.5	V
$T_A$	Operating free-air temperature	−40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.6\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.8	V
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	$V_{IN} = 0\text{ to }5.5\text{ V}$			±1	μA
$I_{OZ}^{(3)}$		$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$			±1	μA
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$			1	μA
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_{IO} = 0$ , Switch ON or OFF, $V_{IN} = V_{CC}\text{ or GND}$		0.7	1.5	mA
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	One input at 3 V, Other inputs at $V_{CC}\text{ or GND}$			30	μA
$I_{CCD}^{(5)}$	Per control input	$V_{CC} = 3.6\text{ V}$ , A and B ports open, Control input switching at 50% duty cycle			0.3	0.35	mA/MHz
$C_{in}$	Control inputs	$V_{CC} = 3.3\text{ V}$ ,	$V_{IN} = 5.5\text{ V}$ , 3.3 V, or 0		2.5	3.5	pF
$C_{io(OFF)}$	A port	$V_{CC} = 3.3\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{IO} = 5.5\text{ V}$ , 3.3 V, or 0		5.5	7	pF
	B port	$V_{CC} = 3.3\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{IO} = 5.5\text{ V}$ , 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$	A port	$V_{CC} = 3.3\text{ V}$ ,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{IO} = 5.5\text{ V}$ , 3.3 V, or 0		10.5	13	pF
	B port				10.5	13	
$r_{on}^{(6)}$		$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$ , $I_O = 30\text{ mA}$		4	8	Ω
			$V_I = 1.7\text{ V}$ , $I_O = -15\text{ mA}$		4	9	
		$V_{CC} = 3\text{ V}$	$V_I = 0$ , $I_O = 30\text{ mA}$		4	6	
			$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$		4	8	

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{OE}\text{ or }f_S^{(1)}$	$\overline{OE}$ or S	A or B		10		20	MHz
$t_{pd}^{(2)}$	A or B	B or A		0.12		0.2	ns
$t_{pd(s)}$	S	A	1.5	6.5	1.5	5.5	ns
$t_{en}$	S	B	1.5	6.5	1.5	5.5	ns
	$\overline{OE}$	A or B	1.5	6.5	1.5	5.5	
$t_{dis}$	S	B	1	6	1	6	ns
	$\overline{OE}$	A or B	1	6	1	6	

(1) Maximum switching frequency for control inputs ( $V_O > V_{CC}$ ,  $V_I = 5\text{ V}$ ,  $R_L \geq 1\text{ M}\Omega$ ,  $C_L = 0$ ).

(2) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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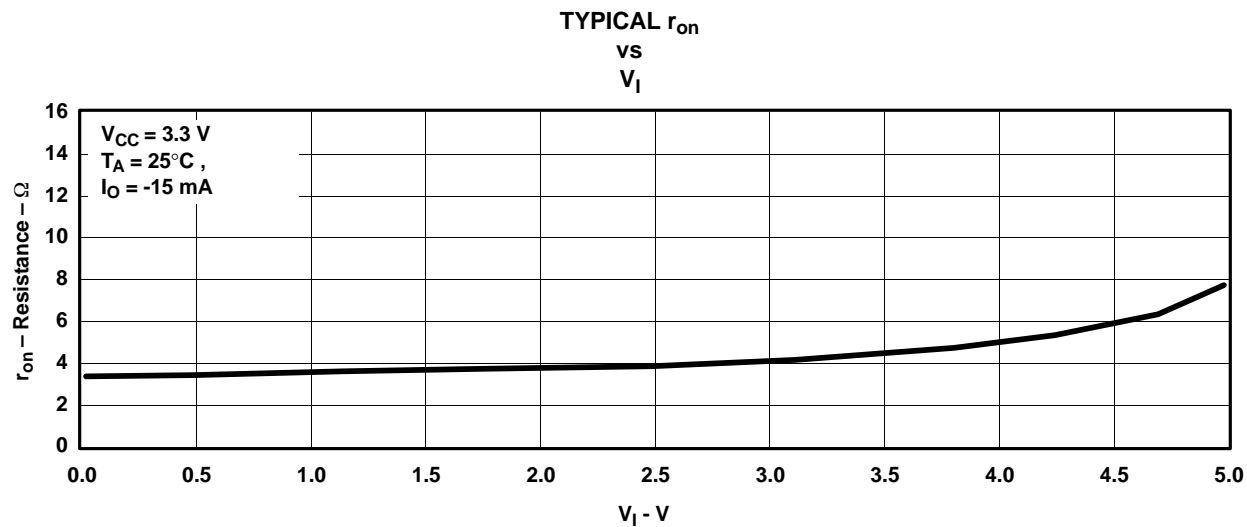


Figure 1. Typical  $r_{on}$  vs  $V_I$

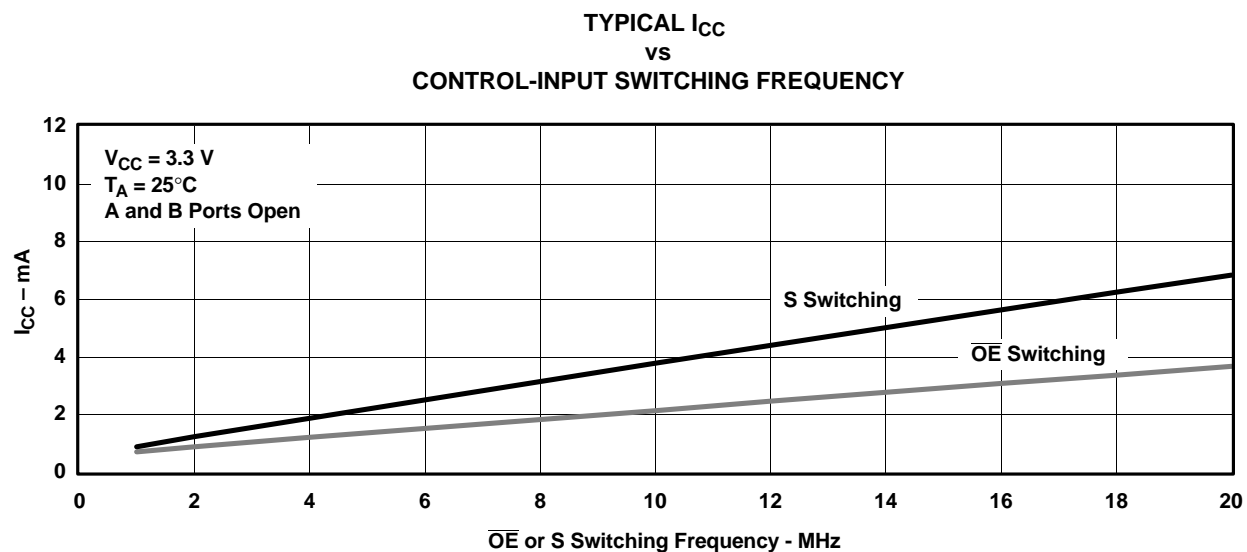
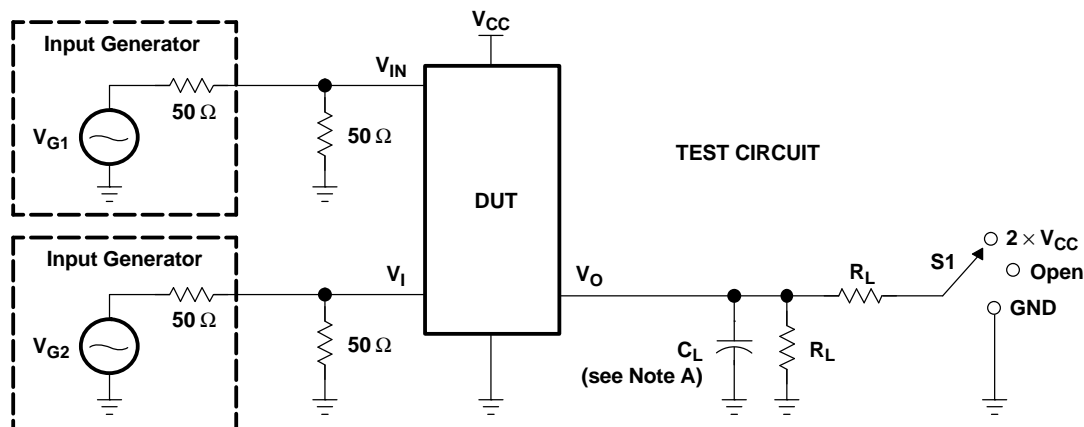
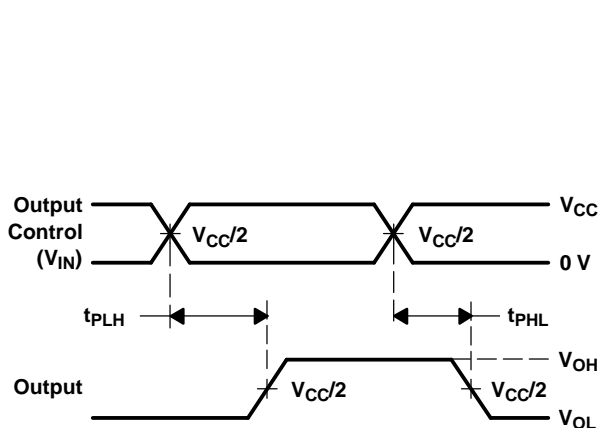


Figure 2. Typical  $I_{CC}$  vs  $\overline{OE}$  or S Switching Frequency

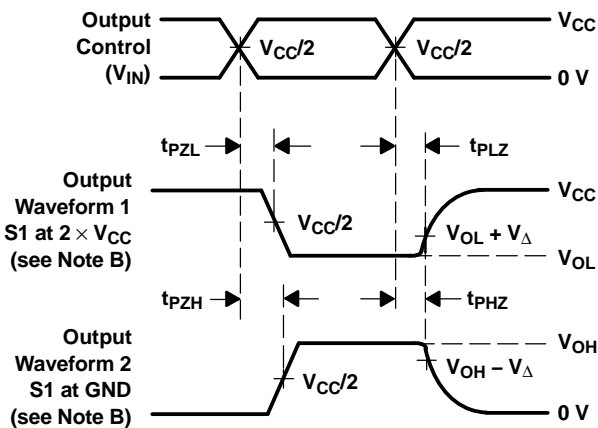
## PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	2.5 V ± 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	V <sub>CC</sub>	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74CB3Q3257DBQRE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	<a href="#">Samples</a>
74CB3Q3257DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	<a href="#">Samples</a>
74CB3Q3257DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
74CB3Q3257DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
74CB3Q3257RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	<a href="#">Samples</a>
SN74CB3Q3257RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

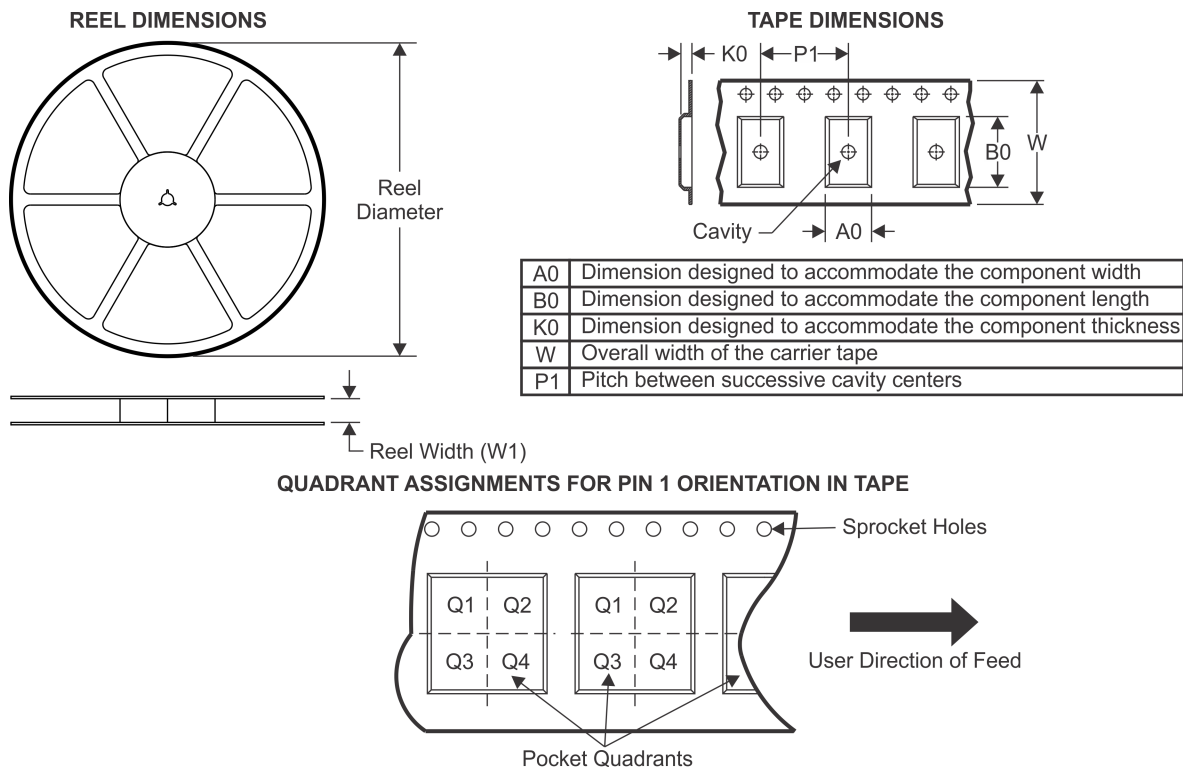
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PW RG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



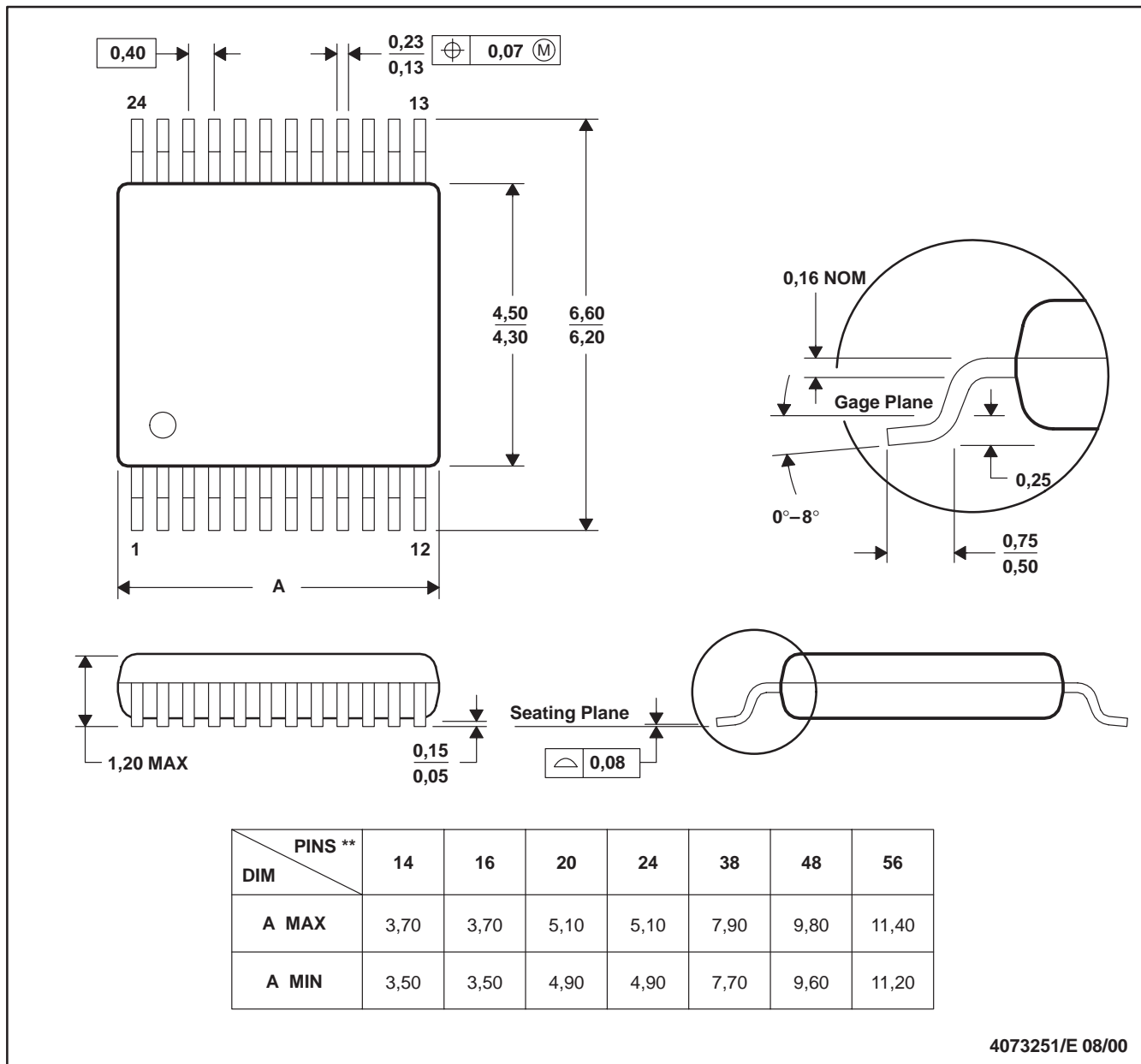
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

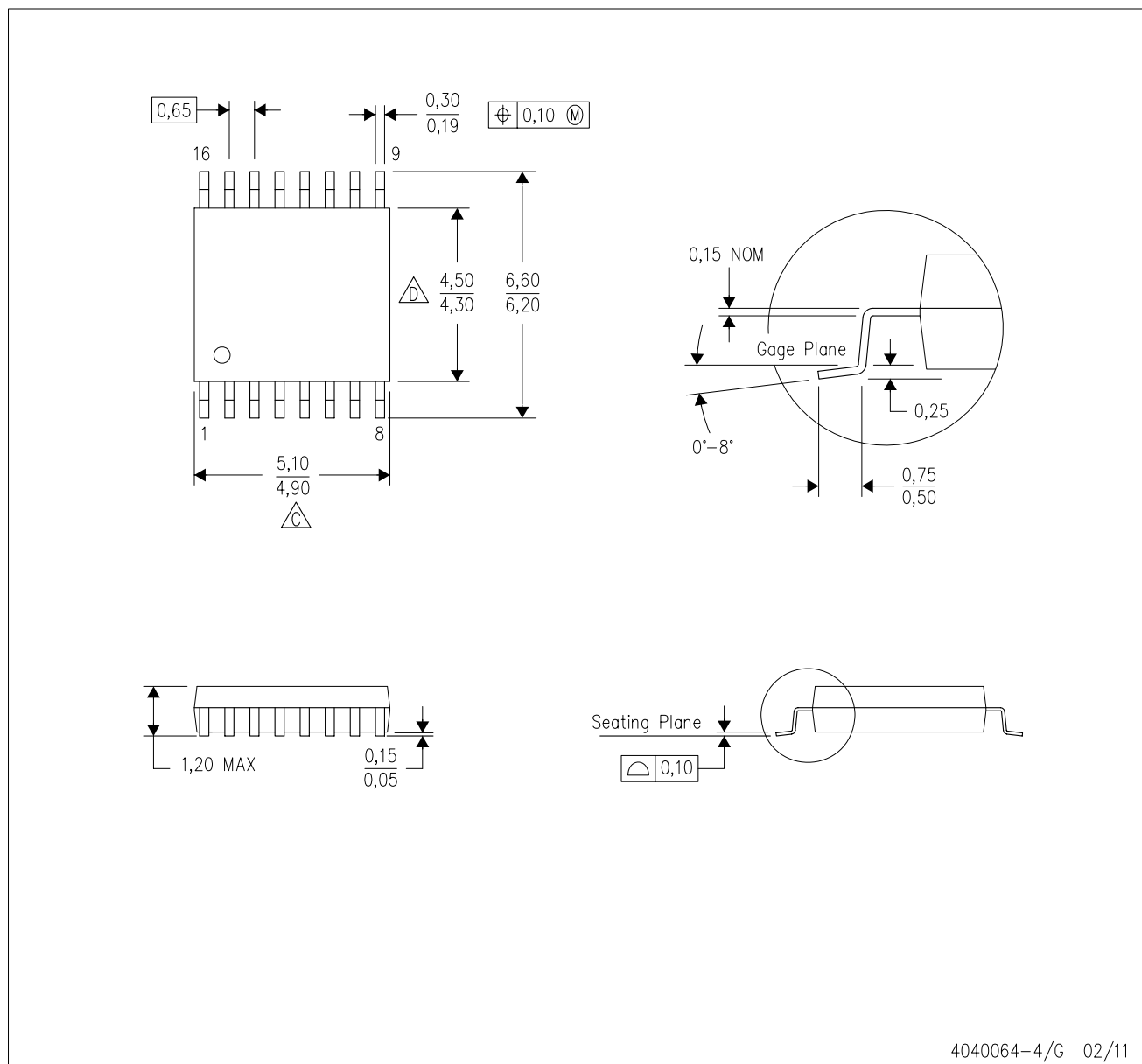
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

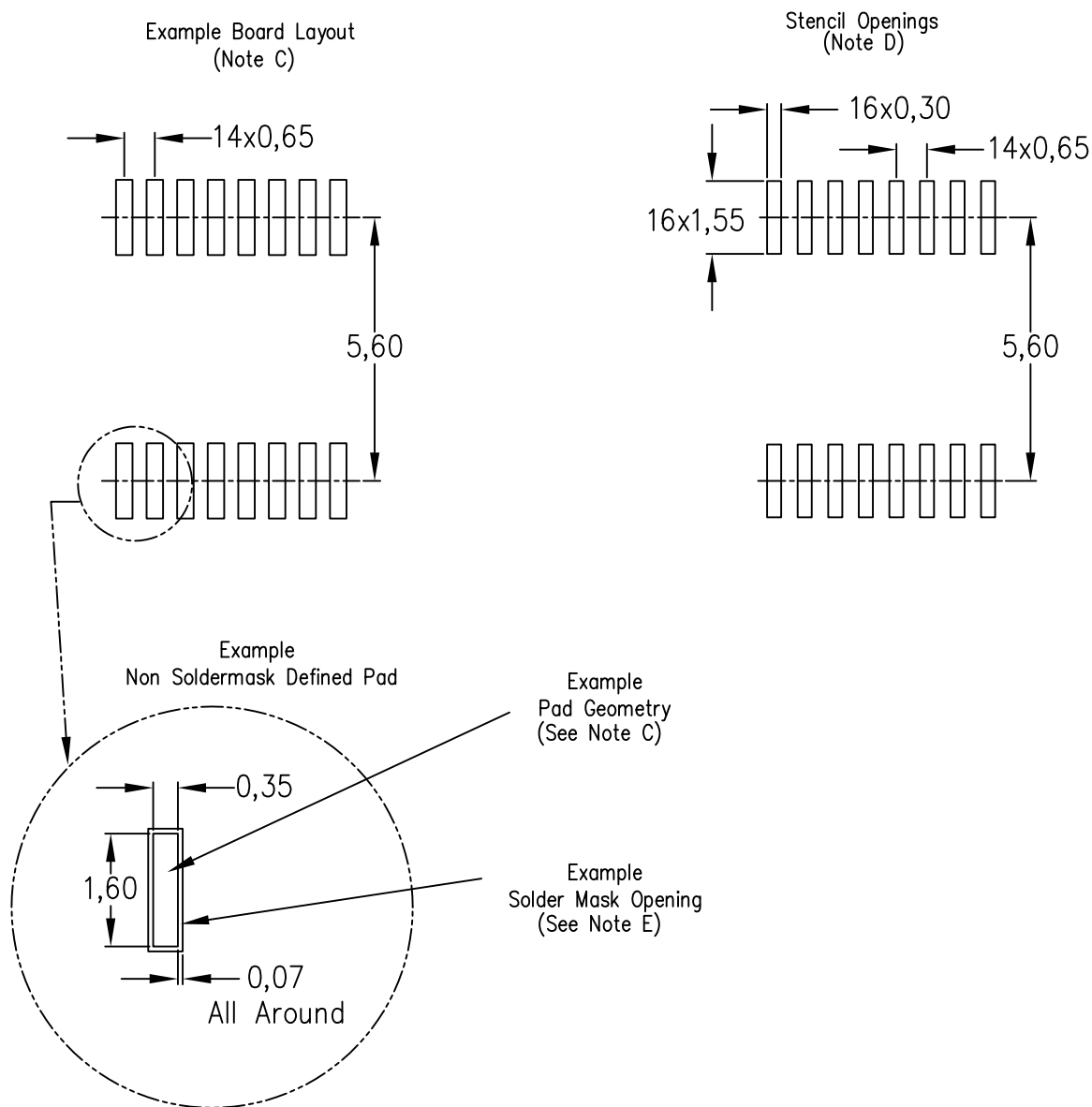


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

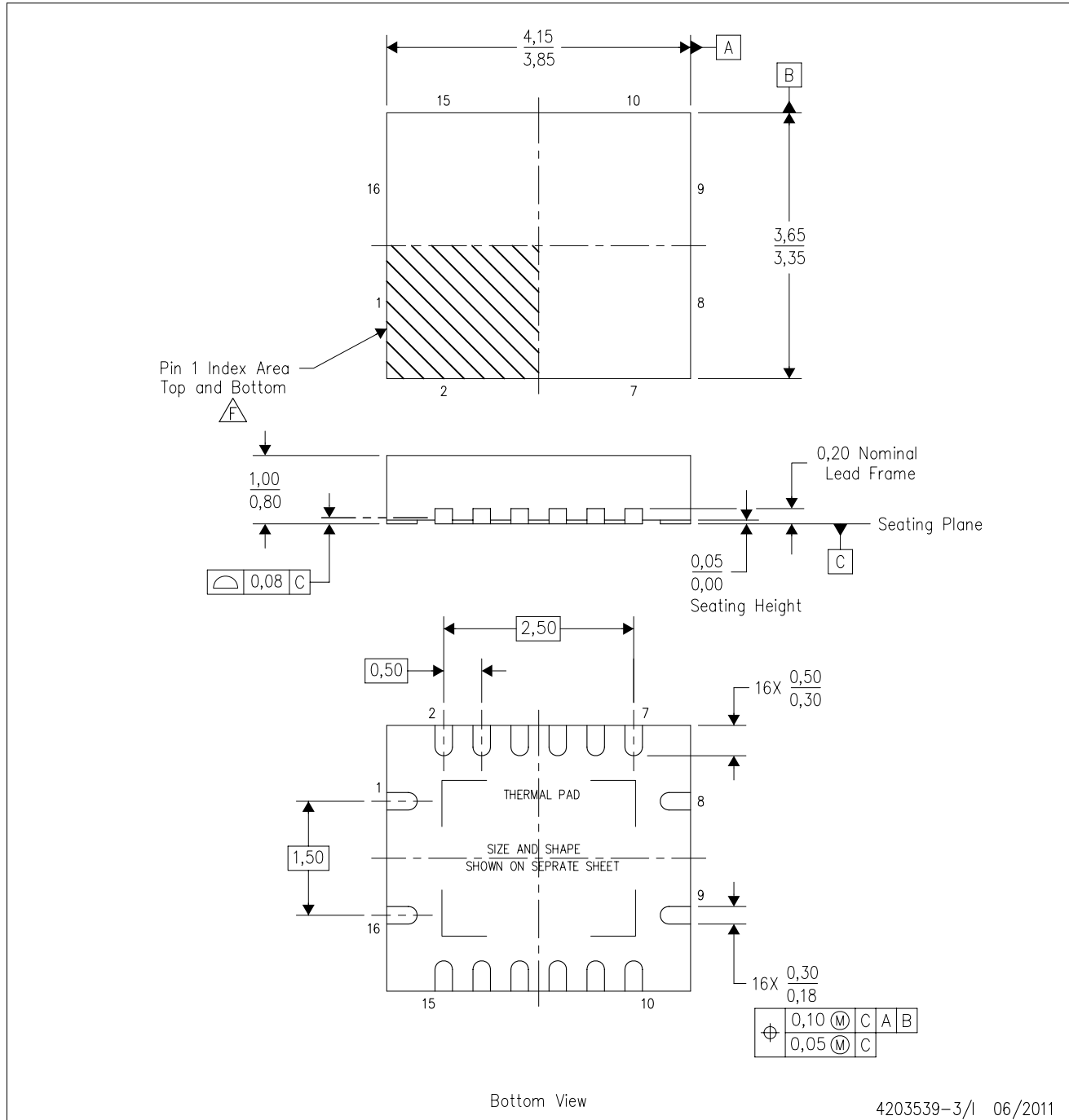


4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

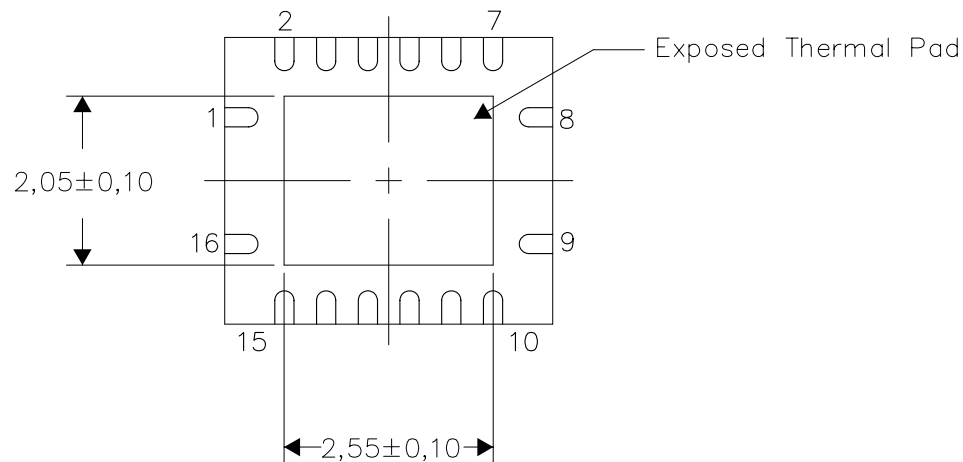
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



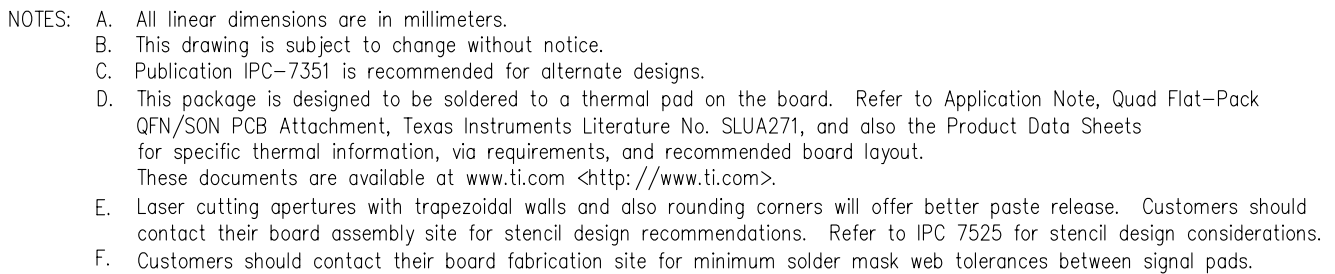
Bottom View

Exposed Thermal Pad Dimensions

4206353-3/0 11/11

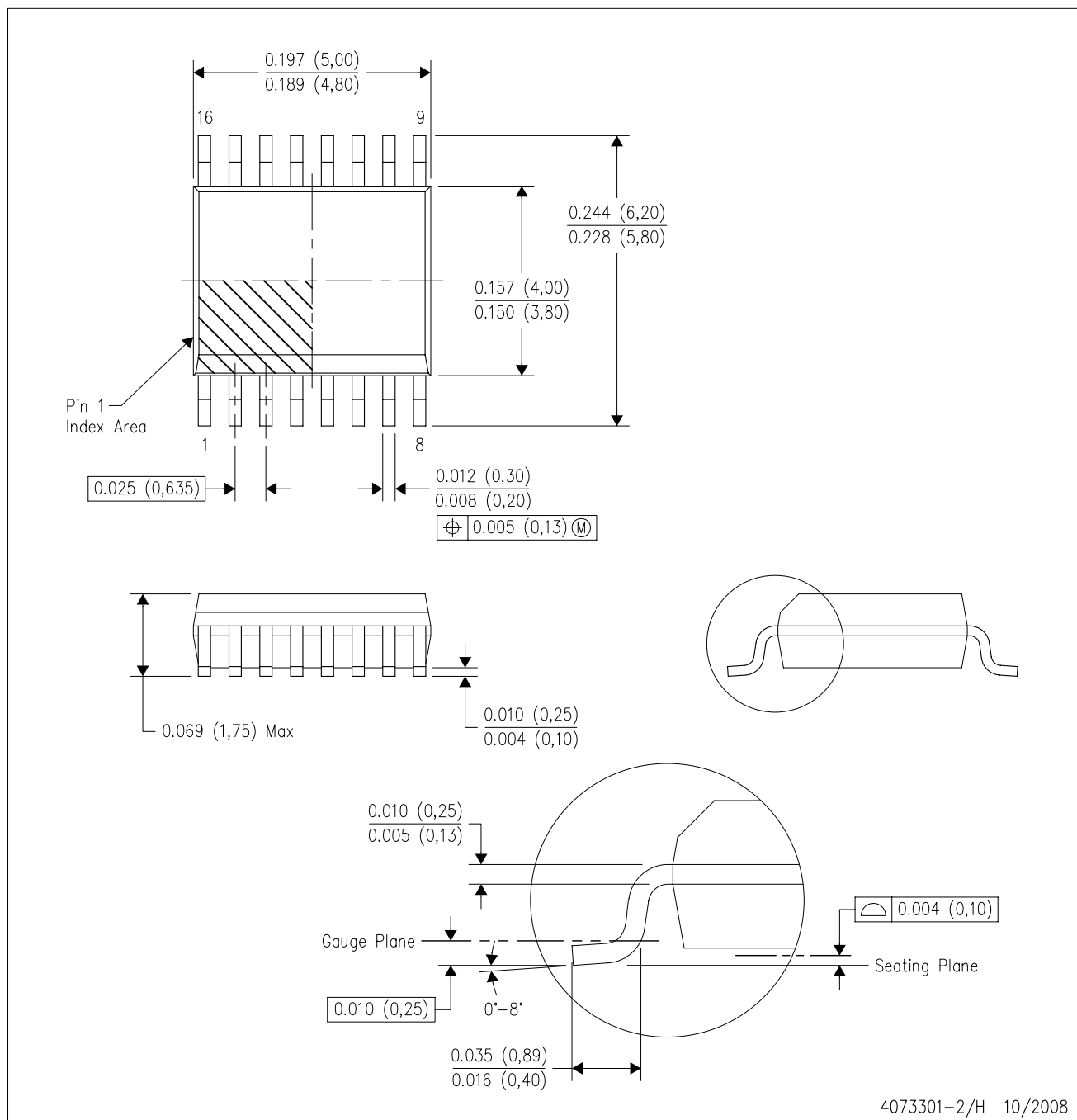
NOTE: All linear dimensions are in millimeters





DBQ (R-PDSO-G16)

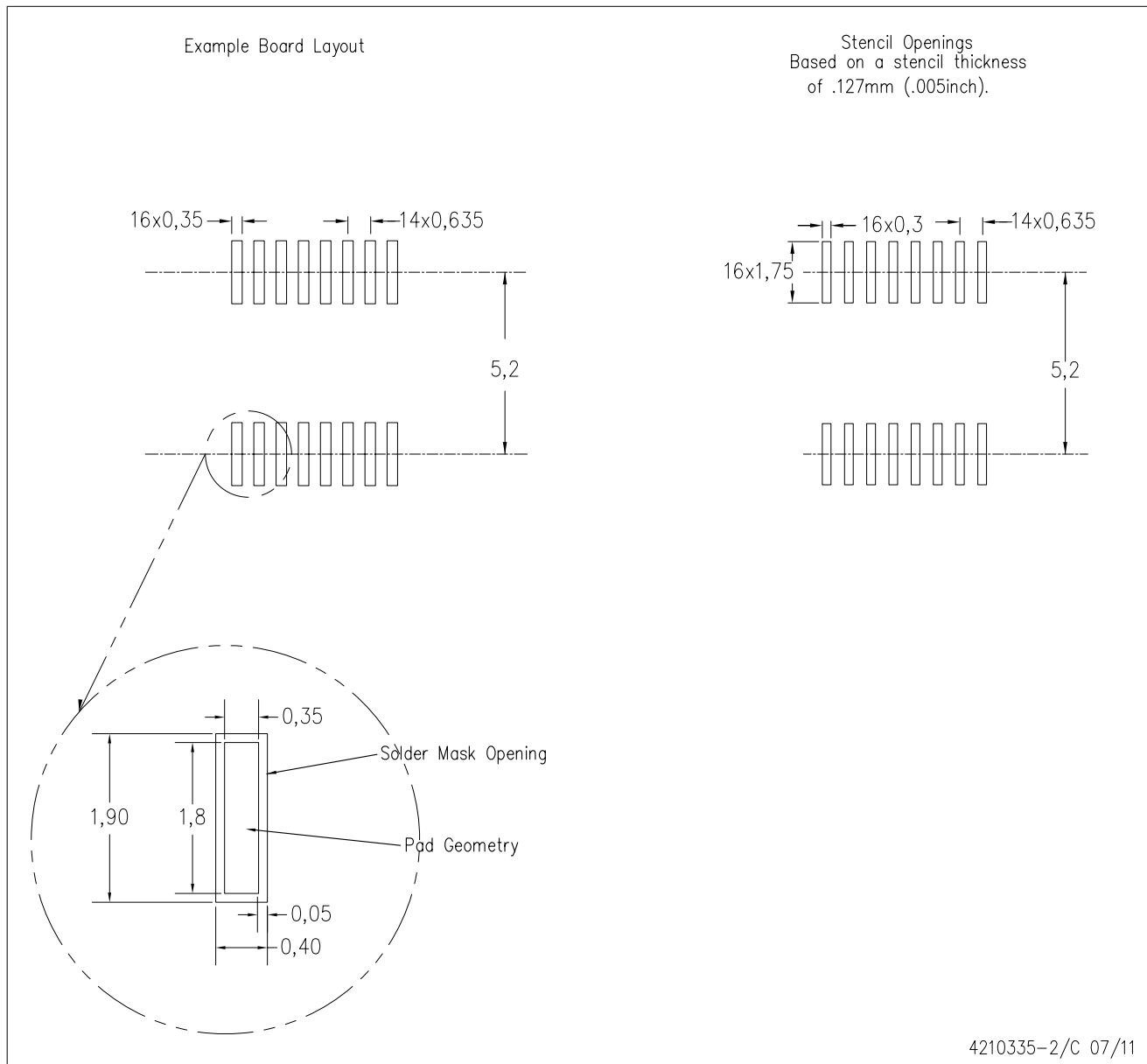
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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