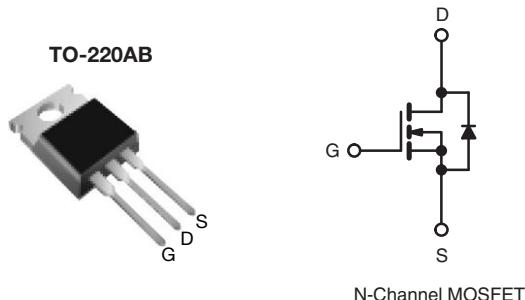


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	500	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.85
Q _g (Max.) (nC)	39	
Q _{gs} (nC)	10	
Q _{gd} (nC)	19	
Configuration	Single	



FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V V_{GS} Rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

ORDERING INFORMATION			
Package		TO-220AB	
Lead (Pb)-free		IRF840LCPbF SiHF840LC-E3	
SnPb		IRF840LC SiHF840LC	

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)			
PARAMETER		SYMBOL	LIMIT
Drain-Source Voltage		V _{DS}	500
Gate-Source Voltage		V _{GS}	± 30
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	8.0
		T _C = 100 °C	5.1
Pulsed Drain Current ^a		I _{DM}	28
Linear Derating Factor			1.0
Single Pulse Avalanche Energy ^b		E _{AS}	510 mJ
Repetitive Avalanche Current ^a		I _{AR}	8.0 A
Repetitive Avalanche Energy ^a		E _{AR}	13 mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	125 W
Peak Diode Recovery dV/dt ^c		dV/dt	3.5 V/ns
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 150 °C
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d °C
Mounting Torque	6-32 or M3 screw		10 lbf · in
			1.1 N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 50 V, starting T_J = 25 °C, L = 14 mH, R_g = 25 Ω, I_{AS} = 8.0 A (see fig. 12).
- I_{SD} ≤ 8.0 A, dI/dt ≤ 100 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE

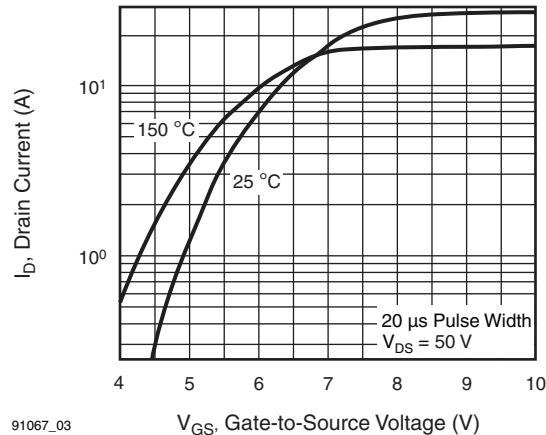
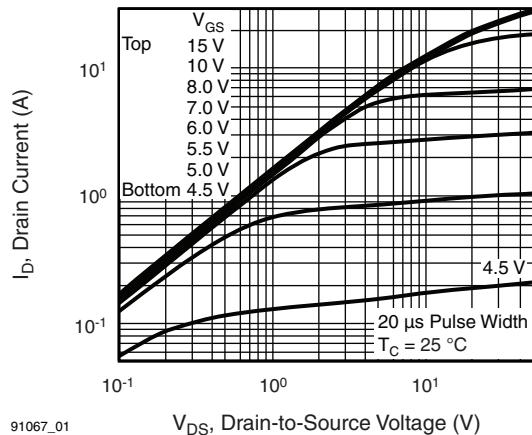
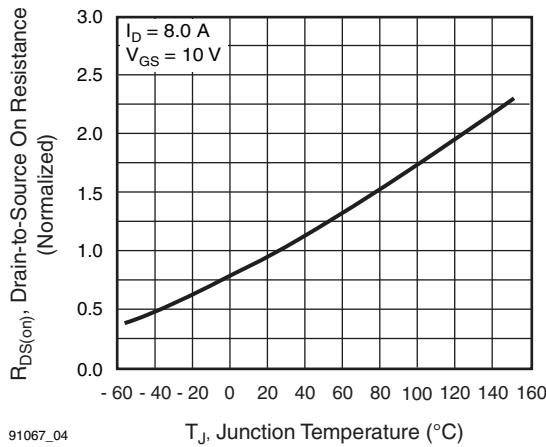
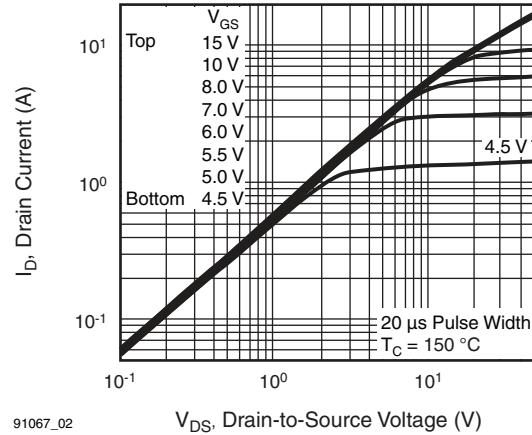
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A		500	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.63	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$ V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500$ V, $V_{GS} = 0$ V		-	-	25	μ A	
		$V_{DS} = 400$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 4.8$ A ^b	-	-	0.85	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50$ V, $I_D = 4.8$ A ^b		4.0	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1.0$ MHz, see fig. 5		-	1100	-	pF	
Output Capacitance	C_{oss}			-	170	-		
Reverse Transfer Capacitance	C_{rss}			-	18	-		
Total Gate Charge	Q_g	$V_{GS} = 10$ V	$I_D = 8.0$ A, $V_{DS} = 400$ V see fig. 6 and 13 ^b	-	-	39	nC	
Gate-Source Charge	Q_{gs}			-	-	10		
Gate-Drain Charge	Q_{gd}			-	-	19		
Turn-On Delay Time	$t_{d(on)}$			-	12	-		
Rise Time	t_r	$V_{DD} = 250$ V, $I_D = 8.0$ A, $R_g = 9.1$ Ω , $R_D = 30$ Ω see fig. 10 ^b		-	25	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	27	-		
Fall Time	t_f			-	19	-		
Internal Drain Inductance	L_D			-	4.5	-	nH	
Internal Source Inductance	L_S	Between lead, 6 mm (0.25") from package and center of die contact		-	7.5	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8.0	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	28		
Body Diode Voltage	V_{SD}	$T_J = 25$ °C, $I_S = 8.0$ A, $V_{GS} = 0$ V ^b		-	-	2.0	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25$ °C, $I_F = 8.0$ A, $dI/dt = 100$ A/ μ s ^b		-	490	740	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.0	4.5	μ C	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μ s; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$
Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150 \text{ }^\circ\text{C}$
Fig. 4 - Normalized On-Resistance vs. Temperature

IRF840LC, SiHF840LC

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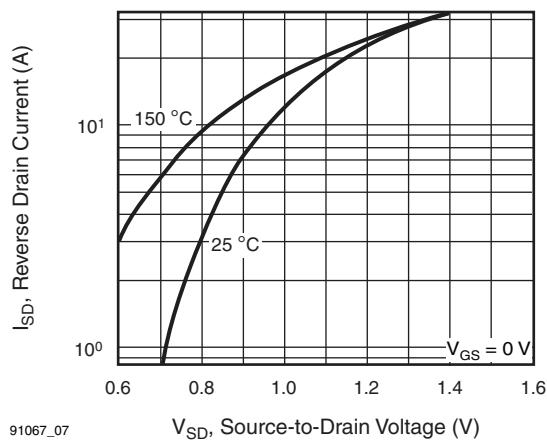
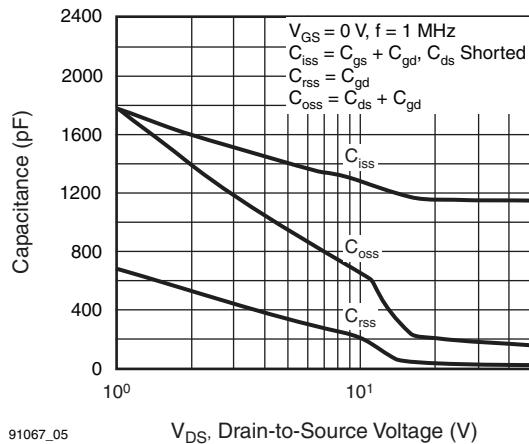


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

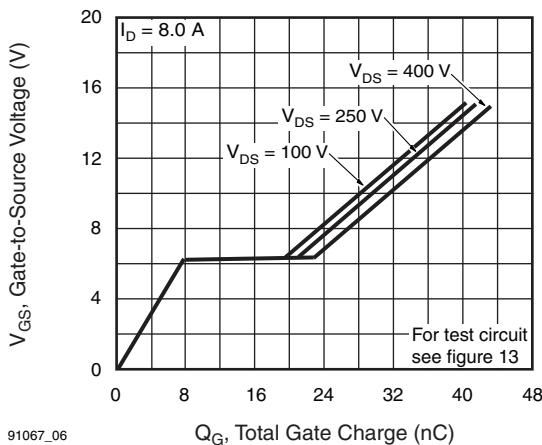


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

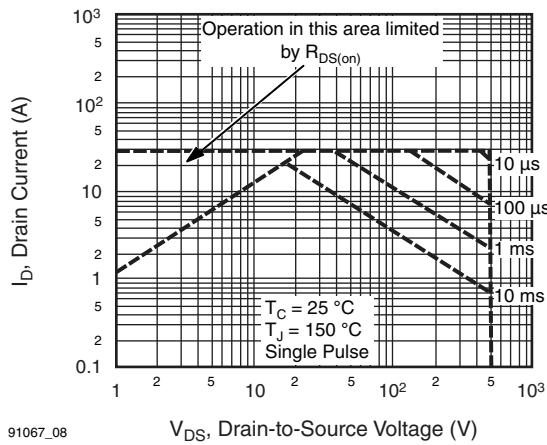
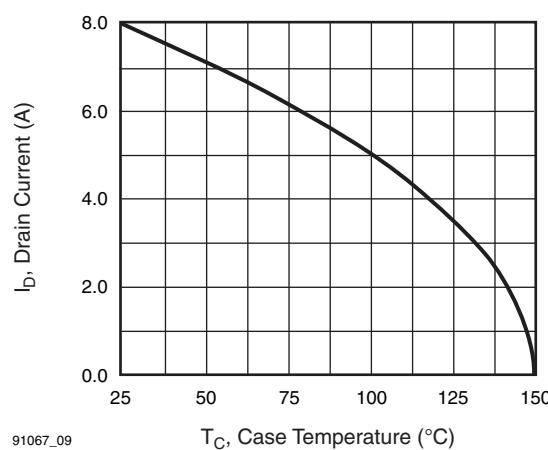
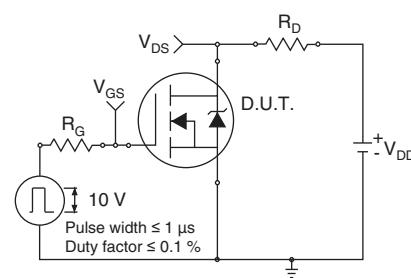
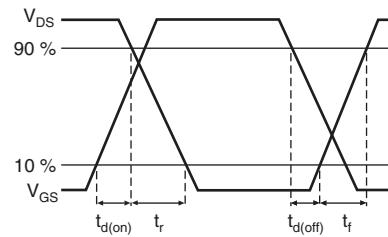
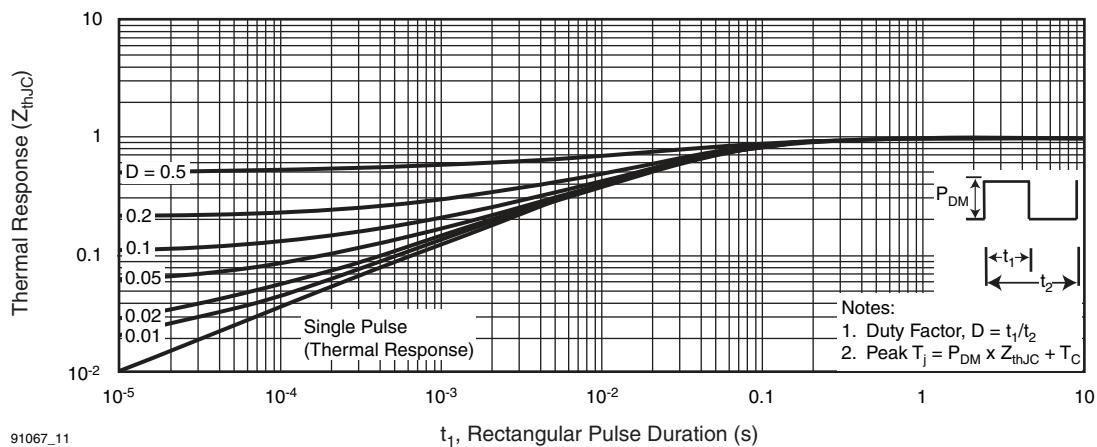


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

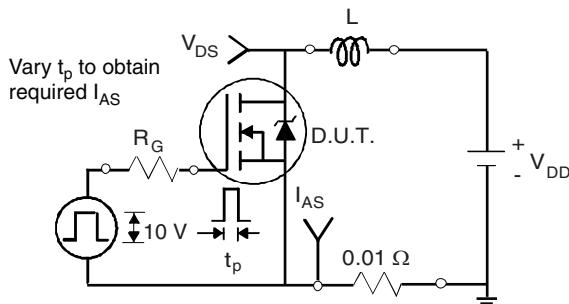


Fig. 12a - Unclamped Inductive Test Circuit

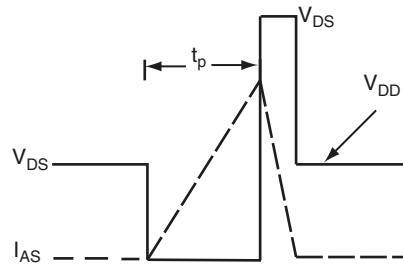


Fig. 12b - Unclamped Inductive Waveforms

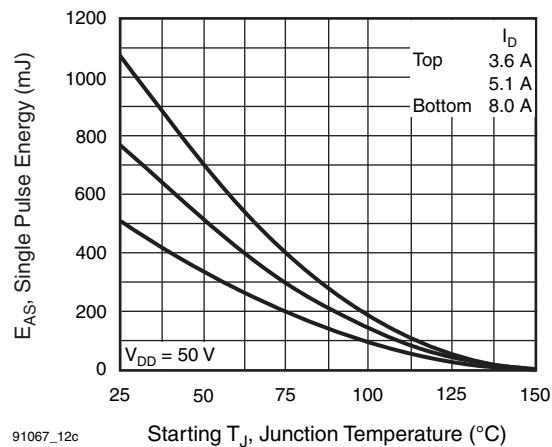


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

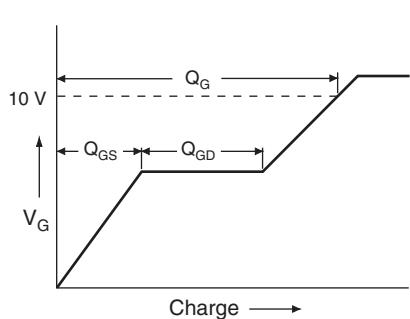


Fig. 13a - Basic Gate Charge Waveform

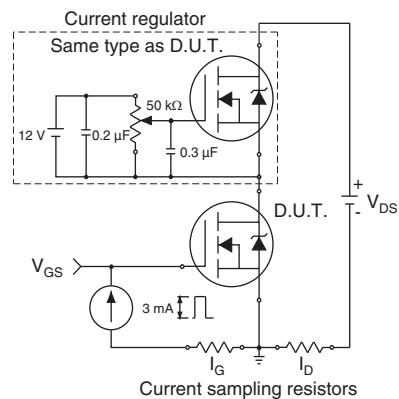
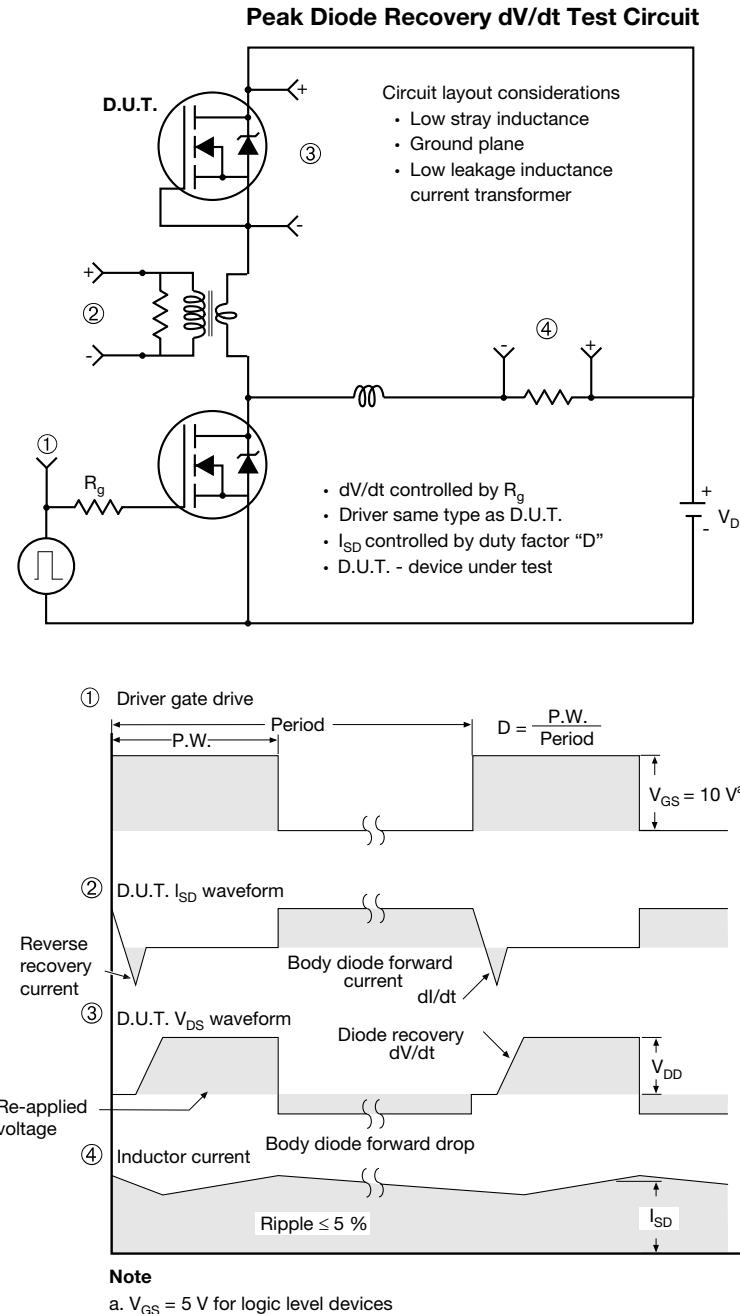
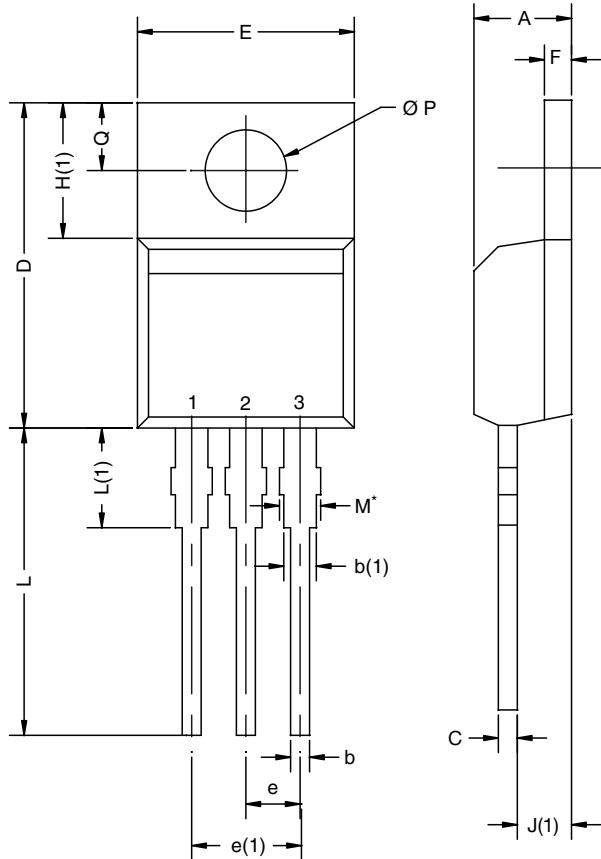


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91067.

TO-220AB



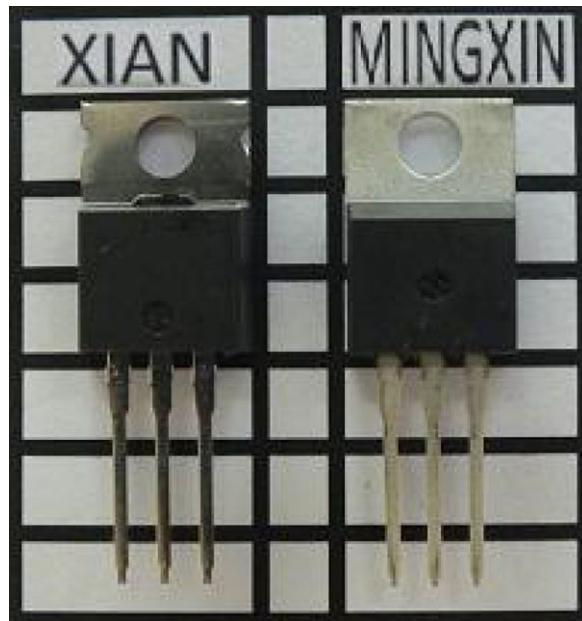
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

- Xi'an and Mingxin actual photo





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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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