

**FC4B21320L1**

**Gate resistor installed Dual N-channel MOS FET**

For lithium-ion secondary battery protection circuits

■ Features

- Source-source ON resistance:  $R_{ss(on)}$  typ. = 39 m $\Omega$  (VGS = 3.8 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1 compliant)

■ Marking Symbol: 2D

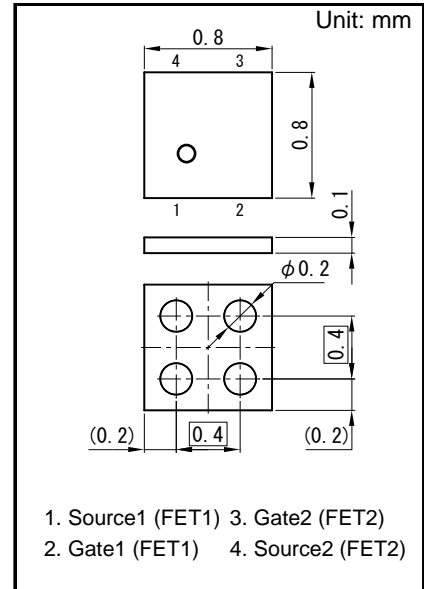
■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

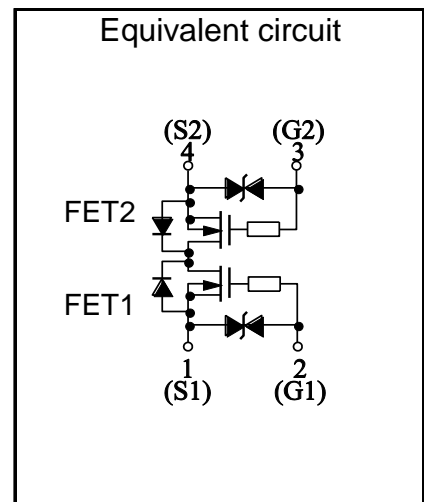
■ Absolute Maximum Ratings  $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	$\pm 8$	V
Source Current (DC)	$I_S^{*1}$	2.5	A
	$I_S^{*2}$	4	A
Source Current (Pulsed)	$I_{Sp}^{*3}$	25	A
Total Power Dissipation	$PD^{*1}$	0.34	W
	$PD^{*2}$	0.9	W
Channel Temperature	Tch	150	$^\circ\text{C}$
Storage Temperature Range	Tstg	-55 to +150	$^\circ\text{C}$
Thermal Resistance (ch-a)	$R_{th}^{*1}$	368	$^\circ\text{C/W}$
	$R_{th}^{*2}$	139	$^\circ\text{C/W}$

- Note \*1 Mounted on FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  t1.0 mm) using the minimum recommended pad size (36 $\mu\text{m}$  Copper).  
 \*2 Mounted on Ceramic substrate (70 mm  $\times$  70 mm  $\times$  t1.0 mm).  
 \*3  $t = 10\text{ }\mu\text{s}$ , Duty Cycle  $\leq 1\%$



Panasonic	XLGA004-W-0808-RA
JEITA	—
Code	—



■ Electrical Characteristics Ta = 25 °C ± 3 °C

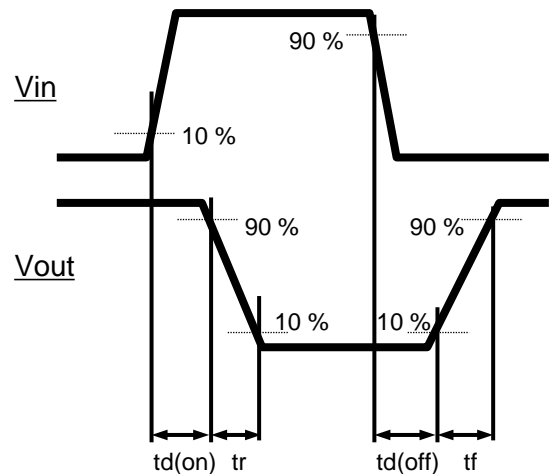
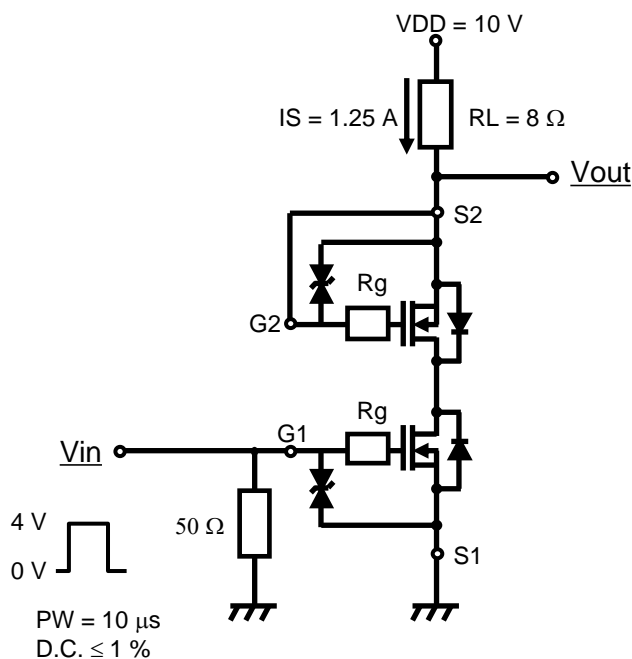
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
		VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.07 mA, VSS = 10 V	0.35	0.9	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 1.25 A, VGS = 4.5 V	27	36	48	mΩ
	RSS(on)2	IS = 1.25 A, VGS = 3.8 V	29	39	53	
	RSS(on)3	IS = 1.25 A, VGS = 3.1 V	32	45	75	
	RSS(on)4	IS = 1.25 A, VGS = 2.5 V	35	58	115	
Body Diode Forward Voltage	VF(s-s)	IF = 1.25 A, VGS = 0 V		0.6	1.2	V
Input Capacitance <sup>*1</sup>	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		205		pF
Output Capacitance <sup>*1</sup>	Coss			50		
Reverse Transfer Capacitance <sup>*1</sup>	Crss			40		
Turn-on delay Time <sup>*1,*2</sup>	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		0.10		μs
Rise Time <sup>*1,*2</sup>	tr	IS = 1.25 A		0.15		
Turn-off delay Time <sup>*1,*2</sup>	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		0.50		μs
Fall Time <sup>*1,*2</sup>	tf	IS = 1.25 A		0.30		
Total Gate Charge <sup>*1</sup>	Qg	VDD = 10 V		3.5		nC
Gate-source Charge <sup>*1</sup>	Qgs	VGS = 0 to 4.0 V,		0.8		
Gate-drain Charge <sup>*1</sup>	Qgd	IS = 1.25 A		1.0		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Guaranteed by design, not subject to production testing

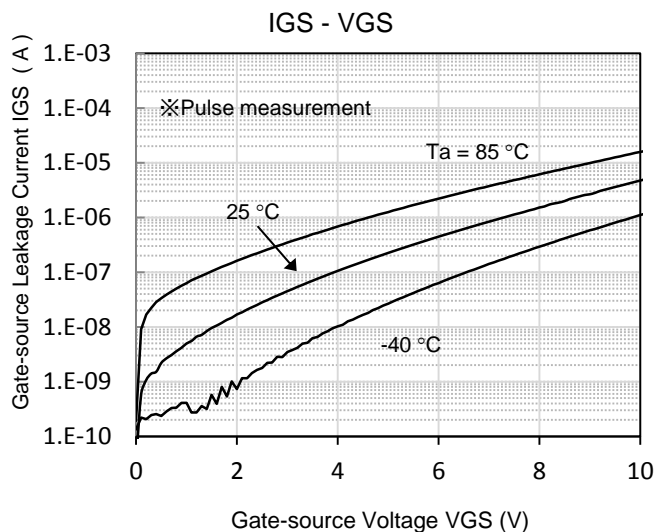
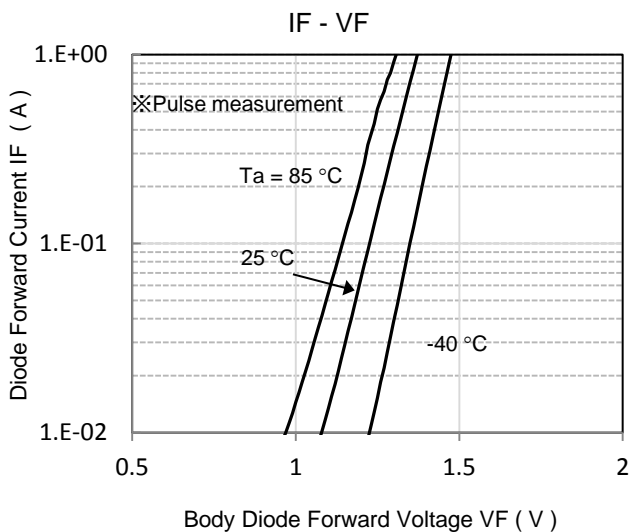
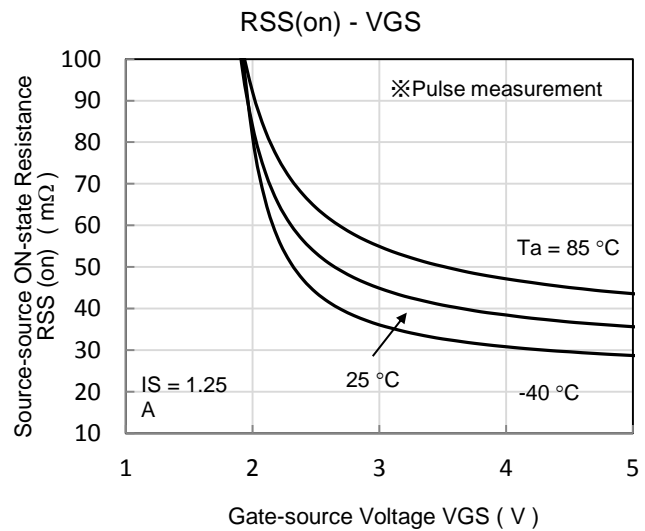
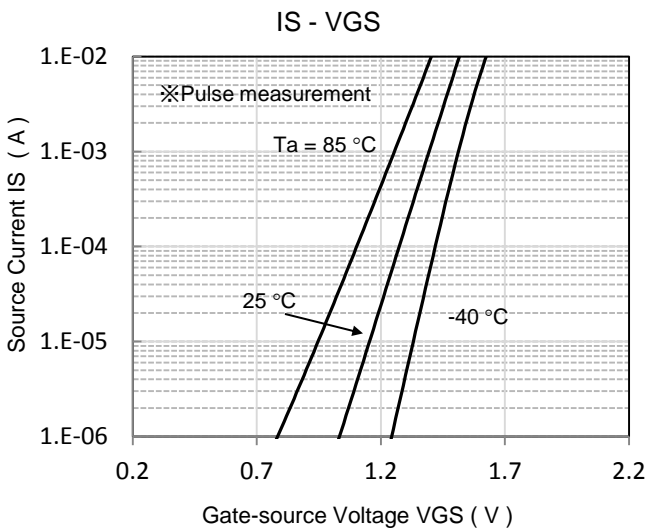
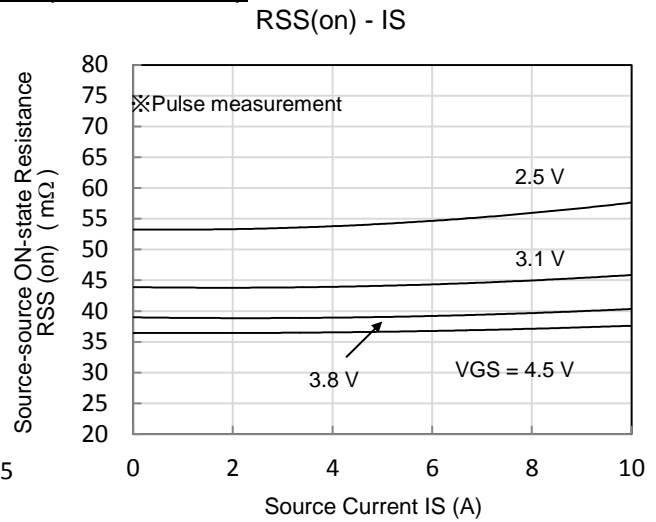
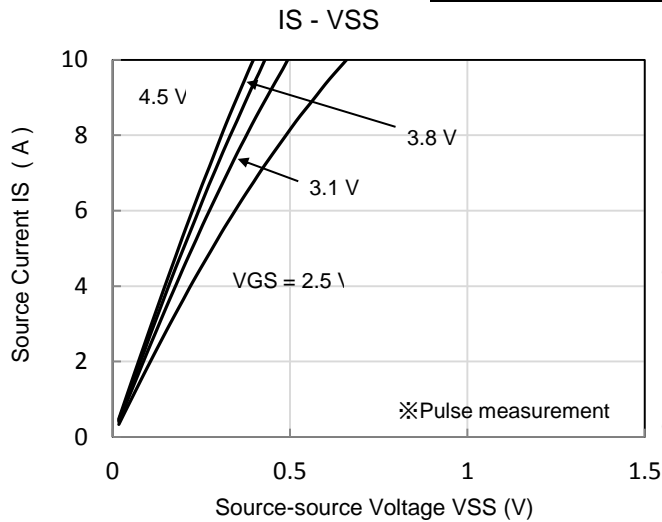
\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2 : Measurement circuit



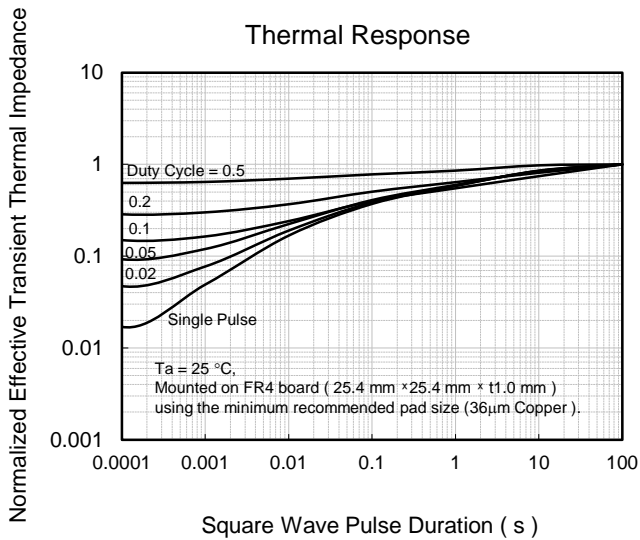
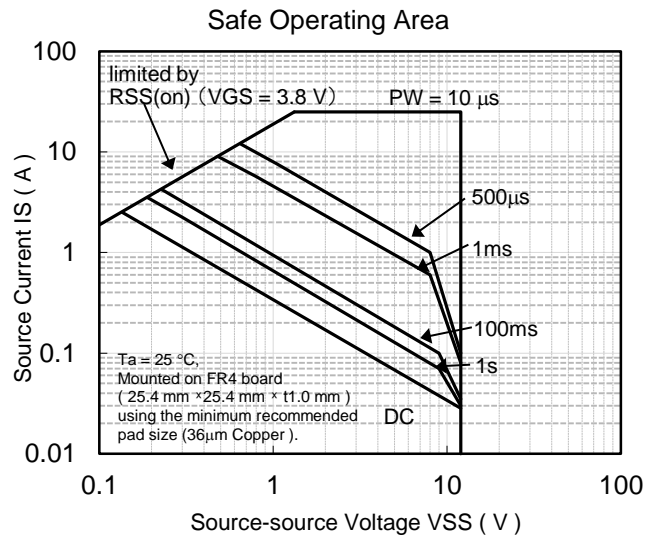
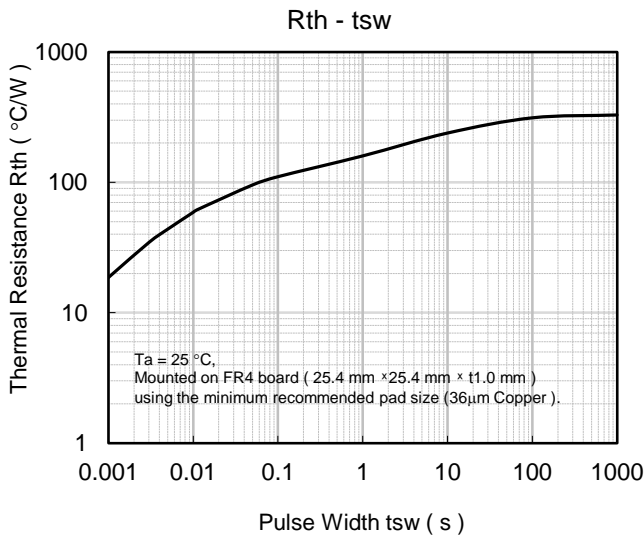
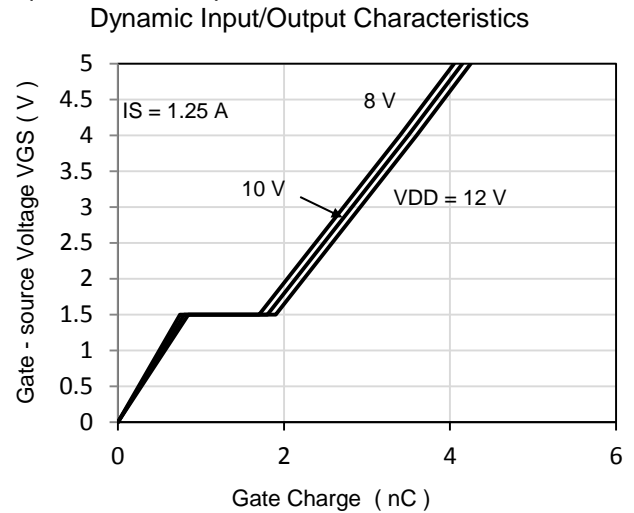
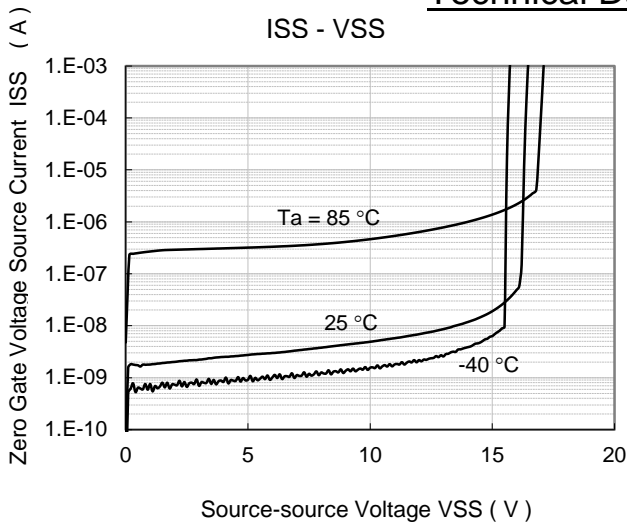


Technical Data ( reference )



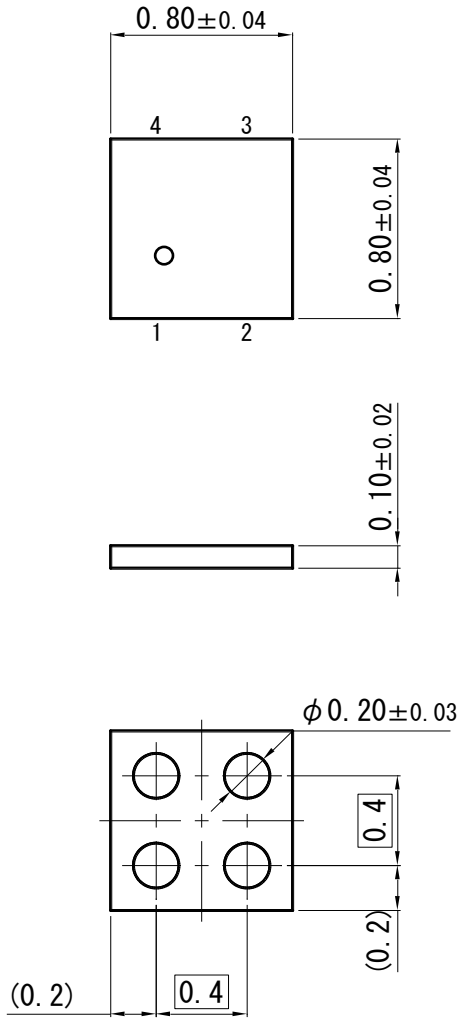


Technical Data ( reference )



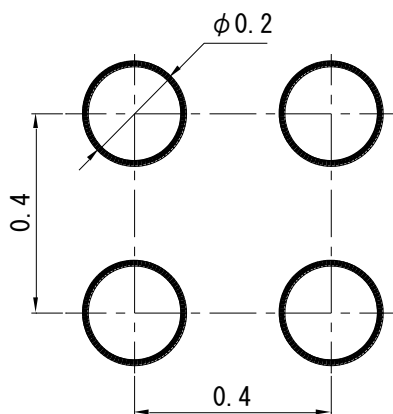
■ Outline (XLGA004-W-0808-RA)

Unit: mm



■ Land Pattern (Reference)

Unit: mm



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