LM3481/LM3481Q High Efficiency Low-Side N-Channel Controller for Switching Regulators

Check for Samples: LM3481

FEATURES

- **LM3481QMM in the VSSOP-10 Package are Automotive Grade Products that are AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)**
- **10-Lead VSSOP Package**
- **Internal Push-Pull Driver with 1A Peak Current Capability**
- **Current Limit and Thermal Shutdown**
- **Frequency Compensation Optimized with a Capacitor and a Resistor**
- **Internal Softstart**
- **Current Mode Operation**
- **Adjustable Undervoltage Lockout with Hysteresis**
- **Pulse Skipping at Light Loads**

APPLICATIONS

- **Distributed Power Systems**
- **Notebook, PDA, Digital Camera, and other Portable Applications**
- **Offline Power Supplies**
- **Set-Top Boxes**

KEY SPECIFICATIONS

- **Wide Supply Voltage Range of 2.97V to 48V**
- **100 kHz to 1 MHz Adjustable and Synchronizable Clock Frequency**
- **±1.5% (Over Temperature) Internal Reference**
- **10 µA Shutdown Current (Over Temperature)**

DESCRIPTION

The LM3481 is a versatile Low-Side N-FET high performance controller for switching regulators. It is suitable for use in topologies requiring a low-side FET, such as boost, flyback, SEPIC, etc. The LM3481 can be operated at extremely high switching frequencies in order to reduce the overall solution size. The switching frequency of the LM3481 can be adjusted to any value between 100 kHz and 1 MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit can be programmed with a single external resistor.

The LM3481 has built in protection features such as thermal shutdown, short-circuit protection and over voltage protection. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

TYPICAL APPLICATION CIRCUIT

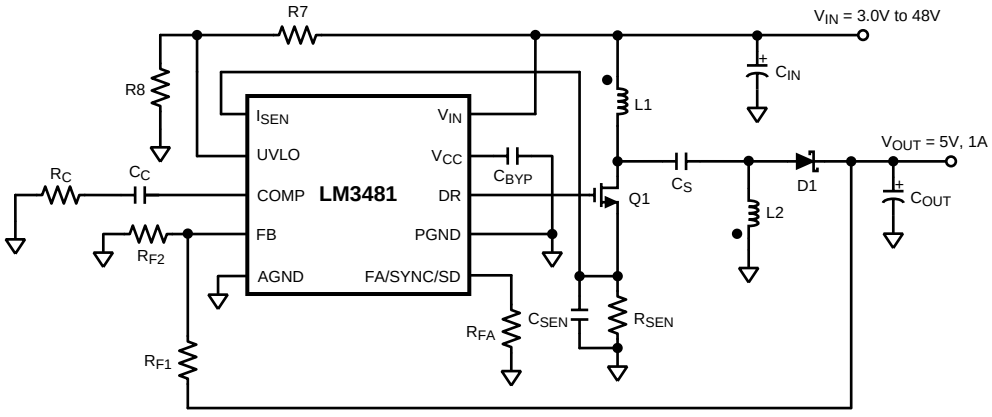


Figure 1. Typical SEPIC Converter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

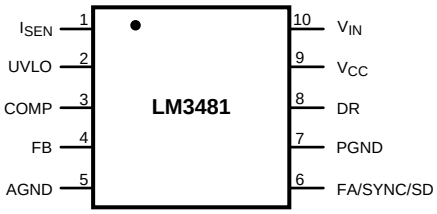


Figure 2. 10-Lead VSSOP Package
(DGS-10 Package)

PIN DESCRIPTIONS

Pin Name	Pin Number	Description
I_{SEN}	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
UVLO	2	Under voltage lockout pin. A resistor divider from V_{IN} to ground is connected to the UVLO pin. The ratio of these resistances determine the input voltage which allows switching and the hysteresis to disable switching.
COMP	3	Compensation pin. A resistor and capacitor combination connected to this pin provides compensation for the control loop.
FB	4	Feedback pin. Inverting input of the error amplifier.
AGND	5	Analog ground pin. Internal bias circuitry reference. Should be connected to PGND at a single point.
FA/SYNC/SD	6	Frequency adjust, synchronization, and shutdown pin. A resistor connected from this pin to ground sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the frequency of the clock. A high level on this pin for ≥ 30 µs will turn the device off and the device will then draw 5 µA from the supply typically.
PGND	7	Power ground pin. External power circuitry reference. Should be connected to AGND at a single point.
DR	8	Drive pin of the IC. The gate of the external MOSFET should be connected to this pin.
V_{CC}	9	Driver supply voltage pin. A bypass capacitor must be connected from this pin to PGND. See DRIVER SUPPLY CAPACITOR SELECTION section.
V_{IN}	10	Power supply input pin.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} pin Voltage	-0.4V to 50V
FB Pin Voltage	-0.4V to 6V
FA/SYNC/SD Pin Voltage	-0.4V to 6V
COMP Pin Voltage	-0.4V to 6V
UVLO Pin Voltage	-0.4V to 6V
V_{CC} Pin Voltage	-0.4V to 6V
DR Pin Voltage	-0.4V to 6V
I_{SEN} Pin Voltage	–0.4V to 600 mV
Peak Driver Output Current	1.0A
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
ESD Susceptibility Human Body Model (2)	2 kV
Lead Temperature DGS Package Vapor Phase (60 sec.) Infared (15 sec.)	 215°C 220°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions.
(2) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS (1)

Supply Voltage	2.97V to 48V
Junction Temperature Range	−40°C to +125°C
Switching Frequency Range	100 kHz to 1 MHz

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, R_{FA}=40 kΩ unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_J = 25°C. Limits appearing in **boldfacetype** apply over the full **Operating Temperature Range** (-40°C to 125°C). Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	V_{COMP} = 1.4V, 2.97 ≤ V_{IN} ≤ 48V	**1.256**	1.275	**1.294**	V
ΔV_{LINE}	Feedback Voltage Line Regulation	2.97 ≤ V_{IN} ≤ 48V		0.003		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{EAO} Source/Sink		±0.5		%/A
$V_{UVLOSEN}$	Undervoltage Lockout Reference Voltage	V_{UVLO} Ramping Down	**1.345**	1.430	**1.517**	V
I_{UVLO}	UVLO Source Current	Enabled	**3**	5	**6**	µA
V_{UVLOSD}	UVLO Shutdown Voltage			0.7		V
I_{COMP}	COMP pin Current Sink	V_{FB} = 0V		640		µA
V_{COMP}		V_{FB} = 1.275V		1		V
f_{nom}	Nominal Switching Frequency	R_{FA} = 40 kΩ	**406**	475	**550**	kHz
$V_{sync-HI}$	Threshold for Synchronization on FA/SYNC/SD pin	Synchronization Voltage Rising		1.4		V
$V_{sync-LOW}$	Threshold for Synchronization on FA/SYNC/SD pin	Synchronization Voltage Falling		0.7		V

(1) All limits are guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, R_{FA}=40 kΩ unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_J = 25°C. Limits appearing in **boldfacetype** apply over the full **Operating Temperature Range** (-40°C to 125°C). Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$R_{DS1\ (ON)}$	Driver Switch On Resistance (top)	I_{DR} = 0.2A, V_{IN}= 5V		4		Ω
$R_{DS2\ (ON)}$	Driver Switch On Resistance (bottom)	I_{DR} = 0.2A		2		Ω
$V_{DR\ (max)}$	Maximum Drive Voltage Swing(3)	V_{IN} < 6V		V_{IN}		V
		V_{IN} ≥ 6V		6		
D_{max}	Maximum Duty Cycle			85		%
t_{min} (on)	Minimum On Time			250		ns
I_{SUPPLY}	Supply Current (switching)	See (4)		3.7	**5.0**	mA
I_Q	Quiescent Current in Shutdown Mode	$V_{FA/SYNC/SD}$ = 3V(5), V_{IN} = 12V		9	**15**	µA
		$V_{FA/SYNC/SD}$ = 3V(5), V_{IN} = 5V		5	**10**	
V_{SENSE}	Current Sense Threshold Voltage		**100**	160	**190**	mV
V_{SC}	Over Load Current Limit Sense Voltage		**157**	220	**275**	mV
V_{SL}	Internal Compensation Ramp Voltage			90		mV
V_{OVP}	Output Over-voltage Protection (with respect to feedback voltage) (6)	V_{COMP} = 1.4V	**26**	85	**135**	mV
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis	V_{COMP} = 1.4V	**28**	70	**106**	mV
Gm	Error Amplifier Transconductance	V_{COMP} = 1.4V	**216**	450	**690**	µmho
A_{VOL}	Error Amplifier Voltage Gain	V_{COMP} = 1.4V I_{EAO} = 100 µA (Source/Sink)	**35**	60	**66**	V/V
I_{EAO}	Error Amplifier Output Current (Source/ Sink)	Source, V_{COMP} = 1.4V, V_{FB} = 1.1V	**475**	640	**837**	µA
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V	**31**	65	**100**	µA
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit, V_{FB} = 0V, COMP Pin Floating	**2.45**	2.70	**2.93**	V
		Lower Limit, V_{FB} = 1.4V	**0.32**	0.60	**0.90**	V
t_{SS}	Internal Soft-Start Delay	V_{FB} = 1.2V, COMP Pin Floating		15		ms
t_r	Drive Pin Rise Time	Cgs = 3000 pf, V_{DR} = 0V to 3V		25		ns
t_f	Drive Pin Fall Time	Cgs = 3000 pf, V_{DR} = 3V to 0V		25		ns
V_{SD}	Shutdown signal threshold (7) FA/SYNC/SD pin	Output = High (Shutdown)		1.31	**1.40**	V
		Output = Low (Enable)	**0.40**	0.68		V
I_{SD}	Shutdown Pin Current FA/SYNC/SD pin	V_{SD} = 5V		−1		µA
		V_{SD} = 0V		20		
T_{SD}	Thermal Shutdown			165		°C
T_{sh}	Thermal Shutdown Hysteresis			10		°C
θ_{JA}	Thermal Resistance	DGS Package		200		°C/W

(3) The drive pin voltage, V_{DR}, is equal to the input voltage when input voltage is less than 6V. V_{DR} is equal to 6V when the input voltage is greater than or equal to 6V.
(4) For this test, the FA/SYNC/SD Pin is pulled to ground using a 40 kΩ resistor .
(5) For this test, the FA/SYNC/SD Pin is pulled to 3V using a 40 kΩ resistor.
(6) The over-voltage protection is specified with respect to the feedback voltage. This is because the over-voltage protection tracks the feedback voltage. The over-voltage threshold can be calculated by adding the feedback voltage (V_{FB}) to the over-voltage protection specification.
(7) The FA/SYNC/SD pin should be pulled to V_{IN} through a resistor to turn the regulator off. The voltage on the FA/SYNC/SD pin must be above the max limit for the Output = High longer than 30 µs to keep the regulator off and must be below the minimum limit for Output = Low to keep the regulator on.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

Comp Pin Voltage vs. Load Current

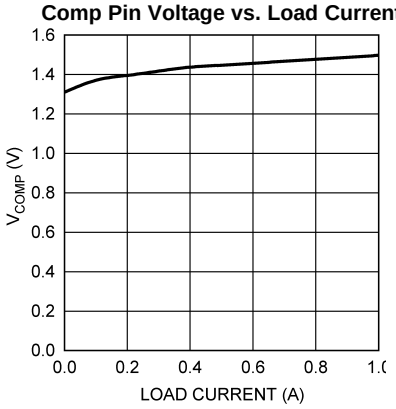


Figure 3.

Switching Frequency vs. R_{FA}

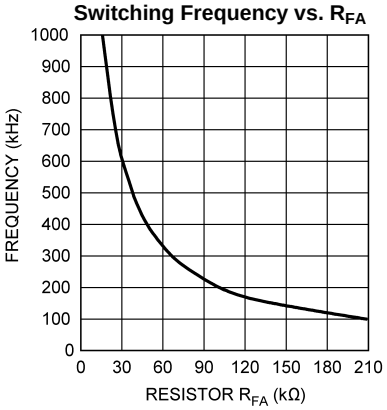


Figure 4.

Efficiency vs. Load Current ($3.3V_{IN}$ and $12V_{OUT}$)

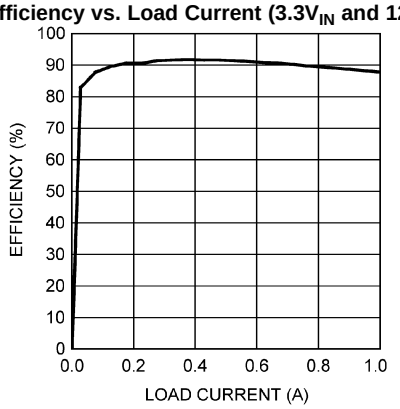


Figure 5.

Efficiency vs. Load Current ($5V_{IN}$ and $12V_{OUT}$)

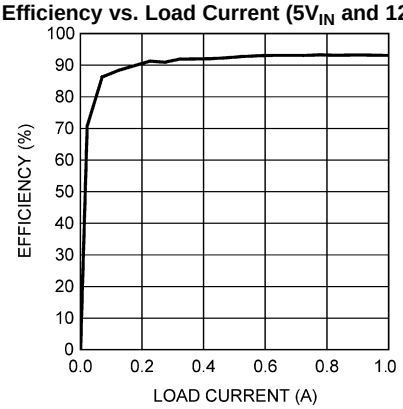


Figure 6.

Efficiency vs. Load Current ($9V_{IN}$ and $12V_{OUT}$)

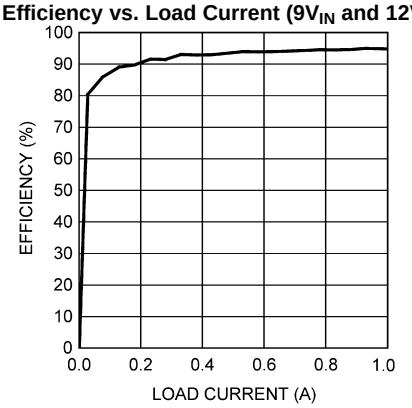


Figure 7.

Frequency vs. Temperature

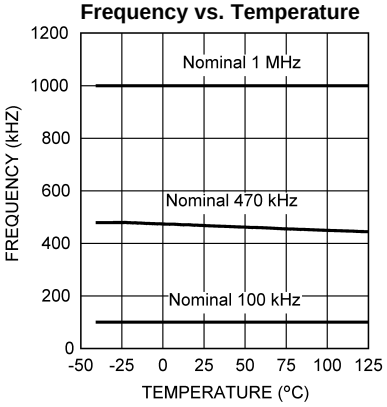


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

COMP Pin Source Current vs. Temperature

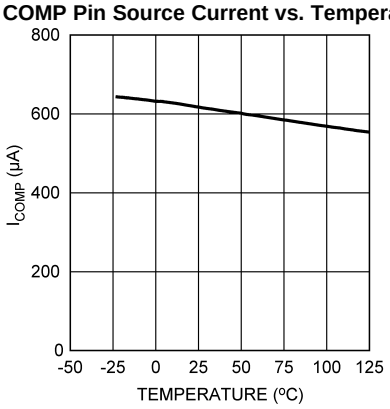


Figure 9.

I_{Supply} vs. Input Voltage (Non-Switching)

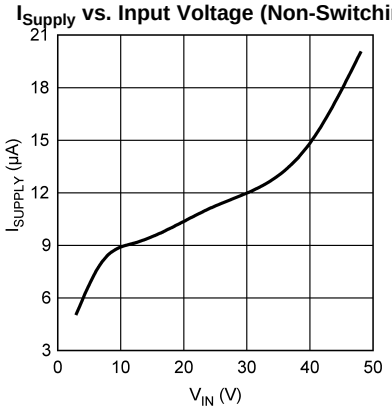


Figure 10.

I_{Supply} vs. Input Voltage (Switching)

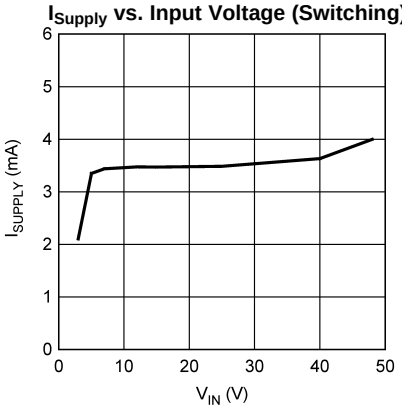


Figure 11.

Shutdown Threshold Hysteresis vs. Temperature

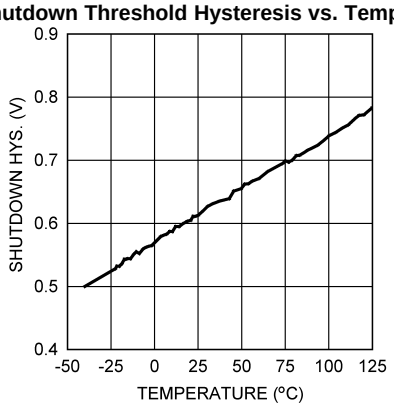


Figure 12.

Drive Voltage vs. Input Voltage

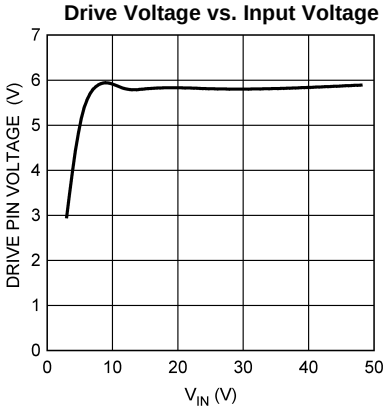


Figure 13.

Short Circuit Protection vs. V_{IN}

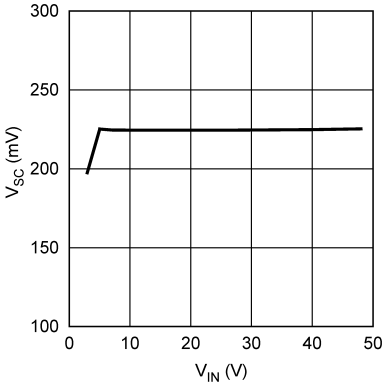


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

Current Sense Threshold vs. Input Voltage

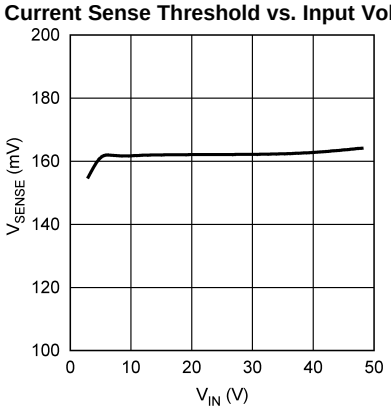


Figure 15.

Compensation Ramp Amplitude vs. Input Voltage

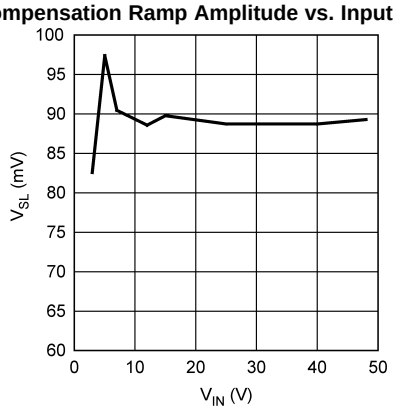


Figure 16.

Minimum On-Time vs. Temperature

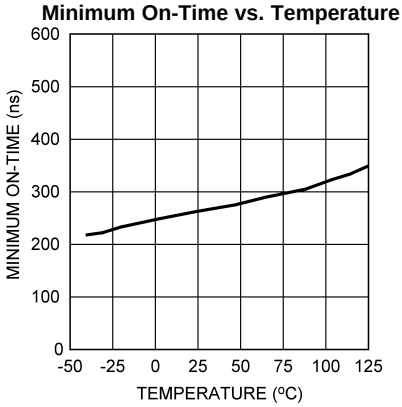
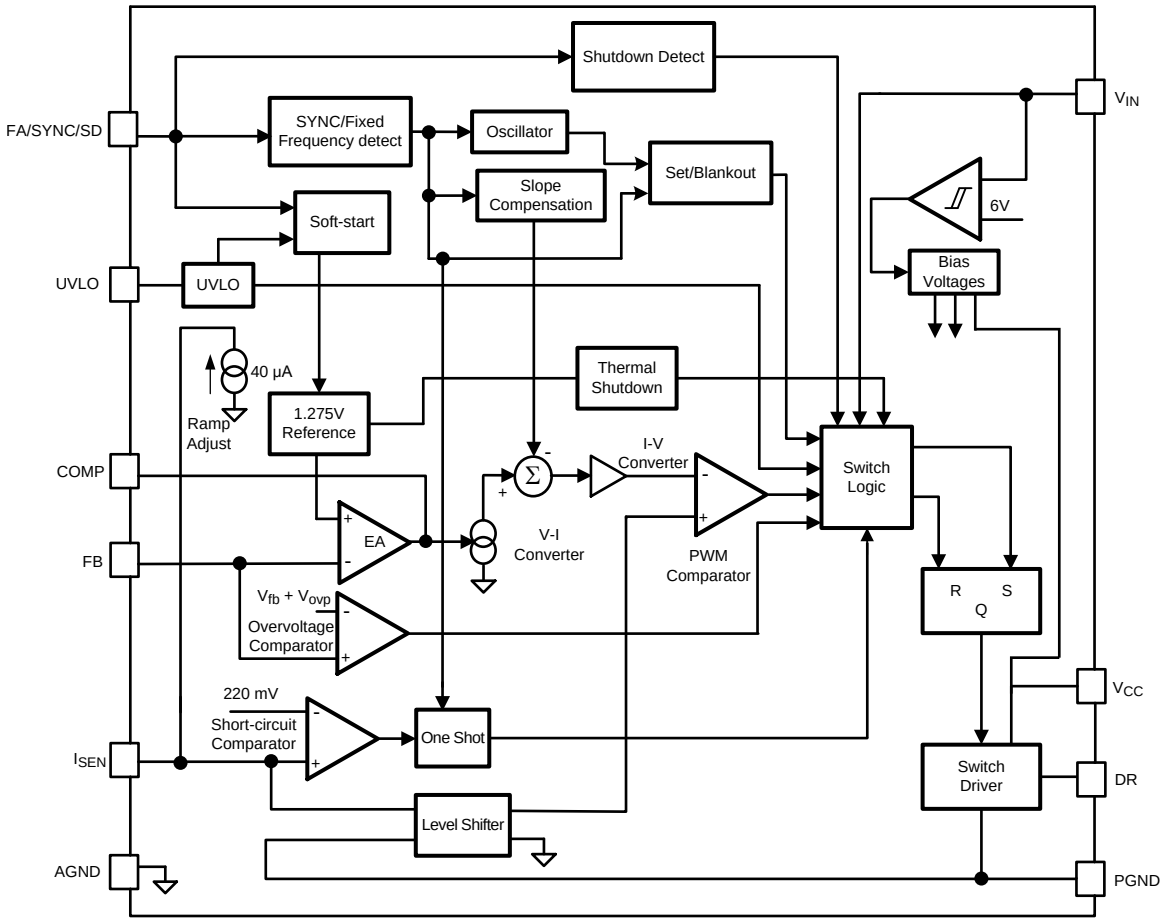


Figure 17.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The LM3481 uses a fixed frequency, Pulse Width Modulated (PWM), current mode control architecture. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is then level shifted and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier (EA) negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator.

At the start of any switching cycle, the oscillator sets the RS latch using the SET/Blank-out and switch logic blocks. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in Figure 18. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration, called the blank-out time, is typically 250 ns and is specified as t_{min} (on) in the electrical characteristics section.

Under extremely light load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the blank-out time is more than what is delivered to the load. An over-voltage comparator inside the LM3481 prevents the output voltage from rising under these conditions by sensing the feedback (FB pin) voltage and resetting the RS latch. The latch remains in a reset state until the output decays to the nominal value. Thus the operating frequency decreases at light loads, resulting in excellent efficiency.

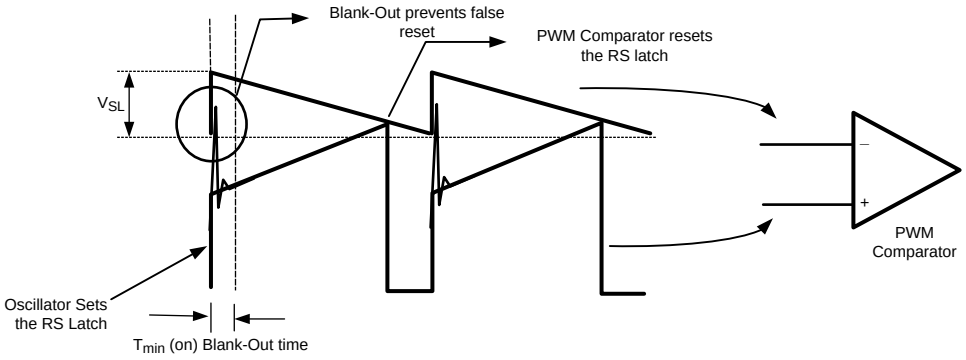


Figure 18. Basic Operation of the PWM Comparator

OVER VOLTAGE PROTECTION

The LM3481 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at anytime the voltage at the feedback pin rises to V_{FB} + V_{OVP}, OVP is triggered. See the electrical characteristics section for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin (DR) to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3481 will begin switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See the electrical characteristics section for limits on $V_{OVP(HYS)}$.

The internal bias of the LM3481 comes from either the internal bias voltage generator as shown in the block diagram or directly from the voltage at the VIN pin. At input voltages lower than 6V the internal IC bias is the input voltage and at voltages above 6V the internal bias voltage generator of the LM3481 provides the bias.

SLOPE COMPENSATION RAMP

The LM3481 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. It is easy to parallel power stages using current mode control since current sharing is automatic. However there is a natural instability that will occur for duty cycles, D, greater than 50% if additional slope compensation is not addressed as described below.

The current mode control scheme samples the inductor current, I_L, and compares the sampled signal, V_{samp}, to a internally generated control signal, V_c. The current sense resistor, R_{SEN}, as shown in Figure 22, converts the sampled inductor current, I_L, to the voltage signal, V_{samp}, that is proportional to I_L such that:

$$V_{samp} = I_L \times R_{SEN}$$

The rising and falling slopes, M_1 and $-M_2$ respectively, of V_{samp} are also proportional to the inductor current rising and falling slopes, M_{on} and $-M_{off}$ respectively. Where M_{on} is the inductor slope during the switch on-time and $-M_{off}$ is the inductor slope during the switch off-time and are related to M_1 and $-M_2$ by:

$$M_1 = M_{on} \times R_{SEN}$$
$$-M_2 = -M_{off} \times R_{SEN}$$

For the boost topology:

$$M_{on} = V_{IN} / L$$
$$-M_{off} = (V_{IN} - V_{OUT}) / L$$
$$M_1 = [V_{IN} / L] \times R_{SEN}$$
$$-M_2 = [(V_{IN} - V_{OUT}) / L] \times R_{SEN}$$
$$M_2 = [(V_{OUT} - V_{IN}) / L] \times R_{SEN}$$

Current mode control has an inherent instability for duty cycles greater than 50%, as shown in Figure 19, where the control signal slope, M_C, equals zero. In Figure 19, a small increase in the load current causes the sampled signal to increase by ΔV_{samp0}. The effect of this load change, ΔV_{samp1}, at the end of the first switching cycle is :

$$\Delta V_{samp1} = -\left(\frac{M_2}{M_1}\right) \Delta V_{samp0} = -\left(\frac{D}{1-D}\right) \Delta V_{samp0}$$

From the above equation, when D > 0.5, ΔV_{samp1} will be greater than ΔV_{samp0}. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase. To ensure that the perturbed signal converges we must maintain:

$$\left|-\frac{M_2}{M_1}\right| < 1$$

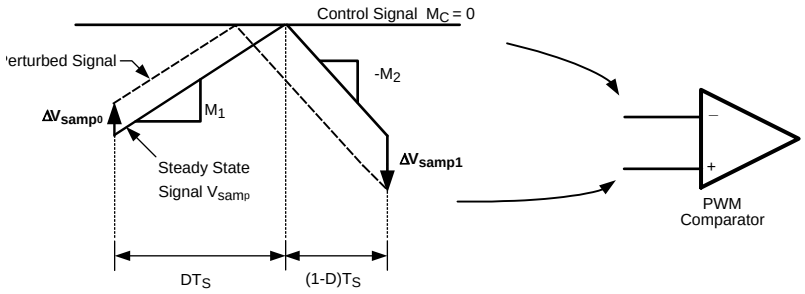


Figure 19. Sub-Harmonic Oscillation for D>0.5

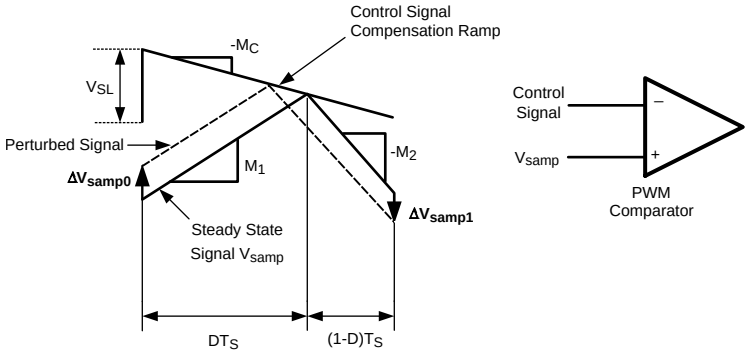


Figure 20. Compensation Ramp Avoids Sub-Harmonic Oscillation

To prevent the sub-harmonic oscillations, a compensation ramp is added to the control signal, as shown in Figure 20.

With the compensation ramp, ΔV_{samp1} and the convergence criteria are expressed by,

$$\Delta V_{samp1} = -\left(\frac{M_2 - M_C}{M_1 + M_C}\right)\Delta V_{samp0}$$

$$\left|-\frac{M_2 - M_C}{M_1 + M_C}\right| < 1$$

The compensation ramp has been added internally in the LM3481. The slope of this compensation ramp has been selected to satisfy most applications, and it's value depends on the switching frequency. This slope can be calculated using the formula:

$$M_C = V_{SL} \times f_S$$

In the above equation, V_{SL} is the amplitude of the internal compensation ramp and f_S is the controller's switching frequency. Limits for V_{SL} have been specified in the electrical characteristics section.

In order to provide the user additional flexibility, a patented scheme has been implemented inside the IC to increase the slope of the compensation ramp externally, if the need arises. Adding a single external resistor, R_{SL}(as shown in Figure 22) increases the amplitude of the compensation ramp as shown in Figure 21.

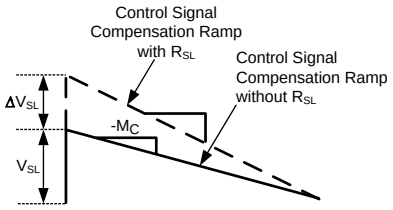


Figure 21. Additional Slope Compensation Added Using External Resistor R_{SL}

Where,

$$\Delta V_{SL} = K \times R_{SL}$$

K = 40 µA typically and changes slightly as the switching frequency changes. Figure 23 shows the effect the current K has on $\Delta V_{SL}$and different values of R_{SL} as the switching frequency changes.

A more general equation for the slope compensation ramp, M_C, is shown below to include ΔV_{SL} caused by the resistor R_{SL}.

$$M_C = (V_{SL} + \Delta V_{SL}) \times f_S$$

It is good design practice to only add as much slope compensation as needed to avoid subharmonic oscillation. Additional slope compensation minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current.

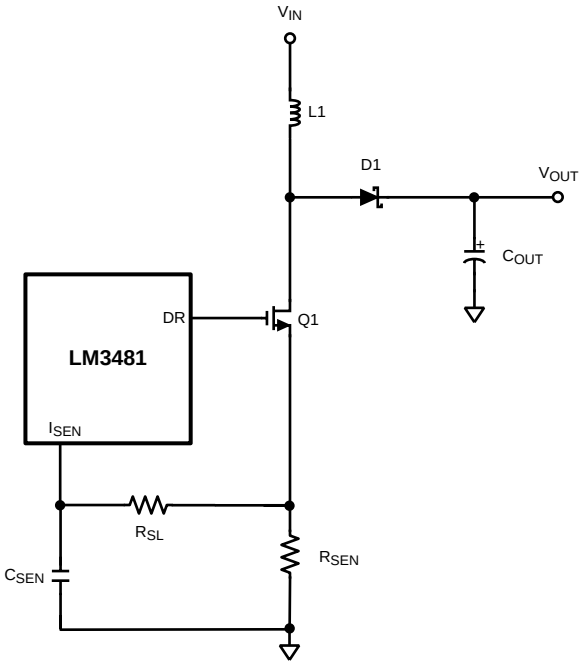


Figure 22. Increasing the Slope of the Compensation Ramp

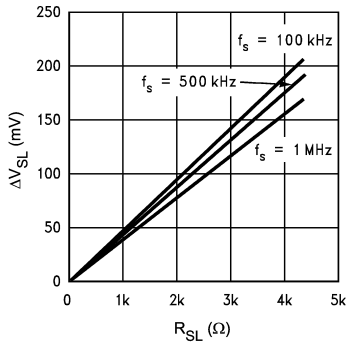


Figure 23. ΔV_{SL} vs R_{SL}

FREQUENCY ADJUST/SYNCHRONIZATION/SHUTDOWN

The switching frequency of the LM3481 can be adjusted between 100 kHz and 1 MHz using a single external resistor. This resistor must be connected between the FA/SYNC/SD pin and ground, as shown in Figure 24. Please refer to the typical performance characteristics to determine the value of the resistor required for a desired switching frequency.

The following equation can also be used to estimate the frequency adjust resistor.

Where f_S is in kHz and R_{FA} in kΩ.

$$R_{FA} = \frac{22 \times 10^3}{f_S} - 5.74$$

The LM3481 can be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground, as shown in Figure 25. The frequency adjust resistor may remain connected while synchronizing a signal, therefore if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor.

It is also necessary to have the width of the synchronization pulse narrower than the duty cycle of the converter and to have the synchronization pulse width ≥ 300 ns.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (refer to the electrical characteristics section for definition of high signal) appears on the FA/SYNC/SD pin, the LM3481 stops switching and goes into a low current mode. The total supply current of the IC reduces to 5 µA, typically, under these conditions.

Figure 26 and Figure 27 shows an implementation of a shutdown function when operating in frequency adjust mode and synchronization mode respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or synchronization mode, a high signal for more than 30 µs shuts down the IC.

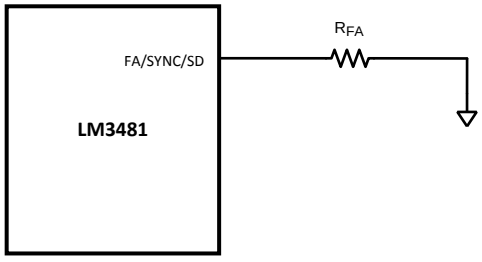


Figure 24. Frequency Adjust

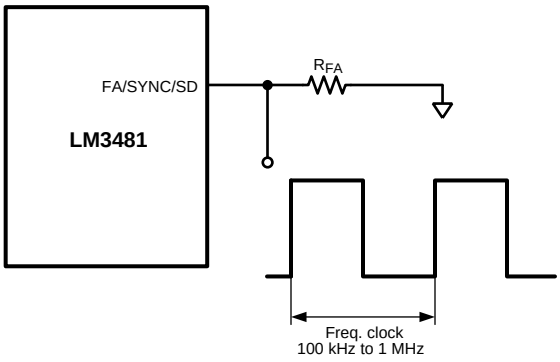


Figure 25. Frequency Synchronization

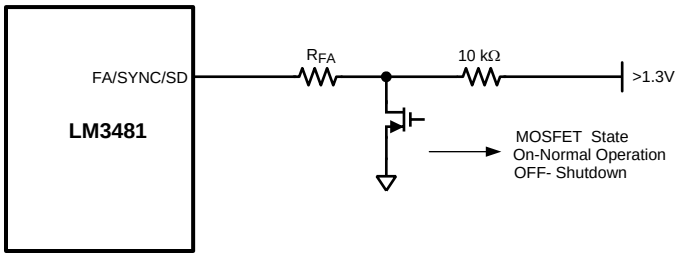


Figure 26. Shutdown Operation in Frequency Adjust Mode

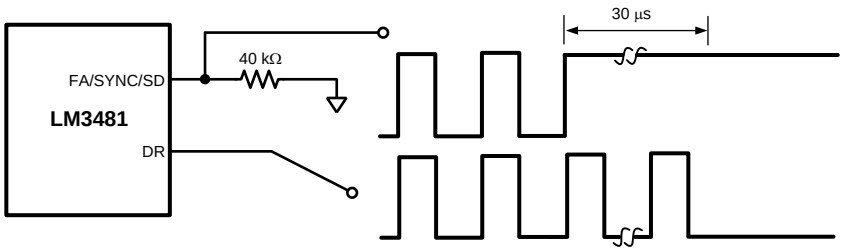


Figure 27. Shutdown Operation in Synchronization Mode

UNDER VOLTAGE LOCKOUT (UVLO) Pin

The UVLO pin provides user programmable enable and shutdown thresholds. The UVLO pin is compared to an internal reference of 1.43V (typical), and a resistor divider programs the enable threshold, V_{EN}. When the IC is enabled, a 5 µA current is sourced out of the UVLO pin, which effectively causes a hysteresis, and the UVLO shutdown threshold, V_{SH}, is now lower than the enable threshold. Setting these thresholds requires two resistors connected from the V_{IN} pin to the UVLO pin and from the UVLO pin to GND (see Figure 28). Select the desired enable, V_{EN}, and UVLO shutdown, V_{SH}, threshold voltages and use the following equations to determine the resistance values:

$$R8 = \frac{1.43V}{I_{UVLO}} \times \left(1 + \frac{1.43V - V_{SH}}{V_{EN} - 1.43V}\right)$$

$$R7 = R8 \times \left(\frac{V_{EN}}{1.43V} - 1\right)$$

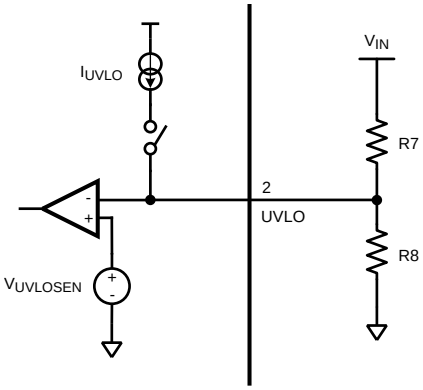


Figure 28. UVLO Pin Resistor Divider

If the UVLO pin function is not desired, select R8 and R7 of equal magnitude greater than 100 kΩ. This will allow V_{IN} to be in control of the UVLO thresholds. The UVLO pin may also be used to implement the enable/disable function. If a signal pulls the UVLO pin below the 1.43V (typical) threshold, the converter will be disabled.

SHORT CIRCUIT PROTECTION

When the voltage across the sense resistor (measured on the I_{SEN} Pin) exceeds 220 mV, short-circuit current limit gets activated. A comparator inside the LM3481 reduces the switching frequency by a factor of 8 and maintains this condition until the short is removed.

TYPICAL APPLICATIONS

The LM3481 may be operated in either continuous or discontinuous conduction mode. The following applications are designed for continuous conduction operation. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

Boost Converter

The most common topology for the LM3481 is the boost or step-up topology. The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost regulator is shown in Figure 29. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles. In the first cycle of operation, MOSFET Q is turned on and energy is stored in the inductor. During this cycle, diode D1 is reverse biased and load current is supplied by the output capacitor, C_{OUT}.

In the second cycle, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined as:

$$V_{OUT} = \frac{V_{IN}}{1\text{-}D}$$

(ignoring the voltage drop across the MOSFET and the diode), or

$$V_{OUT} + V_{D1} - V_Q = \frac{V_{IN} - V_Q}{1\text{-}D}$$

where D is the duty cycle of the switch, V_{D1} is the forward voltage drop of the diode, and V_Q is the drop across the MOSFET when it is on. The following sections describe selection of components for a boost converter.

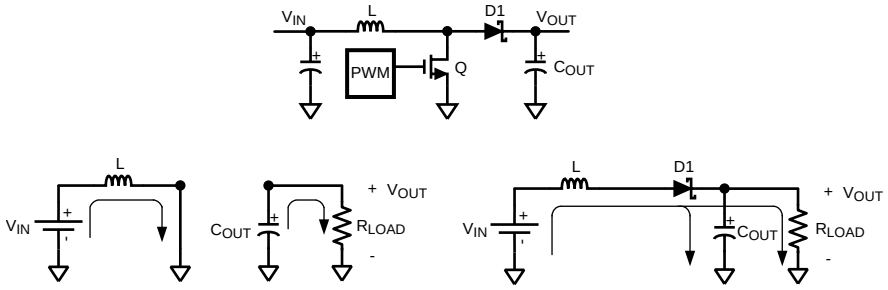


Figure 29. Simplified Boost Converter Diagram (a) First cycle of operation. (b) Second cycle of operation

POWER INDUCTOR SELECTION

The inductor is one of the two energy storage elements in a boost converter. Figure 30 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified as:

$$V_L(t) = L \frac{di_L(t)}{dt}$$

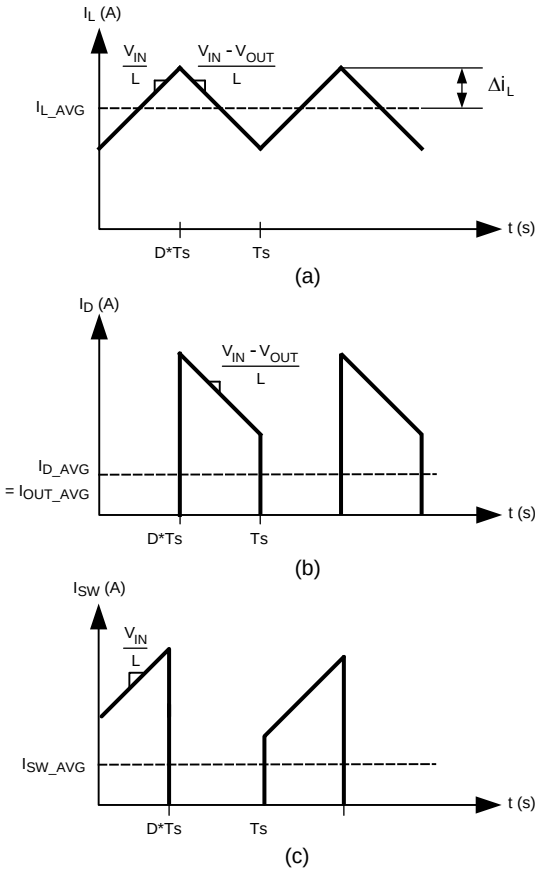


Figure 30. a. Inductor current b. Diode current c. Switch current

If $V_L(t)$ is constant, $di_L(t)/dt$ must be constant. Hence, for a given input voltage and output voltage, the current in the inductor changes at a constant rate.

The important quantities in determining a proper inductance value are I_L (the average inductor current) and Δi_L (the inductor current ripple difference between the peak inductor current and the average inductor current). If Δi_L is larger than I_L, the inductor current will drop to zero for a portion of the cycle and the converter will operate in discontinuous conduction mode. If Δi_L is smaller than I_L, the inductor current will stay above zero and the converter will operate in continuous conduction mode. All the analysis in this datasheet assumes operation in continuous conduction mode. To operate in continuous conduction mode, the following conditions must be met:

$$I_L > \Delta i_L$$

$$\frac{I_{OUT}}{1-D} > \frac{DV_{IN}}{2f_S L}$$

$$L > \frac{D(1-D)V_{IN}}{2I_{OUT}f_S}$$

Choose the minimum I_{OUT} to determine the minimum L. A common choice is to set (2 x Δi_L) to 30% of I_L. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter,

$$I_L = \frac{I_{OUT}}{1-D}$$

$$I_{L\_peak} = I_L(max) + \Delta i_L(max)$$

A core size with ratings higher than these values should be chosen. If the core is not properly rated, saturation will dramatically reduce overall efficiency.

The LM3481 can be set to switch at very high frequencies. When the switching frequency is high, the converter can operate with very small inductor values. With a small inductor value, the peak inductor current can be extremely higher than the output currents, especially under light load conditions.

The LM3481 senses the peak current through the switch. The peak current through the switch is the same as the peak current calculated above.

Programming the Output Voltage and Output Current

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in Figure 31. The resistors are selected such that the voltage at the feedback pin is 1.275V. R_{F1} and R_{F2} can be selected using the equation,

$$V_{OUT} = 1.275 \left(1 + \frac{R_{F1}}{R_{F2}}\right)$$

A 100 pF capacitor may be connected between the feedback and ground pins to reduce noise.

The maximum amount of current that can be delivered at the output can be controlled by the sense resistor, R_{SEN}. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE}. Limits for V_{SENSE} have been specified in the electrical characteristics section. This can be expressed as:

$$I_{sw(peak)} \times R_{SEN} = V_{SENSE} - D \times V_{SL}$$

The peak current through the switch is equal to the peak inductor current.

$$I_{sw(peak)} = I_L(max) + \Delta i_L$$

Therefore for a boost converter

$$I_{sw(peak)} = \frac{I_{OUT(max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}$$

Combining the two equations yields an expression for R_{SEN}

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SL})}{\left[\frac{I_{OUT(max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}\right]}$$

Evaluate R_{SEN} at the maximum and minimum V_{IN} values and choose the smallest R_{SEN} calculated.

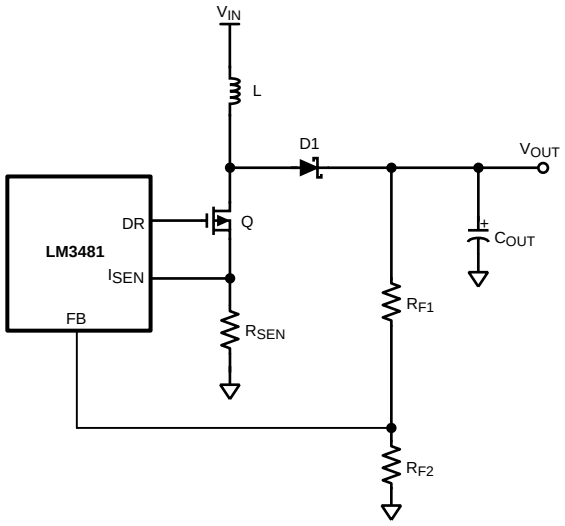


Figure 31. Adjusting the Output Voltage

Current Limit with Additional Slope Compensation

If an external slope compensation resistor is used (see Figure 22) the internal control signal will be modified and this will have an effect on the current limit.

If R_{SL} is used, then this will add to the existing slope compensation. The command voltage, V_{CS}, will then be given by:

$$V_{CS} = V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})$$

Where V_{SENSE} is a defined parameter in the electrical characteristics section and ΔV_{SL} is the additional slope compensation generated as discussed in the Slope Compensation Ramp section. This changes the equation for R_{SEN} to:

$$R_{SEN} = \frac{V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})}{\frac{I_{OUT(max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}}$$

Note that since $\Delta V_{SL} = R_{SL} \times K$ as defined earlier, R_{SL}can be used to provide an additional method for setting the current limit. In some designs R_{SL} can also be used to help filter noise to keep the I_{SEN} pin quiet.

Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than the inductor peak current. The peak diode current can be calculated using the formula:

$$I_{D(Peak)} = [I_{OUT} / (1-D)] + \Delta i_L$$

In the above equation, I_{OUT} is the output current and Δi_L has been defined in Figure 30.

The peak reverse voltage for a boost converter is equal to the regulator output voltage. The diode must be capable of handling this peak reverse voltage. To improve efficiency, a low forward drop Schottky diode is recommended.

Power MOSFET Selection

The drive pin, DR, of the LM3481 must be connected to the gate of an external MOSFET. In a boost topology, the drain of the external N-Channel MOSFET is connected to the inductor and the source is connected to the ground. The drive pin voltage, V_{DR}, depends on the input voltage (see typical performance characteristics). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub-logic level MOSFET should be used.

The selected MOSFET directly controls the efficiency. The critical parameters for selection of a MOSFET are:

1. Minimum threshold voltage, $V_{TH(MIN)}$
2. On-resistance, $R_{DS(ON)}$
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}
5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and ac switching or transition losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, P_{COND}, is the I^2R loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND(MAX)} = \left(\frac{I_{OUT(max)}}{1 - D_{MAX}}\right)^2 D_{MAX} R_{DS(ON)}$$

where D_{MAX} is the maximum duty cycle.

$$D_{MAX} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)$$

At high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often, the individual MOSFET datasheet does not give enough information to yield a useful result. The following formulas give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_{Lmax} \times V_{out}}{2} \times f_{SW} \times (t_{LH} + t_{HL})$$

$$t_{LH} = \left(Qgd + \frac{Qgs}{2}\right) \times \frac{R_{Gate}}{V_{DR} - Vgs_{th}}$$

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular, as shown in Figure 30. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta i_L / \sqrt{3} = \left(\frac{(V_{OUT} - V_{IN})V_{IN}}{\sqrt{12}\, V_{OUT} L f_S}\right)$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 100 µF to 200 µF. If a value lower than 100 µF is used, then problems with impedance interactions or switching noise can affect the LM3481. To improve performance, especially with V_{IN} below 8V, it is recommended to use a 20Ω resistor at the input to provide a RC filter. This resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see Figure 32). A 0.1 µF or 1 µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

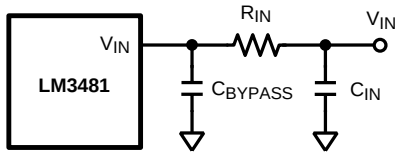


Figure 32. Reducing IC Input Noise

Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum rms current. The rms current in the output capacitor is:

$$I_{COUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}^2 \frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]}$$

Where

$$\Delta i_L = \frac{DV_{IN}}{2Lf_S}$$

and D, the duty cycle is equal to $(V_{OUT} - V_{IN})/V_{OUT}$.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output.

Driver Supply Capacitor Selection

A good quality ceramic bypass capacitor must be connected from the V_{CC} pin to the PGND pin for proper operation. This capacitor supplies the transient current required by the internal MOSFET driver, as well as filtering the internal supply voltage for the controller. A value of between 0.47µF and 4.7µF is recommended.

Layout Guidelines

Good board layout is critical for switching controllers such as the LM3481. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted Ldi/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The current sensing circuit in current mode devices can be easily effected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. Although the LM3481 has 250 ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time.

The most important layout rule is to keep the AC current loops as small as possible. Figure 33 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. They are the most critical ones since current is changing in very short time periods. The dotted lined traces of the bottom schematic are the once to make as short as possible.

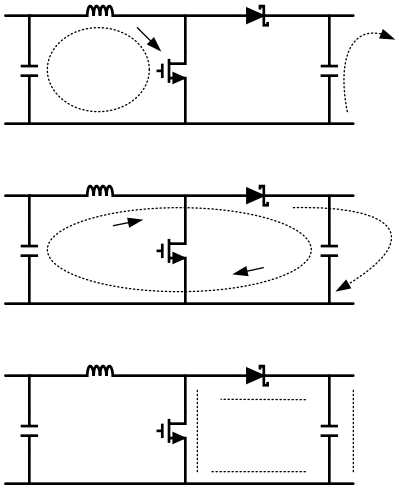


Figure 33. Current Flow In A Boost Application

The PGND and AGND pins have to be connected to the same ground very close to the IC. To avoid ground loop currents attach all the grounds of the system only at one point.

A ceramic input capacitor should be connected as close as possible to the Vin pin and grounded close to the GND pin.

For a layout example please see Application Note 1204 (SNVA042). For more information about layout in switch mode power supplies please refer to Application Note 1229 (SNVA054).

Compensation

For detailed explanation on how to select the right compensation components to attach to the compensation pin for a boost topology please see Application Note 1286 (SNVA067). When calculating the Error Amplifier DC gain, A_{EA}, R_{OUT} = 152 kΩ for the LM3481.

DESIGNING SEPIC USING LM3481

Since the LM3481 controls a low-side N-Channel MOSFET, it can also be used in SEPIC (Single Ended Primary Inductance Converter) applications. An example of SEPIC using the LM3481 is shown in Figure 34. As shown in Figure 34, the output voltage can be higher or lower than the input voltage. The SEPIC uses two inductors to step-up or step-down the input voltage. The inductors L1 and L2 can be two discrete inductors or two windings of a coupled transformer since equal voltages are applied across the inductor throughout the switching cycle. Using two discrete inductors allows use of catalog magnetics, as opposed to a custom transformer. The input ripple can be reduced along with size by using the coupled windings of transformer for L1 and L2.

Due to the presence of the inductor L1 at the input, the SEPIC inherits all the benefits of a boost converter. One main advantage of SEPIC over a boost converter is the inherent input to output isolation. The capacitor C_S isolates the input from the output and provides protection against shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In a boost converter, the output can only fall to the input voltage minus a diode drop.

The duty cycle of a SEPIC is given by:

$$D = \frac{V_{OUT} + V_{DIODE}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}$$

In the above equation, V_Q is the on-state voltage of the MOSFET, Q1, and V_{DIODE} is the forward voltage drop of the diode.

Power MOSFET Selection

As in a boost converter, the parameters governing the selection of the MOSFET are the minimum threshold voltage, $V_{TH(MIN)}$, the on-resistance, $R_{DS(ON)}$, the total gate charge, Q_g, the reverse transfer capacitance, C_{RSS}, and the maximum drain to source voltage, $V_{DS(MAX)}$. The peak switch voltage in a SEPIC is given by:

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE}$$

The selected MOSFET should satisfy the condition:

$$V_{DS(MAX)} > V_{SW(PEAK)}$$

The peak switch current is given by:

$$I_{SWPEAK} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2}$$

Where ΔI_{L1} and ΔI_{L2} are the peak-to-peak inductor ripple currents of inductors L1 and L2 respectively.

The rms current through the switch is given by:

$$I_{SWRMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}\left(\Delta I_{L1} + \Delta I_{L2}\right) + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3}\right] D}$$

Power Diode Selection

The Power diode must be selected to handle the peak current and the peak reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is $V_{IN} + V_{OUT}$. Similar to the boost converter, the average diode current is equal to the output current. Schottky diodes are recommended.

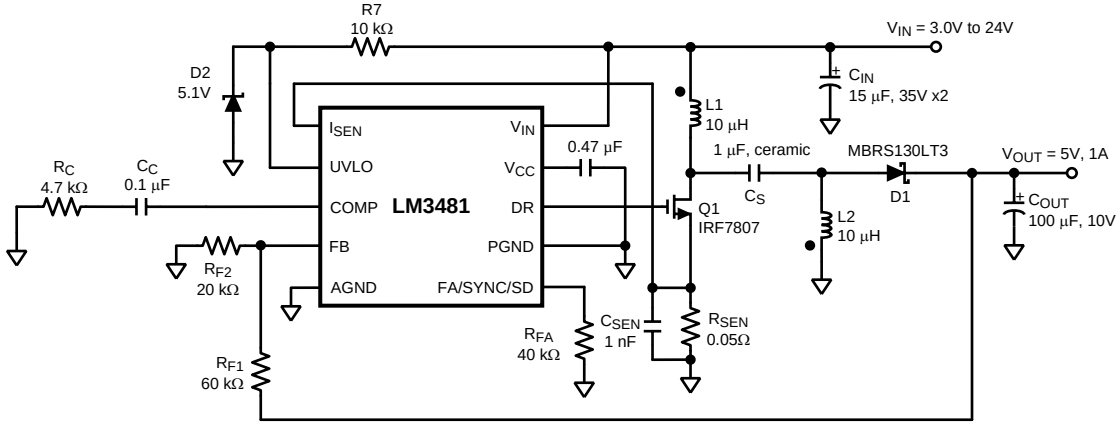


Figure 34. Typical SEPIC Converter

Selection of Inductors L1 and L2

Proper selection of the inductors L1 and L2 to maintain constant current mode requires calculations of the following parameters.

Average current in the inductors:

$$I_{L1AVE} = \frac{DI_{OUT}}{1-D}$$

$$I_{L2AVE} = I_{OUT}$$

Peak to peak ripple current, to calculate core loss if necessary:

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{(L1) f_S}$$

$$\Delta I_{L2} = \frac{(V_{IN} - V_Q)\, D}{(L2) f_S}$$

Maintaining the condition $I_L > \Delta I_L/2$ to ensure continuous conduction mode yields the following minimum values for L1 and L2:

$$L1 > \frac{(V_{IN} - V_Q)(1-D)}{2 I_{OUT} f_S}$$

$$L2 > \frac{(V_{IN} - V_Q) D}{2 I_{OUT} f_S}$$

Peak current in the inductor, to ensure the inductor does not saturate:

$$I_{L1PK} = \frac{D I_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2}$$

$$I_{L2PK} = I_{OUT} + \frac{\Delta I_{L2}}{2}$$

I_{L1PK} must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended value to reduce input ripple and output ripple. However, once ΔI_{L1} is less than 20% of I_{L1AVE}, the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommendation, ΔI_{L2} can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) \text{ESR}$$

where ESR is the effective series resistance of the output capacitor.

If L1 and L2 are wound on the same core, then L1 = L2 = L. All the equations above will hold true if the inductance is replaced by 2L. A good choice for transformer with equal turns is Coiltronics CTX series Octopack.

Sense Resistor Selection

The peak current through the switch, I_{SWPEAK}, can be adjusted using the current sense resistor, R_{SEN}, to provide a certain output current. Resistor R_{SEN} can be selected using the formula:

$$R_{SEN} = \frac{V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})}{I_{SWPEAK}}$$

SEPIC CAPACITOR SELECTION

The selection of SEPIC capacitor, C_S, depends on the rms current. The rms current of the SEPIC capacitor is given by:

$$I_{CSRMS} = \sqrt{I_{SWRMS}^2 + \left(I_{L1PK}^2 - I_{L1PK} \Delta I_{L1} + \Delta I_{L1}^2 \right)(1-D)}$$

The SEPIC capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the rms current through the capacitor is small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum capacitors are the best choice for SMT, having high rms current ratings relative to size. Ceramic capacitors could be used, but the low C values will tend to cause larger changes in voltage across the capacitor due to the large currents, and high C value ceramics are expensive. Electrolytics work well for through hole applications where the size required to meet the rms current rating can be accommodated. There is an energy balance between C_S and L1, which can be used to determine the value of the capacitor. The basic energy balance equation is:

$$\frac{1}{2}C_S\Delta V_S^2 = \frac{1}{2}(L1)\Delta I_{L1}^2$$

Where

$$\Delta V_S = \left(\frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}\right)\frac{I_{OUT}}{f_S C_S}$$

is the ripple voltage across the SEPIC capacitor, and

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{(L1) f_S}$$

is the ripple current through the inductor L1. The energy balance equation can be solved to provide a minimum value for C_S:

$$C_S \geq L1\,\frac{I_{OUT}^2}{(V_{IN} - V_Q)^2}$$

INPUT CAPACITOR SELECTION

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta I_{L1}/\sqrt{12} = \frac{D}{2\sqrt{3}}\left(\frac{V_{IN} - V_Q}{(L1) f_S}\right)$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a SEPIC application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 100 µF to 200 µF. If a value lower than 100 µF is used, then problems with impedance interactions or switching noise can affect the LM3481. To improve performance, especially with V_{IN} below 8V, it is recommended to use a 20Ω resistor at the input to provide a RC filter. This resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see Figure 32). A 0.1 µF or 1 µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

OUTPUT CAPACITOR SELECTION

The output capacitor of the SEPIC sees very large ripple currents similar to the output capacitor of a boost converter. The rms current through the output capacitor is given by:

$$I_{RMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}\,(\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3}\right](1\text{-}D) - I_{OUT}^2}$$

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output for low ripple.

OTHER APPLICATION CIRCUITS

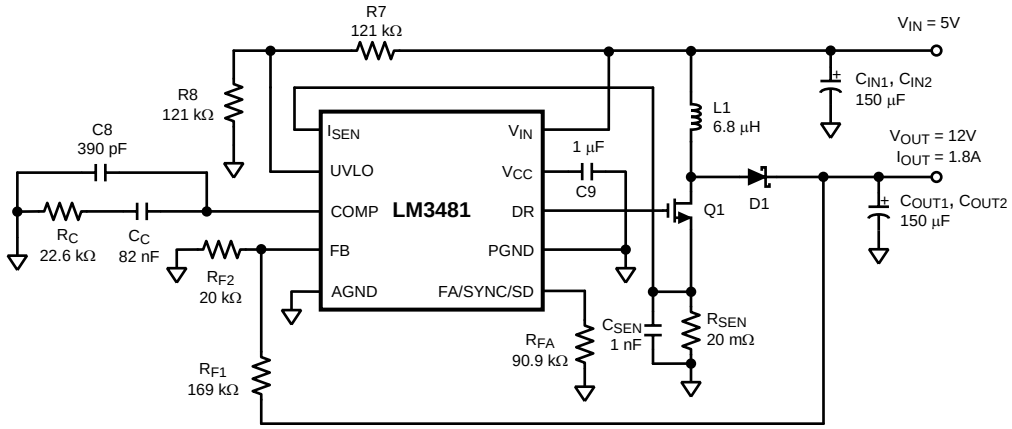


Figure 35. Typical High Efficiency Step-Up (Boost) Converter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3481MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SJPB	Samples
LM3481MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SJPB	Samples
LM3481QMM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SUAB	Samples
LM3481QMMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SUAB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF LM3481, LM3481-Q1 :

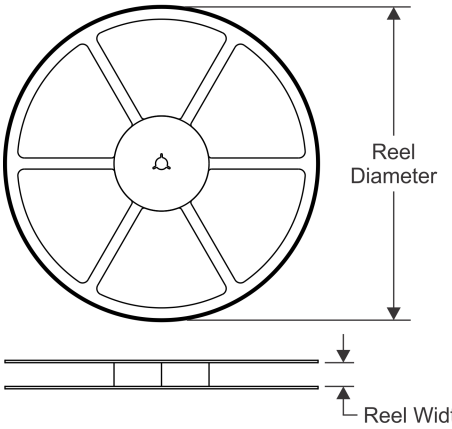
- Catalog: LM3481
- Automotive: LM3481-Q1

NOTE: Qualified Version Definitions:

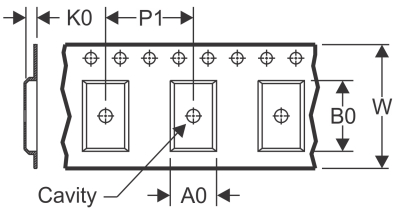
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

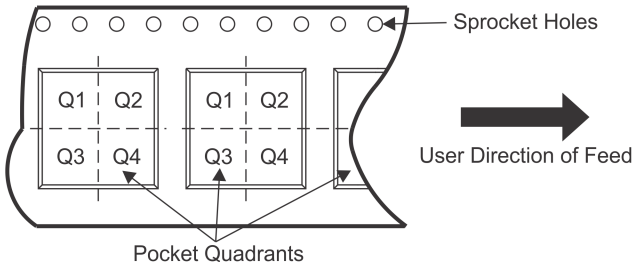


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

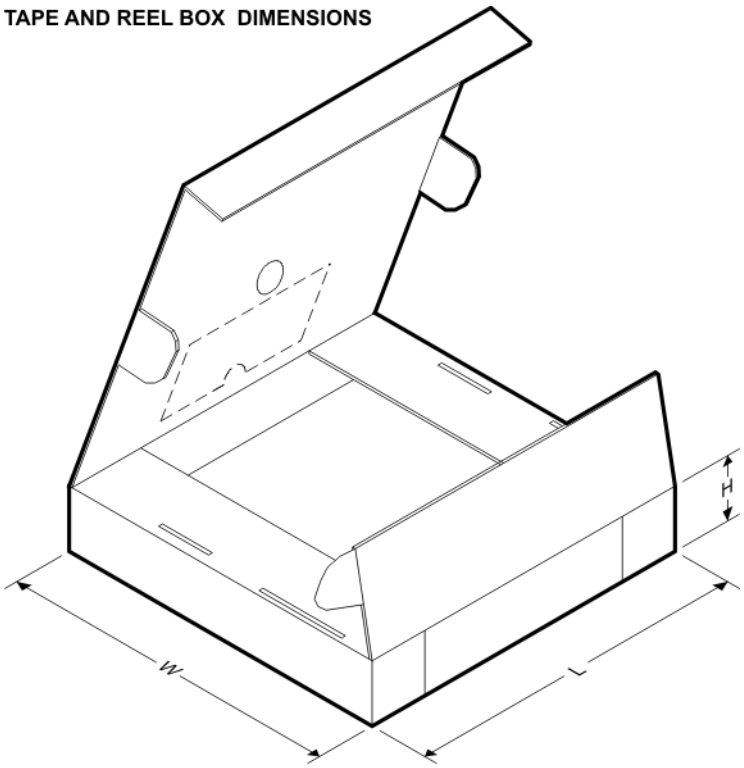
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3481MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3481MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3481QMM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3481QMMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

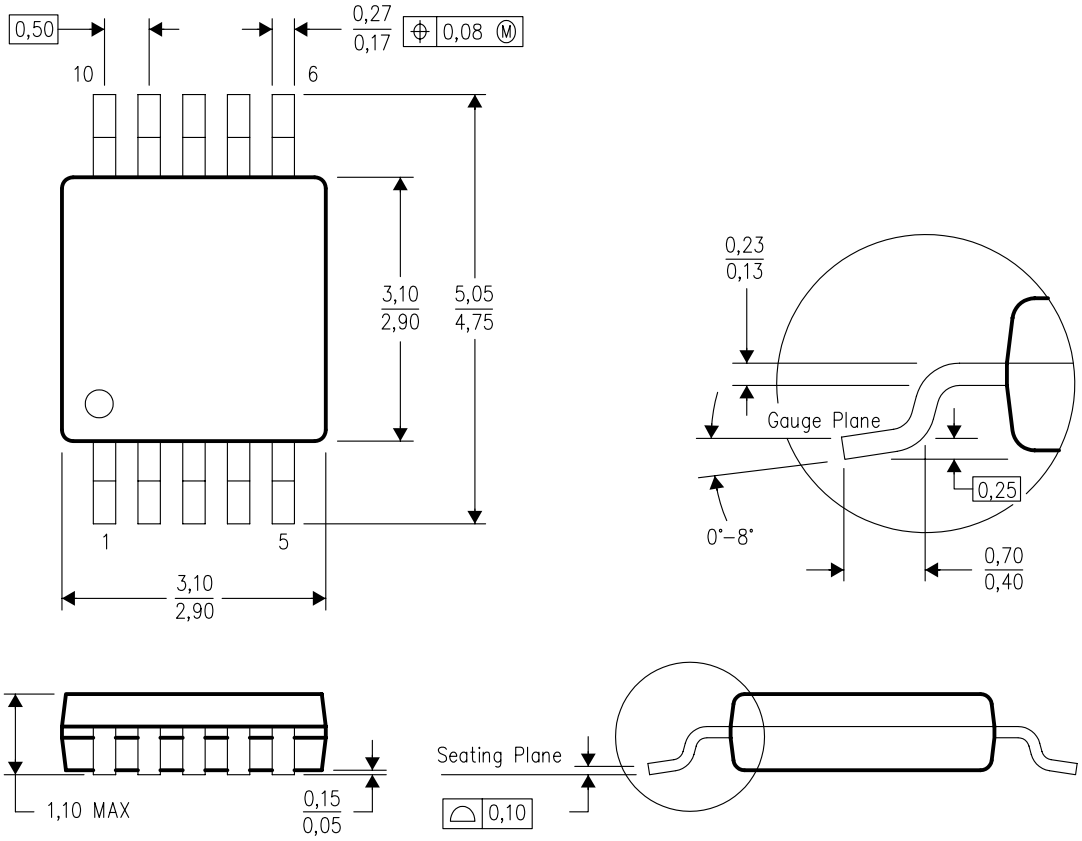
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3481MM/NOPB	VSSOP	DGS	10	1000	203.0	190.0	41.0
LM3481MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM3481QMM/NOPB	VSSOP	DGS	10	1000	203.0	190.0	41.0
LM3481QMMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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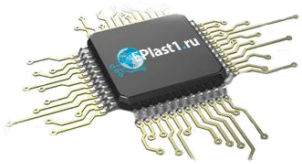

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