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FDMS86500DC

N-Channel Dual Cool™ 56 Power Trench® MOSFET 60 V, 108 A, 2.3 mΩ

Features

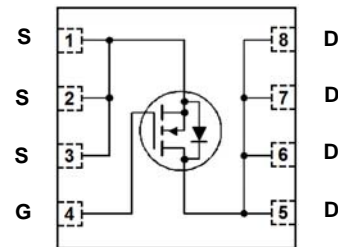
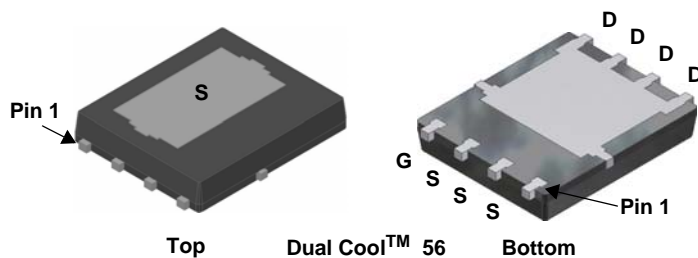
- Dual Cool™ Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 2.3 mΩ at $V_{GS} = 10$ V, $I_D = 29$ A
- Max $r_{DS(on)}$ = 3.3 mΩ at $V_{GS} = 8$ V, $I_D = 24$ A
- High performance technology for extremely low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
V_{DS}	Drain to Source Voltage		60	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	-Continuous $T_C = 25$ °C	108	A
		-Continuous $T_A = 25$ °C (Note 1a)	29	
		-Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	317	mJ
P_D	Power Dissipation	$T_C = 25$ °C	125	W
		$T_A = 25$ °C (Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Conditions	Rated Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.8	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86500	FDMS86500DC	Dual Cool™ 56	13"	12 mm	3000 units

FDMS86500DC N-Channel Dual Cool™ 56 Power Trench® MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		30		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.5	3.7	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-12		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 29\ \text{A}$		1.9	2.3	m Ω
		$V_{GS} = 8\ \text{V}$, $I_D = 24\ \text{A}$		2.4	3.3	
		$V_{GS} = 10\ \text{V}$, $I_D = 29\ \text{A}$, $T_J = 125\text{ }^\circ\text{C}$		3.0	3.7	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 29\ \text{A}$		98		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		5775	7680	pF
C_{oss}	Output Capacitance			1605	2680	pF
C_{rss}	Reverse Transfer Capacitance			48	95	pF
R_g	Gate Resistance		0.1	1	3	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\ \text{V}$, $I_D = 29\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		35	56	ns
t_r	Rise Time			25	40	ns
$t_{d(off)}$	Turn-Off Delay Time			34	54	ns
t_f	Fall Time			8.2	17	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$		76	107
	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $8\ \text{V}$	$V_{DD} = 30\ \text{V}$ $I_D = 29\ \text{A}$	62	87	nC
Q_{gs}	Total Gate Charge			31		nC
Q_{gd}	Gate to Drain "Miller" Charge			15		nC

Drain-Source Diode Characteristics

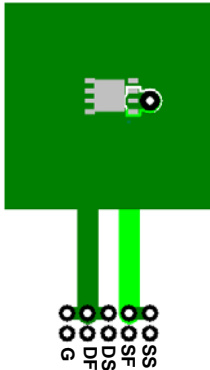
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.7\ \text{A}$ (Note 2)		0.71	1.2	V
		$V_{GS} = 0\ \text{V}$, $I_S = 29\ \text{A}$ (Note 2)		0.79	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 29\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		59	95	ns
Q_{rr}	Reverse Recovery Charge			46	74	nC

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.8	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	13	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 38 $^{\circ}\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. 81 $^{\circ}\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Starting $T_J = 25^{\circ}\text{C}$; N-ch: $L = 0.3 \text{ mH}$, $I_{AS} = 46 \text{ A}$, $V_{DD} = 54 \text{ V}$, $V_{GS} = 10 \text{ V}$.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

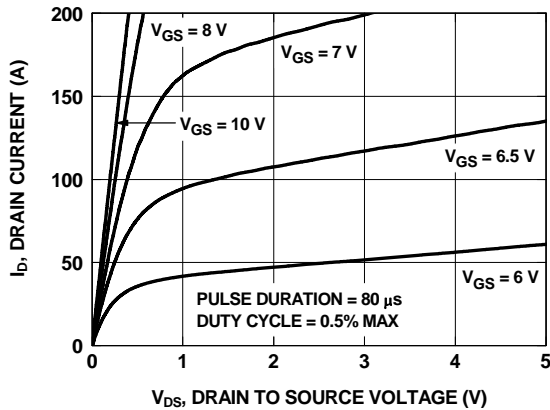


Figure 1. On-Region Characteristics

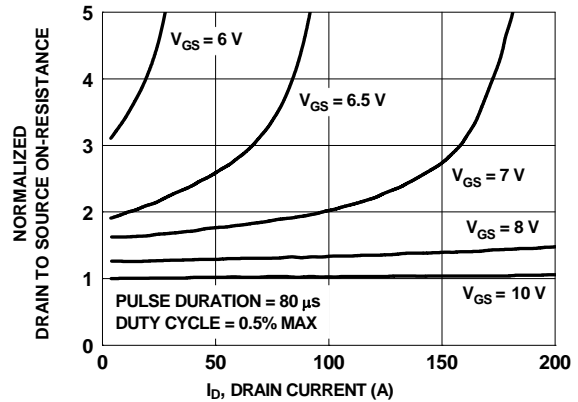


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

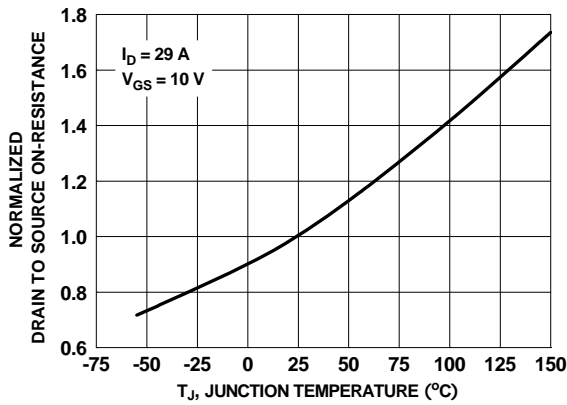


Figure 3. Normalized On-Resistance vs Junction Temperature

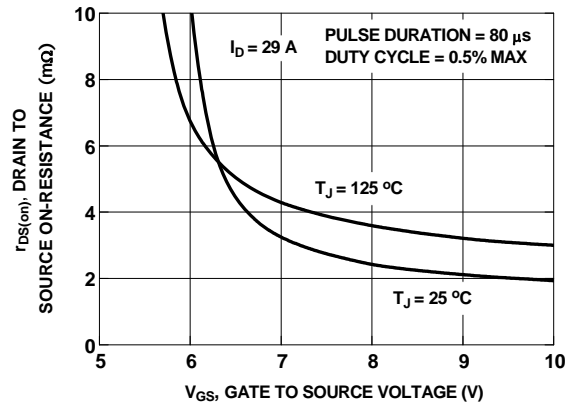


Figure 4. On-Resistance vs Gate to Source Voltage

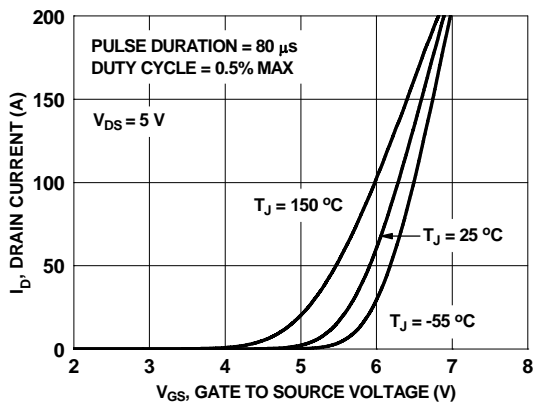


Figure 5. Transfer Characteristics

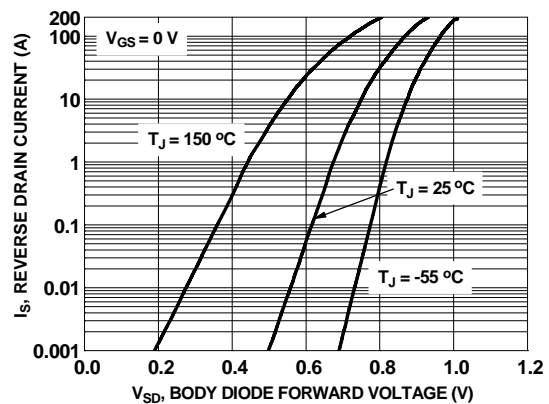


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

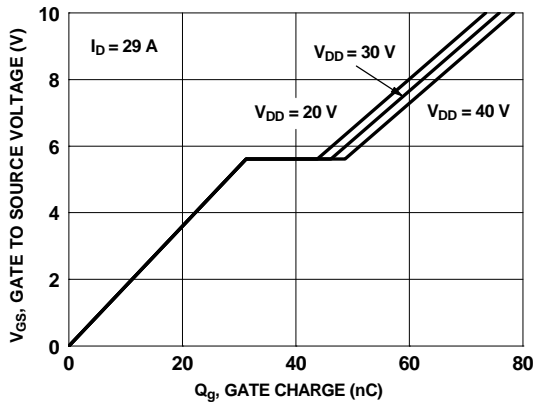


Figure 7. Gate Charge Characteristics

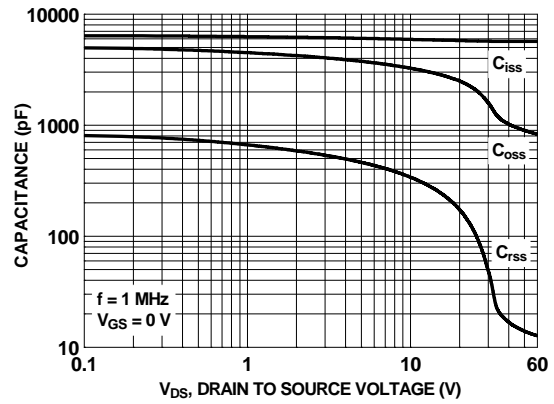


Figure 8. Capacitance vs Drain to Source Voltage

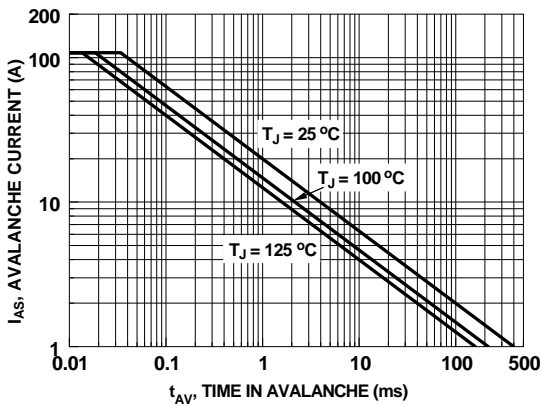


Figure 9. Unclamped Inductive Switching Capability

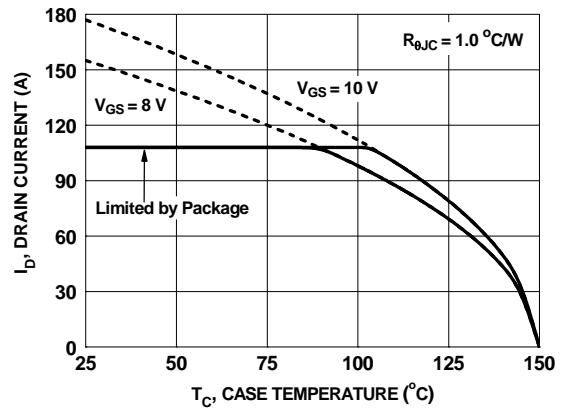


Figure 10. Maximum Continuous Drain Current vs Case Temperature

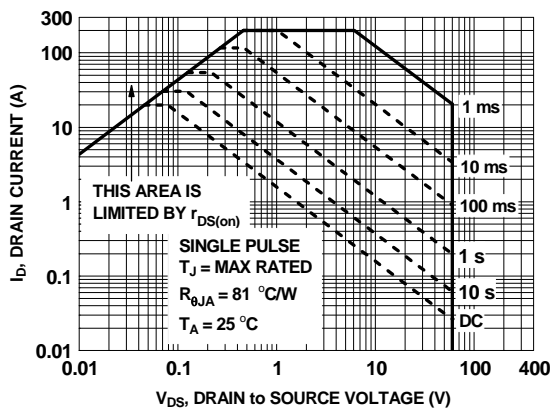


Figure 11. Forward Bias Safe Operating Area

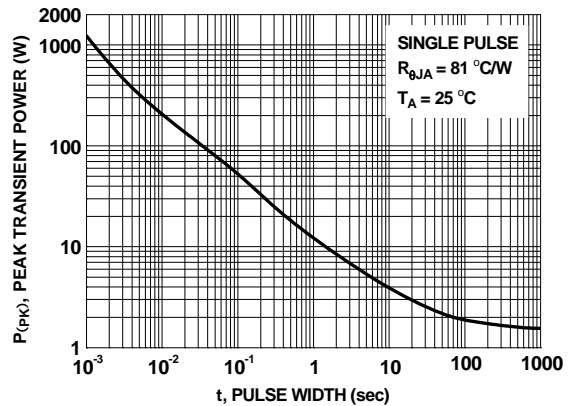


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

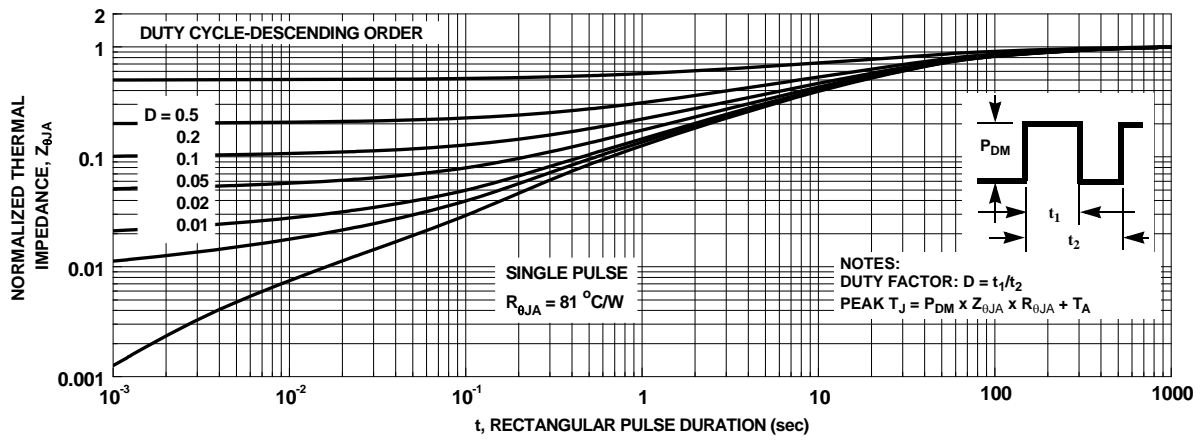
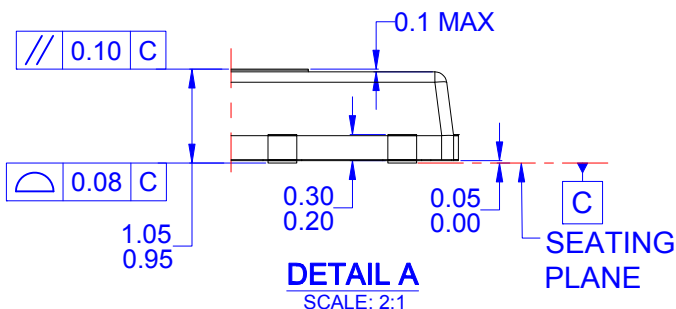
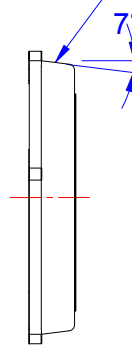
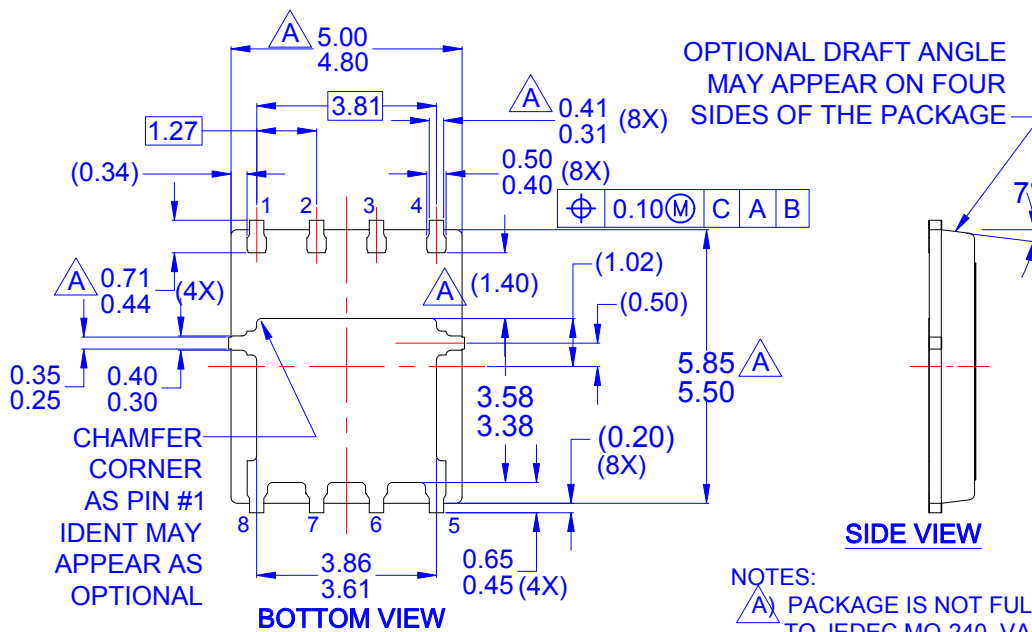
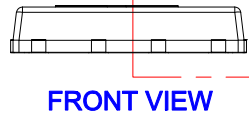
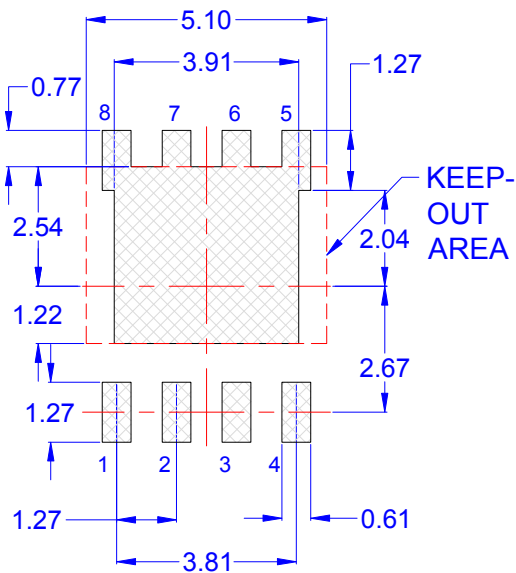
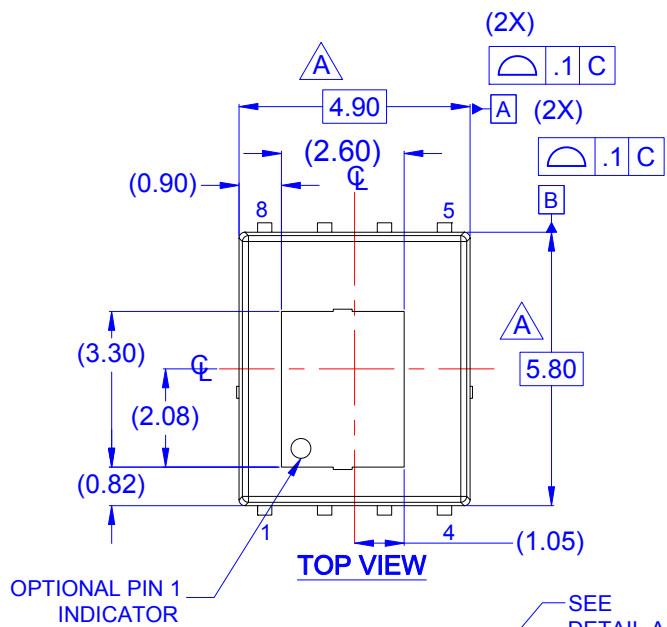


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



- NOTES:
- A) PACKAGE IS NOT FULLY COMPLIANT TO JEDEC MO-240, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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