Single-chip Type with Built-in FET Switching Regulator Series

Output 1.5A or Less High Efficiency Step-down Switching Regulator with Built-in Power MOSFET

BD9151MUV

No.09027EAT11

●Description

ROHM's high efficiency dual step-down switching regulator BD9151MUV is a power supply designed to produce a low voltage including 1.8 volts or 1.2 volts from 2.8 volts to 5.0 volts power supply line. Reset circuits of input power supply voltage and external Pch MOSFET gate controller are incorporated. Offers high efficiency with our original pulse skip control technology and synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

1) Offers fast transient response with current mode PWM control system.
2) Offers highly efficiency for all load range with synchronous rectifier (Pch/Nch FET) and SLLM™ (Simple Light Load Mode)
3) Incorporates soft-start function.
4) Incorporates Thermal / ULVO protection functions.
5) Incorporates thermal protection and short-current protection circuit with timer latch function. .
6) Incorporates shutdown function Icc=0μA(Typ.)
7) Incorporates reset function
8) Incorporates Pch MOSFET gate controller
9) Employs small surface mount package : VQFN020V4040

●Applications

Power supply for LSI including DSP, Micro computer and ASIC

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Vcc Voltage	AVCC	-0.3～+7[*1]	V
	PVcc	-0.3～+7[*1]	V
EN Voltage	VEN	-0.3～+7	V
SW Voltage	VSW1	-0.3～+7	V
	VSW2	-0.3～+7	V
Power Dissipation	Pd1	0.34[*2]	W
	Pd2	0.70[*3]	W
	Pd3	2.21[*4]	W
	Pd4	3.56[*5]	W
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Pd, ASO and Tj=150℃ should not be exceeded.
*2 IC only
*3 1-layer. mounted on a 74.2mm×74.2mm×1.6mm glass-epoxy board, occupied area by copper foil : 10.29mm^2
*4 4-layer. mounted on a 74.2mm×74.2mm×1.6mm glass-epoxy board, occupied area by copper foil : 10.29mm^2, 2-3 layers 5505 mm^2
*5 4-layer. mounted on a 74.2mm×74.2mm×1.6mm glass-epoxy board, occupied area by copper foil : 5505mm^2, in each layers

●Operating conditions (Ta=-40～+85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vcc Voltage	AVCC、PVCC	2.8	3.3	5.5	V
EN Voltage	VEN	0	-	5.5	V
SW Average Output Current	ISW1	-	-	0.4[*6]	A
	ISW2	-	-	0.8[*6]	A

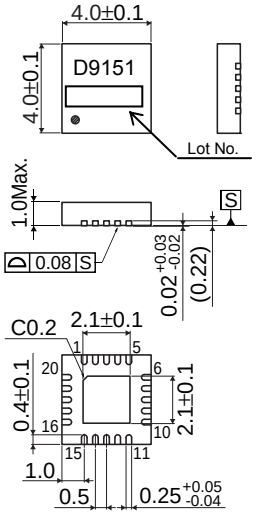
*6 Pd and ASO should not be exceeded.

●Electrical Characteristics

◎(Unless otherwise noted, Ta=25℃, AVCC=PVCC=3.3V, EN=AVCC)

Parameter	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX		
Standby Current	ISTB	-	0	10	μA	EN=0V
Bias Current	ICC	-	400	800	μA	
EN Low Voltage	VENL	-	GND	0.8	V	In standby mode
EN High Voltage	VENH	2	Vcc	-	V	In active mode
EN Input Current	IEN	-	1	10	μA	VEN=2V
Oscillation Frequency	FOSC	0.8	1.0	1.2	MHz	
Pch FET ON Resistance	RONP1	-	0.27	0.46	Ω	AVCC = PVCC =3.3V
	RONP2	-	0.18	0.30	Ω	AVCC = PVCC =3.3V
Nch FET ON Resistance	RONN1	-	0.27	0.46	Ω	AVCC = PVCC =3.3V
	RONN2	-	0.18	0.30	Ω	AVCC = PVCC =3.3V
ITH Sink Current 1	ITHSI1	10	20	-	μA	VFB1=2.0V
ITH Source Current 1	ITHSO1	10	20	-	μA	VFB 1=1.6V
ITH Sink Current 2	ITHSI2	10	20	-	μA	VFB 2=1.4V
ITH Source Current 2	ITHSO2	10	20	-	μA	VFB 2=1.0V
FB Reference Voltage 1	FB1	1.773	1.800	1.827	V	±1.5%
FB Reference Voltage 2	FB2	1.182	1.200	1.218	V	±1.5%
UVLO Threshold Voltage	VUVLOL	2.4	2.5	2.6	V	AVCC =3.3→0V
UVLO Release Voltage	VUVLOH	2.45	2.6	2.8	V	AVCC =0→3.3V
Reset Threshold Voltage	PG1	2.74	2.87	3.00	V	AVCC =3.3V→0V
Reset Release Voltage	PG2	2.84	2.97	3.10	V	AVCC =0V→3.3V
Reset ON resistance	RONPG	-	140	240	Ω	
Reset Delay	TPG	8	16	32	ms	
MONI Discharge Resistance	RMONI	-	110	190	Ω	AVCC =3.3V
PGATEB Sink Current	IPGATEB	1.5	4	6.5	uA	
Soft start time	TSS	0.25	0.5	1.0	ms	
Timer latch time	TLATCH	0.5	1.0	2.0	ms	In SCP/TSD operation
Output Short circuit Threshold Voltage	VSCP1	-	0.9	1.26	V	FB1=1.8→0V
	VSCP2	-	0.6	0.84	V	FB2=1.2→0V

●Top View



VQFN020V4040 (Unit :mm)

Fig.1 BD9151MUV TOP View

●Block Diagram

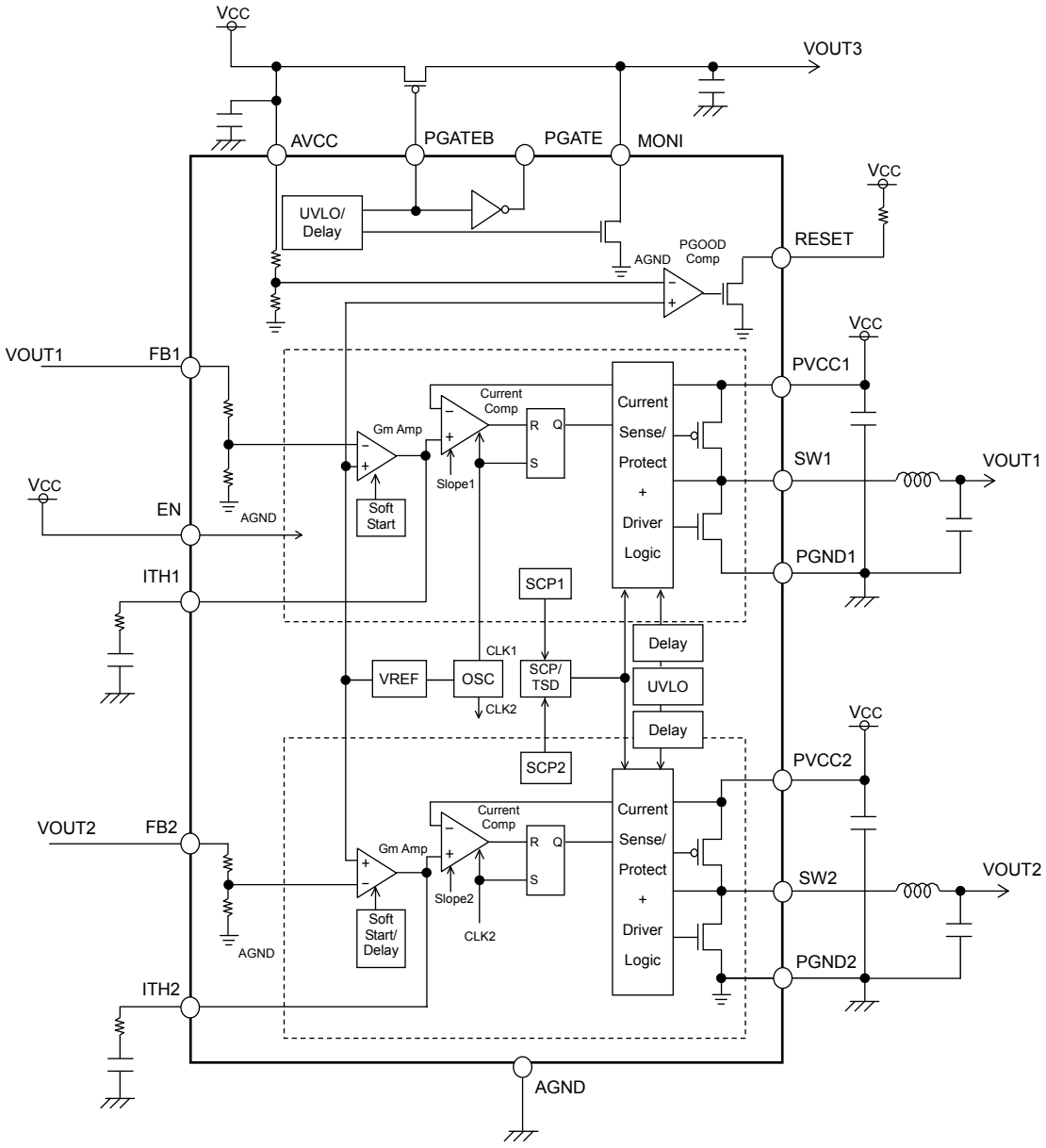


Fig.2 BD9151MUV Block Diagram

●Pin No. & function table

Pin No.	Pin name	PIN Function	Pin No.	Pin name	PIN Function
1	PGND2	Ch2 Low side source pin	11	AGND	Ground
2	PGND2	Ch2 Low side source pin	12	AVCC	Power supply input pin
3	PVCC2	Ch2 High side FET source pin	13	PGATEB	External Pch MOS Gate Drive pin (Low Active)
4	PVCC1	Ch1 High side FET source pin	14	PGATE	PGATEB reverse logic output signal (High Active)
5	PGND1	Ch1 Low side source pin	15	MONI	3.3V Output monitor pin
6	SW1	Ch1 Pch/Nch FET drain output pin	16	ITH2	Ch2 GmAmp output pin / Connected phase compensation capacitor
7	SW1	Ch1 Pch/Nch FET drain output pin	17	FB2	Ch2 output voltage detect pin
8	FB1	Ch1 output voltage detect pin	18	EN	Enable pin (High Active)
9	ITH1	Ch1 GmAmp output pin /Connected phase compensation capacitor	19	SW2	Ch2 Pch/Nch FET drain output pin
10	RESET	RESET Output pin	20	SW2	Ch2 Pch/Nch FET drain output pin

●Characteristics data【BD9151MUV】

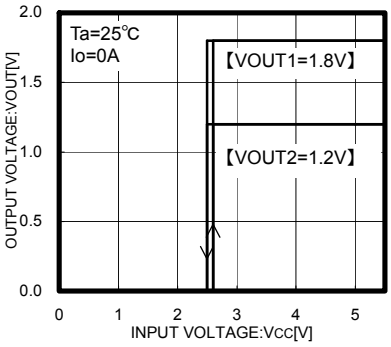


Fig.3 VCC – VOUT1,VOUT2

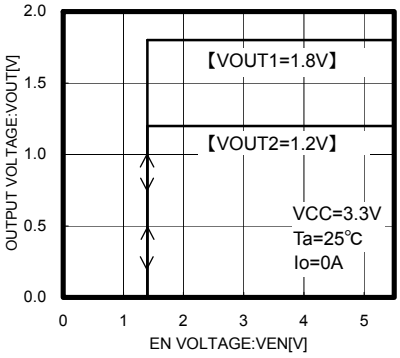


Fig.4 VEN - VOUT

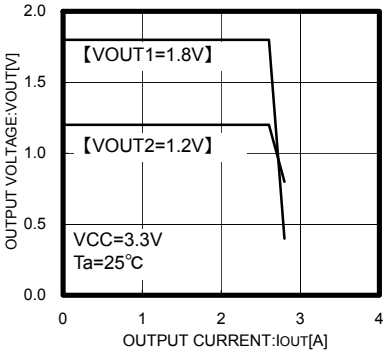


Fig.5 IOUT - VOUT

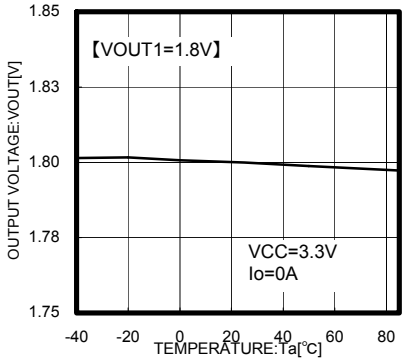


Fig. 6 Ta-VOUT1

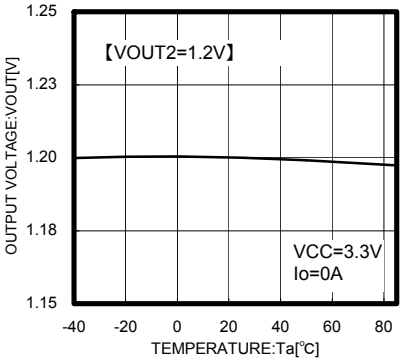


Fig. 7 Ta-VOUT1

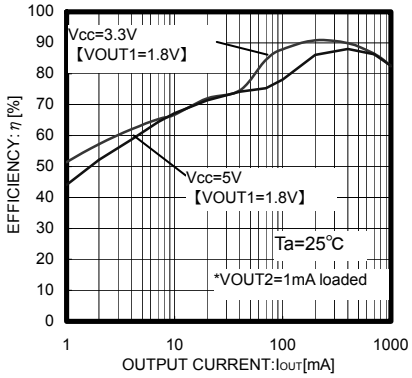


Fig.8 VOUT1 Efficiency

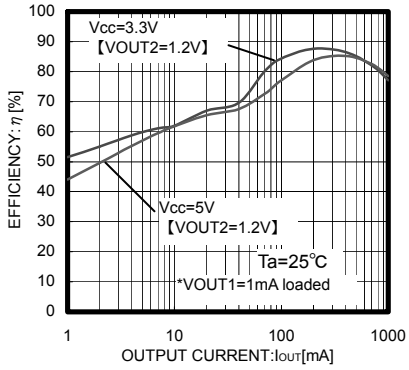


Fig.9 VOUT2 Efficiency

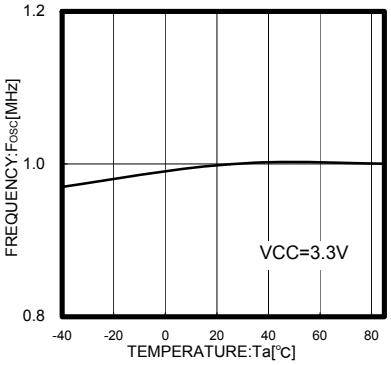


Fig.10 Ta- Fosc

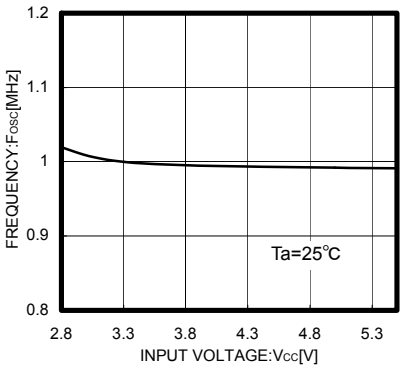


Fig.11 VCC-Fosc

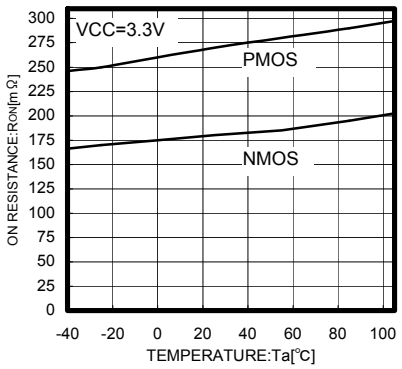


Fig.12 Ta – RONN, RONP

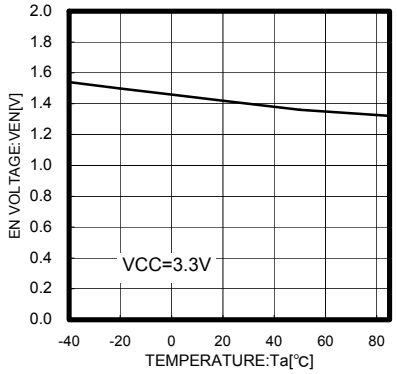


Fig.13 Ta－EN1,EN2

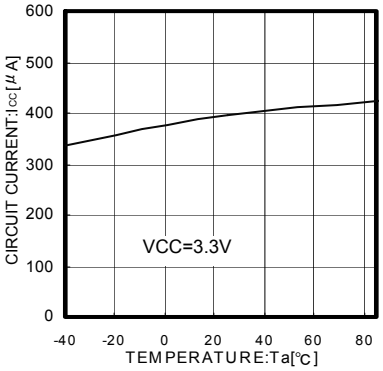


Fig.14 Ta－Icc

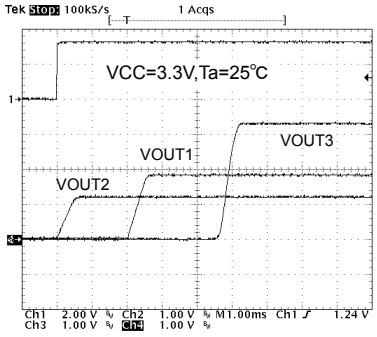


Fig.15 Soft start waveform
(Io1=0mA,Io2=0mA,Io3=0mA)

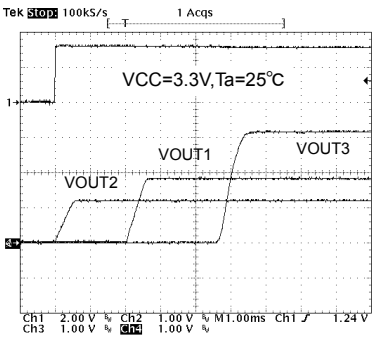


Fig.16 Soft start waveform
(Io1=400mA,Io2=800mA,Io3=600mA)

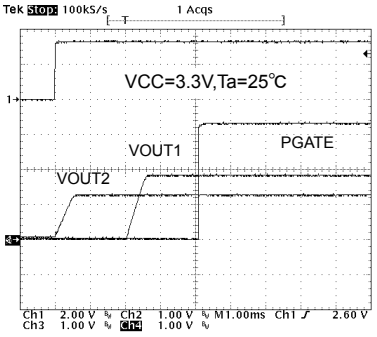


Fig.17 Soft start waveform
(Io1=0mA,Io2=0mA,PGATE)

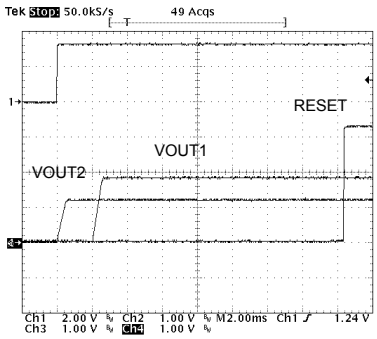


Fig.18 Soft start waveform
(Io1=0mA,Io2=0mA,RESET)

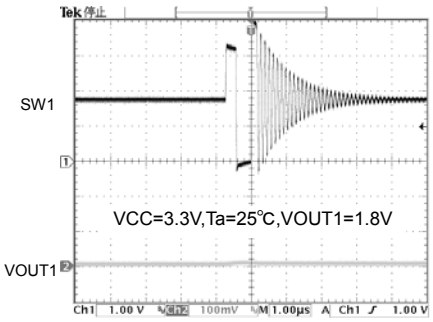


Fig.19 SW1 waveform
(Io=0mA)

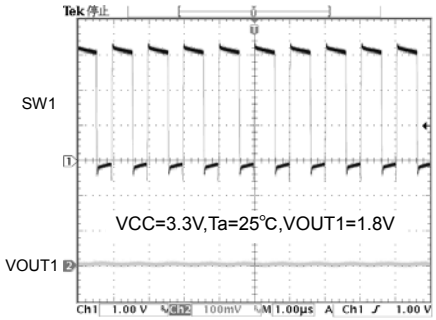


Fig.20 SW1 waveform
(Io=400mA)

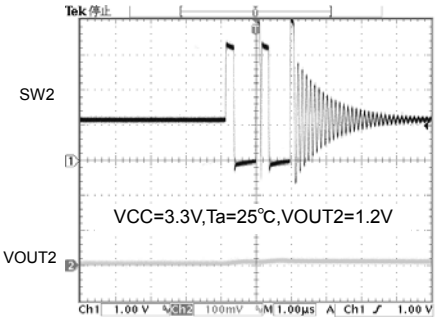


Fig.21 SW2 waveform
(Io=0mA)

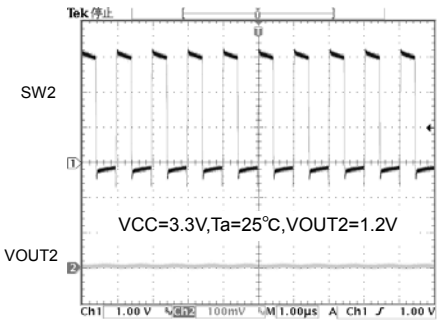


Fig.22 SW2 waveform
(Io=800mA)

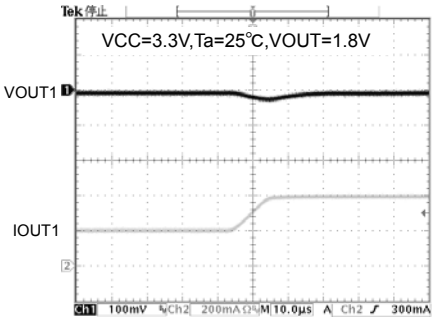


Fig.23 VOUT1 transient response
(Io=200mA→400mA / 10usec)

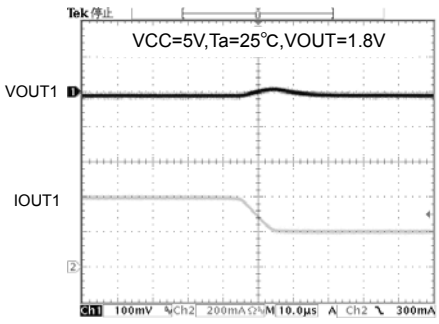


Fig.24 VOUT1 transient response
(Io=400mA→200mA/ 10usec)

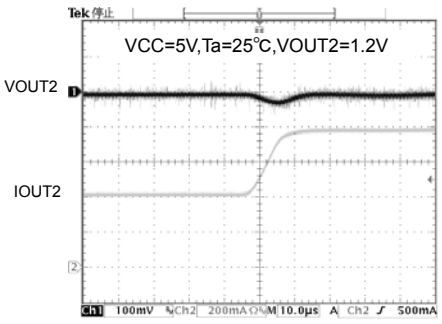


Fig.25 VOUT2 transient response
(Io=400mA→800mA/ 10usec)

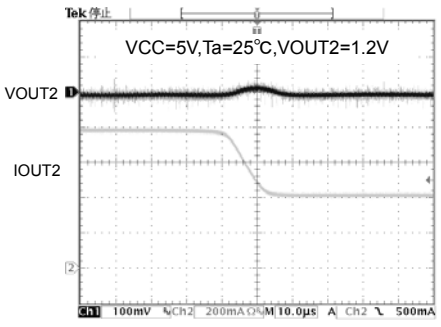


Fig.26 VOUT2 transient response
(Io=800mA→400mA/ 10usec)

●Operation

BD9151MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM™ (Simple Light Load Mode) operation for lighter load to improve efficiency.

○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 1 MHz. SET signal form OSC turns ON a high side MOS FET (while a low side MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the high side MOS FET (while a low side MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

・SLLM™ (Simple Light Load Mode) control

When the control mode is shifted from PWM for heavier load to the one for lighter load or vise versa, the switching pulse is designed to turn OFF with the device held operated in normal PWM control loop, which allows linear operation without voltage drop or deterioration in transient response during the mode switching from light load to heavy load or vise versa.
Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed that the RESET signal is held issued if shifted to the light load mode, with which the switching is tuned OFF and the switching pulses are thinned out under control. Activating the switching intermittently reduces the switching dissipation and improves the efficiency.

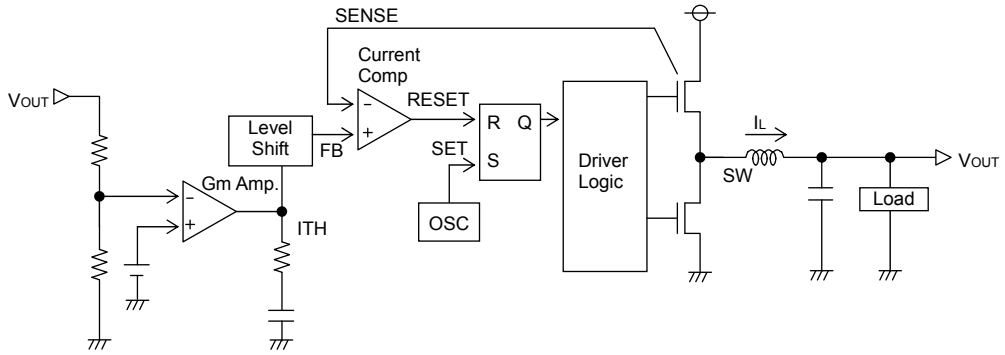


Fig.27 Diagram of current mode PWM control

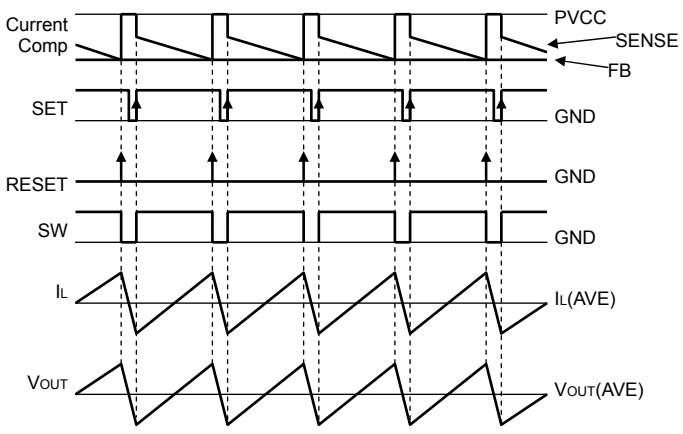


Fig.28 PWM switching timing chart

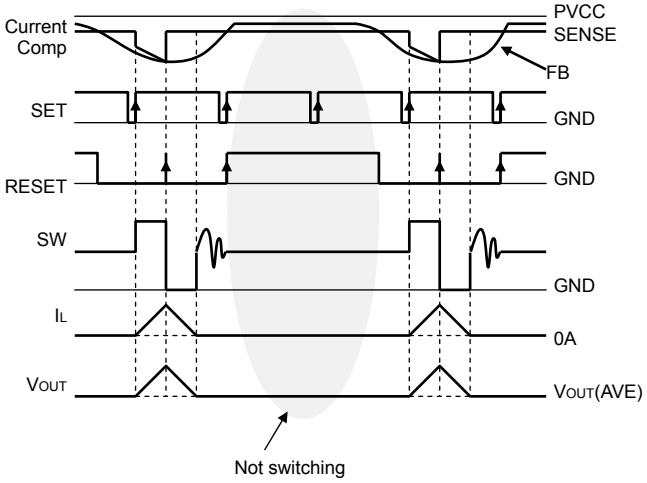
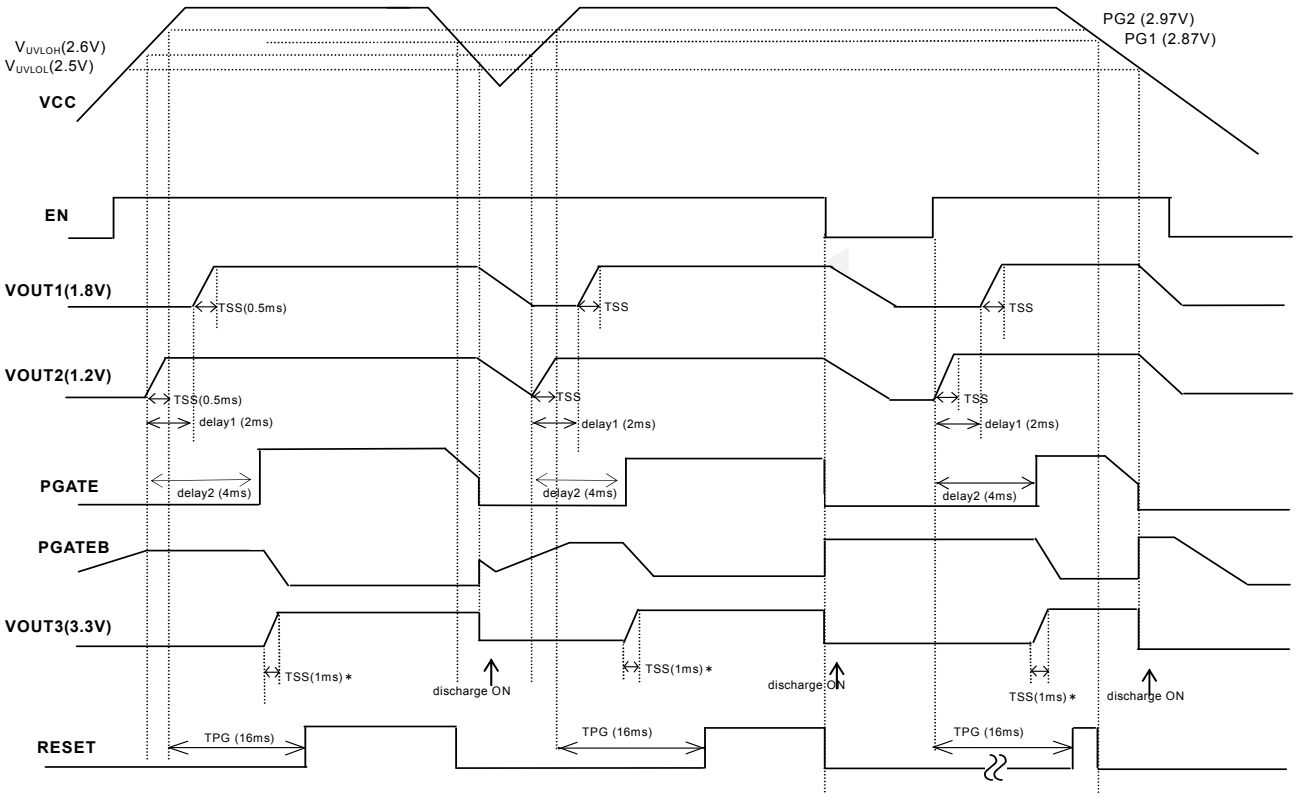


Fig.29 SLLM™ switching timing chart

●Description of operations

- Soft start function
  EN terminal shifted to “High” activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.
- Shutdown function
  With EN terminal shifted to “Low”, the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0μF (Typ.).
- UVLO function
  Detects whether the input voltage sufficient to secure the output voltage of BU9151MUV is supplied. And the hysteresis width of 100mV (Typ.) is provided to prevent output chattering. Each the outputs have UVLO. It is possible to set output sequence easy.
- Reset function
  When AVCC input voltage is over .2.97V (typ), after 16msec (typ.) delay, outputs RESET. The hysteresis is 100mV (Typ).
- Pch MOSFET gate controller function
  PGATEB pin has function to make FET active with steady current. With connecting Pch MOSFET gate, soft start turned to be ON.
- Discharge function
  MONI pin is open drain pin of Nch MOS. After 4msec (typ) delay from the time UVLO release, it turns to be OFF.
  By Low, UVLO detection of EN pin, Nch MOS becomes active and discharge the connection.
- External synchronous signal output function
  PGATE pin outputs High active after 4msec (Typ.) delay from the UVLO release.
- Start up sequence function
  BU9151MUV outputs output voltage 2ch (1.2V) after the UVLO release, and after 2msec(typ.) from the UVLO release, it outputs 1ch(1.8V), and the last, after 4msec from the UVLO release, PGATEB becomes active, and external Pch MOSFET will be ON, and outputs 3ch(VCC equivalent). During the OFF time, 3ch output is discharged by MONI pin, then 1ch output and 2ch output are naturally discharged.



*Starting time of VOUT3 TSS=1ms (when BD9151MUV is used) It depends on gate capacity when using Pch MOSFET

Fig.30 Soft start, Shut down, UVLO timing chart

・Short-current protection circuit with time latch function
Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time(T_{LATCH}) or more. The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

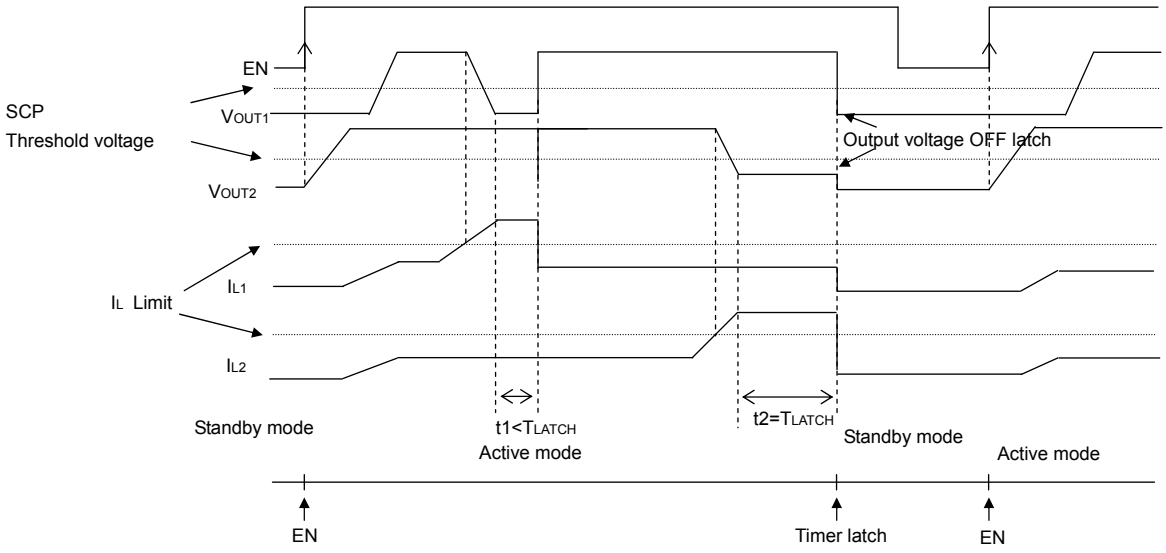


Fig.31 Timer latch short-current protection timing chart

●Switching regulator efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_D\alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:
1) ON resistance dissipation of inductor and FET : PD(I^2R)
2) Gate charge/discharge dissipation : PD(Gate)
3) Switching dissipation : PD(SW)
4) ESR dissipation of capacitor : PD(ESR)
5) Operating current dissipation of IC : PD(IC)

1)PD(I^2R)=$I_{OUT}^2 \times (R_{COIL}+R_{ON})$ (R_{COIL}[Ω] : DC resistance of inductor, R_{ON}[Ω] : ON resistance of FET, I_{OUT}[A] : Output current.)
2)PD(Gate)=Cgs × f × V (Cgs[F] : Gate capacitance of FET, f[H] : Switching frequency, V[V] : Gate driving voltage of FET)
3)PD(SW)= $\frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$ (C_{RSS}[F] : Reverse transfer capacitance of FET, I_{DRIVE}[A] : Peak current of gate.)
4)PD(ESR)=$I_{RMS}^2 \times ESR$ (I_{RMS}[A] : Ripple current of capacitor, ESR[Ω] : Equivalent series resistance.)
5)PD(IC)=Vin × I_{CC} (I_{CC}[A] : Circuit current.)

●Consideration on permissible dissipation and heat generation

As BU9151MUV functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

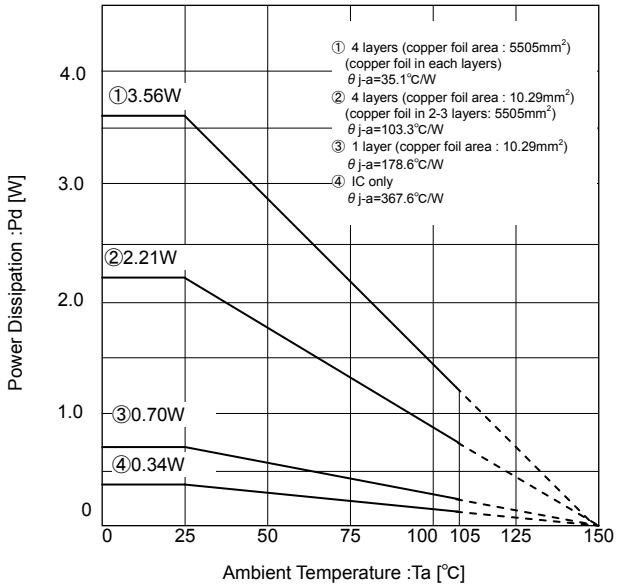


Fig.32 Heat radiation characteristics (VQFN020V4040)

$P=I_{OUT}^2 \times R_{ON}$

$R_{ON}=D \times R_{ONH}+(1-D)R_{ONL}$

D : ON Duty(=V_{OUT}/V_{CC})

R_{ONH} : ON resistance of High side MOS FET

R_{ONL} : ON resistance of Low side MOS FET

I_{OUT} : Output current

If V_{CC}=3.3V, V_{OUT1}=1.8V, V_{OUT2}=1.2V, R_{ONH1}=0.27Ω, R_{ONL1}=0.18Ω, R_{ONH2}=0.27Ω, R_{ONL2}=0.18Ω
I_{OUT1}=0.4A, I_{OUT2}=0.8A, for example,

$D_1=V_{OUT1}/V_{CC}=1.8/3.3=0.55$

$D_2=V_{OUT2}/V_{CC}=1.2/3.3=0.36$

$R_{ON1}=0.55 \times 0.27+(1-0.55) \times 0.18$

$=0.1485+0.081$

$=0.2295[\Omega]$

$R_{ON2}=0.36 \times 0.27+(1-0.36) \times 0.18$

$=0.0972+0.1152$

$=0.2124[\Omega]$

$P=0.4^2 \times 0.2295+0.8^2 \times 0.2124=0.173[W]$

As R_{ONH} is greater than R_{ONL} in BU9151MUV, the dissipation increases as the ON duty becomes greater.
With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●Selection of components externally connected

1. Selection of inductor (L)

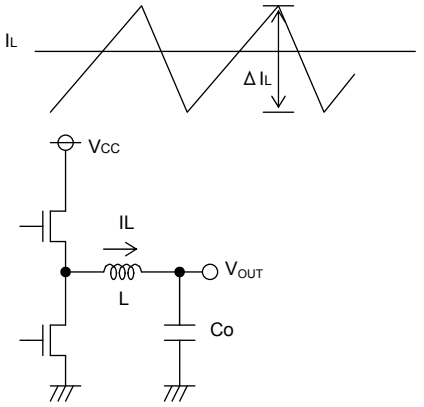


Fig.33 Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the i nductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \text{ [A]} \cdot \cdot \cdot (1)$$

Appropriate ripple current at output should be 20% more or less of the maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}\text{max. [A]} \cdot \cdot \cdot (2)$$

$$L = \frac{(V_{CC}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \text{ [H]} \cdot \cdot \cdot (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

※Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=3.3V, V_{OUT}=1.8V, f=1.0MHz, $\Delta I_L = 0.3 \times 0.8A = 0.24A$, for example,(BD9151MUV)

$$L = \frac{(3.3-1.8) \times 1.8}{0.24 \times 3.3 \times 1.0M} = 2.02\mu \rightarrow 2.2[\mu H]$$

※Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (C_O)

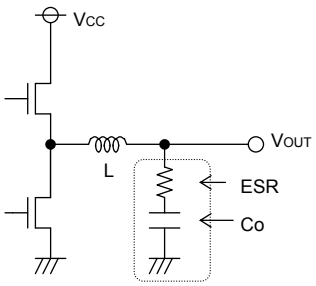


Fig.34 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.

Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \text{ [V]} \cdot \cdot \cdot (4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

※Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 22μF to 100μF ceramic capacitor is recommended. Less ESR allows reduction in output ripple voltage.

3. Selection of input capacitor (Cin)

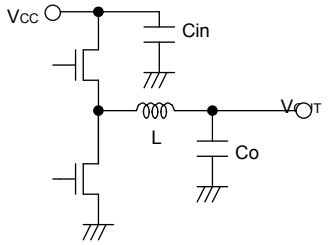


Fig.35 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (5):

$$I_{RMS}=I_{OUT}\times\frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A]\cdot\cdot\cdot(5)$$

< Worst case > $I_{RMS(max.)}$

When $V_{CC}=2\times V_{OUT}$, $I_{RMS}=\frac{I_{OUT}}{2}$

If V_{CC}=5.0V, V_{OUT}=1.8V, and $I_{OUTmax.}$=0.4A, (BD9151MUV)

$$I_{RMS}=2\times\frac{\sqrt{1.8(5.0-1.8)}}{5.0}=0.48[A_{RMS}]$$

A low ESR 22μF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of RITH, CITH that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, adding a zero to the power amplifier output with C easily compensates the phases and R as described below to cancel a pole at the power amplifier.

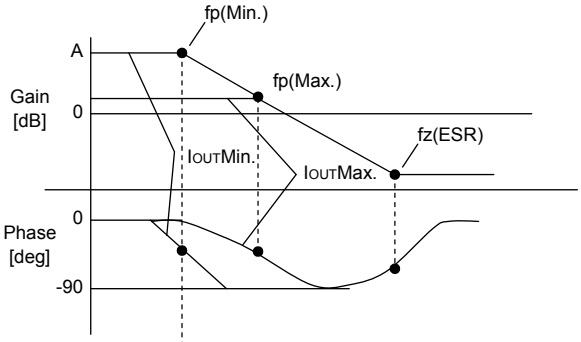


Fig.36 Open loop gain characteristics

$$f_p=\frac{1}{2\pi\times R_O\times C_O}$$

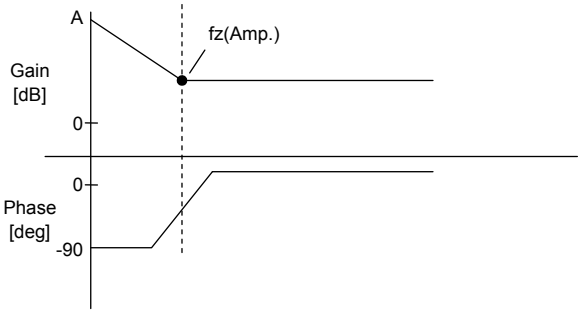
$$f_{z(ESR)}=\frac{1}{2\pi\times E_{SR}\times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$f_{p(Min.)}=\frac{1}{2\pi\times R_{OMax.}\times C_O}\ [Hz]\leftarrow\text{with lighter load}$$

$$f_{p(Max.)}=\frac{1}{2\pi\times R_{OMin.}\times C_O}\ [Hz]\ \leftarrow\text{with heavier load}$$



Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change.
(This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$f_{z(Amp.)}=\frac{1}{2\pi\times R_{ITH}\times C_{ITH}}$$

Fig.37 Error amp phase compensation characteristics

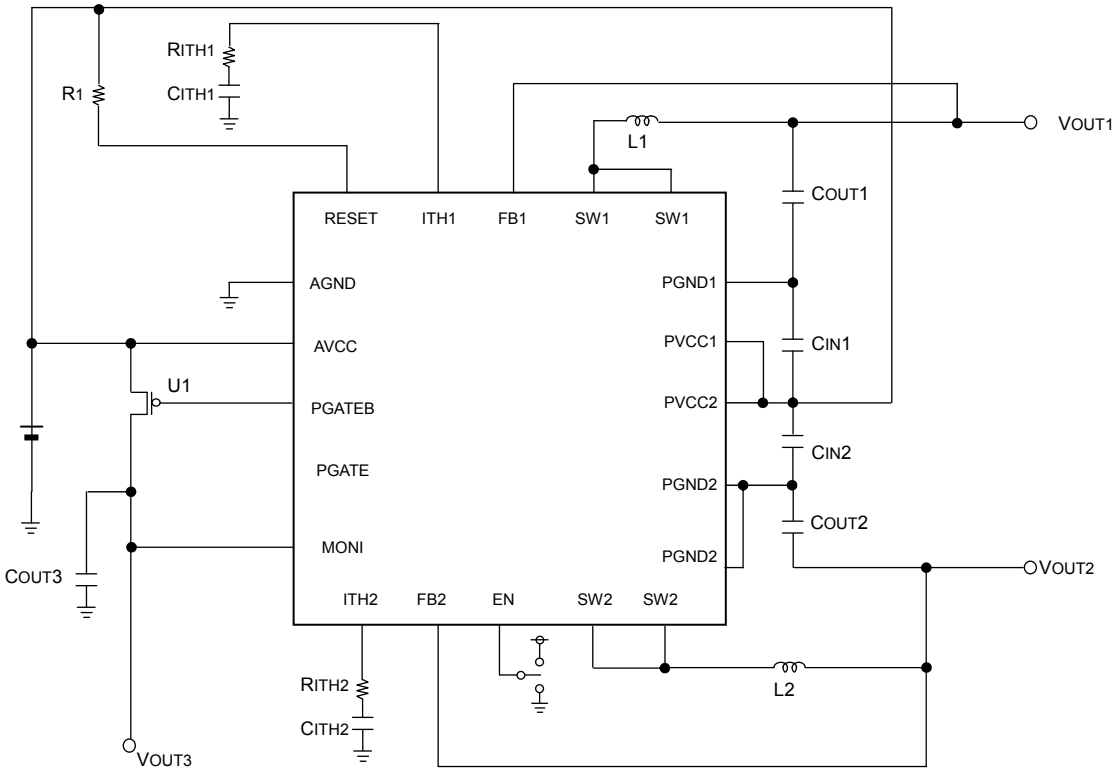


Fig.38 External parts sketch

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz(Amp.) = fp(Min.)$$

$$\longrightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax.} \times C_O}$$

●BD9151MUV Caution of Board layout

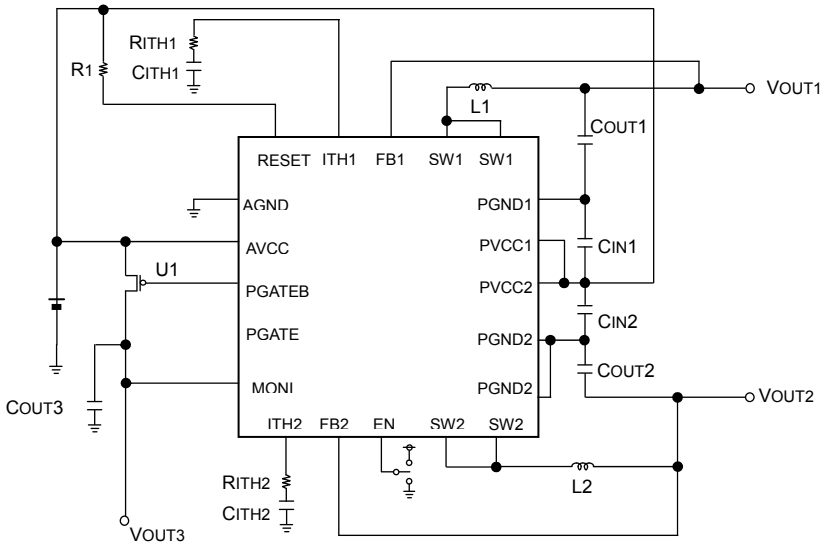


Fig.39 Example of board layout

①Lay out the input ceramic capacitor CIN closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.
②Lay out CITH and RITH between the pins ITH and GND as neat as possible with least necessary wiring.

※VQFN020V4040 (BD9151MUV) has thermal PAD on the reverse of the package.
The package thermal performance may be enhanced by bonding the PAD to GND plane which take a large area of PCB.

●Recommended parts list, using the application above

Symbol	Parts name	Value	Company	Parts number
L1,2	Inductor	2.2μH	TDK	LTF5022-2R2N3R2
			TAIYO YUDEN	NR3012T2R2M
CIN1,CIN2	Ceramic capacitor	22μF	Murata	GRM32EB11A226KE20
Cout1,Cout2	Ceramic capacitor	22μF	Murata	GRM31CB30J226KE18
CITH1	Ceramic capacitor	330pF	Murata	GRM18 Series
RITH1	Resistor	22kΩ	Rohm	MCR03 Series
CITH2	Ceramic capacitor	220pF	Murata	GRM18 Series
RITH2	Resistor	15kΩ	Rohm	MCR03 Series
U1	Pch FET	-	Rohm	RT1A040ZP
Cout3	Ceramic capacitor	22μF	Murata	GRM31CB30J226KE18
R1	Resistor	10kΩ	Rohm	MCR03 Series

※The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and BU9151MUV when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode or snubber established between the SW and PGND pins.

●I/O Equivalent circuits

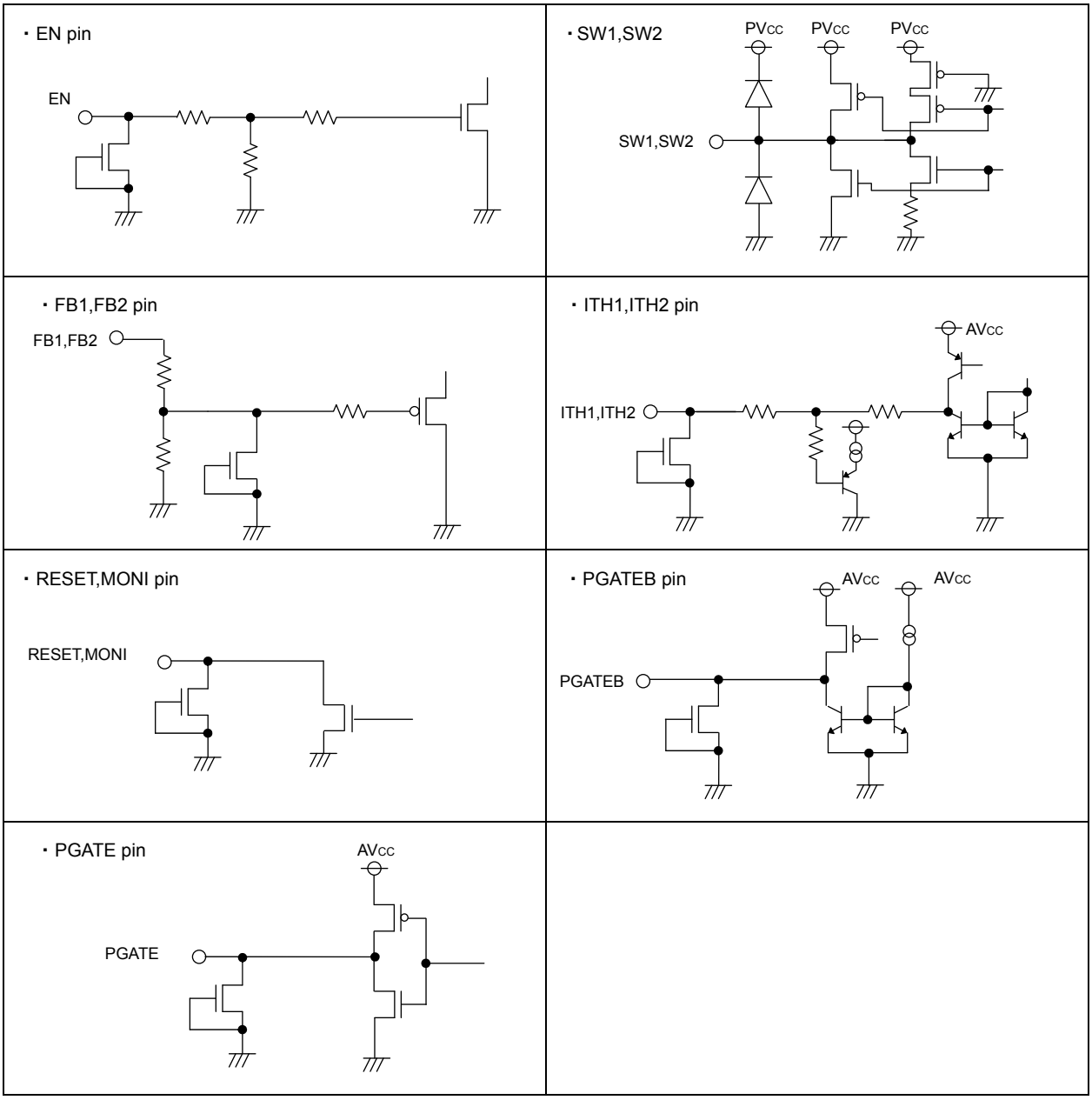


Fig.40 I/O Equivalent circuits

●Notes for use

1. Absolute Maximum Ratings
   While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically including insertion of fuses.
2. Electrical potential at GND
   GND must be designed to have the lowest electrical potential In any operating conditions.
3. Short-circuiting between terminals, and mis-mounting
   When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment. Failure to do so may result in IC breakdown. Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.
4. Thermal shutdown protection circuit
   Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC. So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.
5. Inspection with the IC set to a pc board
   If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC. For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage. When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.
6. Input to IC terminals
   This is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.
   If a resistor is joined to a transistor terminal as shown in Fig 41.
   ○P-N junction works as a parasitic diode if the following relationship is satisfied; GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and
   ○if GND>Terminal B (at NPN transistor side),
   a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.
   The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.

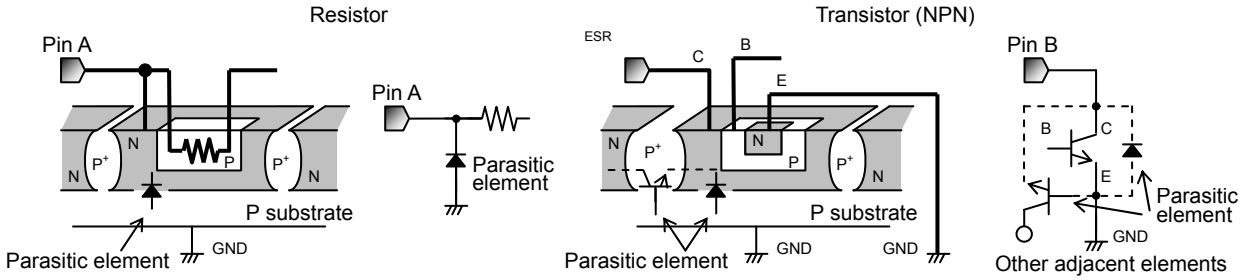


Fig.41 Simplified structure of monorisic IC

7. Ground wiring pattern
   If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.
8. Selection of inductor
   It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. Especially, in case output voltage is set 1.6V or more, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and BU9151MUV, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within operation range.

●**Ordering part number**

B	D	9	1	5	1	M	U	V	-	E	2

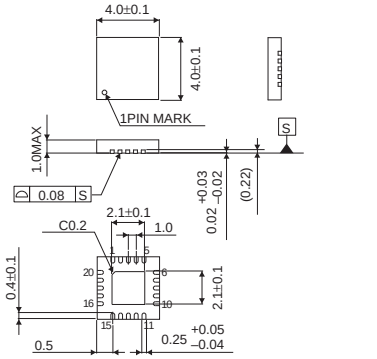
Part No. (BD)

Part No. (9151)

Package
MUV: VQFN20V4040

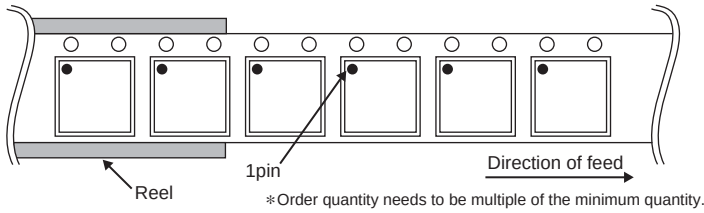
Packaging and forming specification
E2: Embossed tape and reel
(VQFN20V4040)

VQFN020V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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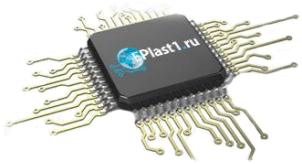

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.