

# 3 MHz, 125 $\mu$ A Low Power Operational Amplifier

## NCS20061/2/4, NCV20061/2/4

The NCS20061/2/4 is a family of single, dual and quad Operational Amplifiers (Op Amps) with 3 MHz of Gain-Bandwidth Product (GBWP) while consuming only 125  $\mu$ A of Quiescent current per opamp. The NCS2006x has Input Offset Voltage of 4 mV and operates from 1.8 V to 5.5 V supply voltage over a wide temperature range ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ). The Rail-to-Rail In/Out operation allows the use of the entire supply voltage range while taking advantage of the 3 MHz GBWP. Thus, this family offers superior performance over many industry standard parts. These devices are AEC-Q100 qualified which is denoted by the NCV prefix.

NCS2006x's low current consumption and low supply voltage performance in space saving packages, makes them ideal for sensor signal conditioning and low voltage current sensing applications in Automotive, Consumer and Industrial markets.

### Features

- Gain-Bandwidth Product: 3 MHz
- Low Supply Current/ Channel: 125  $\mu$ A typ ( $V_S = 1.8\text{ V}$ )
- Low Input Offset Voltage: 4 mV max
- Wide Supply Range: 1.8 V to 5.5 V
- Wide Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Rail-to-Rail Input and Output
- Unity Gain Stable
- Available in Single, Dual and Quad Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Automotive
- Battery Powered/ Portable
- Sensor Signal Conditioning
- Low Voltage Current Sensing
- Filter Circuits
- Unity Gain Buffer

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

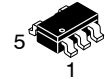


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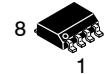
SC70-5  
CASE 419A



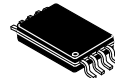
TSOP-5/SOT23-5  
CASE 483



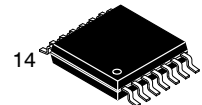
Micro8™/MSOP8  
CASE 846A



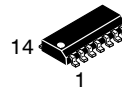
SOIC-8  
CASE 751



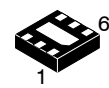
TSSOP-8  
CASE 948S



TSSOP-14  
CASE 948G



SOIC-14  
CASE 751A



UDFN6  
CASE 517AP

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

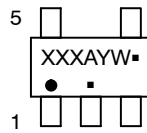
# NCS20061/2/4, NCV20061/2/4

## MARKING DIAGRAMS

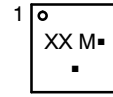
### Single Channel Configuration NCS20061, NCV20061



**SC70-5**  
**CASE 419A**



**TSOP-5/SOT23-5**  
**CASE 483**



**UDFN6**  
**CASE 517AP**

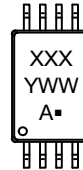
### Dual Channel Configuration NCS20062, NCV20062



**Micro8™/MSOP8**  
**CASE 846A**



**SOIC-8**  
**CASE 751**

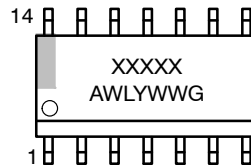


**TSSOP-8**  
**CASE 948S**

### Quad Channel Configuration NCS20064, NCV20064



**TSSOP-14**  
**CASE 948G**



**SOIC-14**  
**CASE 751A**

XXXXX = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot

Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

# NCS20061/2/4, NCV20061/2/4

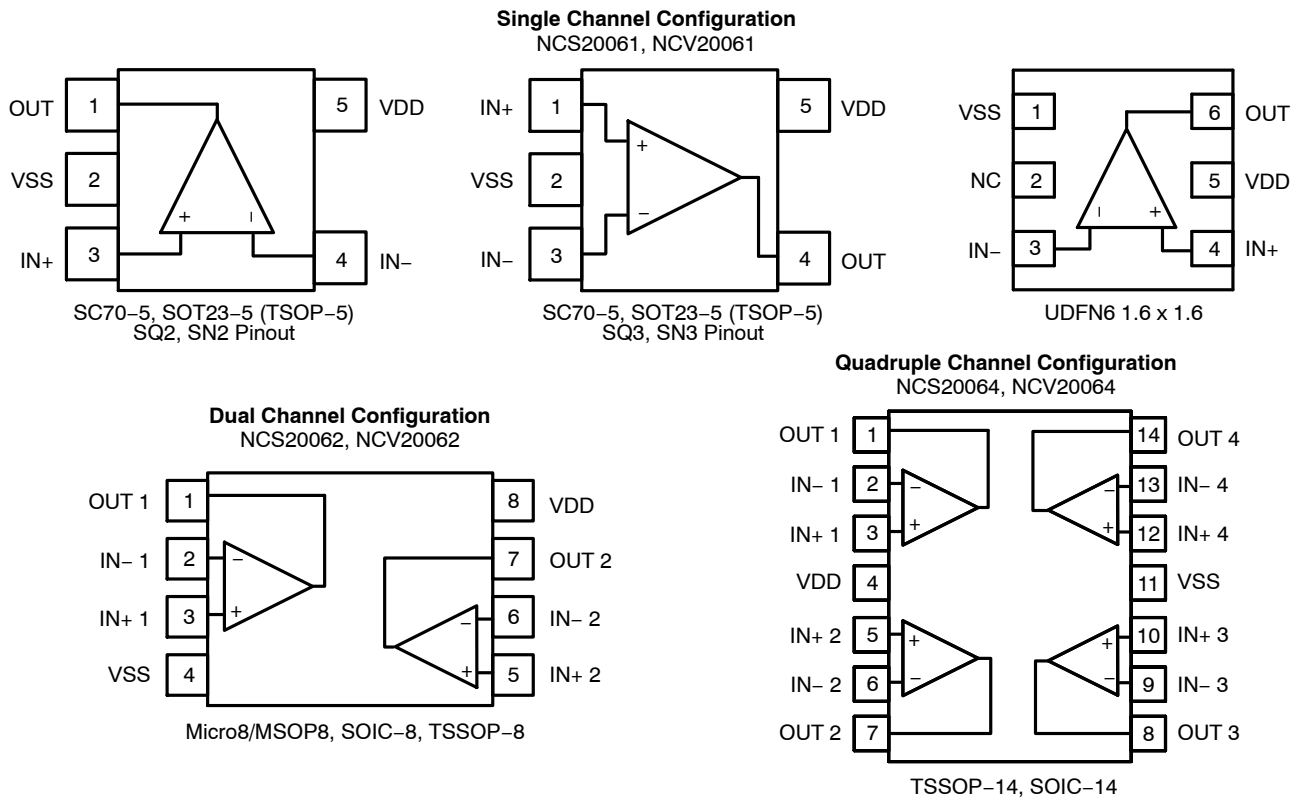


Figure 1. Pin Connections

## ORDERING INFORMATION

Device	Configuration	Automotive	Marking	Package	Shipping†
NCS20061SQ3T2G	Single	No	AAM	SC70	Contact local sales office for more information
NCS20061SN2T1G			AEP	SOT23-5/TSOP-5	
NCS20061SN3T1G			AEQ	SOT23-5/TSOP-5	
NCS20061MUTAG		Yes	AG	UDFN6	
NCV20061SQ3T2G*			AAM	SC70	
NCV20061SN2T1G*			AEP	SOT23-5/TSOP-5	
NCV20061SN3T1G*			AEQ	SOT23-5/TSOP-5	
NCS20062DMR2G	Dual	No	2K62	Micro8/MSOP8	
NCS20062DR2G			NCS20062	SOIC-8	
NCS20062DTBR2G			K62	TSSOP-8	
NCV20062DMR2G*		Yes	2K62	Micro8/MSOP8	
NCV20062DR2G*			NCS20062	SOIC-8	
NCV20062DTBR2G*			K62	TSSOP-8	
NCS20064DR2G**	Quad**	No	20064	SOIC-14	
NCS20064DTBR2G**			264	TSSOP-14	
NCV20064DR2G**		Yes	20064	SOIC-14	
NCV20064DTBR2G**			264	TSSOP-14	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

\*\*In Development. Not yet released.

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Rating	Symbol	Limit	Unit	
Supply Voltage ( $V_{DD} - V_{SS}$ ) (Note 2)	$V_S$	6	V	
Input Voltage	$V_I$	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V	
Differential Input Voltage	$V_{ID}$	$\pm V_S$	V	
Maximum Input Current	$I_I$	$\pm 10$	mA	
Maximum Output Current	$I_O$	$\pm 100$	mA	
Continuous Total Power Dissipation (Note 2)	$P_D$	200	mW	
Maximum Junction Temperature	$T_J$	150	$^{\circ}\text{C}$	
Storage Temperature Range	$T_{STG}$	-65 to 150	$^{\circ}\text{C}$	
Mounting Temperature (Infrared or Convection – 20 sec)	$T_{mount}$	260	$^{\circ}\text{C}$	
ESD Capability (Note 3)	Human Body Model	ESD <sub>HBM</sub>	2000	V
	Charge Device Model	ESD <sub>CDM</sub>	2000	
Latch-Up Current (Note 4)	$I_{LU}$	100	mA	
Moisture Sensitivity Level (Note 5)	MSL	Level 1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS for Safe Operating Area.
2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 $^{\circ}\text{C}$ . Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
3. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per JEDEC standard Js-001-2017 (AEC-Q100-002)  
 ESD Charged Device Model tested per JEDEC standard JS-002-2014 (AEC-Q100-011)
4. Latch-up Current tested per JEDEC standard JESD78E (AEC-Q100-004)
5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J-STD-020A

**THERMAL INFORMATION**

Parameter	Symbol	Channels	Package	Single Layer Board (Note 6)	Multi-Layer Board (Note 7)	Unit
Junction to Ambient Thermal Resistance	$\theta_{JA}$	Single	SC-70	490	444	$^{\circ}\text{C}/\text{W}$
			SOT23-5/TSOP-5	310	247	
			UDFN6	276	239	
		Dual	Micro8/MSOP8	236	167	
			SOIC-8	190	131	
			TSSOP-8	253	194	
		Quad	SOIC-14	130	99	
			TSSOP-14	178	140	

6. Value based on 1S standard PCB according to JEDEC51-3 with 1.0 oz copper and a 300 mm<sup>2</sup> copper area
7. Value based on 1S2P standard PCB according to JEDEC51-7 with 1.0 oz copper and a 100 mm<sup>2</sup> copper area

**OPERATING RANGES**

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage	$V_S$	1.8	5.5	V
Differential Input Voltage	$V_{ID}$		$V_S$	V
Input Common Mode Range	$V_{ICM}$	$V_{SS} - 0.2$	$V_{DD} + 0.2$	V
Ambient Temperature	$T_A$	-40	125	$^{\circ}\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## NCS20061/2/4, NCV20061/2/4

### ELECTRICAL CHARACTERISTICS AT $V_S = 1.8\text{ V}$

$T_A = 25^\circ\text{C}$ ;  $R_L \geq 10\text{ k}\Omega$ ;  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . (Note 8)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Input Offset Voltage	$V_{OS}$			0.5	3.5	mV
					<b>4</b>	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current (Note 8)	$I_{IB}$			1		pA
					<b>1500</b>	pA
Input Offset Current (Note 8)	$I_{OS}$			1		pA
					<b>1100</b>	pA
Channel Separation	XTLK	$f = 1\text{ kHz}$		125		dB
Differential Input Resistance	$R_{ID}$			10		$\text{G}\Omega$
Common Mode Input Resistance	$R_{IN}$			10		$\text{G}\Omega$
Differential Input Capacitance	$C_{ID}$			1		pF
Common Mode Input Capacitance	$C_{CM}$			5		pF
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$	48	73		dB
		$V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$	<b>45</b>			
<b>OUTPUT CHARACTERISTICS</b>						
Open Loop Voltage Gain	$A_{VOL}$		86	120		dB
			<b>80</b>			
Short Circuit Current	$I_{SC}$	Output to positive rail, sinking current		19		mA
		Output to negative rail, sourcing current		15		
Output Voltage High	$V_{OH}$	Voltage output swing from positive rail $V_{OH} = V_{DD} - V_{OUT}$		3	19	mV
					<b>20</b>	
Output Voltage Low	$V_{OL}$	Voltage output swing from negative rail $V_{OL} = V_{OUT} - V_{SS}$		3	19	mV
					<b>20</b>	
<b>AC CHARACTERISTICS</b>						
Unity Gain Bandwidth	UGBW			3		MHz
Slew Rate at Unity Gain	SR	$V_{IN} = 1.2\text{ Vpp}$ , Gain = 1		1.2		$\text{V}/\mu\text{s}$
Phase Margin	$\psi_m$			60		$^\circ$
Gain Margin	$A_m$			10		dB
Settling Time	$t_S$	$V_{IN} = 1.2\text{ Vpp}$ , Gain = 1	Settling time to 0.1%	2.3		$\mu\text{s}$
			Settling time to 0.01%	6		
Open Loop Output Impedance	$Z_{OL}$			See Figure 25		$\Omega$
<b>NOISE CHARACTERISTICS</b>						
Total Harmonic Distortion plus Noise	THD+N	$V_{IN} = 1.2\text{ Vpp}$ , $f = 1\text{ kHz}$ , $A_v = 1$		0.005		%
Input Referred Voltage Noise	$e_n$	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 10\text{ kHz}$		15	
Input Referred Current Noise	$i_n$	$f = 1\text{ kHz}$		300		$\text{fA}/\sqrt{\text{Hz}}$
<b>SUPPLY CHARACTERISTICS</b>						
Power Supply Rejection Ratio	PSRR	No Load	67	90		dB
			<b>64</b>			
Power Supply Quiescent Current	$I_{DD}$	Per channel, no load		125	<b>170</b>	$\mu\text{A}$

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

## NCS20061/2/4, NCV20061/2/4

### ELECTRICAL CHARACTERISTICS AT $V_S = 3.3\text{ V}$

$T_A = 25^\circ\text{C}$ ;  $R_L \geq 10\text{ k}\Omega$ ;  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . (Note 9)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Input Offset Voltage	$V_{OS}$			0.5	3.5	mV
					<b>4</b>	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current (Note 9)	$I_{IB}$			1		pA
					<b>1500</b>	pA
Input Offset Current (Note 9)	$I_{OS}$			1		pA
					<b>1100</b>	pA
Channel Separation	XTLK	$f = 1\text{ kHz}$		125		dB
Differential Input Resistance	$R_{ID}$			10		$\text{G}\Omega$
Common Mode Input Resistance	$R_{IN}$			10		$\text{G}\Omega$
Differential Input Capacitance	$C_{ID}$			1		pF
Common Mode Input Capacitance	$C_{CM}$			5		pF
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$	53	76		dB
		$V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$	<b>48</b>			

### OUTPUT CHARACTERISTICS

Open Loop Voltage Gain	$A_{VOL}$		90	120		dB
			<b>86</b>			
Short Circuit Current	$I_{SC}$	Output to positive rail, sinking current		19		mA
		Output to negative rail, sourcing current		15		
Output Voltage High	$V_{OH}$	Voltage output swing from positive rail $V_{OH} = V_{DD} - V_{OUT}$		3	24	mV
					<b>25</b>	
Output Voltage Low	$V_{OL}$	Voltage output swing from negative rail $V_{OL} = V_{OUT} - V_{SS}$		3	24	mV
					<b>25</b>	

### AC CHARACTERISTICS

Unity Gain Bandwidth	UGBW			3		MHz
Slew Rate at Unity Gain	SR	$V_{IN} = 2.5\text{ Vpp}$ , Gain = 1		1.2		$\text{V}/\mu\text{s}$
Phase Margin	$\psi_m$			60		$^\circ$
Gain Margin	$A_m$			10		dB
Settling Time	$t_S$	$V_{IN} = 2.5\text{ Vpp}$ , Gain = 1	Settling time to 0.1%	2.3		$\mu\text{s}$
			Settling time to 0.01%	3.1		
Open Loop Output Impedance	$Z_{OL}$			See Figure 25		$\Omega$

### NOISE CHARACTERISTICS

Total Harmonic Distortion plus Noise	THD+N	$V_{IN} = 2.5\text{ Vpp}$ , $f = 1\text{ kHz}$ , $A_v = 1$		0.005		%
Input Referred Voltage Noise	$e_n$	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 10\text{ kHz}$		15	
Input Referred Current Noise	$i_n$	$f = 1\text{ kHz}$		300		$\text{fA}/\sqrt{\text{Hz}}$

### SUPPLY CHARACTERISTICS

Power Supply Rejection Ratio	PSRR	No Load	67	90		dB
			<b>64</b>			
Power Supply Quiescent Current	$I_{DD}$	Per channel, no load		135	<b>180</b>	$\mu\text{A}$

9. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

## NCS20061/2/4, NCV20061/2/4

### ELECTRICAL CHARACTERISTICS AT $V_S = 5.5\text{ V}$

$T_A = 25^\circ\text{C}$ ;  $R_L \geq 10\text{ k}\Omega$ ;  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . (Note 10)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Input Offset Voltage	$V_{OS}$			0.5	3.5	mV
					<b>4</b>	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current (Note 10)	$I_{IB}$			1		pA
					<b>1500</b>	pA
Input Offset Current (Note 10)	$I_{OS}$			1		pA
					<b>1100</b>	pA
Channel Separation	XTLK	$f = 1\text{ kHz}$		125		dB
Differential Input Resistance	$R_{ID}$			10		$\text{G}\Omega$
Common Mode Input Resistance	$R_{IN}$			10		$\text{G}\Omega$
Differential Input Capacitance	$C_{ID}$			1		pF
Common Mode Input Capacitance	$C_{CM}$			5		pF
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$	55	79		dB
		$V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$	<b>51</b>			

### OUTPUT CHARACTERISTICS

Open Loop Voltage Gain	$A_{VOL}$		90	120		dB
			<b>86</b>			
Short Circuit Current	$I_{SC}$	Output to positive rail, sinking current		19		mA
		Output to negative rail, sourcing current		15		
Output Voltage High	$V_{OH}$	Voltage output swing from positive rail $V_{OH} = V_{DD} - V_{OUT}$		3	24	mV
					<b>25</b>	
Output Voltage Low	$V_{OL}$	Voltage output swing from negative rail $V_{OL} = V_{OUT} - V_{SS}$		3	24	mV
					<b>25</b>	

### AC CHARACTERISTICS

Unity Gain Bandwidth	UGBW			3		MHz
Slew Rate at Unity Gain	SR	$V_{IN} = 5\text{ Vpp}$ , Gain = 1		1.2		$\text{V}/\mu\text{s}$
Phase Margin	$\psi_m$			60		$^\circ$
Gain Margin	$A_m$			10		dB
Settling Time	$t_S$	$V_{IN} = 5\text{ Vpp}$ , Gain = 1	Settling time to 0.1%	2.3		$\mu\text{s}$
			Settling time to 0.01%	3.1		
Open Loop Output Impedance	$Z_{OL}$			See Figure 25		$\Omega$

### NOISE CHARACTERISTICS

Total Harmonic Distortion plus Noise	THD+N	$V_{IN} = 5\text{ Vpp}$ , $f = 1\text{ kHz}$ , $A_v = 1$		0.005		%
Input Referred Voltage Noise	$e_n$	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		15		
Input Referred Current Noise	$i_n$	$f = 1\text{ kHz}$		300		$\text{fA}/\sqrt{\text{Hz}}$

### SUPPLY CHARACTERISTICS

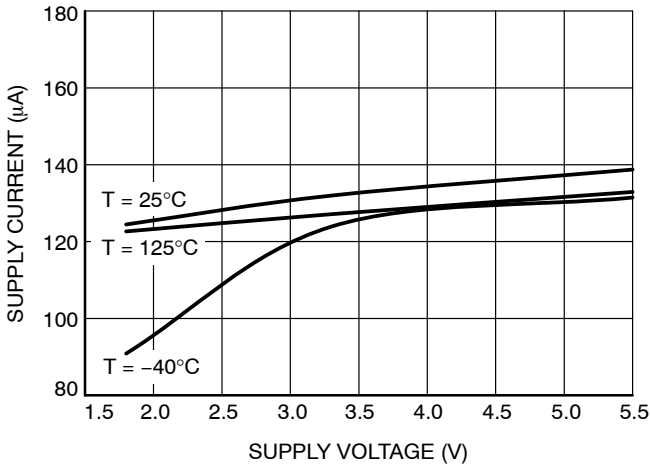
Power Supply Rejection Ratio	PSRR	No Load	67	90		dB
			<b>64</b>			
Power Supply Quiescent Current	$I_{DD}$	Per channel, no load		140	<b>200</b>	$\mu\text{A}$

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

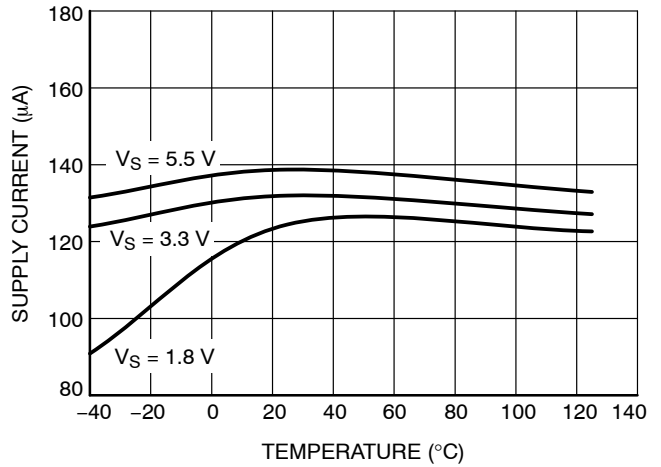
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**TYPICAL PERFORMANCE CHARACTERISTICS**

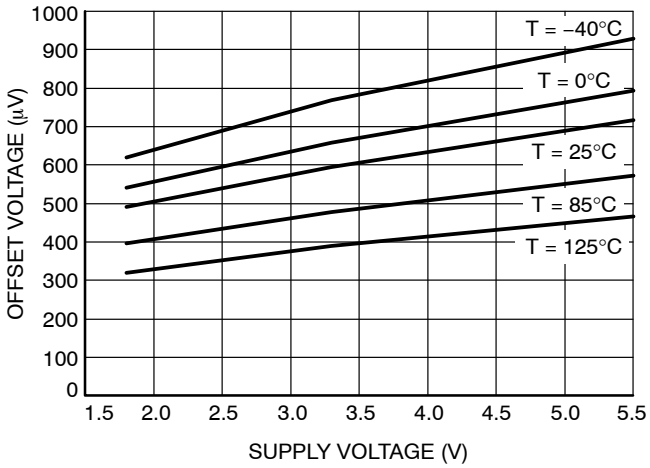
$T_A = 25^\circ\text{C}$ ,  $R_L \geq 10\text{ k}\Omega$ ,  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise specified



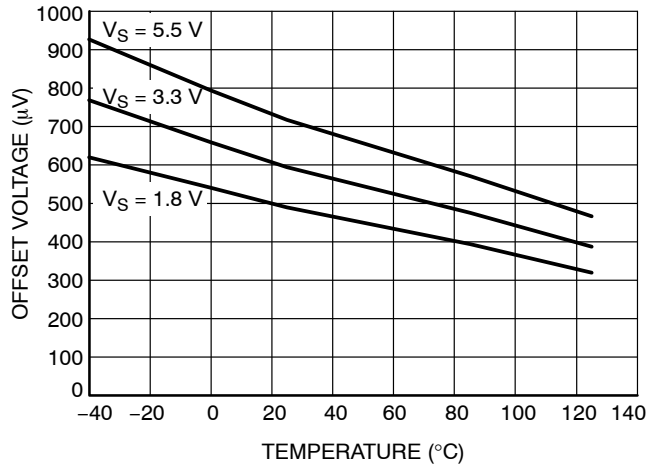
**Figure 2. Quiescent Current per Channel vs. Supply Voltage**



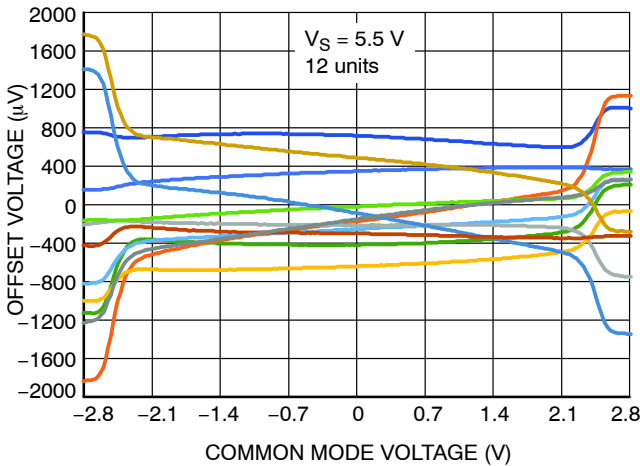
**Figure 3. Quiescent Current vs. Temperature**



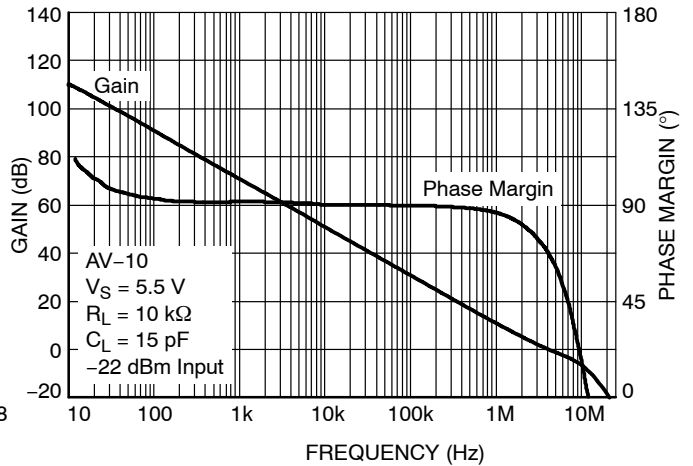
**Figure 4. Offset Voltage vs. Supply Voltage**



**Figure 5. Offset Voltage vs. Temperature**



**Figure 6. Offset Voltage vs. Common Mode Voltage**



**Figure 7. Open-loop Gain and Phase Margin vs. Frequency**



TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $R_L \geq 10\text{ k}\Omega$ ,  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise specified

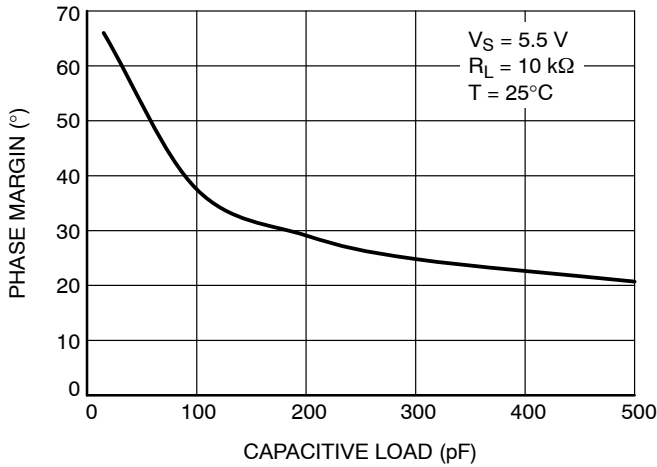


Figure 8. Phase Margin vs. Capacitive Load

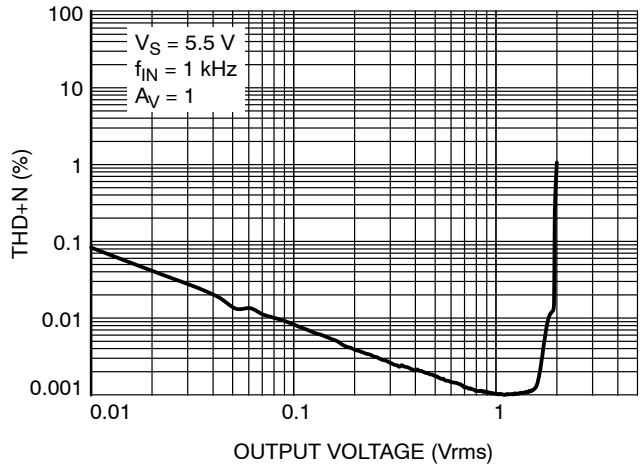


Figure 9. THD + N vs. Output Voltage

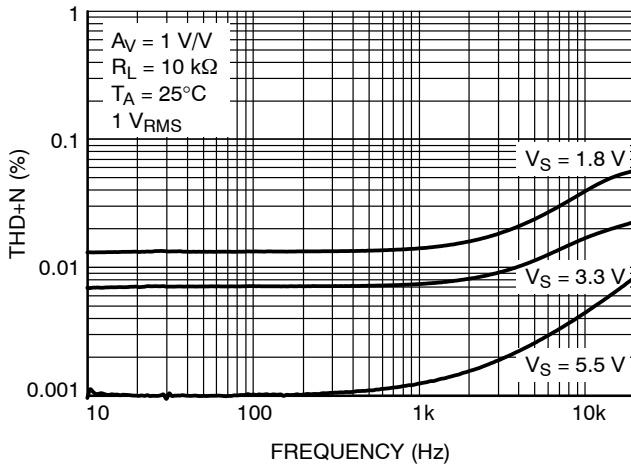


Figure 10. THD + N vs. Frequency



Figure 11. Input Voltage Noise vs. Frequency

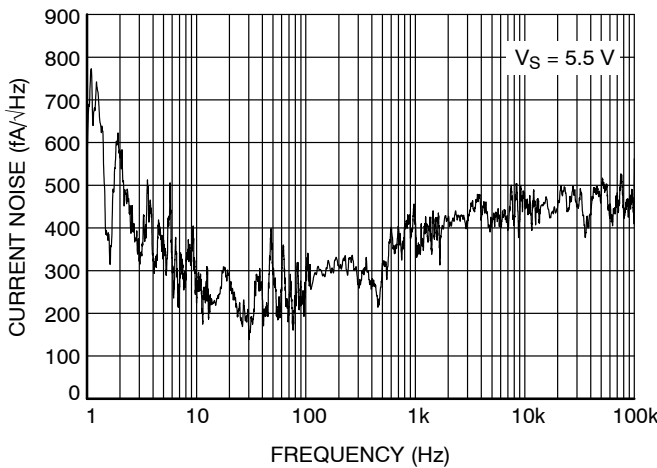


Figure 12. Input Current Noise vs. Frequency

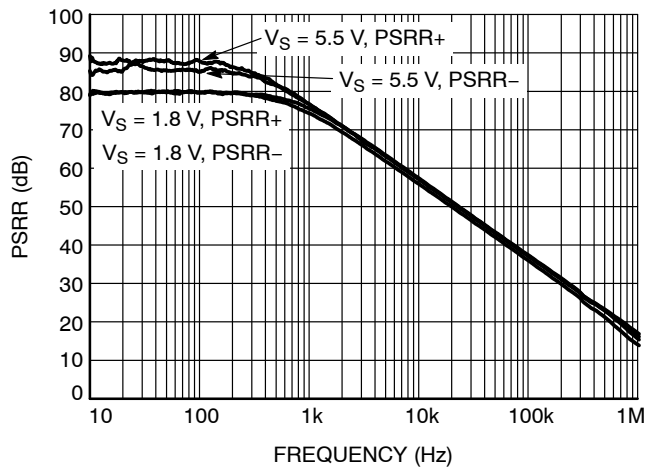


Figure 13. PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $R_L \geq 10\text{ k}\Omega$ ,  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise specified

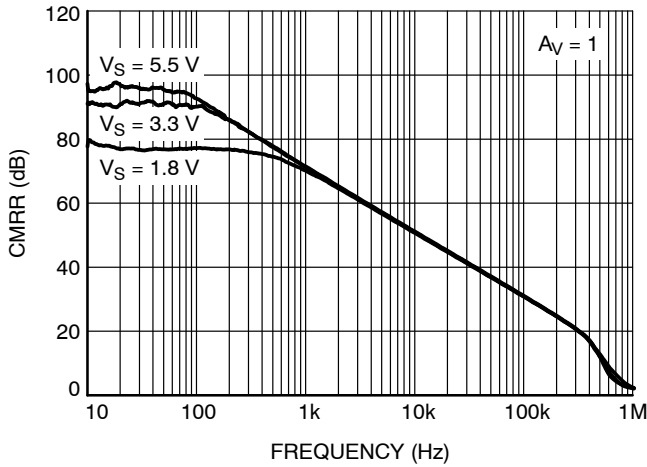


Figure 14. CMRR vs. Frequency

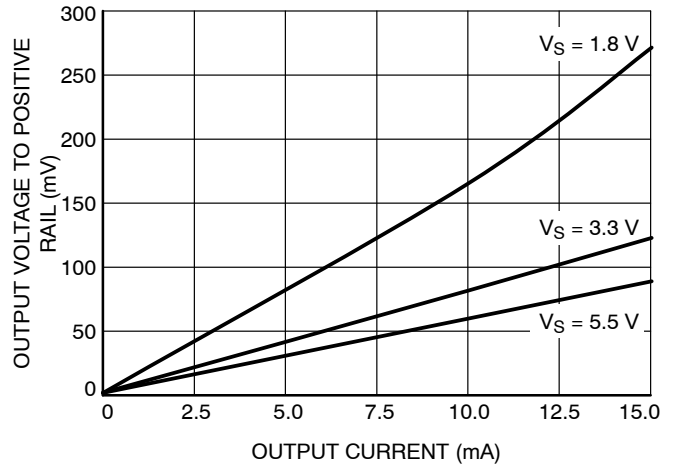


Figure 15. Output Voltage High to Rail

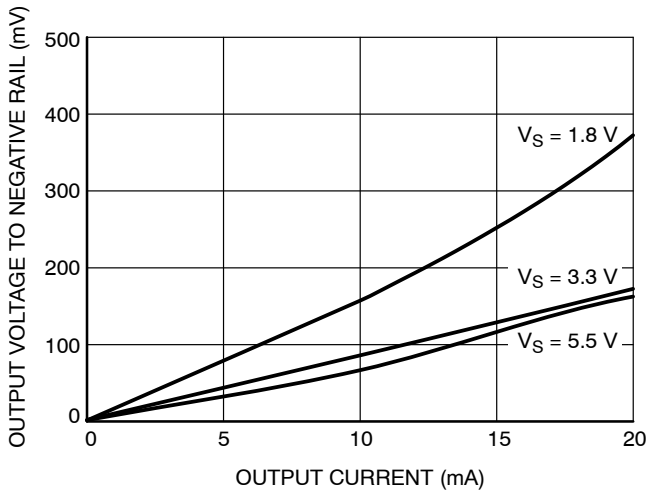


Figure 16. Output Voltage Low to Rail

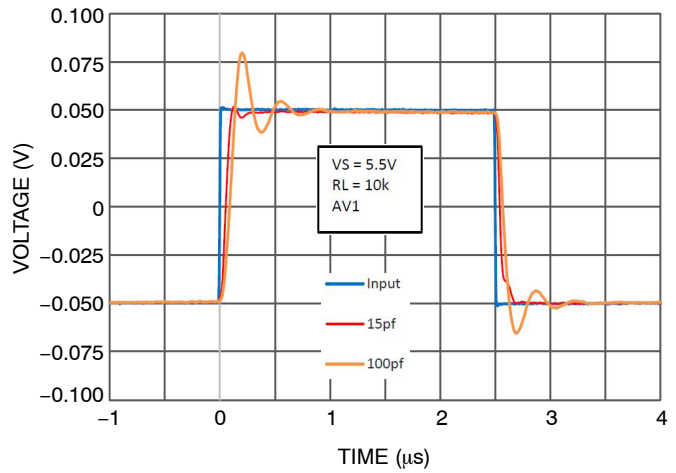


Figure 17. Non-Inverting Small Signal Transient Response

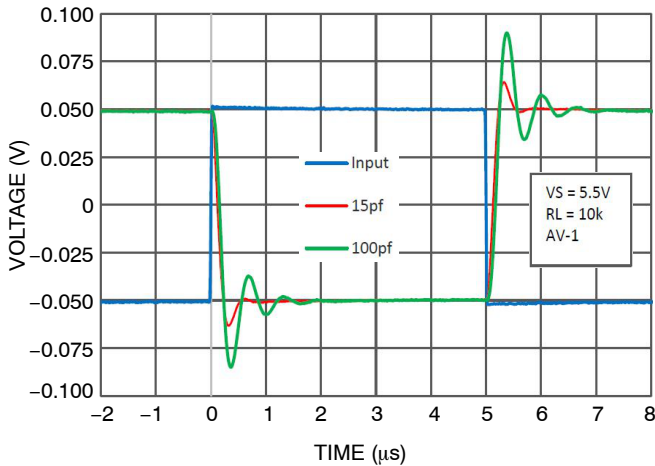


Figure 18. Inverting Small Signal Transient Response

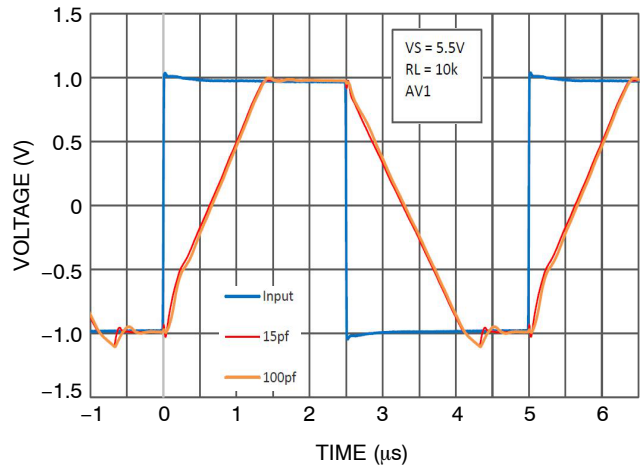


Figure 19. Non-Inverting Large Signal Transient Response

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $R_L \geq 10\text{ k}\Omega$ ,  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise specified

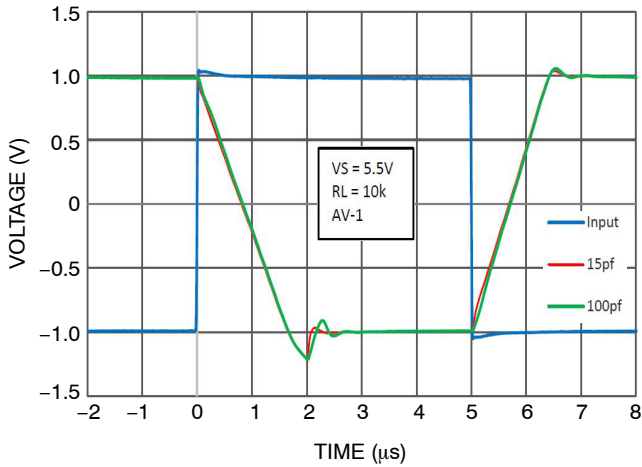


Figure 20. Inverting Large Signal Transient Response

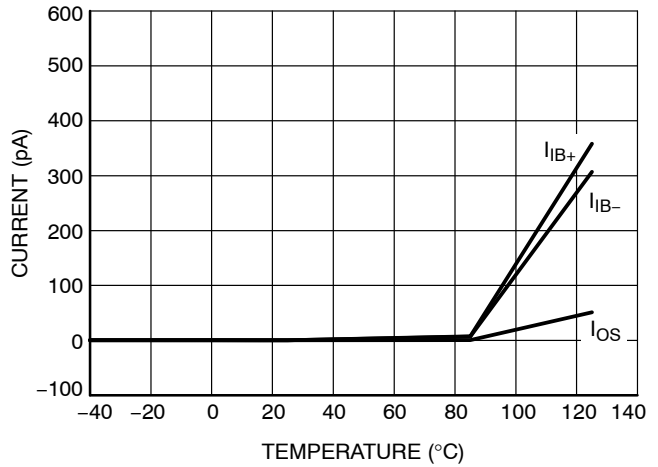


Figure 21. Input Bias and Offset Current vs. Temperature

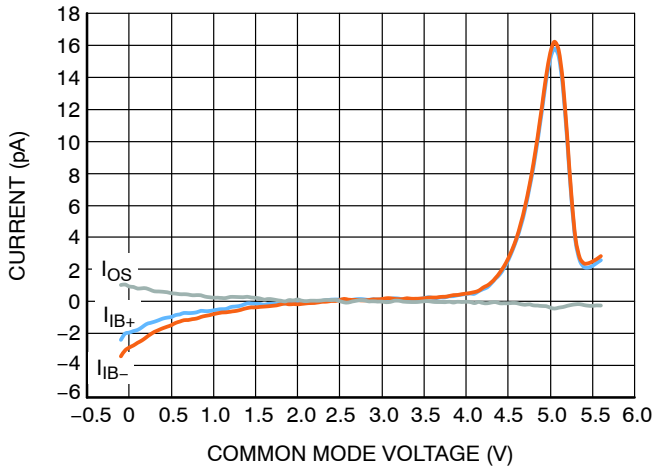


Figure 22. Input Bias Current vs. Common Mode Voltage

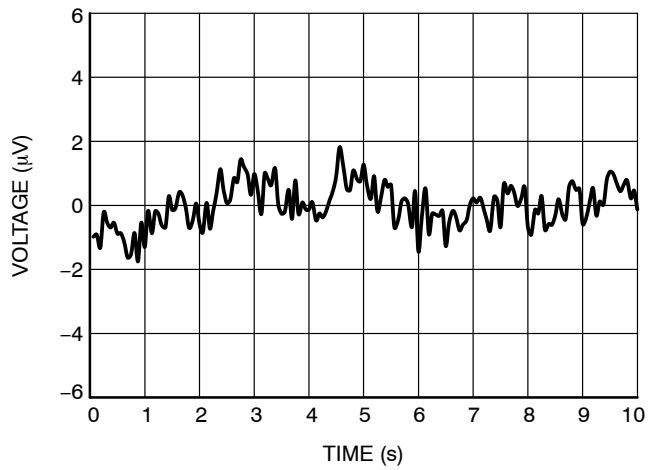


Figure 23. 0.1 Hz to 10 Hz Noise

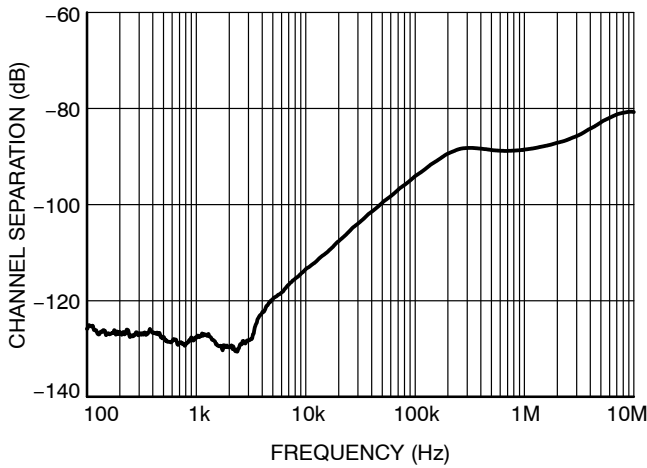


Figure 24. Channel Separation vs. Frequency

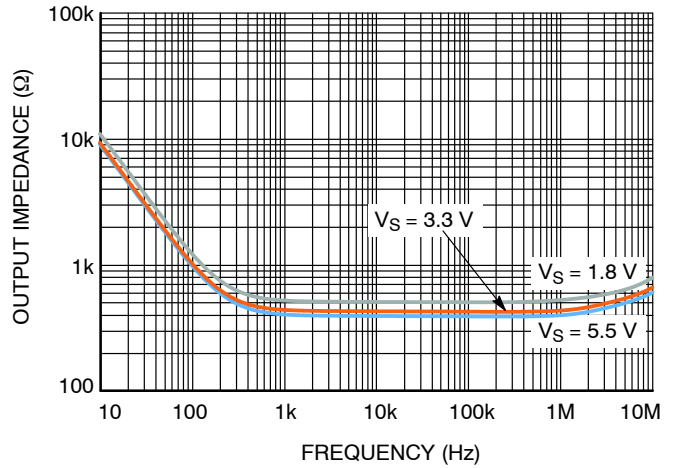
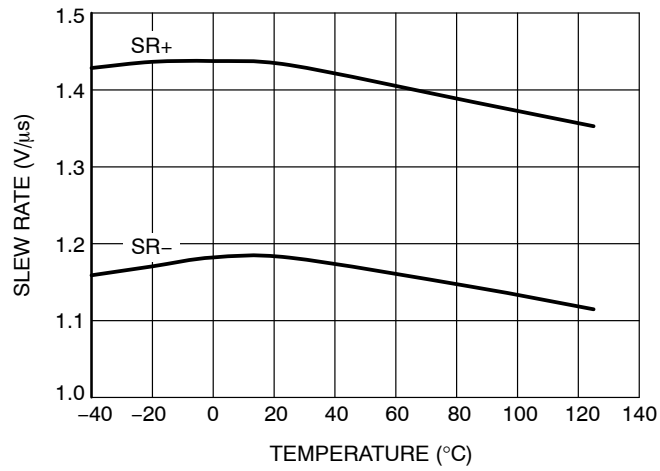


Figure 25. Open Loop Output Impedance vs. Frequency

**TYPICAL PERFORMANCE CHARACTERISTICS**

$T_A = 25^\circ\text{C}$ ,  $R_L \geq 10\text{ k}\Omega$ ,  $V_{CM} = V_{OUT} = \text{mid-supply}$  unless otherwise specified



**Figure 26. Slew Rate vs. Temperature**

**Application Information**

The NCS/NCV20061/2/4 family of operational amplifiers is manufactured using ON Semiconductor’s CMOS process. Products in this class are general purpose, unity-gain stable amplifiers and include single, dual and quad configurations.

**Rail-to-Rail Input with No Phase Reversal**

The NCS operational amplifiers are designed to prevent phase reversal or any similar issues when the input pins potential exceed the supply voltages by up to 100 mV. Figure 6 shows the input voltage exceeding the supply limits.

The input stage of the NCS/NCV 20061/2/4 family consists of two differential CMOS input stages connected in parallel: the first is constructed using paired PMOS devices and it operates at low common mode input voltages (VCM); the second stage is build using paired NMOS devices to operate at high VCM. The transition between the two input stages occurs at a common mode input voltage of approximately  $VDD-1.3V$  and it is visible in Figure 6 (Offset vs. VCM).

**Limiting input voltages**

In order to prevent damage and/or improper operation of these amplifiers, the application circuit must never expose the input pins to voltages or currents higher than the Absolute Maximum Ratings.

The internal ESD structure includes special diodes to protect the input stages while maintaining a low Input Bias (IIB) current. The input protection circuitry clamp the inputs when the signals applied exceed more than one diode drop

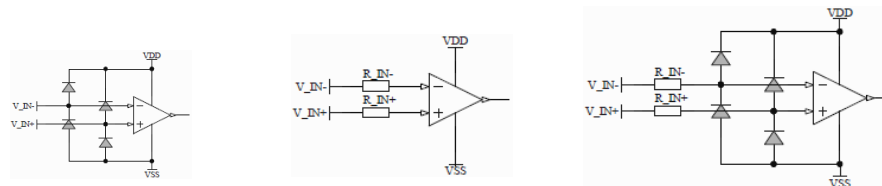
below VSS or one diode drop above VDD. Very fast ESD events (within the limits specified) trigger the protection structure so the operational amplifier is not damaged.

However, in some applications, it can be necessary to prevent excessive voltages from reaching the operational amplifier inputs by adding external clamp diodes. A possible solution is presented in Figure 27, where the four low-drop fast diodes (Schottky preferred) are used in parallel with the internal structure to divert the excessive energy to the supply rails where it can be easily dissipated or absorbed by the supply capacitors. The application designer should also take into account that these external diodes add leakage currents and parasitic capacitance that must be considered when evaluating the end-to-end performance of the amplifier stage.

**Limiting input currents**

In order to prevent damage/ improper operation of these amplifiers, the application circuit must limit the currents flowing in and out of the input pins. A possible solution is presented in Figure 27 by means of the two added series resistors. The minimum value for  $R_{IN-}$  and  $R_{IN+}$  should be calculated using Ohm’s Law so they limit the input pin currents to less than the absolute maximum values specified. The application designer should take into account that these resistors also add parasitic inductance that must be considered when evaluating performance.

Combining the current limiting resistors with the voltage limiting diodes creates a solid input protection structure, that can be used to insure reliable operation of the amplifier even in the hardest conditions.



**Figure 27. Typical Protection of the Operational Amplifier Inputs**

**Rail-to-Rail Output**

The maximum output voltage swing is dependent of the particular output load. According to the specification, the output can reach within 25 mV of either supply rail when load resistance is 10 kΩ. Figure 15 and Figure 16 shows the load drive capabilities of the part under different conditions. Output current is internally limited to 15 mA typ.

**Capacitive Loads**

Driving capacitive loads can create stability problems for voltage feedback opamps, as it is a known possible cause for:

- degraded phase margin
- lowered bandwidth
- gain peaking of the frequency response
- overshoot and ringing of the step response.

While the NCS/NCV20061/2/4 family of opamps are capable of driving capacitive loads up to 100pF, adding a small resistor in series to the output ( $R_{ISO}$  in Figure 28) will increase the feedback loop’s phase margin. This leads to higher stability by making the equivalent load more resistive at high frequencies.



Figure 28. Driving Capacitive Loads

Simulating the application with ON Semiconductor’s P–SPICE models is a good starting point for selecting the isolation resistor’s value, and then bench testing the frequency and step response can be used to fine–tune the value according to the desired characteristic.

**Unity Gain Bandwidth**

Interfacing a high impedance sensor’s output to a relatively low–impedance ADC input usually requires an intermediate stage to avoid unwanted interference of the two devices, and this stage needs to have a high input impedance, a low output impedance and high output current.

The unity gain buffer is recommended here (Figure 29). The ADC’s internal sampling capacitor requires a buffer front–end to recharge it faster than the sampling time, and this problem is even worse if more channels are sampled by the same ADC using an internal multiplexer. In order to achieve a settling time shorter than the multiplexed sampling rate, an RC stage is recommended between the buffer and the ADC input. The R resistor’s value should be low enough to charge the capacitor quickly, but at the same time large enough to isolate the capacitive load from the opamp’s output to preserve phase margin. When transients are generated by the sensor’s output, first the two opamp’s inputs see a high differential voltage between them, then the output settles and brings the inverting input back to the correct voltage.

To successfully accommodate for example a 0.1 V to 4 V sensor signal, the opamp’s differential input range of the NCS(V) 20061/2/4 series is close to the supply range VDD–VSS, and the output will match the input. The differential input voltage is limited only by the ESD protection structure and not by back–to–back diodes between inputs.



Figure 29. Unity Gain Buffer Stage for Sampling with ADC

**Power Supply Bypassing**

For AC, the power supply pins (VDD and VSS for split supply, VDD for single supply) should be bypassed locally with a quality capacitor in the range of 100 nF (ceramics are recommended for their low ESR and good high frequency response) as close as possible to the opamp’s supply pins.

For DC, a bulk capacitor in the range of 1 μF within inches distance from the opamp can provide the increased currents required to drive higher loads.

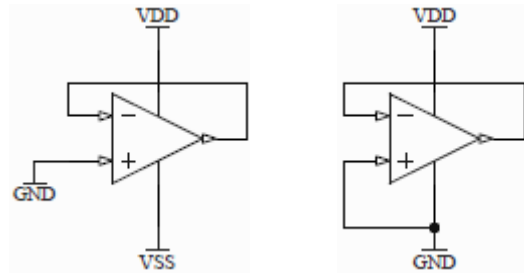


Figure 30. Unused Operational Amplifiers

**Unused Operational Amplifiers**

Occasionally not all the opamps offered in the quad packages are needed for a specific application. They can be connected as “buffering ground” as shown in Figure 30, a solution that does not need any extra parts. Connecting them differently (inputs split to rails, left floating, etc.) can sometimes cause unwanted oscillation, crosstalk, increased current consumption, or add noise to the supply rails.

**PCB Surface Leakage**

The Printed Circuit Board’s surface leakage effects should be estimated if the lowest possible input bias current is critical. Dry environment surface current increases further when the board is exposed to humidity, dust or chemical contamination. For harsh environment conditions, protecting the entire board surface (with all the exposed metal pins and soldered areas) is advised. Conformal coating or potting the board in resin proves effective in most cases.

An alternate solution for reduced leakage is the use of guard rings around sensitive pins and pads. A proper guard ring should have low impedance and be biased to the same voltage as the sensitive pin so no current flows in between.

For an inverting amplifier, the non-inverting input is usually connected to supply's ground (or virtual ground at half the rail voltage in single supply applications) so it can represent a good ring solution. When routing the PCB traces, create a closed perimeter around the inverting input pad (which carries the signal) and connect it to the non-inverting input.

For a non-inverting amplifier, use a similarly shaped (rectangle or circle) copper trace around the non-inverting input pad (which carries the signal) and connect it to the inverting input pin, which presents a much lower impedance thanks to the feedback network.

**PCB Routing Recommendations**

Even when some operational amplifier is expected to amplify only the useful DC signal, it can also pick some high frequency noise altogether and amplify it accordingly, if the design allows it. In order to reach the specified operational amplifier parameters and to avoid high frequency

interference issues, it is recommended that the PCB layout respects some basic guidelines:

- A dedicated layer for the ground plane should be used whenever possible and all supply decoupling capacitors should connect to it by vias.
- Copper traces should be as short as possible.
- High current paths should not be shared by small signal or low current traces.
- If present, switching power supply blocks should be kept away from the analog sensitive areas to avoid potential conducted and radiated noise issues.
- When different circuit taxonomies share the same board, it is recommended to keep separated the power areas, the digital areas and the small signal analog areas. Small-signal parts in the signal path should be placed as close as possible to the opamp's input pins.
- Metal shielding the sensitive areas and the "offender" blocks may be required in some cases.

In a sensitive application, a good PCB design can take longer but it will save troubleshooting time.

**Applications Example**

**Second Order Active Low Pass Filter**

Using an opamp with a low input bias current allows the use of higher value resistors and smaller capacitors for the same filter application. As a trade-off for the increased impedance and lower consumption obtained, the higher value resistors may also bring higher noise and sensibility to board contamination, and possibly frequency response changes (the increased R\*C time constant due to parasitic capacitances can change the gain vs. frequency plot).

An example of an active low-pass filter using the NCS2006x operational amplifier can be found in Figure 31. The filter's 3 dB Bandwidth is approximately 25 KHz, followed by a -40 dB/dec roll-off as in Figure 32. Such filters with flat response in the sampled signal band are recommended as a front-end for ADC's to avoid aliasing.



**Figure 31. Second Order Active Low Pass Filter**



**Figure 32. Filter's Frequency Response**

Using the P-SPICE models provided by ON Semiconductor is recommended as a starting point for component selection, and then values can be further fine-tuned during bench testing the application.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



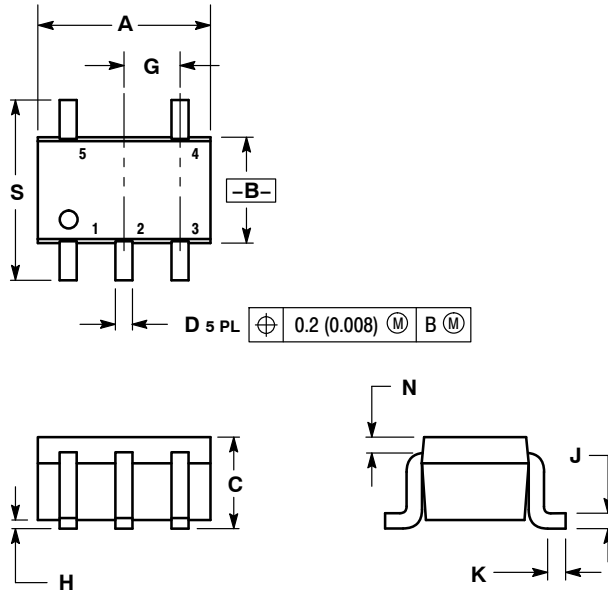
### SC-88A (SC-70-5/SOT-353)

#### CASE 419A-02

#### ISSUE L

SCALE 2:1

DATE 17 JAN 2013

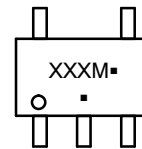


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

### GENERIC MARKING DIAGRAM\*

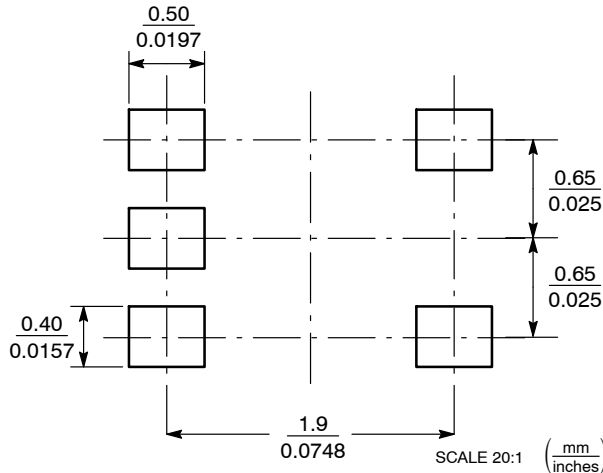


- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDER FOOTPRINT



STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 2:  
PIN 1. ANODE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. CATHODE

STYLE 3:  
PIN 1. ANODE 1  
2. N/C  
3. ANODE 2  
4. CATHODE 2  
5. CATHODE 1

STYLE 4:  
PIN 1. SOURCE 1  
2. DRAIN 1/2  
3. SOURCE 1  
4. GATE 1  
5. GATE 2

STYLE 5:  
PIN 1. CATHODE  
2. COMMON ANODE  
3. CATHODE 2  
4. CATHODE 3  
5. CATHODE 4

STYLE 6:  
PIN 1. EMITTER 2  
2. BASE 2  
3. EMITTER 1  
4. COLLECTOR  
5. COLLECTOR 2/BASE 1

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 8:  
PIN 1. CATHODE  
2. COLLECTOR  
3. N/C  
4. BASE  
5. EMITTER

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. ANODE

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<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>SC-88A (SC-70-5/SOT-353)</b>	<b>PAGE 1 OF 2</b>





ISSUE	REVISION	DATE
C	CONVERTED FROM PAPER DOCUMENT TO ELECTRONIC. REQ. BY N LAFEBRE.	20 JUN 1998
D	CONVERTED FROM MOTOROLA TO ON SEMICONDUCTOR. ADDED STYLE 5. REQ. BY E. KIM.	24 JUL 2000
E	ADDED STYLES 6 & 7. REQ. BY S. BACHMAN.	03 AUG 2000
F	DELETED DIMENSION V, WAS 0.3-0.44MM/0.012-0.016IN. REQ. BY G. KWONG.	14 JUN 2001
G	ADDED STYLE 8, REQ. BY S. CHANG; ADDED STYLE 9, REQ. BY S. BACHMAN; ADDED NOTE 4, REQ. BY S. RIGGS	25 JUN 2003
H	CHANGED STYLE 6. REQ. BY C. LIM	28 APR 2005
J	CHANGED TITLE DESCRIPTION. REQ. BY B. LOFTS.	31 AUG 2005
K	CORRECTED TITLE AND DESCRIPTION TO SC-88A (SC-70-5/SOT-353). CORRECTED MARKING DIAGRAM. REQ. BY D. TRUHITTE.	13 JUL 2010
L	ADDED SOLDER FOOTPRINT. REQ. BY I. MARIANO.	17 JAN 2013

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

## TSOP-5 CASE 483 ISSUE M

DATE 17 MAY 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

### SOLDERING FOOTPRINT\*

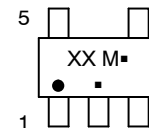


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



Analog



Discrete/Logic

- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package
- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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DESCRIPTION:	TSOP-5	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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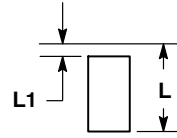
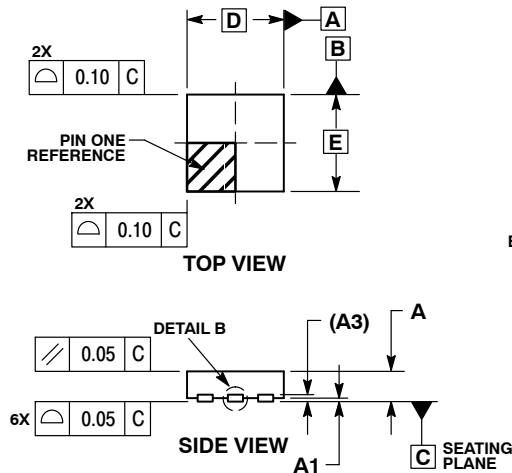


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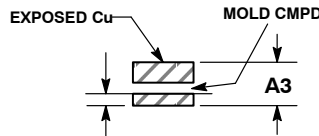
DATE 26 OCT 2007



SCALE 4:1



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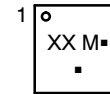
DETAIL B  
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CONSTRUCTION

NOTES:

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2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

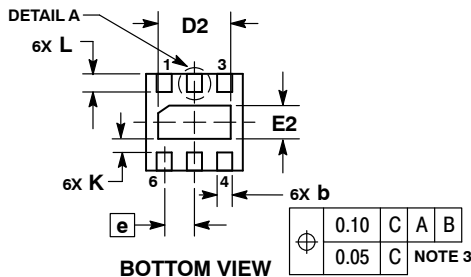
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A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D2	1.10	1.30
E2	0.45	0.65
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

### GENERIC MARKING DIAGRAM\*

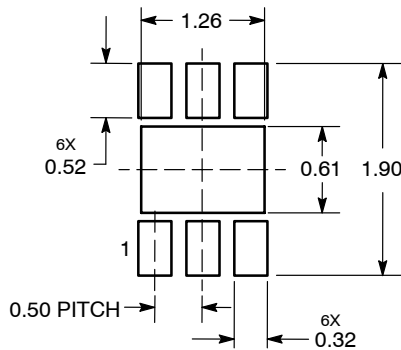


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)  
\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "■", may or may not be present.



### SOLDERMASK DEFINED MOUNTING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON25711D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>6 PIN UDFN, 1.6X1.6, 0.5P</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p><b>STYLE 2:</b><br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p><b>STYLE 6:</b><br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p><b>STYLE 7:</b><br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p><b>STYLE 11:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p><b>STYLE 14:</b><br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p><b>STYLE 18:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p><b>STYLE 19:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p><b>STYLE 26:</b><br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p><b>STYLE 27:</b><br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p><b>STYLE 28:</b><br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p><b>STYLE 29:</b><br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |   |   |

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<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### STYLES ON PAGE 2

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DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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<b>DESCRIPTION:</b>	<b>SOIC-14 NB</b>	<b>PAGE 2 OF 2</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW



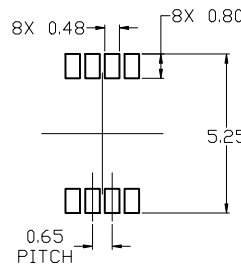
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H<sub>E</sub></i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

<b>DOCUMENT NUMBER:</b>	<b>98ASB14087C</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>MICRO8</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT**

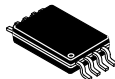


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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

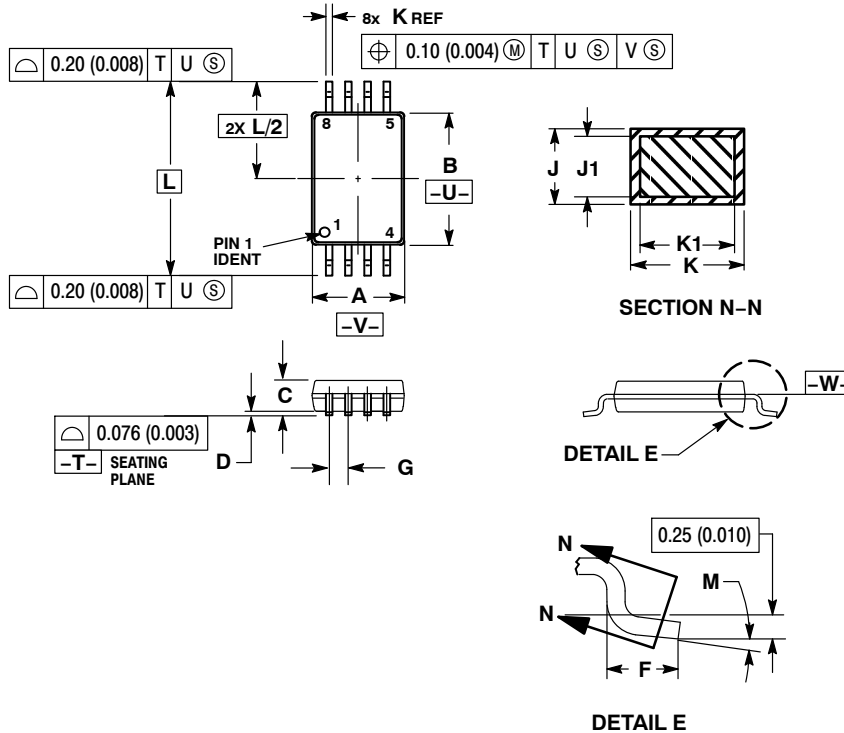
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SCALE 2:1

TSSOP-8  
CASE 948S-01  
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DATE 20 JUN 2008

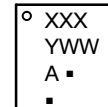


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC  
MARKING DIAGRAM\*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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