- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range: 0°C to 70°C ... 3 V to 16 V -40°C to 85°C ... 4 V to 16 V -55°C to 125°C ... 5 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Types)

- Low Noise . . . 68 nV/√Hz Typically at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . $10^{12} \Omega$ Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

description

The TLC27L1 operational amplifier combines a wide range of input offset-voltage grades with low offset-voltage drift and high input impedance. In addition, the TLC27L1 is a low-bias version of the TLC271 programmable amplifier. These devices use the Texas Instruments silicon-gate LinCMOS[™] technology, which provides offset-voltage stability far exceeding the stability available with conventional metal-gate processes.

Three offset-voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L1 (10 mV) to the TLC27L1B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS[™] operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L1. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input-voltage range includes the negative rail.

The device inputs and output are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC27L1 incorporates internal electrostatic-discharge (ESD) protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

		PACH	AGE
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV 5 mV 10 mV	TLC27L1BCD TLC27L1ACD TLC27L1CD	TLC27L1BCP TLC27L1ACP TLC27L1CP
–40°C to 85°C	2 mV 5 mV 10 mV	TLC27L1BID TLC27L1AID TLC27L1ID	TLC27L1BIP TLC27L1AIP TLC27L1IP
-55°C to 125°C	10 mV	TLC27L1MD	TLC27L1MP

AVAILABLE OPTIONS



The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L1BCDR).



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TLC27L1, TLC27L1A, TLC27L1B LinCMOS[™] LOW-POWER **OPERATIONAL AMPLIFIERS**

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description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from - 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic





TLC27L1, TLC27L1A, TLC27L1B LinCMOS™ LÓW-POWER **OPERATIONAL AMPLIFIERS**

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage, VID (see Note 2)	±Vחס
Input voltage range, V _I (any input)	0.3 V to V
Input current, I	±5 mÅ
Output current, I _O	±30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature, T _A : C suffix	0°C to 70°C
	– 40°C to 85°C
M suffix	– 55°C to 125°C
Storage temperature range, T _{sta}	– 65°C to 150°C
Case temperature for 60 seconds, T _C : FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	ge 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

			C SUFFIX		I SUFFIX		M SUFFIX		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
Supply voltage, V _{DD}		3	16	4	16	5	16	V	
	$V_{DD} = 5 V$	-0.2	3.5	-0.2	3.5	0	3.5	N/	
Common-mode input voltage, VIC	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	V	
Operating free-air temperature, T _A		0	70	-40	85	-55	125	°C	



TLC27L1, TLC27L1A, TLC27L1B LinCMOS™ LOW-POWER OPERATIONAL AMPLIFIERS

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electrical characteristics at specified free-air temperature (unless otherwise noted)

					TLC	27L1C,	TLC27	L1AC, TLC27L1BC			
	PARAMETER			TAT	V	DD = 5	V	V	D = 10	٧	UNIT
			CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	
				25°C		1.1	10		1.1	10	
		TLC27L1C	$V_{0} = 1.4 V$	Full range			12			12	
	· · · · ·	_	$V_{\rm IC} = 0 V_{\rm V}$	25°C		0.9	5		0.9	5	
VIO	Input offset voltage	ILC27L1AC	$R_S = 50 \Omega$,	Full range			6.5			6.5	mV
			R _I = 1 MΩ	25°C		0.24	2		0.26	2	
		TLC27L1BC		Full range			3			3	1
ανιο	Average temperature coefficient of VIO input offset voltage			25°C to 70°C		1.1			1		μV/°C
			$V_{O} = V_{OO}/2$,	25°C		0.1	60		0.1	60	pА
IO	Input offset current (see	Note 4)	$V_{IC} = V_{DD}/2$	70°C		7	300		8	300	
			$V_{O} = V_{OO}/2$	25°C		0.6	60		0.7 60		
IВ	B Input bias current (see Note 4)		$V_{IC} = V_{DD}/2$	70°C		40	600		50	600	рА
Common-mode input			25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V	
VICR	VICR voltage range (see Note 5)			Full range	-0.2 to 3.5			-0.2 to 8.5			V
			$V_{ID} = 100 \text{ mV},$ R _L = 1 M Ω	25°C	3.2	4.1		8	8.9		
∨он	High-level output voltage	put voltage		0°C	3	4.1		7.8	8.9		V
				70°C	3	4.2		7.8	8.9		
			100 M	25°C		0	50		0	50	
VOL	Low-level output voltage	9	$V_{ID} = -100 \text{ mV},$	0°C		0	50		0	50	mV
			·OL ·	70°C		0	50		0	50	
	Leave stars by the second star		D (110)	25°C	50	520		50	870		
AVD	voltage amplification		$R_L = 1 M\Omega$, See Note 6	0°C	50	700		50	1030		V/mV
				70°C	50	380		50	660		
				25°C	65	94		65	97		
CMRR	Common-mode rejection	n ratio	$V_{IC} = V_{ICR}min$	0°C	60	95		60	97		dB
				70°C	60	95		60	97		
				25°C	70	97		70	97		
k SVR	Supply-voltage rejection $(\Delta V \cap \Delta V)$	ratio	$V_{DD} = 5 V to 10 V$, $V_{O} = 1.4 V$	0°C	60	97		60	97		dB
			Ŭ	70°C	60	98		60	98		1
II(SEL)	Input current (BIAS SEL	ECT)	V _{I(SEL)} = V _{DD}	25°C		65			95		nA
			$V_{O} = V_{DD}/2$,	25°C		10	17		14	23	
IDD	Supply current		$V_{IC} = V_{DD}/2$,	0°C		12	21		18	33	μA
			No load	70°C		8	14		11	20	1

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At $V_{DD} = 5 V$, $V_{O} = 0.25 V$ to 2 V; at $V_{DD} = 10 V$, $V_{O} = 1 V$ to 6 V.



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electrical characteristics at	specified free-air tem	nperature (unless otherwi	ise noted)
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TLC27L1I, TLC27L1AI,					L1AI, T	LC27L1	BI				
	PARAMETER			т _А †	V	DD = 5	V	٧Ľ	_{DD} = 10	٧	UNIT
			CONDITIONO		MIN	TYP	MAX	MIN	TYP	MAX	
		TI 007141		25°C		1.1	10		1.1	10	
		TLC27L11	$V_{0} = 1.4 V$	Full range			13			13	
		-	$V_{IC} = 0 V_{,}$	25°C		0.9	5		0.9	5	.,
VIO	Input offset voltage	TLC27L1AI	R _S = 50 Ω,	Full range			7			7	mv
			$R_L = 1 M\Omega$	25°C		0.24	2		0.26	2	
		TLC27L1BI		Full range			3.5			3.5	1
ανιο	Average temperature co of input offset voltage	efficient		25°C to 85°C		1.1			1		μV/°C
			$V_{O} = V_{OO}/2$	25°C		0.1	60		0.1	60	pА
IO	Input offset current (see	Note 4)	$V_{IC} = V_{DD}/2$	85°C		24	1000		26	1000	
			$V_{\Omega} = V_{\Omega \Omega}/2$	25°C		0.6	60		0.7	60	
IВ	Input bias current (see I	Note 4)	$V_{IC} = V_{DD}/2$	85°C		200	2000		220	2000	рА
VICR Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V	
			Full range	-0.2 to 3.5			-0.2 to 8.5			V	
			$\label{eq:VID} \begin{array}{ c c c c c } V_{ID} = 100 \text{ mV}, \\ R_L = 1 \text{ M}\Omega \end{array} \qquad \begin{array}{ c c c c c } \hline 25^\circ \text{C} & 3 & 4.1 \\ \hline -40^\circ \text{C} & 3 & 4.1 \\ \hline 85^\circ \text{C} & 3 & 4.2 \end{array}$	25°C	3	4.1		8	8.9		
∨он	VOH High-level output voltage	e			7.8	8.9		V			
				85°C	3	4.2		7.8	8.9		
			100	25°C		0	50		0	50	
VOL	Low-level output voltage)	V D = -100 mV,	-40°C		0	50		0	50	mV
			OL V	85°C		0	50		0	50	
	Lenne stored d'Mener Cel			25°C	50	520		50	870		
AVD	voltage amplification		See Note 6	-40°C	50	900		50	1550		V/mV
	· · · · · · · · · · · · · · · · · · ·			85°C	50	330		50	585		
				25°C	65	94		65	97		
CMRR	Common-mode rejection	n ratio	$V_{IC} = V_{ICR}min$	-40°C	60	95		60	97		dB
				85°C	60	95		60	98		
				25°C	70	97		70	97		
k SVR	Supply-voltage rejection	ratio	$V_{DD} = 5 V \text{ to } 10 V$, $V_{O} = 1.4 V$	−40°C	60	97		60	97		dB
			10	85°C	60	98		60	98		1
II(SEL)	Input current (BIAS SEL	ECT)	$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
			$V_{\Omega} = V_{\Omega \Omega}/2$	25°C		10	17		14	23	1
IDD	Supply current		$V_{IC} = V_{DD}/2$,	-40°C		16	27		25	43	μΑ
			No load	85°C		17	13		10	18	

[†]Full range is –40 to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At $V_{DD} = 5 V$, $V_{O} = 0.25 V$ to 2 V; at $V_{DD} = 10 V$, $V_{O} = 1 V$ to 6 V.



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electrical characteristics at specified free-air temperature (unless otherwise note

						TLC2	7L1M			
	PARAMETER		T _A †	V	DD = 5	V	V	D = 10	V	UNIT
		CONDITIONO		MIN	TYP	MAX	MIN	TYP	MAX	
N/ a	Innut effect veltege	$V_{O} = 1.4 V,$ $V_{IC} = 0 V,$	25°C		1.1	10		1.1	10	
۷IO	input onset voltage	$R_S = 50 \Omega$, $R_L = 1 M\Omega$	Full range			12			12	mv
αΛΙΟ	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
	In must offer at automate (as a Nieta d)	$V_{O} = V_{DD}/2,$	25°C		0.1	60		0.1	60	pА
١O	Input offset current (see Note 4)	$V_{IC} = V_{DD}/2$	125°C		1.4	15		1.8	15	nA
	hand him a sum of (and him a)	$V_{O} = V_{DD}/2$,	25°C		0.6	60		0.7	60	pА
IВ	Input bias current (see Note 4)	$V_{IC} = V_{DD}/2$	125°C		9	35		10	35	nA
VICR	Common-mode input		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V
	voltage range (see Note 5)		Full range	0 to 3.5			0 to 8.5			V
			25°C	3.2	4.1		8	8.9		
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$ R _I = 1 MO	-55°C	3	4.1		7.8	8.8		V
			125°C	3	4.2		7.8	9		
			25°C		0	50		0	50	mV
VOL	Low-level output voltage	$V_{\rm ID} = -100 {\rm mV},$	-55°C		0	50		0	50	
		10L - 0	125°C		0	50		0	50	
			25°C	50	520		50	870		
AVD	Large-signal differential	$R_L = 1 M\Omega$, See Note 6	−55°C	25	1000		25	1775		V/mV
			125°C	25	200		25	380]
			25°C	65	94		65	97		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	-55°C	60	95		60	97		dB
			125°C	60	85		60	91		
			25°C	70	97		70	97		
k SVR	Supply-voltage rejection ratio	$V_{DD} = 5 V \text{ to } 10 V,$	−55°C	60	97		60	97		dB
		VU V	125°C	60	98		60	98		
II(SEL)	Input current (BIAS SELECT)	$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
		$V_{\Omega} = V_{\Omega \Omega}/2$	25°C		10	17		14	23	
IDD	Supply current	$V_{\text{IC}} = V_{\text{DD}}/2,$ $V_{\text{IC}} = V_{\text{DD}}/2,$	−55°C		17	30		28	48	μΑ
		No load	125°C		7	12		9	15	

[†] Full range is -55° C to 125° C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically. 5. This range also applies to each input individually.

6. At $V_{DD} = 5 V$, $V_{O} = 0.25 V$ to 2 V; at $V_{DD} = 10 V$, $V_{O} = 1 V$ to 6 V.



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•	0	•							
	PARAMETER		TEST CONDITIONS			TLC27L1C, TLC27L1AC, TLC27L1BC			
					MIN	TYP	MAX		
				25°C		0.03			
			VI(PP) = 1 V	0°C		0.04		V/µs	
00		$R_L = 1 MΩ,$ $C_L = 20 pF,$ See Figure 33		70°C		0.03			
58	Siew rate at unity gain			25°C		0.03			
			VI(PP) = 2.5 V	0°C		0.03			
			、 <i>`</i>	70°C		0.02			
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R _S = 20 Ω,	25°C		68		nV/√Hz	
				25°C		5			
Вом	Maximum output-swing bandwidth	$V_{O} = V_{OH}$	$C_L = 20 \text{ pF},$	0°C		6		kHz	
		1×2^{-1} 1×2^{-1}	See Figure 55	70°C		4.5			
				25°C		85			
B ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	0°C		100		kHz	
		See Figure 35		70°C		65		1	
			<i>.</i>	25°C		34°			
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1,$	0°C		36°			
	-	CL = 20 pF,	See Figure 55	70°C		30°]	

operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST CC	TEST CONDITIONS			TLC27L1C, TLC27L1AC, TLC27L1BC		
					ΜΙΝ ΤΥ	P MAX		
				25°C	0.0)5		
			VI(PP) = 1 V	0°C	0.0)5		
CD.	Slew rate at unity gain	$R_L = 1 M\Omega$,		70°C	0.0)4		
SK		See Figure 33		25°C	0.0)4	v/µs	
			VI(PP) = 5.5 V	0°C	0.0)5		
			× ,	70°C	0.0)4		
V _n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R _S = 20 Ω,	25°C	6	8	nV/√Hz	
				25°C		1	kHz	
ВОМ	Maximum output-swing bandwidth	$V_{O} = V_{OH}$	$C_{L} = 20 \text{ pF},$	0°C	1	.3		
		$R_{L} = 1.0132$,	See Figure 55	70°C	0	.9		
				25°C	11	0		
B ₁	Unity-gain bandwidth	$V_{\rm I} = 10 {\rm mV},$	CL = 20 pF,	0°C	12	25	kHz	
		See Figure 55		70°C	ę	00		
			(F	25°C	3	3°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$	t = B ₁ , See Figure 35	0°C	4)°		
	5	ο _L – 20 pi ,	oce i igure 55	70°C	3	1°]	



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operating characteristics at specified free-air temperature, V_{DD} = 5 V

	PARAMETER	TEST CO	TEST CONDITIONS			TLC27L1I, TLC27L1AI, TLC27L1BI		
					MIN	TYP	MAX	
				25°C		0.03		
			VI(PP) = 1 V	-40°C		0.04		
0.0	Slew rate at unity gain	$R_L = 1 M\Omega$,		85°C		0.03]
SK		See Figure 33		25°C		0.03		v/µs
			VI(PP) = 2.5 V	-40°C		0.04		
				85°C		0.02		
V _n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R _S = 20 Ω,	25°C		68		nV/√Hz
				25°C		5		
ВОМ	Maximum output-swing bandwidth	$V_{O} = V_{OH}$	$C_{L} = 20 \text{ pF},$	-40°C		7		kHz
		1×1^{-1} 1 10122,	See Figure 35	85°C		4		
				25°C		85		
B ₁	Unity-gain bandwidth	V _I = 10 mV,	CL = 20 pF,	-40°C		130		MHz
		Occ right 55		85°C		55		
			<i>.</i> .	25°C		34°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$	t = B ₁ , See Figure 35	-40°C		38°		
	· · · · · · · · · · · · · · · · · · ·	Ο _L – 20 pi ,	oce i igure 55	85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER TEST CONDIT			ONDITIONS	NS T _A		TLC27L1C, TLC27L1AC, TLC27L1BC		UNIT
					MIN	TYP	MAX	
	Slew rate at unity gain	$R_L = 1 MΩ,$ $C_L = 20 pF,$ See Figure 33	VI(PP) = 1 V	25°C		0.05		V/µs
				-40°C		0.06		
CD.				85°C		0.03		
SK			V _{I(PP)} = 5.5 V	25°C		0.04		
				-40°C		0.05		
				85°C		0.03		
V _n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R _S = 20 Ω,	25°C		68		nV/√Hz
Вом	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ R _L = 1 MΩ,	C _L = 20 pF, See Figure 33	25°C		1		kHz
				-40°C		1.4		
				85°C		0.8		
	Unity-gain bandwidth	VI = 10 mV, See Figure 35	C _L = 20 pF, 5	25°C		110		MHz
B ₁				-40°C		155		
				85°C		80		
φm	Phase margin	$V_{I} = 10 \text{ mV,I}$	f = B ₁ , See Figure 35	25°C		38°		
				-40°C		42°		
		$O_{L} = 20 \text{ pr}$	occ rigare 55	85°C		32°		



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PARAMETER		TEST CONDITIONS		TA	TLC27L1M			
					MIN	TYP	MAX	UNIT
	Slew rate at unity gain	R _L = 1 MΩ, C _L = 20 pF, See Figure 33	VI(PP) = 1 V	25°C		0.03		V/µs
				−55°C		0.04		
				125°C		0.02		
SR			V _{I(PP)} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R _S = 20 Ω,	25°C		68		nV/√Hz
	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ R _L = 1 MΩ,	C _L = 20 pF, See Figure 33	25°C		5		kHz
^В ОМ				−55°C		8		
				125°C		3		
	Unity-gain bandwidth	V _I = 10 mV, See Figure 35	C _L = 20 pF,	25°C		85		kHz
B ₁				−55°C		140		
				125°C		45		
φm	Phase margin	VI = 10 mV, CL = 20 pF,	f = B ₁ , See Figure 35	25°C		34°		
				-55°C		39°		
				125°C		25°		

operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

operating characteristics at specified free-air temperature, V_{DD} = 10 V

			TEAT CONDITIONS		TLC27L1M			
PARAMETER		TEST CONDITIONS		'A	MIN	TYP	MAX	UNIT
	Slew rate at unity gain	$R_L = 1 MΩ,$ $C_L = 20 pF,$ See Figure 33	VI(PP) = 1 V	25°C		0.05		V/µs
				−55°C		0.06		
				125°C		0.03		
SK			VI(PP) = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V _n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R _S = 20 Ω,	25°C		68		nV/√Hz
BOM	Maximum output-swing bandwidth	$V_O = V_{OH},$ R _L = 1 MΩ,	C _L = 20 pF, See Figure 33	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
	Unity-gain bandwidth	V _I = 10 mV, See Figure 35	C _L = 20 pF,	25°C		110		kHz
B ₁				−55°C		165		
				125°C		70		
φm	Phase margin	VI = 10 mV, C _L = 20 pF,	f = B ₁ , See Figure 35	25°C		38°		
				−55°C		43°		
				125°C		29°		



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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
VIO	Input offset voltage	Distribution	1, 2
ανιο	Temperature coefficient	Distribution	3, 4
VOH	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	5, 6 7 8
V _{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	9, 10 11 12 13, 14
AVD	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	15 16 27, 28
I _{IB}	Input bias current	vs Free-air temperature	17
lio	Input offset current	vs Free-air temperature	17
VI	Maximum input voltage	vs Supply voltage	18
IDD	Supply current	vs Supply voltage vs Free-air temperature	19 20
SR	Slew rate	vs Supply voltage vs Free-air temperature	21 22
	Bias-select current	vs Supply voltage	23
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	24
В ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	25 26
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive load	29 30 31
Vn	Equivalent input noise voltage	vs Frequency	32
	Phase shift	vs Frequency	27, 28















































[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L1 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.





(a) SINGLE SUPPLY





PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits (continued)



Figure 35. Gain-of-100 Inverting Amplifier

input bias current

Due to the high input impedance of the TLC27L1 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 36). Leakages that would otherwise flow to the inputs are shunted away.
- 2. Compensate for the leakage of the test socket by actually performing an input bias-current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.



PARAMETER MEASUREMENT INFORMATION



Figure 36. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. When conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset-voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset-voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset-voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Since there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit in Figure 33. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 37). A square wave allows a more accurate determination of the point at which the maximum peak-to-peak output is reached.



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full-power response (continued)



Figure 37. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLC27L1 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a





reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low-input bias-current consumption of the TLC27L1 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L1 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- 1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



single-supply operation (continued)



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

input offset voltage nulling

The TLC27L1 offers external input-offset null control. Nulling of the input-offset voltage may be achieved by adjusting a $25-k\Omega$ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 40. Total nulling may not be possible.



Figure 40. Input Offset-Voltage Null Circuit

input characteristics

The TLC27L1 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.5$ V at all other temperatures.



input characteristics (continued)

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L1 very good input offset-voltage drift characteristics relative to conventional metal-gate processes. Offset-voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset-voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLC27L1 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 36 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 41).

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low-input bias-current requirements of the TLC27L1 results in a very-low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.







(a) NONINVERTING AMPLIFIER

(b) INVERTING AMPLIFIER

Figure 41. Guard-Ring Schemes

(c) UNITY-GAIN AMPLIFIER



feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 42). The value of this capacitor is optimized empirically.



electrostatic discharge protection

Figure 42. Compensation for Input Capacitance

The TLC27L1 incorporates an internal ESD protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L1 inputs and output were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established when latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.



output characteristics

The output stage of the TLC27L1 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage (see Figure 43).

All operating characteristics of the TLC27L1 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 44). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



Figure 43. Test Circuit for Output Characteristics



Figure 44. Effect of Capacitive Loads in Low-Bias Mode

Although the TLC27L1 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 45). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of R_P , a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.









NOTE A: d = damping factor, I/O





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NOTES: A. $V_{O(PP)} = 8 V$ B. $V_{O(PP)} = 4 V$





Figure 48. Amplifier With Digital-Gain Selection



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Figure 51. Set/Reset Flip-Flop



NOTE A: Normalized to F_{C} = 1 kHz and R_{L} = 10 $k\Omega$

Figure 52. Two-Pole Low-Pass Butterworth Filter



MECHANICAL INFORMATION

PLASTIC SMALL-OUTLINE PACKAGE

D (R-PDSO-G**) 14 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad.
- E. Falls within JEDEC MS-012



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