agere systems

Data Sheet
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L9215A/G
Short-Loop Sine Wave Ringing SLIC

Introduction

The Agere Systems Inc. L9215 is a subscriber line interface circuit that is optimized for short-loop, power-sensitive applications. This device provides the complete set of line interface functionality (including power ringing) needed to interface to a subscriber loop. This device has the capability to operate with a V_{CC} supply of 3.3 V or 5 V and is designed to minimize external components required at all device interfaces.

Features

- Onboard ringing generation
- Three ringing input options:
  — Sine wave
  — PWM
  — Logic level square wave
- Flexible V_{CC} options:
  — 5 V or 3.3 V V_{CC}
  — No –5 V required
- Battery switch to minimize off-hook power
- 11 operating states:
  — Scan mode for minimal power dissipation
  — Forward and reverse battery active
  — On-hook transmission states
  — Meter pulse states
  — Ring mode
  — Disconnect mode
- Ultralow on-hook power:
  — 27 mW scan mode
  — 42 mW active mode
- Two SLIC gain options to minimal external components in codec interface
- Loop start, ring trip, and ground key detectors
- Software- or hardware-controllable current-limit and overhead voltage
- Meter pulse compatible
- 32-pin PLCC package
- 48-pin MLCC package

Applications

- Voice over Internet Protocol (VoIP)
- Cable Modems
- Terminal Adapters (TA)
- Wireless Local Loop (WLL)
- *Telcordia Technologies*™ GR-909 Access
- Network Termination (NT)
- Key Systems

Description

This device is optimized to provide battery feed, ringing, and supervision on short-loop plain old telephone service (POTS) loops.

This device provides power ring to the subscriber loop through amplification of a low-voltage input. It provides forward and reverse battery feed states, on-hook transmission, a low-power scan state, meter pulse states, and a forward disconnect state.

The device requires a V_{CC} and battery to operate. V_{CC} may be either a 5 V or a 3.3 V supply. The ringing signal is derived from the high-voltage battery. A battery switch is included to allow for use of a lower-voltage battery in the off-hook mode, thus minimizing short-loop off-hook power.

Loop closure, ring trip, and ground key detectors are available. The loop closure detector has a fixed threshold with hysteresis. The ring trip detector requires a single-pole filter, thus minimizing external components required.

This device supports meter pulse applications. Meter pulse is injected into a dedicated meter pulse input. Injection of meter pulse onto tip and ring is controlled by the device's logic input pin.

Both the dc current limit and overhead voltage are programmable. Programming may be done by external resistors or an applied voltage source. If the voltage source is programmable, the current limit and overhead may be set via software control.

The device is offered with two gain options. This allows for an optimized codec interface, with minimal external components regardless of whether a first-generation or a programmable third-generation codec is used.

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Features

- Onboard balanced ringing generation:
  - — No ring relay
  - — No bulk ring generator required
  - — 15 Hz to 70 Hz ring frequency supported
  - — Sine wave input-sine wave output
  - — PWM input-sine wave output
  - — Square wave input-trapezoidal output
- Power supplies requirements:
  - — V_{CC} talk battery and ringing battery required
  - — No –5 V supply required
  - — No high-voltage positive supply required
- Flexible Vcc options:
  - — 5 V or 3.3 V V_{CC} operation
  - — 5 V or 3.3 V V_{CC} interchangeable and transparent to users
- Logic-controlled battery switch:
  - — Minimize off-hook power dissipation
- Minimal external components required
- 11 operating states:
  - — Forward active, V_{BAT2} applied
  - — Polarity reversal active, V_{BAT2} applied
  - — On-hook transmission, V_{BAT1} applied
  - — On-hook transmission polarity reversal, V_{BAT1} applied
  - — PPM active forward active, V_{BAT2} applied
  - — PPM active polarity reversal active, V_{BAT2} applied
  - — PPM active on-hook transmission, V_{BAT1} applied
  - — PPM active on-hook transmission polarity reversal, V_{BAT1} applied
  - — Scan
  - — Forward disconnect
  - — Ring mode
- Unlatched parallel data control interface
- Ultralow SLIC power:
  - — Scan 38 mW (V_{CC} = 5 V)
  - — Forward/reverse active 57 mW (V_{CC} = 5 V)
  - — Scan 27 mW (V_{CC} = 3.3 V)
  - — Forward/reverse active 42 mW (V_{CC} = 3.3 V)
- Supervision:
  - — Loop start, fixed threshold with hysteresis
  - — Ring trip, single-pole ring trip filtering, fixed threshold as a function of battery voltage
  - — Common-mode current for ground key applications, user-adjustable threshold
- Adjustable current limit:
  - — 10 mA to 70 mA programming range
- Overhead voltage:
  - — Clamped typically <51 V differentially
  - — Clamped maximum <56.5 V single-ended
  - — Adjustable in active mode
- Thermal shutdown protection with hysteresis
- Longitudinal balance:
  - — ETSI/ITU-T balance
  - — *Telcordia Technologies* GR-909 balance
- Meter pulse compatible:
  - — Dedicated meter pulse signal input
  - — On-hook transmission of PPM
- ac interface:
  - — Two SLIC gain options to minimize external components required for interface to first- or third-generation codecs
  - — Sufficient dynamic range for direct coupling to codec output
- 32-pin PLCC package/48-pin MLCC package
- 90 V CBIC-S technology

Description

The L9215 is designed to provide battery feed, ringing, and supervision functions on short plain old telephone service (POTS) loops. This device is designed for ultralow power in all operating states.

The L9215 offers 11 operating states. The device assumes use of a lower-voltage talk battery, a higher-voltage ringing battery, and a V_{CC} supply.

The L9215 requires only a positive V_{CC} supply. No –5 V supply is needed. The L9215 can operate with a V_{CC} of either 5 V or 3.3 V, allowing for greater user flexibility. The choice of V_{CC} voltage is transparent to the user; the device will function with either supply voltage connected.

Two batteries are used:

1. A high-voltage ring battery (V_{BAT1}).
   V_{BAT1} is a maximum –75 V. V_{BAT1} is used for power ring signal amplification and for scan and on-hook transmission modes. This supply is current limited to approximately the maximum power ringing current, typically 50 mA.
2. A lower-voltage talk battery (V_{BAT2}).
   V_{BAT2} is used for active mode powering.

Description (continued)

Forward and reverse battery active modes are used for off-hook conditions. Since this device is designed for short-loop applications, the lower-voltage V_{BAT2} is applied during the forward and reverse active states. Battery reversal is quiet, without breaking the ac path. Rate of battery reversal may be ramped to control switching time.

The magnitude of the overhead voltage in the forward and reverse active modes has a typical default value of 6.0 V, allowing for an undistorted signal of 3.14 dBm into 900 Ω. This overhead can be increased to accommodate higher signal levels and/or PPM. The ring trip detector is turned off during active modes to conserve power.

Because on-hook transmission is not allowed in the scan mode, an on-hook transmission mode is defined. This mode is functionally similar to the active mode, except the tip ring voltage is derived from the higher V_{BAT1} rather than V_{BAT2}.

In the on-hook transmission modes with a primary battery whose magnitude is greater than a nominal 51 V, the magnitude of the tip-to-ground and ring-to-ground voltage is clamped at less than 56.5 V.

To minimize on-hook power, a low-power scan mode is available. In this mode, all functions except off-hook supervision are turned off to conserve power. On-hook transmission is not allowed in the scan mode.

In the scan mode with a primary battery whose magnitude is greater than a nominal 51 V, the magnitude of the tip-to-ground and ring-to-ground voltage is clamped at less than 56.5 V.

A forward disconnect mode is provided, where all circuits are turned off and power is denied to the loop.

The device offers a ring mode, in which a power ring signal is provided to the tip/ring pair. During the ring mode, a user-supplied, low-voltage ring signal (ac coupled) is input to the device's $RING_{IN}$ input. This signal is amplified to produce the power ring signal. This signal may be a sine wave or filtered square wave to produce a sine wave on trapezoidal output. Ring trip detector and common-mode current detector are active during the ring mode.

This feature eliminates the need for a separate external ring relay, associated external circuitry, and a bulk ringing generator. See the Applications section of this data sheet for more information.

PPM is injected at the PPM_{IN} pin (ac coupled). This is a high-impedance input that controls the PPM differential voltage on tip and ring. The PPM signal may be present at this pin at all times; however, PPM will only be transmitted to tip and ring during a PPM active mode. There are forward and reverse active, and forward and reverse on-hook transmission modes with PPM active.

No PPM shaping is done by the device. It is assumed that a shaped PPM input is presented to PPM_{IN}.

The maximum allowed PPM current at the 200 Ω ac meter pulse load to avoid saturation of the device's internal AAC amplifier is 3 mArms. This signal level is sufficient to provide a minimum 200 mVrms to the 200 Ω PPM load under maximum specified dc loop conditions. Above 3 mArms PPM current, external meter pulse rejection may be required. See the Applications section of this data sheet for more information if on-hook transmission of PPM is required. Sufficient overhead to accommodate on-hook transmission must be programmed by the user at the OVH input.

Both the ring trip and loop closure supervision functions are included. The loop closure has a fixed typical 10.5 mA on- to off-hook threshold in the active mode and a fixed 11.5 mA on- to off-hook threshold from the scan mode. In either case, there is a 2 mA hysteresis. The ring trip detector requires only a single-pole filter at the input, minimizing external components. The ring trip threshold at a given battery voltage is fixed. Typical ring trip threshold is 42.5 mA for a –75 V V_{BAT1}.

Description (continued)

A common-mode current detector for tip or ring ground detection is included for ground key applications. The threshold is user programmable via external resistors. See the Applications section of this data sheet for more information on supervision functions.

Upon reaching the thermal shutdown temperature, the device will enter an all off mode. Upon cooling, the device will re-enter the state it was in prior to thermal shutdown. Hysteresis is built in to prevent oscillation.

Longitudinal balance is consistent with European ETSI and North American GR-909 requirements. Specifications are given in Table 6.

Data control is via a parallel unlatched control scheme.

The dc current limit is programmable in the active modes via an applied voltage source. The voltage source may be an external independent voltage source. Also, the programming voltage may be derived via a resistor divider network from the V_{REF} SLIC output. A programmable external voltage source may be used to provide software control of the loop closure threshold. Design equations for this feature are given in the dc Loop Current Limit section of the Applications section of this data sheet.

Programming range is 10 mA to 70 mA with V_{CC} = 5 V and 10 mA to 45 mA with V_{CC} = 3.3 V. Programming accuracy is ±8% at 22 mA to 28 mA current limit.

Circuitry is added to the L9215 to minimize the inrush of current from the V_{CC} supply and to the battery supply during an on- to off-hook transition, thus saving in power supply design cost. See the Applications section of this data sheet for more information.

Overhead is programmable in the active modes via an applied voltage source. The voltage source may be an external independent voltage source. Also the programming voltage may be derived via a resistor divider network from the V_{REF} SLIC output.

If the overhead is not programmed, a default overhead of approximately 6.0 V is achieved. This is adequate for a 3.14 dBm overload into 900 Ω. For the default overhead, pin OVH is connected to ground. See the Applications section of this data sheet for more information.

Transmit and receive gains have been chosen to minimize the number of external components required in the SLIC-codec ac interface, regardless of the choice of codec.

The L9215 uses a voltage feed-current sense architecture; thus, the transmit gain is a transconductance. The L9215 transconductance is set via a single external resistor, and this device is designed for optimal performance with a transconductance set at 300 V/A.

The L9215 offers an option for a single-ended to differential receive gain of either 8 or 2. These options are mask programmable at the factory and are selected by choice of code.

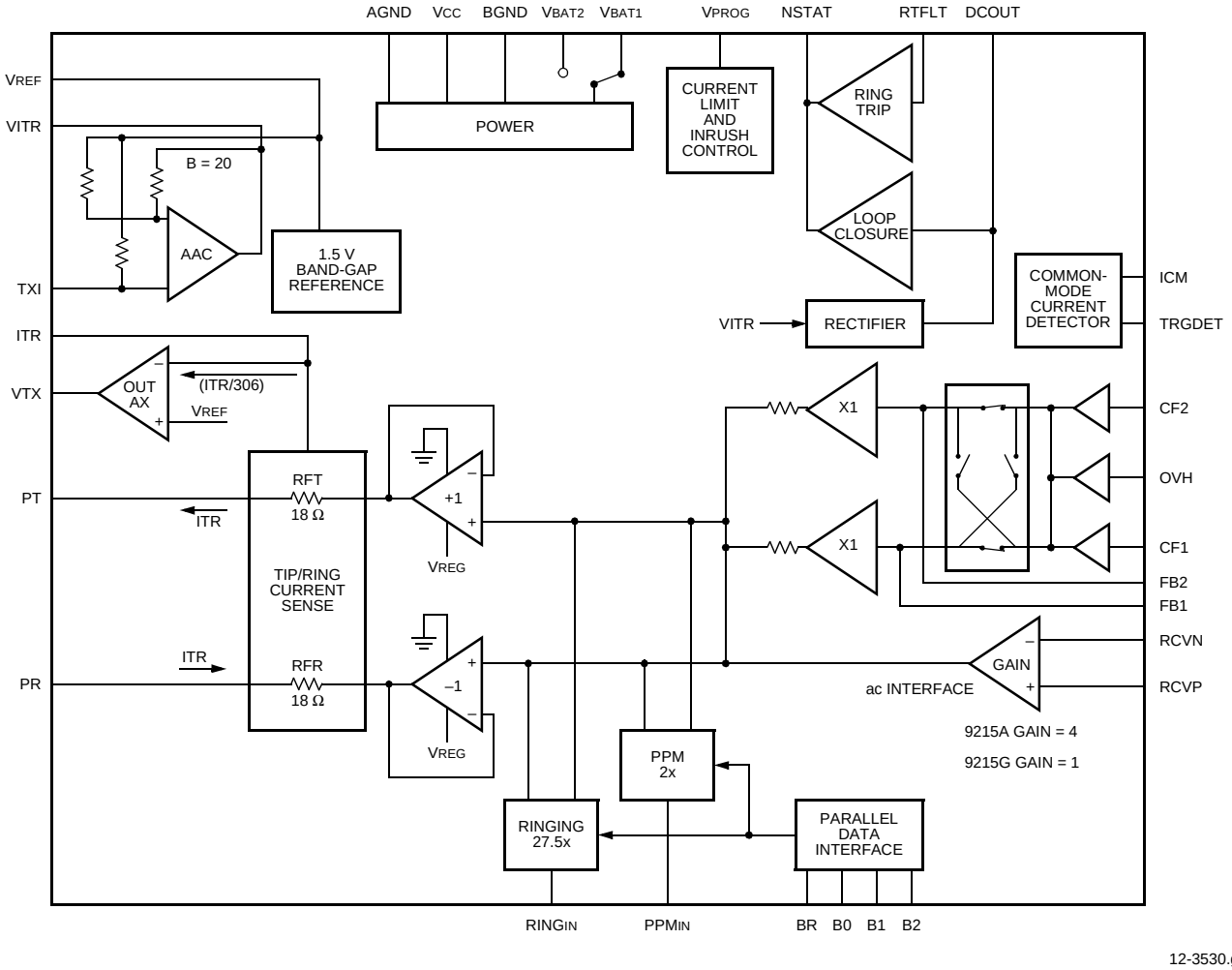
A receive gain of 8 is more appropriate when choosing a first-generation type codec where termination impedance, hybrid balance, and overall gains are set by external analog filters. The higher gain is typically required for synthesization of complex termination impedance.

A receive gain of 2 is more appropriate when choosing a third-generation type codec. Third-generation codecs will synthesize termination impedance and set hybrid balance and overall gains. To accomplish these functions, third-generation codecs typically have both analog and digital gain filters. For optimal signal-to-noise performance, it is best to operate the codec at a higher gain level. If the SLIC then provides a high gain, the SLIC output may be saturated causing clipping distortion of the signal at tip and ring. To avoid this situation, with a higher gain SLIC, external resistor dividers are used. These external components are not necessary with the lower gain offered by the L9215. See the Applications section of this data sheet for more information.

The L9215 is internally referenced to 1.5 V. This reference voltage is output at the V_{REF} output of the device. The SLIC output VITR is also referenced to 1.5 V; therefore, it must be ac coupled to the codec input. However, the SLIC inputs RCVP/RCVN are floating inputs. If there is not feedback from RCVP/RCVN to VITR, RCVP/RCVN may be directly coupled to the codec output. If there is feedback from RCVP/RCVN to VITR, RCVP/RCVN must be ac coupled to the codec output.

The L9215 is packaged in a 32-pin PLCC surface-mount package and a 48-pin MLCC ultrasmall surface-mount package. Use L9215A for gain of 8 applications and L9215G for gain of 2 applications.

Architecture Diagram



12-3530.g (F)

Figure 1. Architecture Diagram

Pin Information

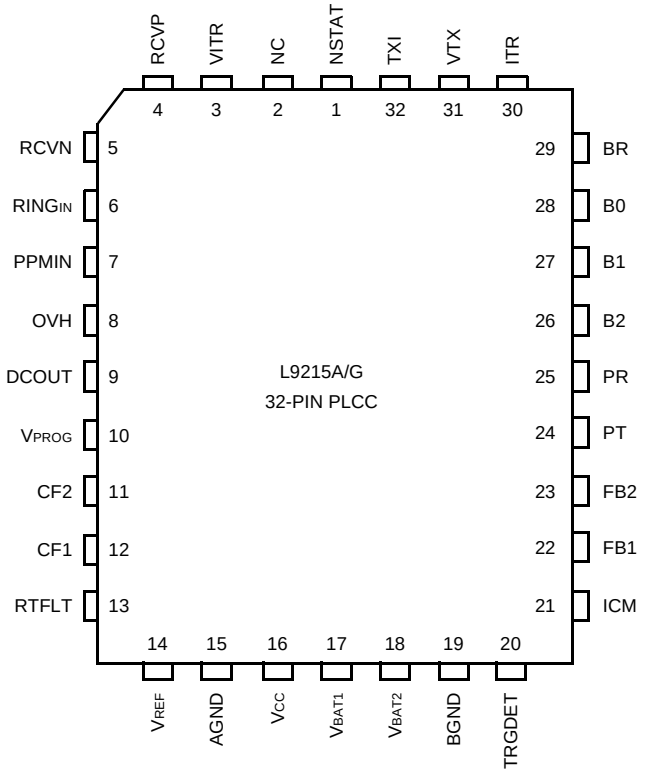


Figure 2. 32-Pin PLCC Diagram

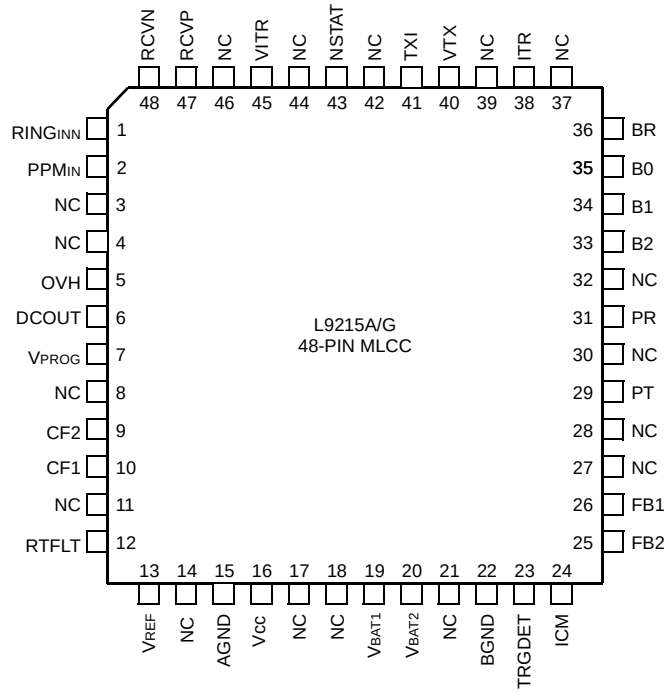


Figure 3. 48-Pin MLCC Diagram

Pin Information (continued)

Table 1. Pin Descriptions

32-Pin PLCC	48-Pin MLCC	Symbol	Type	Name/Function
1	43	NSTAT	O	**Loop Closure Detector Output—Ring Trip Detector Output.** When low, this logic output indicates that an off-hook condition exists or ringing is tripped.
2	3, 4, 8, 11, 14, 17, 18, 21, 27, 28, 30, 32, 37, 39, 42, 44, 46	NC	—	**No Connection.**
3	45	VITR	O	**Transmit ac Output Voltage.** Output of internal AAC amplifier. This output is a voltage that is directly proportional to the differential ac tip/ring current.
4	47	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls to ac differential voltage on tip and ring. This node is a floating input.
5	48	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls to ac differential voltage on tip and ring. This node is a floating input.
6	1	$RING_{IN}$	I	**Power Ring Signal Input.** ac-couple to a sine wave or lower crest factor low-voltage ring signal. The input here is amplified to provide the full-power ring signal at tip and ring. This signal may be applied continuously, even during nonringing states.
7	2	PPM_{IN}	I	**Receive PPM Signal Input.** ac-couple to a 12 kHz or 16 kHz PPM signal. The input here is amplified to provide the differential PPM voltage on tip and ring. This signal may be applied continuously, even during non-PPM modes.
8	5	OVH	I	**Overhead Voltage Program Input.** Connect a voltage source to this point to program the overhead voltage. Voltage source may be external or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the overhead voltage. If a resistor or voltage source is not connected, the overhead voltage will default to a nominal 6.0 V. If the default overhead is desired, connect this pin to ground.
9	6	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current. This is used to set ring trip threshold.
10	7	V_{PROG}	I	**Current-Limit Program Input.** Connect a voltage source to this point to program the dc current limit. Voltage source may be external or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the current limit.
11	9	CF2	—	**Filter Capacitor.** Connect a capacitor from this node to ground.
12	10	CF1	—	**Filter Capacitor.** Connect a capacitor from this node to CF2.
13	12	RTFLT	—	**Ring Trip Filter.** Connect this lead to DCOUT via a resistor and to AGND with a capacitor to filter the ring trip circuit to prevent spurious responses. A single-pole filter is needed.
14	13	V_{REF}	O	**SLIC Internal Reference Voltage.** Output of internal 1.5 V reference voltage.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

32-Pin PLCC	48-Pin MLCC	Symbol	Type	Name/Function
15	15	AGND	GND	**Analog Signal Ground.**
16	16	V_{CC}	PWR	**Analog Power Supply.** User choice of 5 V or 3.3 V nominal power or supply.
17	19	V_{BAT1}	PWR	**Battery Supply 1.** High-voltage battery.
18	20	V_{BAT2}	PWR	**Battery Supply 2.** Lower-voltage battery.
19	22	BGND	GND	**Battery Ground.** Ground return for the battery supplies.
20	23	TRGDET	O	**Tip/Ring Ground Detect.** When high, this open collector output indicates the presence of a ring ground or a tip ground. This supervision output may be used in ground key or common-mode fault detection applications.
21	24	ICM	I	**Common-Mode Current Sense.** To program tip or ring ground sense threshold, connect a resistor to V_{CC} and connect a capacitor to AGND to filter 50/60 Hz. If unused, the pin is connected to ground.
22	25	FB2	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. If ramped battery reversal is not desired, this pin is left open.
23	26	FB1	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. If ramped battery reversal is not desired, this pin is left open.
24	29	PT	I/O	**Protected Tip.** The output drive of the tip amplifier and input to the loop sensing circuit. Connect to loop through overvoltage and overcurrent protection.
25	31	PR	I/O	**Protected Ring.** The output drive of the ring amplifier and input to the loop sensing circuit. Connect to loop through overvoltage and overcurrent protection.
26	33	B2	I^u	**State Control Input.** These pins have an internal 60 kΩ pull-up.
27	34	B1		
28	35	B0		
29	36	BR		
30	38	ITR	I	**Transmit Gain.** Input to AX amplifier. Connect a resistor from this node to VTX to set transmit gain. Gain shaping for termination impedance with a COMBO I codec is also achieved with a network from this node to VTX.
31	40	VTX	O	**ac Output Voltage.** Output of internal AX amplifier. The voltage at this pin is directly proportional to the differential tip/ring current.
32	41	TXI	I	**ac/dc Separation.** Input to internal AAC amplifier. Connect a 0.1 µF capacitor from this pin to VTX.

Operating States

Table 2. Control States

B0	B1	B2	BR	State
1	1	0	1	Forward active
1	1	0	0	Forward active with PPM
1	0	0	1	Reverse active
1	0	0	0	Reverse active with PPM
1	1	1	1	On-hook transmission forward battery (in this state, the device will power up)
1	1	1	0	On-hook transmission with PPM forward battery
1	0	1	1	On-hook transmission reverse battery
1	0	1	0	On-hook transmission with PPM reverse battery
0	1	1	1	Scan
0	0	0	1	Disconnect
0	1	1	0	Ring

Table 3. Supervision Coding

NSTAT	TRGDET
0 = off-hook or ring trip or TSD. 1 = on-hook and no ring trip and no TSD or DISCONNECT state.	0 = no ring or tip ground 1 = ring or tip ground

State Definitions

Forward Active

- Pin PT is positive with respect to PR.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- PPM input is off.
- Overhead is set to nominal 6.0 V for undistorted transmission of 3.14 dBm into 900 Ω and may be increased via OVH.

Reverse Active

- Pin PR is positive with respect to PT.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- PPM input is off.
- Overhead is set to nominal 6.0 V for undistorted transmission of 3.14 dBm into 900 Ω and may be increased via OVH.

Forward Active with PPM

- Pin PT is positive with respect to PR.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- PPM input is on.
- Overhead is set to nominal 6.0 V for undistorted transmission of 3.14 dBm into 900 Ω and may be increased via OVH to accommodate higher-voltage meter pulse signals.

Reverse Active with PPM

- Pin PR is positive with respect to PT.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- PPM input is on.
- Overhead is set to nominal 6.0 V for undistorted transmission of 3.14 dBm into 900 Ω and may be increased via OVH to accommodate higher-voltage meter pulse signals.

Scan

- Except for loop closure, all circuits (including ring trip and common-mode detector) are powered down.
- On-hook transmission is disabled.
- Pin PT is positive with respect to PR and V_{BAT1} is applied to tip/ring.
- The tip-to-ring on-hook differential voltage will be typically between –44 V and –51 V with a –70 V primary battery.

On-Hook Transmission—Forward Battery

- Pin PT is positive with respect to PR.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip-to-ring on-hook differential voltage will be between –41 V and –49 V with a –70 V primary battery.
- PPM is off.

State Definitions (continued)

On-Hook Transmission with PPM—Forward Battery

- Pin PT is positive with respect to PR.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip-to-ring on-hook differential voltage will be between –41 V and –49 V with a –70 V primary battery.
- PPM is on.

On-Hook Transmission—Reverse Battery

- Pin PR is positive with respect to PT.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip-to-ring on-hook differential voltage will be between –41 V and –49 V with a –70 V primary battery.
- PPM is off.

On-Hook Transmission with PPM—Reverse Battery

- Pin PR is positive with respect to PT.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip-to-ring on-hook differential voltage will be between –41 V and –49 V with a –70 V primary battery.
- PPM is on.

Disconnect

- The tip/ring amplifiers and all supervision are turned off.
- The SLIC goes into a high-impedance state.
- NSTAT is forced high (on-hook).

Ring

- Power ring signal is applied to tip and ring.
- Input waveform at $RING_{IN}$ is amplified.
- Ring trip supervision and common-mode current supervision are active; loop closure is inactive.
- Overhead voltage is reduced to typically 4 V, regardless of programming on OVH, and current limit set at V_{PROG} is disabled.
- Current is limited by saturation current of the amplifiers themselves, typically 100 mA at 125 °C.

Thermal Shutdown

- Not controlled via truth table inputs.
- NSTAT is forced low (off-hook) during this state
- This mode is caused by excessive heating of the device, such as may be encountered in an extended power cross situation.

Absolute Maximum Ratings (@ T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
dc Supply (V_{CC})	—	–0.5	—	7.0	V
Battery Supply (V_{BAT1})	—	—	—	–80	V
Battery Supply (V_{BAT2})	—	—	—	V_{BAT1}	V
Logic Input Voltage	—	–0.5	—	V_{CC} + 0.5	V
Logic Output Voltage	—	–0.5	—	V_{CC} + 0.5	V
Operating Temperature Range	—	–40	—	125	°C
Storage Temperature Range	—	–40	—	150	°C
Relative Humidity Range	—	5	—	95	%
Ground Potential Difference (BGND to AGND)	—	—	—	±1	V
PT or PR Fault Voltage (dc)	V_{PT}, V_{PR}	V_{BAT} – 5	—	3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	V_{BAT} – 15	—	15	V

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Table 4. Recommended Operating Characteristics

Parameter	Min	Typ	Max	Unit
5 V dc Supplies (V_{CC})	—	5.0	5.25	V
3 V dc Supplies (V_{CC})	3.13	3.3	—	V
High Office Battery Supply (V_{BAT1})	–60	–70	–75	V
Auxiliary Office Battery Supply (V_{BAT2})	–12	—	V_{BAT1}	V
Operating Temperature Range	–40	25	85	°C

Table 5. Thermal Characteristics

Parameter	Min	Typ	Max	Unit
Thermal Protection Shutdown (Tjc)	150	165	—	°C
32-pin PLCC Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]:				
Natural Convection 2S2P Board	—	35.5	—	°C/W
Natural Convection 2S0P Board	—	50.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S2P Board	—	31.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S0P Board	—	42.5	—	°C/W
48-pin MLCC Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]	—	38	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Airflow, PCB board layers, and other factors can greatly affect this parameter.

Electrical Characteristics

Table 6. Environmental Characteristics

Parameter	Min	Typ	Max	Unit
Temperature Range	–40	—	85	°C
Humidity Range[1]	5	—	95[1]	%RH

1. Not to exceed 26 grams of water per kilogram of dry air.

Table 7. 5 V Supply Currents

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 5 V.

Parameter	Min	Typ	Max	Unit
Supply Currents (scan state; no loop current):				
I_{VCC}	—	4.30	4.80	mA
I_{VBAT1}	—	0.24	0.35	mA
I_{VBAT2}	—	3	6	µA
Supply Currents (forward/reverse active; no loop current, with or without PPM, V_{BAT2} applied):				
I_{VCC}	—	5.95	7.0	mA
I_{VBAT1}	—	25	85	µA
I_{VBAT2}	—	1.2	1.40	mA
Supply Currents (on-hook transmission mode; no loop current, with or without PPM, V_{BAT1} applied):				
I_{VCC}	—	6.0	7.0	mA
I_{VBAT1}	—	1.5	1.9	mA
I_{VBAT2}	—	1.5	6	µA
Supply Currents (disconnect mode):				
I_{VCC}	—	2.7	3.75	mA
I_{VBAT1}	—	15	110	µA
I_{VBAT2}	—	3.5	25	µA
Supply Currents (ring mode; no load):				
I_{VCC}	—	5.9	6.5	mA
I_{VBAT1}	—	1.8	2.2	mA
I_{VBAT2}	—	2	6	µA

Table 8. 5 V Powering

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 5 V.

Parameter	Min	Typ	Max	Unit
Power Dissipation (scan state; no loop current)	—	38	46	mW
Power Dissipation (forward/reverse active; no loop current, with or without PPM)	—	57	64	mW
Power Dissipation (on-hook transmission mode; no loop current, with or without PPM, V_{BAT1} applied)	—	135	165	mW
Power Dissipation (disconnect mode)	—	14	23	mW
Power Dissipation (ring mode; no load)	—	156	184	mW

Electrical Characteristics (continued)

Table 9. 3.3 V Supply Currents

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 3.3 V.

Parameter	Min	Typ	Max	Unit
Supply Currents (scan state; no loop current):				
I_{VCC}	—	3.2	3.6	mA
I_{VBAT1}	—	0.24	0.35	mA
I_{VBAT2}	—	3	6	µA
Supply Currents (forward/reverse active; no loop current, with/without PPM, V_{BAT2} applied):				
I_{VCC}	—	4.8	5.7	mA
I_{VBAT1}	—	25	85	µA
I_{VBAT2}	—	1.2	1.4	mA
Supply Currents (on-hook transmission mode; no loop current, with/without PPM, V_{BAT1} applied):				
I_{VCC}	—	4.9	5.7	mA
I_{VBAT1}	—	1.5	1.9	mA
I_{VBAT2}	—	1.5	6	µA
Supply Currents (disconnect mode):				
I_{VCC}	—	1.8	2.5	mA
I_{VBAT1}	—	8	110	µA
I_{VBAT2}	—	2	25	µA
Supply Currents (ring mode; no loop current):				
I_{VCC}	—	4.70	5.4	mA
I_{VBAT1}	—	1.8	2.2	mA
I_{VBAT2}	—	2	6	µA

Table 10. 3.3 V Powering

V_{BAT1} = –70 V, V_{BAT2} = –21 V, V_{CC} = 3.3 V.

Parameter	Min	Typ	Max	Unit
Power Dissipation (scan state; no loop current)	—	27	36.5	mW
Power Dissipation (forward/reverse active; no loop current, with/without PPM, V_{BAT2} applied)	—	42	53	mW
Power Dissipation (on-hook transmission mode; no loop current, with/without PPM, V_{BAT1} applied)	—	121	151	mW
Power Dissipation (disconnect mode)	—	6.5	15	mW
Power Dissipation (ring mode; no loop current)	—	141	172	mW

Electrical Characteristics (continued)

Table 11. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents + PPM	105	—	—	mAp
Tip or Ring Drive Current = Ringing + Longitudinal	65	—	—	mAp
Signal Current	10	—	—	mArms
Longitudinal Current Capability per Wire (Longitudinal current is independent of dc loop current.)	8.5	15	—	mArms
PPM Signal Current = 1.25 V_{MAX} into 200 Ω ac	6.25	—	—	mArms
Ringing Current (R_{LOAD} = 1386 Ω + 40 µF)	29	—	—	mArms
Ringing Current Limit (R_{LOAD} = 100 Ω)	—	—	50	mAp
dc Loop Current—I_{LIM} (R_{LOOP} = 100 Ω):				
Programming Range (V_{CC} = 5 V)	15	—	70	mA
Programming Range (V_{CC} = 3.3 V)	15	—	45	mA
Voltage at V_{PROG}	0.194	—	1.01	V
dc Current Variation (current limit 22 mA to 28 mA)	—	—	±8	%
dc Current Variation (current limit 70 mA)	—	—	±10	%
dc Feed Resistance (does not include protection resistors)	—	50	—	Ω
Open Loop Voltages:				
Scan Mode:				
$\|V_{BAT1}\|$ > 51 V $\|V_{TIP}\| - \|V_{RING}\|$	44	51	—	V
PR to Battery Ground	—	—	56.5	V
PT to Battery Ground	—	—	56.5	
OHT Mode:				
$\|V_{BAT1}\|$ > 51 V (V_{OH} = 0 V) $\|V_{TIP}\| - \|V_{RING}\|$	41	49	—	V
PR to Battery Ground	—	—	56.5	V
PT to Battery Ground	—	—	56.5	
Active Mode (V_{OH} = 0 V):				
$\|PT - PR\| - \|V_{BAT2}\|$	5.65	6.0	6.5	V
Ring Mode:				
$\|PT - PR\| - \|V_{BAT1}\|$	—	4.0	—	V

Electrical Characteristics (continued)

Table 11. 2-Wire Port (continued)

Parameter	Min	Typ	Max	Unit
Loop Closure Threshold:				
Active/On-hook Transmission Modes	—	10.5	—	mA
Scan Mode	—	11.5	—	mA
Loop Closure Threshold Hysteresis:				
V_{CC} = 5 V	—	2	—	mA
V_{CC} = 3.3 V	—	1	—	mA
Ground Key:				
Differential Detector Threshold	5	8	10	mA
Detection	50	—	—	ms
Longitudinal to Metallic Balance at PT/PR				
Test Method: Q552 (11/96) Section 2.1.2 and *IEEE*® 455:				
300 Hz to 600 Hz	52	—	—	dB
600 Hz to 3.4 kHz	52	—	—	dB
Metallic to Longitudinal (harm) Balance:				
200 Hz to 1000 Hz	40	—	—	dB
100 Hz to 4000 Hz	40	—	—	dB
PSRR 500 Hz—3000 Hz:				
V_{BAT1}, V_{BAT2}	45	—	—	dB
V_{CC} (5 V operation)	35	—	—	dB

Table 12. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
TXI (input impedance)	—	100	—	kΩ
Output Offset (VTX)	—	—	±10	mV
Output Offset (VITR)	—	—	±100	mV
Output Drive Current (VTX)	±300	—	—	µA
Output Drive Current (VITR)	±10	—	—	µA
Output Voltage Swing:				
Maximum (VTX, VITR)	AGND	—	V_{CC}	V
Minimum (VTX)	AGND + 0.25	—	V_{CC} – 0.5	V
Minimum (VITR)	AGND + 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance	10	—	—	kΩ
Output Load Capacitance	—	20	—	pF
RCVN and RCVP:				
Input Voltage Range (V_{CC} = 5 V)	0	—	V_{CC} – 0.5	V
Input Voltage Range (V_{CC} = 3.3 V)	0	—	V_{CC} – 0.3	V
Input Bias Current	—	0.05	—	µA
Differential PT/PR Current Sense (DCOUT):				
Gain (PT/PR to DCOUT)	—	67	—	V/A
Offset Voltage at I_{LOOP} = 0	–20	—	20	mV

Electrical Characteristics (continued)

Table 13. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	600	1400	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain (f = 1004 Hz, 1020 Hz, current limit)[3]:				
PT/PR Current to VITR	300 – 3%	300	300 + 3%	V/A
Receive Gain, f = 1004 Hz, 1020 Hz Open Loop:				
RCVP or RCVN to PT—PR (gain of 8 option, L9215A)	7.76	8	8.24	—
RCVP or RCVN to PT—PR (gain of 2 option, L9215G)	1.94	2	2.06	—
Gain vs. Frequency (transmit and receive)[2] 600 Ω Termination, 1004 Hz, 1020 Hz Reference:				
200 Hz—300 Hz	–0.3	0	0.05	dB
300 Hz—3.4 kHz	–0.05	0	0.05	dB
3.4 kHz—20 kHz	–3.0	0	0.05	dB
20 kHz—266 kHz	—	—	2.0	dB
Gain vs. Level (transmit and receive)[2] 0 dBV Reference:				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (tip/ring) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn
Idle-channel Noise (VTX) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn

1. Set externally either by discrete external components or a third- or fourth-generation codec. Any complex impedance R1 + R2 ‖ C between 150 Ω and 1400 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. VITR transconductance depends on the resistor from ITR to VTX. This gain assumes an ideal 4750 Ω, the recommended value. Positive current is defined as the differential current flowing from PT to PR.

Electrical Characteristics (continued)

Table 14. Logic Inputs and Outputs (V_{CC} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.4	0.7	V
High Level	V_{IH}	2.0	2.4	V_{CC}	V
Input Current:					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	—	—	±50	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	—	—	±50	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 4.75 V, I_{OL} = 200 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Table 15. Logic Inputs and Outputs (V_{CC} = 3.3 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.2	0.5	V
High Level	V_{IH}	2.0	2.5	V_{CC}	V
Input Current:					
Low Level (V_{CC} = 3.46 V, V_I = 0.4 V)	I_{IL}	—	—	±50	µA
High Level (V_{CC} = 3.46 V, V_I = 2.4 V)	I_{IH}	—	—	±50	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 3.13 V, I_{OL} = 200 µA)	V_{OL}	0	0.2	0.5	V
High Level (V_{CC} = 3.13 V, I_{OH} = –5 µA)	V_{OH}	2.2	—	V_{CC}	V

Electrical Characteristics (continued)

Table 16. Ringing Specifications

Parameter	Min	Typ	Max	Unit
$RING_{IN}$ (This input is ac coupled through 0.47 µF.):				
Input Voltage Swing	0	—	V_{CC}	V
Input Impedance	—	100	—	kΩ
Ring Signal Isolation: PT/PR to VITR Ring Mode	—	60	—	dB
Ring Signal Isolation: $RING_{IN}$ to PT/PR Nonring Mode	—	80	—	dB
Ringing Voltage (5 REN 1380 Ω + 40 µF load, 100 Ω loop, 2 x 50 Ω protection resistors, –70 V battery)	40	—	—	Vrms
Ringing Voltage (3 REN 2310 Ω + 24 µF load, 250 Ω loop, 2 x 50 Ω protection resistors, –70 V battery)	40	—	—	Vrms
Ring Signal Distortion:				
5 REN 1380 Ω, 40 µF Load, 100 Ω Loop	—	3	—	%
3 REN 2310 Ω, 24 µF Load, 250 Ω Loop	—	3	—	%
Differential Gain:				
$RING_{IN}$ to PT/PR—No Load	—	55	—	—

Table 17. Ring Trip

Parameter	Min	Typ	Max	Unit
Ring Trip (NSTAT = 0): Loop Resistance (total)	100	—	600	Ω
Ring Trip (NSTAT = 1): Loop Resistance (total)	—	—	10	kΩ
Trip Time (f = 20 Hz)	—	—	100	ms

Ringing will not be tripped by the following loads:

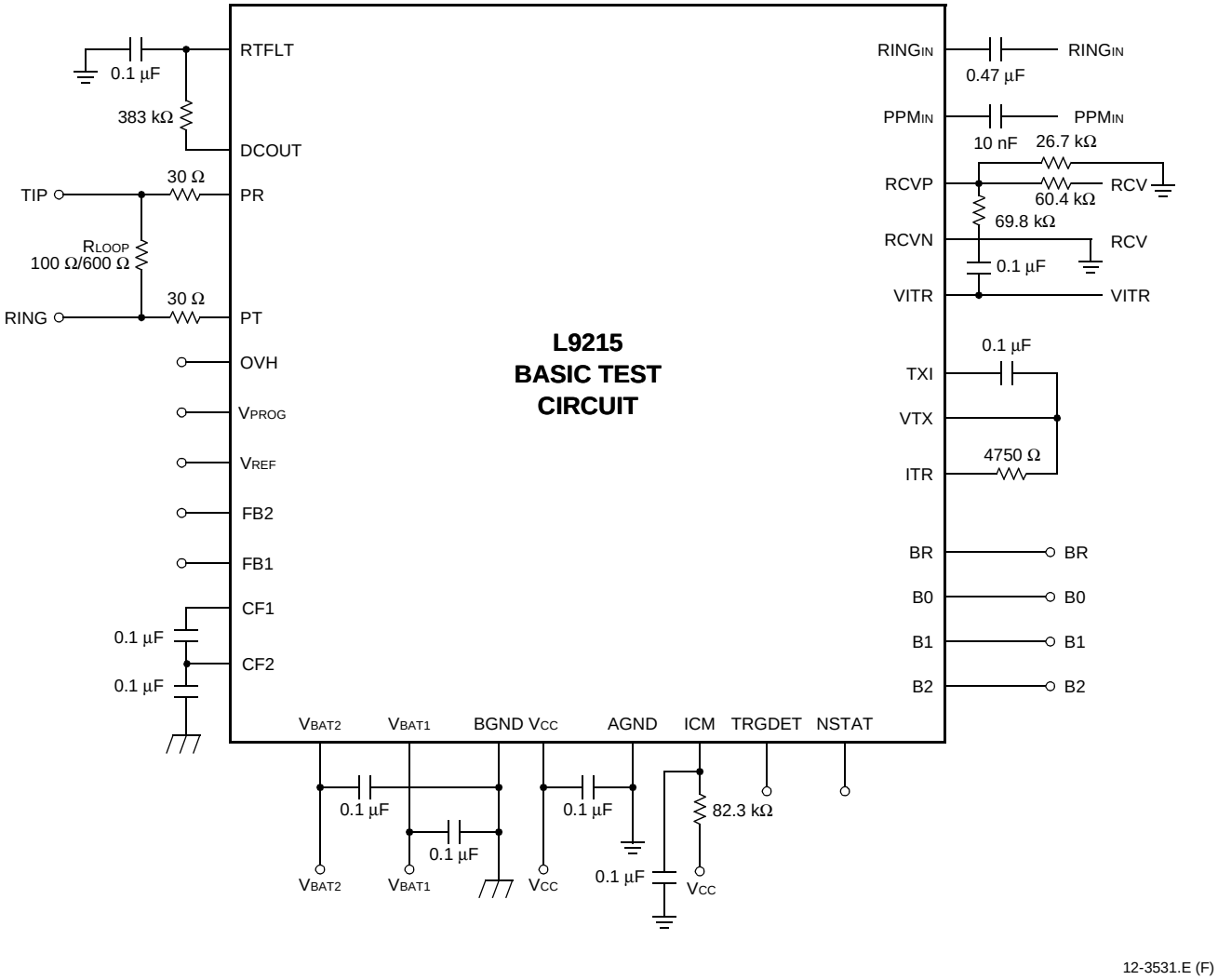
- 10 kΩ resistor in parallel with a 6 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.
- 100 Ω resistor in series with a 2 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.

Table 18. PPM

Parameter	Min	Typ	Max	Unit
PPM Source*:				
Frequency (f1)	11.88	12	12.12	kHz
Frequency (f2)	15.80	16	16.20	kHz
Input Signal	0	1.1	1.25	Vrms
Input Impedance	—	50	—	kΩ
Signal Gain (2.2 Vrms maximum at PT/PR)	5.5	6	6.5	dB
Isolation	—	60	—	dB
Harmonic Distortion	—	—	5	%

* PPM signal should be ac coupled through 10 nF.

Test Configurations



12-3531.E (F)

Figure 4. Basic Test Circuit

Test Configurations (continued)

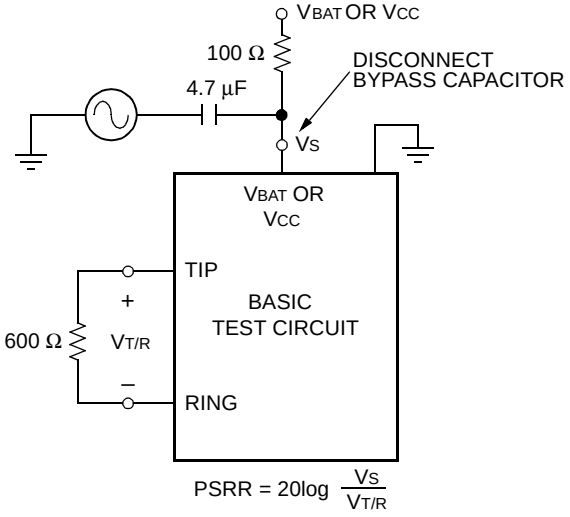


Figure 5. Metallic PSRR

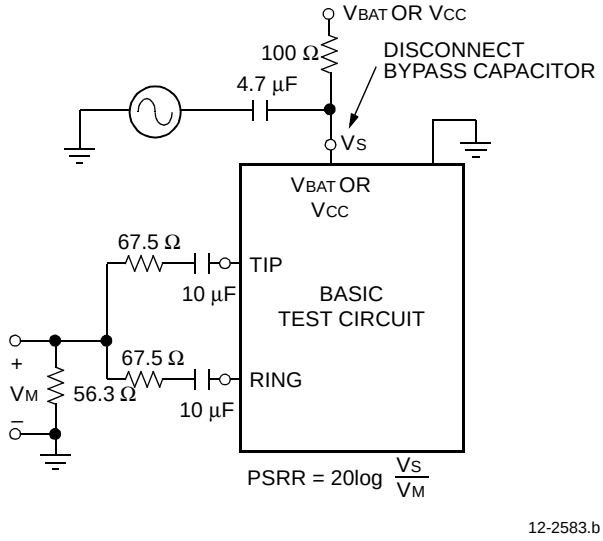


Figure 6. Longitudinal PSRR

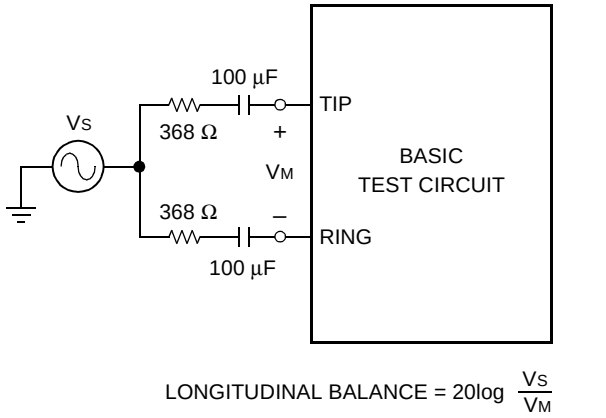


Figure 7. Longitudinal Balance

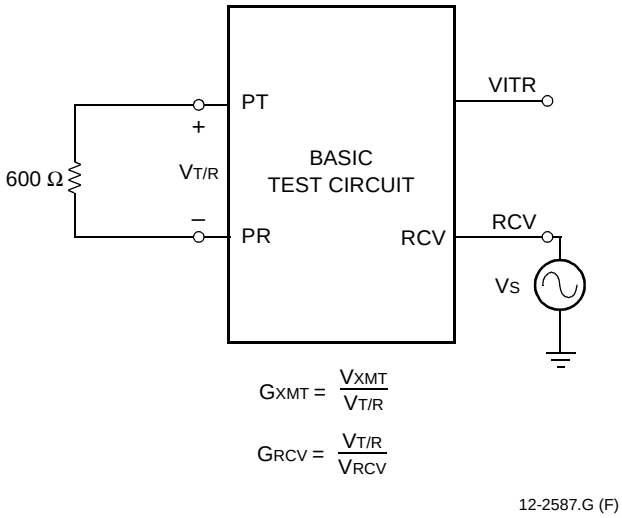


Figure 8. ac Gains

Applications

Power Control

Under normal device operating conditions, power dissipation on the device must be controlled to prevent the device temperature from rising above the thermal shutdown and causing the device to shut down. Power dissipation is highest with higher battery voltages, higher current limit, and under shorter dc loop conditions. Additionally, higher ambient temperature will also reduce thermal margin.

To support required power ringing voltages, this device is meant to operate with a high-voltage primary battery (–65 V to –75 V typically). Thus, power control is normally achieved by use of the battery switch and an auxiliary lower absolute voltage battery. Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop length and protection resistors values, airflow, and number of PC board layers will influence the overall thermal performance. The following example illustrates typical thermal design considerations.

The thermal resistance of the 32-pin PLCC package is typically 50.5 °C/W, which is representative of the natural airflow as seen in a typical switch cabinet with a two-layer board.

The L9215 will enter thermal shutdown at a minimum temperature of 150 °C. The thermal design should ensure that the SLIC does not reach this temperature under normal operating conditions.

For this example, assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 30 mA, a maximum battery of –70 V, and an auxiliary battery of –21 V. Assume a (worst-case) minimum dc loop of 20 Ω of wire resistance, 30 Ω protection resistors, and 200 Ω for the handset. Additionally, include the effects of parameter tolerance.

1. $T_{TSD} – T_{AMBIENT(max)}$ = allowed thermal rise.
   150 °C – 85 °C = 65 °C.
2. Allowed thermal rise = package thermal impedance • SLIC power dissipation.
   65 °C = 50.5 °C/W • SLIC power dissipation
   SLIC power dissipation (P_D) = 1.29 W.

Thus, if the total power dissipated in the SLIC is less than 1.29 W, it will not enter the thermal shutdown state. Total SLIC power is calculated as:

Total P_D = maximum battery • maximum current limit + SLIC quiescent power.

For the L9215, the worst-case SLIC on-hook active power is 76.4 mW. Thus,

Total off-hook power = (I_{LOOP})(current-limit tolerance)*($V_{BATAPPLIED}$) + SLIC on-hook power
Total off-hook power = (0.030 A)(1.08) * (21) + 76.4 mW
Total off-hook power = 756.8 mW

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_D = total power – loop power
Loop off-hook power = $(I_{LOOP} * 1.08)^2$ • ($R_{LOOP(dc)}$ min + $2R_{HANDSET}$)
Loop off-hook power = $(0.030\ A)(1.08)^2$ • (20 Ω + 60 Ω + 200 Ω)
Loop off-hook power = 293.9 mW
SLIC off-hook power = Total off-hook power – loop off-hook power
SLIC off-hook power = 756.8 mW – 293.9 mW
SLIC off-hook power = 462.9 mW < 1.29 W

Thus, under the worst-case normal operating conditions of this example, the thermal design, using the auxiliary, is adequate to ensure the device is not driven into thermal shutdown under worst-case operating conditions.

dc Loop Current Limit

In the active modes, dc current limit is programmable via an applied voltage source at the device's V_{PROG} control input. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output or an external voltage source. A programmable external voltage source may be used to provide software control of the loop current limit. The loop current limit (I_{LIM}) is related to the V_{PROG} voltage at the onset of current limit by:

I_{LIM} (mA) = 67 (mA/V) * V_{PROG} (V)

Note that there is a 12.5 kΩ slope to the I/V characteristic in the current-limit region; thus, once in current limit, the actual loop current will increase slightly, as loop length decreases.

Applications (continued)

dc Loop Current Limit (continued)

Note that the overall current-limit accuracy achieved will not only be affected by the specified accuracy of the internal SLIC current-limit circuit (accuracy associated with the 67 term), but also by the accuracy of the voltage source and the accuracy of any external resistor divider network used and voltage offsets due to the specified input bias current. Tolerance of the current limit is ±8%. If a resistor divider from V_{REF} is used, it is recommended that the sum of the two resistors be greater than 100 kΩ.

The above equations describe the active mode steady-state current-limit response. There will be a transient response of the current-limit circuit upon an on- to off-hook transition. Typical active mode transient current-limit response is given in Table 19.

Table 19. Typical Active Mode On- to Off-Hook Tip/Ring Current-Limit Transient Response

Parameter	Value	Unit
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 5 ms	I_{LIM} + 60	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 50 ms	I_{LIM} + 20	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 300 ms	I_{LIM}	mA

Overhead Voltage

Active Mode

Overhead is programmable in the active mode via an applied voltage source at the device's OVH control input. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output or an external voltage source. A programmable external voltage source may be used to provide software control of the overhead voltage. The overhead voltage (V_{OH}) is related to the OVH voltage by:

V_{OH} = 6.0 V + 5 * V_{OVH} (V)

Overall accuracy is determined by the accuracy of the voltage source and the accuracy of any external resistor divider network used and voltage offsets due to the specified input bias current. If a resistor divider from V_{REF} is used, a lower magnitude resistor will give a more accurate result due to a lower offset associated with the input bias current; however, lower value resistors will also draw more power from V_{REF}.

Note that a default overhead voltage of 6.0 V is achieved by shorting input pin OVH to analog ground.

The default overhead provides sufficient headroom for an on-hook transmission of a 3.14 dBm signal into 900 Ω.

Overhead voltage may need to be increased to accommodate on-hook transmission of higher-voltage signals, such as meter pulse. The following example is meant to illustrate the design procedure that can be followed.

Assume we need on-hook transmission of a 1.0 Vrms meter pulse into 200 Ω. Further, assume 50 Ω protection resistors are used.

V_{OH} = 6.0 V + (1+ [2 * Rp]/200) * Vpeak
V_{OH} = 6.0 + (1+ [2 * 50]/200) * 1 (1.414)
V_{OH} = 8.121 V

Applications (continued)

Overhead Voltage (continued)

Active Mode (continued)

Adding 0.5 V for tolerance, the overhead needs to be increased to (8.121 V + 0.5 V) = 8.621 V to allow for an undistorted on-hook transmission of a 1 Vrms meter pulse into 200 Ω. This is done by applying voltage to pin V_{OH}.

V_{OH} (V) = 6.0 V + 5 * V_{OVH} (V)
8.621 V = 6 V + 5 * V_{OVH}
V_{OVH} = 0.5242 V

Thus, a nominal 0.5242 V is applied to pin V_{OVH} to increase the overhead.

Scan Mode

If the magnitude of the primary battery is greater than 51 V, the magnitude of the open loop tip-to-ring open loop voltage is clamped typically between 44 V and 51 V. If the magnitude of the primary battery is less than a nominal 51 V, the overhead voltage will track the magnitude of the battery voltage, i.e., the magnitude of the open circuit tip-to-ring voltage will be 4 V to 6 V less than battery. In the scan mode, overhead is unaffected by V_{OVH}.

On-Hook Transmission Mode

If the magnitude of the primary battery is greater than 51 V, the magnitude of the open loop tip-to-ring open loop voltage is clamped typically between 41 V and 49 V. If the magnitude of the primary battery is less than a nominal 51 V, the overhead voltage will track the magnitude of the battery voltage, i.e., the magnitude of the open circuit tip-to-ring voltage will be 6 V to 8 V less than battery. In the scan mode, overhead is unaffected by V_{OVH}.

Ring Mode

In the ring mode, to maximize ringing loop length, the overhead is decreased to the saturation of the tip ring drive amplifiers, a nominal 4 V. The tip-to-ground voltage is 1 V, and the ring to V_{BAT1} voltage is 3 V. In the ring mode, overhead is unaffected by V_{OVH}.

During the ring mode, to conserve power the receive input at RCVN/RCVP is deactivated. During the ring mode, to conserve power, the ACC amplifier in the transmit direction at VITR is deactivated. However, if the AX amplifier at VTX is active during the ring mode, differential ring current may be sensed at VTX during the ring mode.

Loop Range

The dc loop range is calculated using:

$$R_L = \frac{|V_{BAT2}| - V_{OH}}{I_{LIMIT}} - 2R_P - R_{DC}$$

V_{BAT2} is typically applied under off-hook conditions for power conservation and SLIC thermal considerations. The L9215 is intended for short-loop applications and, therefore, will always be in current limit during off-hook conditions. However, note that the ringing loop length rather than the dc loop length, will be the factor to determine operating loop length.

Battery Reversal Rate

The rate of battery reverse is controlled or ramped by capacitors FB1 and FB2. A chart showing FB1 and FB2 values versus typical ramp time is given below. Leave FB1 and FB2 open if it is not desired to ramp the rate of battery reversal.

Table 20. FB1 and FB2 Values vs. Typical Ramp Time

C_{FB1} and C_{FB2}	Transition Time
0.01 µF	20 ms
0.1 µF	220 ms
0.22 µF	440 ms
0.47 µF	900 ms
1.0 µF	1.8 s
1.22 µF	2.25 s
1.3 µF	2.5 s
1.4 µF	2.7 s
1.6 µF	3.2 s

Supervision

The L9215 offers the loop closure and ring trip supervision functions. Internal to the device, the outputs of these detectors are multiplexed into a single package output, NSTAT. Additionally, a common-mode current detector for tip or ring ground detection is included for ground key applications.

Loop Closure

The loop closure has a fixed typical 10.5 mA on- to off-hook threshold in the active mode and a fixed 11.5 mA on- to off-hook threshold from the scan mode. In either case, there is a 2 mA hysteresis with V_{CC} = 5 V and a 1 mA hysteresis with V_{CC} = 3.3 V.

Ring Trip

The ring trip detector requires only a single-pole filter at the input, minimizing external components. An R/C combination of 383 kΩ and 0.1 µF, for a filter pole at 5.15 Hz, is recommended.

The ring trip threshold is internally fixed as a function of battery voltage and is given by:

$RT\ (mA) = 67 * \{(0.0045 * V_{BAT1}) + 0.317\}$

where:

RT is ring trip current in mA.
V_{BAT1} is the magnitude of the ring battery in V.
There is a 6 mA to 8 mA hysteresis.

Tip or Ring Ground Detector

In the ground key or ground start applications, a common-mode current detector is used to indicate either a tip- or ring-ground has occurred (ground key) or an off-hook has occurred (ground start). The detection threshold is set by connecting a resistor from ICM to V_{CC}.

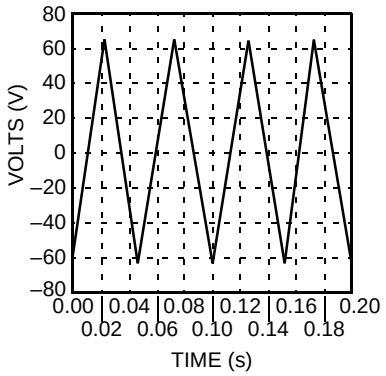
$170 \times V_{CC}/R_{ICM}\ (k\Omega) = I_{TH}\ (mA)$

Additionally, a filter capacitor across R_{ICM} will set the time constant of the detector. No hysteresis is associated with this detector.

Power Ring

The device offers a ring mode, in which a balanced power ring signal is provided to the tip/ring pair. During the ring mode, a user-supplied low-voltage ring signal is input to the device's $RING_{IN}$ input. This signal is amplified to produce the balanced power ring signal. The user may supply a sine wave input, PWM input, or a square wave to produce sinusoidal or trapezoidal ringing at tip and ring.

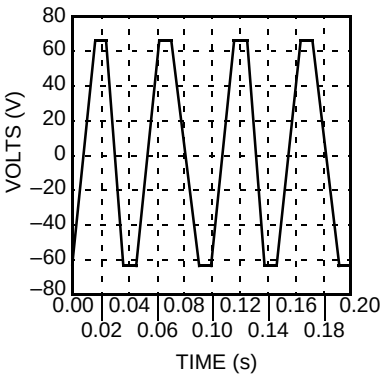
Various crest factors are shown below for illustrative purposes.



12-3346a (F)

Note: Slew rate = 5.65 V/ms; trise = tfall = 23 ms; pwidth = 2 ms; period = 50 ms.

Figure 9. Ringing Waveform Crest Factor = 1.6



12-3347a (F)

Note: Slew rate = 10.83 V/ms; trise = tfall = 12 ms; pwidth = 13 ms; period = 50 ms.

Figure 10. Ringing Waveform Crest Factor = 1.2

Voltage applied to the load may be increased by using a filtered square wave input to produce a lower crest factor trapezoidal power ring signal at tip and ring.

Supervision (continued)

Power Ring (continued)

Sine Wave Input Signal and Sine Wave Power Ring Signal Output

The low-voltage sine wave input is applied to the L9215 at pin RINGIN. This signal should be ac-coupled through 0.47 µF. During the ring mode, the signal at RINGIN is amplified and presented to the subscriber loop. The differential gain from RINGIN to tip and ring is a nominal 55.

When the device enters the ring mode, the tip/ring overhead set at OVH and the scan clamp circuit is disabled, allowing the voltage magnitude of the power ring signal to be maximized. Additionally, in the ring mode, the loop current limit is increased 2.5X the value set by the VPROG voltage.

The magnitude of the power ring voltage will be a function of the gain of the ring amplifier, the high-voltage battery, and the input signal at RINGIN. The input range of the signal at RINGIN is 0 V to Vcc. As the input voltage at RINGIN is increased, the magnitude of the power ring voltage at tip and ring will increase linearly, per the differential gain of 55, until the tip and ring drive amplifiers begin to saturate. Once the tip and ring amplifiers reach saturation, further increases of the input signal will cause clipping distortion of the power ring signal at tip and ring. The ring signal will appear balanced on tip and ring. That is, the power ring signal is applied to both tip and ring, with the signal on tip 180° out of phase from the signal on ring.

Figure 11 shows typical operation of the ring mode, prior to saturation of the tip and ring drive amplifiers. A –70 V battery is used with a 100 Ω loop and a 1 REN load. The input signal is 1 V through a 0.47 µF capacitor at RINGIN, (the input circuit is shown in Figure 12). This produces a voltage swing from –34 V to –60 V on ring and from –8 V to –34 V on tip, as shown in Figure 11. Thus, the total voltage swing is 52 V (60 V to 8 V) for a 1 V input, which is approximately the differential gain of the device. Note that the tip and ring power ring signals will swing around VBATTERY divided by two. In this case, there is a –70 V battery so tip and ring swing around –34 V.

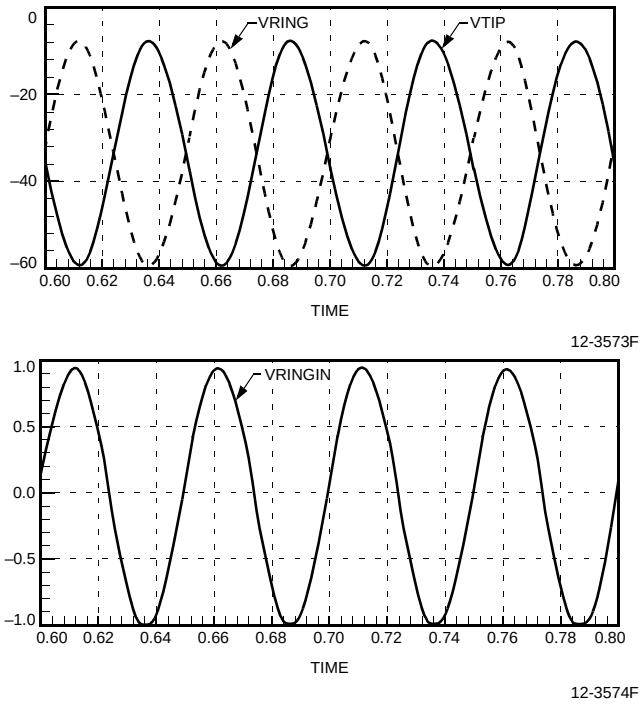


Figure 11. Ring Mode Typical Operation

Supervision (continued)

Power Ring (continued)

Sine Wave Input Signal and Sine Wave Power Ring Signal Output (continued)

It is recommended that the input level at RINGIN be adjusted so that the power ring signal at tip and ring is just at the edge or slightly clipping. This gives maximum power transfer with minimal distortion of the sine wave. The tip side will saturate at a nominal 1 V above ground. The ring side will saturate at a nominal 3 V above battery. The input circuit for a sine wave along with waveforms to illustrate the tip and ring saturation is shown in Figure 12.

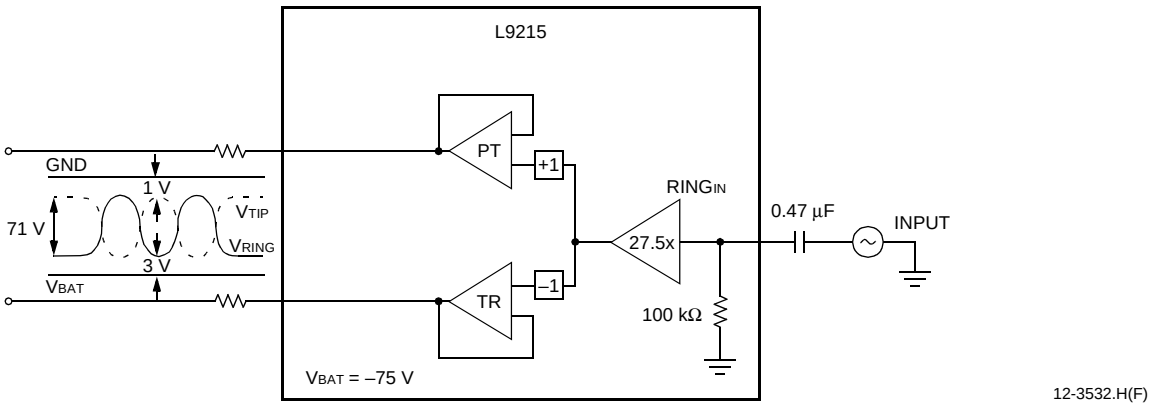


Figure 12. RINGIN Operation

The point at which clipping of the power ring signal begins at tip and ring is a function of the battery voltage, the input capacitor at RINGIN, and the input signal at RINGIN and Vcc. Typical characteristic conditions showing the onset of clipping are given below.

Table 21. Onset of Power Ringing Clipping Vcc = 5 V, Cinput = 0.47 µF

Input		T/R	
VBAT1 (V)	Vrms (mV)	Vrms (V)	Gain
–70.15	891	46.88	52.62
–68.06	858	45.11	52.58
–66.00	833	43.69	52.45
–64.08	814	42.57	52.30
–62.04	789	41.21	52.23
–60.05	747	39.11	52.36

Table 22. Onset of Power Ringing Clipping Vcc = 3.1 V, Cinput = 0.47 µF

Input		T/R	
VBAT1 (V)	Vrms (mV)	Vrms (V)	Gain
–70.12	894	47.15	52.74
–68.07	855	45.11	52.76
–66.06	824	43.38	52.65
–64.01	799	41.95	52.5
–62.00	780	40.79	52.29
–60.00	749	39.09	52.19

Supervision (continued)

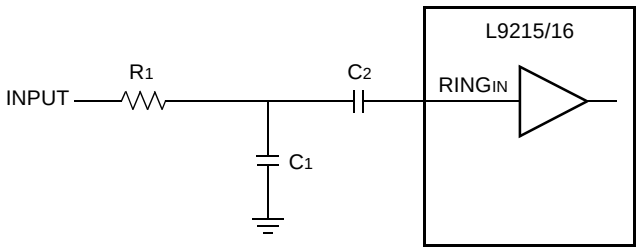
Power Ring (continued)

Sine Wave Input Signal and Sine Wave Power Ring Signal Output (continued)

During nonring modes, the sinusoidal ringing waveform may be left on at RINGIN. Via the state table, the ring signal will be removed from tip and ring even if the low-voltage input is still present at RINGIN. There are certain timing considerations that should be made with respect to state changes which are detailed in the *Switching Behavior of L9215 Ringing SLIC* Application Note.

PWM Input Signal and Sine Wave Power Ring Signal Output

A pulse-width modulated (PWM) signal may be used to provide the ringing input to RINGIN. The signal is applied through a low-pass filter and ac-coupled into RINGIN as shown below. This approach gives a sine wave output at tip and ring.



12-3578bF

Figure 13. L9215/16 Ringing Input Circuit Selection Table for Square Wave and PWM Inputs

Table 23. Signal and Component Selection Chart

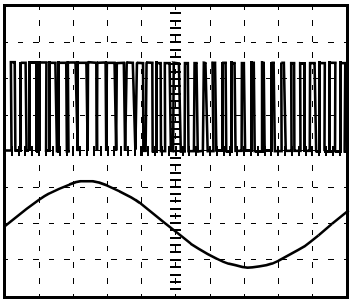
VBAT	VCC	Input	R1	C1	C2	CF	Typical 5 REN Ringing Voltage RMS
70 V	5 V	5 V Square	12 kΩ	1 µF	0.47 µF	1.3	48 V
70 V	3 V	3 V Square	7 kΩ	1 µF	0.47 µF	1.3	49 V
70 V	5 V	10 kHz PWM 5 V	10 kΩ	0.22 µF	0.47 µF	sine	42 V
70 V	3 V	10 kHz PWM 3 V	10 kΩ	0.22 µF	0.47 µF	sine	42 V
70 V	5 V	90 kHz PWM 5 V	7 kΩ	0.1 µF	0.47 µF	sine	42 V
70 V	3 V	90 kHz PWM 3 V	7 kΩ	0.1 µF	0.47 µF	sine	42 V
85 V	5 V	5 V Square	10 kΩ	1 µF	0.47 µF	1.3	59 V
85 V	3 V	3 V Square	7 kΩ	1 µF	0.47 µF	1.3	51 V
85 V	5 V	10 kHz PWM 5 V	10 kΩ	0.22 µF	0.47 µF	sine	51 V
85 V	3 V	10 kHz PWM 3 V	4 kΩ	0.22 µF	0.47 µF	sine	47 V
85 V	5 V	90 kHz PWM 5 V	4 kΩ	0.1 µF	0.47 µF	sine	51 V
85 V	3 V	90 kHz PWM 3 V	4 kΩ	0.1 µF	0.47 µF	sine	49 V

Supervision (continued)

Power Ring (continued)

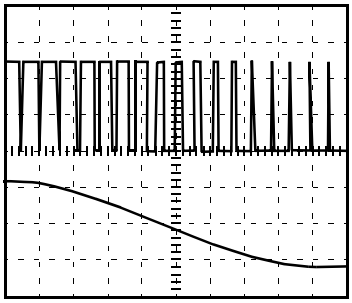
PWM Input Signal and Sine Wave Power Ring Signal Output (continued)

Modulation waveforms showing PWM are in Figure 14 below.



12-3381(F)

**A. Upper = Pwm Signal Centered at 10 kHz
Lower = Modulation Signal**



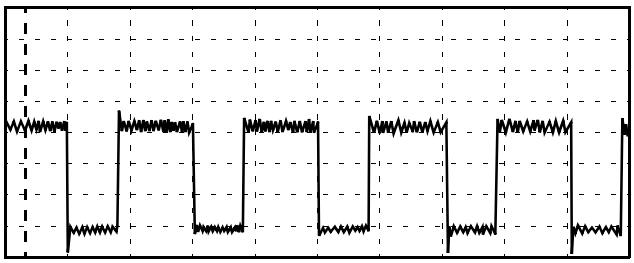
12-3380(F)

B. Same as A but Expanded

Figure 14. Modulation Waveforms

5 V V_{CC} Operation

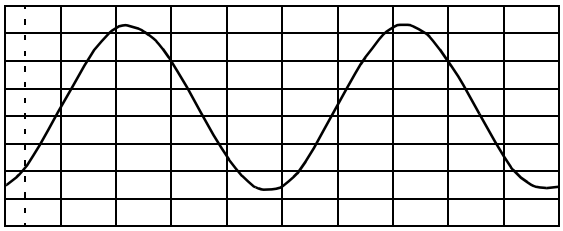
A PWM signal was generated with an *HP*™ 8116 Function Generator modulated with a 20 Hz signal. The optimal frequency used was 10 kHz. THE PWM signal amplitude was 5.0 V (0 V to 5 V). This signal is shown in Figure 15.



12-3575F

Figure 15. 5 V PWM Signal Amplitude

This input produced 44.96 Vrms ringing signal on tip/ring under open loop conditions and 42.0 Vrms was delivered to 5 REN load. The ringing output on ring, with V_{CC} = 5 V, is shown in Figure 16.



1660

Notes:
The modulating 20 Hz signal THD was measured at 1.3 %.

The tip/ring 20 Hz signal THD was measured at 1 %.

V_{BAT1} = –70.6 V, V_{BAT2} = –26.5 V, V_{CC} = 5.019 V.

PWM input 10 kHz, 5.0 Vp-p.

R_1 = 10 kΩ, C_1 = 0.22 µF, C_2 = 0.47 µF.

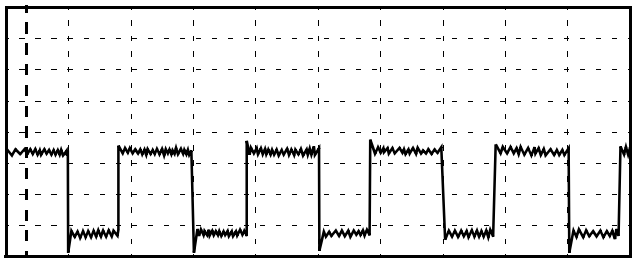
Figure 16. Ringing Output on RING, with V_{CC} = 5 V

Supervision (continued)

Power Ring (continued)

3.3 V V_{CC} Operation

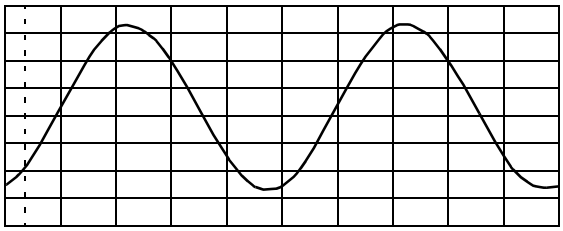
A PWM signal was generated with an *HP* 8116 Function Generator modulated with a 20 Hz signal. The optimal frequency used was 10 kHz. The PWM signal amplitude was 3.10 V (0 V to 3.10 V). This input signal is shown in Figure 17.



12-3571F

Figure 17. 3.3 V PWM Signal Amplitude

This produced 44.96 Vrms ringing signal on tip/ring under open-loop conditions and 42.0 Vrms was delivered to 5 REN load. The ringing output on ring, with V_{CC} = 3.1 V is shown in Figure 18.



1660

Notes:
The modulating 20 Hz signal THD was measured at 1.3 %.

The tip/ring 20 Hz signal THD was measured at 1 %.

V_{BAT1} = –70.6 V, V_{BAT2} = –26.5 V, V_{CC} = 3.10 V.

PWM input 10 kHz, 3.1 Vp-p.

R_1 = 10 kΩ, C_1 = 0.22 µF, C_2 = 0.47 µF.

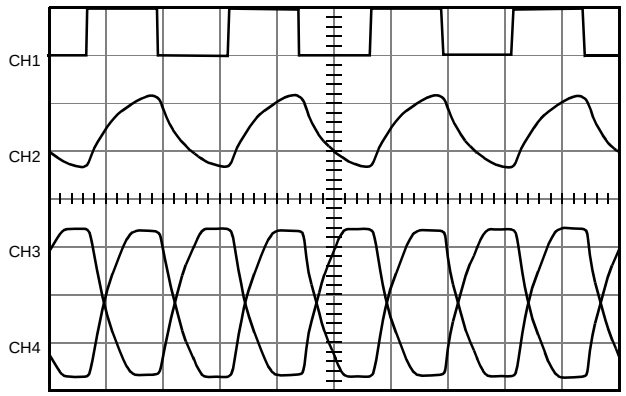
Figure 18. Ringing Output on RING, with V_{CC} = 3.1 V

During nonring modes, the PWM waveform may be left on at $RING_{IN}$. Via the state table, the ring signal will be removed from tip and ring even if the low-voltage input is still present at $RING_{IN}$. There are certain timing consideration that should be made with respect to state changes which are detailed in the *Switching Behavior of L9215 Ringing SLIC* Application Note.

Square Wave Input Signal and Trapezoidal Power Ring Signal Output

A low-voltage square wave signal may be used to provide the ringing input to $RING_{IN}$. The signal is applied through a low-pass filter and ac-coupled into $RING_{IN}$ as shown in Figure 13 and Table 23. This approach gives a trapezoidal wave output at tip and ring.

Using this approach, a trapezoidal waveform can be achieved at tip and ring. This has the advantage of increasing the power transfer to the load for a given battery voltage, thus increasing the effective ringing loop length as compared to a sine wave. The actual crest factor achieved is a function of the magnitude of the battery, the magnitude of the input voltage, frequency, and R_1.



12-3572F

Notes:
CH1 = CMOS Input (5 V) at $RING_{IN}$.

CH2 = Filtered input at $RING_{IN}$.

CH3 = Tip.

CH4 = Ring.

R_1 = 14 kΩ, C_1 = 1.0 µF, C_2 = 0.47 µF.

V_{BAT1} = –70 V, Vrms = 51 V, V_{p-p} = 67 V, frequency = 20 Hz, crest factor = 1.3.

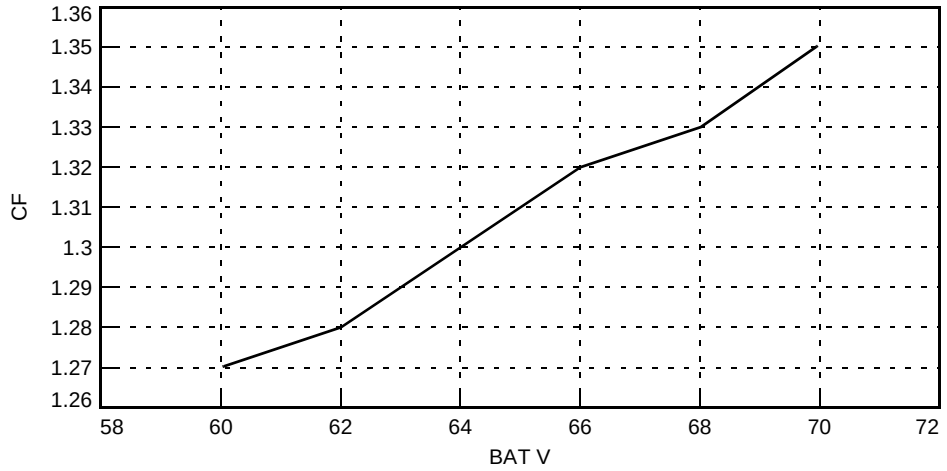
Figure 19. Square Wave Input Signal and Trapezoidal Power Ring Signal Output

Supervision (continued)

Power Ring (continued)

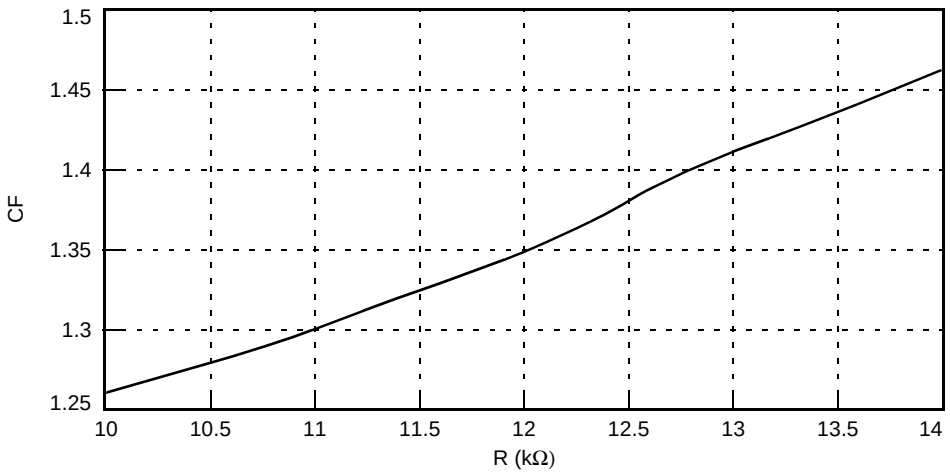
Square Wave Input Signal and Trapezoidal Power Ring Signal Output (continued)

The following charts are meant to give some guidance to the relationship between crest factor, battery voltage, and R_1 value.



12-3576F

Figure 20. Crest Factor vs. Battery Voltage



12-3577F

Figure 21. Crest Factor vs. R (kΩ)

During nonring modes, the square wave input may be left on or removed from RINGIN. Via the state table, the ring signal will be removed from tip and ring even if the low-voltage input is still present at RINGIN. However, removing the waveform has certain advantages in terms of the timing of state. These advantages are detailed in the *Switching Behavior of L9215 Ringing SLIC* Application Note.

Periodic Pulse Metering (PPM)

Periodic pulse metering (PPM), also referred to as teletax (TTX), is input to the PPMIN input of the L9215. Upon application of appropriate logic control, this signal is presented to the tip/ring subscriber loop. The state of the L9215 should be changed while applying PPM signals during the quiet interval of the PPM cadence. The L9215 assumes that a shaped PPM signal is applied to the PPMIN input.

PPM input signals may be a maximum 1.25 V at PPMIN. The gain from PPMIN to tip/ring is 6 dB. Thus, for 1.0 Vrms at tip and ring, apply a 0.50 Vrms signal at PPMIN. The PPM signal should be ac coupled to PPMIN through a 10 nF capacitor.

When applied to tip and ring, the PPM signal will also be returned through the SLIC and will appear at the SLIC VITR output. The concern is that this high-voltage signal can overload an internal SLIC amplifier or the codec input and cause distortion of the (desired) ac signal. Because the L9215 is intended for short dc loops, the assumption is that low meter pulse signals are sufficient. The maximum allowed PPM current at the 200 Ω ac meter pulse load to avoid saturation of the device's internal AAC amplifier is 3 mArms. This signal level is sufficient to provide a minimum 200 mVrms to the 200 Ω PPM load under maximum specified dc loop conditions. Above 3 mArms PPM current, external meter pulse rejection may be required. If on-hook transmission of PPM is required, sufficient overhead to accommodate on-hook transmission must be programmed by the user at the OVH input.

ac Applications

ac Parameters

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Transmit and receive gains may be specified in terms of an actual gain, or in terms of a transmission level point (TLP), that is the actual ac transmission level in dBm. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

Codec Types

At this point in the design, the codec needs to be selected. The interface network between the SLIC and codec can then be designed. Below is a brief codec feature summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, 5 V only or ±5 V operation, and μ-law/A-law selectability. These are available in single and quad designs. This type of codec requires continuous time analog filtering via external resistor/capacitor networks to set the ac design parameters. An example of this type of codec is the Agere T7504 quad 5 V only codec.

This type of codec tends to be the most economical in terms of piece part price, but tends to require more external components than a third-generation codec. Further ac parameters are fixed by the external R/C network so software control of ac parameters is difficult.

Third-Generation Codecs

This class of devices includes all ac parameters set digitally under microprocessor control. Depending on the device, it may or may not have data control latches. Additional functionality sometimes offered includes tone plant generation and reception, PPM generation, test algorithms, and echo cancellation. Again, this type of codec may be 3.3 V, 5 V only, or ±5 V operation, single quad or 16 channel, and μ-law/A-law or 16-bit linear coding selectable. Examples of this type of codec are the Agere T8535/6 (5 V only, quad, standard features), T8537/8 (3.3 V only, quad, standard features), T8533/4 (5 V only, quad with echo cancellation), and the T8531/32 (5 V only 16 channel).

ac Interface Network

The ac interface network between the L9215 and the codec will vary depending on the codec selected. With a first-generation codec, the interface between the L9215 and codec actually sets the ac parameters. With a third-generation codec, all ac parameters are set digitally, internal to the codec; thus, the interface between

ac Applications (continued)

ac Interface Network (continued)

the L9215 and this type of codec is designed to avoid overload at the codec input in the transmit direction and to optimize signal to noise ratio (S/N) in the receive direction.

Because the design requirements are very different with a first- or third-generation codec, the L9215 is offered with two different receive gains. Each receive gain was chosen to optimize, in terms of external components required, the ac interface between the L9215 and codec.

With a first-generation codec, the termination impedance is set by providing gain shaping through a feedback network from the SLIC VITR output to the SLIC RCVN/RCVP inputs. The L9215 provides a transconductance from T/R to VITR in the transmit direction and a single-ended to differential gain from either RCVN or RCVP to T/R in the receive direction. Assuming a short from VITR to RCVN or RCVP, the maximum impedance that is seen looking into the SLIC is the product of the SLIC transconductance times the SLIC receive gain, plus the protection resistors. The various specified termination impedance can range over the voiceband as low as 300 Ω up to over 1000 Ω. Thus, if the SLIC gains are too low, it will be impossible to synthesize the higher termination impedances. Further, the termination that is achieved will be far less than what is calculated by assuming a short for SLIC output to SLIC input. In the receive direction, in order to control echo, the gain is typically a loss, which requires a loss network at the SLIC RCVN/RCVP inputs, which will reduce the amount of gain that is available for termination impedance. For this reason, a high-gain SLIC is required with a first-generation codec.

With a third-generation codec, the line card designer has different concerns. To design the ac interface, the designer must first decide upon all termination impedance, hybrid balances, and transmission-level point (TLP) requirements that the line card must meet. In the transmit direction, the only concern is that the SLIC does not provide a signal that is too hot and overloads the codec input. Thus, for the highest TLP that is being designed to, given the SLIC gain, the designer, as a function of voiceband frequency, must ensure the codec is not overloaded. With a given TLP and a given SLIC gain, if the signal will cause a codec overload, the designer must insert some sort of loss, typically a resistor divider, between the SLIC output and codec input.

Note also that some third-generation codecs require the designer to provide an inherent resistive termination via external networks. The codec will then provide gain shaping, as a function of frequency, to meet the return loss requirements. This feedback will increase the signal at the codec input and increase the likelihood that a resistor divider is needed in the transmit direction. Further stability issues may add external components or excessive ground plane requirements to the design.

In the receive direction, the issue is to optimize the S/N. Again, the designer must consider all the considered TLPs. The idea is, for all desired TLPs, to run the codec at or as close as possible to its maximum output signal, to optimize the S/N. Remember, noise floor is constant, so the hotter the signal from the codec, the better the S/N. The problem is if the codec is feeding a high-gain SLIC, either an external resistor divider is needed to knock the gain down to meet the TLP requirements, or the codec is not operated near maximum signal levels, thus compromising the S/N.

Thus, it appears that the solution is to have a SLIC with a low gain, especially in the receive direction. This will allow the codec to operate near its maximum output signal (to optimize S/N), without an external resistor divider (to minimize cost).

To meet the unique requirements of both type of codecs, the L9215 offers two receive gain choices. These receive gains are mask-programmable at the factory and are offered as two different code variations. For interface with a first-generation codec, the L9215 is offered with a receive gain of 8. For interface with a third-generation codec, the L9215 is offered with a receive gain of 2. In either case, the transconductance in the transmit direction or the transmit gain is 300 Ω.

This selection of receive gain gives the designer the flexibility to maximize performance and minimize external components, regardless of the type of codec chosen.

Design Examples

First-Generation Codec ac Interface Network—Resistive Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T7504 first-generation codec for a resistive termination impedance. For this example, the ac interface was designed for a 600 Ω resistive termination and hybrid balance with transmit gain and receive gain set to 0 dBm. For illustration purposes, no PPM injection was assumed in this example. This implies use of the default overhead voltage and no components for meter pulse rejection.

ac Applications (continued)

Design Examples (continued)

First-Generation Codec ac Interface Network—Resistive Termination (continued)

This is a lower feature application example and uses single battery operation, fixed overhead, current limit, and loop closure threshold.

Resistor R_{GN} is optional. It compensates for any mismatch of input bias voltage at the RCVN/RCVP inputs. If it is not used, there may be a slight offset at tip and ring due to mismatch of input bias voltage at the RCVN/RCVP inputs. It is very common to simply tie RCVN directly to ground in this particular mode of operation. If used, to calculate RGN, the impedance from RCVN to ac ground should equal the impedance from RCVP to ac ground.

Example 1, Real Termination

The following design equations refer to the circuit in Figure 22. Use these to synthesize real termination impedance.

Termination Impedance:

$$z_T = \frac{V_{T/R}}{-I_{T/R}}$$

$$z_T = 50\ \Omega + 2R_P + \frac{2400}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{T/R}}{V_{FR}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{Z_T}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{-R_X}{R_{T2}} \times \frac{300}{Z_{T/R}}$$

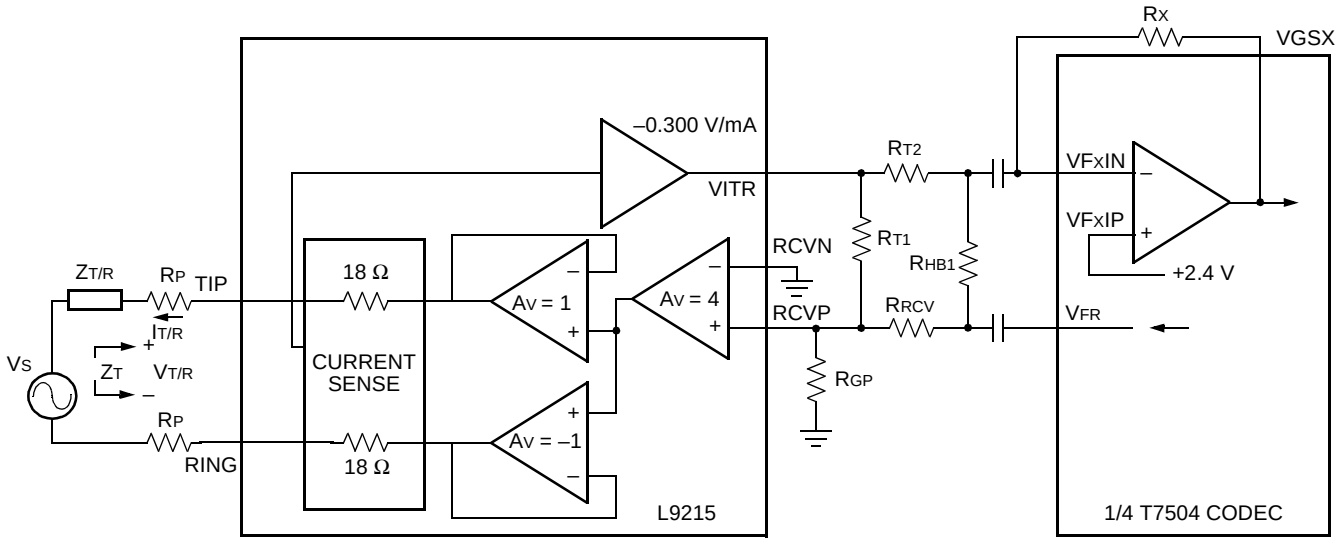
Hybrid Balance:

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB}} - g_{tx} \times g_{rcv}\right)$$

$$h_{bal} = 20\log\left(\frac{V_{GSX}}{V_{FR}}\right)$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The expression for ZHB becomes the following:

$$R_{HB}(k\Omega) = \frac{R_X}{g_{tx} \times g_{rcv}}$$



12-2554.V (F)

Figure 22. ac Equivalent Circuit

ac Applications (continued)

Design Examples (continued)

Example 1, Real Termination (continued)

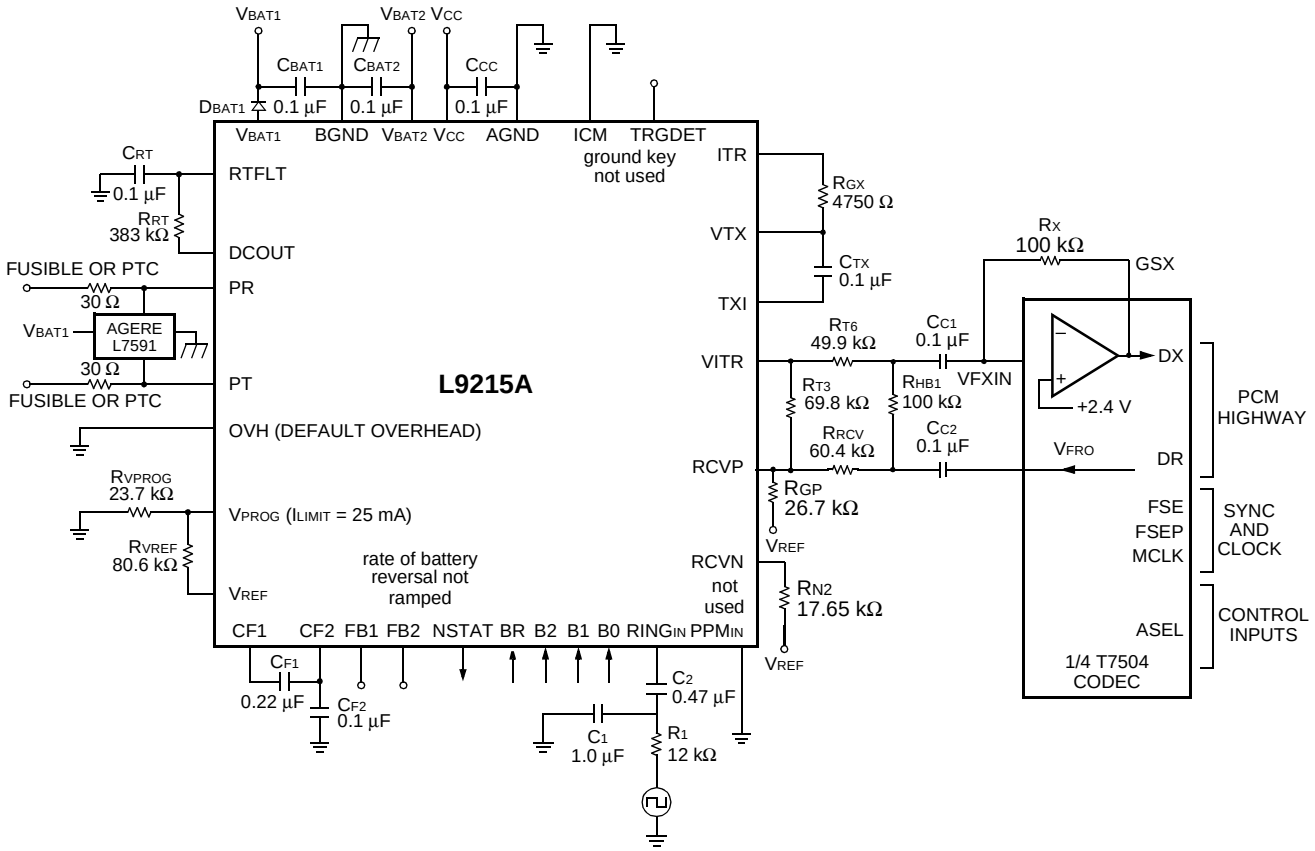


Figure 23. Agere T7504 First-Generation Codec Resistive Termination; Nonmeter Pulse Application

ac Applications (continued)

Design Examples (continued)

Example 1, Real Termination (continued)

Table 24. Parts List L9215; Agere T7504 First-Generation Codec Resistive Termination; Nonmeter Pulse Application

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PT}	30 Ω	1%	Fusible or PTC	Protection resistor.
R_{PR}	30 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Agere L7591	—	—	Secondary protection.
Power Supply				
C_{BAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.1 µF	20%	10 V	V_{CC} filter capacitor.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
dc Profile				
R_{VPROG}	23.7 kΩ	1%	1/16 W	With R_{VREF} fixes dc current limit.
R_{VREF}	80.6 kΩ	1%	1/16 W	With R_{VPROG} fixes dc current limit.
Ring/Ring Trip				
C_1	1.0 µF	20%	10 V	Ring filter for square wave.
C_2	0.47 µF	20%	10 V	ac-couple input ring signal.
R_1	12 kΩ	1%	1/16 W	Ring filter for square wave.
C_{RT}	0.1 µF	20%	10 V	Ring trip filter capacitor.
R_{RT}	383 kΩ	1%	1/16 W	Ring trip filter resistor.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
C_{TX}	0.1 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.
C_{C2}	0.1 µF	20%	10 V	dc blocking capacitor.
R_{T3}	69.8 kΩ	1%	1/16 W	With R_{GP} and R_{RCV}, sets termination impedance and receive gain.
R_{T6}	49.9 kΩ	1%	1/16 W	With R_X, sets transmit gain.
R_X	100 kΩ	1%	1/16 W	With R_{T6}, sets transmit gain.
R_{HB1}	100 kΩ	1%	1/16 W	With R_X, sets hybrid balance.
R_{RCV}	60.4 kΩ	1%	1/16 W	With R_{GP} and R_{T3}, sets termination impedance and receive gain.
R_{GP}	26.7 kΩ	1%	1/16 W	With R_{RCV} and R_{T3}, sets termination impedance and receive gain.
R_{GN} Optional	17.6 kΩ	1%	1/16 W	Optional. Compensates for input offset at RCVN/RCVP.

Notes:
Termination impedance = 600 Ω.
Hybrid balance = 600 Ω.
T x = 0 dBm Rx = 0 dBm.

ac Applications (continued)

Design Examples (continued)

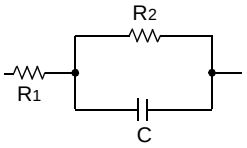
First-Generation Codec ac Interface Network—Complex Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T7504 first-generation codec for the German complex termination impedance. For this example, the ac interface was designed for a 220 Ω + (820 Ω || 115 nF) complex termination and hybrid balance with transmit gain and receive gain set to 0 dBm. For illustration purposes, 1 Vrms PPM injection was assumed in this example. This implies the overhead voltage is increased to 7.24 V and no meter pulse rejection is required. Also, this example illustrates the device using fixed overhead and current limit.

Complex Termination Impedance Design Example

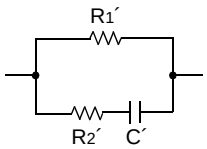
The gain shaping necessary for a complex termination impedance may be done by shaping across the AX amplifier at nodes ITR and VTX.

Complex termination is specified in the form:



5-6396(F)

To work with this application, convert termination to the form:



5-6398(F)

where:

$R_1' = R_1 + R_2$

$R_2' = \frac{R_1}{R_2}(R_1 + R_2)$

$C' = \left(\frac{R_2}{R_1 + R_2}\right)^2 C$

ac Interface Using First-Generation Codec

$R_{GX}/R_{TGS}/C_{GS}$ (Z_{TG}): these components give gain shaping to get good gain flatness. These components are a scaled version of the specified complex termination impedance.

Note for pure (600 Ω) resistive terminations, components R_{TGS} and C_{GS} are not used. Resistor R_{GX} is used and is still 4750 Ω.

R_X/R_{T6}: with other components set, the transmit gain (for complex and resistive terminations) R_X and R_{T6} are varied to give specified transmit gain.

$R_{T3}/R_{RCV}/R_{GP}$: for both complex and resistive terminations, the ratio of these resistors sets the receive gain. For resistive terminations, the ratio of these resistors sets the return loss characteristic. For complex terminations, the ratio of these resistors sets the low-frequency return loss characteristic.

$C_N/R_{N1}/R_{N2}$: for complex terminations, these components provide high-frequency compensation to the return loss characteristic.

For resistive terminations, these components are not used and RCVN is connected to ground via a resistor.

R_{HB}: sets hybrid balance for all terminations.

Set Z_{TG}—Gain Shaping

$Z_{TG} = R_{GX} || R_{TGS} + C_{GS}$ which is a scaled version of $Z_{T/R}$ (the specified termination resistance) in the $R_1' || R_2' + C'$ form.

R_{GX} must be 4750 Ω to set SLIC transconductance to 300 V/A.

$R_{GX} = 4750\ \Omega$

At dc, C_{GS} and C' are open.

$R_{GX} = M \times R_1'$

where M is the scale factor.

$$M = \frac{4750}{R_1'}$$

It can be shown:

$R_{TGS} = M \times R_2'$

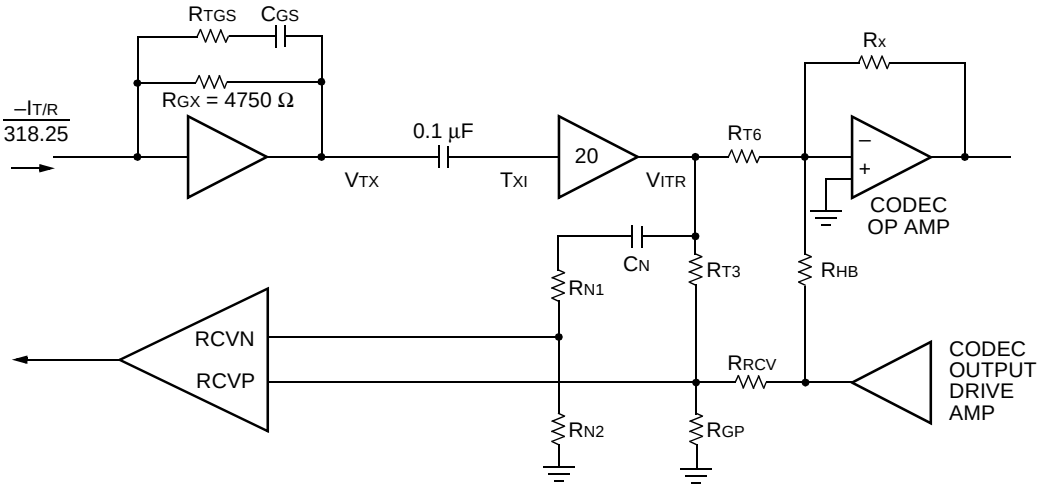
and

$$C_{TGS} = \frac{C'}{M}$$

ac Applications (continued)

Design Examples (continued)

Set Z_{TG}—Gain Shaping (continued)



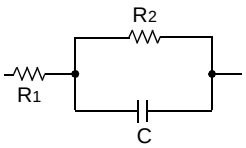
5-6400.P (F)

Figure 24. Interface Circuit Using First-Generation Codec (Blocking Capacitors Not Shown)

Transmit Gain

Transmit gain will be specified as a gain from T/R to PCM, T_X (dB). Since PCM is referenced to 600 Ω and assumed to be 0 dB, and in the case of T/R being referenced to some complex impedance other than 600 Ω resistive, the effects of the impedance transformation must be taken into account.

Again, specified complex termination impedance at T/R is of the form:



5-6396(F)

First, calculate the equivalent resistance of this network at the midband frequency of 1000 Hz.

$$R_{EQ} = \sqrt{\left(\frac{(2\pi f)^2 C_1^2 R_1 R_2^2 + R_1 + R_2}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2 + \left(\frac{2\pi f R_2^2 C_1}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2}$$

Using R_{EQ}, calculate the desired transmit gain, taking into account the impedance transformation:

$$T_X\ (\text{dB}) = T_{X\ (\text{specified[dB]})} + 20\log\sqrt{\frac{600}{R_{EQ}}}$$

$T_{X\ (\text{specified[dB]})}$ is the specified transmit gain. 600 Ω is the impedance at the PCM, and R_{EQ} is the impedance at tip and ring. $20\log\sqrt{\frac{600}{R_{EQ}}}$ represents the power loss/gain due to the impedance transformation.

Note in the case of a 600 Ω pure resistive termination at T/R $20\log\sqrt{\frac{600}{R_{EQ}}} = 20\log\sqrt{\frac{600}{600}} = 0$.

Thus, there is no power loss/gain due to impedance transformation and T_X (dB) = $T_{X\ (\text{specified[dB]})}$.

Finally, convert T_X (dB) to a ratio, g_{TX}:

T_X (dB) = 20log g_{TX}

The ratio of R_X/R_{T6} is used to set the transmit gain:

$\frac{R_X}{R_{T6}} = g_{TX} \bullet \frac{318.25}{20} \bullet \frac{1}{M}$ with a quad Agere codec such as T7504:

$R_X < 200\ k\Omega$

ac Applications (continued)

Design Examples (continued)

Receive Gain

Ratios of R_{RCV}, R_{T3}, and R_{GP} will set both the low-frequency termination and receive gain for the complex case. In the complex case, additional high-frequency compensation, via C_N, R_{N1}, and R_{N2}, is needed for the return loss characteristic. For resistive termination, C_N, R_{N1}, and R_{N2} are not used and RCVN is tied to ground via a resistor.

Determine the receive gain, g_{RCV}, taking into account the impedance transformation in a manner similar to transmit gain.

$$R_X\ (dB) = R_{X\ (specified[dB])} + 20\log\sqrt{\frac{R_{EQ}}{600}}$$

$$R_X\ (dB) = 20\log g_{RCV}$$

Then:

$$g_{RCV} = \frac{4}{1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}}$$

and low-frequency termination

$$Z_{TER(low)} = \frac{2400}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}} + 2R_P + 50\ \Omega$$

$Z_{TER(low)}$ is the specified termination impedance assuming low frequency (C or C´ is open).

R_P is the series protection resistor.

50 Ω is the typical internal feed resistance.

These two equations are best solved using a computer spreadsheet.

Next, solve for the high-frequency return loss compensation circuit, C_N, R_{N1}, and R_{N2}:

$$C_N R_{N2} = \frac{2R_P}{2400}\ C_G\ R_{TGP}$$

$$R_{N1} = R_{N2}\left[\frac{2400}{2R_P}\left(\frac{R_{TGS}}{R_{TGP}}\right) - 1\right]$$

There is an input offset voltage associated with nodes RCVN and RCVP. To minimize the effect of mismatch of this voltage at T/R, the equivalent resistance to ac ground at RCVN should be approximately equal to that at RCVP. Refer to Figure 25 (with dc blocking capacitors). To meet this requirement, $R_{N2} = R_{GP} \parallel R_{T3}$.

Hybrid Balance

Set the hybrid cancellation via R_{HB}.

$$R_{HB} = \frac{R_X}{g_{RCV} \times g_{TX}}$$

If a 5 V only codec such as the Agere T7504 is used, dc blocking capacitors must be added as shown in Figure 25. This is because the codec is referenced to 2.5 V and the SLIC to ground—with the ac coupling, a dc bias at T/R is eliminated and power associated with this bias is not consumed.

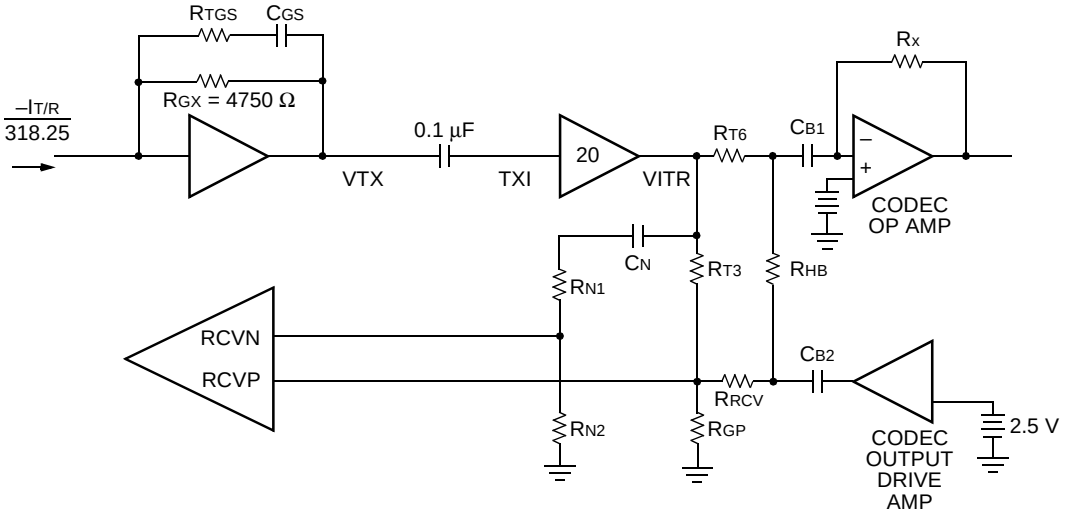
Typically, values of 0.1 µF to 0.47 µF capacitors are used for dc blocking. The addition of blocking capacitors will cause a shift in the return loss and hybrid balance frequency response toward higher frequencies, degrading the lower-frequency response. The lower the value of the blocking capacitor, the more pronounced the effect is, but the cost of the capacitor is lower. It may be necessary to scale resistor values higher to compensate for the low-frequency response. This effect is best evaluated via simulation. A *PSPICE*® model for the L9215 is available.

Design equation calculations seldom yield standard component values. Conversion from the calculated value to standard value may have an effect on the ac parameters. This effect should be evaluated and optimized via simulation.

ac Applications (continued)

Design Examples (continued)

Blocking Capacitors



5-6401.M (F)

Figure 25. ac Interface Using First-Generation Codec (Including Blocking Capacitors) for Complex Termination Impedance

ac Applications (continued)

Design Examples (continued)

Blocking Capacitors (continued)

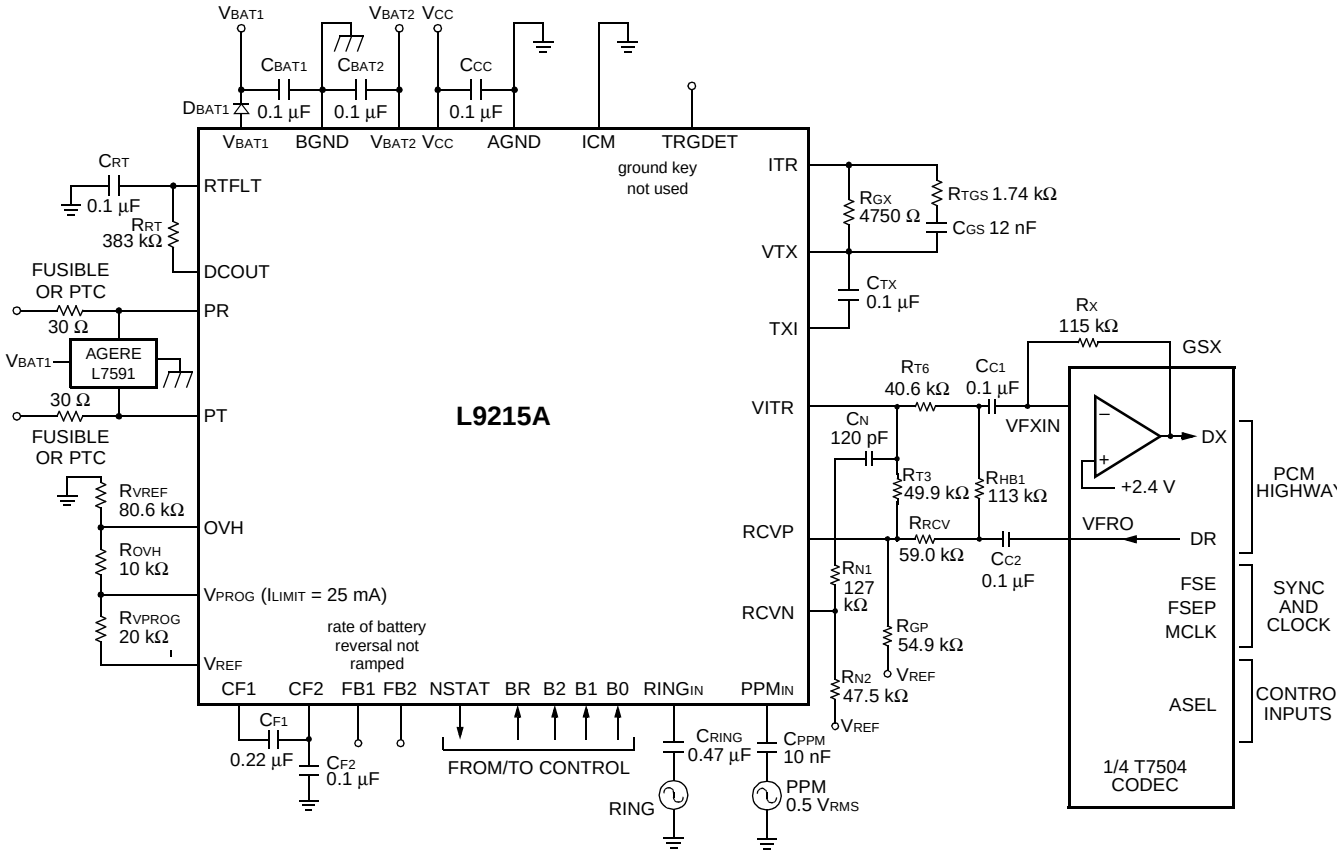


Figure 26. Agere T7504 First-Generation Codec Complex Termination; Meter Pulse Application

Applications (continued)

Design Examples (continued)

Blocking Capacitors (continued)

Table 25. Parts List L9215; Agere T7504 First-Generation Codec Complex Termination; Meter Pulse Application

Termination impedance = 220 Ω + (820 Ω || 115 nF), hybrid balance = 220 Ω + (820 Ω || 115 nF) Tx = 0 dBm, Rx = 0 dBm.

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PT}	30 Ω	1%	Fusible or PTC	Protection resistor.
R_{PR}	30 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Agere L7591	—	—	Secondary protection.
Power Supply				
C_{BAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.1 µF	20%	10 V	V_{CC} filter capacitor.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
dc Profile				
R_{VPROG}	20 kΩ	1%	1/16 W	With R_{VREF} fixes dc current limit.
R_{VOVH}	10 kΩ	1%	1/16 W	With R_{VREF} fixes overhead voltage.
R_{VREF}	80.6 kΩ	1%	1/16 W	With R_{VPROG} fixes dc current limit/overhead.
Ring/Ring Trip				
C_{RING}	0.47 µF	20%	10 V	ac-couple input ring signal.
C_{RT}	0.1 µF	20%	10 V	Ring trip filter capacitor.
R_{RT}	383 kΩ	1%	1/16 W	Ring trip filter resistor.
PPM				
C_{PPM}	10 nF	20%	10 V	ac-couple PPM input.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
R_{TGS}	1.74 kΩ	1%	1/16 W	Gain shaping for complex termination.
C_{GS}	12 nF	5%	10 V	Gain shaping for complex termination.
C_{TX}	0.1 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.
C_{C2}	0.1 µF	20%	10 V	dc blocking capacitor.
R_{T3}	49.9 kΩ	1%	1/16 W	With R_{GP} and R_{RCV}, sets termination impedance and receive gain.
R_{T6}	40.2 kΩ	1%	1/16 W	With R_X, sets transmit gain.
R_X	115 kΩ	1%	1/16 W	With R_{T6}, sets transmit gain.
R_{HB1}	113 kΩ	1%	1/16 W	With R_X, sets hybrid balance.
R_{RCV}	59.0 kΩ	1%	1/16 W	With R_{GP} and R_{T3}, sets termination impedance and receive gain.
R_{GP}	54.9 kΩ	1%	1/16 W	With R_{RCV} and R_{T3}, sets termination impedance and receive gain.
C_N	120 pF	20%	10 V	High frequency compensation.
R_{N1}	127 kΩ	1%	1/16 W	High frequency compensation.
R_{N2}	47.5 kΩ	1%	1/16 W	High frequency compensation, compensate for dc offset at RCVP/RCVN.

ac Applications (continued)

Design Examples (continued)

Third-Generation Codec ac Interface Network—Complex Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T8536 third-generation codec. All ac parameters are programmed by the T8536. Note this codec differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. For illustration purposes, 0.5 Vrms PPM injection was assumed in this example and no meter pulse rejection is used. Also, this example illustrates the device using programmable overhead and current limit. Please see the T8535/6 data sheet for information on coefficient programming.

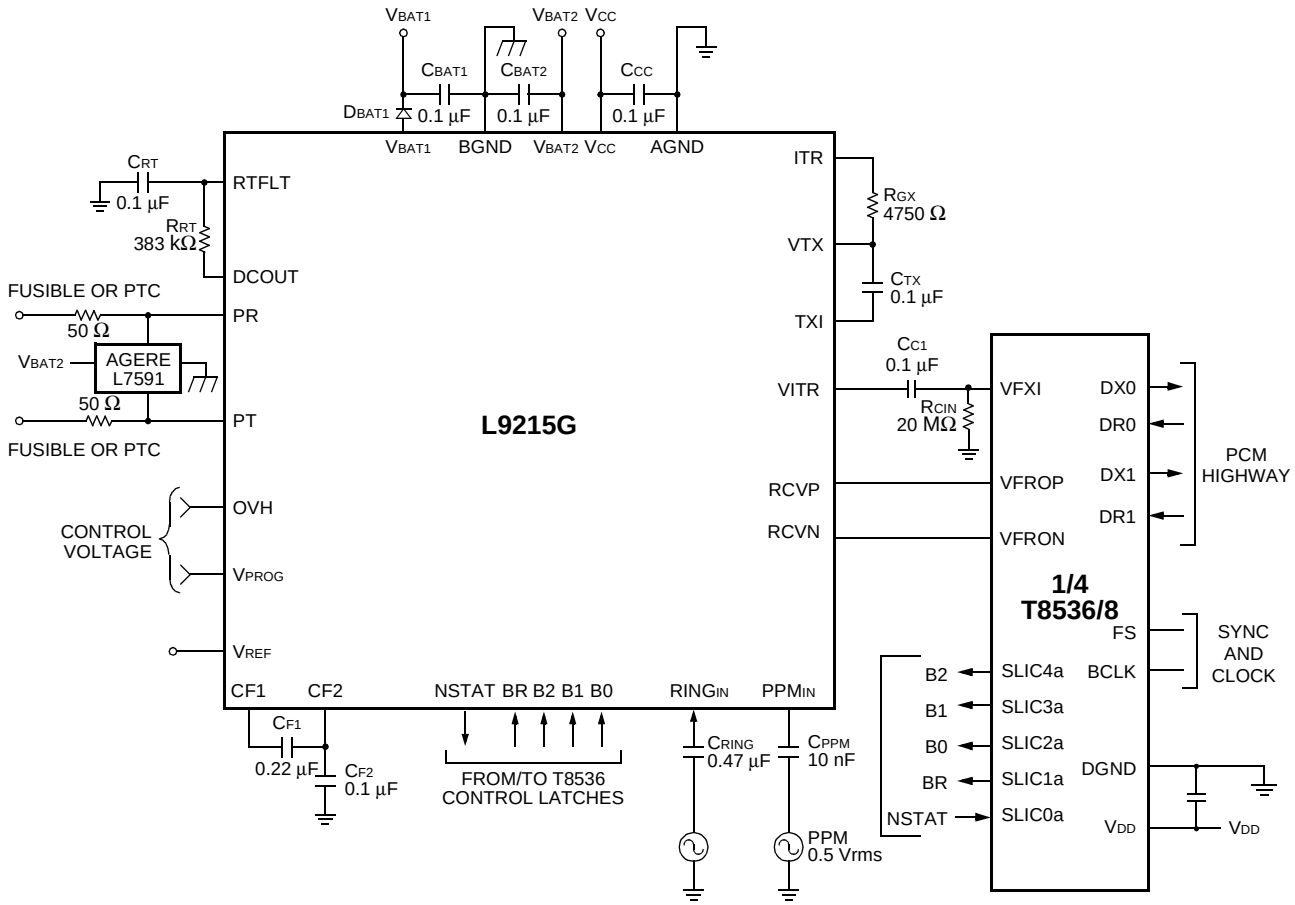


Figure 27. Third-Generation Codec ac Interface Network; Complex Termination

ac Applications (continued)

Design Examples (continued)

Third-Generation Codec ac Interface Network—Complex Termination (continued)

Table 26. Parts List L9215; Agere T8536 Third-Generation Codec Meter Pulse Application ac and dc Parameters; Fully Programmable

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PT}	50 Ω	1%	Fusible or PTC	Protection resistor*.
R_{PR}	50 Ω	1%	Fusible or PTC	Protection resistor*.
Protector	Agere L7591	—	—	Secondary protection.
Power Supply				
C_{BAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.1 µF	20%	10 V	V_{CC} filter capacitor.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
Ring/Ring Trip				
C_{RING}	0.47 µF	20%	10 V	ac-couple input ring signal.
C_{RT}	0.1 µF	20%	10 V	Ring trip filter capacitor.
R_{RT}	383 kΩ	1%	1/16 W	Ring trip filter resistor.
PPM				
C_{PPM}	10 nF	20%	10 V	ac-couple PPM input.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
R_{CIN}	20 MΩ	5%	1/16 W	dc Bias
C_{TX}	0.1 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.

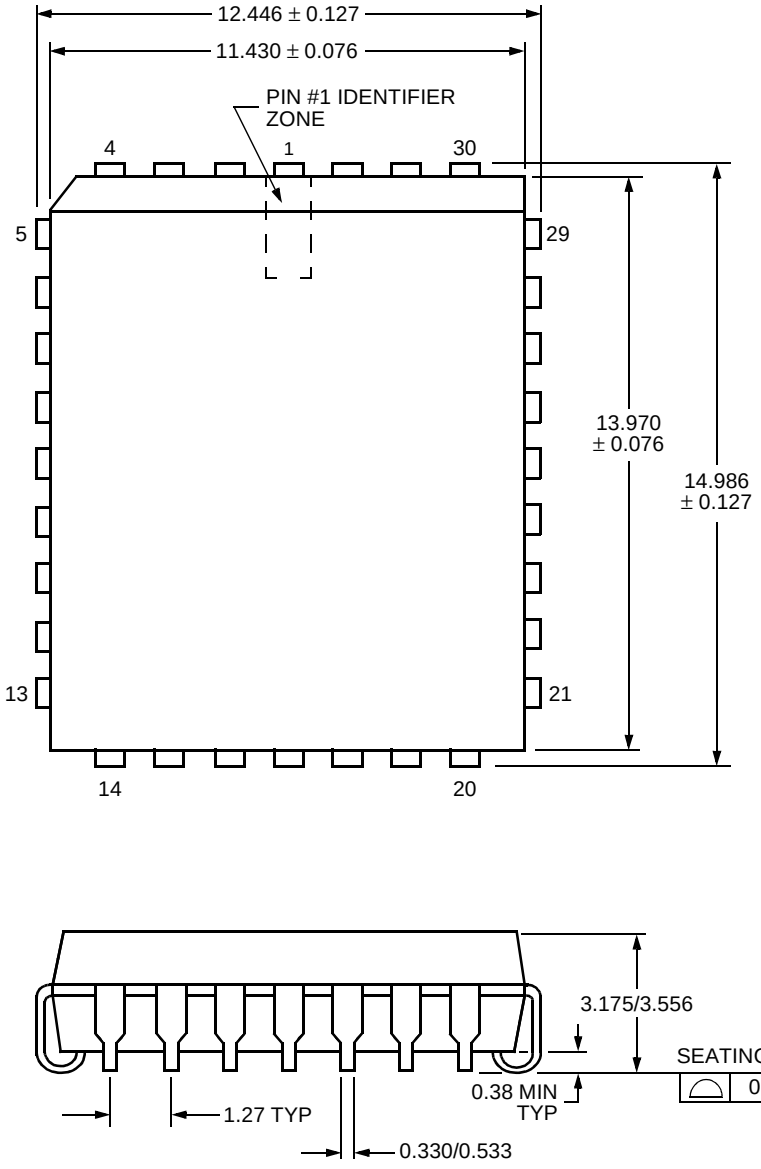
* For loop stability, increase to 50 Ω minimum if synthesizing 900 Ω or 900 Ω + 2.16 µF termination impedance.

Outline Diagrams

32-Pin PLCC

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.



5-3813F

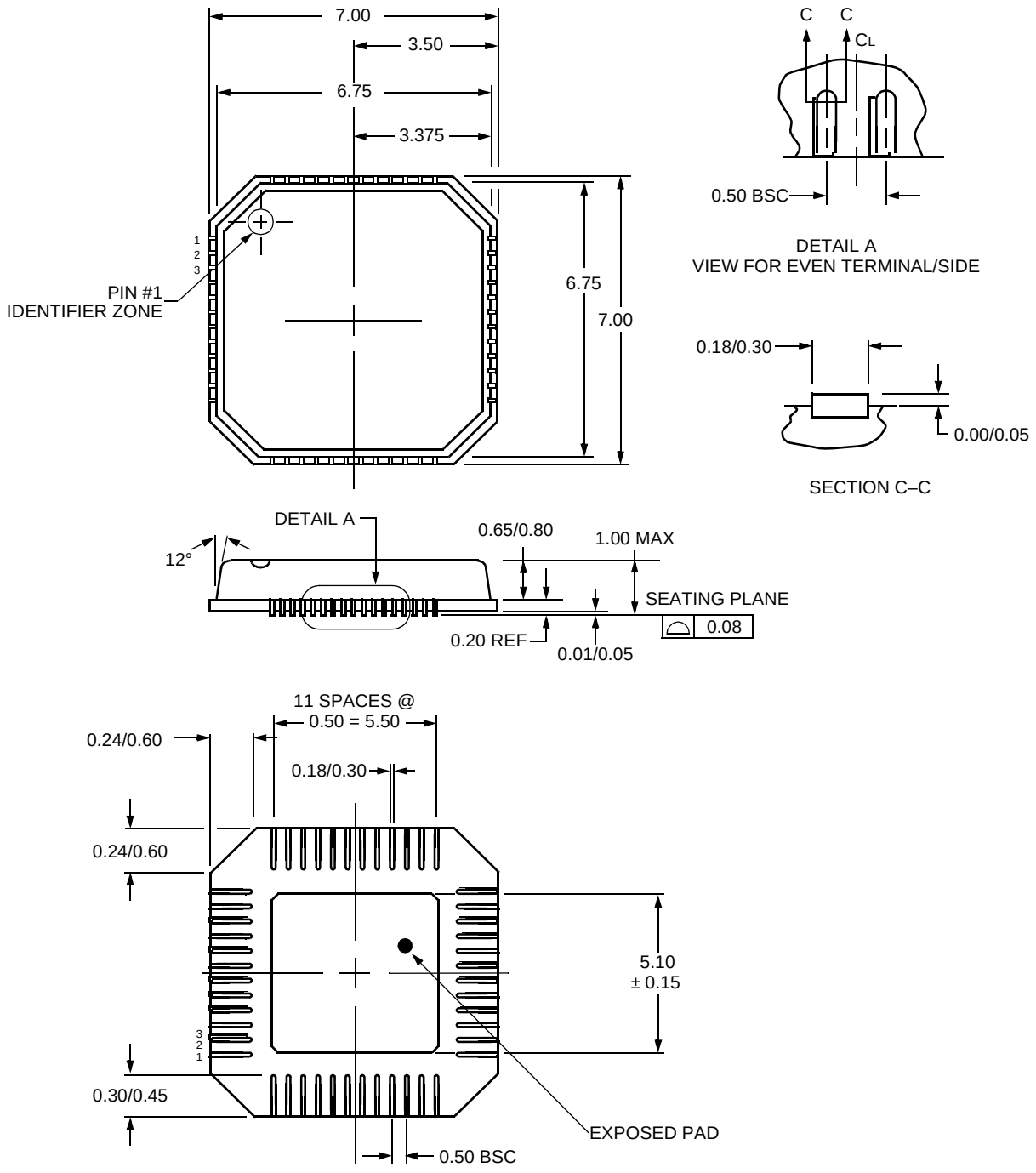
Outline Diagrams (continued)

48-Pin MLCC

Dimensions are in millimeters.

Notes: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

The exposed pad on the bottom of the package will be at V_{BAT1} potential.



0195mod

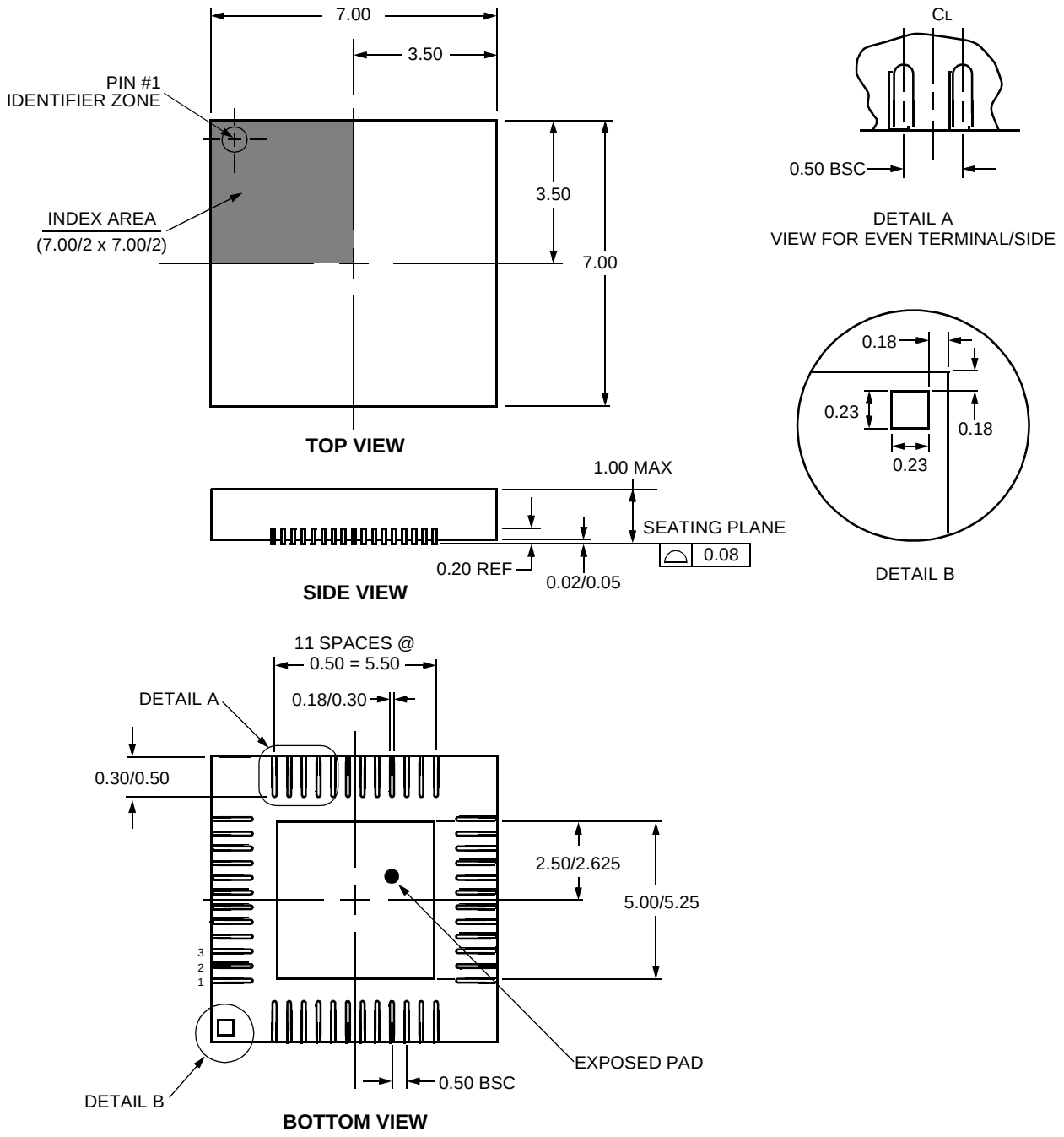
Outline Diagrams (continued)

48-Pin MLCC, JEDEC MO-220 VKKD-2

Dimensions are in millimeters.

Notes: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

The exposed pad on the bottom of the package will be at V_{BAT1} potential.



Ordering Information

Device Part No.	Description	Package	Comcode
LUCL9215AAU-D	SLIC Gain = 8	32-Pin PLCC Dry Bag	108327214
LUCL9215AAU-DT	SLIC Gain = 8	32-Pin PLCC Tape & Reel	108327222
LUCL9215GAU-D	SLIC Gain = 2	32-Pin PLCC Dry Bag	108417932
LUCL9215GAU-DT	SLIC Gain = 2	32-Pin PLCC Tape & Reel	108417940
LUCL9215ARG-D	SLIC Gain = 8	48-Pin MLCC Dry Bag	108955451
LUCL9215GRG-D	SLIC Gain = 2	48-Pin MLCC Dry Bag	108955444

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DS01-299ALC (Replaces DS01-104ALC)

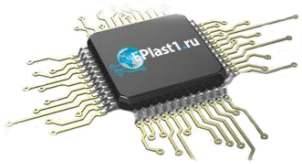
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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