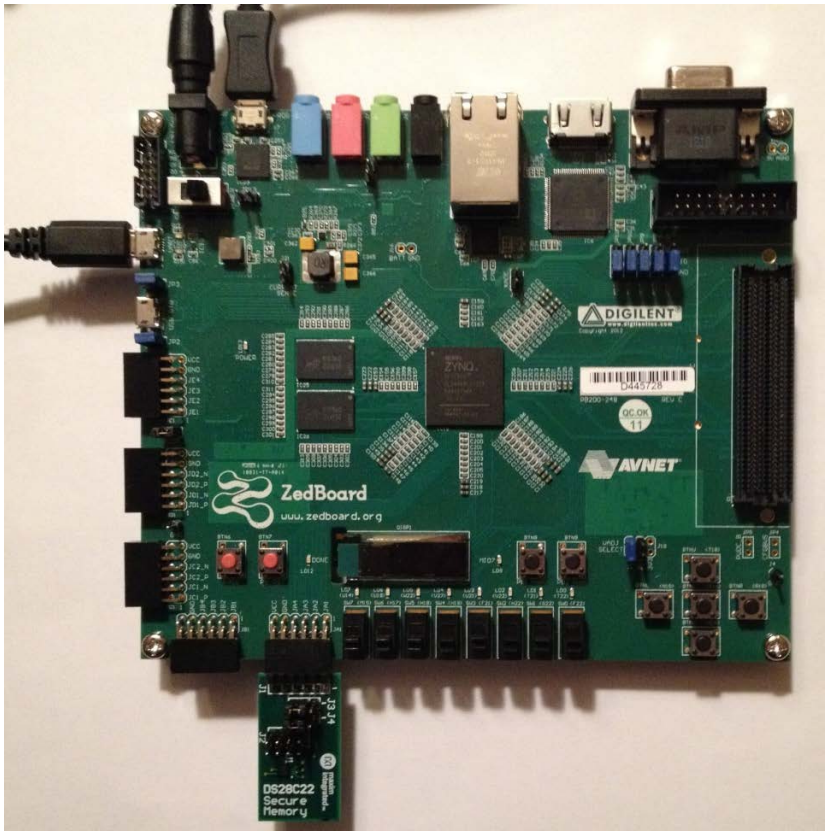
MAXREFDES43# ZedBoard Quick Start Guide

Rev 0; 4/15



Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

Table of Contents

1. Required Equipment

- MAXREFDES43# board
- ZedBoard™ development kit
- To run the binary from SD card:
  - Host PC with Windows® OS with Terminal Software installed (HyperTerminal) and two USB ports
  - CP2104 device drivers (Silicon Labs USB-UART)
  - 4GB FAT32 formatted SD card
- To run the software from the Xilinx® SDK:
  - PC with Windows OS with Xilinx SDK version 14.4 and two USB ports
  - License for Xilinx EDK/SDK (free WebPACK™ license is OK)

2. Overview

The MAXREFDES43# software can be downloaded to the ZedBoard via two methods:

- (Easiest) Boot from an SD card containing a binary file that loads the necessary CPU bootloader, FPGA bitstream, and MAXREFDES43# executable file. This approach is explained in detail in Section 3 of this document.
- (Flexible) Use the Xilinx SDK to download the board bitstream and executable file. This approach allows the source code to be modified. This approach is explained in detail of Section 4 of this document.

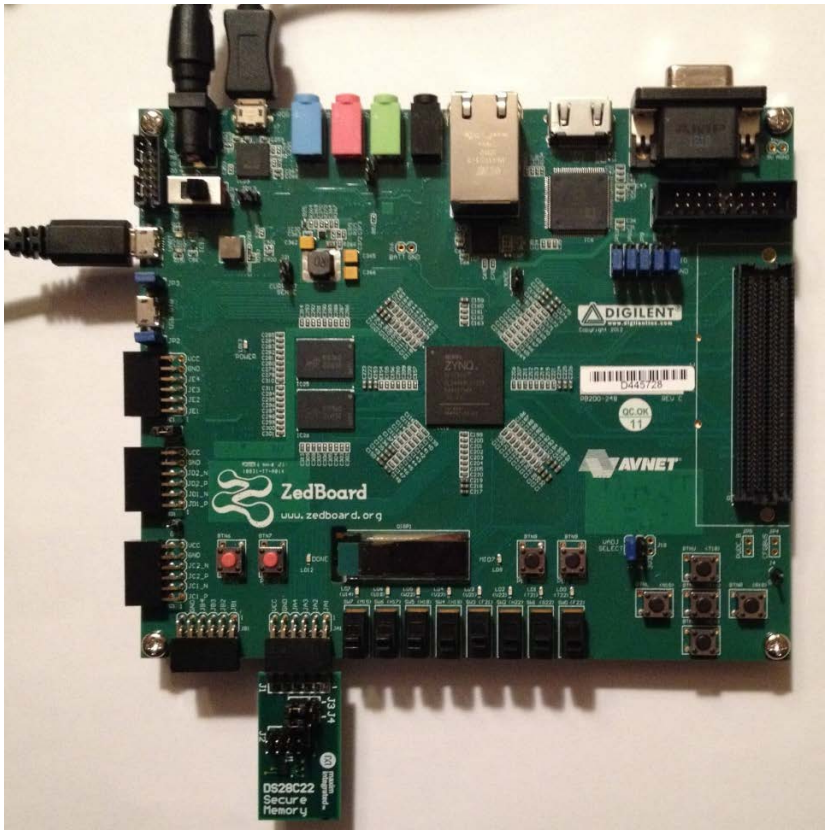


Figure 1. MAXREFDES43# board connected to ZedBoard development kit.

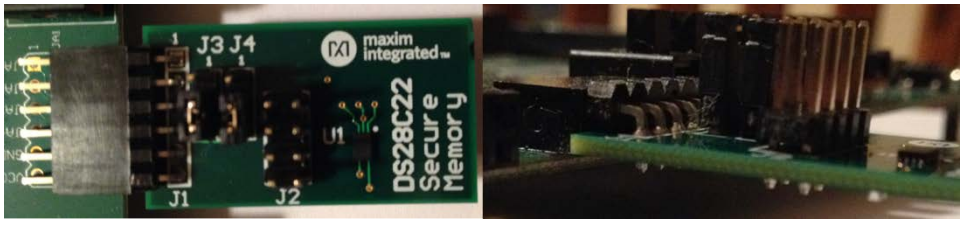


Figure 2. Pmod™ connector alignment.

3. Boot from an SD Card

The steps below describe how to download a binary image (BOOT.BIN), install on an SD card, and begin using the MAXREFDES43# system.

1) Download the latest BOOT.BIN file from the MAXREFDES43# page.
2) Obtain a FAT32 formatted 4GB SD card such as the one provided with the ZedBoard.
3) Copy the BOOT.BIN file onto the SD card. A USB-to-SD adapter and micro-SD to SD adapter may be required to do this on a Windows PC.
4) Ensure the only file on the micro-SD card is the BOOT.BIN file. **Note that if using the Avnet-supplied SD card, it comes pre-installed with a Linux test image. This image needs to be removed.**
5) Remove the SD card from the host PC. Make sure the ZedBoard is powered off, and insert the SD card in the ZedBoard (Figure 3).
6) Configure the ZedBoard boot source jumpers to boot from SD (Figure 4).
7) Insert the MAXREFDES43# reference board in the JA1 connector (Figure 2). Note the orientation so that the component side of the MAXREFDES43# board faces the component side of the ZedBoard and the MAXREFDES43# must be plugged into the top row of the Pmod connector.
8) Connect to your PC through both the UART connector, J14, and the programming connector, J17. (Alternatively, you can connect to the JTAG connector to the ZedBoard, instead of the programming connector.) Connect 12V power supply to barrel jack, J20. Power up the ZedBoard development kit by turning SW8 to the On position. If the BOOT.BIN file has loaded successfully, the red LEDs (LD0−LD7) should begin blinking, indicating that the MAXREFDES43 software is running.
9) Open HyperTerminal or a similar terminal program on the PC. Select a serial connection and find the appropriate COM port, usually a higher number port, and configure the connection for 115200, n, 8, 1, none (flow control).
10) Press the zero “**0**” key to display the MAXREFDES43# demonstration menu, (Figure 5).
11) Press the nine “**9**” key to return to the MAXREFDES43# main menu (Figure 6).

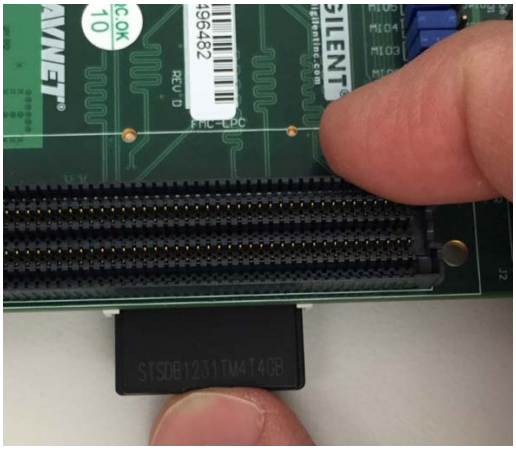


Figure 3. Inserting the SD card into the ZedBoard.

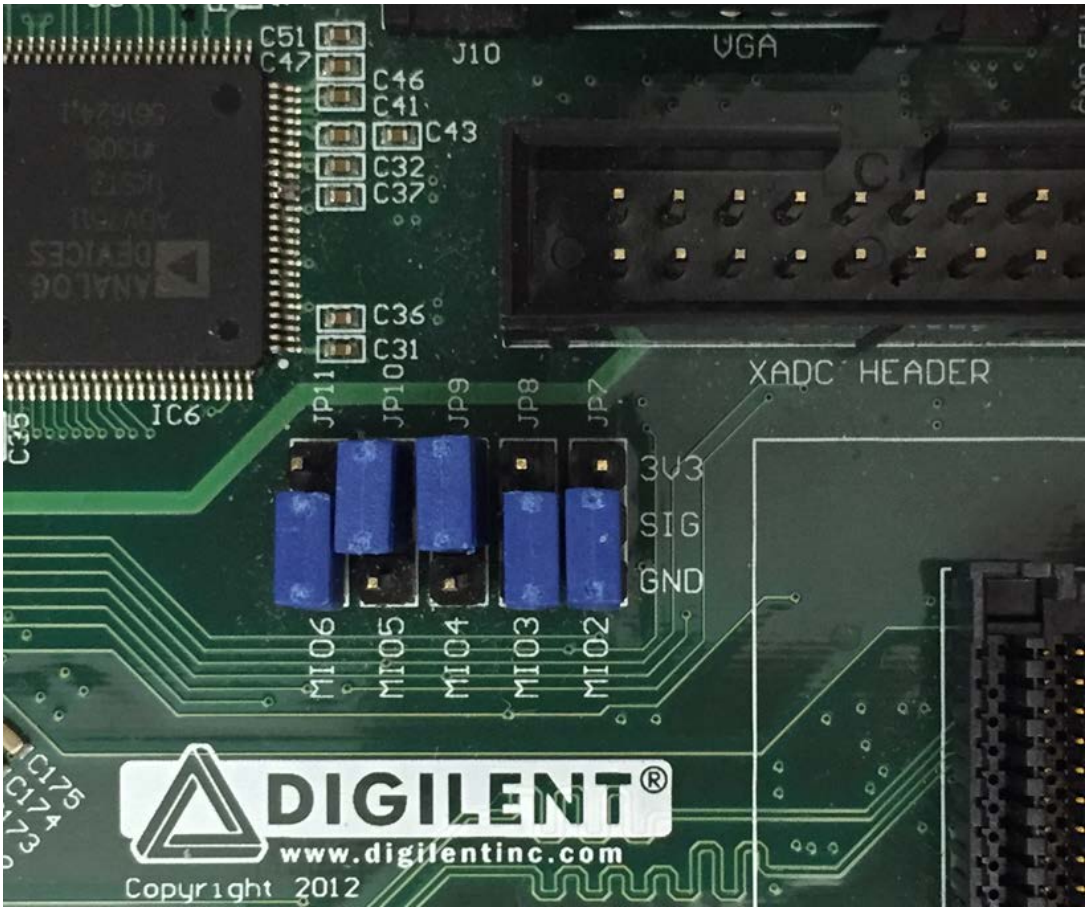


Figure 4. Jumper confirmation for booting from the BOOT.BIN file.

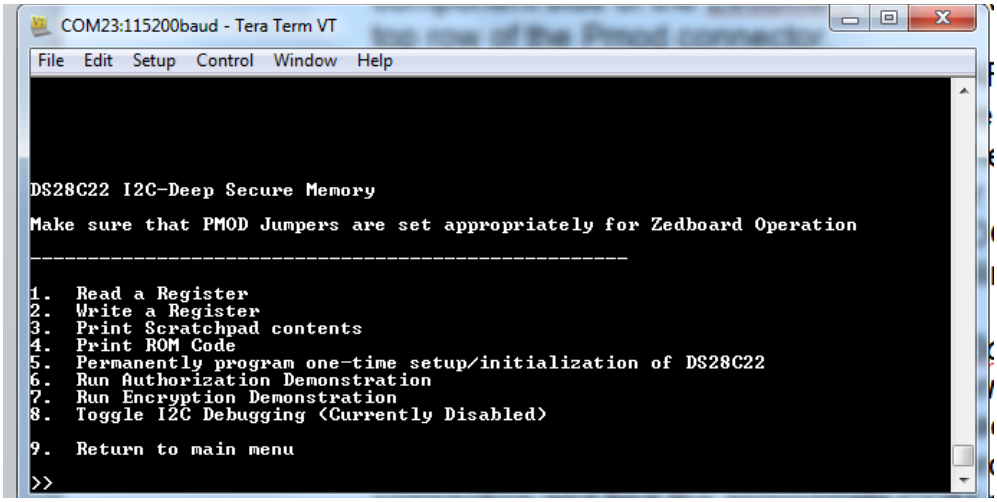


Figure 5. MAXREFDES43# demonstration menu.

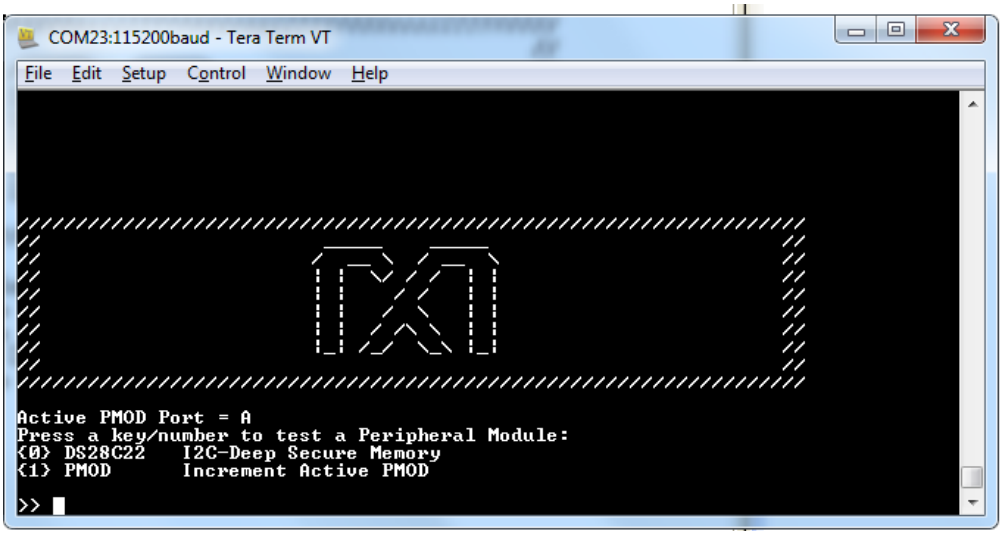


Figure 6. MAXREFDES43# main menu.

4. Download Demonstration from Xilinx SDK

Below is a high-level overview of the steps required to quickly get the MAXREFDES43# design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. **The MAXREFDES43# subsystem reference design will be referred to as MAXREFDES43# throughout this document.**

1) Connect the MAXREFDES43# board to the JA1 port of a ZedBoard development kit as shown in Figure 1. Ensure the connector is aligned as shown in Figure 2 with the 6-pin Pmod connector of MAXREFDES43# connected to the top row of the ZedBoard Pmod connector.
2) Download the latest **RD43V02_70.ZIP** file located at the MAXREFDES43# page.
3) Extract the **RD43V02_70.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (top_mem.bit) file to the board. This bitstream contains the FPGA hardware design with Master Secret (see Appendix C: Pre-Install Master Secret into Bitstream for more details on generation of Master Secret) and software bootloader.
6) Open a terminal program to communicate with FPGA board.
7) Use Xilinx SDK to download and run the executable file (.ELF) on the ARM® Cortex®-A9.

5. Included Files

The top level of the hardware design is a Xilinx ISE® Project Navigator Project (.XISE) for Xilinx ISE version 14.4. The C-code design instantiates the Zynq® ARM core, the support hardware required to run the Zynq ARM core, and the peripherals that interface to the Pmod ports. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the MAXREFDES43# subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

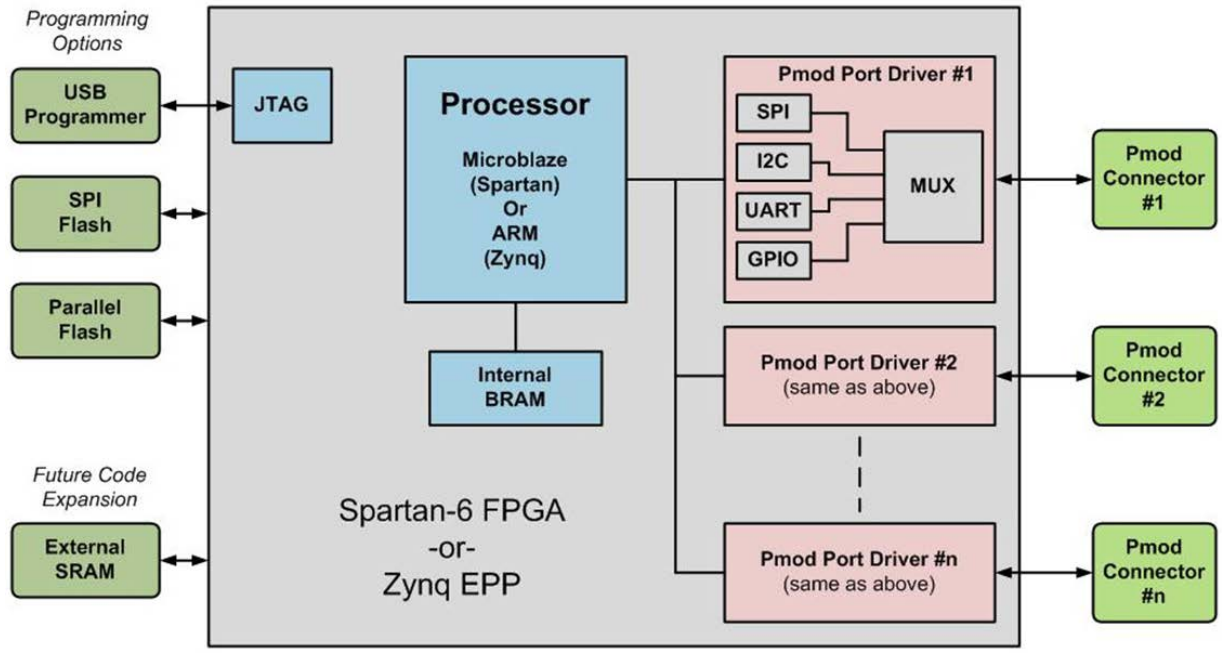


Figure 7. Block diagram of FPGA hardware design.

6. Procedure

1. Connect the MAXREFDES43# board to the JA1 port of a ZedBoard development kit as shown in Figure 1. The other Pmod ports, JB1, JC1, JD1, can be enabled at a later time. Make sure that jumpers are connected across pins 2 and 3 of J3 and across pins 2 and 3 of J4. This is the ZedBoard configuration. Connect the ZedBoard to your PC through both the UART connector, J14, and the programming connector, J17 (alternatively, you can connect to the JTAG connector to the ZedBoard, instead of the programming connector). Connect 12V power supply to barrel jack, J20. Power up the ZedBoard development kit by turning SW8 to the On position. The MAXREFDES43# board is completely powered from the ZedBoard development kit and no external power is required.

2. Download the latest **RD43V02_70.ZIP** file at **www.maximintegrated.com/MAXREFDES43.** All files available for download are available under the **DESIGN RESOURCES** tab.

3. Extract the **RD43V02_70.ZIP** file to a directory on your PC. The location is arbitrary but the path prior to where you extract the .ZIP file must not exceed 82 characters due to the Windows 250-character total path limitation. For example, this 90-character preceding path would be an example of a path that would be too long:

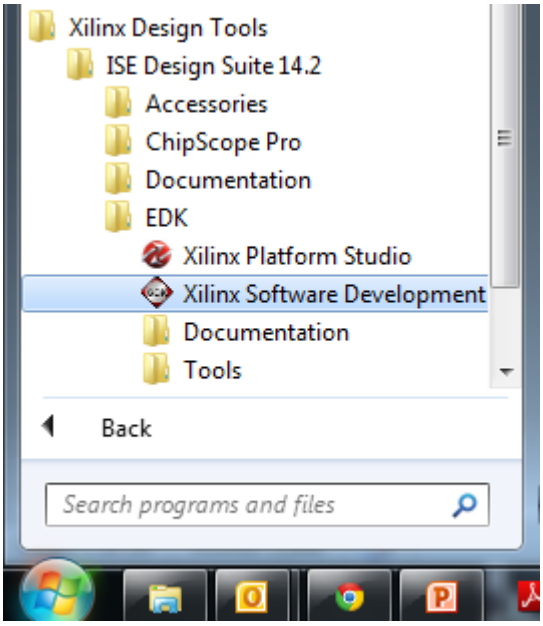
   C:\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\RD43V02_40.ZIP
   (This path is too long.)

   In addition, the Xilinx tools require the path to not contain any spaces.

   C:\Do Not Use Spaces In The Path\RD43V02_70.ZIP
   (This path has spaces.)

   For the purposes of this document, it will be **C:\designs\maxim\RD43V02_70**. See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

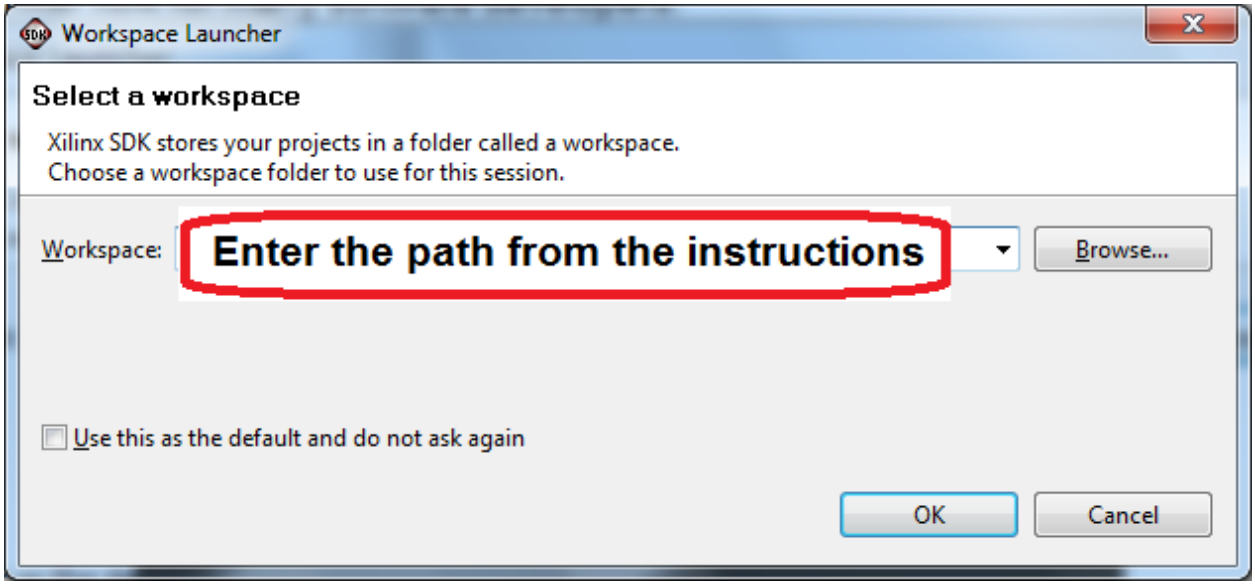
4. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu. Note that this design requires Xilinx EDK/SDK version 14.4.



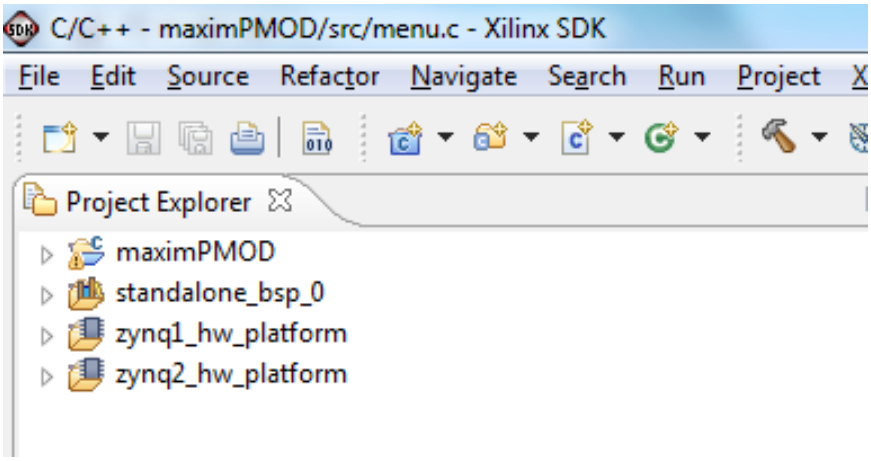
5. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

   C:\designs\maxim\RD43V02_70\Zedboard_HDL_and_SW\v2_7\sdkWorkspace

   Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



6. Review the SDK IDE. The **Project Explorer** in the upper left tab should have four components as shown in the image below. If all four subfolders are present, you can skip the next step.

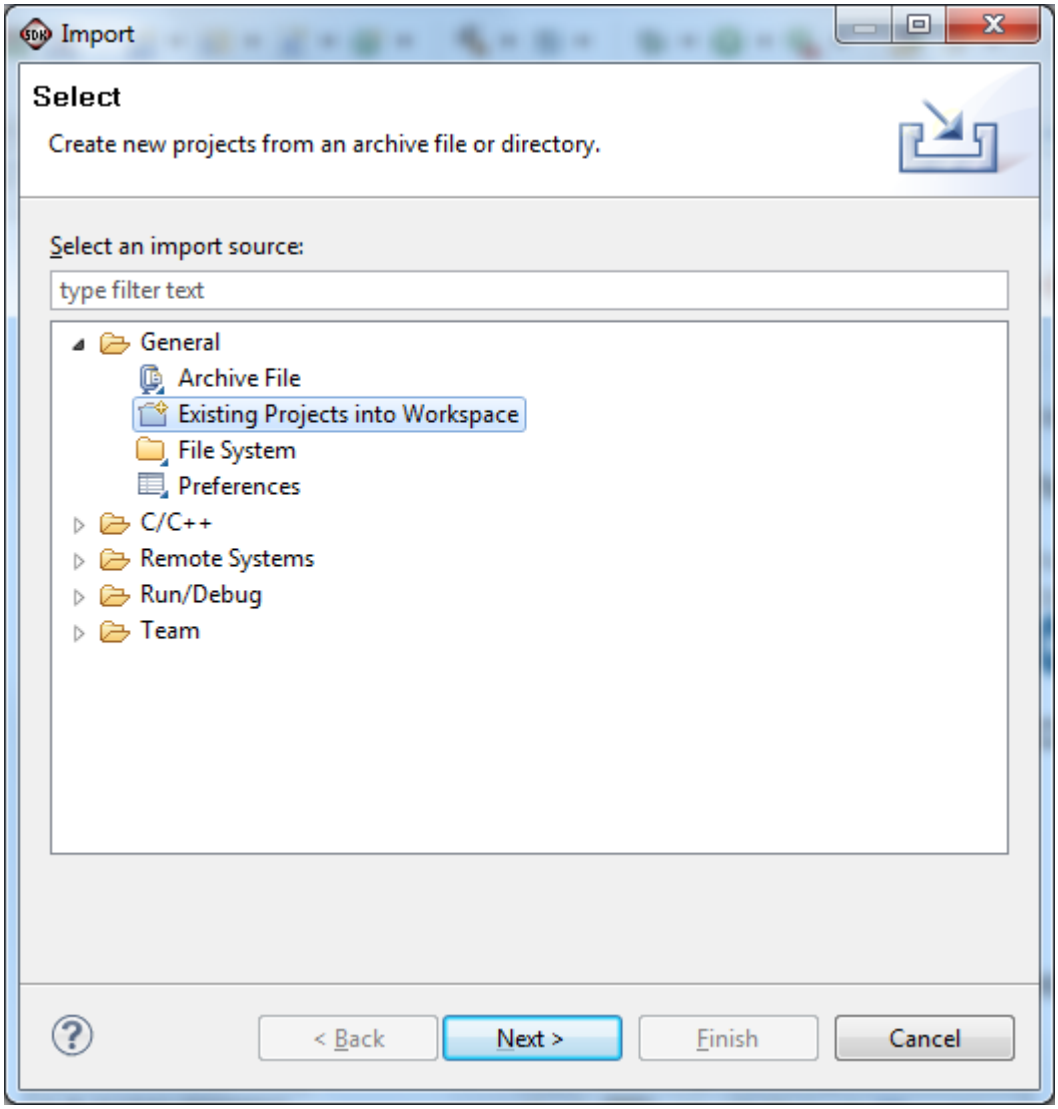


7. If the **Project Explorer** does not contain these four subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

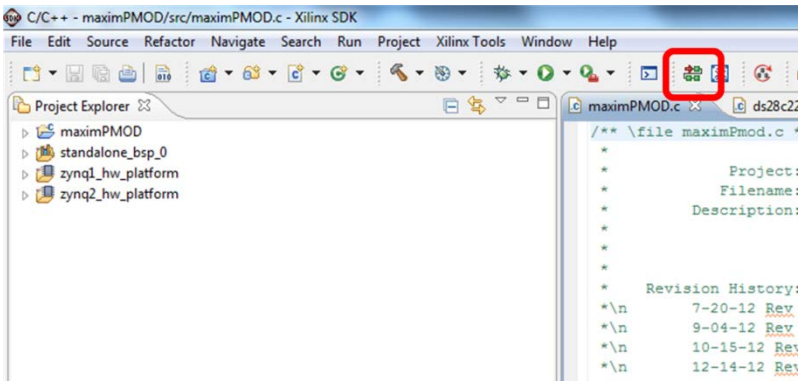
   C:\designs\maxim\RD43V02_70\Zedboard_HDL_and_SW\v2_7sdkWorkspace

   and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

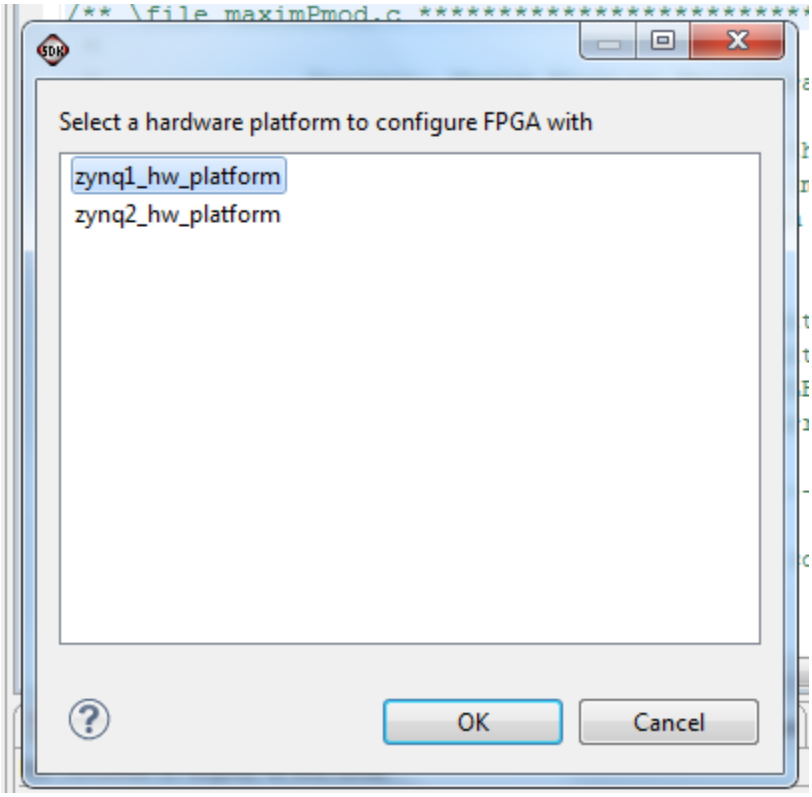
   Click **Finish** to import the projects.



8. Download the bitstream (top_mem.bit) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices). **Note:** The top_mem.bit file is pre-generated per Appendix C: Pre-Install Master Secret into Bitstream to contain the Master Secret.



The **Program FPGA** dialog box appears. A prompt will appear, requiring selection of **zynq1_hw_platform** or **zynq2_hw_platform**. Select **zynq1_hw_platform**, as indicated below.



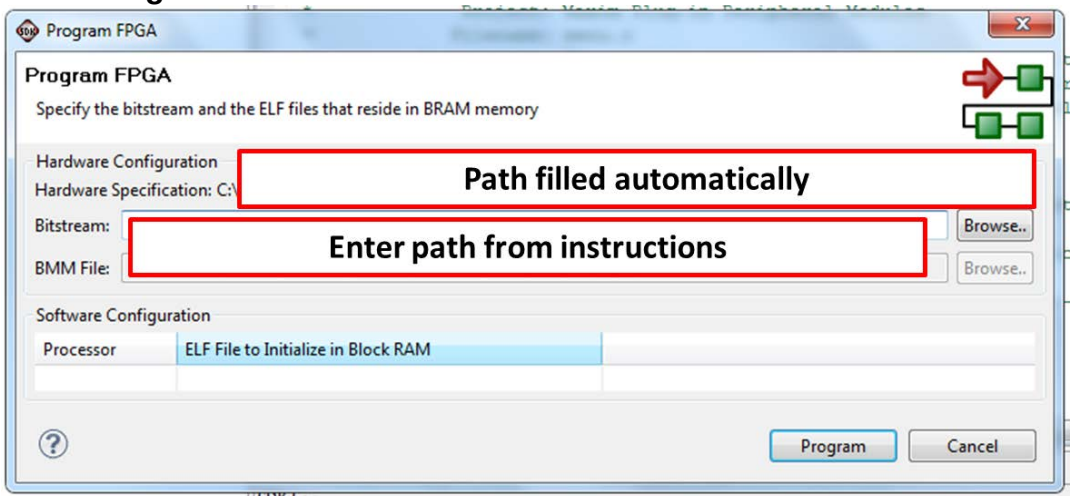
From here, an FPGA bitstream (top_mem.bit) file is selected as well as an FPGA BMM (.BMM) file. Be sure to select the .BIT file and the .BMM by using the paths below.

Bitstream:
C:\designs\maxim\RD43V02_70\Zedboard_HDL_and_SW\v2_7\top_mem.bit

BMM File:
C:\designs\maxim\RD43V02_70\Zedboard_HDL_and_SW\v2_7\edkBmmFile.bmm

The BMM file request may be grayed out. This does not matter and the system still works.

Press **Program**.



It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

9. Set up the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

   The ZedBoard utilizes the Cypress CY7C64255 USB-to-UART Bridge IC, so if Windows does not automatically recognize it, you may need to install Cypress's virtual COM port (VCP) driver. For directions on how to install the driver, download the "Cypress USB-to-UART Setup Guide" from here: www.zedboard.org/support/documentation/1521

   Once installed, Windows assigns a previously unused COM port. Use the Windows **Control Panel | System | Device Manager** to determine the COM port number. (It will be named **USB Serial Port**). Make a note of which COM port this is. That information is needed in the next step.

   Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

   bits per second: **921,600**;

   data bits: **8**;

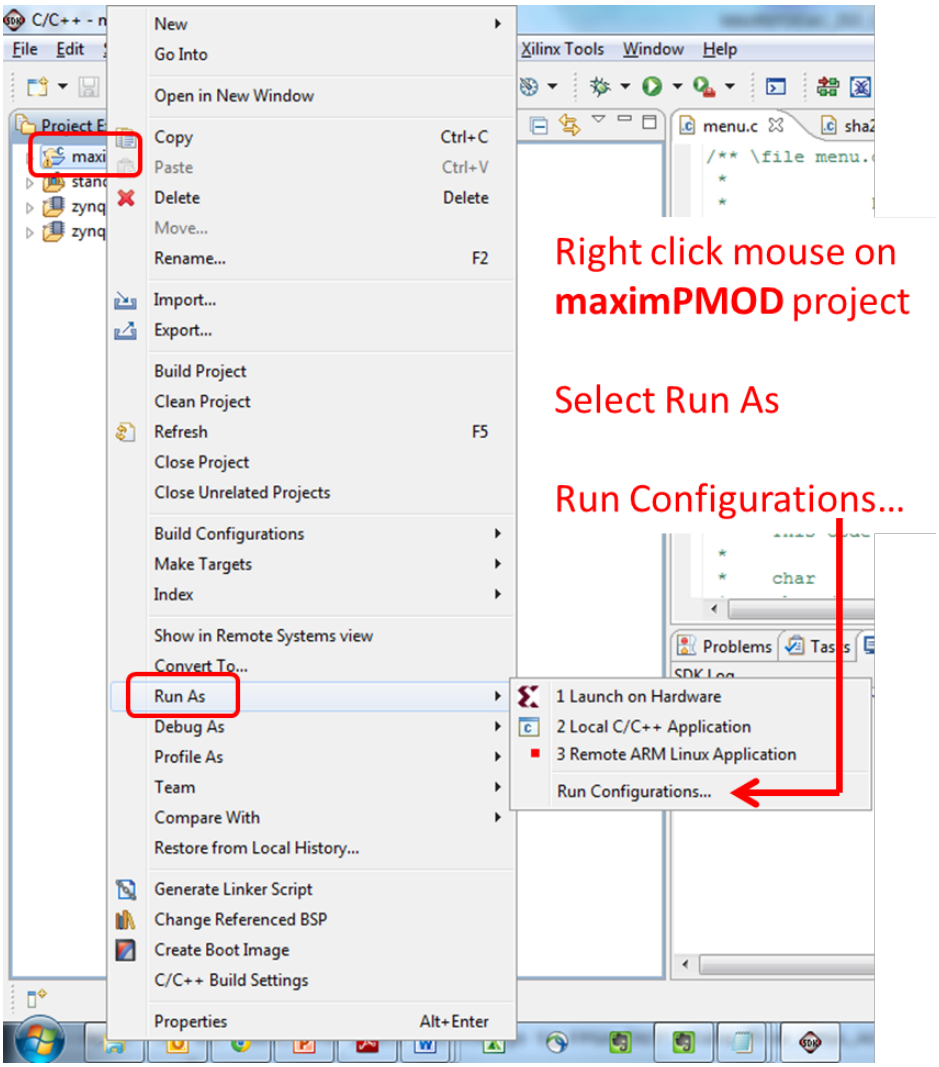
   parity: **none**;

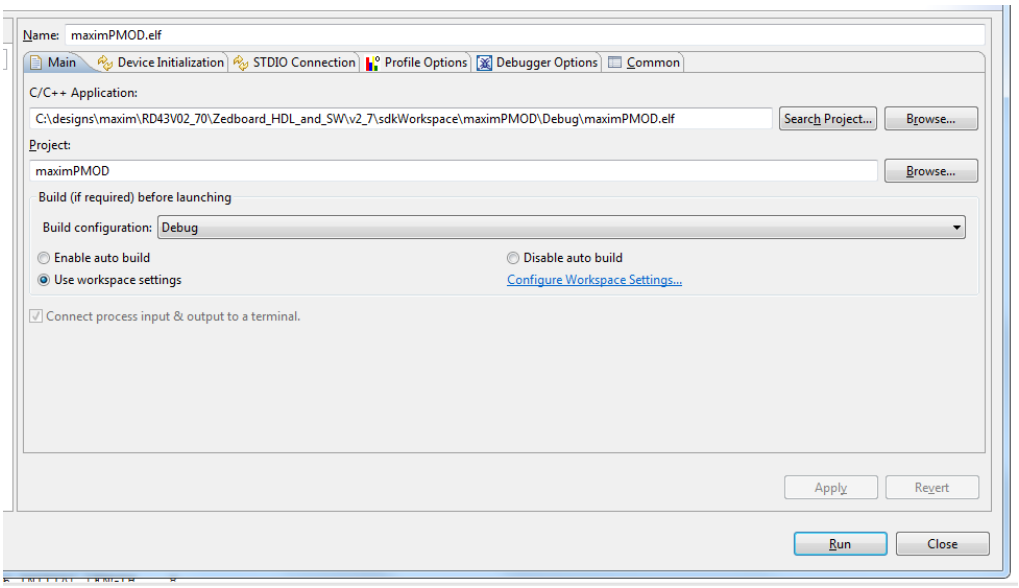
   stop bits: **1**;

   flow control: **none**.

10. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the ARM Cortex-A9 using the following steps.

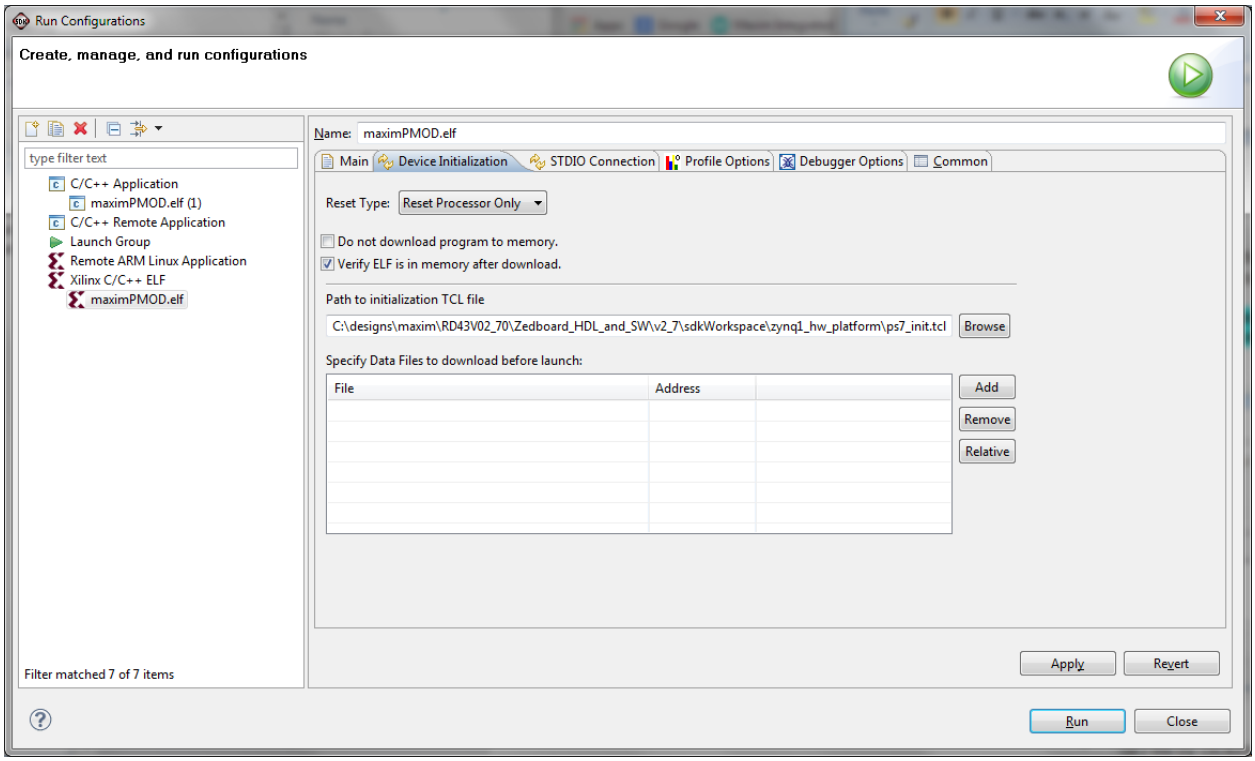
    Right-click the mouse while the **maximPMOD** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.





Select the maximPMOD.elf file by selecting **Project Search**, or by selecting **Browse** to find the correct file location, similar to:

C:\designs\maxim\RD43V02_70\Zedboard_HDL_and_SW\v2_7\sdkWorkspace\maximPMOD\Debug\maximPMOD.elf



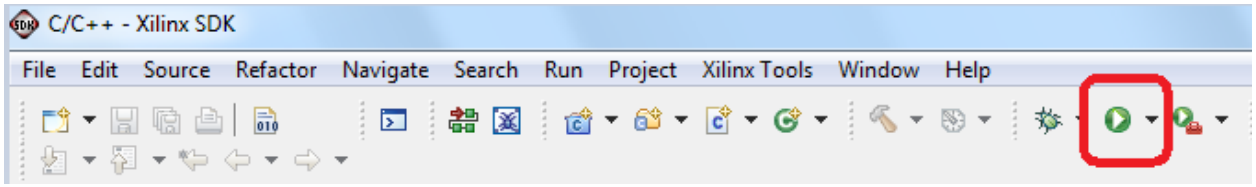
Also, select the ps7_init.tcl file by clicking on **Device Initialization** and browsing to the ps7_init.tcl file, in a location similar to:

C:\designs\maxim\RD43V02_70\Zedboard_HDL_and_SW\v2_7\sdkWorkspace\zynq1_hw_platform\ps7_init.tcl

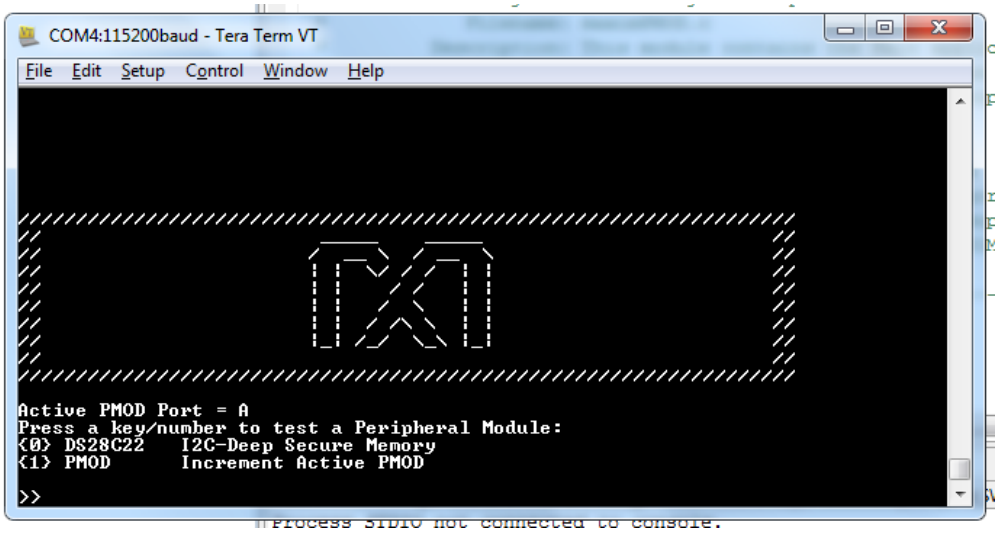
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.

Once both the **maximPMOD.elf** and the ps7_init.tcl files are selected, press **Run**.

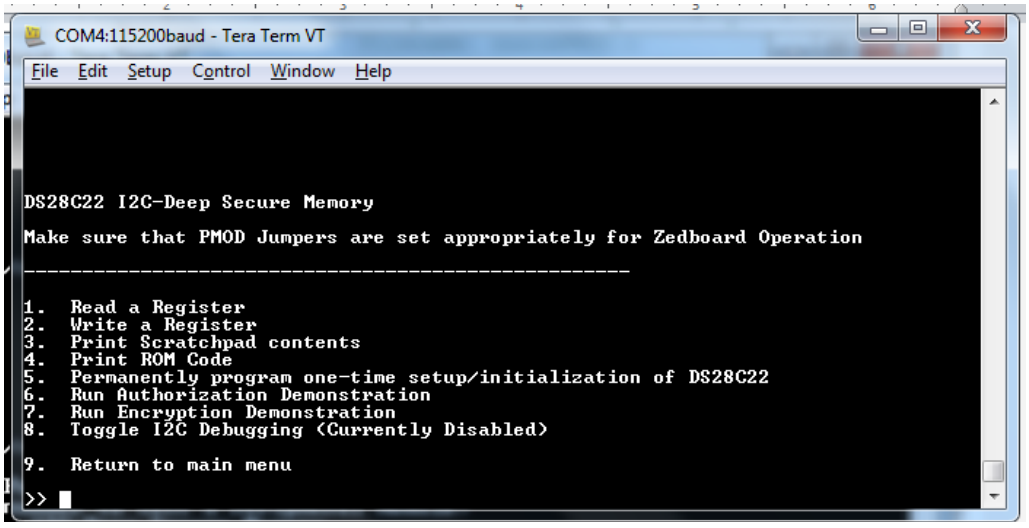
Once the Debug\maximPMOD configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.



At this point, the application is running on the ARM Cortex and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, select **1** to move the active Pmod port to a different connector.

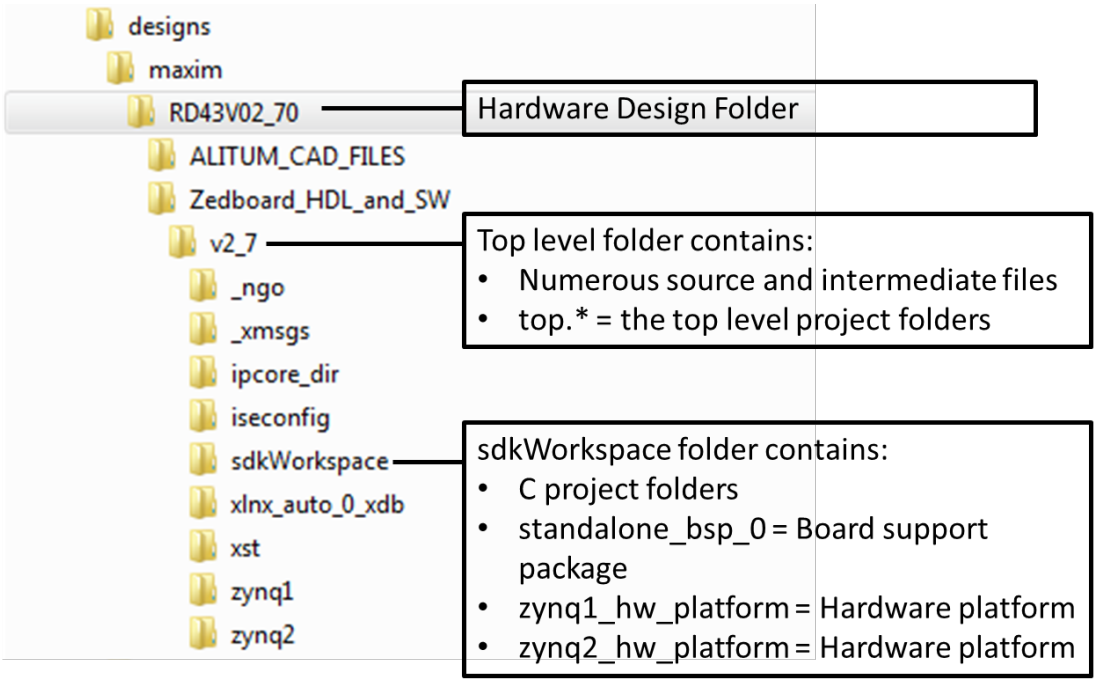


Select **0** to run the MAXREFDES43 demonstration menu, as shown below.



The DS28C22 will not be setup for authentication until running step 5. Once programmed, both the authorization (authentication) and encryption demonstrations will run successfully.

7. Appendix A: Project Structure and Key Filenames



8. Appendix B: Code Snippets of Importants

The ‘C’ code provided in this demo does not include precautions such as placing any authentication code in a TrustZone or bootable area where the code can never change by hacker intervention. See the Xilinx’s UG1019 found here for more details:

www.xilinx.com/support/documentation/user_guides/ug1019-zynq-trustzone.pdf

9. Appendix C: Pre-Install Master Secret into Bitstream

Background: The DS28C22 ZedBoard Reference Design contains a block RAM in the ZC7020 FPGA fabric. It is memory mapped at address 0x82cd0000. It is intended to be used a location to store the master secret for the reference design. This section describes how to merge a new master secret into the design bitstream. **Note:** In your design, it is best to change the memory-mapped address so a hacker will not know the actual location in memory.

Bitstream: The output of the Xilinx ISE tools will generate a bitstream (top.bit) that configures all programmable logic inside the FPGA fabric, including block memories. The default block RAM configuration will have the data at all memory addresses set to zero. This Block RAM can be initialized to any set of values by using a Xilinx command line tool called data2mem to merge an existing bitstream with a text file (test.mem) that contains the desired block memory contents.

Test.mem: The test.mem file alternates memory locations followed by the data for that memory location. An example configuration is shown below. Each line should contain a carriage return, and the file does not contain any headers, footers, or checksums.

```
@82cd0000
3378D863
@82cd0004
0537C88A
@82cd0008
4F57FA55
@82cd000C
98E81450
@82cd0010
AF66F5C5
@82cd0014
20F79E58
@82cd0018
E589FF3A
@82cd001C
758DB5B7
```

Command-line to merge test.mem with top.bit resulting in a new bitstream top_mem.bit:

data2mem -bm edkBmmFile_bd.bmm -bt top.bit -bd test.mem tag processing_system7_0 -o b top_mem.bit

Note that if the Xilinx tools are not included in the command line path, the data2mem.exe and DLLs can be copied to a directory containing the top.bit and test.mem file. These tools are typically found in the Xilinx tools install directory at: C:\Xilinx\14.4\ISE_DS\ISE\bin\nt

The following files are needed :

- Data2mem.exe
- libData2MEMDataUtil.dll
- libData2MEMDesignUtil.dll

When downloading the new bitstream for the design, make sure to use the new top_mem.bit file instead of the old top.bit file.

10. Trademarks

ARM is a registered trademark of ARM, Ltd.
Cortex is a registered trademark of ARM, Ltd.
Eclipse is a trademark of Eclipse Foundation, Inc.
ISE is a registered trademark of Xilinx, Inc.
MicroBlaze is a trademark of Xilinx, Inc.
Pmod is a trademark of Digilent Inc.
Spartan is a registered trademark of Xilinx, Inc.
WebPACK is a trademark of Xilinx, Inc.
Windows is a registered trademark and registered service mark and Windows XP is a registered trademark of Microsoft Corporation.
Xilinx is a registered trademark and registered service mark of Xilinx, Inc.
ZedBoard is a trademark of ZedBoard.org.
Zynq is a registered trademark of Xilinx, Inc.

11. Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/15	Initial release	—

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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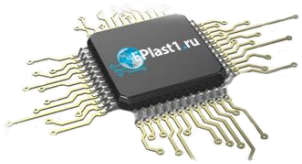
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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