STP100N8F6

N-channel 80 V, 0.008 Ω typ., 100 A, STripFET™ F6 Power MOSFET in a TO-220 package

Datasheet - production data

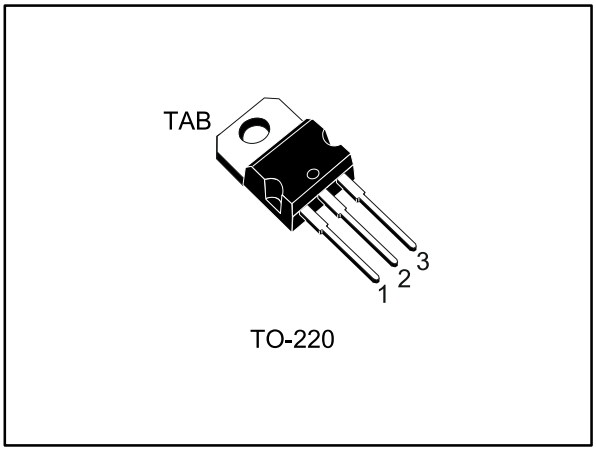
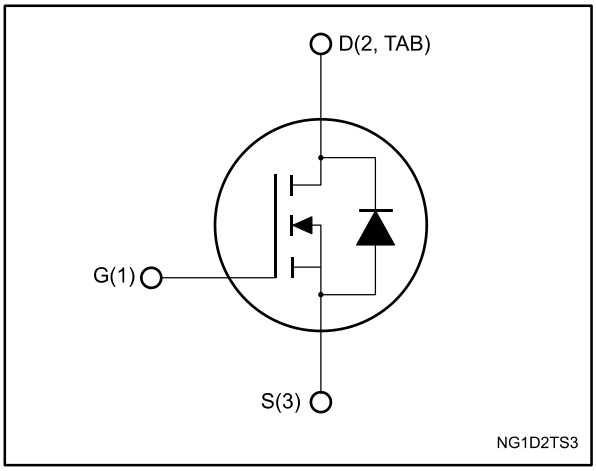


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max.}$	I_D	P_{TOT}
STP100N8F6	80 V	0.009 Ω	100 A	176 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STP100N8F6	100N8F6	TO-220	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	100	A
I_D	Drain current (continuous) at T_C = 100 °C	70	A
I_{DM}(1)	Drain current (pulsed)	400	A
P_{TOT}	Total dissipation at T_C = 25 °C	176	W
E_{AS}(2)	Single pulse avalanche energy	170	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		°C

Notes:

(1)Pulse width is limited by safe operating area.

(2)Starting T_j = 25 °C, I_d = 25 A, V_{dd} = 40 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	0.85	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	80			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0, V_{DS} = 80 V			1	µA
		V_{GS} = 0, V_{DS} = 80 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 50 A		0.008	0.009	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	-	5955	-	pF
C_{oss}	Output capacitance		-	244	-	pF
C_{rss}	Reverse transfer capacitance		-	160	-	pF
Q_g	Total gate charge	V_{DD} = 40 V, I_D = 100 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	100	-	nC
Q_{gs}	Gate-source charge		-	30	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 40 V, I_D = 50 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	33	-	ns
t_r	Rise time		-	46	-	ns
$t_{d(off)}$	Turn-off delay time		-	103	-	ns
t_f	Fall time		-	21	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0, I_{SD} = 100 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 100 A, di/dt = 100 A/µs V_{DD} = 64 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	38		ns
Q_{rr}	Reverse recovery charge		-	63		nC
I_{RRM}	Reverse recovery current		-	3.3		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

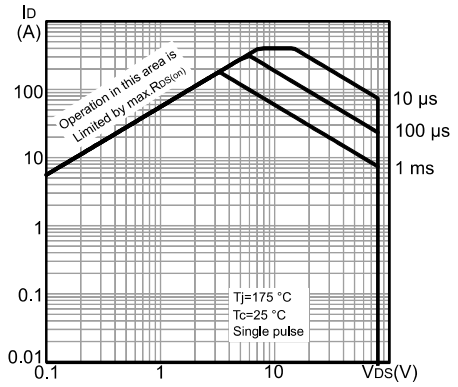


Figure 3: Thermal impedance

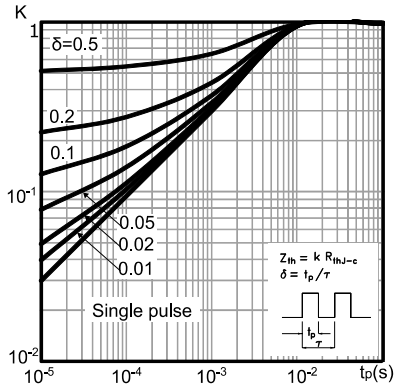


Figure 4: Output characteristics

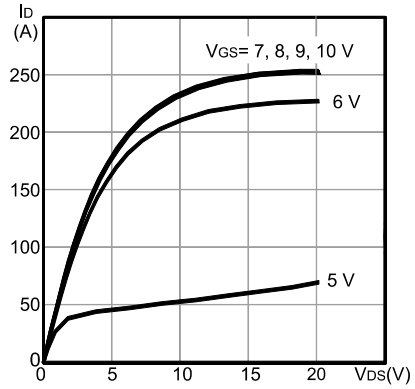


Figure 5: Transfer characteristics

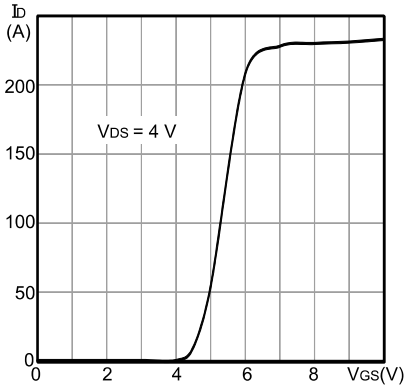


Figure 6: Normalized gate threshold voltage vs. temperature

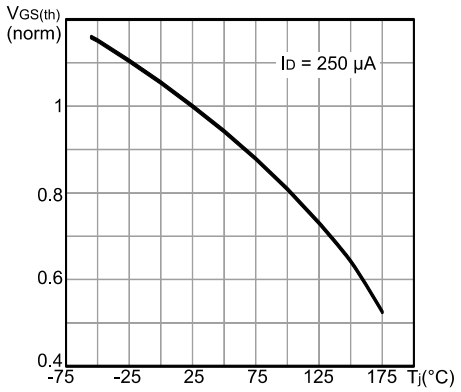


Figure 7: Normalized $V_{(BR)DSS}$ vs. temperature

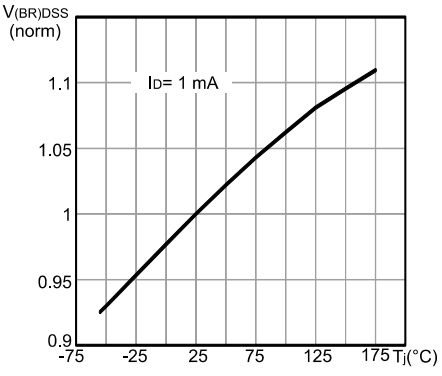


Figure 8: Static drain-source on-resistance

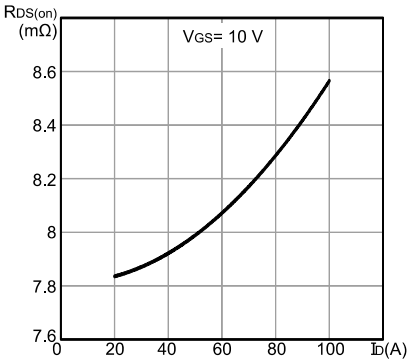


Figure 9: Normalized on-resistance vs. temperature

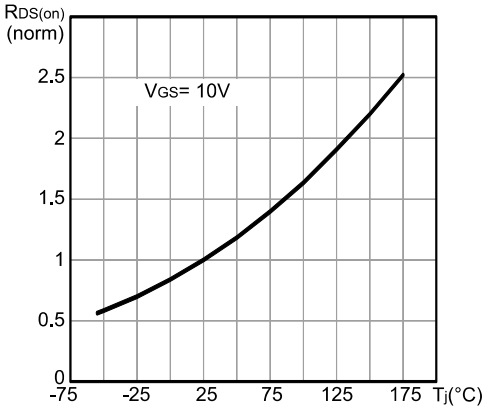


Figure 10: Gate charge vs. gate-source voltage

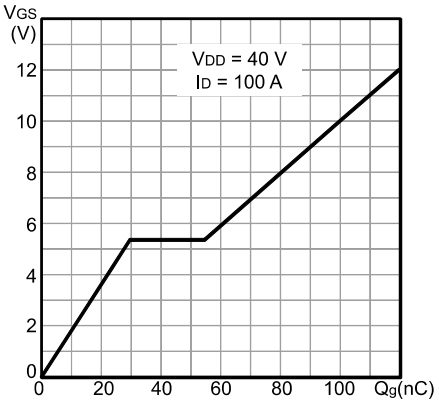


Figure 11: Capacitance variations

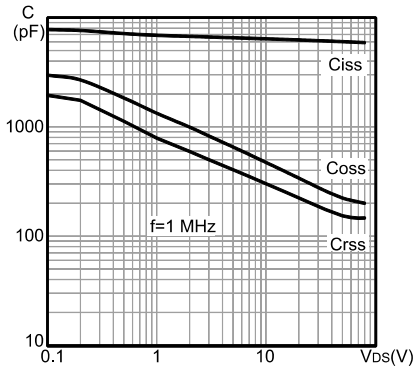
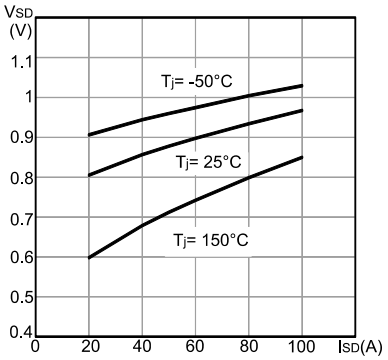


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

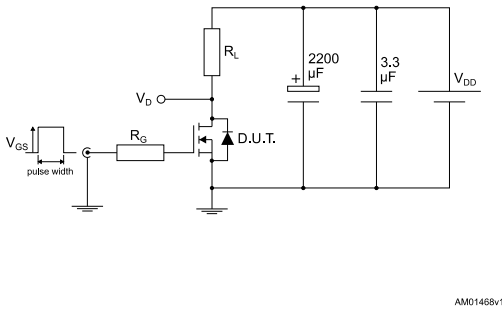


Figure 14: Test circuit for gate charge behavior

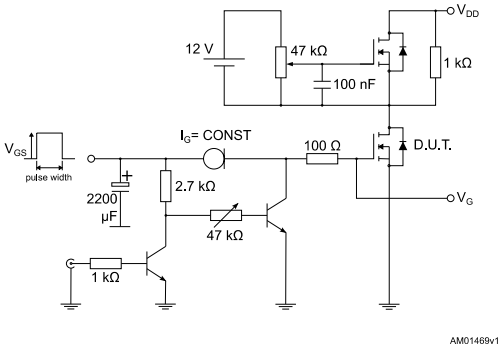


Figure 15: Test circuit for inductive load switching and diode recovery times

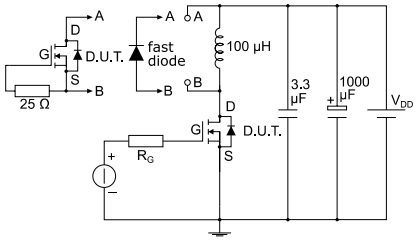


Figure 16: Unclamped inductive load test circuit

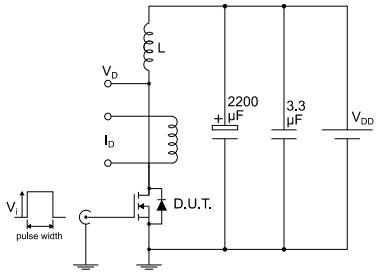


Figure 17: Unclamped inductive waveform

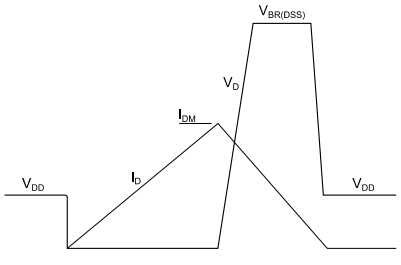
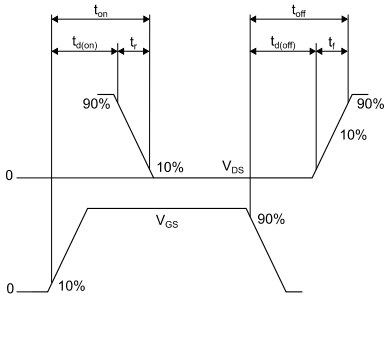


Figure 18: Switching time waveform



4 Package information

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4.1 TO-220 type A package information

Figure 19: TO-220 type A package outline

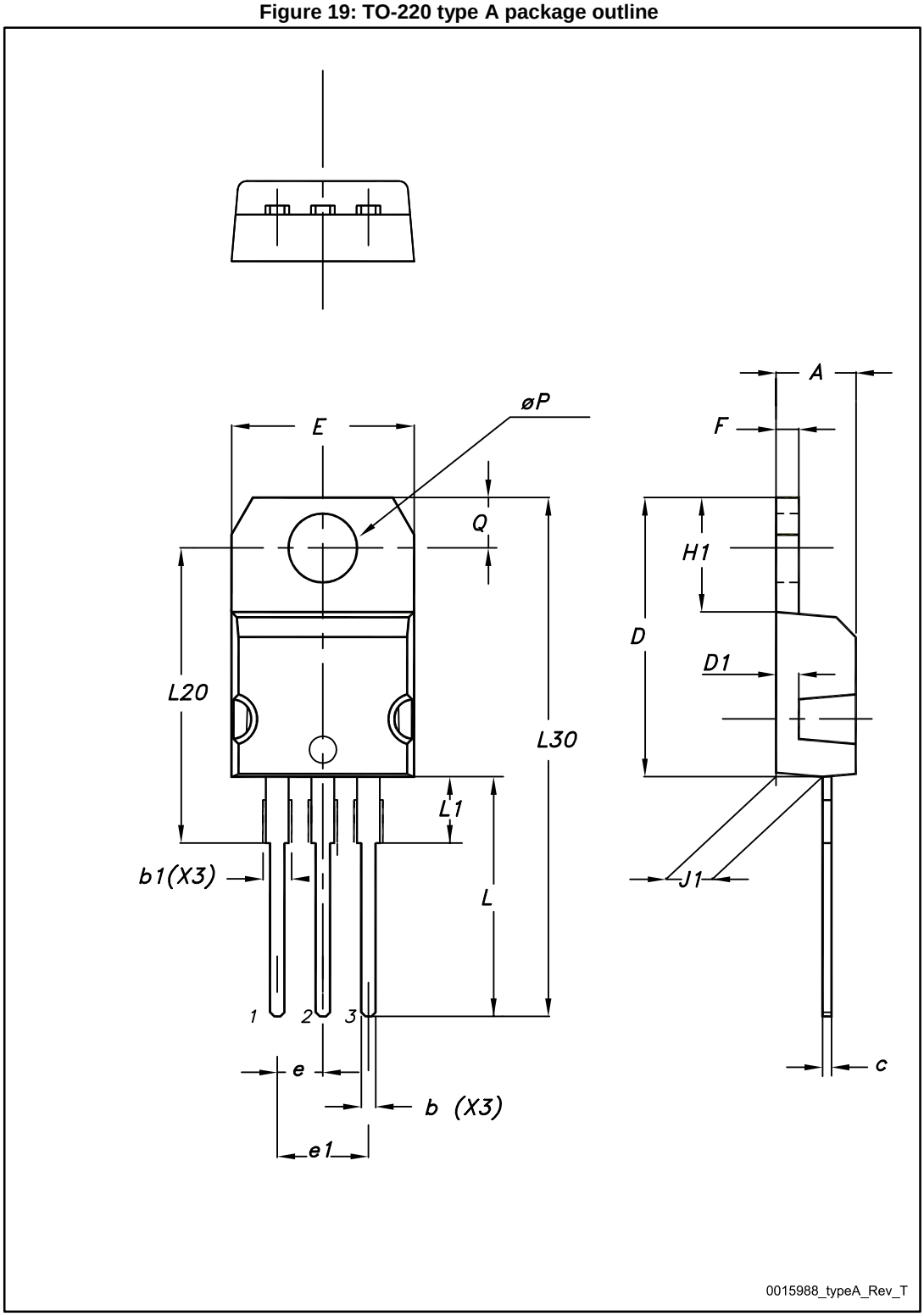

Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 TO-220 type H package information

Figure 20: TO-220 type H package outline

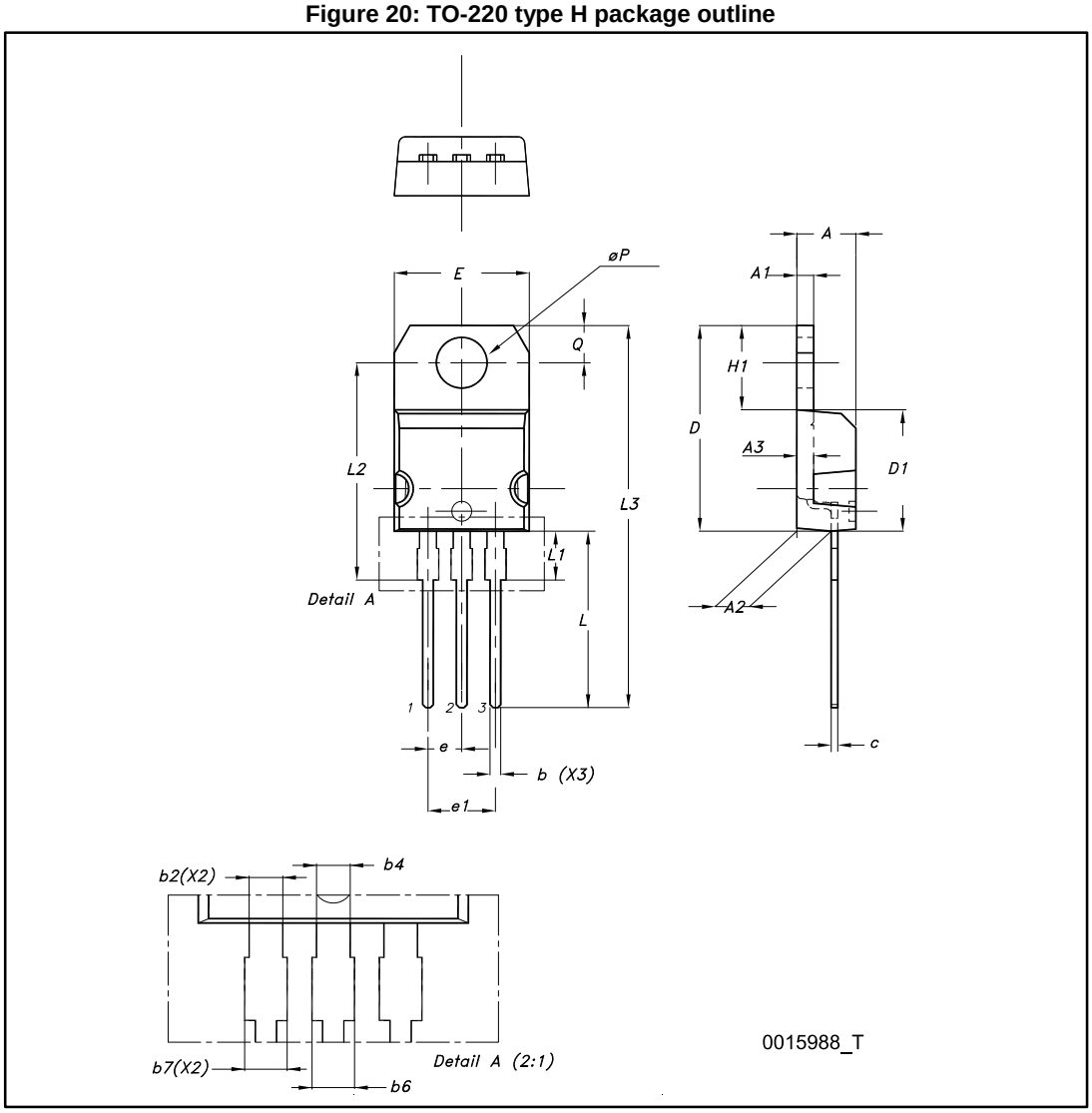

Table 9: TO-220 type H package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	4.45	4.50
A1	1.22		1.32
A2	2.49	2.59	2.69
A3	1.17	1.27	1.37
b	0.78		0.87
b2	1.25		1.34
b4	1.20		1.29
b6			1.50
b7			1.45
c	0.49		0.56
D	15.40	15.50	15.60
D1	9.05	9.15	9.25
E	10.08	10.18	10.28
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
H1	6.25	6.35	6.45
L	13.20	13.40	13.60
L1	3.50	3.70	3.90
L2	16.30	16.40	16.50
L3	28.70	28.90	29.10
ØP	3.75	3.80	3.85
Q	2.70	2.80	2.90

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
02-Sep-2014	1	Initial release.
02-Dec-2014	2	Document status promoted from preliminary to production data. Added the section of electrical characteristics (curves). Minor text changes.
08-Feb-2016	3	Added *Section 4.2: "TO-220 type H package information"*.

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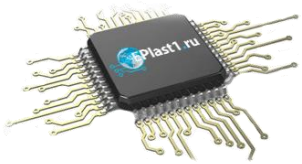
- Защита от снятия компонента с производства.



Как с нами связаться

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