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Kind regards,

Team Nexperia

PBLS4001Y; PBLS4001V

40 V PNP BISS loadswitch

Rev. 03 — 12 February 2009

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in one package.

Table 1. Product overview

Type number	Package	
	NXP	JEITA
PBLS4001Y	SOT363	SC-88
PBLS4001V	SOT666	-

1.2 Features

- Low V_{CEsat} (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
TR1; PNP low V_{CEsat} transistor							
V_{CEO}	collector-emitter voltage	open base	-	-	-40	V	
I_C	collector current		-	-	-500	mA	
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	440	700	$\text{m}\Omega$
TR2; NPN resistor-equipped transistor							
V_{CEO}	collector-emitter voltage	open base	-	-	50	V	

Table 2. Quick reference data ...continued

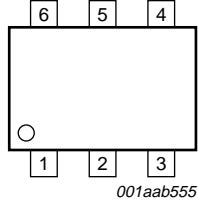
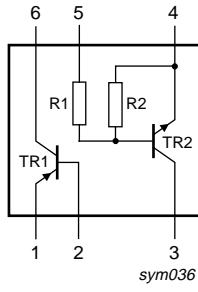
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

[1] Pulse test: $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$.

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package			Version
	Name	Description		
PBLS4001Y	SC-88	plastic surface-mounted package; 6 leads		SOT363
PBLS4001V	-	plastic surface-mounted package; 6 leads		SOT666

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PBLS4001Y	S1*
PBLS4001V	K1

- [1] * = -: made in Hong Kong
 * = p: made in Hong Kong
 * = t: made in Malaysia
 * = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter	-	-40	V	
V_{CEO}	collector-emitter voltage	open base	-	-40	V	
V_{EBO}	emitter-base voltage	open collector	-	-6	V	
I_C	collector current		-	-500	mA	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-1	A	
I_B	base current		-	-50	mA	
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	-	-100	mA	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
TR2; NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter	-	50	V	
V_{CEO}	collector-emitter voltage	open base	-	50	V	
V_{EBO}	emitter-base voltage	open collector	-	10	V	
V_I	input voltage					
	positive		-	+12	V	
	negative		-	-10	V	
I_O	output current		-	100	mA	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	100	mA	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation		-	300	mW	
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-65	+150	°C	
T_{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	-	K/W
	SOT666		[1][2]	-	-	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8. Characteristics $T_{amb} = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
TR1; PNP low V_{CEsat} transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = -40 \text{ V}; I_E = 0 \text{ A}$	-	-	-100	nA	
		$V_{CB} = -40 \text{ V}; I_E = 0 \text{ A}; T_j = 150^\circ\text{C}$	-	-	-50	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$	-	-	-100	nA	
h_{FE}	DC current gain	$V_{CE} = -2 \text{ V}; I_C = -10 \text{ mA}$	200	-	-		
		$V_{CE} = -2 \text{ V}; I_C = -100 \text{ mA}$	[1]	150	-		
		$V_{CE} = -2 \text{ V}; I_C = -500 \text{ mA}$	[1]	40	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$	-	-	-50	mV	
		$I_C = -100 \text{ mA}; I_B = -5 \text{ mA}$	-	-	-130	mV	
		$I_C = -200 \text{ mA}; I_B = -10 \text{ mA}$	-	-	-200	mV	
		$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	-350	mV	
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	440	700	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	-	-1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2 \text{ V}; I_C = -100 \text{ mA}$	[1]	-	-	-1.1	V
f_T	transition frequency	$I_C = -100 \text{ mA}; V_{CE} = -5 \text{ V}; f = 100 \text{ MHz}$	100	300	-	MHz	
C_c	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A}; f = 1 \text{ MHz}$	-	-	10	pF	
TR2; NPN resistor-equipped transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 \text{ A}$	-	-	100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}$	-	-	1	μA	
		$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_j = 150^\circ\text{C}$	-	-	50	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}$	-	-	2	mA	
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 20 \text{ mA}$	30	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_C = 1 \text{ mA}$	-	1.2	0.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_C = 20 \text{ mA}$	2	1.6	-	V	
R_1	bias resistor 1 (input)			1.54	2.2	2.86	k Ω
R_2/R_1	bias resistor ratio			0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A}; f = 1 \text{ MHz}$	-	-	2.5	pF	

[1] Pulse test: $t_p \leq 300 \mu\text{s}; \delta \leq 0.02$.

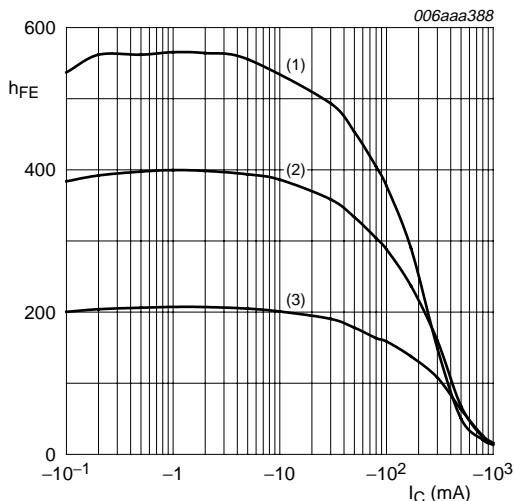


Fig 1. TR1 (PNP): DC current gain as a function of collector current; typical values

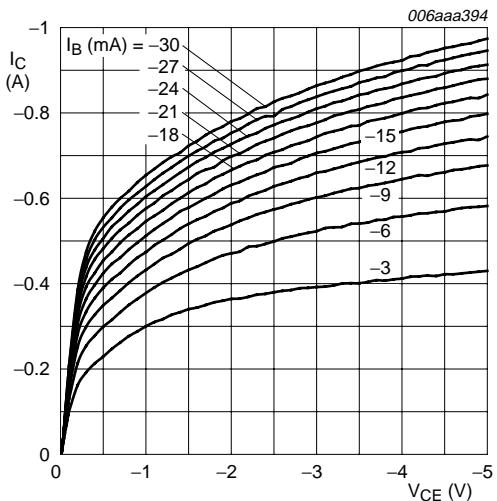


Fig 2. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values

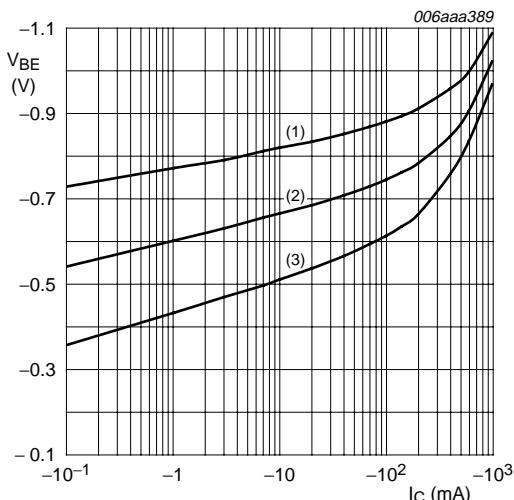


Fig 3. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values

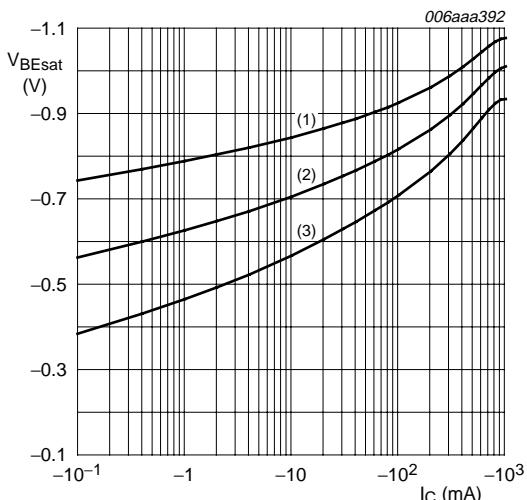


Fig 4. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

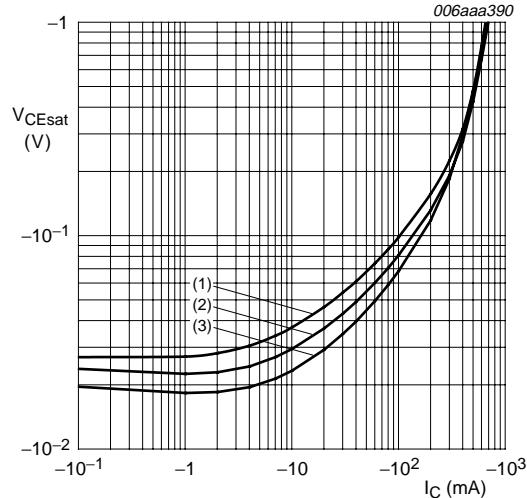


Fig 5. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

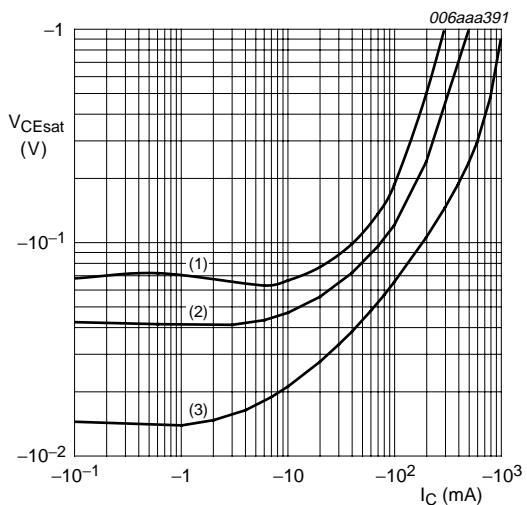


Fig 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

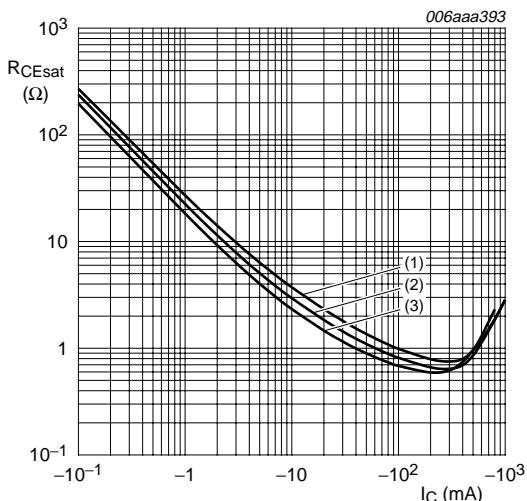


Fig 7. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

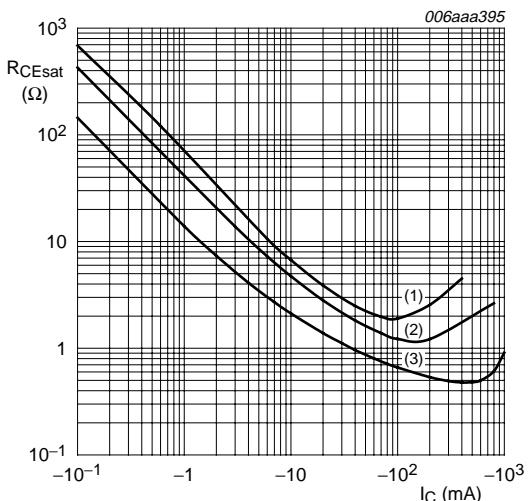


Fig 8. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

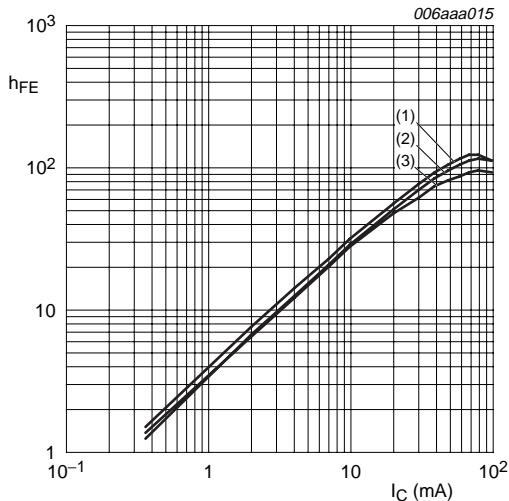


Fig 9. TR2 (NPN): DC current gain as a function of collector current; typical values

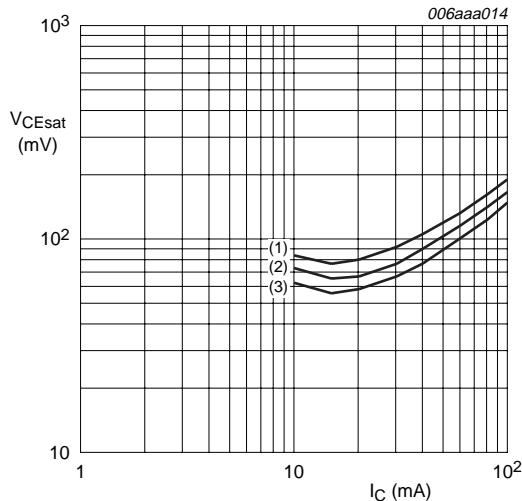


Fig 10. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

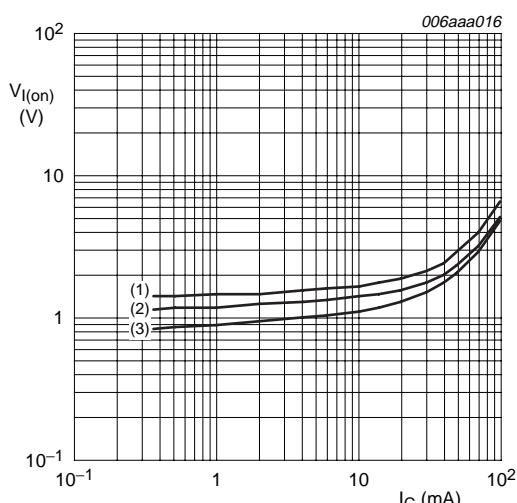


Fig 11. TR2 (NPN): On-state input voltage as a function of collector current; typical values

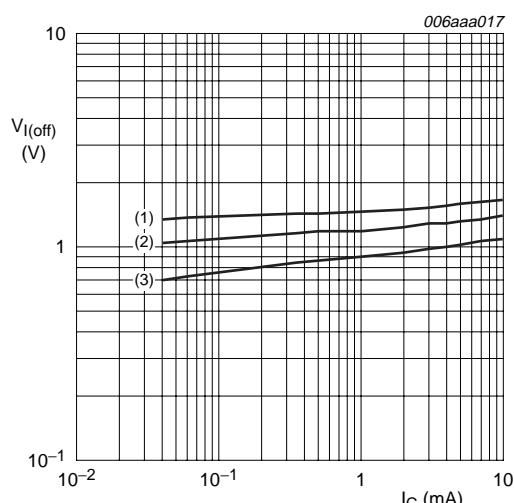
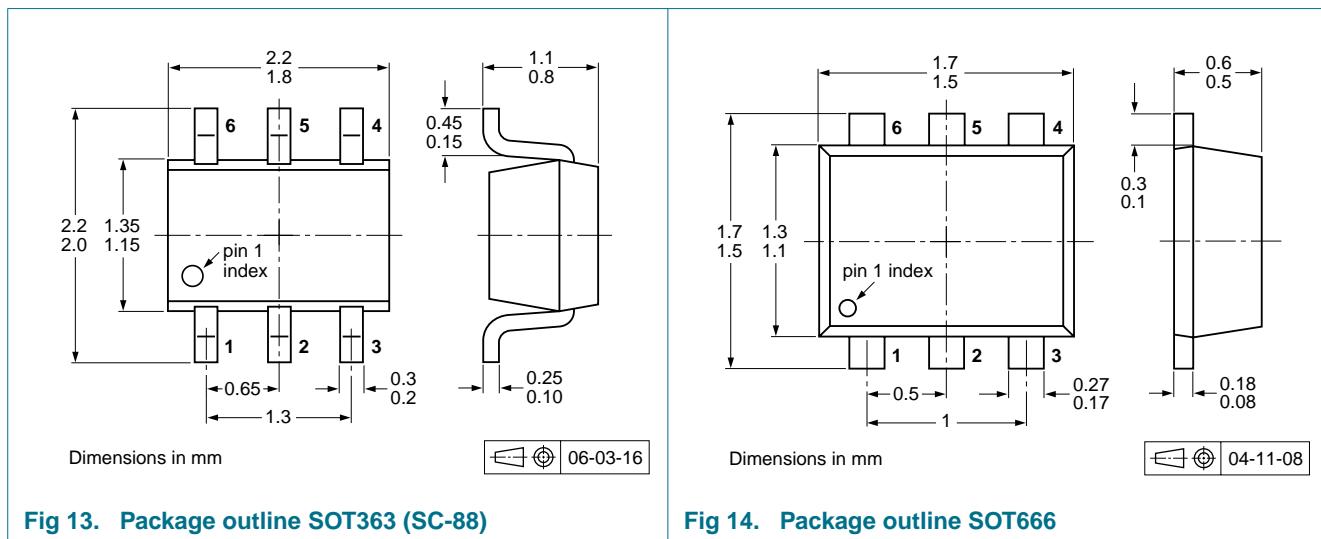


Fig 12. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

8. Package outline



9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PBLS4001Y	SOT363	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-	-
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-	-
PBLS4001V	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-

[1] For further information and the availability of packing methods, see [Section 12](#).

[2] T1: normal taping

[3] T2: reverse taping

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBLS4001Y_PBLS4001V_3	20090212	Product data sheet	-	PBLS4001Y_PBLS4001V_2
Modifications:		<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.Figure 5: y-axis value unit amendedFigure 6: y-axis value unit amendedSection 11 "Legal information": updated		
PBLS4001Y_PBLS4001V_2	20050425	Product data sheet	-	PBLS4001Y_PBLS4001V_1
PBLS4001Y_PBLS4001V_1	20041108	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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