TEA19051BTK

USB-PD 2.0/USB-PD 3.0/QC 2.0/QC 3.0/QC 4 (+) controller for SMPS

Rev. 3 — 21 January 2019 Product data sheet

1 General description

The TEA19051BTK is a highly configurable secondary side SMPS controller that is available in many factory configured versions. Section 15 gives an overview of the off-the-shelf available versions of the TEA19051BTK. To inquire about the possibilities of customer-specific versions, contact your local sales representative.

The TEA19051BTK supports the following protocols:

- USB Type-C v.1.3
- USB power delivery (USB-PD) including programmable power supply (PPS)
- Battery Charging 1.2 (BC1.2)
- Qualcomm® QuickCharge™ QC2.0, QC3.0, and QC4+

A complete smart-charging switch mode power supply (SMPS) can be built in combination with the TEA193x primary controller and the TEA199x secondary side synchronous rectifier (SR) controller.

The TEA19051BTK can be provided in several small packages with low pin count. Due to its small number of external components, a small form factor SMPS can be built that meets efficiency requirements like CoC Tier-2, EuP Iot6, and DOE v6 with an extremely no-load power (< 30 mW).

The TEA19051BTK has a high level of digital integration. It incorporates all required circuits, including a charge pump to drive an external NMOS load switch directly, a USB-PD physical interface (PHY), and an integrated driver for fast output discharge.

The output voltage and output current are continuously measured and are used to control the SMPS. Two GPIO pins measure the adapter temperature and the temperature in the cable/connector. Optionally, the GPIO pins can be used for other features, like supply (see Table 4). The die temperature of the TEA19051BTK is monitored via an internal temperature sensor.

Multiple protections ensure the best-in-class charging safety for the TEA19051BTK.

To ensure correct operation under all conditions, all protections except UVP are implemented in hardware. The response of these protections can be programmed as latched or safe restart. Although not recommended, these protections can also be disabled individually via the settings in the non-volatile multi-time programmable (MTP) memory.

If an output short circuit occurs, the power dissipation in the adapter can be below 50 mW.

For output voltage regulation, current regulation, and protection, only a single optocoupler is required in the application.

The TEA19051BTK operates in CV mode with a better than 2 % voltage accuracy. In CC mode, it operates with a better than 2 % full-load current accuracy.

2 Features and benefits

2.1 General

- Best-in-class fail-safe application for high-power adapters; gives complete protection against overload conditions in the load (e.g. phone)
- Wide output voltage operating range (2.9 V to 21 V)
- Ultra-high efficiency together with TEA193x QR/DCM controller and TEA199x SR controller
- Very low no-load power (< 30 mW for the complete system solution)
- High power density
- Dedicated SW pin to drive external NMOS directly
- Constant voltage (CV) and constant current (CC) control (programmable level)
- Precise voltage and current control with low minimum step size (voltage 12-bit DAC, current 10-bit DAC)
- Continuous measurement of output voltage and output current with a better than 2 % accuracy
- Low-cost HVSON16 package (suitable for reflow soldering)
- Low-cost bill of materials (BOM; ≈15 external components)
- Embedded MCU (with ROM, RAM, and MTP memory)
- Discharge pin for fast output voltage ramp down
- Built-in series regulator and programmable cable compensation
- Non-volatile MTP memory for storage of system configuration parameters

2.2 Protocol support

- USB Type-C v.1.3
- USB power delivery (USB-PD) 2.0 and 3.0 including programmable power supply (PPS)
- Qualcomm® QuickCharge™ QC2.0, QC3.0, and QC4+ protocols
- Battery Charging 1.2 (BC 1.2)
- Unstructured vendor defined messages (VDMs), which can be used for MTP programming, e.g. to get Vendor IDs

2.3 Protections

- Overtemperature protection (OTP): one internal and two external
- Adaptive overvoltage protection (OVP)
- Adaptive undervoltage protection (UVP)
- Overcurrent protection (OCP)
- Undervoltage lockout (UVLO) protection
- Output short protection (OSP)
- Open-supply protection (OSUP)
- Open-ground protection (OGP)
- Overvoltage protection DP, DM, CC1, and CC2 pins
- Soft short protection at the CC1 and CC2 pins
- Soft short protection at the output

To ensure safe operation, the TEA19051BTK switches off the load during fault conditions.

3 Applications

- USB chargers for smart phones and tablets supporting the Qualcomm® QuickCharge™ QC2.0, QC3.0, and QC4+ protocols
- USB-PD 3.0, type C 1.3 chargers with optional VDM support for smartphones and tablets

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA19051BAATK/1	HVSON16	plastic small enhanced very thin small outline package; no leads; 16 terminals; body: 3.5 × 5.5 × 0.85 mm	SOT1308-1
TEA19051BABTK/1			
TEA19051BACTK/1			
TEA19051BAFTK/1			
TEA19051BAGTK/1			
TEA19051BAHTK/1			
TEA19051BAKTK/1			
TEA19051BAMTK/1			
TEA19051BAPTK/1			
TEA19051BARTK/1			

5 Marking

Table 2. Marking

Type number	Marking code
TEA19051BAATK	A19051BAA
TEA19051BABTK	A19051BAB
TEA19051BACTK	A19051BAC
TEA19051BAFTK	A19051BAF
TEA19051BAGTK	A19051BAG
TEA19051BAHTK	A19051BAH
TEA19051BAKTK	A19051BAK
TEA19051BAMTK	A19051BAM
TEA19051BAPTK	A19051BAP
TEA19051BARTK	A19051BAR

6 Block diagram

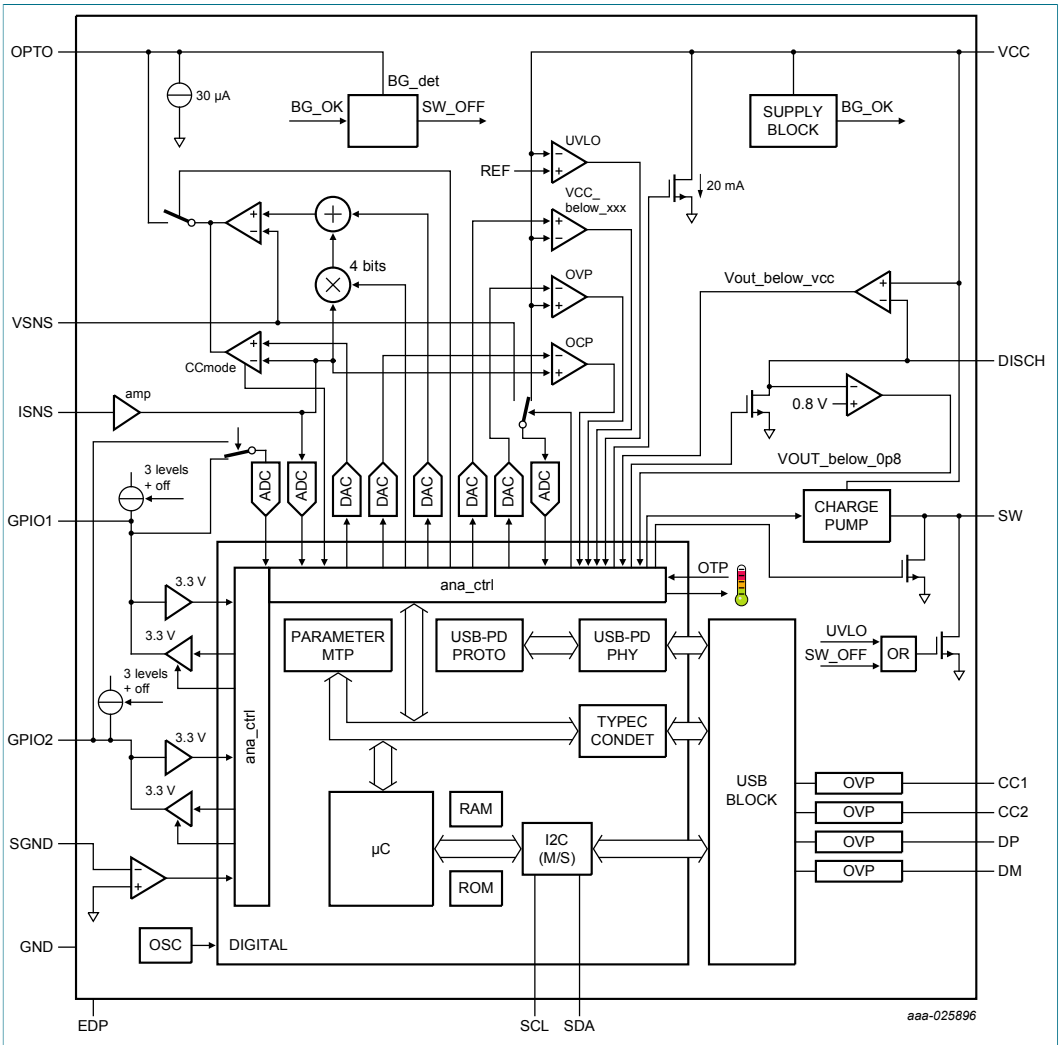


Figure 1. TEA19051BTK block diagram

7 Pinning information

7.1 Pinning

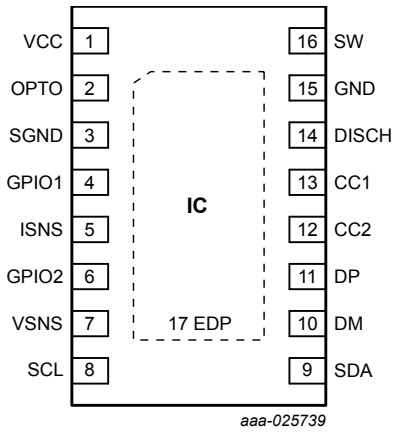


Figure 2. TEA19051BTK pinning diagram (SOT1308-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
OPTO	2	OPTO driver
SGND	3	sense ground
GPIO1	4	general-purpose input/output
ISNS	5	current sense input
GPIO2	6	general-purpose input/output
VSNS	7	voltage sense input
SCL	8	I^2C clock line
SDA	9	I^2C data line
DM	10	negative terminal of the data communication line
DP	11	positive terminal of the data communication line
CC2	12	type C CC2 line detection and USB-PD communication
CC1	13	type C CC1 line detection and USB-PD communication
DISCH	14	fast discharge sink
GND	15	ground
SW	16	NMOS gate drive output
EDP	17	exposed die pad

8 Functional description

The TEA19051BTK can be considered as a versatile programmable replacement for the well-known TL431 shunt regulator series, where:

- The VSNS pin takes the role of the REF input of the TL431
- The OPTO pin takes the role of the cathode
- The GND pin takes the role of the anode

In addition to the constant voltage (CV) mode, which is regulated via the VSNS pin, the system supports constant current (CC) mode. The current control loop is regulated and the cable compensation is added via the ISNS pin.

Alternatively, the ISNS input can be used for overcurrent protection (OCP; see Table 4). Several other protections are available. Many of these protections are programmable as latched or safe restart. For guaranteed safety, all protections are implemented in hardware. So, even when the microcontroller stops, the protections are still functional.

The output voltage and the output current can be controlled via USB-PD using the CC pins. They can also be controlled via QC using the DP and DM pins.

The output current and the output voltage are continuously measured via an integrated AD-converter. The values can be made available continuously via the USB-PD protocol. The applied time constant of the digital filter is initialized via the firmware. A dedicated signal that indicates a stable output voltage/output current for a reliable measurement is available. It can be used, for example, to determine and monitor the cable resistance in the portable device.

The external temperatures, measured via the GPIO1 and GPIO2 pins, are continuously monitored. From the GPIO voltages and applied currents, the controller calculates the corresponding temperatures. These temperatures can be communicated to the portable device. Optionally, an OTP function is added to this external temperature measurement, which is programmable via MTP (see Table 4).

The available protections are implemented in hardware. They are independent of processor actions. These protections in combination with the NMOS load switch ensure a fully safe operation with only one optocoupler. When the optocoupler fails, the OVP of the primary side controller (TEA1936x) limits the maximum output voltage.

The TEA19051BTK fully supports the type-C connector standard.

When a Type C receptacle is used, the CC1/CC2 pair is used for plug attach/detach detection. It is also meant to support the USB-PD communication standard. The DP/DM pair is meant to support:

- Battery Charging 1.2
- Qualcomm® QuickCharge™ QC2.0 and QC3.0

The USB-PD specification requires the use of a load switch and certain discharge behavior of the output voltage at the connector V_{bus}. So, to drive the gate of an external NMOS switch, the TEA19051BTK is equipped with an SW pin. To be able to discharge V_{bus} using an external resistor in series with an internal switch, the TEA19051BTK is equipped with a DISCH pin.

User-defined parameters can be stored in the non-volatile multi-time programmable (MTP) memory.

8.1 Start-up and supply

The TEA19051BTK is supplied via the VCC pin connected to the secondary DC voltage of an AC-to-DC SMPS converter (see Figure 7). To control the primary side controller, this VCC voltage is regulated via an integrated voltage/current control loop with external loop compensation and an external optocoupler. This optocoupler is part of the gain loop of the primary side SMPS controller.

At each start-up and after power-on reset, the optocoupler current is initially zero. So, the AC-to-DC converter starts up with full output power, resulting in a rapid increase of the VCC voltage. Due to the low $V_{CC(start)}$ level (≈3 V), the TEA19051BTK ensures that it is fully operating before the V_{CC} reaches the default initial regulation level. The default values of the initial regulation level are 5 V and 3 A and they are programmed in the non-volatile memory (MTP).

At power-on reset, the safe default values, which are read from MTP, are set.

When the V_{CC} voltage is below the UVLO level, the external NMOS load switch is off. When the output is shorted while the load switch is closed, the UVLO is also triggered. The load switch is then immediately opened and the system restarts after the safe restart timer.

When the V_{CC} exceeds the UVLO level, all circuits, the initial DAC value, and the resistive divider ratio are initialized. The system regulates the output to 5 V with a limited output current of 3 A. All these values can be set via the MTP.

To minimize the output voltage overshoot after start-up, an internal 20 mA current sink is applied to VCC when the VCC voltage exceeds 1.05 × $V_{o(default)}$. The sink current remains active until the VCC voltage has dropped to below 1.05 × $V_{o(default)}$ again.

After the output voltage has stabilized, the load switch becomes conducting and the system waits for an attach. Before the attach, only the essential circuits are working which reduces the no-load power to its minimum.

When the voltage on one of the CC pins drops to below the $V_{IH(Rd)}$ level, an attach is detected and all circuits are enabled.

If a protocol is detected, it is allowed to change the voltage and current.

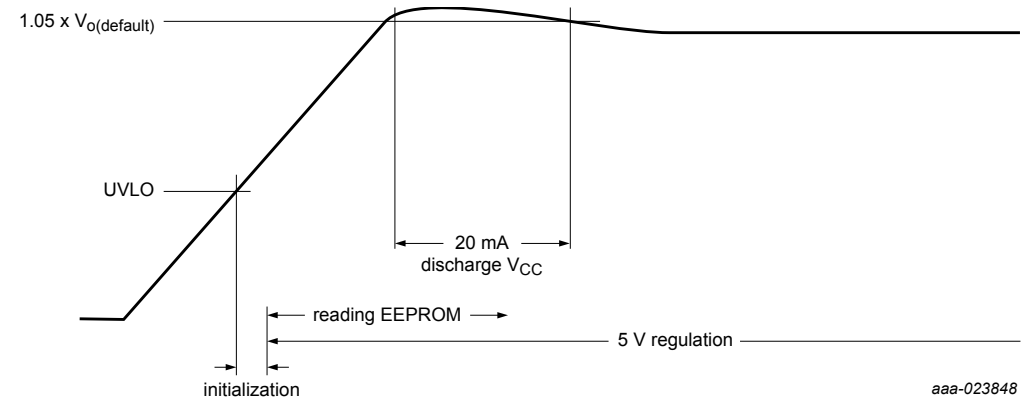


Figure 3. Start-up sequence

The TEA19051BTK operates on supply voltages up to 21 V. The voltage on the VCC pin is used to detect an OVP and UVP. The OVP and UVP level are set as a percentage of the requested output voltage level.

If the supply voltage drops to below the UVLO level, the system returns to the no-supply state and opens the load switch. Analog circuits are reset below UVLO. The internal digital circuits are reset below the band gap voltage reference level.

8.2 Voltage loop

The analog constant voltage (CV) loop regulates VCC such that the voltage on the VSNS pin equals the internal reference voltage. An external resistor divider is connected between VCC, the VSNS pin, and ground. The value of this divider must match the value that is programmed in MTP exactly. It depends on the maximum voltage in the application. The divider values are:

- 1/ 2.5; maximum PDO voltage ≤ 6 V
- 1/5.476; maximum PDO voltage ≤ 13 V
- 1/8.325; maximum PDO voltage ≤ 20 V
- 1/8.828; maximum PDO voltage ≤ 21 V

The CV loop is regulated by varying the current through an optocoupler diode similar to a TL431 driven control loop commonly used in switch mode power supplies. The RC combination between the OPTO and VSNS pin determines the dynamic behavior of the integrating part of the control loop. The resistor in series with the optocoupler diode determines the dynamic behavior of the proportional part of the control loop. To prevent saturation of the control loop during switching, a diode is placed in parallel to this resistor. See Section 13.3 for more information about the control loop.

When the voltage loop reference is set to a higher value using the USB-PD or the QC protocol, the internal reference voltage is updated to the new setting within 20 µs. The output voltage is regulated to the requested voltage with a speed determined by the control loop. If there is a transition down, a predefined ramp down sequence is followed to prevent a high undershoot. Depending on the step size, the ramp down either follows a linear or a parabolic slope. For a transition up, no special measures are required to prevent an overshoot. The reason is that the charging current of the loop capacitor lifts the voltage on the VSNS pin when the V_{CC} voltage in the application increases.

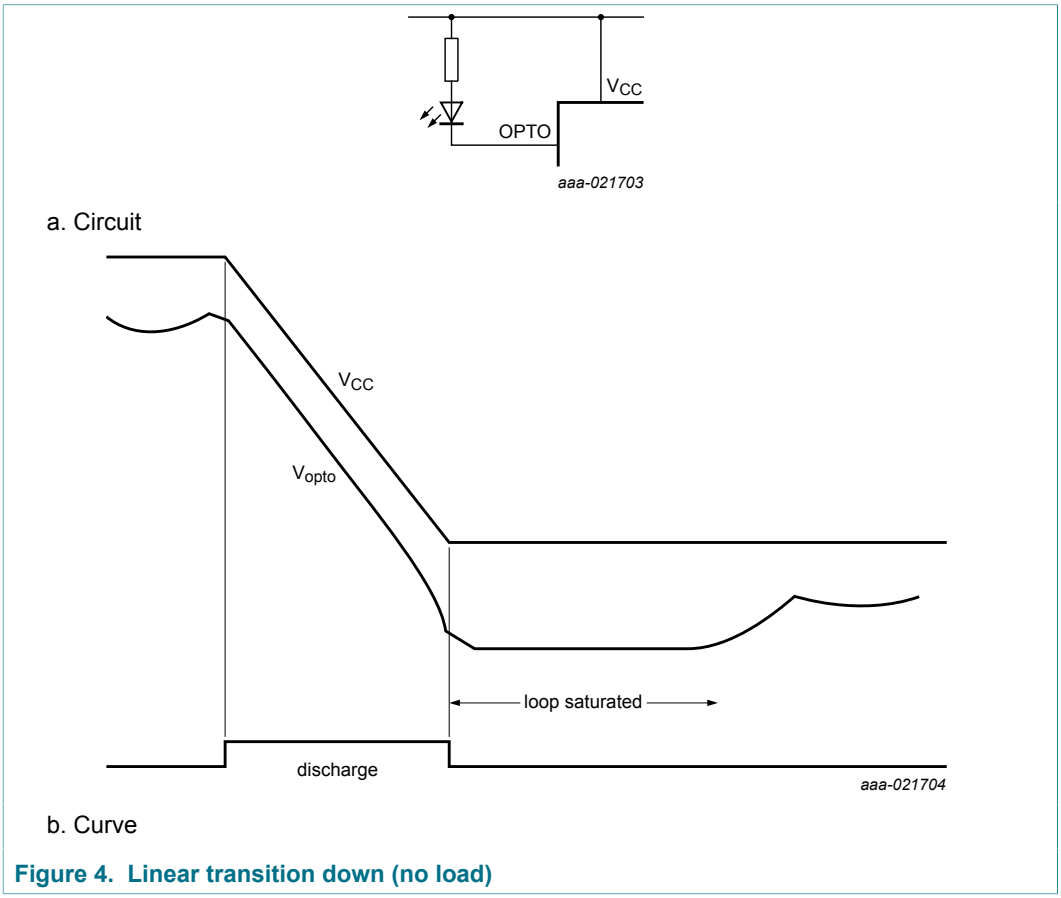
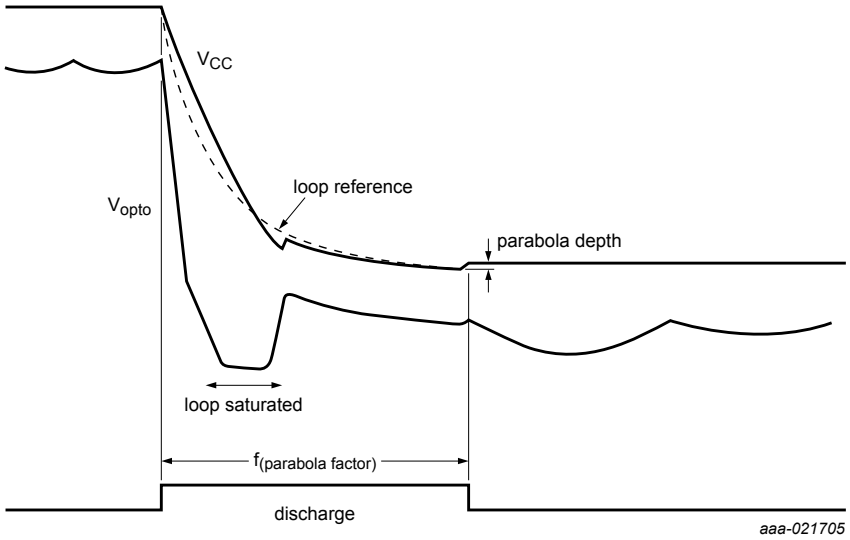


Figure 4. Linear transition down (no load)

A linear ramp-down (see Figure 4) can yield a perfect linear ramp of the output voltage without any undershoot. However, depending on the loop bandwidth, the voltage loop can end up in saturation. Saturation hampers a fast response to a load step immediately following the end of the ramp (most protocols do not allow any load to be drawn during a transition). Making the ramp down slower can prevent saturation of the loop. However, a slower ramp down can contradict with the maximum discharge time most protocols specify.

A parabolic discharge curve (see Figure 5; patent pending) initially causes the voltage loop to saturate, due to the initial rapid ramp down. However, it allows the loop to recover and to resume regulation toward the end of the curve. The total parabolic sequence time must be chosen such that no undershoot under the final end value occurs.

a. Circuit



b. Curve

Figure 5. Parabolic transition down (no-load)

8.3 Current loop

The voltage drop across a small external series resistor between the output return terminal and the converter ground is supplied to the ISNS pin. An internal amplifier multiplies the voltage on the ISNS pin by a factor of 50. The output voltage of the amplifier must remain below 2.5 V. The external resistor value can be chosen from 2 mΩ up to 22.5 mΩ in steps of 0.02 mΩ. The external resistor value must correspond to the programmed value in MTP. Any deviation from this MTP value, e.g. due to PCB-layout imperfections, causes a current error and must be corrected (see Section 13.2). The ground connection of the external sense resistor must be connected to the SGND pin via an independent sense wire.

The combination of the maximum current in the application, the sense resistor, and the gain of the internal amplifier must be chosen such that the output voltage of the internal amplifier remains below 2.5 V.

When the application is used in CC-mode, an RC-combination must be connected between the OPTO pin and the ISNS pin (see Section 13.4).

8.4 Cable compensation

With cable compensation enabled, the output voltage is increased when the output current increases to compensate for the voltage drop over the cable. The value of the cable compensation is the same for all PDOs. It is set in MTP between the minimum and maximum values (see Table 4).

Setting the cable compensation above 200 mV/A is not recommendable. The cable compensation can be enabled/disabled for each individual PDO.

8.5 Load switch

A low-cost NMOS transistor is used as load switch between V_{CC} and V_{bus} (see Figure 7). A dedicated switch-drive output pin (SW pin) controls this NMOS transistor. The output (high) level of the switch drive output is V_{CC} + 6 V using an internal charge pump.

As long as V_{CC} is below the UVLO level or if the VCC connection is open, the SW pin is held low, ensuring that the load switch is off. To ensure that the NMOS is also kept off when the SW pin is disconnected, an external (high-ohmic) resistor is required between the gate of the NMOS and V_{bus}.

To avoid charging V_{CC} via the back-gate diode of the load switch, it is possible to apply two NMOS switches in series, with their sources connected together.

8.6 Discharge function

The DISCH pin, which has an internal low-ohmic switch, provides the means to discharge the output V_{bus} quickly. An external series resistor limits the maximum current and the IC dissipation.

To check if the output voltage has dropped to below 0.8 V, a comparator is implemented. This voltage drop is a requirement of the USB-PD specification (vSafe0V) if there is a hard reset.

When the internal DISCH switch is activated, the voltage at the DISCH pin is always low, because of the external current limiting resistor. A mechanism has been implemented to check the real output voltage. During a hard reset discharge sequence, when V_{CC} is below vSafe5V, the switch is opened every millisecond for 20 µs to check the output voltage at the end of the 20 µs period. The check of the output voltage is done until the voltage remains below 0.7 V and the hard reset discharge sequence is terminated. For this check to work properly, the capacitance on the DISCH pin and the external current limiting resistor must have a time constant that is short enough.

To ensure that the output remains low, a 1 mA sink current is present on the DISCH pin when both the load switch and discharge switch are off. The period that the DISCH pin is active in unattached state ($t_{d(act)}$) is typically 100 ms. The reason for this limitation is to prevent that excessive power dissipation occurs if an external V_{bus} voltage is applied.

8.7 Detach detection

When the voltage on one of the CC pins is greater than 1.2 V, a detach is detected. If the type C cable is disconnected, the output voltage is regulated to its default value (5 V) after 200 µs.

8.8 Internal temperature measurement

The internal die temperature is monitored continuously. Its value can be requested with the appropriate vendor defined message (VDM). When the internal OTP (see Table 5) is enabled, the internal OTP is triggered when the die temperature exceeds the value that is programmed in MTP.

8.9 GPIO pins

The internal hardware of the GPIO1 and GPIO2 pins is identical.

In the MTP, the following functions can be selected for each GPIO pin:

- Off
- NTC
- NTC + OTP
- Supply

In the sections below, the functions are further explained.

8.9.1 Off

The GPIO pin is disabled and can be connected to ground.

8.9.2 NTC

With the NTC function enabled, the GPIO pins can be used to measure the adapter and cable connector temperature via NTC resistors. The NTC connected to GPIO1 is meant for measuring the (cable) connector temperature. The NTC connected to GPIO2 for measuring the adapter temperature. The temperature values can be requested with the appropriate VDM command. To ensure an accurate temperature measurement over the complete temperature range, both external NTCs are supplied via an adaptive current source (see Figure 6).

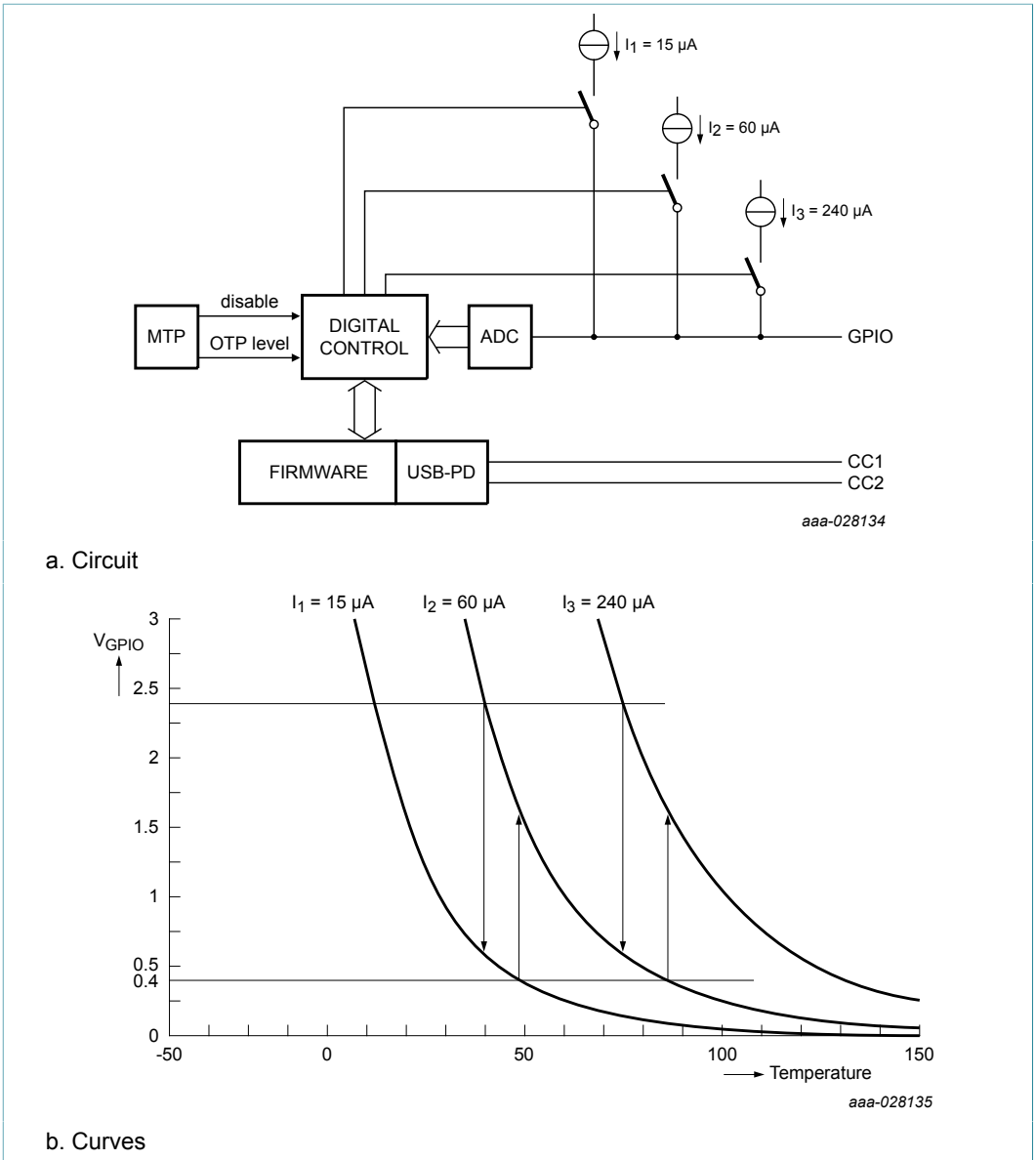


Figure 6. External NTC is supplied via adaptive current sources

The voltage at a GPIO pin is measured via an internal A-to-D converter. If the voltage on the GPIO pin drops to below 400 mV, the source current is increased. If the voltage on the GPIO pin exceeds 2.4 V, the source current is decreased. When a 47 kΩ NTC resistor with a Beta of 4108 is used, the temperature is accurately measured with a better than < 5 °C accuracy within a range of 0 °C to > 120 °C.

8.9.3 NTC + OTP

With this function enabled, an OTP function is added to the NTC function. The OTP function is integrated in hardware. The OTP level is set in MTP.

When the NTC (+ OTP) function is enabled for a GPIO pin, but this GPIO pin is not used in the application, it must be connected to ground via a fixed 47 kΩ resistor. Do not leave the unused pin floating or connect it to ground.

8.9.4 Supply

When the supply functionality is chosen for the GPIO pin in MTP, the output of the GPIO can be used to supply, e.g., an EEPROM. The following modes can be chosen via MTP:

- The supply signal is high continuously
- Dynamic switching of the I^2C slave supply on the GPIO pin.
  When the master activates I^2C communication, the supply is turned on first. After a delay, the I^2C communications start. When I^2C communications stops for 1 s, the supply is turned off.
- The signal on the GPIO can have inverted behavior

8.10 Communication

If a type-C receptacle is used, attach/detach detection and USB-PD communication is provided on the CC pins.

DP and DM provide the communication interface for QC2.0 and QC3.0.

If a type-A receptacle is used, attach/detach detection can be disabled (via MTP). The load switch is closed (when no protection is triggered).

8.10.1 USB Type-C

The TEA19051BTK complies with the USB Type-C 1.3 specification (see Ref. 2) in the sense that the distinct pull-up current values support attach/detach and current capability advertising. The attach/detach detection is done in the hardware. So, if there is a detach, a return of V_{bus} to vSafe5V is always ensured. The hardware implementation of the return of V_{bus} to vSafe5V eliminates the risk of software implementations where V_{bus} may stay at an unsafe level if the program execution stalls.

To support currents higher than 3 A, use a captive cable. V_{conn} is not supported.

8.10.2 USB-PD

The TEA19051BTK supports the USB-PD, release 3.0 specification (see Ref. 4) as far as it is required for a DFP.

The TEA19051BTK supports the programmable power supply (PPS) part of the USB-PD 3.0 specification.

The TEA19051BTK can be programmed such that it only complies with the USB-PD 2.0 specification. With these MTP settings, power-brick USB-PD-2.0 testing can be done and USB-PD 2.0 qualification is possible.

Maximum seven different power data objects (PDO) can be defined in the non-volatile memory (MTP). Released types have a predefined set of PDOs programmed (see Table 4). For each PDO, current limit type (OCP/CC) and cable compensation on/off can be set. However, any other voltage or current within the range can be defined in a PDO.

Four of the seven PDOs can be set as programmable power supply (PPS) instead of a Fixed Power Supply via MTP.

The TEA19051BTK supports the QC4+ VDMs.

To make USB-PD certification possible, QC2.0 and QC3.0 must be disabled. Disabling QC2.0 and QC3.0 can be done in MTP or by not connecting the TEA19051BTK DP and DM pins. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

8.10.3 Discover identification

The TEA19051BTK supports the discover identification protocol in USB-PD. It is possible to program VID, PID, and BCD values in MTP. These values can be requested via VDM messages.

The maximum power, which is used to determine the power profile, can be set in MTP.

8.10.4 Battery charging

The standard battery charging protocol is supported according to the BC1.2 specification (see Ref. 1).

8.10.5 Quick charge

The Qualcomm® QuickCharge™ QC2.0, QC3.0, and QC4+ protocols are fully supported (see Ref. 5, Ref. 6, and Ref. 7). The required fixed and PPS PDOs can be configured in MTP. The fixed PDO settings that are used for QC2.0 can be set via MTP.

When QC 3.0 is used, the voltage can be set via this protocol from 3.6 V to 12 V in steps of 200 mV. The maximum voltage can be limited if wanted via MTP settings.

8.10.6 MTP configuration

The TEA19051BTK is configurable via MTP. The different types are defined in Section 15. Table 4 gives an overview of the programmability with their minimum/ maximum values.

Table 4. MTP configuration options

Function	Options	minimum level	maximum level	step size
default output voltage	-	3 V	10 V	50 mV
default maximum output current	-	0.3 A	5 A	20 mA
GPIO1	disable; NTC; NTC with OTP[1]; Supply	-	-	-
GPIO1 protection level	-	62 °C	111 °C	variable but < 5 °C
GPIO2	disable; NTC; NTC with OTP[1]; Supply	-	-	-
GPIO2 protection level	-	62 °C	111 °C	variable but < 5 °C
OTP internal	-	27 °C	135 °C	4.3 °C
external sense resistor(R_{sns})	-	2 mΩ	22 mΩ	0.02 mΩ
external resistor divider VCC/ VSNS (=DIV)[2]	8.325; 2.5; 5.476; 8.828	-	-	-
cable compensation[3]	-	0 mV/A	R_{sns} * DIV * 8 V/A	variable
CC mode or OCP mode	OCP-mode/CC-mode	-	-	-
PDO1	5 V 3 A	-	-	-
PDO2; PDO3; PDO4; PDO5; PDO6; PDO7	- -	3 V 0.3 A	20 V 10 A	0.05 V 0.01 A
OVP level (PDO)[4]	120 %; 125 %; 130 %	-	-	-
UVP level (PDO)[4]	off; 60 %; 70 %; 80 %	-	-	-
UVP level (APDO)[4]	off; 70 %; 80 %; 90 %	-	-	-
PDO QC enable[4]	TRUE/FALSE	-	-	-
PDO PPS enable[5]	TRUE/FALSE	-	-	-
QC3.0 cable compensation enable	TRUE/FALSE	-	-	-
QC3.0 maximum power	-	0 W	102.3 W	0.1 W
USB3.0 enable	TRUE/FALSE	-	-	-
power limit PPS	TRUE/FALSE	-	-	-
minimum voltage APDO	-	3.3 V	20 V	-

[1] The NTC readout and OTP levels are defined with an NTC of 47 kΩ and a B-constant of 4108.
[2] Maximum output voltage for 5.476 is 13 V. Maximum output voltage for 2.5 V is 6 V.
[3] Cable compensation above 200 mV/A is not recommended.
[4] Can be selected for each PDO individually.
[5] Maximum 4 PDOs can be an APDO.

8.11 Protections

Table 5 gives an overview of the available protections. All protections except the OGP operate in safe restart mode. All protections except UVP are implemented in hardware. When a fault condition occurs, the load switch is immediately opened. When the fault condition is removed, the load switch is closed again. The VCC is set to default and the minimum delay defined in MTP is passed.

8.11.1 Protections overview

Table 5. Overview of protections

Protection	Description	Implementation	Default filter
UVLO	undervoltage lockout	hardware	-
OVP	overvoltage protection	hardware	30 µs
OCP	overcurrent protection	hardware	20 ms
OTP (internal)	overtemperature protection	hardware	-
2 times OTP (external)	overtemperature protection	hardware	-
OGP	open-ground protection	hardware	-
UVP	undervoltage protection	software	-
OSUP	open-supply (VCC) protection	hardware	-
OV_DP_DM	overvoltage protection DP and DM pins	hardware	127 µs
OV_CC1_CC2	overvoltage protection CC1 and CC2 pins	hardware	127 µs

8.11.2 Secondary side safe restart protection

When a safe restart protection is triggered, the load switch is immediately turned off. The voltage loop is kept on and is regulated to the initial value (5 V typical). As the load switch is immediately turned off before the regulation reduces the output power, the VCC voltage may increase. To ensure that the VCC voltage has dropped to a safe value, before the load switch is turned on again, V_{CC} is discharged via an internal current source of 20 mA if it exceeds the level of $1.05 \times V_{default}$.

When the protection is triggered, the safe restart timer is started. After 1 s (default value), a restart sequence is performed, which reinitializes all circuits. Optionally, most protections can be changed to latched protections in MTP.

8.11.3 Undervoltage lockout (UVLO)

The level at which the UVLO protection is triggered is fixed. When V_{CC} drops to below the UVLO level, the load switch is immediately turned off. All settings are reset to their initial values. Internal circuitries are disabled.

8.11.4 Overvoltage protection (OVP)

The OVP level is set as a percentage of the requested output voltage level. The OVP level is set to default 125 % (V < 9 V) or 120 % (V ≥ 9 V) of the programmed output voltage. When V_{CC} continuously exceeds this level for longer than the minimum OVP time (default 30 µs), the OVP protection is triggered.

8.11.5 Overcurrent protection (OCP)

The default TEA19051BTK setting is CC mode. In CC mode, the current loop defines the maximum current. Instead, the OCP mode can be selected via MTP. The OCP level can be programmed individually for each PDO. OCP is only triggered if the OCP mode is set for the corresponding PDO and the output current is continuously higher than the programmed current level for more than the programmed OCP blanking time.

8.11.6 Overtemperature protection (OTP)

8.11.6.1 Internal OTP

When the internally measured temperature exceeds the programmed OTP setting, OTP is triggered, unless the protection is disabled in MTP. The temperature level can be defined in MTP. The default value is 113 °C.

Furthermore, the internal temperature sensor can be used to measure the temperature. The measured temperature can be sent via USB-PD.

8.11.6.2 External OTP

When the mode "NTC+OTP" is selected for GPIO1 (cable connector temperature) or GPIO2 (adapter temperature) in the MTP and the externally measured temperature exceeds the programmed OTP setting, OTP is triggered. The temperature level can be defined in MTP. The default value is 90 °C (see Section 15 and Table 4).

8.11.7 Open-ground protection (OGP)

An open-ground event is detected by monitoring the difference in voltage between the GND and SGND pins. When the difference is greater than the specified maximum voltage difference, OGP is triggered, unless the protection is disabled.

This feature protects the application from supplying high currents to the load when the ground pins of the sense resistor are not properly connected.

8.11.8 Open-supply protection (OSUP)

When the IC is not supplied via the VCC pin any more, the voltage on the OPTO pin is used to open the external load switch. Opening the external load switch prevents that the load is damaged if the VCC pin is disconnected.

8.11.9 Undervoltage protection (UVP)

The UVP level is set to 60 % PDO level. The reaction to a triggering of UVP is programmed in the firmware. The protection is a safe restart protection by default. The level can never be lower than the UVLO level. The level can be adjusted via MTP.

8.11.10 Output short protection (OSP)

At a shorted output, the VCC voltage drops to below the UVLO level. The load switch is turned off. After the programmed safe restart time, the output is enabled again. To meet the average input power requirement at a shorted output, a proper safe restart time must be chosen. When the VCC voltage exceeds the UVLO level, the primary controller initially limits the maximum output power.

Because the safe restart time is set to 1 s, the dissipation is limited to < 50 mW. This limitation prevents that the application heats up when the output is shorted.

8.11.11 OVP DP and DM pins (OV_DP_DM)

The overvoltage protection of the DP and DM pins can be enabled in MTP. However, it is switched off by default.

OV_DP_DM is a safe restart protection. When the DP or DM pin is shorted to V_{bus}, this protection is triggered. The trigger level of the OV_DP_DM is at 4.5 V. To prevent unwanted triggering, it has a 127 µs (default) blanking time.

8.11.12 OVP CC1 and CC2 pins (OV_CC1_CC2)

The overvoltage protection of the CC1 and CC2 pins can be enabled in MTP. However, it is switched off by default.

OV_CC1_CC2 is a safe restart protection. When the CC1 or CC2 pin is shorted to V_{bus}, this protection is triggered. The trigger level of the OV_CC1_CC2 is at 4.5 V. To prevent unwanted triggering, it has a 127 µs (default) blanking time.

8.11.13 Soft short protection CC pins (SHORT_CC1_CC2)

The CC pins are protected with a soft-short protection that measures the impedance of the CC lines. When the measured impedance is not according to the USB-PD specification, the load switch is opened.

9 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCC}	voltage on pin VCC		−0.5	+26	V
V_{OPTO}	voltage on pin OPTO		−0.5	+26	V
V_{CC1}	voltage on pin CC1		−0.5	+26	V
V_{CC2}	voltage on pin CC2		−0.5	+26	V
V_{DP}	voltage on pin DP		−0.5	+6	V
V_{DM}	voltage on pin DM		−0.5	+6	V
V_{SW}	voltage on pin SW		−0.5	V_{CC} + 9	V
V_{DISCH}	voltage on pin DISCH		−0.5	+26	V
V_{VSNS}	voltage on pin VSNS		−0.5	+3.6	V
V_{ISNS}	voltage on pin ISNS		−0.5	+3.6	V
V_{GPIO1}	voltage on pin GPIO1		−0.5	+3.6	V
V_{GPIO2}	voltage on pin GPIO2		−0.5	+3.6	V
V_{SDA}	voltage on pin SDA		−0.5	+3.6	V
V_{SCL}	voltage on pin SCL		−0.5	+3.6	V
General					
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−40	+150	°C
Electrosatic discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	human body model (HBM)	−2000	+2000	V
		charged device model (CDM)	−500	+500	V
		machine model (MM)	−200	+200	V

10 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCC}	voltage on pin VCC		0	21	V
V_{OPTO}	voltage on pin OPTO		0	21	V
V_{CC1}	voltage on pin CC1		0	5	V
V_{CC2}	voltage on pin CC2		0	5	V
V_{DP}	voltage on pin DP		0	5	V
V_{DM}	voltage on pin DM		0	5	V
V_{SW}	voltage on pin SW		0	V_{CC} + 6	V
V_{DISCH}	voltage on pin DISCH		0	21	V
V_{VSNS}	voltage on pin VSNS		0	2.5	V
V_{ISNS}	voltage on pin ISNS		0	3.3	V
V_{GPIO1}	voltage on pin GPIO1		0	3.3	V
V_{GPIO2}	voltage on pin GPIO2		0	3.3	V
V_{SDA}	voltage on pin SDA		0	3.3	V
V_{SCL}	voltage on pin SCL		0	3.3	V
General					
T_j	junction temperature		−20	+105	°C

11 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	60	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	30	K/W

12 Characteristics

Table 9. Characteristics

T_{amb} = 25 °C; V_{CC} = 5.0 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (VCC pin)						
$V_{th(UVLO)}$	undervoltage lockout threshold	falling	-	2.85	2.9	V
I_{CC}	supply current	unattached; V_{CC} = 5 V	-	1.8	-	mA
		nominal; V_{CC} = 5 V	-	3	-	mA
$I_{CC(dch)}$	discharge supply current	extra discharge current; V_{CC} = 1.05 × $V_{o(default)}$	-	20	-	mA
		discharge current of VCC during safe restart protection; depends on load conditions	-	20	-	mA
V_{os}	overshoot voltage	protection level voltage	-	1.05 × $V_{o(default)}$	-	V
CC1/CC2 section (CC1 and CC2 pins)						
Type C						
I_{pu}	pull-up current	current source for DFP pull-up indication				
		default current	−96	−80	−64	µA
		1.5 A mode	−194	−180	−166	µA
		3 A mode	−356	−330	−304	µA
V_{IH}	HIGH-level input voltage	with standard 5.1 kΩ pull-down resistance				
		default current	1.5	1.6	1.7	V
		1.5 A mode	1.5	1.6	1.7	V
		3 A mode	2.45	2.60	2.75	V
V_{IL}	LOW-level input voltage	with standard 5.1 kΩ pull-down resistance				
		default current	0.15	0.2	0.25	V
		1.5 A mode	0.35	0.40	0.45	V
		3 A mode	0.75	0.80	0.85	V
V_{ovp}	overvoltage protection voltage	CC1 and CC2 pins	-	4.5	-	V
USB-PD normative specification						
f_{bit}	bit rate	BMC bit rate	270	300	330	Kbps

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USB-PD transmitter normative specification						
t_{fall}	fall time	10 % and 90 % amplitude points; minimum is underloaded condition	300	-	650	ns
t_{rise}	rise time	10 % and 90 % amplitude points; minimum is underloaded condition	300	-	650	ns
V_o	output voltage	signal voltage swing	1.05	1.125	1.2	V
Z_o	output impedance	transmitter	-	45	-	Ω
USB-PD receiver normative specification						
C_{in}	input capacitance	receiver	-	250	-	pF
$\|t_{fltr(lim)}$	time constant limiting filter	receiver bandwidth	100	-	-	ns
z_i	input impedance	receiver	10	-	-	MΩ
V_i	input voltage	receiver comparator				
		low level	-	0.55	-	V
		high level	-	0.8	-	V
		hysteresis	-	250	-	mV
DP and DM pins						
V_{ovp}	overvoltage protection voltage	DM and DP pins	-	4.5	-	V
Qualcomm® QuickCharge™ QC2.0 and QC3.0						
R_{sw}	switch resistance	when DP and DM pins are shorted	-	-	20	Ω
V_i	input voltage	DM and DP comparator pins				
		high level	1.8	2.0	2.2	V
		low level	0.250	0.325	0.400	V
R_{pd}	pull-down resistance	pin DP	300	900	1500	kΩ
		pin DM	14.25	19.53	24.80	kΩ
t_d	delay time	attach debounce time (BC1.2)	1	-	1.5	s
		DM low debounce time after BC1.2 is completed	1	-	-	ms
		signal detection debounce time	20	40	60	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage control (VSNS pin)						
V_{ref}	reference voltage	input voltage range on the VSNS pin to control the voltage loop	0.3	-	2.4	V
V_{acc}	voltage accuracy	voltage loop accuracy; V_{CC} = 5 V	−2	-	+2	%
		measurement voltage accuracy	−2	-	+2	%
g_m	transconductance	VCC in; OPTO out	4	-	-	mA/mV
G_{max}	maximum gain	cable compensation	-	8	-	mV/mV
Current control (ISNS pin)						
I_{ref}	reference current	parameter can be programmed in MTP 10 bits	0	-	40	mV
I_{out}	output current	current loop accuracy; R_{sense} = 5 mΩ				
		0.5 A < I_{out} < 5 A	−100	-	+100	mA
		I_{out} > 5 A	−2	-	+2	%
		measurement current accuracy; R_{sense} = 5 mΩ				
		0.5 A < I_{out} < 5 A [1]	−100	-	+100	mA
		I_{out} > 5 A	−3	-	+3	%
g_m	transconductance	gain current; amplifier = 50	200	-		mA/mV
		gain current; amplifier = 25	100	-	-	mA/mV
GPIO1 and GPIO2 pins						
$I_{O(GPIOX)}$	output current on pin GPIOX	GPIO function = NTC (+OTP)				
		low temperatures (see Figure 6)	−15.75	−15.00	−14.25	µA
		medium temperatures (see Figure 6)	−63	−60	−57	µA
		high temperatures (see Figure 6)	−252	−240	−228	µA
T_{acc}	temperature accuracy	47 kΩ NTC (Beta = 4108)	−5	-	+5	°C
T_{res}	temperature resolution	temperature measurement	−1	-	+1	°C
V_I	input voltage	high level	1.5	-	-	V
		low level	-	-	0.9	V
V_O	output voltage	GPIO function = supply				
		high level; no load	2.7	3.0	3.3	V
		low level; no load	-	-	0.3	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_O	output current	GPIO function = supply				
		source; V_O = 2.3 V	-	-	−1	mA
		sink; V_O = 0.4 V	1	-	-	mA
SDA and SCL pins						
V_I	input voltage	high level	2.1	-	-	V
		low level	-	-	0.9	V
I_O	output current	$V_{o(SCL/SDA)}$ = 0.6 V	6	-	-	mA
V_{pu}	pull-up voltage		-	3	-	V
R_{pu}	pull-up resistance	for SDA and SCL	-	1	-	kΩ
Protections						
V_{ovp}	overvoltage protection voltage	with control loop in voltage control mode	3	-	25	V
$V_{ovp(acc)}$	overvoltage protection voltage accuracy	VCC pin; V_{ovp} = 6 V	−3	-	+3	%
V_{ocp}	overcurrent protection voltage		6	-	40	mV
$V_{ocp(acc)}$	overcurrent protection voltage accuracy		−3	-	+3	%
V_{uvp}	undervoltage protection voltage		3	-	21	V
$V_{uvp(acc)}$	undervoltage protection voltage accuracy		−3	-	+3	%
$I_{CC(dch)}$	discharge supply current	during safe restart protection	-	20	-	mA
SW driver						
R_O	output resistance	switch-on	-	80	-	kΩ
		switch-off	-	600	-	Ω
DISCH part (DISCH pin)						
R_{dch}	discharge resistance		-	3	-	Ω
$V_{det(rst)}$	reset detection voltage	hard reset	0.65	0.70	0.75	V
t_{act}	active time	maximum on-time during attached state	-	100	-	ms
OPTO pin						
$I_{O(min)}$	minimum output current		-	30	-	µA
$I_{O(max)}$	maximum output current		3.75	5	6.25	mA
Internal oscillator						
f_{osc}	internal oscillator frequency		-	10	-	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal temperature protection						
$T_{otp(acc)}$	overtemperature protection trip accuracy	temperature regarding the trip level programmed in MTP	−10	-	+10	°C

[1] The current sense pin can be used up to 40 mV. The result is a current range that depends on the programmed R_{sense} resistor. (e.g. with 10 mΩ, the value can be up to 4 A).

13 Application information

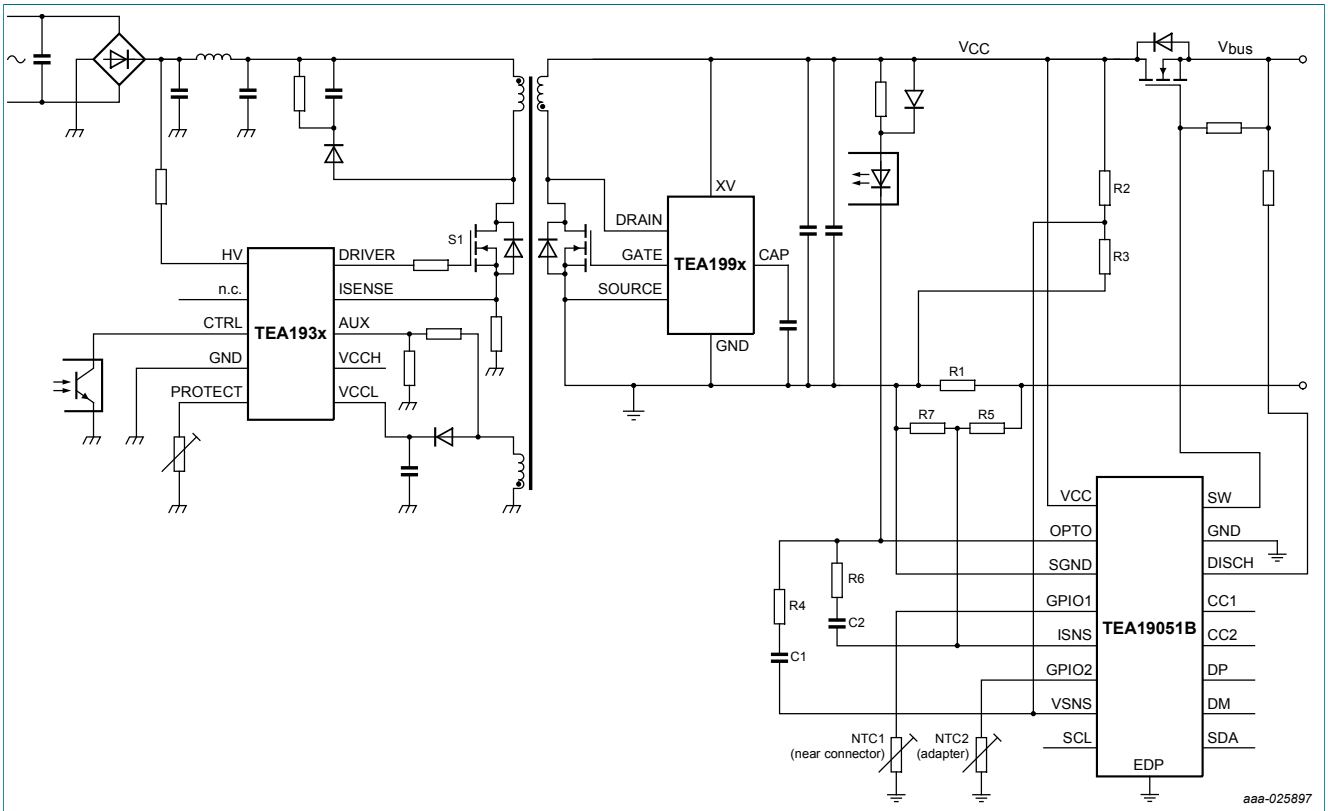


Figure 7. Typical application diagram, including TEA1938, TEA1999 (low-side SR), and TEA19051BTK

13.1 Resistor divider

The resistor divider (R3 / (R2 + R3) connected from the VCC pin to the VSNS pin must reduce the output voltage to < 2.5 V for the maximum output voltage. See Section 8.2 for more information about the divider ratios. To minimize the voltage drop at the connector, the resistor divider must be connected as close as possible to the load switch.

It is important that the external resistive divider exactly matches the internal value (MTP), because internal measurements depend on it. In the resistive divider, use resistors with a 1 % or better accuracy.

13.2 Sense resistor

The accuracy of the sense resistor R1 is very important. Any deviation from the value in MTP gives an offset in the current measurement. Because the sense resistor is very low-ohmic, the layout of the connections in the PCB can give major deviations from its initial value.

To overcome these deviations, several options are available:

- Change the sense resistor value such that the complete value is matching the typical MTP value (5 mΩ or 10 mΩ).
- Trim the value with a resistor divider so that the (R7 / (R5 + R7)) × (R1 + R_{PCB}) matches the MTP default value. R_{PCB} is the resistance of copper wires and the resistance change of the sense resistor due to its soldering profile.

To maximize accuracy and temperature stability, keep R_{pcb} as low as possible. The sense resistor must have a temperature coefficient that is as low as possible. To prevent magnetic coupling, keep the length and the area of the connections between the sense resistor and the SGND and ISNS pins as small as possible.

Connect the exposed die pad to the GND pin. Ensure that high currents flowing through the plane below the IC is prevented.

13.3 Voltage loop

In the application diagram, an integrator network is connected between the VSNS pin and the optocoupler. The recommended values of these components are:

- R2 = 160 kΩ to 180 kΩ
- R4 = 1 kΩ
- C1 = 10 nF; for the integral part

To prevent magnetic coupling to these parts, which results in pollution in output voltage, the length and the area of the connection must be kept as small as possible.

13.4 Current loop

For applications using the CC loop in the application, an integrator network is connected between the ISNS pin and the optocoupler. The recommended values for these components are:

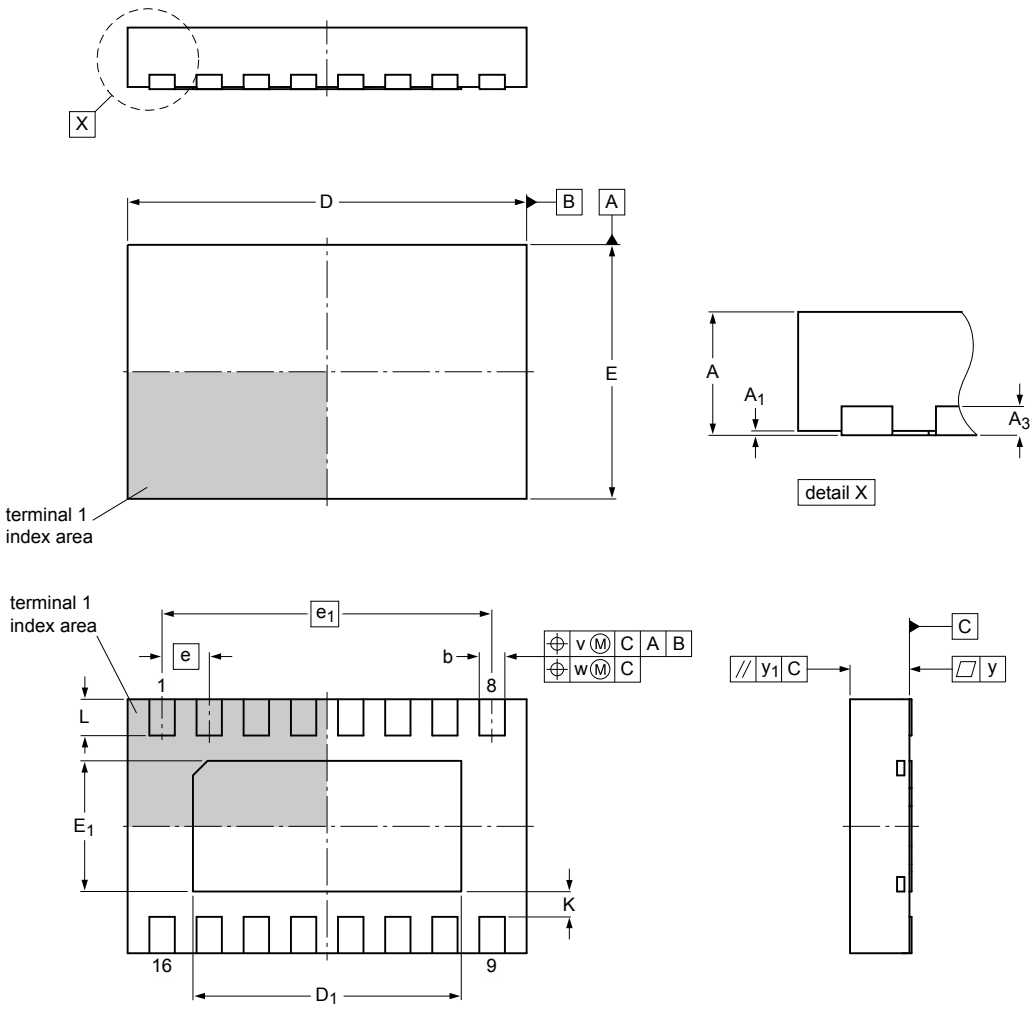
- R5 = 330 Ω when R1 = 10 mΩ; R5 = 160 Ω when R1 = 5 mΩ; connected between sense resistor and the ISNS pin for the proportional part.
- R6 = 5 kΩ
- C2 = 100 nF; for the integral part

To prevent magnetic coupling to these parts, which results in pollution in output currents, the length and the area of the connection must be kept as small as possible.

Resistor R6 and capacitor C2 can be removed in applications that use OCP mode.

14 Package outline

HVSON16: plastic thermal enhanced very thin small outline package; no leads; 16 terminals; body 3.5 x 5.5 x 0.85 mm **SOT1308-1**



Dimensions

Unit		A	A_1	A_3	b	D	D_1	E	E_1	e	e_1	k	L	v	w	y	y_1
mm	max	1.00	0.05		0.35	5.6	3.75	3.6	1.85				0.55				
	nom	0.85		0.2	0.32	5.5	3.70	3.5	1.80	0.65	4.55		0.50	0.1	0.05	0.05	0.1
	min	0.80	0.00		0.29	5.4	3.65	3.4	1.75			0.2	0.45				

sot1308-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1308-1		MO-229				~~11-07-04~~ 11-11-25

Figure 8. Package outline SOT1308-1 (HVSON16)

15 Appendix: Internal parameter settings per type

In this section, the internal parameter settings per type are given.

15.1 TEA19051BAATK

Table 10 gives an overview of the function settings in the TEA19051BAATK.

Table 10. Internal parameter settings

Function	TEA19051BAATK
power rating	27 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	NTC with OTP
GPIO2 protection level	90 °C
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	5.476
cable compensation	117 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	off
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAATK
PDO3	
PPS enable	FALSE
voltage	12 V
current	2.25 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	TRUE
maximum voltage	5.9 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	FALSE
OVP level	125 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE
PDO5	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.2 TEA19051BABTK

Table 11 gives an overview of the function settings in the TEA19051BABTK.

Table 11. Internal parameter settings

Function	TEA19051BABTK
power rating	45 W
supported standards	USB-PD3[1]; QC2.0; QC3.0
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	NTC with OTP
GPIO2 protection level	90 °C
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	8.325
cable compensation	100 mV/A
CC mode or OCP	OCP
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	off
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BABTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	FALSE
voltage	20 V
current	2.25 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.3 TEA19051BACTK

Table 12 gives an overview of the function settings in the TEA19051BACTK.

Table 12. Internal parameter settings

Function	TEA19051BACTK
power rating	65 W
supported standards	USB-PD3[1]; QC2.0; QC3.0
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	NTC with OTP
GPIO2 protection level	90 °C
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	8.325
cable compensation	100 mV/A
CC mode or OCP	OCP
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	off
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BACTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	FALSE
voltage	20 V
current	3.25 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.4 TEA19051BAFTK

Table 13 gives an overview of the function settings in the TEA19051BAFTK.

Table 13. Internal parameter settings

Function	TEA19051BAFTK
power rating	18 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5.10 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	disabled
GPIO2 protection level	-
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	5.476
cable compensation	88 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5.10 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	2 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAFTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	1.50 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	TRUE
maximum voltage	5.90 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	FALSE
OVP level	125 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE
PDO5	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	2 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.5 TEA19051BAGTK

Table 14 gives an overview of the function settings in the TEA19051BAGTK.

Table 14. Internal parameter settings

Function	TEA19051BAGTK
power rating	27 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	disabled
GPIO2 protection level	-
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	8.325
cable compensation	111 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAGTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	2.25 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	1.80 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	FALSE
voltage	20 V
current	1.35 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO6	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.6 TEA19051BAHTK

Table 15 gives an overview of the function settings in the TEA19051BAHTK.

Table 15. Internal parameter settings

Function	TEA19051BAHTK
power rating	30 W
supported standards	QC2; QC3[1]
default output voltage	5 V
default maximum current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	disabled
GPIO2 protection level	-
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	5.476
cable compensation	117 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	6 V
current	3 A
OVP level	125 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE

Function	TEA19051BAHTK
PDO3	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	12 V
maximum current	2.5 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO5	
PPS enable	TRUE
maximum voltage	5.9 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	FALSE
OVP level	125 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE
PDO6	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	125 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] The TEA19051BAH is USB-PD3/QC4 compliant, but USB-PD3/QC4 certification is not possible.

15.7 TEA19051BAKTK

Table 16 gives an overview of the function settings in the TEA19051BAKTK.

Table 16. Internal parameter settings

Function	TEA19051BAKTK
power rating	30 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	disabled
GPIO2 protection level	-
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	8.325
cable compensation	111 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAKTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	2.50 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	2.00 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	FALSE
voltage	20 V
current	1.50 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO6	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

Function	TEA19051BAKTK
PDO7	
PPS enable	TRUE
maximum voltage	16 V
minimum voltage	3.3 V
maximum current	2 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.8 TEA19051BAMTK

Table 17 gives an overview of the function settings in the TEA19051BAMTK.

Table 17. Internal parameter settings

Function	TEA19051BAMTK
power rating	60 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	NTC with OTP
GPIO2 protection level	90 °C
chip OTP trigger level	131 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	8.828
cable compensation	118 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAMTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	3.00 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	3.00 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	FALSE
voltage	20 V
current	3.00 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO6	
PPS enable	TRUE
maximum voltage	16 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	FALSE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

Function	TEA19051BAMTK
PDO7	
PPS enable	TRUE
maximum voltage	21 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.9 TEA19051BAPTK

Table 18 gives an overview of the function settings in the TEA19051BAPTK.

Table 18. Internal parameter settings

Function	TEA19051BAPTK
power rating	27 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	disabled
GPIO2 protection level	-
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	8.325
cable compensation	111 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAPTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	2.25 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	1.80 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	TRUE
maximum voltage	5.90 V
minimum voltage	3.30 V
maximum current	3.00 A
power limit enabled	FALSE
OVP level	125 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE
PDO6	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %

Function	TEA19051BAPTK
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

15.10 TEA19051BARTK

Table 19 gives an overview of the function settings in the TEA19051BARTK.

Table 19. Internal parameter settings

Function	TEA19051BARTK
power rating	100 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	NTC with OTP
GPIO2 protection level	90 °C
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	5 mΩ
external resistor divider VCC/VSNS (= DIV)	8.828
cable compensation	106 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	OFF
QC enable	TRUE
cable compensation enable	TRUE
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BARTK
PDO3	
PPS enable	FALSE
voltage	12 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	FALSE
voltage	15 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO5	
PPS enable	FALSE
voltage	20 V
current	5 A
OVP level	120 %
UVP level	60 %
QC enable	FALSE
cable compensation enable	TRUE
PDO6	
PPS enable	TRUE
maximum voltage	16 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	FALSE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

Function	TEA19051BARTK
PDO 7	
PPS enable	TRUE
maximum voltage	21 V
minimum voltage	3.3 V
maximum current	5 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

16 Abbreviations

Table 20. Abbreviations

Acronym	Description
AC	alternating current
APDO	augmented PDO
BMC	bi-phase mark coding
BOM	bill of materials
CC	constant current
CV	constant voltage
DC	direct current
DCM	discontinuous conduction mode
DFP	downstream facing port
DM	data minus
DP	data plus
EEPROM	electrically erasable programmable read-only memory
MTP	multi-time programmable
OCP	overcurrent protection
OGP	open-ground protection
OSP	output short protection
OSUP	output supply protection
OTP	overtemperature protection
OVP	overvoltage protection
PDO	power data object
PPS	programmable power supply
QR	quasi-resonant
RAM	random-access memory
ROM	read-only memory
RPDO	regular PDO
SCL	serial clock line
SDA	serial data line
SMPS	switched-mode power supply
UFP	upstream facing port
USB	universal serial bus
UVLO	undervoltage lockout
UVP	undervoltage protection
VDM	vendor defined messages

17 References

[1] **Battery Charging Specification** — Revision 1.2; including errata and ECNs through March 15, 2012; March 15, 2012

[2] **USB Type-C Cable and Connector Specification** — Revision 1.3; and ECNs; July 14, 2017

[3] **USB Power Delivery Specification** — Revision 2.0, version 1.3; January 12, 2017

[4] **USB Power Delivery Specification** — Revision 3.0, version 1.1; ECNs as of June 12, 2017; June 12, 2017

[5] **Qualcomm® QuickCharge™ 2.0 Interface Specification** — 80-NH008-1, revision AG; Qualcomm®, March 27, 2014

[6] **Qualcomm® QuickCharge™ 3.0 Interface Specification** — 80-NH008-2, revision K; Qualcomm®, August 1, 2017

[7] **Qualcomm® QuickCharge™ 4 Interface Specification** — 80-NH008-3, revision D; Qualcomm®, August 1, 2017

18 Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA19051BTK v.3	20190121	Product data sheet	-	TEA19051BTK v.2
Modifications:	• Section 4 "Ordering information" has been updated. • Section 5 "Marking" has been updated. • Section 15.9 "TEA19051BAPTK" has been added. • Section 15.10 "TEA19051BARTK" has been added.			
TEA19051BTK v.2	20180827	Product data sheet	-	TEA19051BTK v.1
TEA19051BTK v.1	20180206	Product data sheet	-	-

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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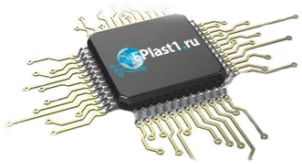

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