

Product Description

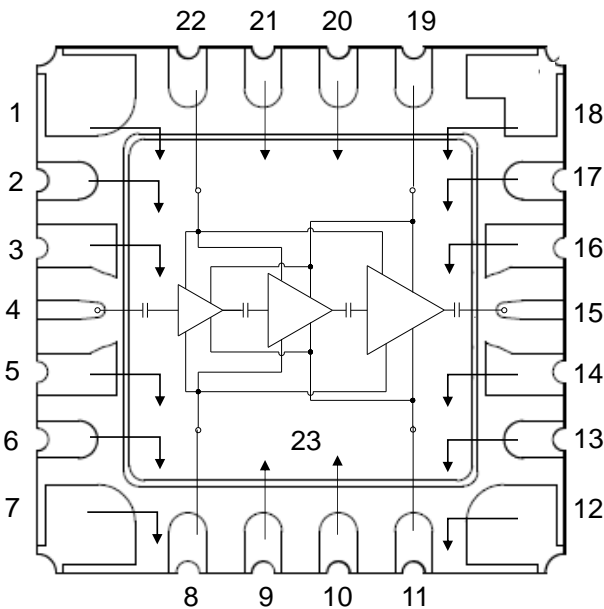
Qorvo's TGA2594-HM is a packaged power amplifier fabricated on Qorvo's 0.15um GaN on SiC process (QGaN15). Operating from 27 to 31 GHz, the TGA2594-HM achieves 36.5dBm saturated output power with a power-added efficiency of 25%, and 25dB small signal gain.

The TGA2594-HM is offered in a hermetically sealed 22-lead 7x7 mm ceramic QFN designed for surface mount to a printed circuit board. The package has a Cu-Mo base, offering superior thermal management. The TGA2594-HM is ideally suited to support both commercial and military applications.

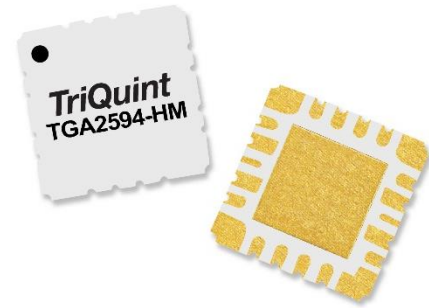
Both RF ports have integrated DC blocking capacitors and are fully matched to 50 Ohms.

Lead free and RoHS compliant.

Functional Block Diagram



Top View



Product Features

- Frequency Range: 27 – 31 GHz
- P_{OUT}: 36.5 dBm at P_{IN} = 14 dBm
- PAE: 25 % CW
- Small Signal Gain: 25 dB
- IM3: -35 dBc @ 25 dBm P_{OUT} / Tone
- Bias: V_D = +20 V, I_{DQ} = 140 mA, V_G = -3.0 V Typical
- Package Dimensions: 7 x 7 x 1.3 mm

Applications

- Military SATCOM Terminals
- Commercial SATCOM Terminals
- Point-to-Point Digital Radio
- Point-to Multipoint Digital Radio

Ordering Information

| Part No. | Description |
|------------|---------------------------------|
| TGA2594-HM | 27 – 31 GHz GaN Power Amplifier |



TGA2594-HM

27 – 31 GHz GaN Power Amplifier

Absolute Maximum Ratings

| Parameter | Value / Range |
|---|--------------------|
| Drain Voltage (V_D) | +29.5 V |
| Gate Voltage Range (V_G) | -5 to 0 V |
| Drain Current (I_D) | 1.4 A |
| Gate Current (I_G) | 85 °C: -3 to 17 mA |
| Power Dissipation (P_{DISS}), 85 °C | 15 W |
| Input Power, CW, 50 Ω , (P_{IN}) | 30 dBm |
| Mounting Temperature (30 Seconds) | 260 °C |
| Storage Temperature | -55 to 150 °C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

| Parameter | Value / Range |
|---|----------------|
| Drain Voltage (V_D) | +20 V |
| Drain Current (I_{DQ}) | 140 mA |
| Drain Current Under RF Drive (I_{D_DRIVE}) | See plots p. 7 |
| Gate Voltage (V_G) | -3 V (Typ.) |
| Gate Current Under RF Drive (I_{G_DRIVE}) | See plots p. 7 |
| Temperature (T_{BASE}) | -40 to 85 °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|--|-----|-------|-----|--------|
| Operational Frequency Range | 27 | - | 31 | GHz |
| Small Signal Gain | - | 25 | - | dB |
| Input Return Loss | - | > 5 | - | dB |
| Output Return Loss | - | > 5 | - | dB |
| Output Power @ $P_{IN} = 14$ dBm | - | 36.5 | - | dBm |
| Power Added Efficiency @ $P_{IN} = 14$ dBm | - | 25 | - | % |
| IM3 (P_{OUT} / Tone = 25 dBm/Tone) | - | -35 | - | dBc |
| IM5 (P_{OUT} / Tone = 25 dBm/Tone) | - | -43 | - | dBc |
| Small Signal Gain Temperature Coefficient | - | -0.05 | - | dB/°C |
| Output Power Temperature Coefficient | - | -0.04 | - | dBm/°C |

Test conditions unless otherwise noted: 25 °C, $V_D = +20$ V, $I_{DQ} = 140$ mA, $V_G = -3$ V Typ, CW.

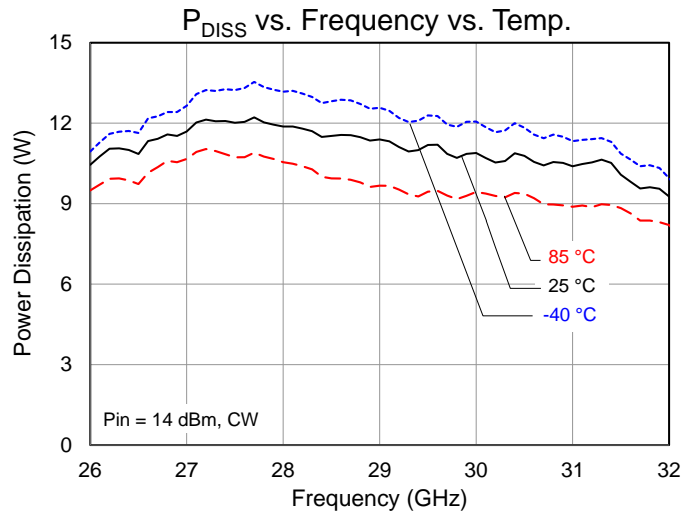
Thermal and Reliability Information

| Parameter | Test Conditions | Value | Units |
|---|---|-------|-----------------------------|
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | $T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = +20\text{ V}$ (CW) | 6.89 | $^{\circ}\text{C}/\text{W}$ |
| Channel Temperature (T_{CH}) (Under RF drive) | Freq=29 GHz, $P_{IN} = 14\text{ dBm}$, $I_{DQ} = 140\text{ mA}$, $I_{D_Drive} = 640\text{ mA}$, $P_{OUT} = 36\text{ dBm}$, $P_{DISS} = 9\text{ W}$ | 147 | $^{\circ}\text{C}$ |

Notes:

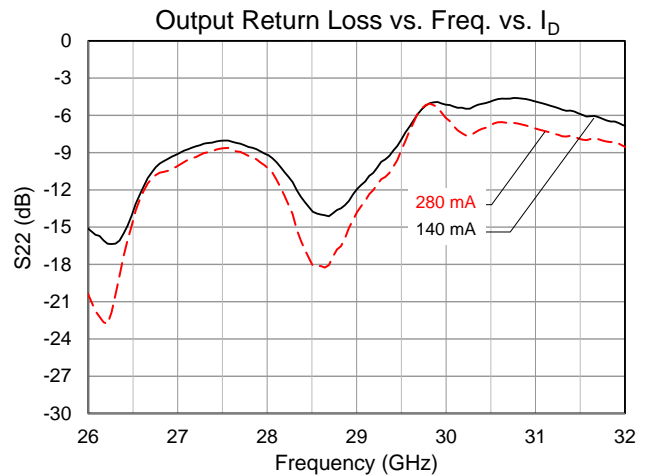
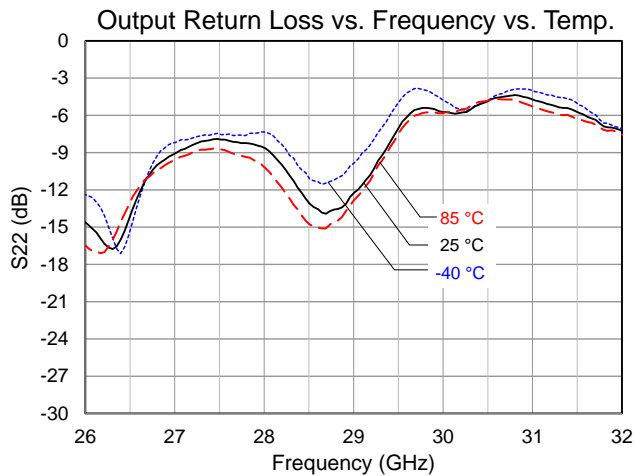
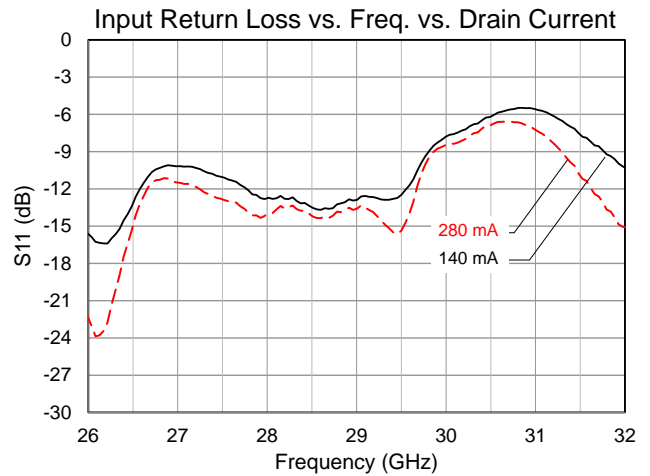
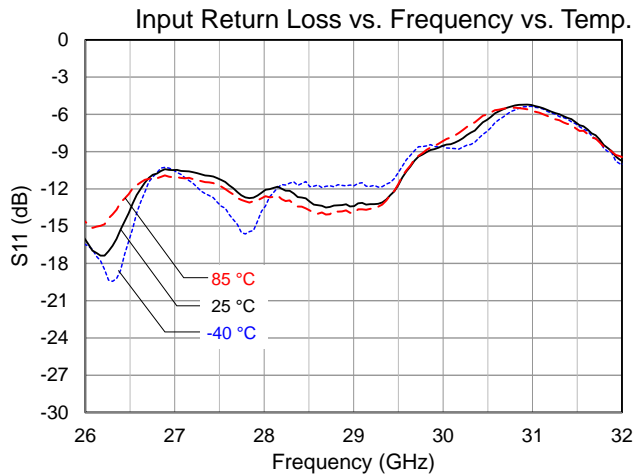
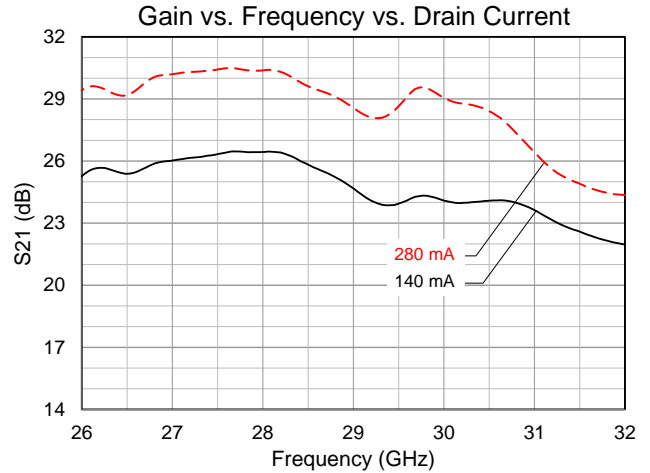
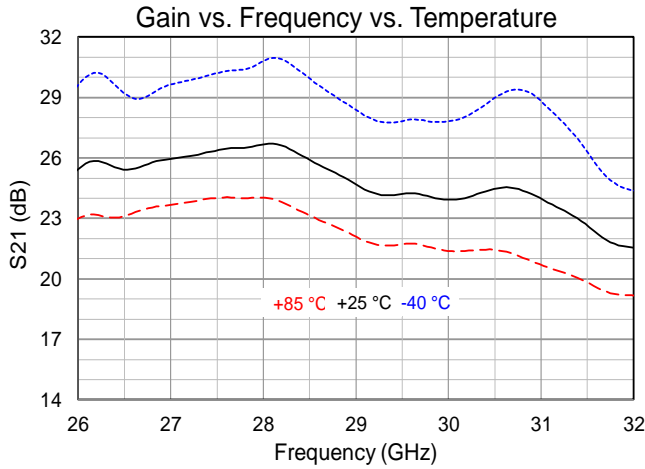
1. Thermal resistance measured to back of package.
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Power Dissipation



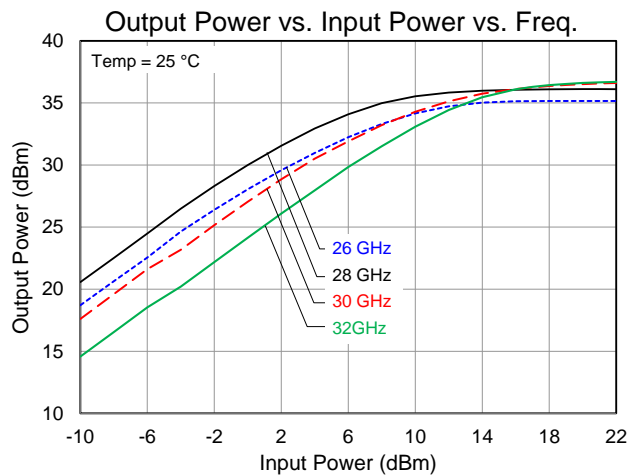
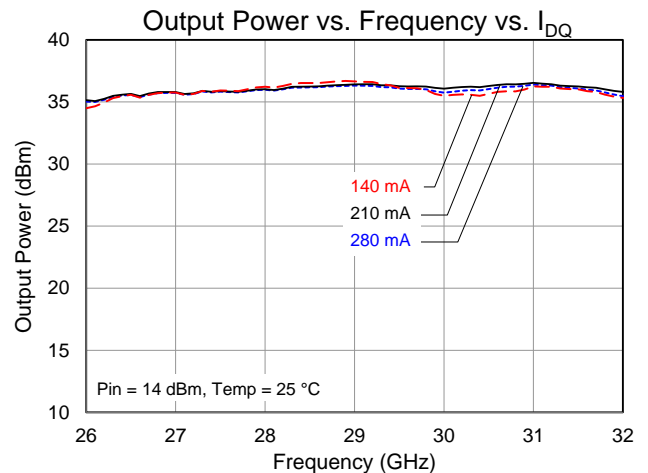
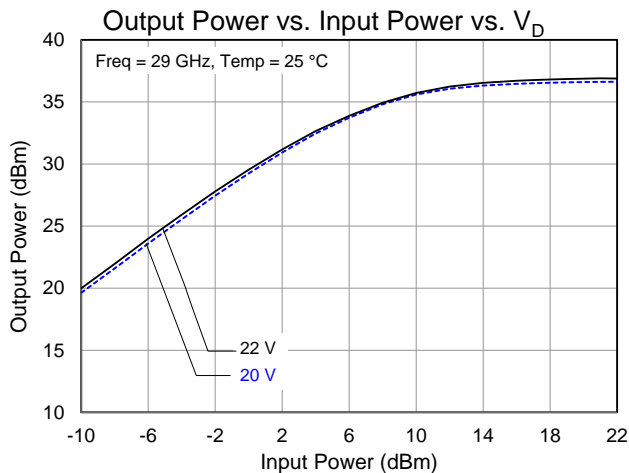
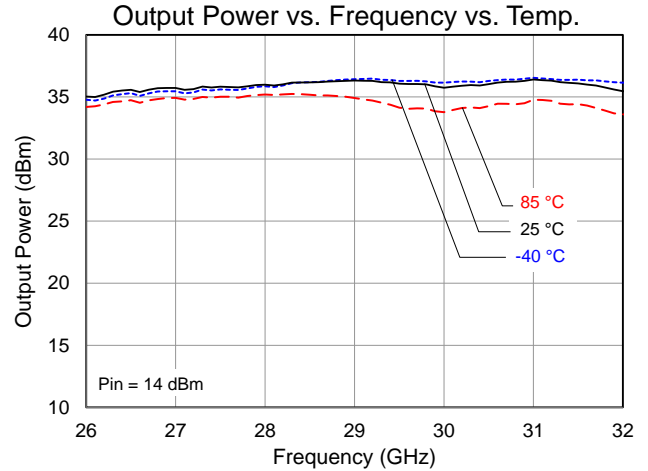
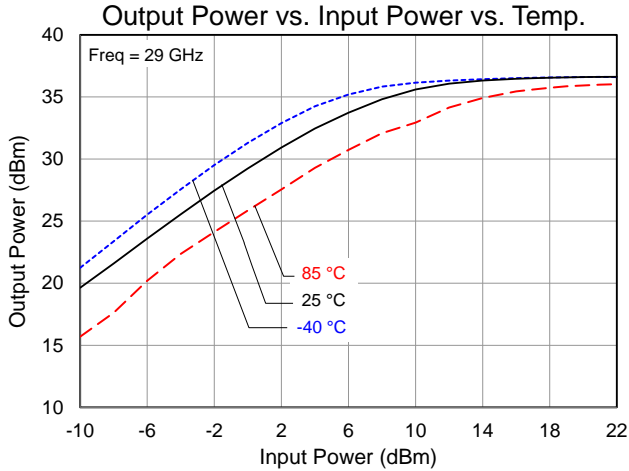
Performance Plots – Small Signal

Conditions unless otherwise specified: $V_D = +20\text{ V}$, $I_{DQ} = 140\text{ mA}$, $V_G = -3\text{ V}$ Typical, CW.



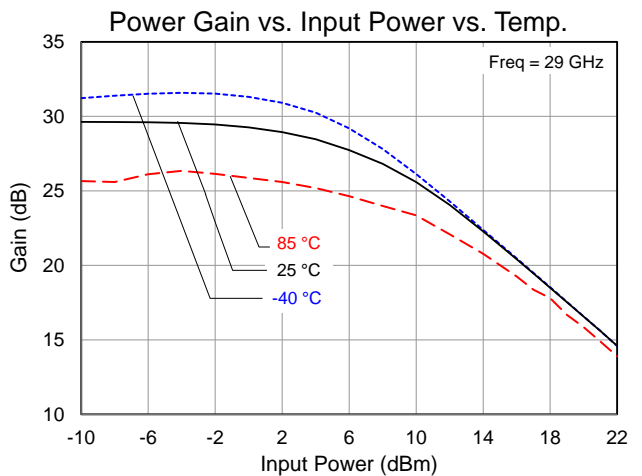
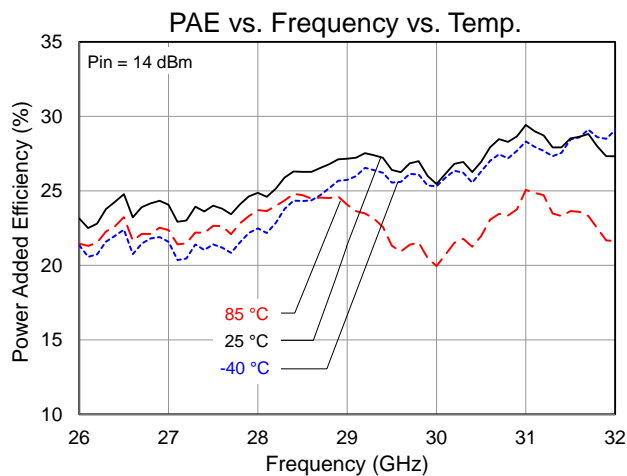
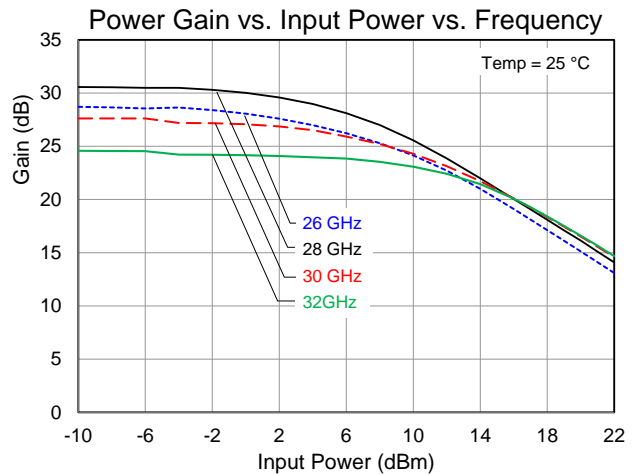
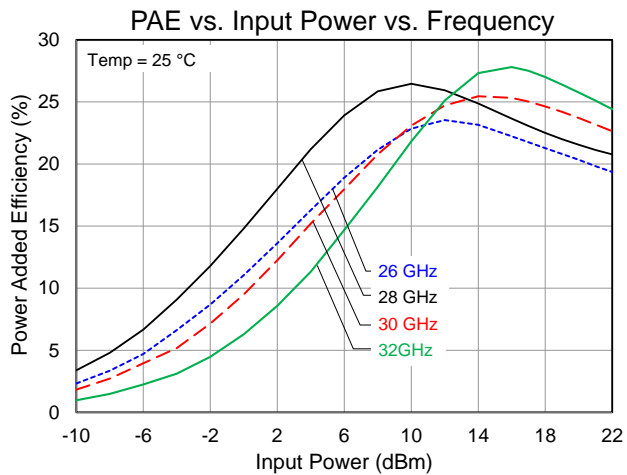
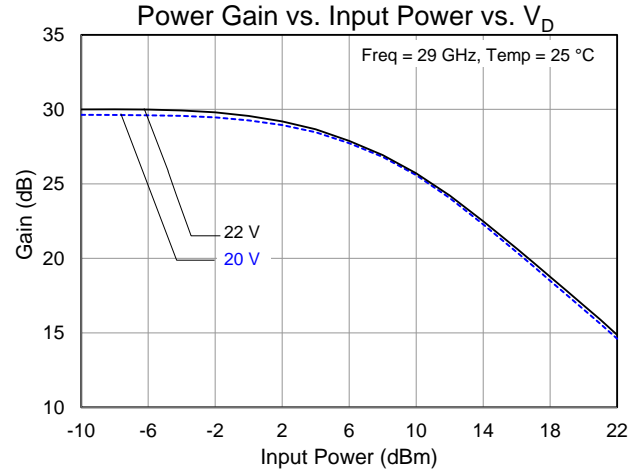
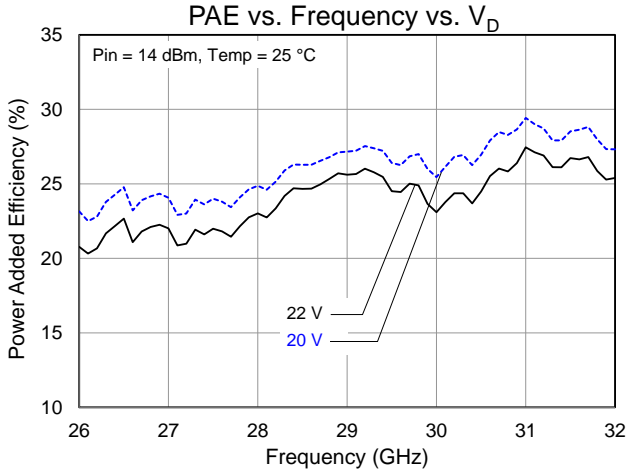
Performance Plots – Large Signal

Conditions unless otherwise specified: $V_D = +20\text{ V}$, $I_{DQ} = 140\text{ mA}$, $V_G = -3\text{ V}$ Typical, CW.



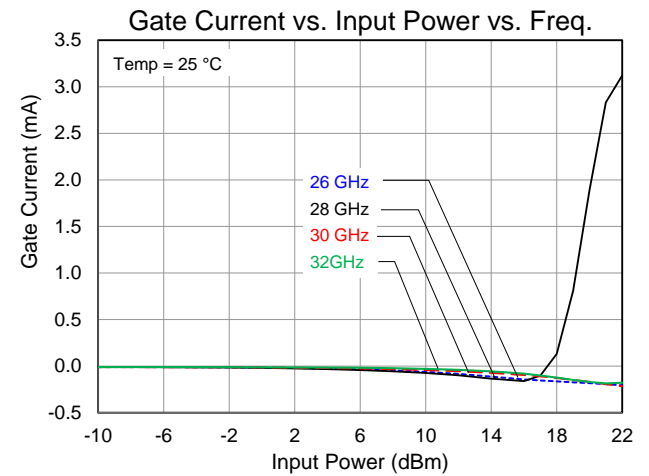
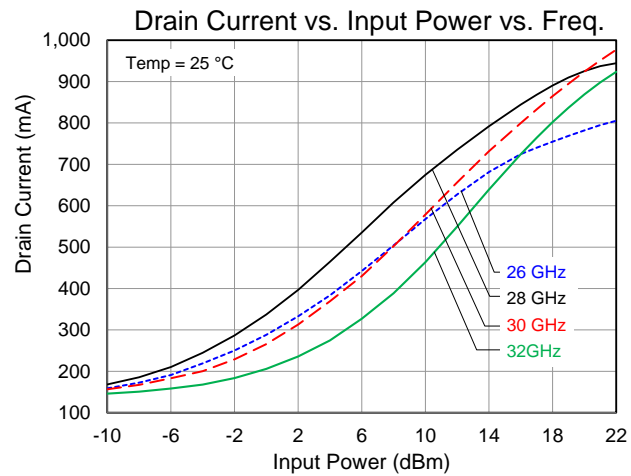
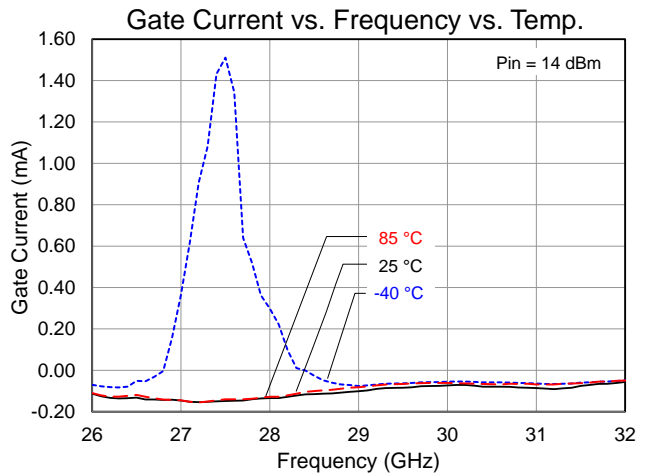
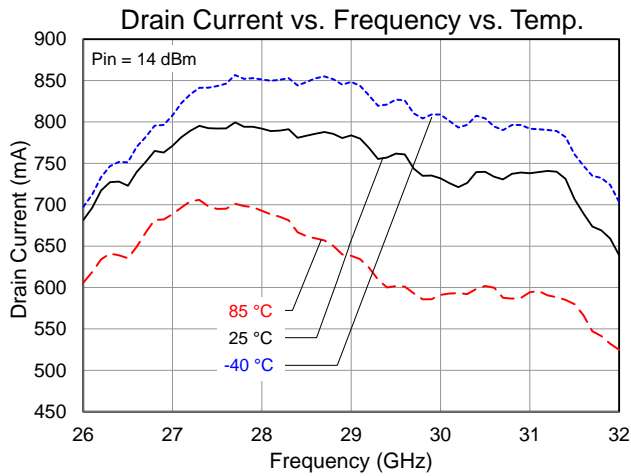
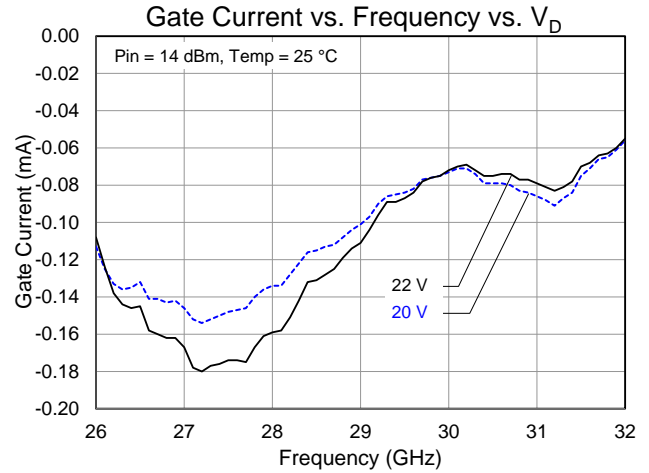
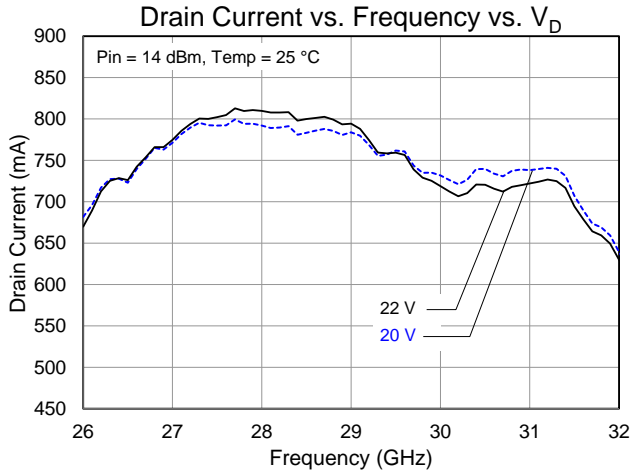
Performance Plots – Large Signal

Conditions unless otherwise specified: $V_D = +20\text{ V}$, $I_{DQ} = 140\text{ mA}$, $V_G = -3\text{ V}$ Typical, CW.



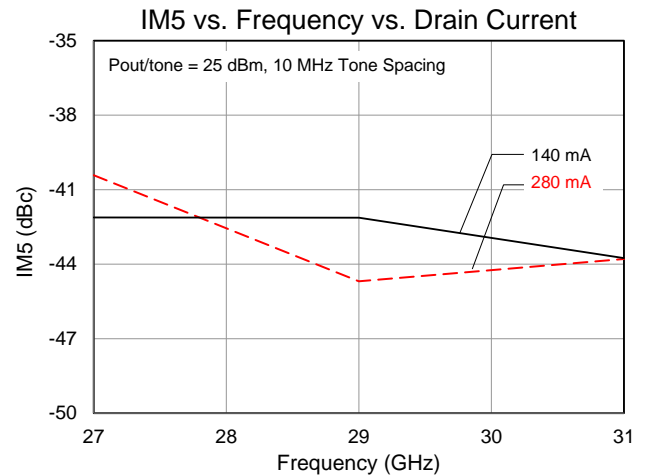
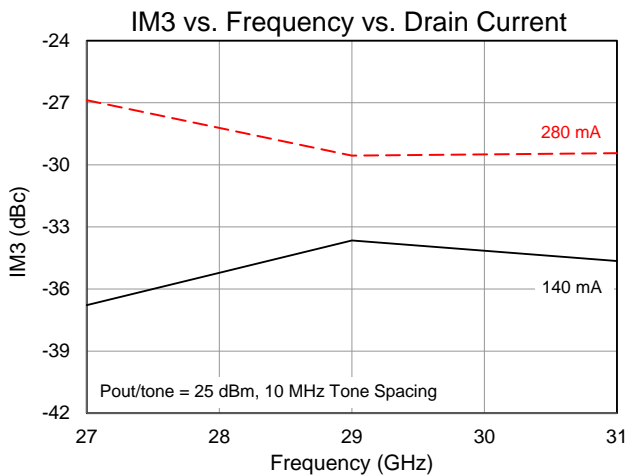
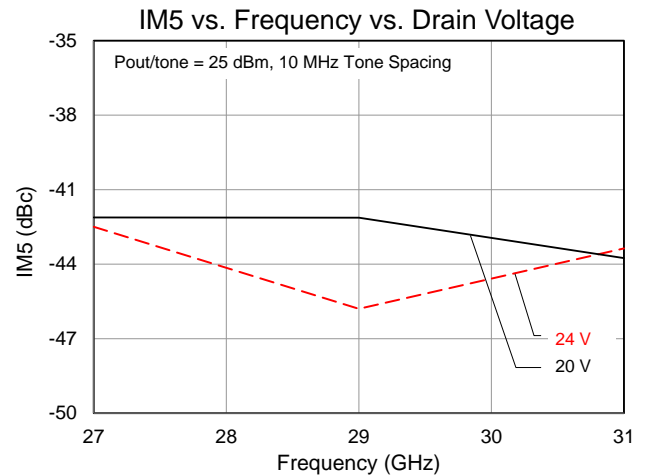
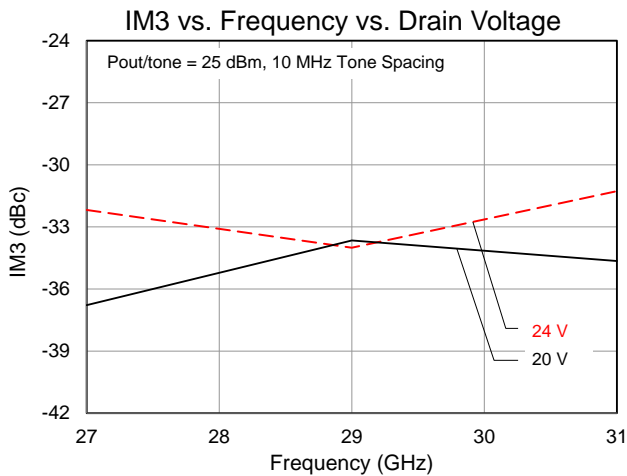
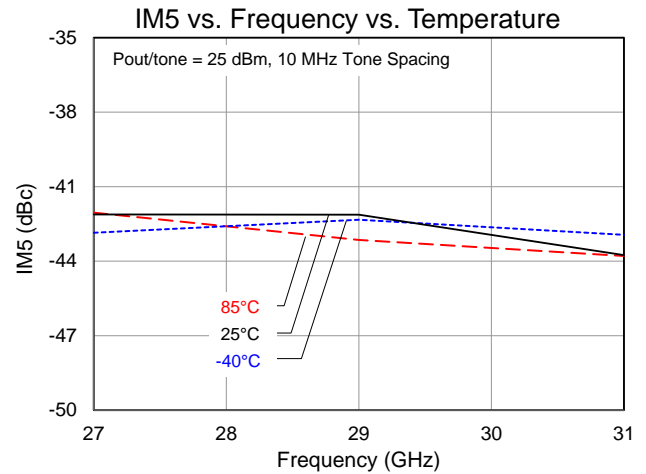
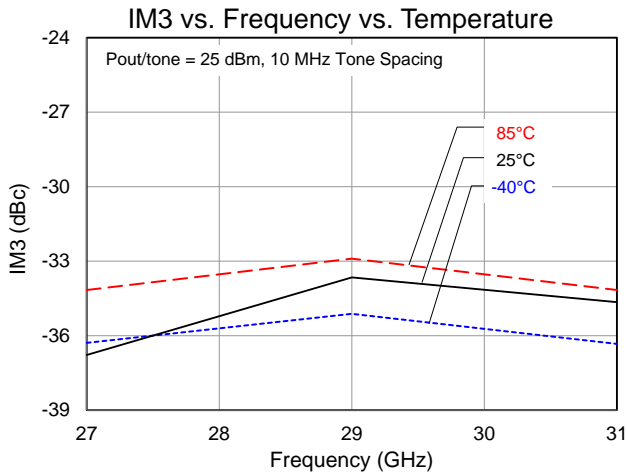
Performance Plots – Large Signal

Conditions unless otherwise specified: $V_D = +20\text{ V}$, $I_{DQ} = 140\text{ mA}$, $V_G = -3\text{ V}$ Typical, CW.

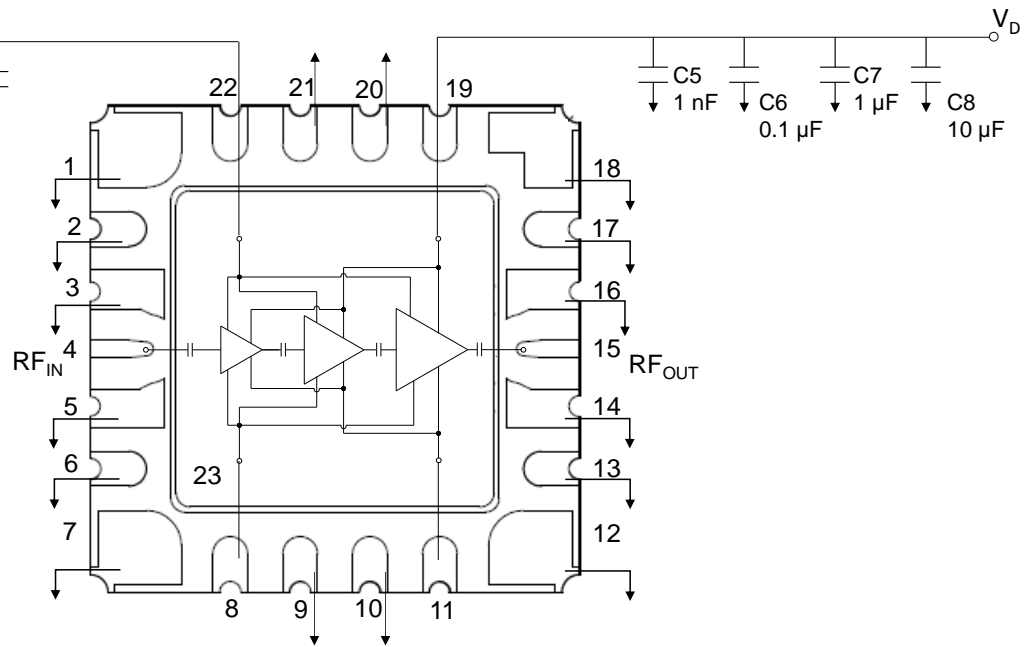


Performance Plots – Large Signal and Linearity

Conditions unless otherwise specified: $V_D = +20\text{ V}$, $I_{DQ} = 140\text{ mA}$, $V_G = -3\text{ V}$ Typical, CW.



Applications Information and Pad Layout



Top View

Bias Up Procedure

1. Set I_D limit to 1.2 A, I_G limit to 10 mA
2. Apply -5 V to V_G
3. Apply $+20\text{ V}$ to V_D ; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until $I_{DQ} = 140\text{ mA}$ ($V_G \sim -3\text{ V Typ.}$).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to -5 V ; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

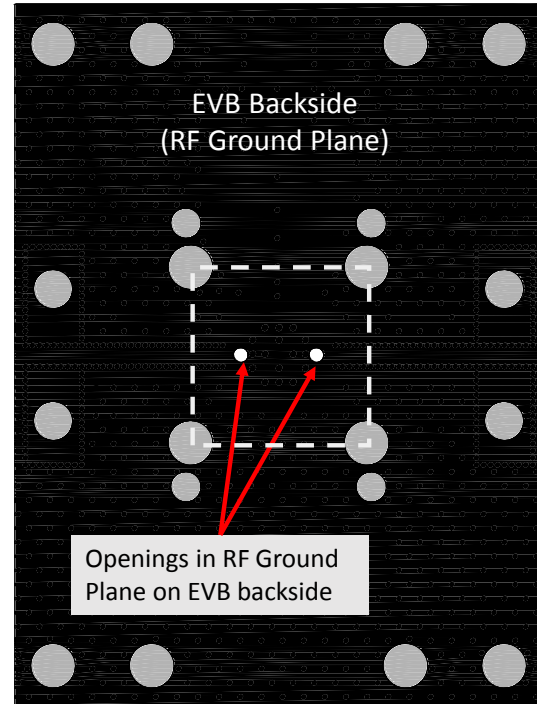
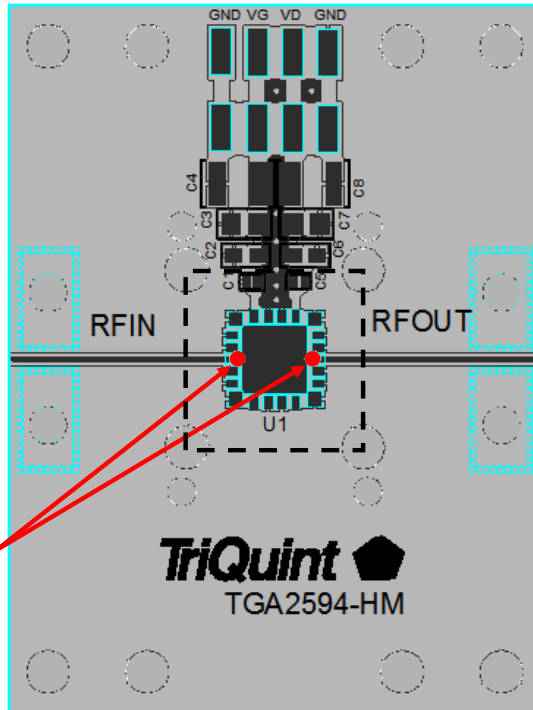
Pad Description

| Pad No. | Symbol | Description |
|---------------------------------------|--------------------|---|
| 1-3, 5-7, 9,10,12-14, 16-18, 20,21,23 | GND | Must be grounded on the PCB. |
| 4 | RF _{IN} | Output; matched to 50 Ω; DC blocked |
| 8, 11 | NC | For use with Q EVB, do not connect (pins are connected internal to package) |
| 15 | RF _{OUT} | Input; matched to 50 Ω; DC blocked |
| 19 | V _D (1) | Drain voltage; Bias network is required; see recommended Application Information above. |
| 22 | V _G (2) | Gate Voltage; Bias network is required; see recommended Application Information above. |

Notes:

1. If not using TQ EVB, V_D may be applied to either pin 11 or pin 19.
2. If not using TQ EVB, V_G may be applied to either pin 8 or pin 22.

Evaluation Board



Location of openings on backside of EVB

Openings in RF Ground Plane on EVB backside

- Notes:
1. Existence of 1 mm diameter opening on backside of EVB – the openings are required for all EVBs.
 2. See Assembly Notes (page 11) for additional detail.

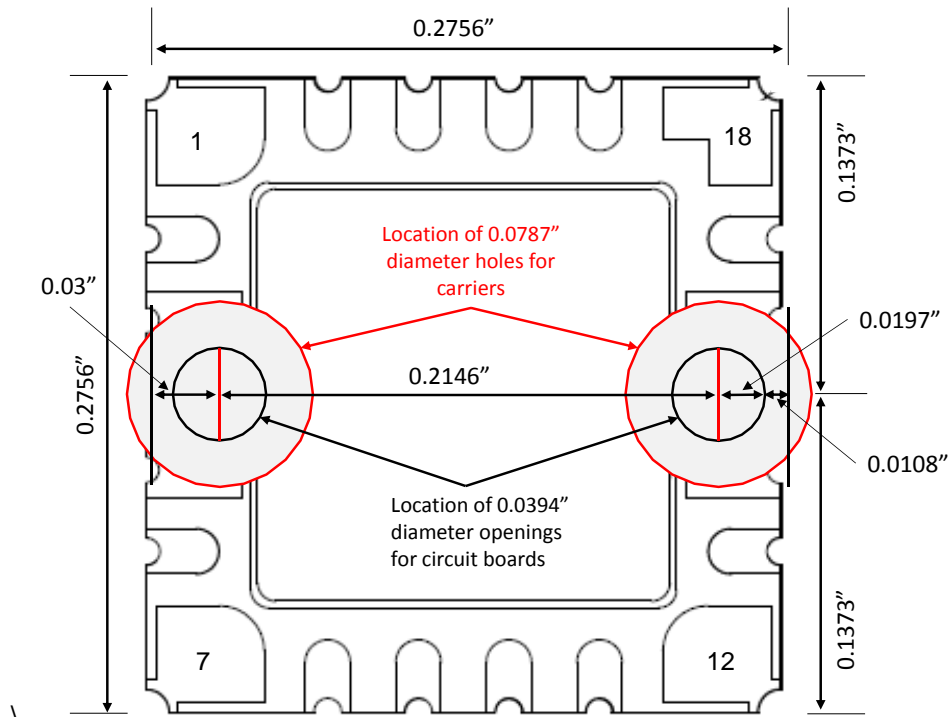
Bill of Materials

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|-------------|-----------------------------|---------|-------------|
| C1, C5 | 1 nF | Cap, 0402, +50 V, 10 %, X7R | Various | – |
| C2, C6 | 0.1 μ F | Cap, 0603, +50 V, 10 %, X7R | Various | – |
| C3, C7 (1) | 1 μ F | Cap, 0805, +50 V, 10 %, X7R | Various | – |
| C4, C8 (1) | 10 μ F | Cap, 1206, +50 V, 10 %, X7R | Various | – |

- Notes:
1. If the designated application is not sensitive to IM3, capacitors C3, C4, C7, and C8 may omitted.

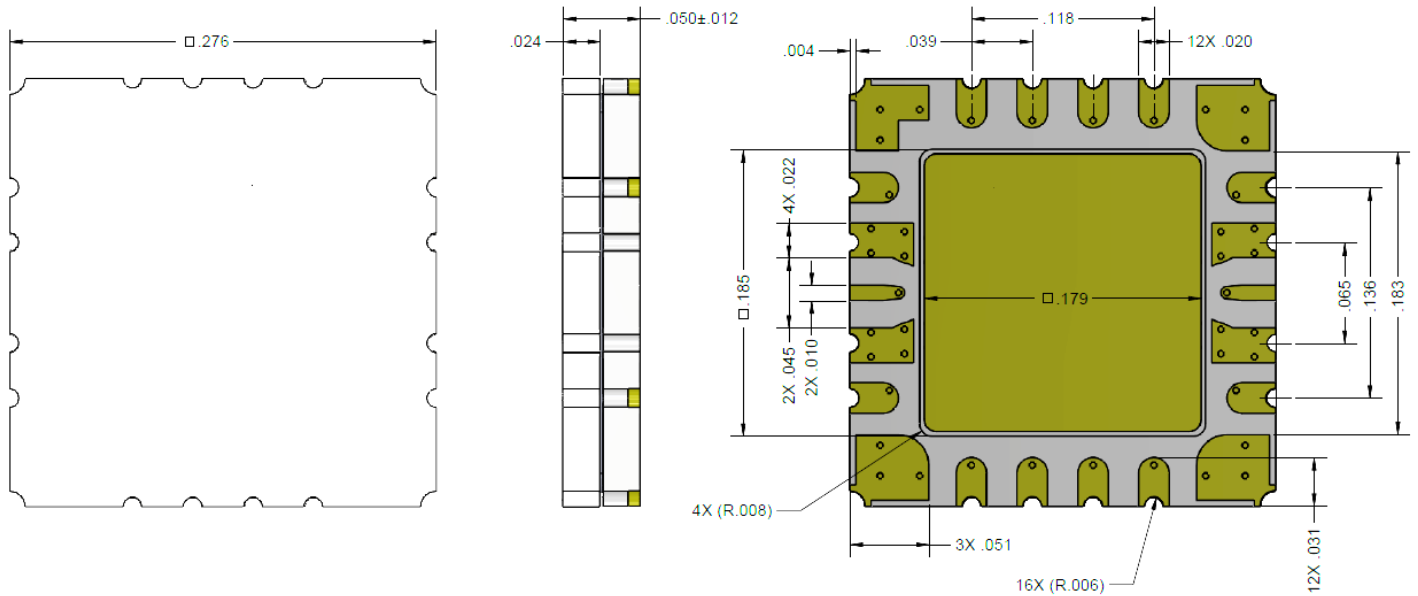
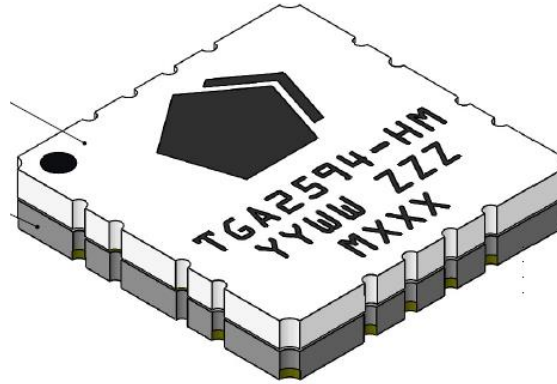
Assembly Notes

1. Clean the board or module with alcohol. Allow it to dry fully.
2. Apply solder paste to each pin of the TGA2594-HM, and heat achieve reflow, being careful not to exceed the thermal budget.
3. Clean the assembly with alcohol.
4. To attain quoted RF performance, the following is required:
 - i. On the printed circuit board, there must be two 1 mm (0.0394") diameter openings on the backside (RF Ground Plane) of the circuit board.
 - Location of the openings is contained in the Q Evaluation Board layout.
 - The 1 mm diameter openings for the board are shown in the diagram below in reference to the base of the package.
 - ii. Use of a carrier plate with 2 mm (0.0787") diameter holes.
 - The holes should be located with respect to the package pin-out as shown in the diagram below.
 - The holes should be 4 mm deep.
5. To improve thermal performance, the following is recommended:
 - i. The use of a 4 mil indium shim between the circuit board and the carrier plate.
 - ii. The In shim should have the same hole diameter and positioning as the carrier plate (see diagram below for location with respect to the package backside). The holes should be machined fully through the In shim.



Top View (through package to PCB/carrier)

Mechanical Information



Units: inches

Tolerances: unless specified

x.xx = ± 0.01

x.xxx = ± 0.006

Materials:

Package: Metal/Ceramic

Lid: Ceramic

All metalized features are gold plated

Part is solder sealed

Marking:

2594: Part number

YY: Part Assembly year

WW: Part Assembly week

ZZZ: Serial Number

MXXX: Batch ID

Handling Precautions

| Parameter | Rating | Standard |
|------------------------------|-----------------------|-------------------------------------|
| ESD – Human Body Model (HBM) | Class 1A, 400 V | JEDEC Standard JESD22 A114 |
| MSL – Convection Reflow | N/A, Hermetic Package | JEDEC standard IPC/JEDEC J-STD-020. |



Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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