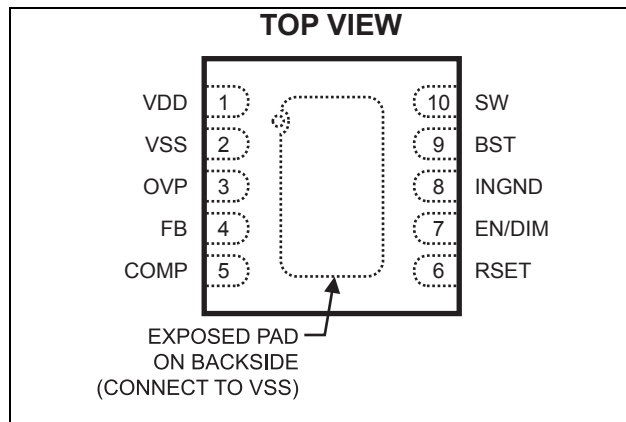


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T _A)
MP24183DQ	3x3 QFN10	9M	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP24183DQ–Z).
 For RoHS compliant packaging, add suffix –LF (e.g. MP24183DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage V _{DD} – V _{SS}	60V
V _{SW} – V _{SS}	-0.3V to V _{IN} + 0.3V
V _{BST}	V _{SW} + 6V
V _{OVP} – V _{SS}	-0.3V to +6V
V _{EN} – V _{INGND}	-0.3V to +6V
V _{DIM} – V _{INGND}	-0.3V to +6V
V _{INGND} – V _{SS}	-0.3V to 60V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	2.5W
Junction Temperature.....	150°C
Lead Temperature	260°C
Storage Temperature.....	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply Voltage V _{DD} – V _{SS}	4.5V to 55V
Operating Junct. Temp (T _J).....	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
3x3 QFN10.....	50	12 ... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)–T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device function is not guaranteed outside of the recommended operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_A = +25^\circ C$, all voltages with respect to V_{SS} , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	$4.5V \leq V_{IN} \leq 55V$	0.188	0.198	0.208	V
Feedback Current	I_{FB}	$V_{FB} = 0.22V$	-50		50	nA
Switch-On Resistance ⁽⁵⁾	$R_{DS(ON)}$			280		m Ω
Switch Leakage		$V_{EN} = 0V, V_{SW} = 0V$			1	μA
Current Limit ⁽⁵⁾				2.0		A
Oscillator Frequency	f_{SW}	$V_{FB} = 0.19V$, $R_{set} = 100k\Omega$		0.5		MHz
Default oscillator frequency	$f_{SW_default}$	$V_{FB} = 0.19V$, Rset open	1.05	1.35	1.65	MHz
Fold-back Frequency		$V_{FB} = 0V, V_{OVP} = 0V$		250		kHz
Maximum Duty Cycle		$V_{FB} = 0.19V$		90		%
Minimum On-Time ⁽⁵⁾	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising			3	3.3	3.6	V
Under Voltage Lockout Threshold Hysteresis				100		mV
EN Input Current		$V_{EN} = 2V$		2.1		μA
EN OFF Threshold (w/Respect to INGND)		V_{EN} Falling	0.4			V
EN ON Threshold (w/Respect to INGND)		V_{EN} Rising			0.6	V
Minimum EN Dimming Threshold		$V_{FB} = 0V$	0.6	0.7	0.8	V
Maximum EN Dimming Threshold		$V_{FB} = 0.2V$	1.25	1.4	1.5	V
Supply Current (Quiescent)	I_Q	$V_{EN} = 2V, V_{FB} = 1V$		0.8	1.0	mA
Supply Current (Quiescent) at EN Off	I_{off}	$V_{EN} = 0V$		3.4	15	μA
Thermal Shutdown ⁽⁵⁾				150		$^\circ C$
Open LED OV Threshold	V_{OVP_th}		1.1	1.2	1.3	V
Open LED OV Hysteresis	V_{OVP_hys}			60		mV

Notes:

5) Guaranteed by design.

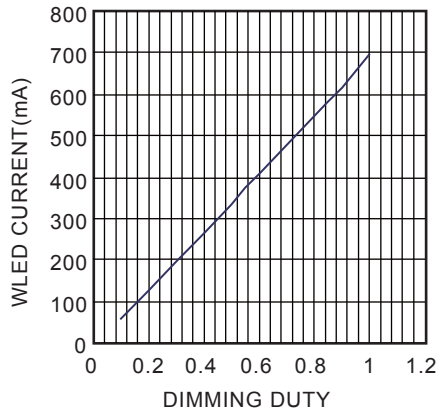
PIN FUNCTIONS

Pin #	Name	Description
1	VDD	Supply Voltage. The MP24183 operates from a +4.5V to +55V unregulated input (with respect to VSS). C1 is needed to prevent large voltage spikes from appearing at the input.
2	VSS	Power Return Pin. Connect to the lowest potential in the circuit, which is typically the anode of the Schottky rectifier. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part. The exposed pad is also connected to this pin.
3	OVP	Over Voltage Protection Pin. Use a voltage divider to program OVP threshold. When the OVP pin voltage reaches the shutdown threshold 1.2V, the switch will be turned off and will recover when OVP voltage decreases sufficiently. When the OVP pin voltage (with respect to VSS) is lower than 0.4V and FB pin voltage is lower than 0.1V, the chip recognizes this as short circuit condition and the operating frequency will be folded back. Program the OVP pin voltage from 0.4V to 1.2V for normal operation.
4	FB	LED Current Feedback Input. MP24183 regulates the voltage across the current sensing resistor between FB and VSS. Connect the current sensing resistor from the bottom of the LED strings to VSS. The FB pin is connected to the bottom of the LED strings. The regulation voltage is 0.198V.
5	COMP	Output of error amplifier. Connect a 1nF or larger capacitor on COMP to improve the stability and to provide a soft on at start up and PWM dimming.
6	RSET	Frequency Set Pin. Connect a resistor to VSS to set the switching frequency and an 1nF capacitor to VSS to bypass the noise. Leaving this pin open gets a default operating frequency 1.35MHz.
7	EN/DIM	On/Off Control Input and Dimming Command Input. A voltage greater than 0.6V will turn on the chip. Both DC and PWM dimming are implemented on this pin. When the EN/DIM pin voltage (with respect to INGND) rises from 0.7V to 1.4V, the LED current will change from 0% to 100% of the maximum LED current. To use PWM dimming, apply a 100Hz to 2kHz square wave signal with amplitude greater than 1.4V to this pin.
8	INGND	Input Ground Reference. This pin is the reference for the EN/DIM signal.
9	BST	Bootstrap. A capacitor is connected between SW and BST pin to form a floating supply across the power switch driver. A 100nF or larger ceramic capacitor is recommended to provide sufficient energy to drive the power switch's gate above the supply voltage.
10	SW	Switch Output. SW is the source of the internal MOSFET switch. Connect this pin to the power inductor and the cathode of the Schottky rectifier.
		Exposed pad should be connected to VSS in step up/down mode.

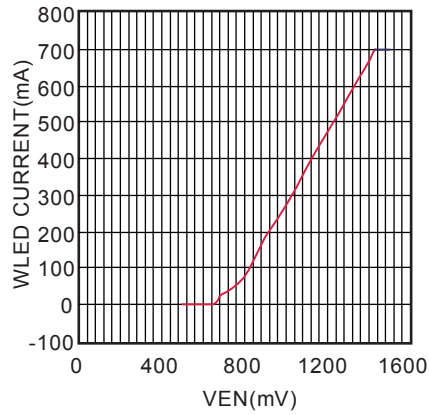
TYPICAL PERFORMANCE CHARACTERISTICS

VIN=20V, ILED=0.7A, two 3W LED in series, step down application, unless otherwise noted.

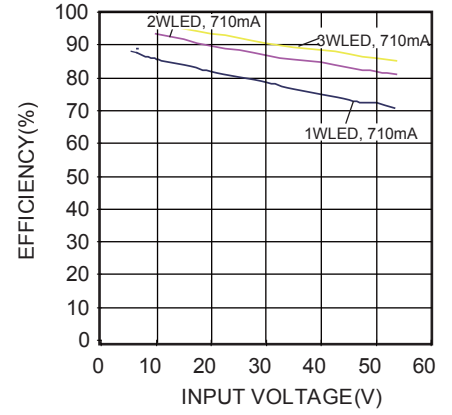
WLED current vs Dimming Duty

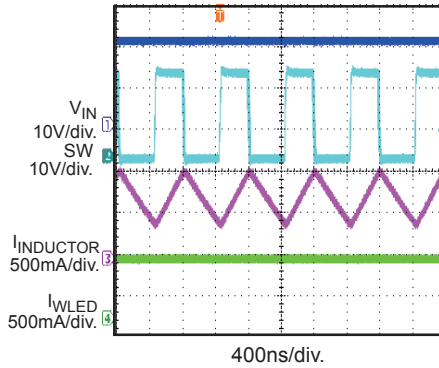
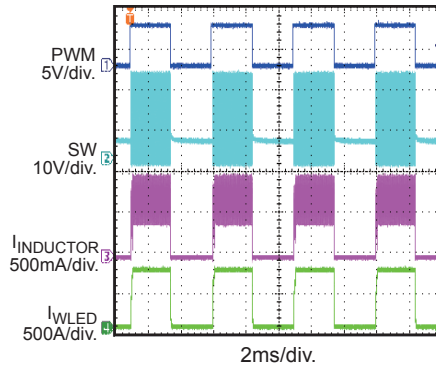
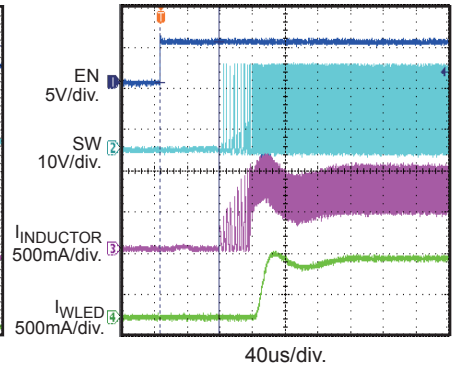
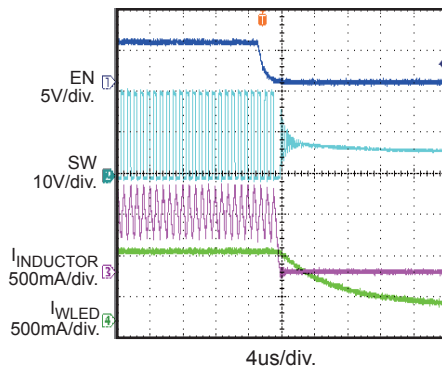
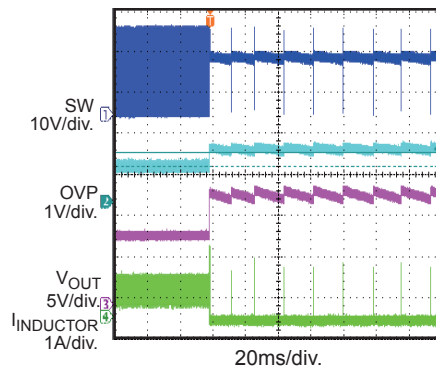
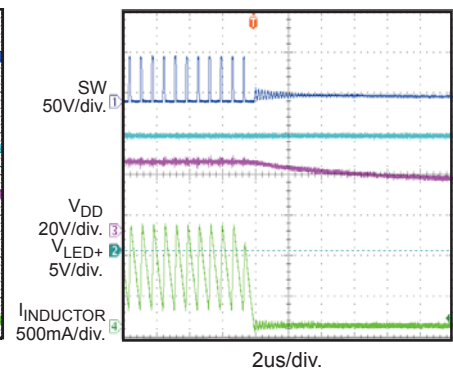


WLED Current vs VEN



Efficiency



TYPICAL PERFORMANCE CHARACTERISTICS (continued)
V_{IN}=20V, I_{LED}=0.7A, two 3W LED in series, step down application, unless otherwise noted.
Steady State

PWM Dimming

EN on

EN off

Open LED Protection

VDD-VSS OVP Protection


FUNCTIONAL BLOCK DIAGRAM

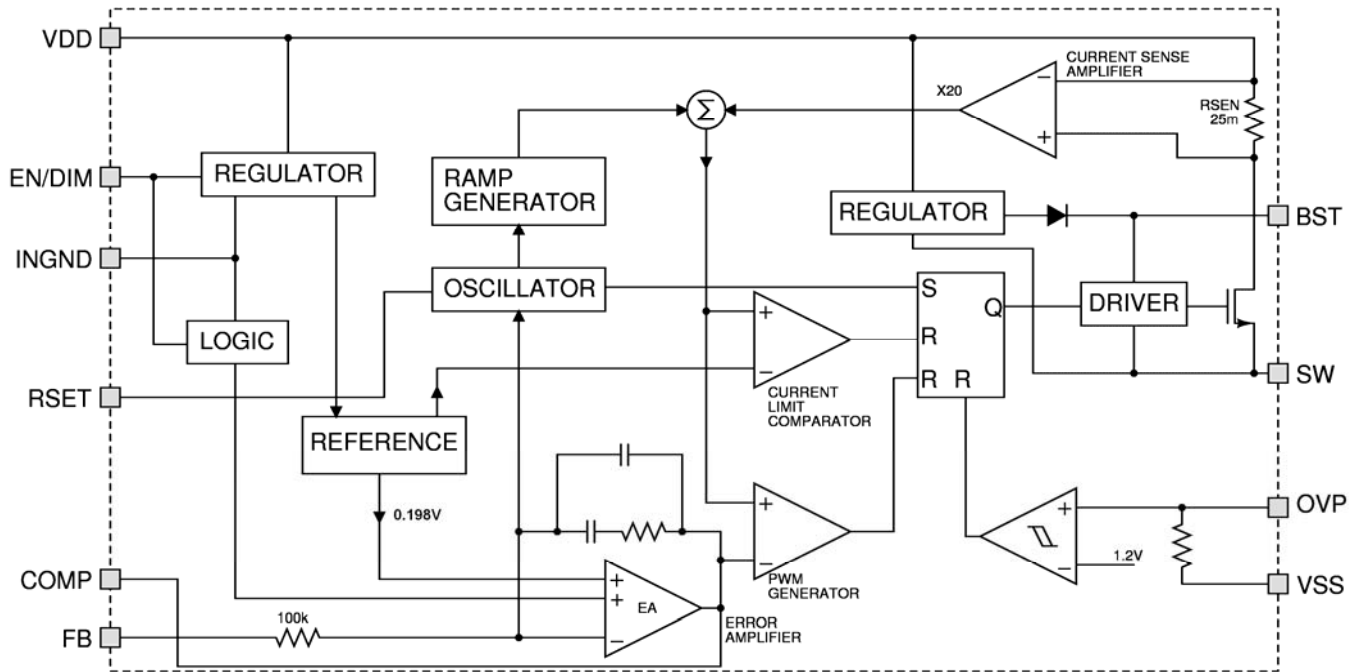


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

Setting the LED Current

The external resistor is used to set the maximum LED current (see the schematic on front page) through the use of the equation:

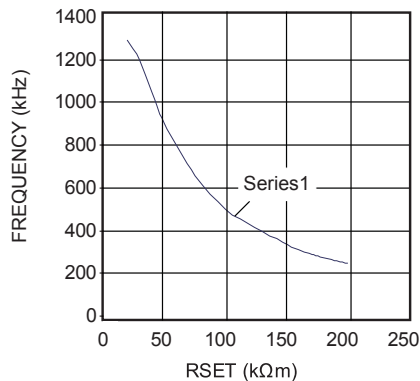
$$R_{\text{SENSE}} = \frac{0.198\text{V}}{I_{\text{LED}}}$$

Setting the Operating Frequency

The resistor on Rset pin is used to set the operating frequency. A 1nF capacitor is recommended to bypass this pin to GND.

The relationship between the operating frequency and the Rset resistor is as the following curve. A 20kΩ to 200kΩ Rset resistor is recommended, which sets the operating frequency from around 1.3MHz to 250kHz. Leaving the RSET pin open will set the operating frequency to the default operating frequency 1.35MHz.

Frequency vs. RSET



Selecting the Inductor

(Step-Down Applications, see Figure 3)

A 1μH to 47μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For high efficiency, the inductor's DC resistance should be less than 200mΩ. Refer to Table 2 for suggested surface mount inductors. For most designs, the required inductance value can be derived from the following equation.

$$L = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \times \Delta I_L \times f_{\text{SW}}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(\text{MAX})} = I_{\text{LOAD}} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Also note that the maximum recommended load current is 2A if the duty cycle exceeds 35%.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stable. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 2.2μF ceramic capacitor will be sufficient.

PC Board Layout

The high current paths (VSS, VDD and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the VDD and VSS pins. The external feedback resistors should be placed next to the FB pin. Keep the switch node traces short and away from the feedback network.

Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance(μH)	Max DCR(Ω)	Current Rating (A)	Dimensions L x W x H (mm ³)
Toko	A921CY-4R7M	4.7	0.027	1.66	6 x 6.3 x 3
Sumida	CDRH4D28C/LD	4.7	0.036	1.5	5.1 x 5.1 x 3
Würth Electronics	7440530047	4.7	0.038	2.0	5.8 x 5.8 x 2.8

TYPICAL APPLICATION CIRCUITS

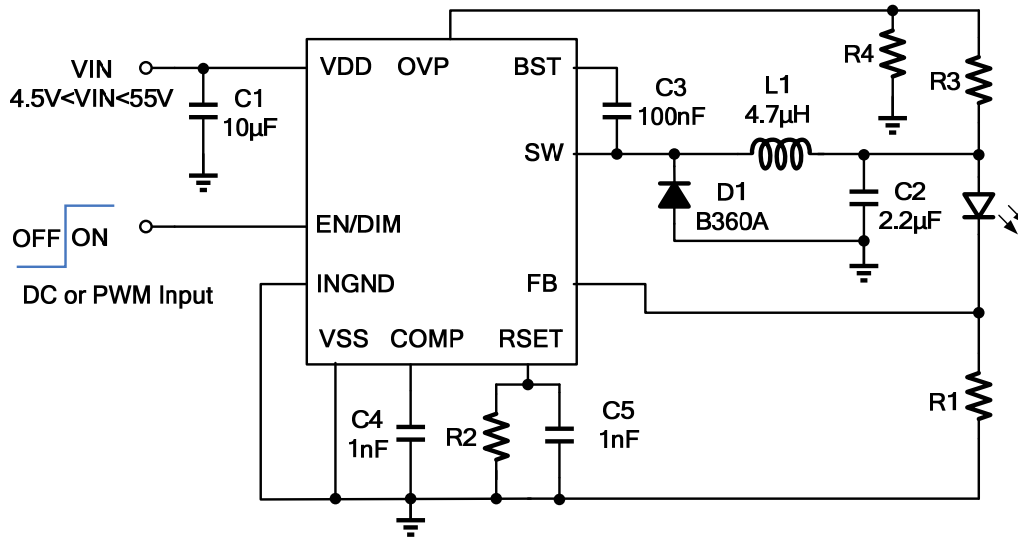


Figure 3—Step-Down White LED Driver Application

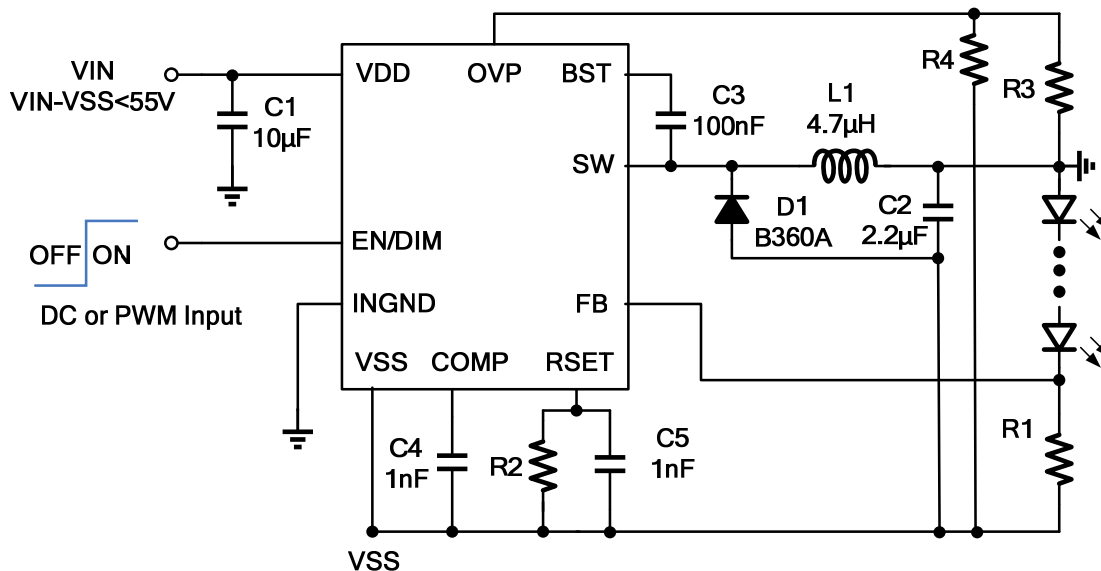


Figure 4— Step-up/down White LED Driver Application

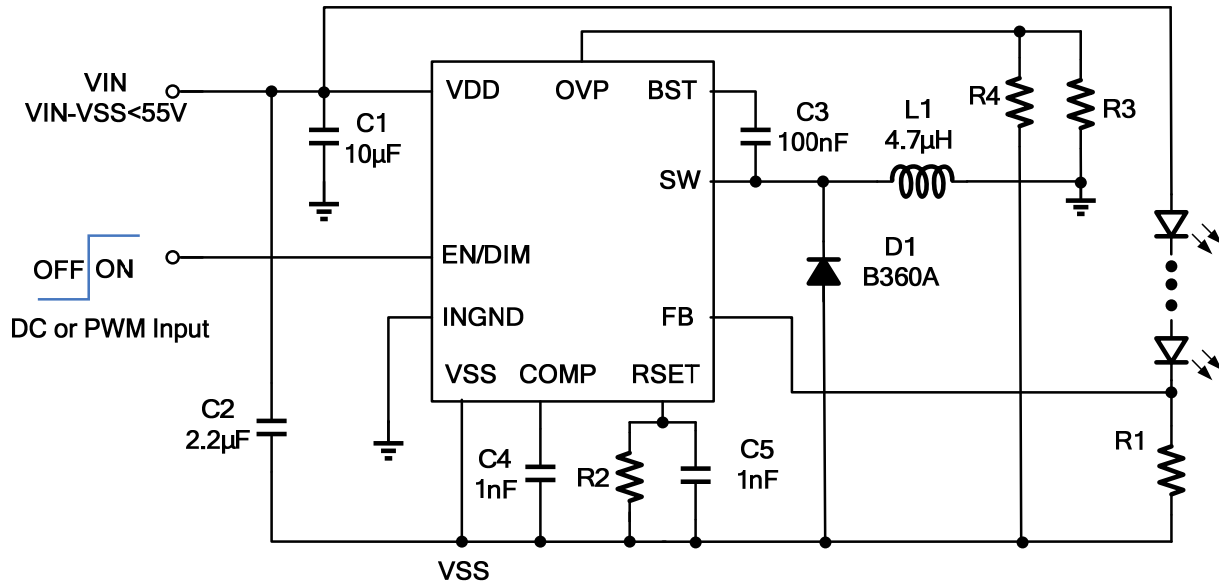
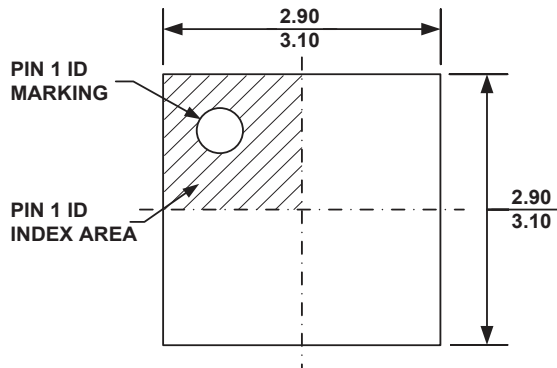


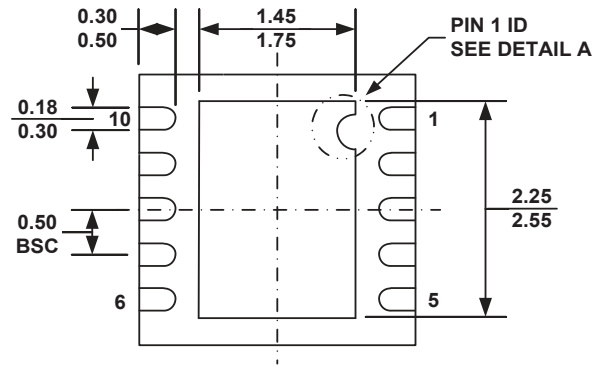
Figure 5— Step-up White LED Driver Application

PACKAGE INFORMATION

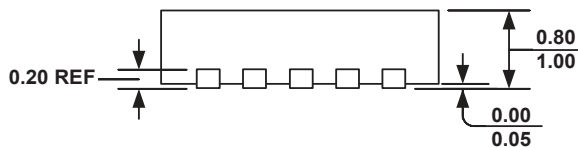
3mm x 3mm QFN10



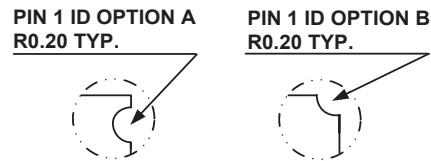
TOP VIEW



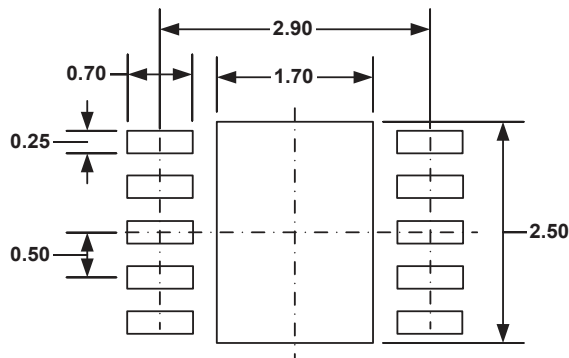
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
- 5) DRAWING IS NOT TO SCALE.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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