

SIPMOS® Small-Signal-Transistor
Features

- P-Channel
- Enhancement mode
- Normal level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC61249-2-21

Product Summary

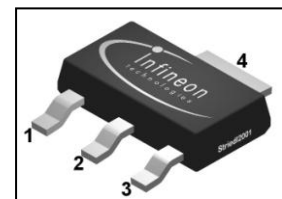
V_{DS}	-100	V
$R_{DS(on),max}$	900	mΩ
I_D	-0.98	A



Halogen-Free



PG-SOT-223



Type	Package	Tape and Reel Information	Marking	Lead free	Packing
BSP321P	PG-SOT-223	H6327: 1000 pcs/reel	BSP321P	Yes	Non dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	-0.98	A
		$T_C=70\text{ °C}$	-0.79	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}$	-3.9	
Avalanche energy, single pulse	E_{AS}	$I_D=-0.98\text{ A}$, $R_{GS}=25\text{ Ω}$	57	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	1.8	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	°C
ESD Class		JESD22-A114-HBM	1A (250V to 500V)	
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, steady state	-	-	115	
		6 cm ² cooling area ¹⁾ , steady state	-	-	70	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=-250\text{ }\mu\text{A}$	-100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-380\text{ }\mu\text{A}$	-2.1	-3.0	-4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-0.1	-1	μA
		$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10\text{ V}$, $I_D=-0.98\text{ A}$	-	689	900	m Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=-0.79\text{ A}$	0.6	1.2	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-25\text{ V},$ $f=1\text{ MHz}$	-	240	319	pF
Output capacitance	C_{oss}		-	62	82	
Reverse transfer capacitance	C_{rss}		-	28	42	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-50\text{ V}, V_{GS}=-10\text{ V}, I_D=-0.98\text{ A},$ $R_G=6\ \Omega$	-	5.9	8.8	ns
Rise time	t_r		-	4.4	6.6	
Turn-off delay time	$t_{d(off)}$		-	16.5	24.7	
Fall time	t_f		-	8.5	12.7	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-80\text{ V}, I_D=-0.98\text{ A}, V_{GS}=0\text{ to }-10\text{ V}$	-	1.1	1.4	nC
Gate to drain charge	Q_{gd}		-	4	6	
Gate charge total	Q_g		-	9	12	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	V

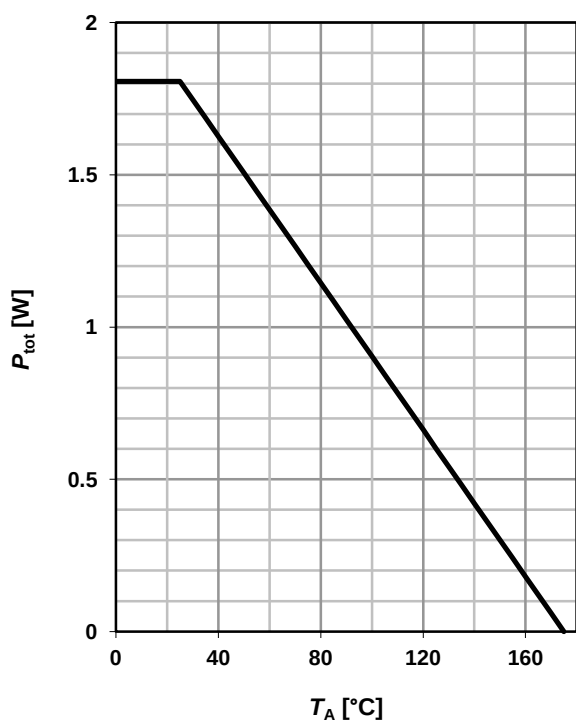
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	-0.98	A
Diode pulse current	$I_{S,pulse}$		-	-	-3.9	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=0.98\text{ A},$ $T_j=25\text{ °C}$	-	0.84	1.2	V
Reverse recovery time	t_{rr}	$V_R=50\text{ V}, I_F= I_S ,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	47	-	ns
Reverse recovery charge	Q_{rr}		-	96	-	nC

²⁾ See figure 16 for gate charge parameter definition

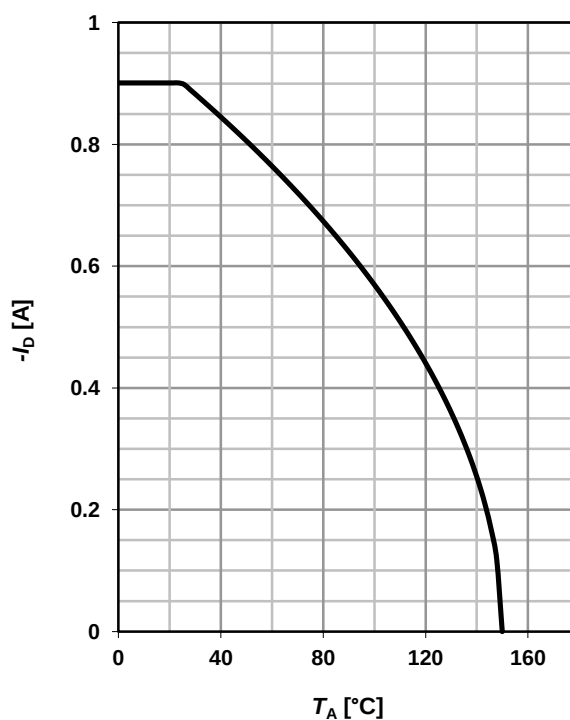
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

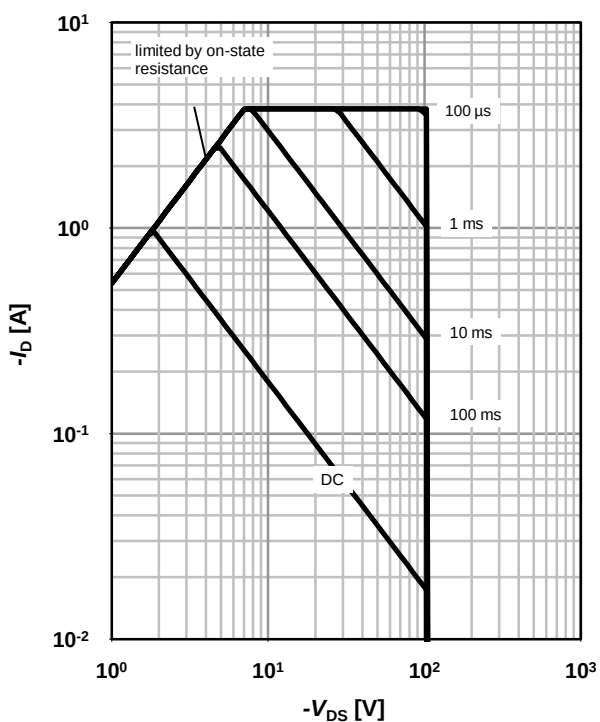
$$I_D = f(T_C); |V_{GS}| \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

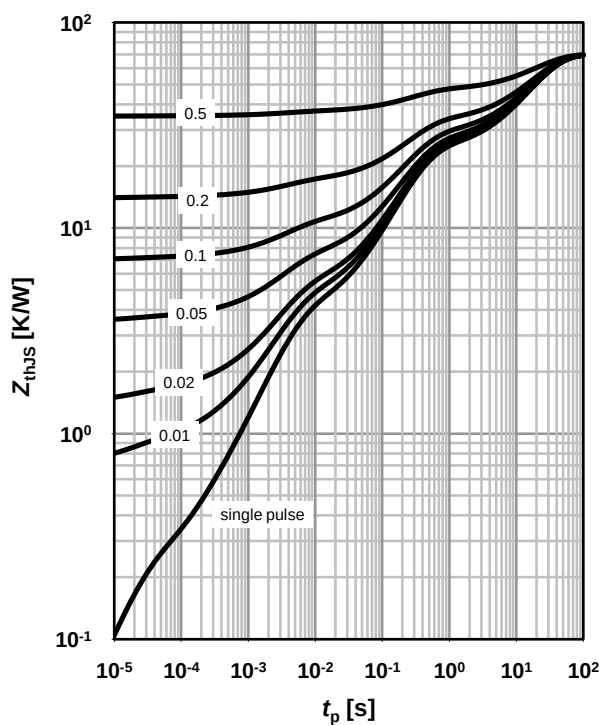
parameter: t_p



4 Max. transient thermal impedance

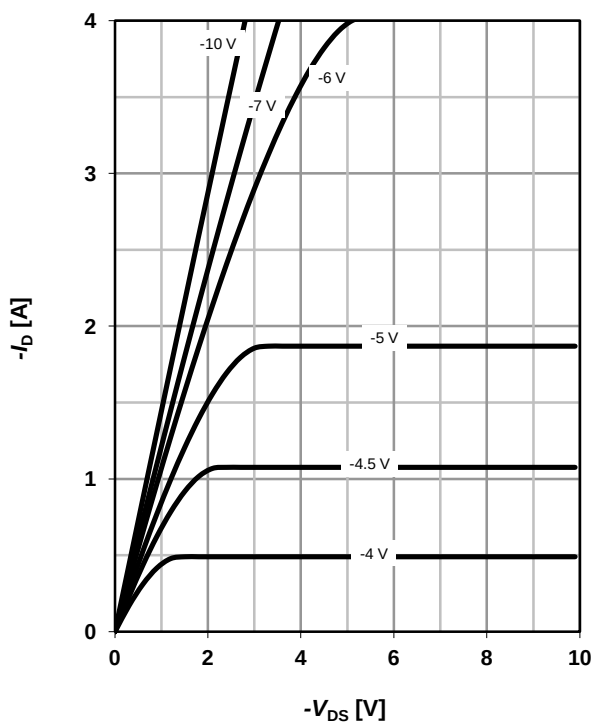
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



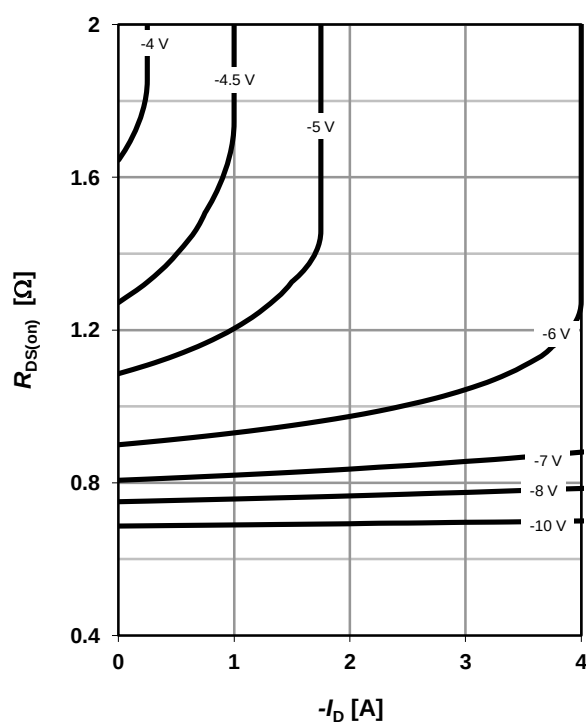
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


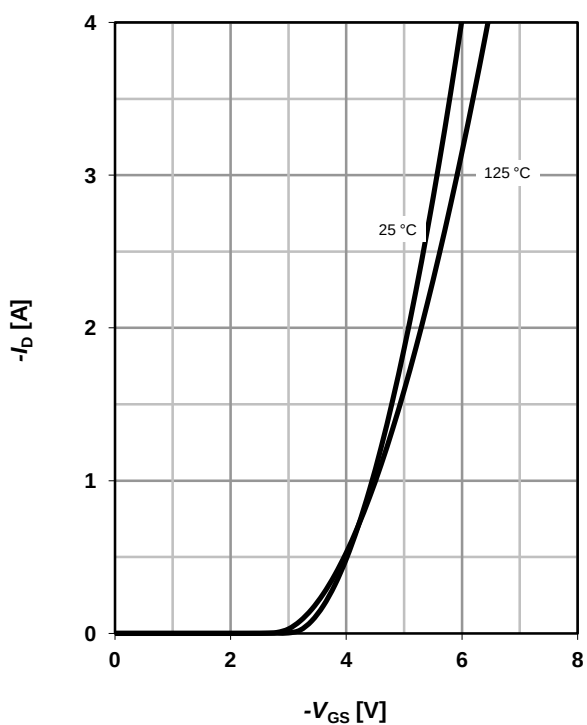
6 Typ. drain-source on resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

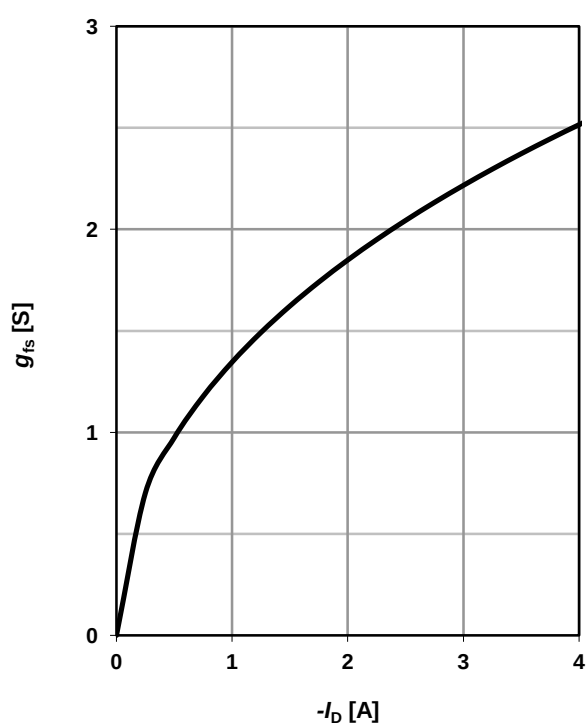
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

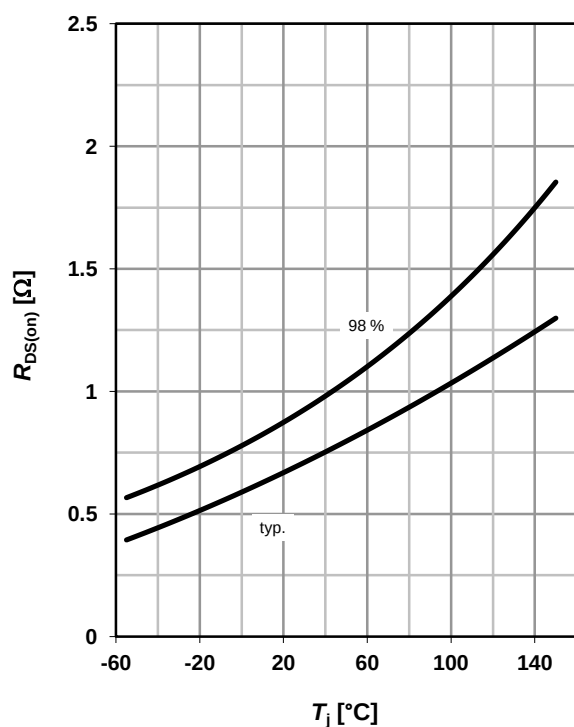
parameter: T_j


8 Typ. forward transconductance

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$


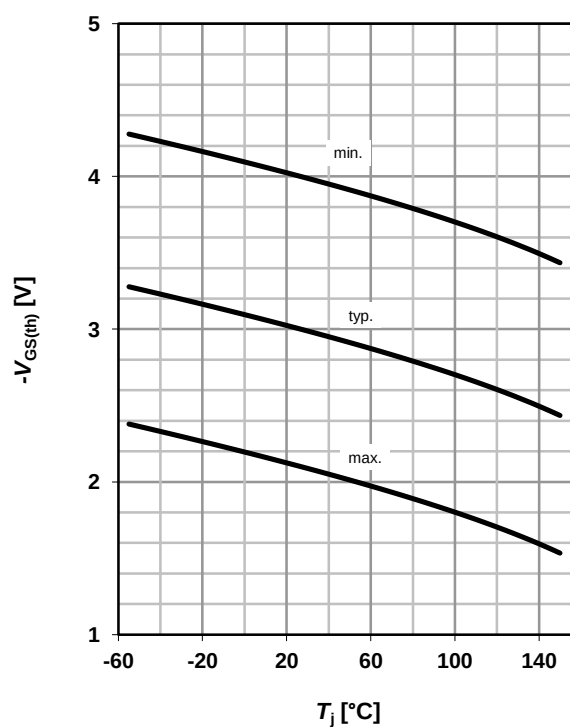
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = -0.98 \text{ A}; V_{GS} = -10 \text{ V}$$



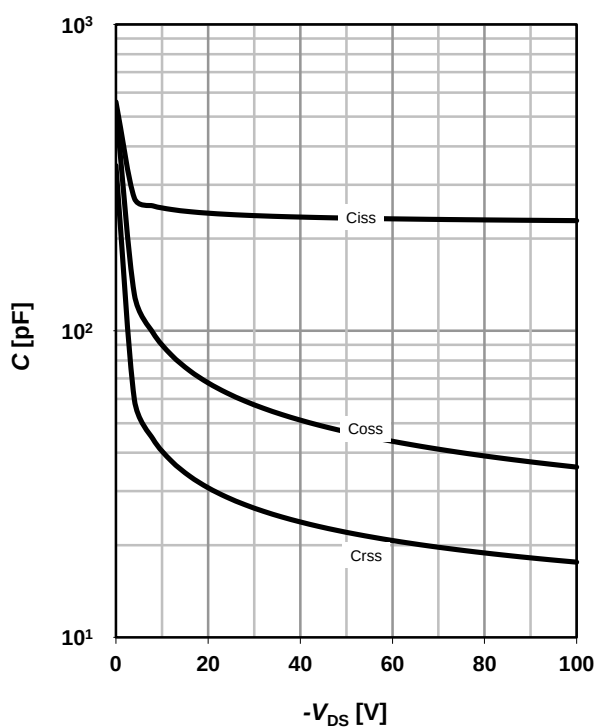
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -380 \text{ μA}$$



11 Typ. capacitances

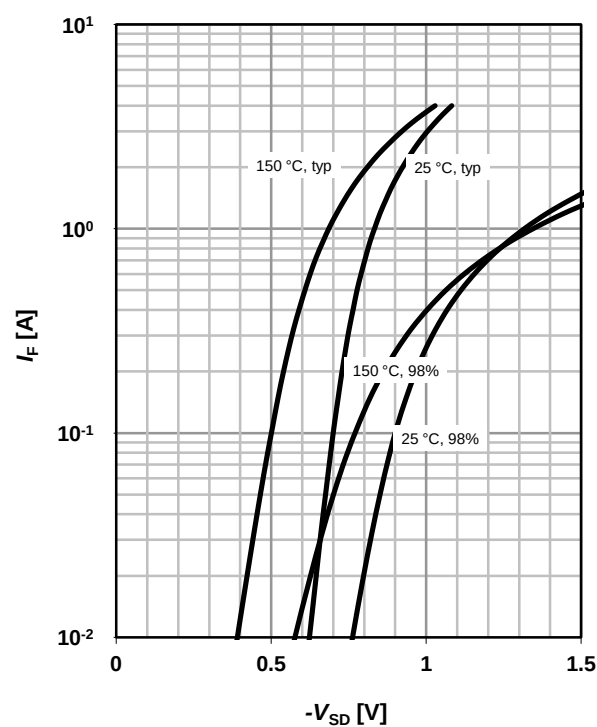
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

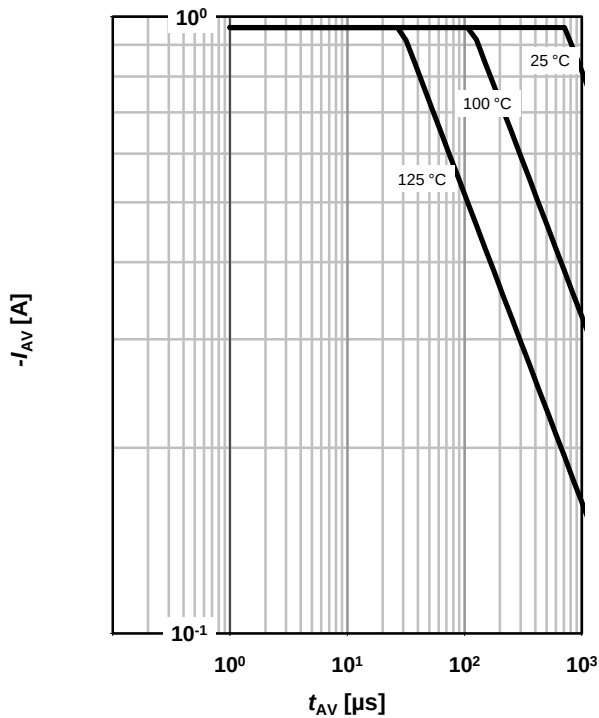
$$I_F = f(V_{SD})$$

parameter: T_j



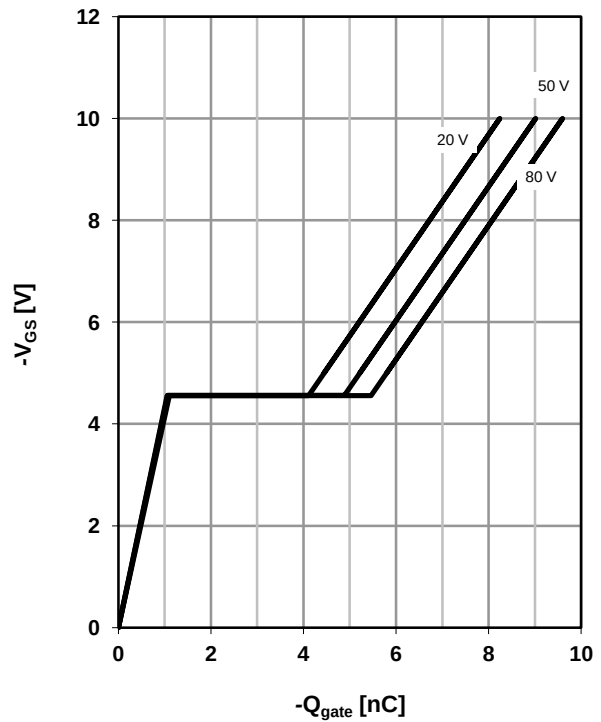
13 Avalanche characteristics

 $I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$

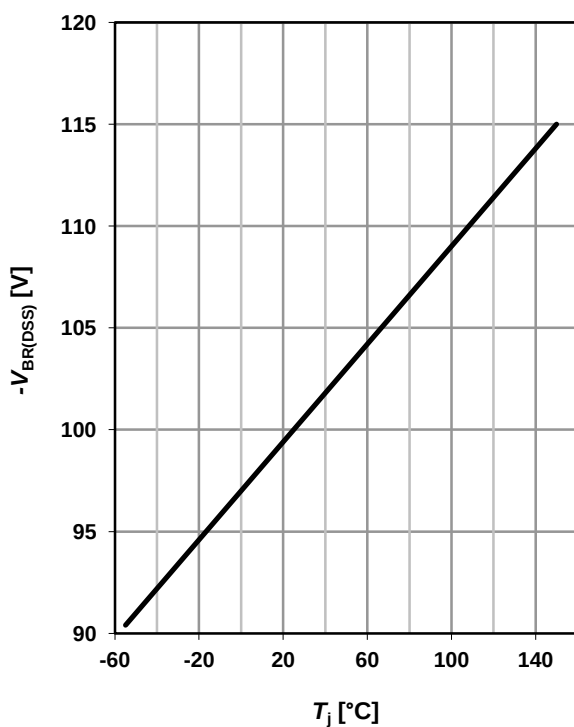
parameter: $T_{j(\text{start})}$


14 Typ. gate charge

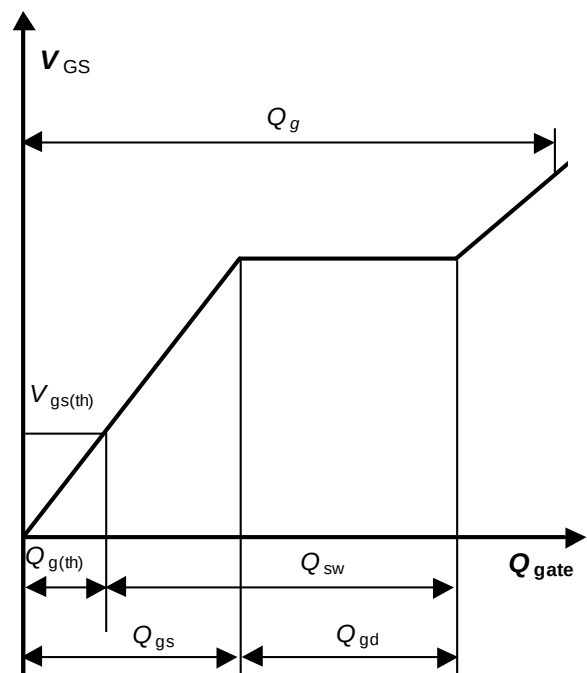
 $V_{GS}=f(Q_{\text{gate}}); I_D=-0.98\ \text{A pulsed}$

parameter: V_{DD}


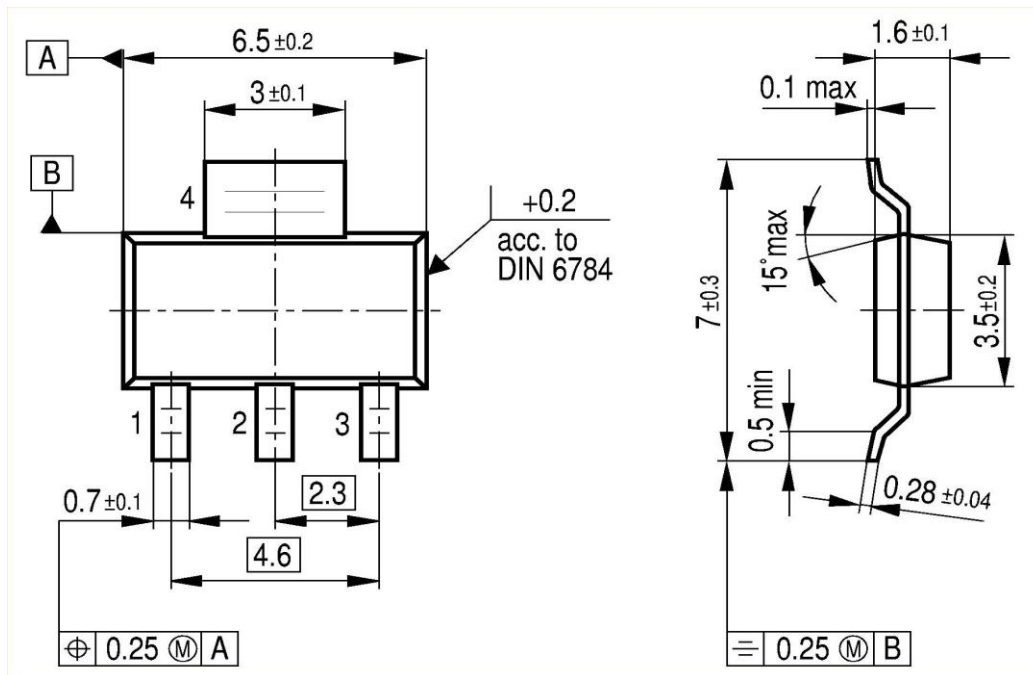
15 Drain-source breakdown voltage

 $V_{BR(DSS)}=f(T_j); I_D=-250\ \mu\text{A}$


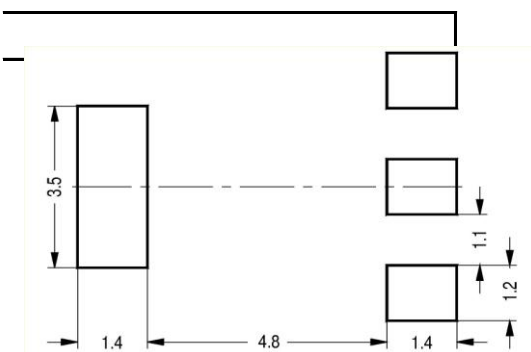
16 Gate charge waveforms



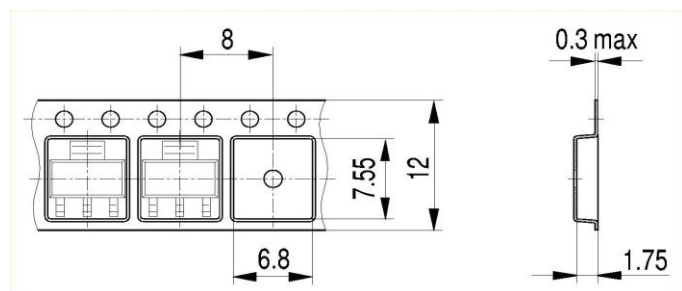
Package Outline: PG-SOT-223



Footprint:



Packaging:



Dimensions in mm

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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