L6738

Single-phase PWM controller with light-load efficiency optimization

Datasheet – production data

Features

- Flexible power supply from 5 V to 12 V bus
- Power conversion input as low as 1.5 V
- Light-load efficiency optimization
- Embedded bootstrap diode
- VIN detector
- 0.8 V internal reference
- 0.5% output voltage accuracy
- Remote GND recovery
- High-current integrated drivers
- Sensorless and programmable precise-OC sense across inductor DCR
- OV protection
- Programmable oscillator up to 600 kHz
- LS-less to manage pre-bias startup
- Adjustable output voltage
- Disable function
- Internal soft-start
- VFQFPN 16 3x3 mm package

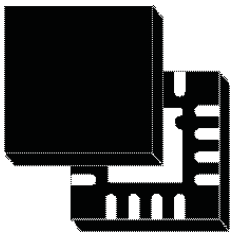
Applications

- Memory and termination supply
- Subsystem power supply (MCH, IOCH, PCI)
- CPU and DSP power supply
- Distributed power supply
- General DC-DC converter

Description

The L6738 is a single-phase step-down controller with integrated high-current drivers that provides complete control logic and protection to realize a DC-DC converter.

The device flexibility allows the management of conversions with power input V_{IN} as low as 1.5 V and the device supply voltage ranging from 5 V to 12 V bus.



VFQFPN16

The L6738 features a proprietary algorithm that allows light-load efficiency optimization, boosting efficiency without compromising the output voltage ripple.

The integrated 0.8 V reference allows the generation of output voltages with ±0.5% accuracy over line and temperature variations.

The oscillator is programmable up to 600 kHz.

The L6738 provides a programmable dual-level overcurrent protection and overvoltage protection. The current information is monitored across the inductor DCR.

The L6738 is available in a VFQFPN 16 3x3 mm package.

Table 1. Device summary

Order code	Package	Packing
L6738	VFQFPN16	Tube
L6738TR	VFQFPN16	Tape and reel

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1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical application circuit (fast protection)

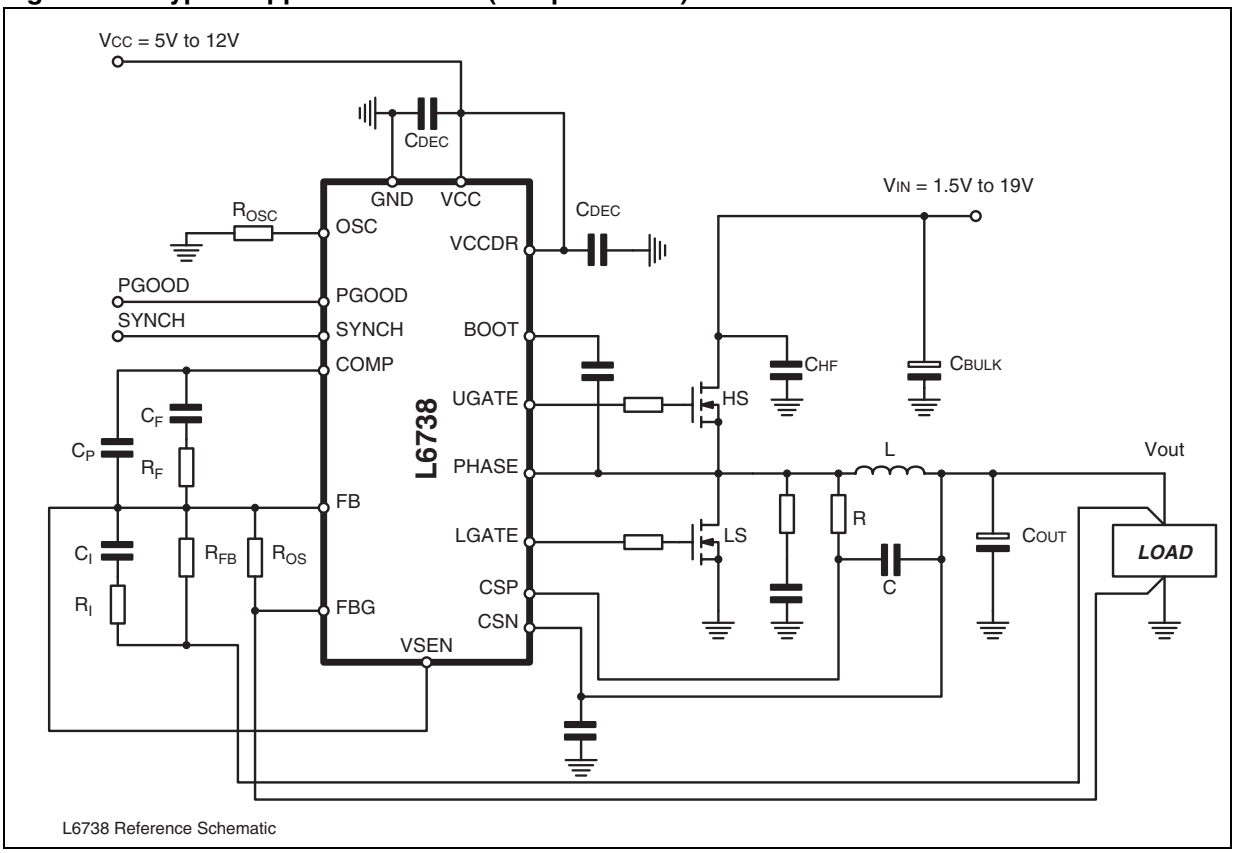
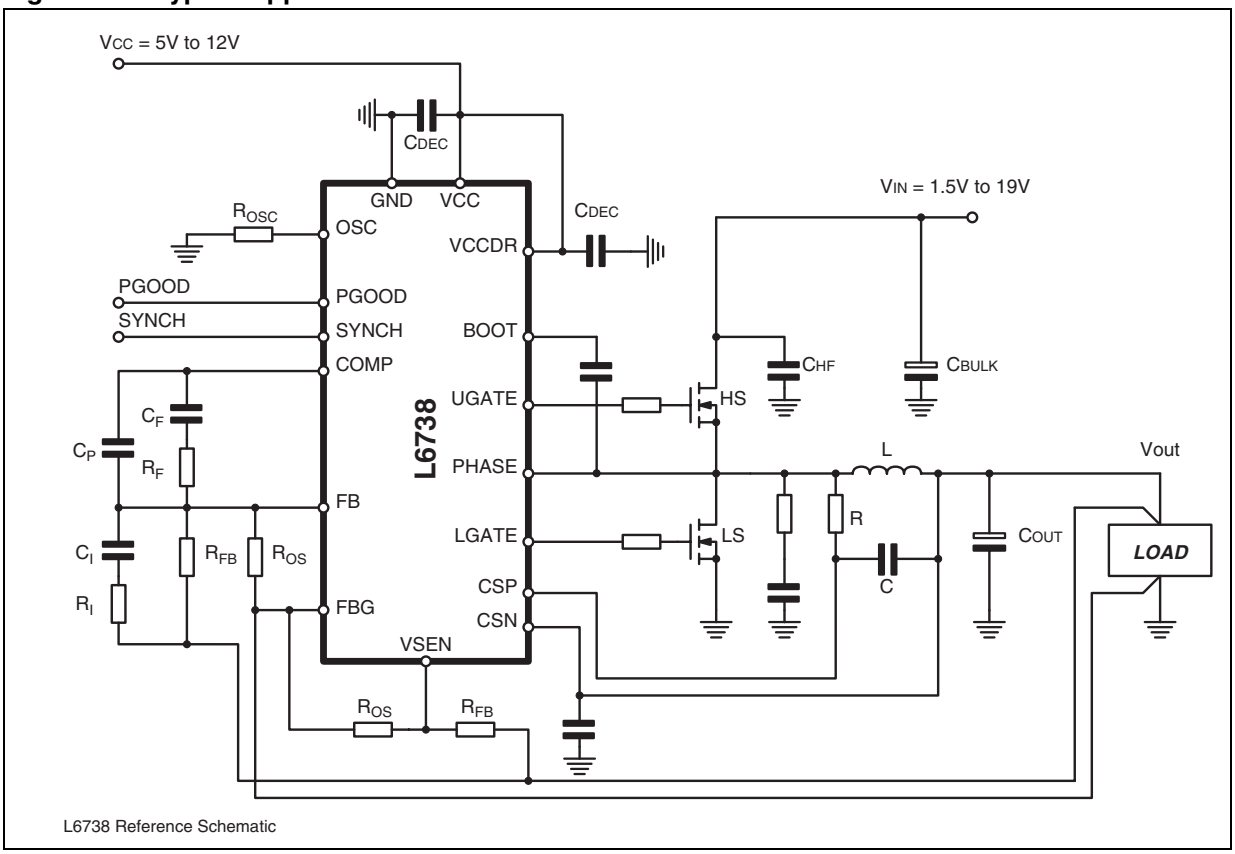
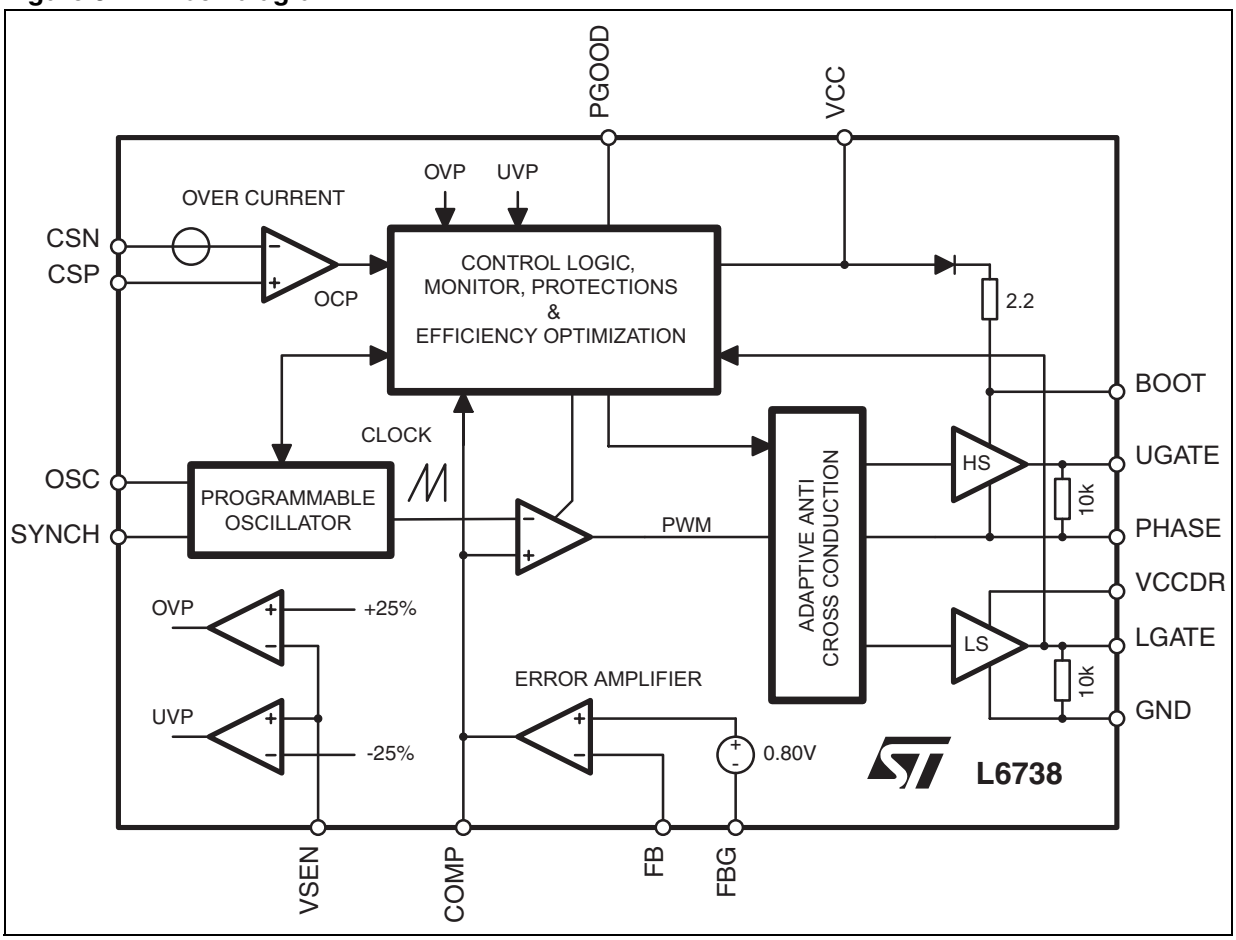


Figure 2. Typical application circuit



1.2 Block diagram

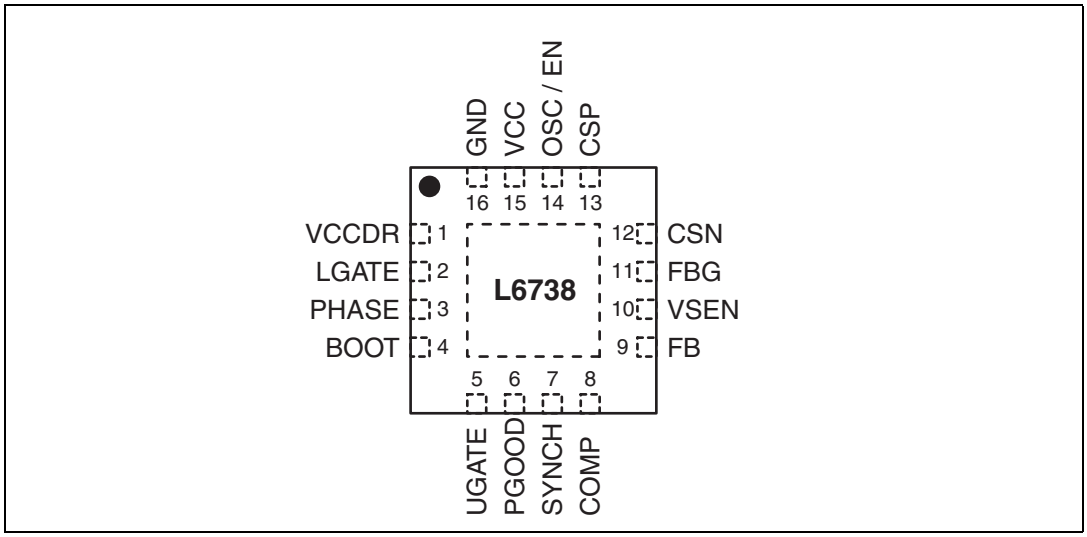
Figure 3. Block diagram



2 Connection diagram and pin description

2.1 Connection diagram

Figure 4. Pin connection (top view)



2.2 Pin description

Table 2. Pin description

Pin#	Name	Function
1	VCCDR	Low-side driver section power supply. Operative voltage is 5 V to 12 V bus. Filter with 1 µF MLCC to GND.
2	LGATE	Low-side driver output. Connect directly to the low-side MOSFET gate. A small series resistor can be useful to reduce dissipated power especially in high frequency applications.
3	PHASE	High-side driver return path. Connect to the high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
4	BOOT	High-side driver supply. This pin supplies the high-side floating driver. Connect through the C_{BOOT} capacitor to the PHASE pin. The pin is internally connected through a boot diode to the VCCDR pin. A 2.2 Ohm series resistor is also provided. See *Section 8* for a guide to designing the capacitor value.
5	UGATE	High-side driver output. Connect to high-side MOSFET gate. A small series resistor may help in reducing the PHASE pin negative spike as well as cooling the device.

Table 2. Pin description (continued)

Pin#	Name	Function
6	PGOOD	Power good. It is an open-drain output set free after SS (with 3x clock cycle delay) as long as the output voltage monitored through VSEN is within specifications. Pull up to 3.3 V (typ.) or lower, if not used it can be left floating.
7	SYNCH	Synchronization pin. The controller synchronizes on the falling edge of a square wave provided to this pin. Short to GND if not used. See *Section 7.1* for details.
8	COMP	Error amplifier output. Connect with an R_F - C_F to FB. The device cannot be disabled by grounding this pin.
9	FB	Error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an R_F - C_F to COMP.
10	VSEN	Output voltage monitor. It manages OVP and UVP protections and PGOOD. Connect to the positive side of the load for remote sensing. See *Section 6* for details.
11	FBG	Remote ground sense. Connect to the negative side of the load for remote sensing.
12	CSN	Current sense negative input. Connect to the output side of the main inductor. Filter with 100 nF (typ.) to GND.
13	CSP	Current sense positive input. Connect through an R-C filter to the phase side of the main inductor.
14	OSC / EN	OSC: internally set to 1.24 V, it allows the programming of the switching frequency F_{SW} of the device. Switching frequency can be increased according to the resistor R_{OSC} connected to SGND with a gain of 10 kHz/µA (see *Section 7* for details). If floating, the switching frequency is 200 kHz. EN: pull low to disable the device (also protection latch reset).
15	VCC	Device power supply. The embedded bootstrap diode is internally connected to this pin. Operative voltage is 5 V to 12 V bus. Filter with 1 mF MLCC to GND. For proper operation, VCC needs to be >1.5 V higher than the programmed V_{OUT}.
16	GND	All internal references, logic and driver return path are referenced to this pin. Connect to the PCB GND ground plane and filter to VCC and VCCDR.
	Thermal PAD	The thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Use VIAs to connect to the PGND plane.

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction-to-ambient (device soldered on 2s2p PC board)	45	°C/W
R_{THJC}	Thermal resistance junction to case	1	°C/W

Table 3. Thermal data (continued)

Symbol	Parameter	Value	Unit
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC},V_{CCDR}	to GND	-0.3 to 15	V
V_{BOOT}, V_{UGATE}	to GND to PHASE to GND, VCCDR = 12 V, t < 200 nsec.	-0.3 to 41 15 45	V
V_{PHASE}	to GND to GND, VCCDR = 12 V, t < 200 nsec.	-5 to 26 -8 to 30	V
V_{LGATE}	to GND	-0.3 to VCCDR + 0.3	V
SYNCH	to GND, VCC < 7 V to GND, VCC > 7 V	-0.3 to VCC + 0.3 -0.3 to 7	V
CSP, CSN	to GND(1)	-0.3 to VCC - 1.5	V
	All other pins to GND	-0.3 to 3.6	V

1. The current sense network needs to be properly biased and loop closed.

3.2 Electrical characteristics

(V_{CC} = 5 V to 12 V; T_j = 0 to 70 °C unless otherwise specified.)

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current			9		mA
		EN = GND		8		mA
I_{CCDR}	VCCDR supply current	UGATE and LGATE = open		2.6	5	mA
		EN = GND UGATE and LGATE = open		0.3	3.8	mA
$UVLO_{VCC}$, $UVLO_{VCCDR}$	Turn-on threshold	VCC, VCCDR rising			4.1	V
	Hysteresis			0.2		V
Oscillator, synchronization, and soft-start						
F_{SW}	Main oscillator accuracy	OSC = open	180	200	220	kHz
k_{OSC}	Oscillator gain	Current sink/source from OSC		10		kHz/µA
DIS	Disable threshold	OSC falling			0.5	V
Tss	Soft-start time	OSC = open	4.5	5.12	5.7	msec
Tssdelay	SS delay	OSC = open, before SS	4.5	5.12	5.7	msec
ΔV_{OSC}	PWM ramp amplitude			2		V
d	Duty cycle		0		100	%
SYNCH	Synchronization input	V_{IL}			1.0	V
		V_{IH}	2.5			V
Reference and error amplifier						
	Output voltage accuracy	Vout to FBG	-0.5	-	0.5	%
A_0	DC gain(1)			120		dB
GBWP	Gain-bandwidth product(1)			15		MHz
SR	Slew rate(1)			8		V/µs
Gate driver						
I_{UGATE}	HS source current(1)	BOOT - PHASE = 12 V; C_{UGATE} to PHASE = 3.3 nF		2		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 12 V; 100 mA		2	2.5	Ω
I_{LGATE}	LS source current(1)	C_{LGATE} to GND = 5.6 nF		3		A
R_{LGATE}	LS sink resistance	100 mA		1	1.5	Ω
Current sense amplifier						
V_{OCTH}	OC current threshold	CSP - CSN; 7x masking	17	20	23	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PGOOD and protection						
PGOOD	OVP threshold	VSEN rising	0.970	1.000	1.030	V
		Un-latch, VSEN falling	0.350	0.400	0.450	V
	UVP threshold	VSEN falling	0.570	0.600	0.630	V

1. Guaranteed by design, not subject to test.

4 Device description and operation

The L6738 is a single-phase PWM controller with embedded high-current drivers that provides complete control logic and protection to realize a general DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, with its high level of integration, this 16-pin device allows a reduction of cost and size of the power supply solution and also provides real-time PGOOD in a compact VFQFPN16 3x3 mm.

The L6738 is designed to operate from a 5 V or 12 V supply. The output voltage can be precisely regulated to as low as 0.8 V with ±0.5% accuracy over line and temperature variations. The controller performs remote GND recovery to prevent losses and GND drops to affect the regulation.

The switching frequency is internally set to 200 kHz and adjustable through the OSC pin. The IC can be disabled by pulling the OSC pin low.

The L6738 provides a simple control loop with a voltage-mode error amplifier. The error amplifier features a 15 MHz gain-bandwidth product and 8 V/µs slew rate, allowing high regulator bandwidth for fast transient response.

To avoid load damages, the L6738 provides overcurrent protection, and overvoltage and undervoltage protection. The overcurrent trip threshold is monitored through the inductor DCR, assuring optimum precision, saving the use of an expensive and space-consuming sense resistor. The output voltage is monitored through the dedicated VSEN pin.

The L6738 implements soft-start by increasing the internal reference in closed loop regulation. The low-side-less feature allows the device to perform the soft-start over pre-biased output avoiding high-current return through the output inductor and dangerous negative spikes at the load side.

The device features a unique synchronization feature that allows the reduction of the input capacitor RMS current resulting in a cheap and cost-effective system design.

The L6738 is available in a compact VFQFN16 3x3 mm package with exposed pad.

5 Soft-start

The L6738 implements a soft-start to smoothly charge the output filter avoiding the requirement of high in-rush currents to the input power supply. During this phase, the device increases the internal reference from zero up to 0.8 V in closed loop regulation. The soft-start is implemented only when VCC and VCCDR are above their own UVLO threshold and the EN pin is set free. When SS takes place, the IC initially waits for 1024 clock cycles and then starts ramping up the reference in 1024 clock cycles in closed-loop regulation. At the end of the digital soft-start, the PWRGOOD signal is set free with 3x clock cycles delay.

Protections are active during this phase, as follows:

- undervoltage is enabled when the reference voltage reaches 80% of the final value
- overvoltage is always enabled
- FB disconnection is enabled.

Soft-start time depends on the programmed frequency, initial delay and reference ramp-up lasts for 1024 clock cycles. SS time and initial delay can be determined as follows:

Equation 1

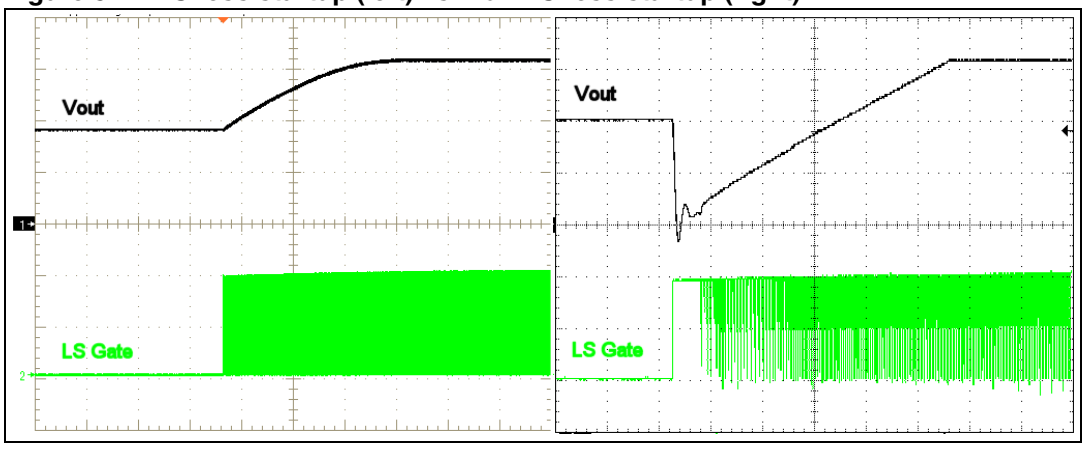
$$T_{SS}[ms] = \frac{1024}{Fsw[kHz]]}$$

5.1 LS-less startup

In order to avoid any kind of negative undershoot on the load side during startup, the L6738 performs a special sequence in enabling the drivers for both sections: during the soft-start phase, the LS MOSFET is kept OFF until the first PWM pulse. This particular sequence avoids the dangerous negative spike on the output voltage that can occur if starting over a pre-biased output.

Low-side MOSFET turn-on is masked only from the control loop point of view: protections are still allowed to turn on the low-side MOSFET in the case of overvoltage, if needed.

Figure 5. LS-less startup (left) vs. non-LS-less startup (right)



6 Output voltage setting and protections

The L6738 is capable of precisely regulating an output voltage as low as 0.8 V. In fact, the device comes with a fixed 0.8 V internal reference that guarantees the output regulated voltage to be within ±0.5% tolerance over line and temperature variations (excluding output resistor divider tolerance, when present).

Output voltage higher than 0.8 V can be easily achieved by adding a resistor R_{OS} between the FB pin and ground. Referring to *Figure 1*, the steady-state DC output voltage is:

Equation 2

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

where V_{REF} is 0.8 V.

The L6738 monitors the voltage at the VSEN pin and compares it to the internal reference voltage in order to provide undervoltage and overvoltage protection, as well as PGOOD signal. According to the level of VSEN, different actions are performed from the controller:

- PGOOD

  If the voltage monitored through VSEN exits from the PGOOD window limits, the device de-asserts the PGOOD signal. PGOOD is asserted at the end of the soft-start phase with 3x clock cycles delay.
- Undervoltage protection (UV)

  If the voltage at the VSEN pin drops below the UV threshold, the device turns off both HS and LS MOSFETs, latching the condition. Cycle VCC or EN to recover. UV is also active during SS acting as VIN detection protection. See description below.
- Overvoltage protection (OV)

  If the voltage at the VSEN pin rises over the OV threshold, overvoltage protection turns off the HS MOSFET and turns on the LS MOSFET. The LS MOSFET is turned off as soon as VSEN goes below Vref/2. The condition is latched, cycle VCC/EN to recover. Note that, even if the device is latched, the device still controls the LS MOSFET and can switch it on whenever VSEN rises above the OV threshold.
- PreOVP protection

  Monitors VSEN when IC is disabled. If VSEN surpasses the OV threshold, IC turns on the low-side MOSFET to protect the load. On the EN rising edge, the protection is disabled and the IC implements the SS procedure. PreOVP is disabled when EN is high but the OV protection becomes operative.
- VIN detection

  UV protection active during SS allows the IC to detect whether input voltage VIN is present. If UV is triggered during the soft-start, it resets the SS procedure: the controller re-implements the initial delay and re-ramps-up the reference with the same SS timings described in *Section 5*. The UV protection then avoids that IC starts up if VIN is not present.

Protections are active also during soft-start (see *Section 5*).

For proper operations, VCC needs to be at least 1.5 V higher than the programmed output voltage.

Table 6. L6738 protection at a glance

L6738	Comments
Overvoltage (OV)	VSEN = +25% above reference. ***Action:*** IC latch; LS=ON until VSEN = 50% of Vref; PGOOD = GND. ***Action (EN=0):*** IC latch; LS=ON; reset by EN rising edge (PreOVP).
Undervoltage (UV)	VSEN = -25% below reference. ***Action:*** IC latch; HiZ; PGOOD = GND. ***Action (SS):*** SS reset (VIN detection).
PGOOD	PGOOD is set to zero whenever VSEN falls outside +/-25% of Vref. ***Action:*** PGOOD transition coincides with OV/UV protection set.
Overcurrent (OC)	Current monitor across inductor DCR. ***Action:*** 1st threshold (20 mV): IC latch after 7 consecutive constant current events.

6.1 Overcurrent

The overcurrent function protects the converter from a shorted output or overload, by sensing the output current information across the inductor DCR. This method reduces costs and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The inductor DCR current sense is implemented by comparing and monitoring the difference between the CSP and CSN pins. If the monitored voltage is bigger than the internal thresholds, an overcurrent event is detected.

DCR current sensing requires time constant matching between the inductor and the reading network:

Equation 3

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad V_{CSP\text{-}CSN} = DCR \cdot I_{OUT}$$

The L6738 monitors the voltage between CSP and CSN, when this voltage exceeds the OC threshold, an overcurrent is detected. The IC works in constant current mode, turning on the low-side MOSFET immediately while the OC persists and, in any case, until the next clock cycle. After seven consecutive OC events, overcurrent protection is triggered and the IC latches.

When overcurrent protection is triggered, the device turns off both LS and HS MOSFETs in a latched condition.

To recover from an overcurrent protection triggered condition, VCC power supply or EN must be cycled.

For proper current reading, the CSN pin must be filtered by 100 nF (typ.) MLCC to GND.

6.2 Overcurrent threshold setting

The L6738 detects OC when the difference between CSP and CSN is equal to 20 mV (typ.). By properly designing the current reading network, it is possible to program the OC threshold as desired (see *Figure 6*).

Equation 4

$$I_{OCP} = \frac{20mV}{DCR} \cdot \frac{R1 + R2}{R2}$$

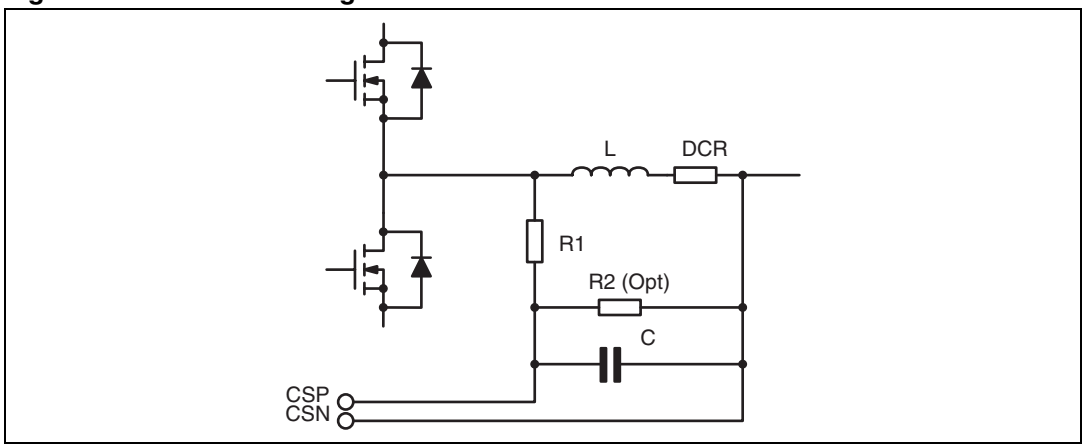
Time constant matching is, in this case, designed considering:

Equation 5

$$\frac{L}{DCR} = (R1 // R2) \cdot C$$

This means that once the inductor has been chosen, the two conditions above define the proper values for R1 and R2.

Figure 6. Current reading network



7 Main oscillator

The controller embeds a programmable oscillator. The internal oscillator generates the sawtooth waveform for the PWM charging with a constant current and resets an internal capacitor. The switching frequency, F_{SW}, is internally fixed at 200 kHz.

The current delivered to the oscillator is typically 20 µA (corresponding to the free running frequency F_{SW} = 200 kHz) and it may be varied using an external resistor (R_{OSC}) typically connected between the OSC pin and GND. As the OSC pin is fixed at 1.240 V, the frequency is varied proportionally to the current sunk from the pin considering the internal gain of 10 KHz/µA (see *Figure 7*).

Connecting R_{OSC} to GND, the frequency is increased (current is sunk from the pin), according to the following relationships:

Equation 6

$$F_{SW} = 200kHz + \frac{1.240V}{R_{OSC}} \cdot 10\frac{kHz}{\mu A}$$

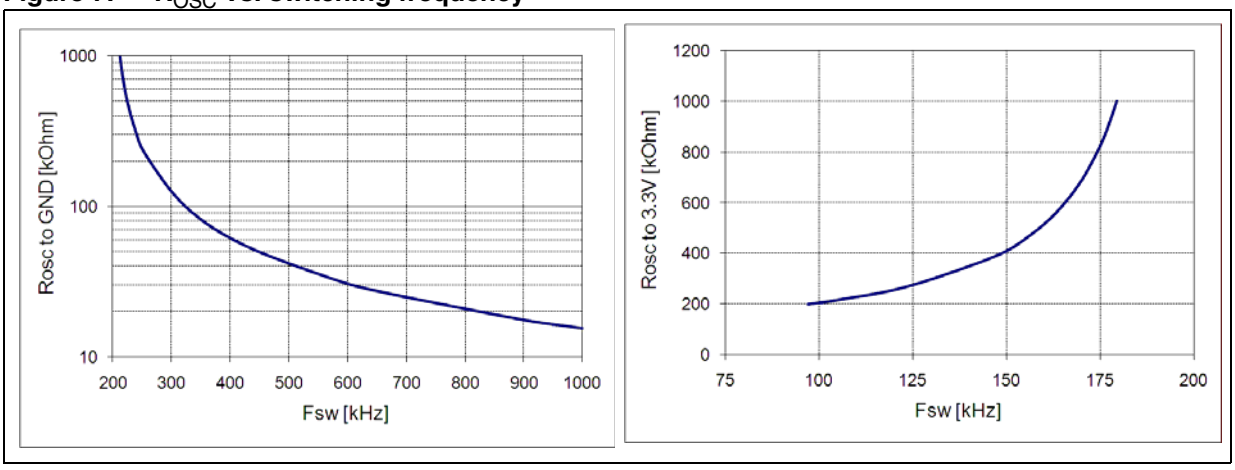
Connecting R_{OSC} to a positive voltage, the frequency is reduced (current is forced into the pin), according to the following relationships:

Equation 7

$$F_{SW} = 200kHz - \frac{+V - 1.240}{R_{OSC}} \cdot 10\frac{kHz}{\mu A}$$

where +V is the positive voltage to which the R_{OSC} resistor is connected.

Figure 7. R_{OSC} vs. switching frequency



7.1 Synchronization

The L6738 provides the user with the possibility to synchronize with an external signal when properly connected to the SYNCH pin. Synchronization allows different converters to share the same input filter reducing the resulting IRMS and so reducing the total capacitor count required to sustain the load. Furthermore, synchronized systems generally exhibit higher noise immunity and better regulation.

The device synchronizes the high-side MOSFET turn-on with the falling-edge of the synch signal locking the internal sawtooth generator to the external signal.

8 High-current embedded drivers

The L6738 provides high-current driving control. The driver for the high-side MOSFET uses the BOOT pin for supply and the PHASE pin for return. The driver for the low-side MOSFET uses the VCCDR pin for supply and the GND pin for return.

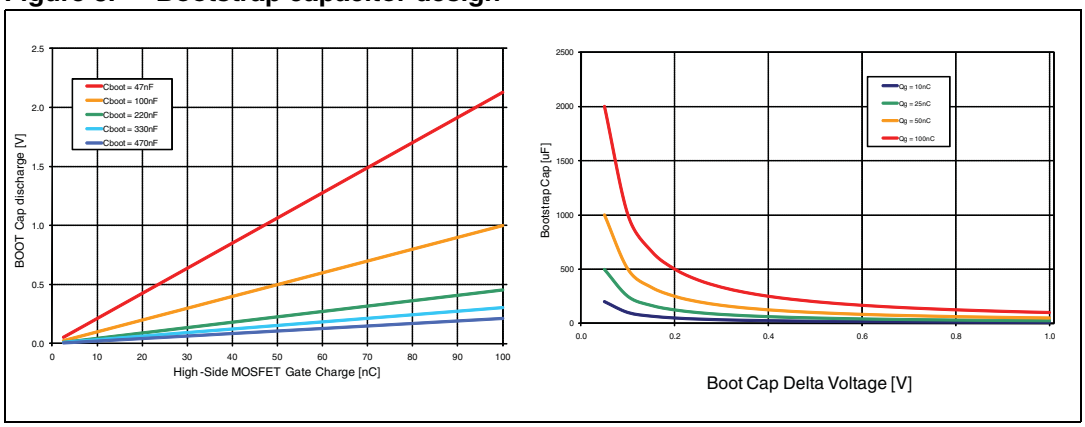
The embedded driver embodies an anti-shoot-through and adaptive dead-time control to minimize the low-side body diode conduction time maintaining good efficiency and saving the use of Schottky diodes: when the high-side MOSFET turns off, the voltage on its source begins to fall; when the voltage reaches about 2 V, the low-side MOSFET gate drive voltage is suddenly applied. When the low-side MOSFET turns off, the voltage at the LGATE pin is sensed. When it drops below about 1 V, the high-side MOSFET gate drive voltage is suddenly applied. If the current flowing in the inductor is negative, the source of the high-side MOSFET never drops. To allow the low-side MOSFET to turn on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low-side MOSFET is switched on, so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

8.1 Boot capacitor design

The bootstrap capacitor needs to be designed in order to show a negligible discharge due to the high-side MOSFET turn on. In fact, it must give a stable voltage supply to the high-side driver during the MOSFET turn-on, also minimizing the power dissipated by the embedded boot diode. *Figure 8* gives some guidelines on how to select the capacitance value for the bootstrap according to the desired discharge and depending on the selected MOSFET.

To prevent extra-charge of the bootstrap capacitor, as a consequence of large negative spikes, an internal 2.2 Ohms series resistance R_{BOOT} is provided in series to the BOOT diode pin.

Figure 8. Bootstrap capacitor design



8.2 Power dissipation

It is important to consider the power that the device is going to dissipate in driving the external MOSFETs in order to avoid surpassing the maximum junction operative temperature.

Two main terms contribute to the device power dissipation: bias power and driver power.

- Bias power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follows:

Equation 8

$$P_{DC} = V_{CC} \cdot I_{CC} + V_{VCCDR} \cdot I_{VCCDR}$$

- Driver power is the power needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW}, dissipated to switch the MOSFETs, is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined in order to calculate the device power dissipation.

  The total power dissipated to switch the MOSFETs for each phase featuring an embedded driver results:

Equation 9

$$P_{SW} = F_{SW} \cdot (Q_{GHS} \cdot VCCDR + Q_{GLS} \cdot VCCDR)$$

where Q_{GHS} is the total gate charge of the HS MOSFETs and Q_{GLS} is the total gate charge of the LS MOSFETs.

9 Application details

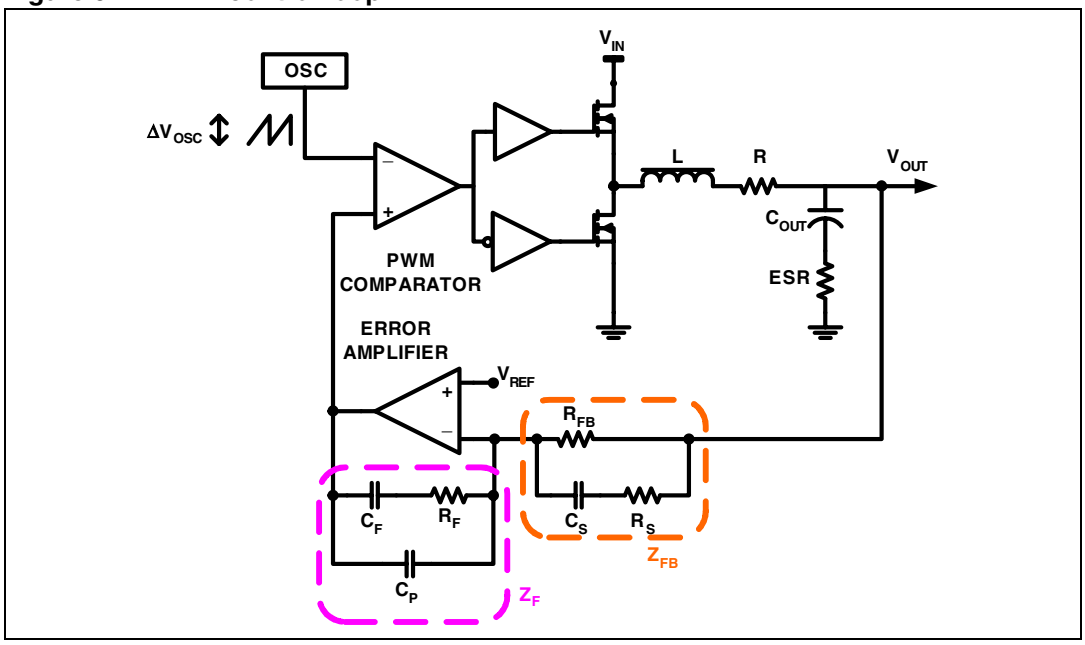
9.1 Compensation network

The control loop shown in *Figure 9* is a voltage-mode control loop. The output voltage is regulated to the internal reference (when present, an offset resistor between FB node and GND can be neglected in control loop calculation).

Error amplifier output is compared to the oscillator sawtooth waveform to provide a PWM signal to the driver section. The PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR} depending on the output capacitor ESR. The DC gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Figure 9. PWM control loop



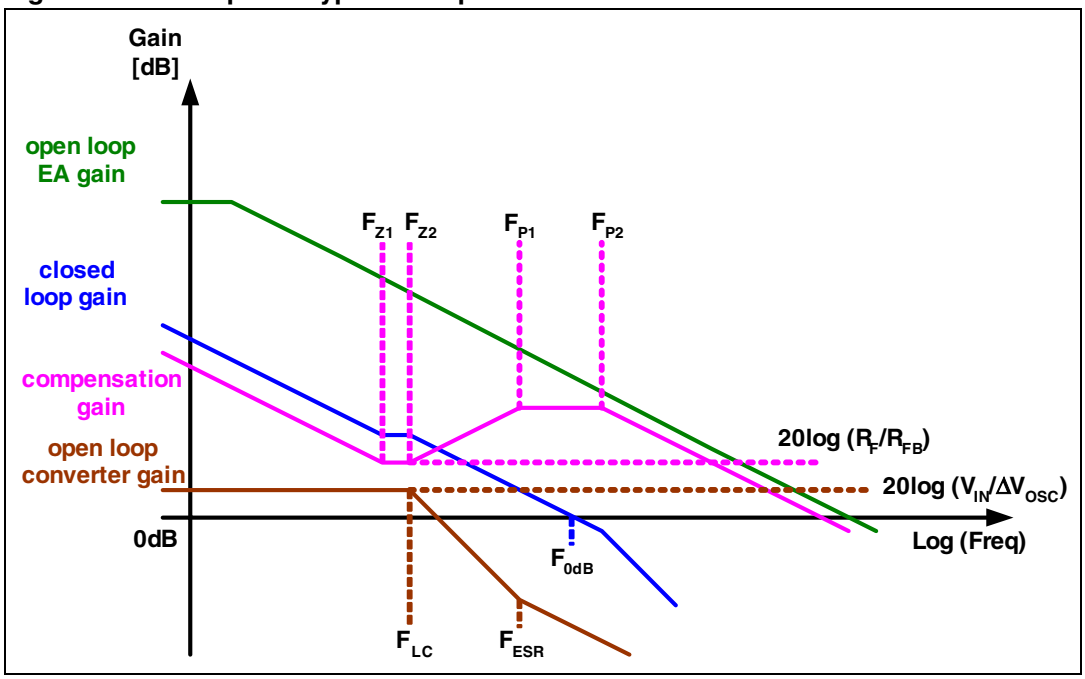
The compensation network closes the loop joining V_{OUT} and EA output with transfer function ideally equal to $-Z_F / Z_{FB}$.

The compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performance and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

High DC gain is achieved giving an integrator shape to the compensation network transfer function. Loop bandwidth (F_{0dB}) can be fixed choosing the right R_F/R_{FB} ratio, however, for stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain must cross the 0dB axis with -20 dB/decade slope.

For example, *Figure 10* shows an asymptotic Bode plot of a Type III compensation.

Figure 10. Example of Type III compensation



- Open loop converter singularities:

Equation 10

a) $$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$$

b) $$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

- Compensation network singularity frequencies:

Equation 11

a) $$F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

b) $$F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$$

c) $$F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$$

d) $$F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$$

To place the poles and zeros of the compensation network, the following suggestions may be followed:

a) Set the gain R_F/R_{FB} in order to obtain the desired closed loop regulator bandwidth according to the approximated formula (suggested values for R_{FB} are in the range of some kΩ):

Equation 12

$$\frac{R_F}{R_{FB}} = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}}$$

b) Place F_{Z1} below F_{LC} (typically $0.5*F_{LC}$):

$$C_F = \frac{1}{\pi \cdot R_F \cdot F_{LC}}$$

c) Place F_{P1} at F_{ESR}:

$$C_P = \frac{C_F}{2\pi \cdot R_F \cdot C_F \cdot F_{ESR} - 1}$$

d) Place F_{Z2} at F_{LC} and F_{P2} at half of the switching frequency:

$$R_S = \frac{R_{FB}}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_S = \frac{1}{\pi \cdot R_S \cdot F_{SW}}$$

e) Check that compensation network gain is lower than open loop EA gain before F_{0dB}

f) Check phase margin obtained (it should be greater than 45°) and repeat if necessary.

9.2 Layout guidelines

The L6738 provides control functions and a high-current integrated driver to implement high-current step-down DC-DC converters. In this kind of application, a good layout is very important.

The first priority of component placement for these applications must be reserved for the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) power connections (highlighted in *Figure 11*) must be a part of a power plane and realized by wide and thick copper traces: loop must be minimized. The critical components, i.e. the Power MOSFETs, must be close to one another. The use of a multi-layer printed circuit board is recommended.

The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, must be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCCs are recommended to be connected near the HS drain.

Use a proper number of vias when power traces must move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the

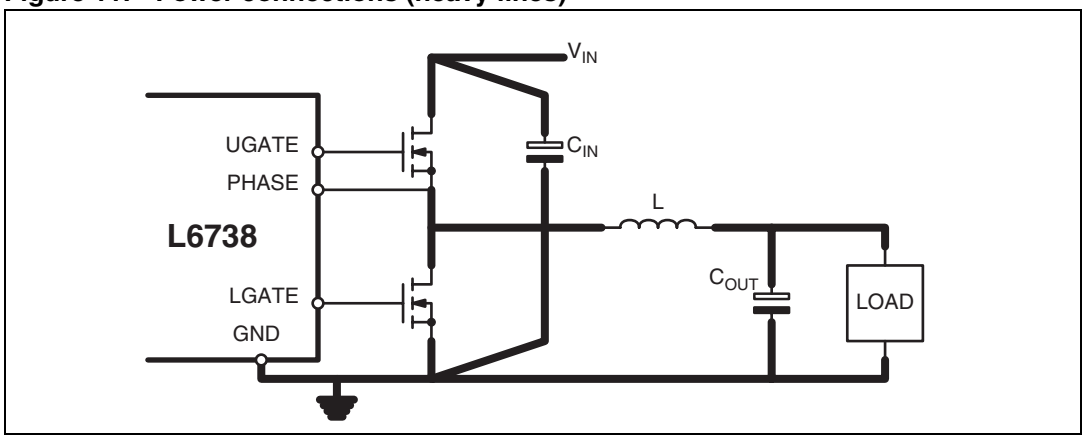
same high-current trace on more than one PCB layer reduces the parasitic resistance associated to that connection.

Connect output bulk capacitors (C_{OUT}) as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace, also adding extra de-coupling capacitors along the way to the load when this results in being far from the bulk capacitors bank.

Remote sense connection must be routed as parallel nets from the FBG/VSEN pins to the load in order to avoid the pick-up of any common mode noise. Connecting these pins in points far from the load causes a non-optimum load regulation, increasing output tolerance.

Locate current reading components close to the device. The PCB traces connecting the reading point must use dedicated nets, routed as parallel traces in order to avoid the pick-up of any common mode noise. It's also important, to avoid any offset in the measurement and obtain better precision, to connect the traces as close as possible to the sensing elements. A small filtering capacitor can be added, near the controller, between V_{OUT} and GND, on the CSN line to allow higher layout flexibility.

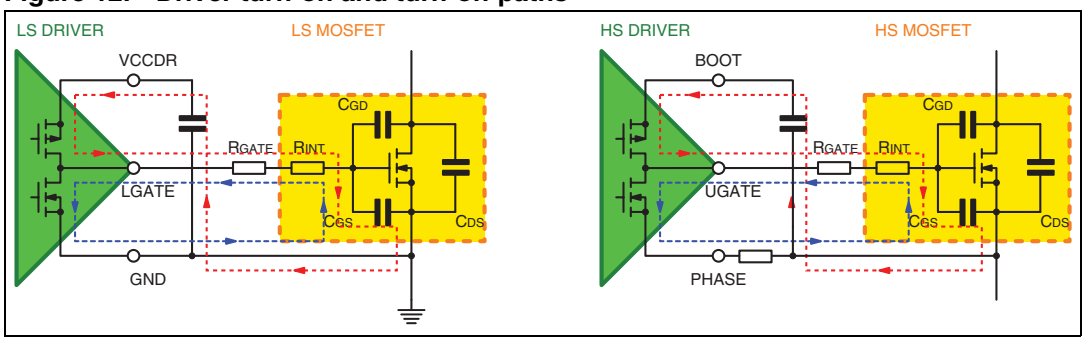
Figure 11. Power connections (heavy lines)



Gate traces and phase trace must be sized according to the driver RMS current delivered to the Power MOSFET. The device robustness allows the managing of applications with the power section far from the controller without losing performance. However, when possible, it is recommended to minimize the distance between the controller and power section.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate the bypass capacitor (VCC and bootstrap capacitor) and feedback compensation components as close to the device as is practical.

Figure 12. Driver turn-on and turn-off paths



10 Application information

10.1 Inductor design

The inductance value is defined through a compromise between the dynamic response time, the efficiency, the cost, and the size. The inductor must be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current (typ.). The inductance value can be calculated with the following relationship:

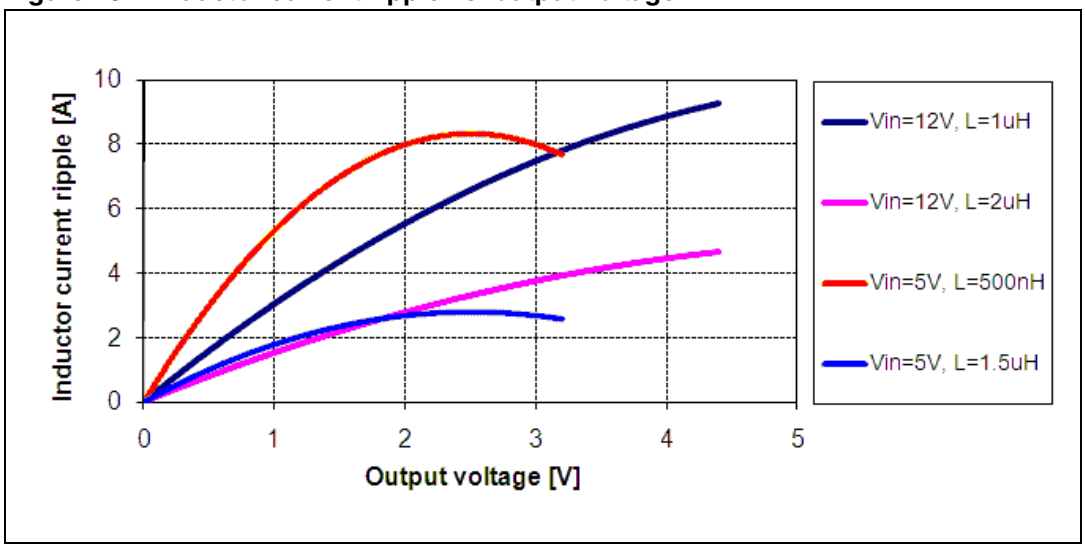
Equation 13

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. *Figure 13* shows the ripple current vs. the output voltage for different values of the inductor, with V_{IN} = 5 V and V_{IN} = 12 V.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from initial to final value. Until the inductor has finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required. If the compensation network is well designed, during a load variation the device is able to set a duty cycle value very different (0% or 80%) from the steady-state one. When this condition is reached, the response time is limited by the time required to change the inductor current.

Figure 13. Inductor current ripple vs. output voltage



10.2 Output capacitor(s)

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both the ESR and capacitive value of the output capacitors as follows:

Equation 14

$$\Delta V_{OUT\_ESR} = \Delta I_L \cdot ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

where ΔI_L is the inductor current ripple. In particular, the expression that defines ΔV_{OUT_C} takes into consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

During a load variation, the output capacitors supply the current to the load or absorb the current stored in the inductor until the converter reacts. In fact, even if the controller immediately recognizes the load transient and sets the duty cycle at 80% or 0%, the current slope is limited by the inductor value. The output voltage has a drop that, also in this case, depends on the ESR and capacitive charge/discharge as follows:

Equation 15

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \cdot ESR$$

$$\Delta V_{OUT\_C} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

where ΔV_L is the voltage applied to the inductor during the transient response ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitance which does not minimize the voltage deviation during dynamic load variations. On the contrary, electrolytic capacitors have large capacitance to minimize voltage deviation during load transients while they do not show the same ESR values as the MLCC, resulting therefore in higher ripple voltages. For these reasons, a mix between electrolytic and MLCC capacitors is suggested to minimize ripple as well as reduce voltage deviation in dynamic mode.

10.3 Input capacitors

The input capacitor bank is designed considering mainly the input RMS current that depends on the output deliverable current (I_{OUT}) and the duty-cycle (D) for the regulation as follows:

Equation 16

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depend on the input capacitor ESR and, in the worst case, are:

Equation 17

$$P = ESR \cdot (I_{OUT} / 2)^2$$

11 Package mechanical data

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Table 7. VFQFPN16 3x3x1.0 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3.00	3.15
D1		1.50	
D2	See next table		
E	2.85	3.00	3.15
E1		1.50	
E2	See next table		
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd			0.08

Table 8. Exposed pad variation

Variation	D2			E2		
	Min.	Typ.	Max.	Min.	Typ.	Min.
A	0.95	1.10	1.25	0.95	1.10	1.25
B	1.45	1.60	1.75	1.45	1.60	1.75

Figure 14. VFQFPN16 package drawing

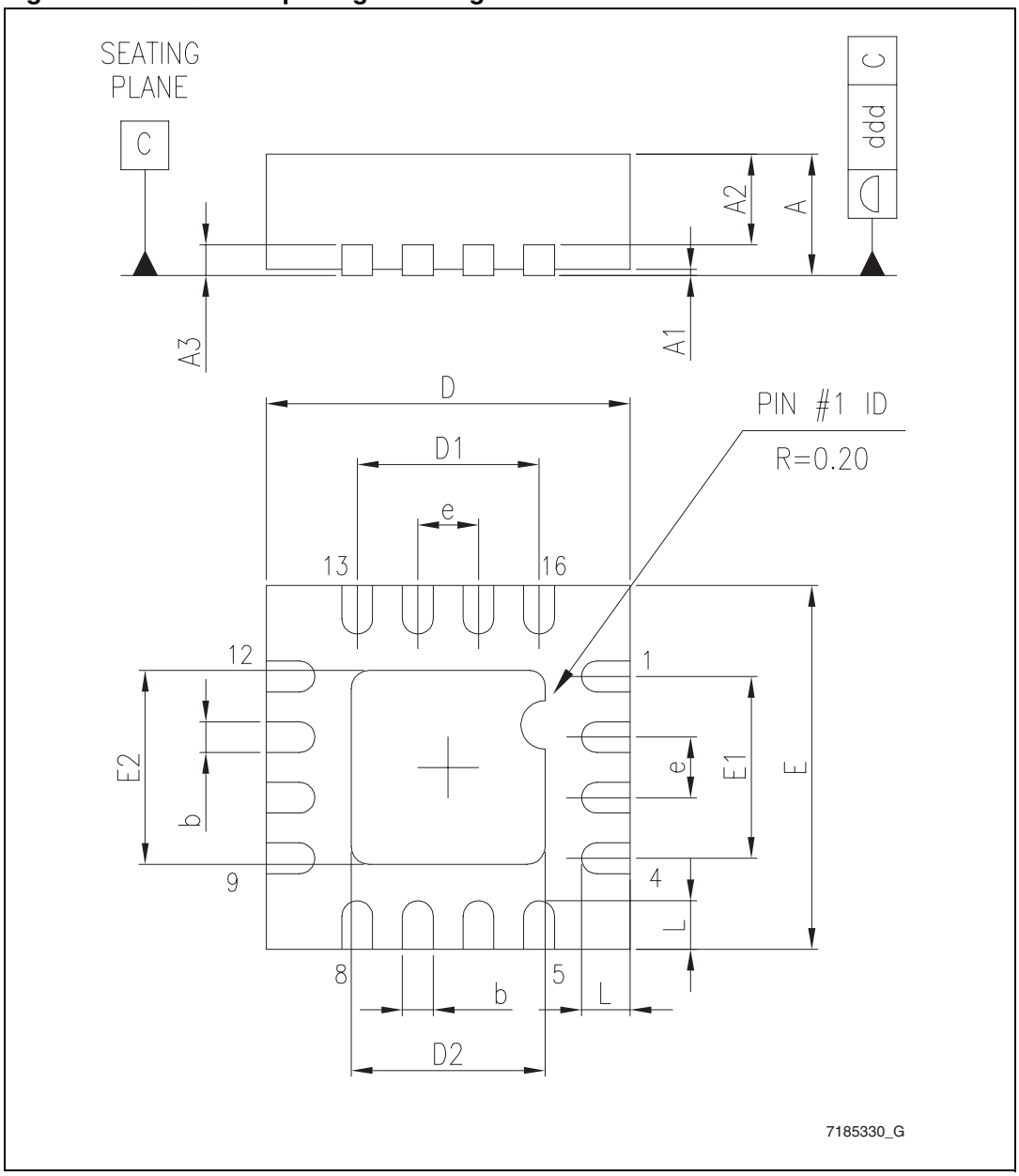
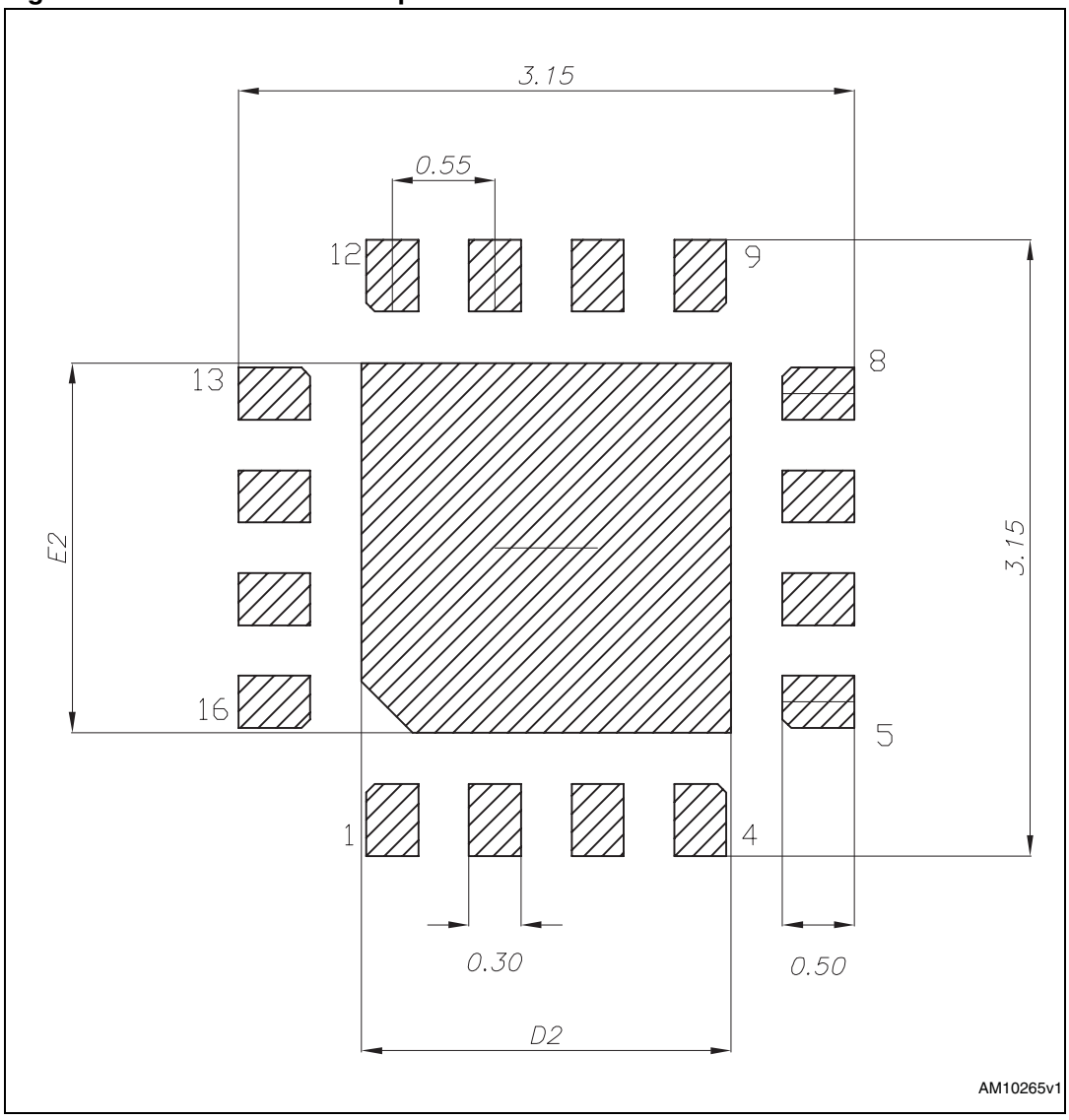


Figure 15. Recommended footprint



12 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Nov-2010	1	Initial release.
04-Jul-2012	2	Updated PGOOD limits in *Table 5*. Minor text changes.

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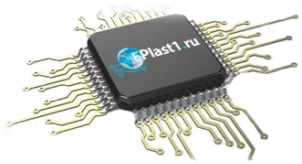

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