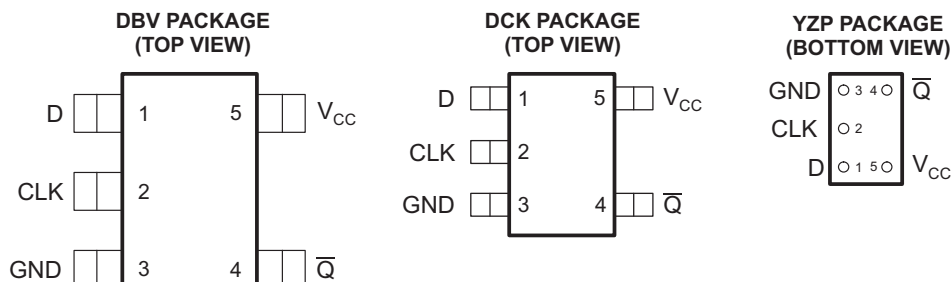


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.2 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the \bar{Q} output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G80YZPR	__CX__
		Reel of 250	SN74LVC1G80DBVT	C80__
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G80DBVR	C80__
		Reel of 250	SN74LVC1G80DCKT	CX__

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
 YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



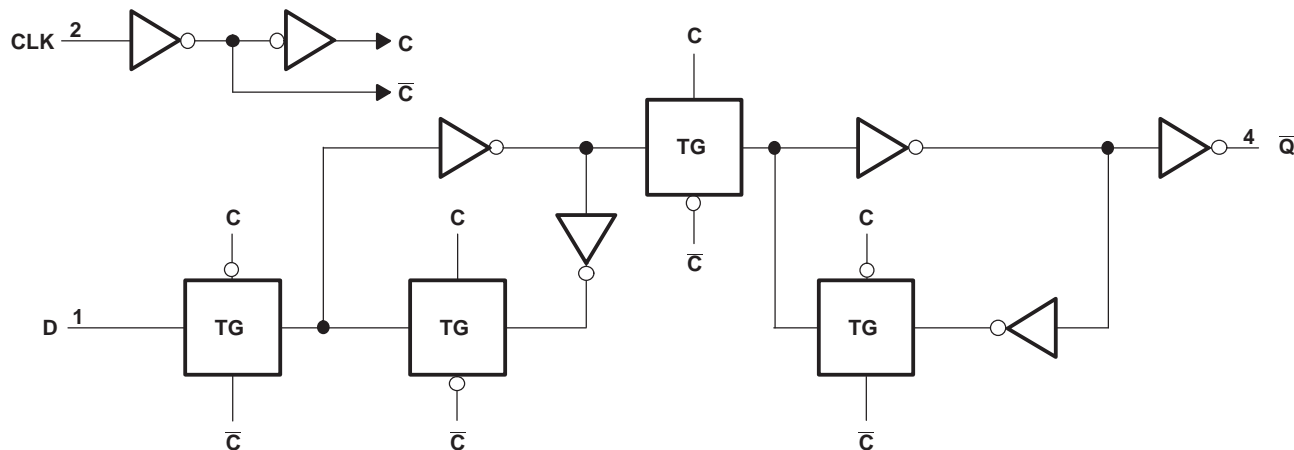
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

FUNCTION TABLE

INPUTS		OUTPUT \bar{Q}
CLK	D	
\uparrow	H	L
\uparrow	L	H
L	X	Q_0

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	6.5	V
V _I	Input voltage range ⁽²⁾		−0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−50	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DBV package		206	°C/W
		DCK package		252	
		YZP package		132	
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		mA
		V _{CC} = 2.3 V	–8		
		V _{CC} = 3 V	–16		
			–24		
		V _{CC} = 4.5 V	–32		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
			24		
		V _{CC} = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V _{CC} = 3.3 V ± 0.3 V	10		
		V _{CC} = 5 V ± 0.5 V	5		
T _A	Operating free-air temperature	–40	85	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES221Q–APRIL 1999–REVISED JANUARY 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = −100 μA	1.65 V to 5.5 V	V _{CC} − 0.1			V
		I _{OH} = −4 mA	1.65 V	1.2			
		I _{OH} = −8 mA	2.3 V	1.9			
		I _{OH} = −16 mA	3 V	2.4			
		I _{OH} = −24 mA		2.3			
		I _{OH} = −32 mA	4.5 V	3.8			
V _{OL}		I _{OL} = 100 μA	1.65 V to 5.5 V			0.1	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.3	
		I _{OL} = 16 mA	3 V			0.4	
		I _{OL} = 24 mA				0.55	
		I _{OL} = 32 mA	4.5 V			0.55	
I _I	CLK or D inputs	V _I = 5.5 V or GND	0 to 5.5 V			±10	μA
I _{off}		V _I or V _O = 5.5 V	0			±10	μA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10	μA
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500	μA
C _i		V _I = V _{CC} or GND	3.3 V	3.5			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5.5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160			160	160		MHz
t _w	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
t _{su}	Setup time before CLK↑	Data high	2.3		1.5		1.3		1.1		ns
		Data low	2.5		1.5		1.3		1.1		
t _h	Hold time, data after CLK↑		0		0.2		0.9		0.4		ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	\overline{Q}	3	9.1	1.5	6	1.3	4.2	1.1	3.8	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	\overline{Q}	4.4	9.9	2.3	7	2	5.2	1.3	4.5	ns

Operating Characteristics

$T_A = 25^\circ\text{C}$

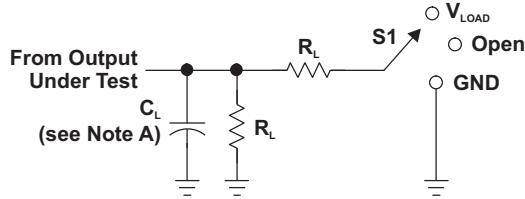
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	24	24	25	27	pF

SN74LVC1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES221Q—APRIL 1999—REVISED JANUARY 2007

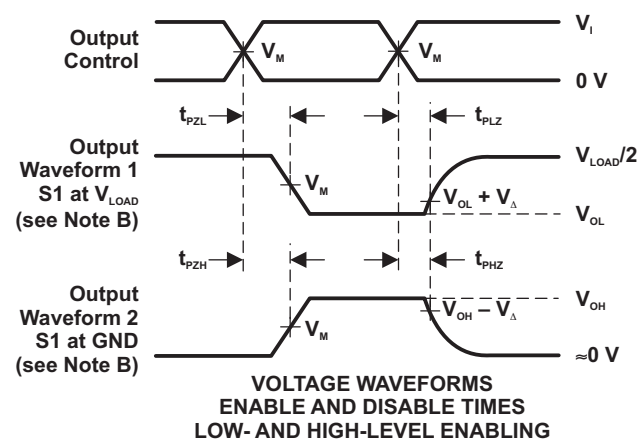
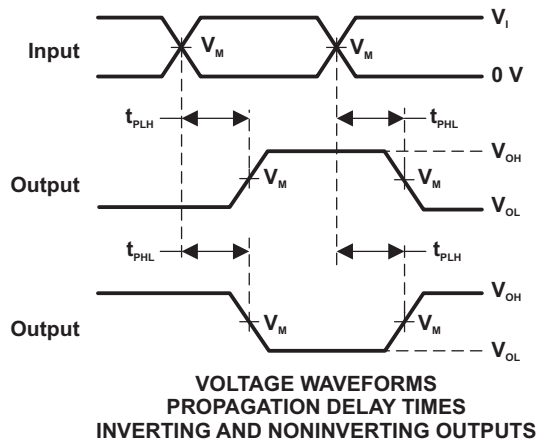
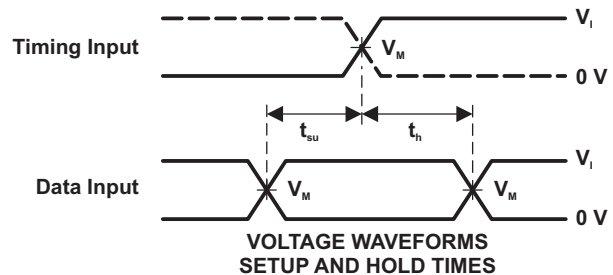
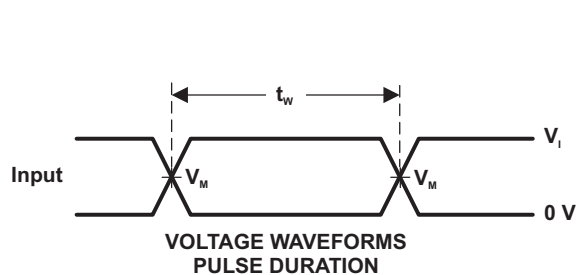
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

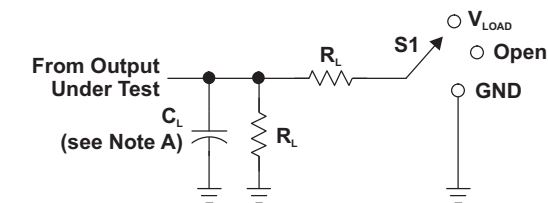
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_i/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

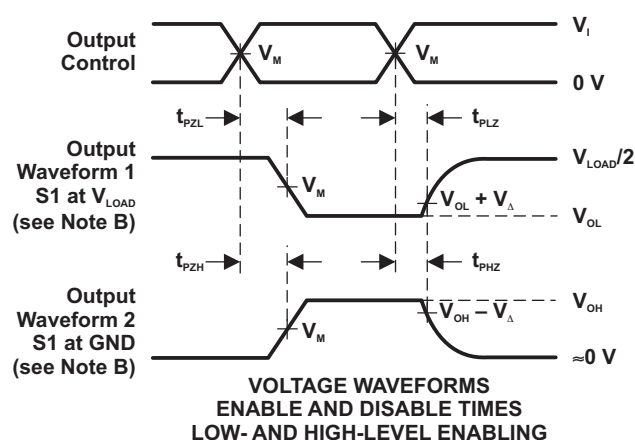
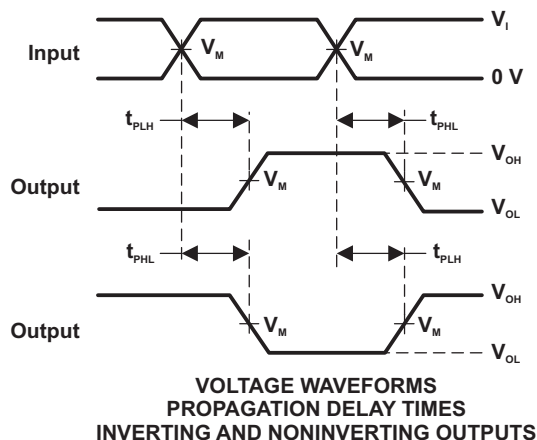
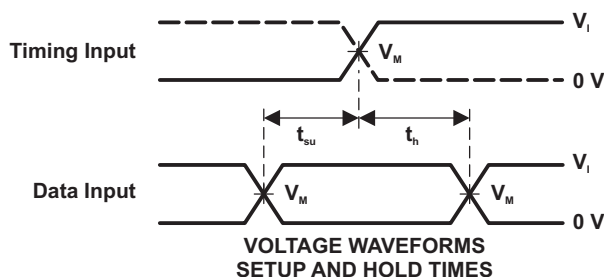
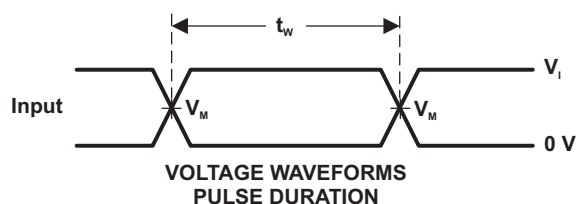
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_I/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC1G80DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C802 ~ C805 ~ C80F ~ C80R)	Samples
SN74LVC1G80DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C802 ~ C805 ~ C80F ~ C80R)	Samples
SN74LVC1G80DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C802 ~ C805 ~ C80F ~ C80R)	Samples
SN74LVC1G80DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C805 ~ C80F ~ C80R)	Samples
SN74LVC1G80DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C805 ~ C80F ~ C80R)	Samples
SN74LVC1G80DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C805 ~ C80F ~ C80R)	Samples
SN74LVC1G80DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CX5 ~ CXF ~ CXK ~ CXR)	Samples
SN74LVC1G80DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CX5 ~ CXF ~ CXK ~ CXR)	Samples
SN74LVC1G80DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CX5 ~ CXF ~ CXK ~ CXR)	Samples
SN74LVC1G80DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CX5 ~ CXF ~ CXK ~ CXR)	Samples
SN74LVC1G80DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CX5 ~ CXF ~ CXK ~ CXR)	Samples
SN74LVC1G80DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CX5 ~ CXF ~ CXK ~ CXR)	Samples
SN74LVC1G80YEAR	OBSOLETE	DSBGA	YEA	5		TBD	Call TI	Call TI	-40 to 85		
SN74LVC1G80YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CX7 ~ CXN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

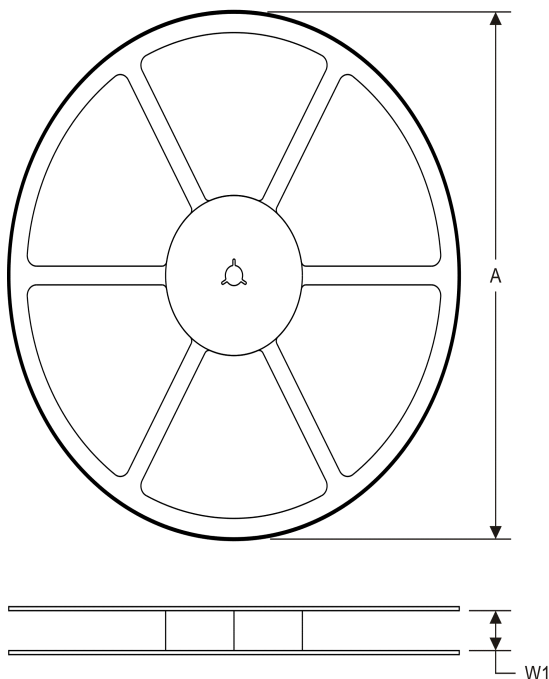
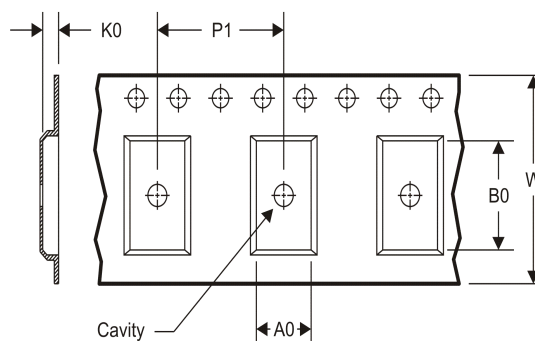
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


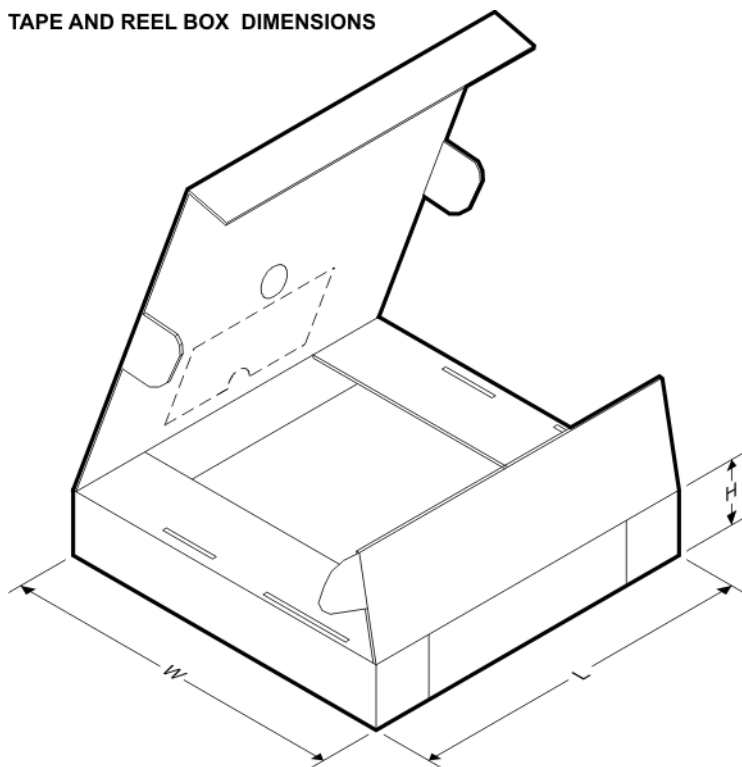
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

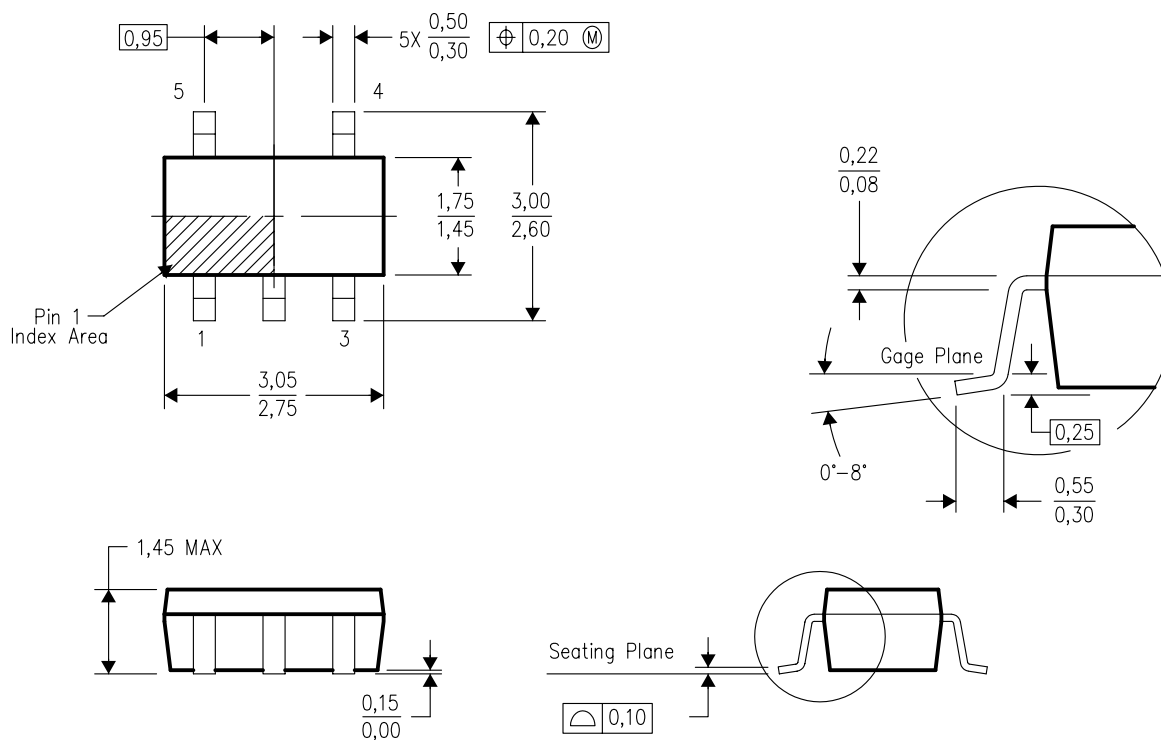


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

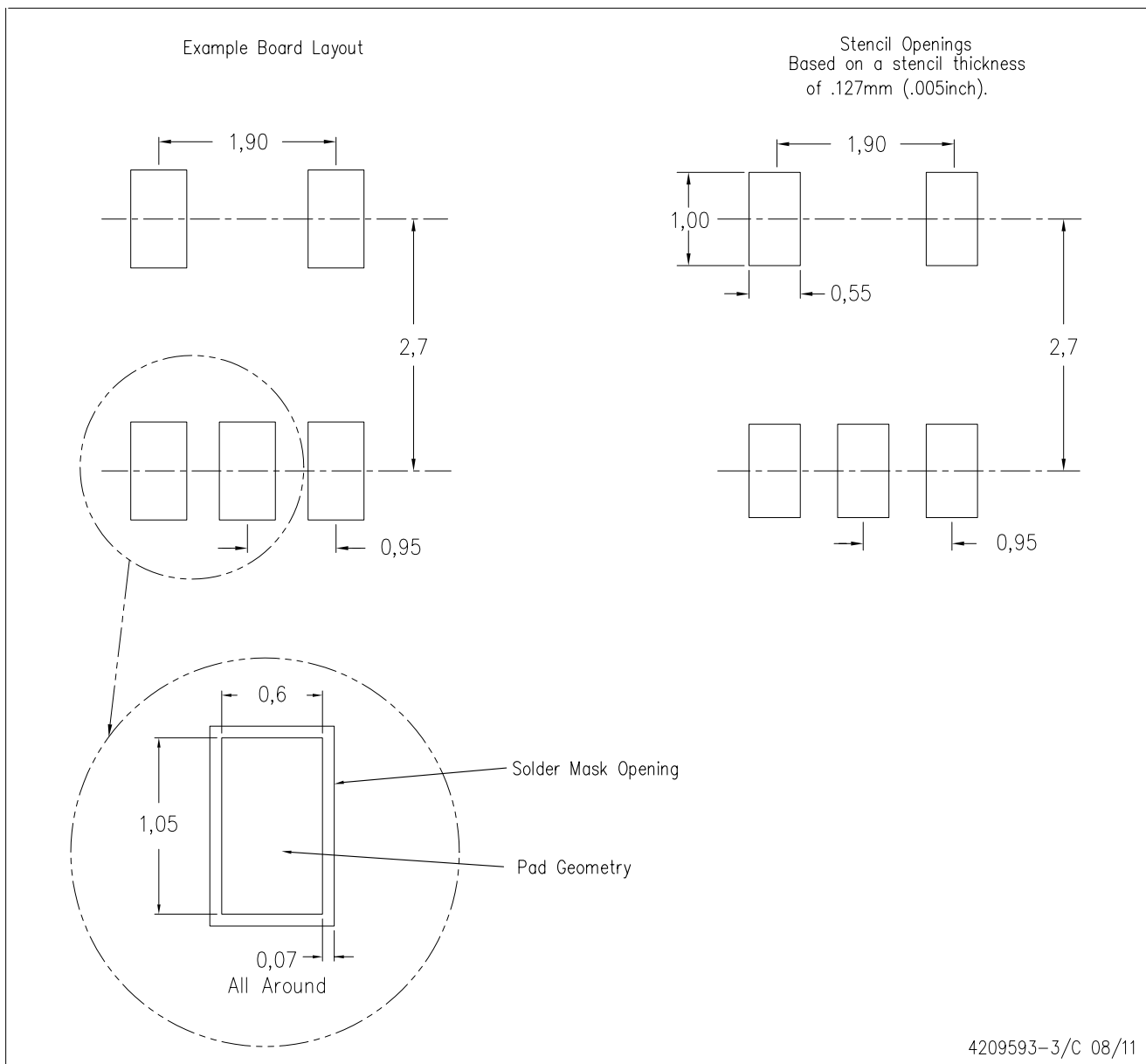


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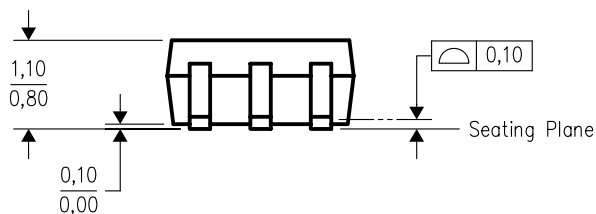
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

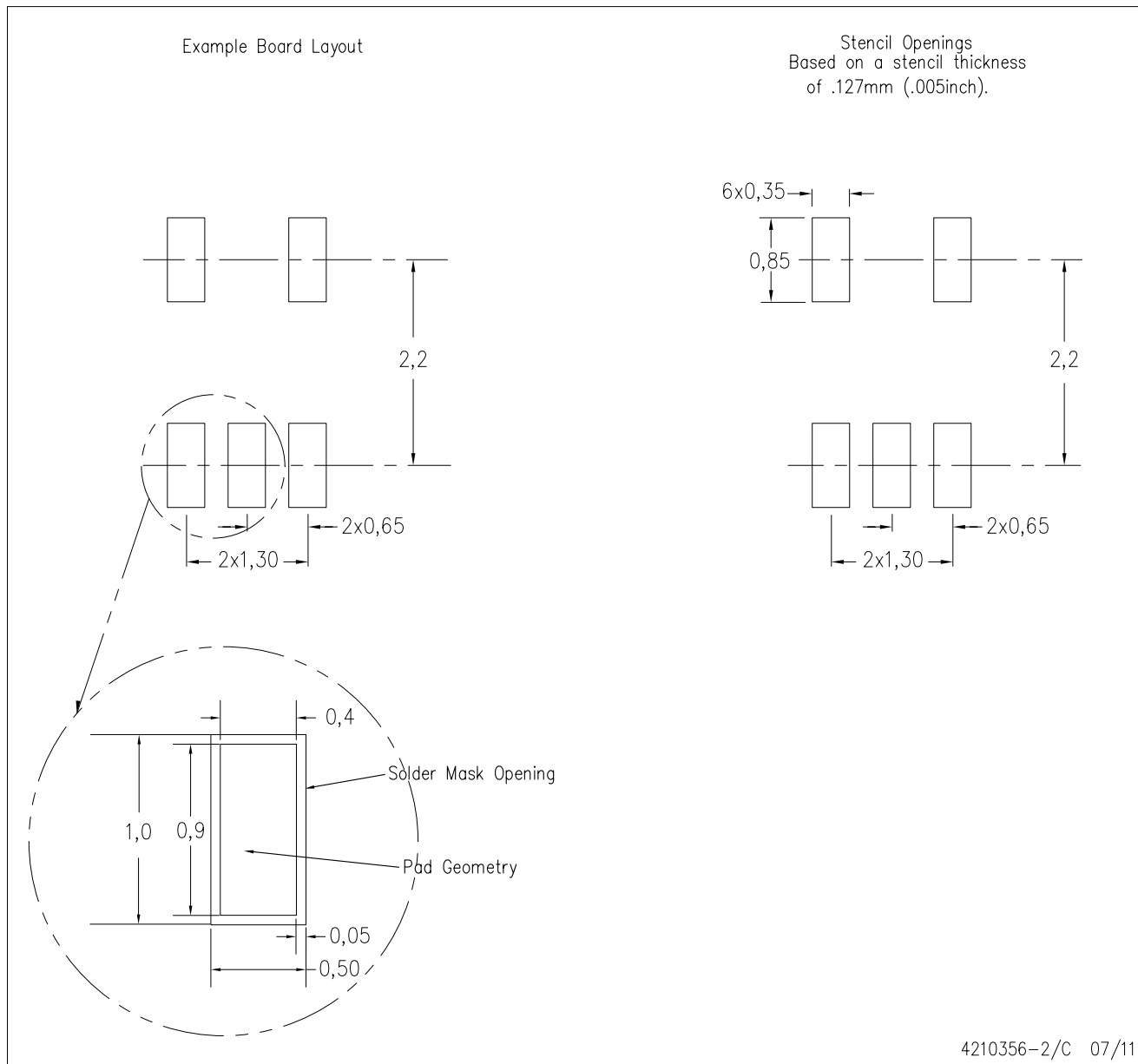


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

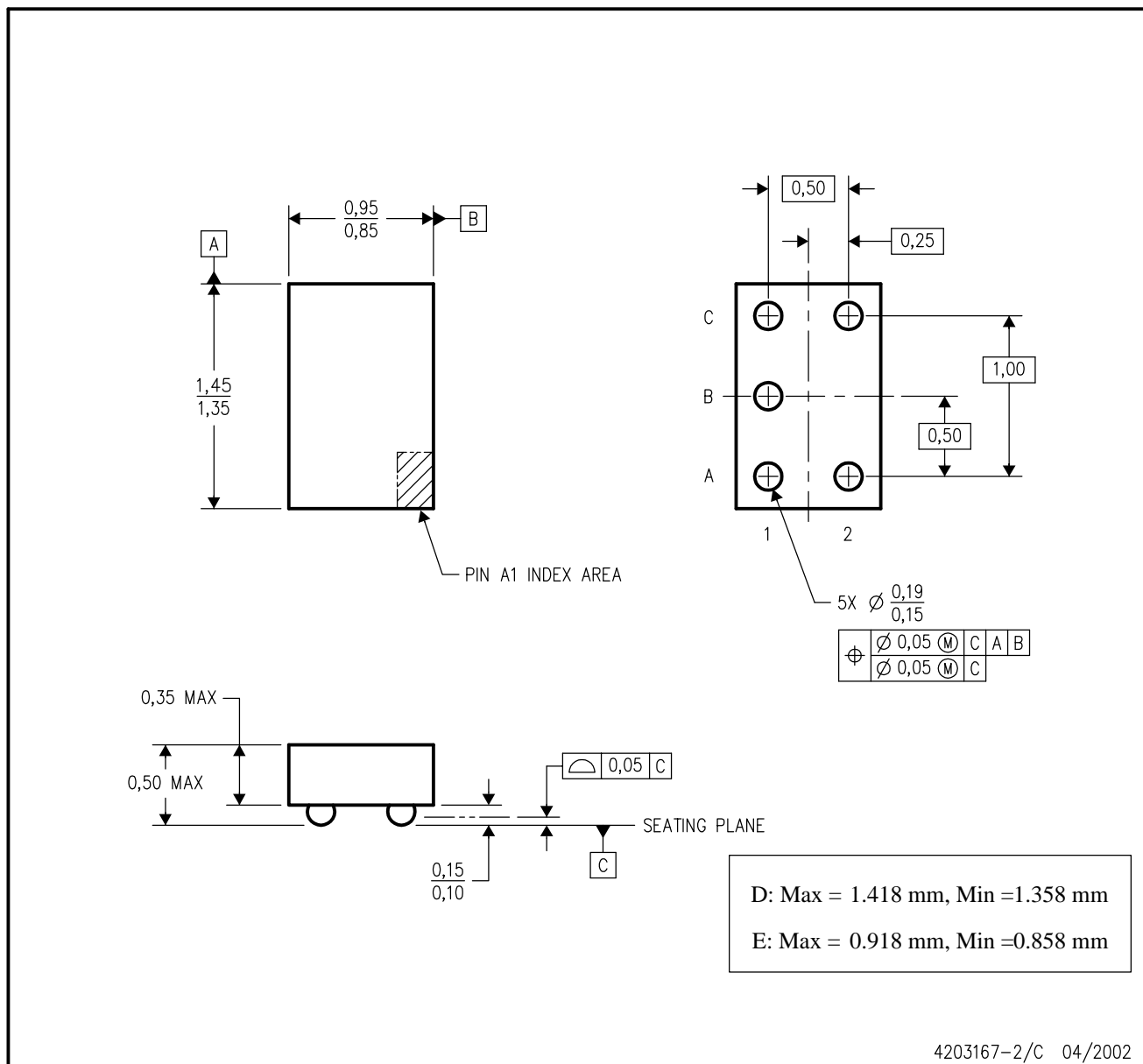
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

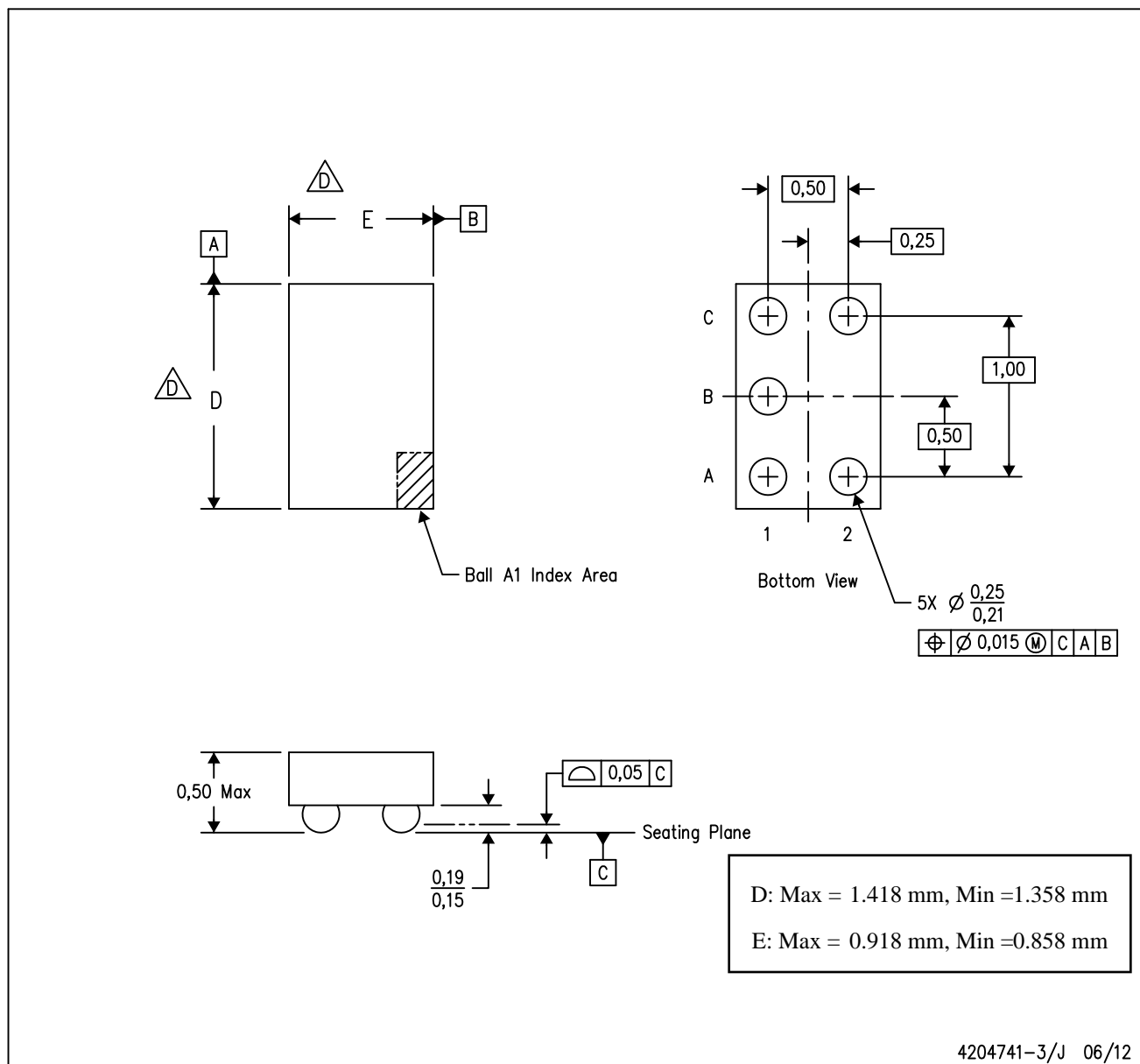


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoStar™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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