ANALOG DEVICES

# Circuit Note
## CN-0372

Circuits from the Lab® Reference Designs

*Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0372.*

| Devices Connected/Referenced | |
|---|---|
| AD7091R-5 | 4-Channel, $I^2C$, Ultralow Power, 12-Bit ADC |
| ADP5090 | Ultralow Power Boost Regulator with MPPT and Charge Management |
| ADA4805-1 | 0.2 µV/°C Offset Drift, 105 MHz Low Power, Low Noise, Rail-to-Rail Amplifier |
| ADP1607 | 2 MHz, Synchronous Boost DC-to-DC Converter |

# Ultralow Power, General-Purpose, Multichannel Data Acquisition System with Energy Harvesting Circuit and Alert Function

## EVALUATION AND DESIGN SUPPORT

**Circuit Evaluation Boards**

- **CN-0372 Circuit Evaluation Board (EVAL-CN0372-PMDZ)**
- **System Demonstration Platform (EVAL-SDP-CB1Z)**
- **SDP-I-PMOD Interposer Board (SDP-PMD-IB1Z)**

**Design and Integration Files**

- **Schematics, Layout Files, Bill of Materials**

## CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an ultralow power, multichannel data acquisition system that can be powered by a photovoltaic (PV) cell or thermoelectric generator (TEG). The circuit uses the industry's lowest power, multichannel, 12-bit successive approximation analog-to-digital converter (SAR ADC), the AD7091R-5, along with an efficient energy harvesting circuit based on the ADP5090 boost regulator. The ADC has a typical power consumption of 100 µW on a single 3 V supply when sampling at 22 kSPS. Typical signal-to-noise ratio (SNR) is 68 dB for a 1 kHz input signal.

The low power consumption and small form factor make this combination of devices ideally suited for portable low power applications, particularly for wearable and self-powered devices.

**Rev. 0**



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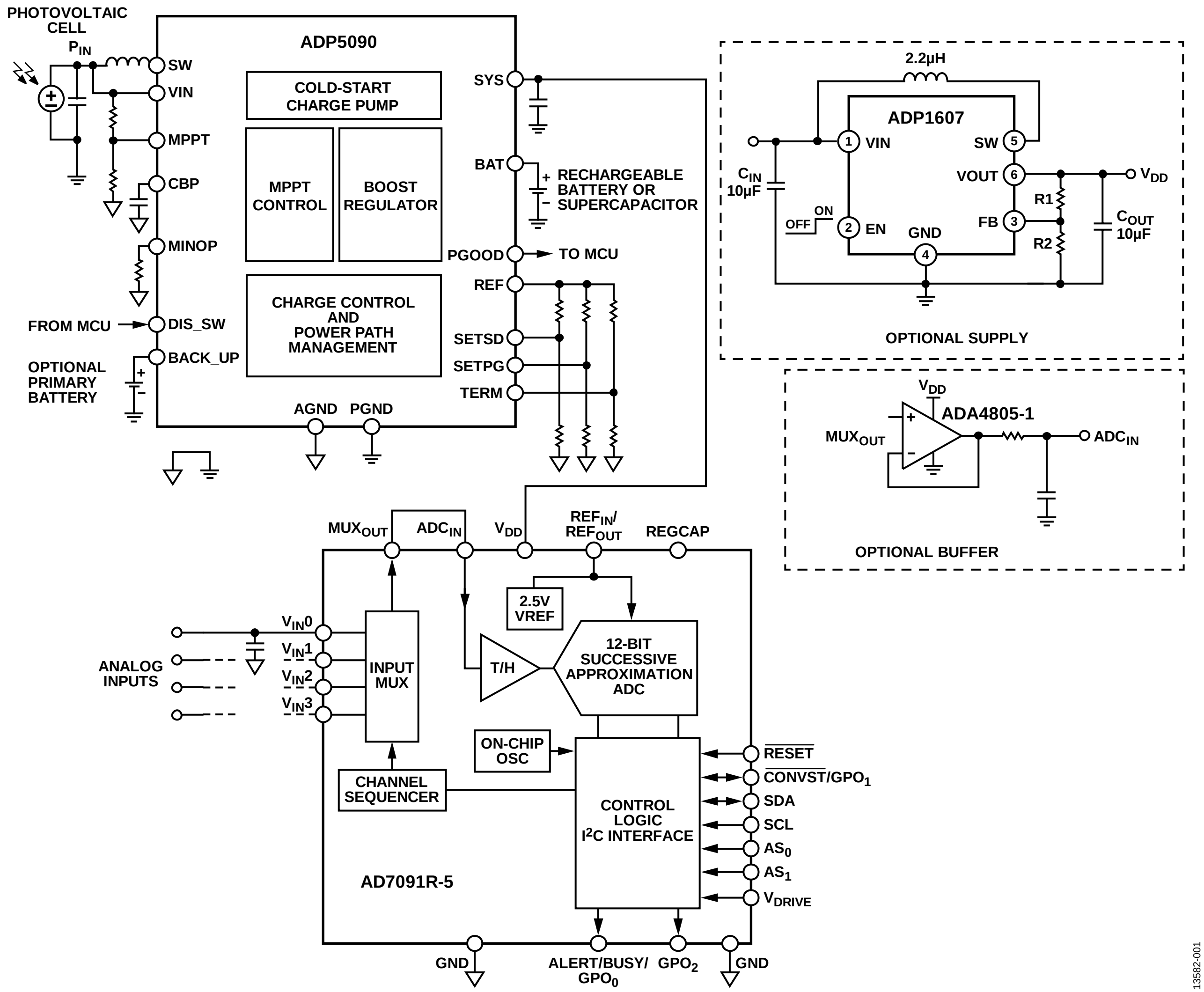


*Figure 1. Low Power Data Acquisition System with Energy Harvesting Circuit (Simplified Schematic: All Connections and Decoupling Not Shown)*

## CIRCUIT DESCRIPTION

This circuit provides an optimized low power compact solution for multichannel system monitoring. These characteristics are particularly important in wearable and self-powered applications where form factor and power consumption are critical system specifications.

### *Analog-to-Digital Converter*

The AD7091R-5 is a 12-bit, ultralow power, successive approximation ADC. The device operates from a single 2.7 V to 5.25 V power supply. This ADC features an on-chip conversion clock, an accurate reference, and an I²C interface that operates in both standard ($f_{SCL}$ = 100 kHz) and fast ($f_{SCL}$ = 400 kHz) modes.

The conversion process and data acquisition are controlled using the I²C interface and an internal oscillator. The AD7091R-5 interface allows data read after the conversion, achieving a maximum 22.22 kSPS throughput rate in fast mode. This device uses advanced design and process techniques to achieve ultralow power dissipation without compromising performance.

An on-chip, accurate 2.5 V reference is available on the $REF_{IN}$/$REF_{OUT}$ pin.

The AD7091R-5 has an autocycle mode that allows the user to configure the ADC for autonomous operation and is ideal for the monitoring of events outside of a user defined range. Conversions automatically take place at configured intervals as shown in Table 25 of the AD7091R-5 data sheet. Typically, this mode is used to monitor a selection of channels with limit registers programmed to signal out of bounds conditions via the alert function.

### *Energy Harvester*

The ADP5090 is an integrated boost regulator that converts dc power from photovoltaic cells or thermoelectric generators. The device charges storage elements (rechargeable battery or super capacitor). The CN-0372 board uses a super capacitor that supplies power for small electronic devices and battery-free systems. The ADP5090 provides efficient conversion of the small amounts of harvested power available from PV cells or TEGs. The ADP5090 operates on an input power range from 16 µW to 200 mW range with sub-microwatt operation losses.

With the internal cold-start circuit, the regulator can start operating at an input voltage as low as 380 mV. This solution eliminates the need for an external battery to power the circuit (although backup battery options are available) and makes full use of harvestable energy instead.

The SYS voltage output of the ADP5090 supplies the entire circuit as shown in Figure 1.

### Circuit Design

The circuit in Figure 2 shows the minimal connections needed for the AD7091R-5 ADC.

The analog input range for the AD7091R-5 is 0 V to $V_{REF}$ and is unipolar. The circuit is not designed to accept negative voltages. While the AD7091R-5 contains a wide bandwidth track-and-hold amplifier that can handle input frequencies up to 1.5 MHz, the circuit is tested to resolve lower frequencies up to 2 kHz in fast mode.

The AD7091R-5 provides access to the multiplexer output eliminating the need for a signal conditioning circuit in each channel when additional filtering is required. The input signal of the active channel appears at $MUX_{OUT}$. The filters before the ADC $V_{IN}$ pins are designed to have a cutoff frequency of about 8.6 MHz. These filters attenuate noise at the ADC input and absorb the charge kickbacks from the ADC. It is recommended to use a low series resistance value and a reasonably sized capacitor that can source and sink the high frequency charge kickbacks from the ADC.

If no additional filtering or signal conditioning is required, the $MUX_{OUT}$ pin is tied directly to $ADC_{IN}$. Control of the AD7091R-5 is through the $I^2C$-compatible serial bus.

Figure 3 shows the ADP5090 energy harvesting circuit. The circuit converts power from an energy source connected to the J4 terminal, stores charge in the super capacitor (C26), and provides power to the entire circuit.

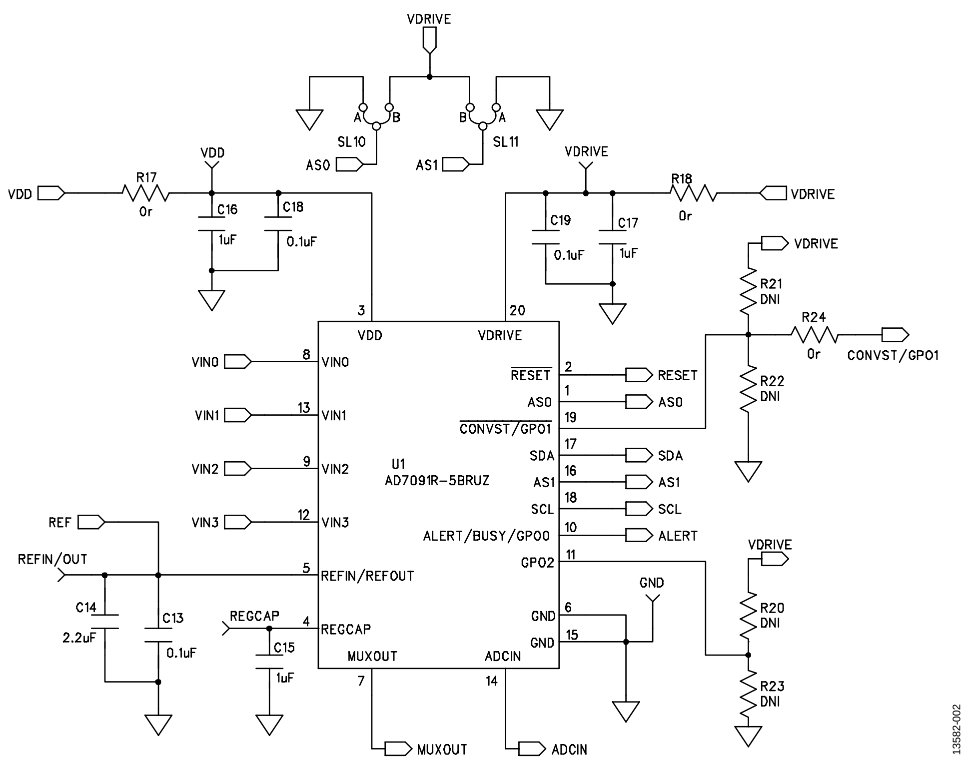


*Figure 2. CN-0372 ADC Connection (Simplified Schematic: All Connections Not Shown)*

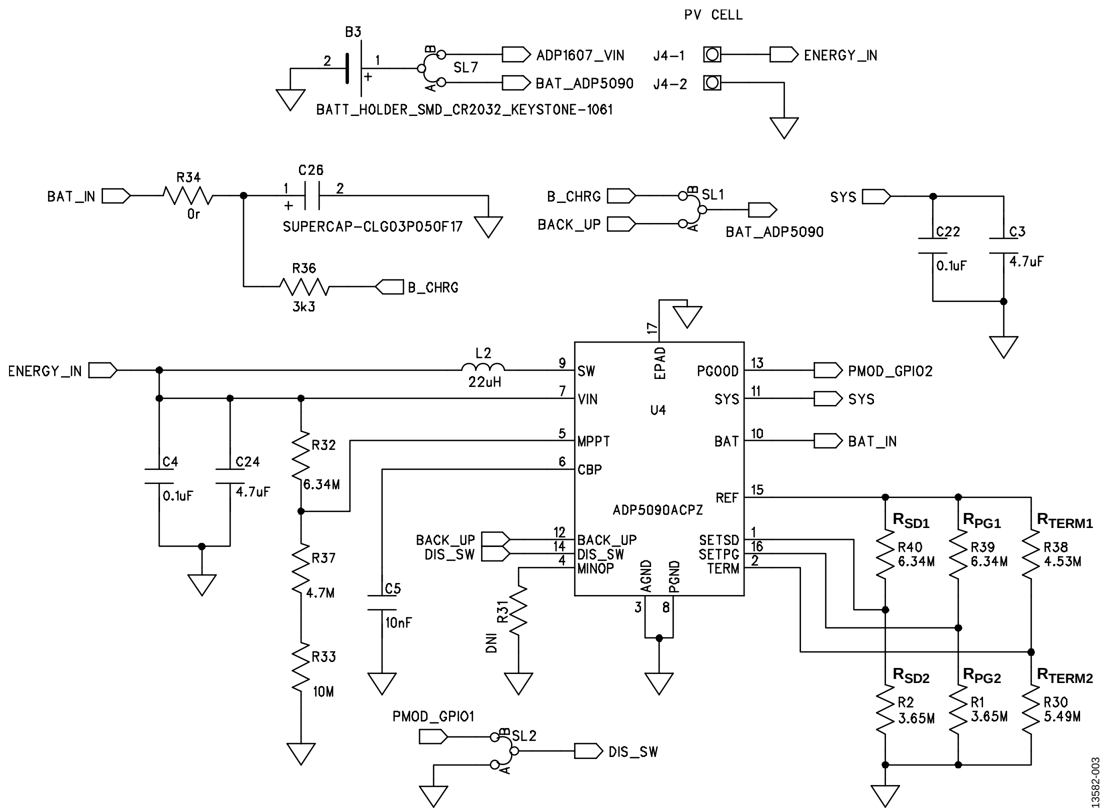


*Figure 3. CN-0372 Energy Harvesting Circuit*

Harvested energy from a PV cell or TEG is introduced at ENERGY_IN. When ENERGY_IN exceeds 380 mV, the ADP5090 enters cold start-up. The device then exits cold-startup, and main boost is enabled when the SYS voltage exceeds $V_{SYS\_TH}$, which is typically 1.93 V. The logic high level on PGOOD is equal to the SYS voltage, and when the battery terminal voltage is reached, the main boost charger is turned off.

The ADP5090 boost regulator operates in pulse frequency mode (PFM), transferring energy stored in the input capacitor to SYS and the C26 super capacitor (Cellergy CLG03P050F17, 50 mF, 3.5 V). A PGOOD threshold is set by external connectors to indicate that the SYS voltage is at an acceptable voltage, given by

$$V_{SYS\_PGOOD} = V_{REF\_ADP5090}\left(1+\frac{R_{PG1}}{R_{PG2}}\right), \sim 3.3\text{ V}$$

where:

$R_{PG1}$ and $R_{PG2}$ are the values from Figure 3.

$V_{REF\_ADP5090}$ is typically 1.21 V.

The ADP5090 is also equipped with battery overcharging and discharging protection thresholds, which are also set by external resistors.

To prevent overcharging, the rising threshold for the battery terminal voltage is given by

$$V_{BAT\_TERM} = \frac{3}{2}V_{REF\_ADP5090}\left(1+\frac{R_{TERM1}}{R_{TERM2}}\right), \sim 3.3\text{ V}$$

where $R_{TERM1}$ and $R_{TERM2}$ are the values from Figure 3.

To prevent deep discharge, the falling threshold for the battery discharge shutdown voltage is given by

$$V_{BAT\_SD} = V_{REF\_ADP5090}\left(1+\frac{R_{SD1}}{R_{SD2}}\right), \sim 3.3\text{ V}$$

where $R_{SD1}$ and $R_{SD2}$ are the values from Figure 3.

An illustration of these threshold voltages is shown in Figure 4.

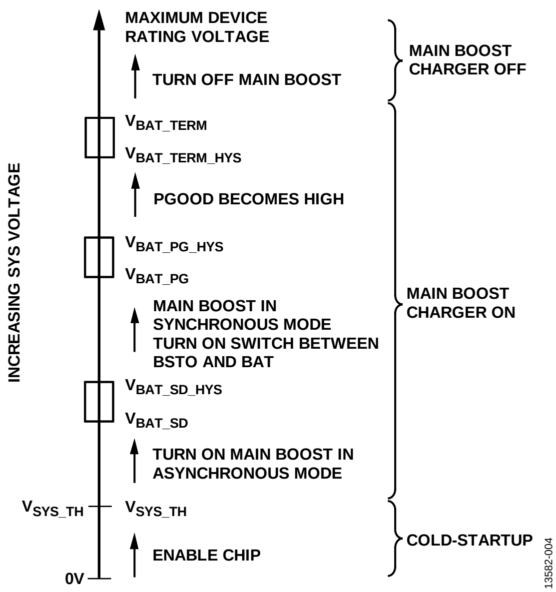


*Figure 4. States of Various Threshold Voltages*

The circuit in Figure 3 also has a provision through SL7 to provide a low energy state backup option to accelerate cold-start.

A complete documentation package including schematics, board layout, and bill of materials (BOM) can be found at www.analog.com/CN0372-DesignSupport. The circuit is compatible with the Digilent PMOD interface standard.

### *Measurement Results for DAS with Energy Harvesting Circuit*

The circuit comes with a graphical user interface that facilitates configuring the devices on-board and evaluating the circuit performance. Tabs are available for device configuration, as well as for displaying noise performance, histogram, and register readout. For a complete description of the software package, see the CN-0372 Software User Guide.

Figure 5 and Figure 6 show the ac performance of the circuit, configured with $MUX_{OUT}$ connected directly to $ADC_{IN}$, for a 2.4 V p-p, 1 kHz sine wave with a common-mode voltage of 1.25 V. While the default configuration generates a 3.3 V supply on SYS, all measurements in this circuit note were taken with the external resistors configured for 3 V supplies.

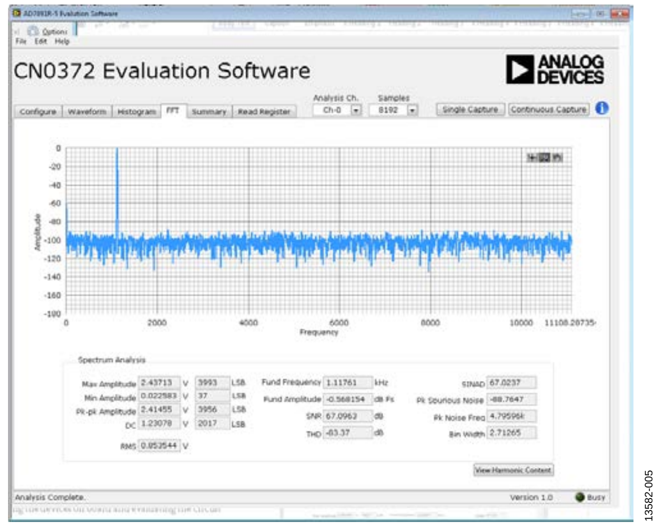


*Figure 5. CN-0372 AC Performance*

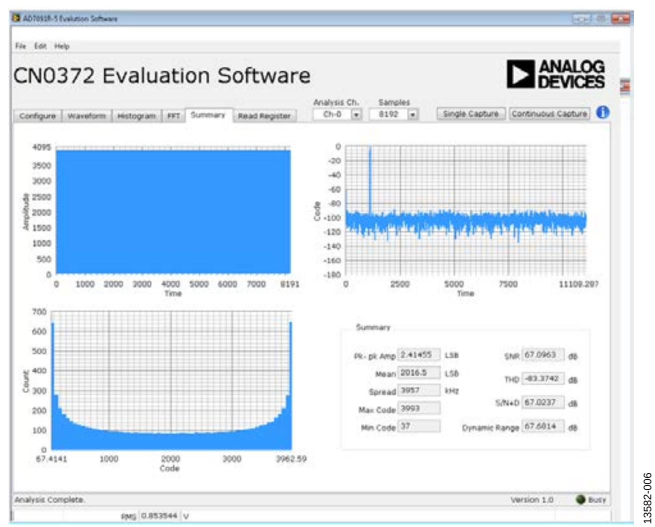


*Figure 6. CN-0372 AC Performance Full Summary*

Power consumed is computed using the following equation:

$$P_T = I_T \times V_S$$

where:

$P_T$ is the total consumed power.

$I_T$ is the total current consumption measured in series with $V_{DD}$.

$V_S$ is the supply voltage at $V_{DD}$.

The circuit, configured without the buffer and with $V_{DD}$ and $V_{DRIVE}$ coming from SYS, consumes 34 µA.

## COMMON VARIATIONS

An on-board option for external buffering of the $MUX_{OUT}$ signal using an ADA4805-1 is available, as well as an option to use the backup battery to power an on-board ADP1607 regulator to generate the board supply rails.

Figure 7 shows the on-board optional buffer circuitry. When used, R6 is removed, SL9 and SL12 are set to Position B, SL13 is set to Position A, and R43 is installed. The circuit also has provisions for any gain, attenuation, or level shifting that is desired. The ADA4805-1 consumes approximately 500 µA of quiescent current, but has the option to power down and scale with throughput. As shown in Figure 8, controlling the ADA4805-1 SHUTDOWN pin allows users to dynamically manage its power consumption. Adjusting the duty cycle of the SHUTDOWN signal through the evaluation software achieves significant power savings.

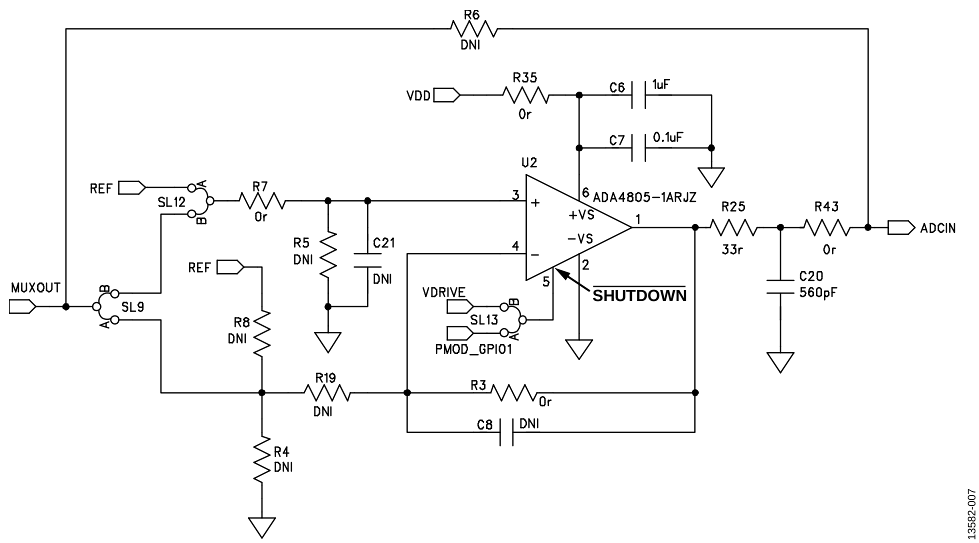


*Figure 7. Optional Buffer Circuitry*

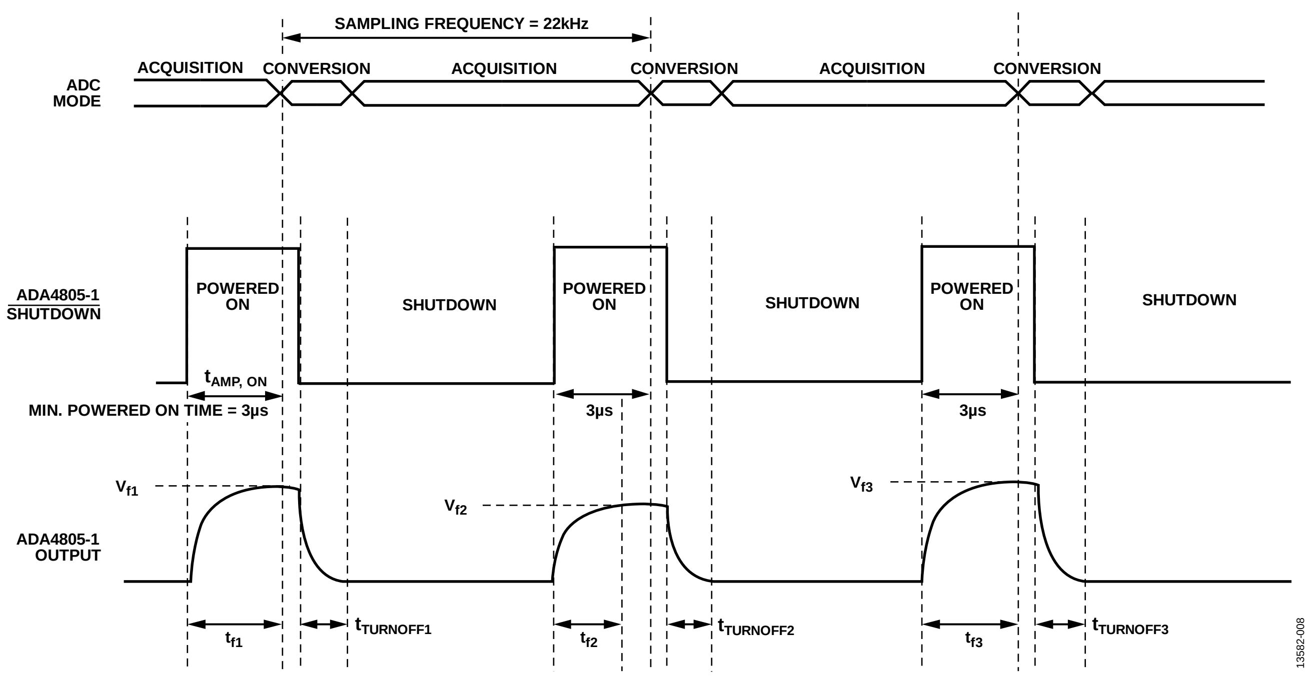


*Figure 8. Dynamic Power Scaling with ADA4805-1*

See the CN-0372 Software User Guide for additional details on controlling the power-scaling feature of the ADA4805-1 in the evaluation software.

With power scaling, the equation for consumed power becomes

$$P_T = I_T \times V_S + I_Q \times V_S \times \frac{t_{AMP,ON}}{t_S}$$

where:

$P_T$ is the total consumed power.

$I_Q$ is the quiescent current.

$t_{AMP,ON}$ is the time the ADA4805-1 is on.

$t_S$ is the sampling time.

Overall system consumption with the ADA4805-1 in use and dynamically powered, and with VDD and VDRIVE coming from SYS, was as low as 70 µA without performance degradation, as shown in Figure 9.

Table 1 shows typical current consumption of the circuit at different configurations.

**Table 1. Current Consumption at Different Configurations**

| Configuration | Current (µA) |
|---|---|
| Without Buffer Amplifier | 34 |
| AD7091R-5 in Full Power Down | 13.4 |
| AD7091R-5 in Full Power Down, No Internal Reference | 0.5 |
| With Buffer Amplifier Always On | 530 |
| AD7091R-5 in Full Power Down | 520.4 |
| AD7091R-5 in Full Power Down, No Internal Reference | 507.3 |
| Dynamic Power Scaling with Buffer Amplifier | See Figure 9 |

Typical performance and current consumption of the system with different duty cycles is shown in Figure 9.

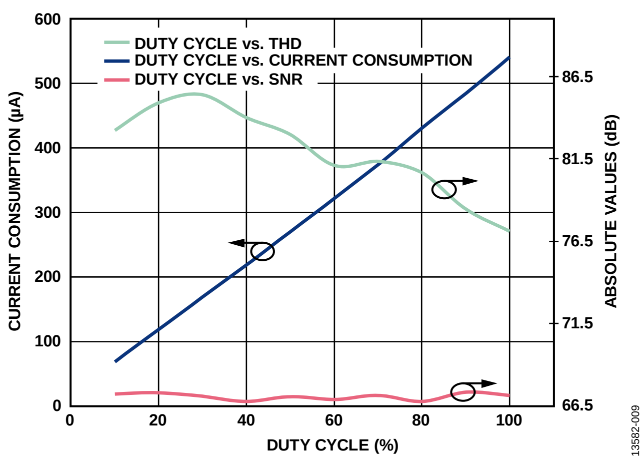


*Figure 9. Current Consumption and AC Performance with Varying Duty Cycle in Fast Mode*

Figure 10 shows the optional ADP1607 circuitry, which can be configured through SL7 to be powered by the B3 backup battery in Figure 3.

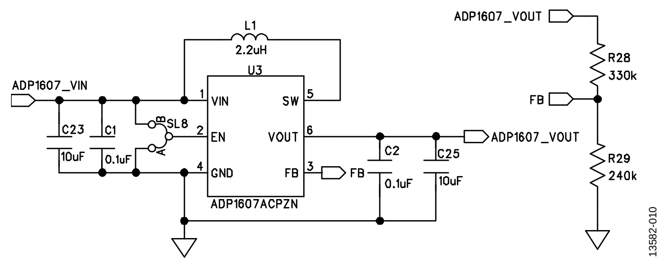


*Figure 10. Optional Regulator Circuitry*

The output voltage is configured by the R28 and R29 external resistors for a 3 V output using the following equation:

$$V_{OUT} = V_{FB}\left(1 + \frac{R28}{R29}\right) + I_{FB} \times R28$$

where:

$V_{FB}$ = 1.259 V.

$I_{FB}$ = 0.1 µA.

## CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0372-PMDZ circuit board, the SDP-PMD-IB1Z interposer board, and the EVAL-SDP-CB1Z system demonstration platform (SDP) board. The PMOD interposer board and the SDP controller board have 120-pin mating connectors. The interposer board and the EVAL-CN0372-PMDZ board have 12-pin PMOD interface Type 2A and 8-pin I²C interface matching connectors, allowing quick setup and evaluation of the circuit performance. The EVAL-CN0372-PMDZ board contains the circuit to be evaluated. The SDP controller board is used in conjunction with the CN0372 Evaluation Software to capture data and present results to the user.

**Table 2. PMOD Interface Type 2A connection**

| Pin No. | Signal | Description |
|---|---|---|
| 1 | CONVST/GPO1 | Connects to AD7091R-5 CONVST/GPO₁ pin. |
| 2, 3, 4 | NC | No connection. |
| 5, 11 | GND | Connects to GND. |
| 6, 12 | VDD_PMOD | Connects to PMOD power supply. |
| 7 | ALERT | Connects to AD7091R-5 ALERT pin. |
| 8 | RESET | Connects to AD7091R-5 RESET pin. |
| 9 | PMOD_GPIO1 | Connects to ADA4805-1 SHUTDOWN pin. Also connects to ADP5090 DIS_SW pin through SL2. |
| 10 | PMOD_GPIO2 | Connects to ADP5090 PGOOD pin. |

**Table 3. I²C Interface Connection**

| Pin No. | Signal | Description |
|---|---|---|
| 1, 2 | SCL | Connects to AD7091R-5 SCL pin |
| 3, 4 | SDA | Connects to AD7091R-5 SDA pin |
| 5, 6 | GND | Connects to GND |
| 7, 8 | VDD_PMOD | Connects to PMOD power supply |

### Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP, Windows Vista® (32-bit), or Windows 7 (32-bit)
- EVAL-CN0372-PMDZ circuit evaluation board
- EVAL-SDP-CB1Z SDP controller board
- SDP-PMD-IB1Z interposer board
- 8-pin IDSD-04-D flexible cable: needed to connect the $I^2C$ interface between the EVAL-CN0372-PMDZ and SDP-PMD-IB1Z boards (included with the EVAL-CN0372-PMDZ board)
- CN0372 Evaluation Software
- Power supply: 6 V wall wart
- USB cable
- SRS DS360 ultralow distortion function generator or similar precision source
- Cymbet CBC-PV-01 PV cell: typical operating voltage is 0.8 V with an output current of approximately 200 μA at 200 Lux in fluorescent light

### Getting Started

Before connecting the boards to the PC, install the CN0372 Evaluation Software. The most up to date version of the evaluation software can be downloaded from ftp://ftp.analog.com/pub/cftl/CN0372. Follow the on-screen prompts to finish the installation. It is recommended to install all software components to the default locations.

Connect the EVAL-CN0372-PMDZ in the desired regulator configuration, and connect the circuit evaluation board to the SDP-PMD-IB1Z interposer board.

Connect the $I^2C$ interface on the EVAL-CN0372-PMDZ board to the SDP-PMD-IB1Z interposer board with the 8-pin flexible cable.

Connect the SDP-PMD-IB1Z board to the EVAL-SDP-CB1Z controller board. Apply power to the SDP-PMD-IB1Z board, and connect the EVAL-SDP-CB1Z SDP controller board to the PC via the provided USB cable. Open the evaluation software and start evaluation.

Information regarding the EVAL-SDP-CB1Z can be found in the SDP User Guide (UG-277).

### Functional Block Diagram

Figure 11 shows the functional block diagram of the test setup used for evaluating the circuit.

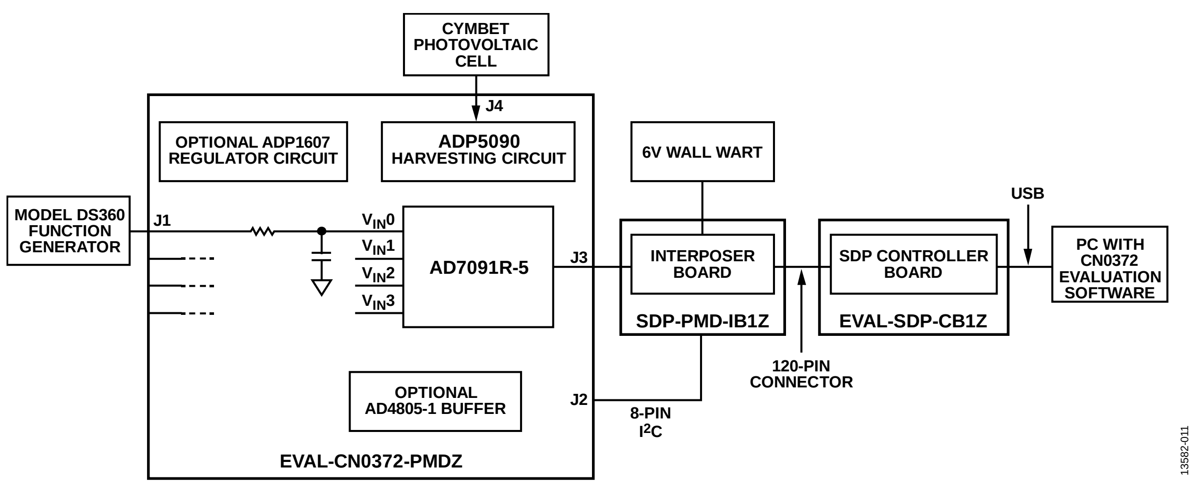


*Figure 11. Test Setup Block Diagram*

### *Power Supply Configuration*

Connect a low power, high impedance dc source (such as the Cymbet CBC-PV-01 PV cell or TEG) to the J4 terminal, and place SL4 and SL5 in Position A before opening the evaluation software. This makes use of the ADP5090 energy harvesting circuit as system supply. For the complete power supply options available, see Table 4 and Table 5.

Table 6 contains the complete description of all solder links on the EVAL-CN0372-PMDZ.

**Table 4. $V_{DD}$ Options**

| | Solder Link Position | |
|---|---|---|
| **$V_{DD}$** | **SL5** | **SL7** |
| ADP5090 SYS | A | A |
| ADP1607 $V_{OUT}$ | B | B |

**Table 5. $V_{DRIVE}$ Options**

| | Solder Link Position | |
|---|---|---|
| **$V_{DRIVE}$** | **SL3** | **SL4** |
| ADP5090 SYS | A | B |
| ADP1607 $V_{OUT}$ | B | B |
| VDD_PMOD | No connect | A |

**Table 6. Link Options**

| Link | Default | Description |
|---|---|---|
| SL1 | A | This link is used in conjunction with SL7 connected A to center.<br>A to center connects the ADP5090 BACK_UP pin to the CR2302 battery.<br>B to center connects the ADP5090 B_CHRG pin to R36 near the super capacitor. |
| SL2 | A | This link selects the ADP5090 DIS_SW pin connection.<br>A to center connects the ADP5090 DIS_SW pin to ground.<br>B to center connects the ADP5090 DIS_SW pin to PMOD_GPIO1 (Pin 9 of J3). |
| SL3 | A | This link selects the $V_{DRIVE}$ connection in conjunction with SL4.<br>A to center connects the ADP5090 SYS pin to $V_{DRIVE}$.<br>B to center connects the ADP1607 $V_{OUT}$ pin to $V_{DRIVE}$. |
| SL4 | A | This link selects the $V_{DRIVE}$ source.<br>A to center connects VDD_PMOD to $V_{DRIVE}$.<br>B to center connects $V_{DRIVE}$ to either the ADP1607 or ADP5090 output through SL3. |
| SL5 | A | This link selects the $V_{DD}$ source.<br>A to center connects the ADP5090 SYS output to $V_{DD}$.<br>B to center connects the ADP1607 output to $V_{DD}$. |
| SL6 | open | This link selects the VDD_PMOD source when SDP-I-PMOD is not used.<br>A to center connects the ADP5090 SYS output to VDD_PMOD.<br>B to center connects the ADP1607 output to VDD_PMOD. |
| SL7 | A | This link selects the CR2032 battery path.<br>A to center connects the battery to SL1 to serve as backup (SL1 connected A to center) or to charge the super capacitor (SL1 connected B to center).<br>B to center connects the battery to the ADP1607 $V_{IN}$ pin. |
| SL8 | B | This link is used to select the ADP1607 EN pin connection.<br>A to center connects EN to GND, and turns synchronous boost off.<br>B to center connects EN to the ADP1607 $V_{IN}$ pin, and turns synchronous boost on. |
| SL9 | B | This link selects the $MUX_{OUT}$ connection.<br>A to center connects $MUX_{OUT}$ to the ADA4805-1 inverting input.<br>B to center connects $MUX_{OUT}$ to the ADA4805-1 noninverting input if SL12 is in Position B. |
| SL10 | A | This link selects the $AS_0$ connection.<br>A to center connects $AS_0$ to GND.<br>B to center connects $AS_0$ to $V_{DRIVE}$. |
| SL11 | A | This link selects the $AS_1$ connection.<br>A to center connects $AS_1$ to GND.<br>B to center connects $AS_1$ to $V_{DRIVE}$. |
| SL12 | B | This link selects the optional buffer.<br>A to center connects REF to the ADA4805-1 noninverting input.<br>B to center connects $MUX_{OUT}$ to the ADA4805-1 noninverting input if SL9 is in Position B. |
| SL13 | A | This link selects the ADA4805-1 $\overline{\text{SHUTDOWN}}$ connection.<br>A to center connects $\overline{\text{SHUTDOWN}}$ to PMOD_GPIO1.<br>B to center connects $\overline{\text{SHUTDOWN}}$ to the $V_{DD}$ source selected in SL5. |

### *Setup and Test*

After the board is powered up and the evaluation software is initialized, set the ADC to convert at the desired channel. Introduce an input signal at the J1 terminal, click **Single Capture** or **Continuous Capture**, and observe the results.

To test the alert function, set **Low Limit** or **High Limit** in the evaluation software **Configure** tab and observe the LED alert indicator outside of the set range.

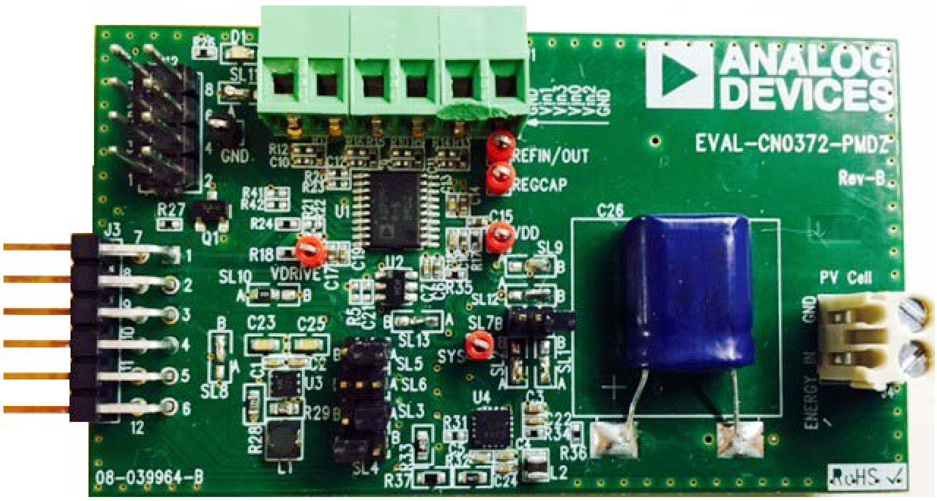


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*Figure 12. EVAL-CN0372-PMDZ PCB Photograph*

## LEARN MORE

CN-0372 Design Support Package: www.analog.com/CN0372-DesignSupport

SDP User Guide, UG-277

AN-931 Application Note. *Understanding PulSAR ADC Support Circuitry.* Analog Devices.

Walsh, Alan. *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter.* Analog Dialogue Vol. 46, No. 4. Analog Devices.

### *Data Sheets and Evaluation Boards*

AD7091R-5 Data Sheet

ADP5090 Data Sheet

ADA4805-1 Data Sheet

ADP1607 Data Sheet

## REVISION HISTORY

**9/15—Revision 0: Initial Version**

$I^2C$ refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


**CN13582-0-9/15(0)**

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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**Как с нами связаться**

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