CY4502

EZ-PD™ CCG2 Development Kit Guide

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Contents

Safety Information

Regulatory Compliance

CY4502 is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. Due to this reason, the board may interfere with other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In such cases, the user may be required to take adequate preventive measures. Make certain that this board is not used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and interfere with other apparatus in the immediate vicinity. If you detect such interference, take suitable mitigating measures.

CY4502 contains electrostatic discharge (ESD) sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY4502 boards in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

CY4502 boards are sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide the board over any surface.

CY4502 boards are expected to be handled with care, especially while connecting and disconnecting to other Type-C receptacles. Careless handling may cause PCB damage.

CY4502 bumpers are designed to work with CCG1 host and client boards. Ensure that the CY4502 board rests on a firm base while operating it with other setups. This is to avoid stress on the CY4502 PCB and Type-C connectors.

1. Introduction

Thank you for your interest in the CY4502 EZ-PD™ CCG2 Development Kit (CCG2 DVK). This DVK enables designers to evaluate the functionality of CCG2 controllers in Electronically Marked Cable Assembly (EMCA) USB Power Delivery (PD) Type-C cables. It combines hardware and documentation, and showcases the passive EMCA solution with one CCG2 per cable plug (two-chip solution) and one CCG2 per cable (one-chip solution).

CCG2 is a USB Type-C cable controller that complies with the latest USB Type-C and USB PD standards. CCG2 provides a complete USB Type-C and USB PD port control solution for passive cables, active cables, and powered accessories. It combines an industry-standard, high-performance 32-bit ARM® Cortex™-M0 CPU; communication blocks to support standard serial communication protocols such as I^2C, SPI, UART; and a complete USB Type-C transceiver including the termination resistors[a] (R_P, R_D and R_A).

This guide describes the steps to install the software related to the DVK and to operate the development board provided with the DVK. It documents different types of firmware downloading and debugging methods with detailed instructions. This guide briefly explains the hardware interfaces available on the development board.

This document assumes that you have the relevant knowledge of USB PD and the USB Type-C™ specification and its applications. It covers the following topics:

- Introduction chapter lists the DVK contents and document conventions.
- Getting Started chapter describes how to use the DVK and install the associated software.
- Kit Operation chapter explains the DVK operation.
- Hardware chapter describes the hardware details of the DVK.

1.1 Kit Contents

The CY4502 CCG2 DVK includes the following:

- CY4502 development board
- Quick start guide
- Extra Jumpers

Visit the DVK web page (www.cypress.com/CY4502) for more information. Inspect the contents of the DVK. If any parts are missing, contact your nearest Cypress sales office for further assistance.

1.1.1 Software

The CY4502 CCG2 DVK installer package available at www.cypress.com/CY4502, installs documentation, such as a user guide, a quick start guide, and release notes as well as hardware files, such as a schematic, PCB layout, and gerber.

a. See USB Type-C™ specification for more details on termination resistors.

1.1.2 Tools Not Included

- USB PD–capable/Type-C PC host: The CY4502 board works with a USB PD–capable PC host with a Type-C receptacle. If a Type-C USB PD–enabled PC is not available, the CCG1 Host board that comes with CY4501 CCG1 Development Kit, can be used in conjunction with a standard USB PC.
- USB PD–capable/Type-C device: The CY4502 board can work with a USB PD–capable device with a Type-C interface. If a Type-C USB PD–enabled device is not available, the CCG1 Client board that comes with CY4501 CCG1 Development Kit can be used in conjunction with a standard USB 3.1 (or USB3.0/USB 2.0) device.

Visit the CY4501 web page for more details on the CY4501 CCG1 Development Kit.

1.2 Additional Learning Resources

Visit the CCG2 web page for additional learning resources, including a datasheet, a technical reference manual, application notes, knowledge base articles, and training videos.

Visit the CCG1 web page for additional information on CCG1.

1.3 Document Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user-entered text, and source code: C:\ ...cd\icc\
Italics	Displays file names and reference documentation.
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]
File > Open	Represents menu paths: File > Open > NewProject
Bold	Displays commands, menu paths, and icon names in procedures: Click the File icon and then click Open.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes cautions or unique functionality of the product.

1.4 Abbreviations

Table 1-2. List of Abbreviations

Definitions and Acronyms	Meaning
Active cable	Electronically Marked Cable Assembly with a re-driver to condition USB data signals.
Biphase Mark Code (BMC)	Modification of Manchester code in which a zero has one transition and a one has two transitions.
Cable plug	Term used to describe a PD-capable element in a multidrop system addressed by SOP'/SOP'' packets. Logically, the cable plug is associated with a USB plug at one end of the cable. In a practical implementation, the electronics may reside anywhere in the cable.
Configuration channel (CC)	Single wire used by the BMC PHY layer signaling in Type-C.
CRC	Cyclic Redundancy Check - The USB PD packet header and data shall be protected by a 32-bit CRC.
DFP	Downstream facing port is a USB Type-C port on a host or a hub to which devices are connected.
DVK	Development kit.
EEPROM	Electrically erasable programmable read-only memory.
Electronically Marked Cable Assembly (EMCA)	A USB Type-C cable that uses USB PD to provide the cable's characteristics.

Definitions and Acronyms	Meaning
End Of Packet (EOP)	K-code marker used to delineate the end of a packet
I^2C	Inter-integrated circuit.
Packet	An entire unit of PD communication, including a preamble, SOP, payload, CRC, and EOP.
Passive cable	Cable with a USB plug on each end, at least one of which is a cable plug supporting SOP' that does not incorporate data bus signal conditioning circuits. Supports the Structured VDM to determine its characteristics. USB Type-C™ specification does not discuss passive cables that are not EMCAs.
PC	Personal computer.
PD	Power Delivery
SBU	Sideband Use Signals are used in the Alternate Mode supported by the USB Type-C™ specification, which enables multi-purposing of Type-C signals for alternate uses such as DisplayPort
SCL	I^2C serial clock line.
SDA	I^2C serial data line.
SDK	Software development kit.
Start of packet (SOP)	K-code marker used to delineate the start of a packet. Three SOP sequences are defined: SOP, SOP', and SOP'', with SOP* used to refer to all three.
SOP packet	PD packet that starts with an SOP.
SOP' packet	PD packet that starts with an SOP'; used to communicate with a cable plug at the near end/host side of the cable.
SOP'' packet	PD packet that starts with an SOP''; used to communicate with a cable plug at the far end/device side of the cable.
UFP	Upstream facing port is a USB Type-C port on a device or a hub that connects to a host or a hub DFP.
USB	Universal Serial Bus.
USB-IF	Universal Serial Bus Implementers' Forum.
Vendor Defined Message (VDM)	PD Data Message defined for vendor/standards usage. These are further partitioned into Structured VDM messages, where Commands are defined in this specification, and Unstructured VDM messages, which are entirely Vendor Defined.

2. Getting Started

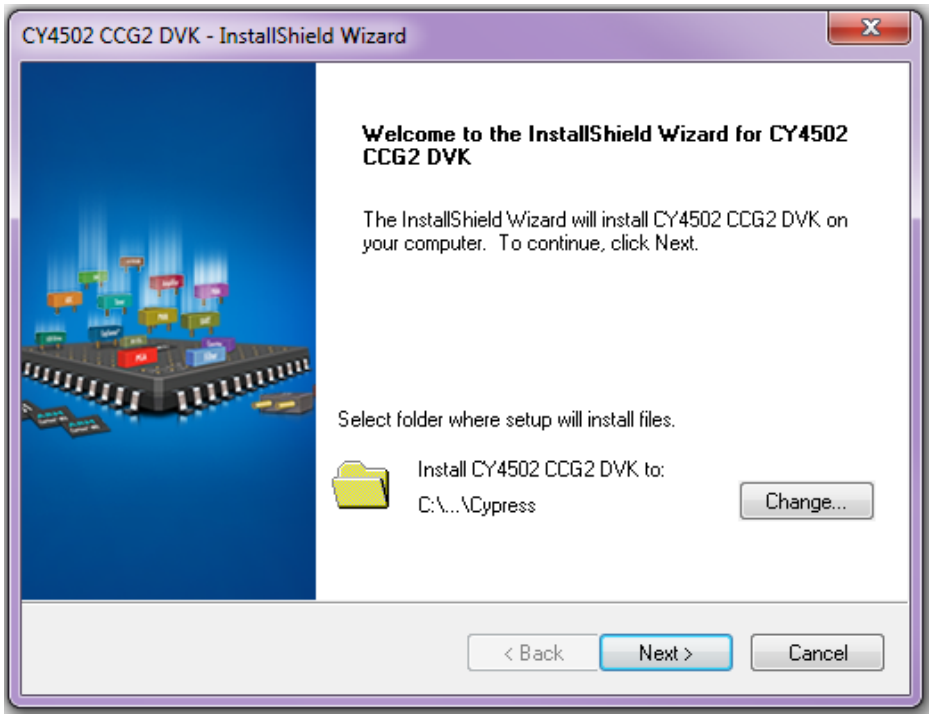
This chapter describes how to install and configure the CY4502 CCG2 DVK.

2.1 CY4502 CCG2 DVK Installation

To install the DVK software, follow these steps:

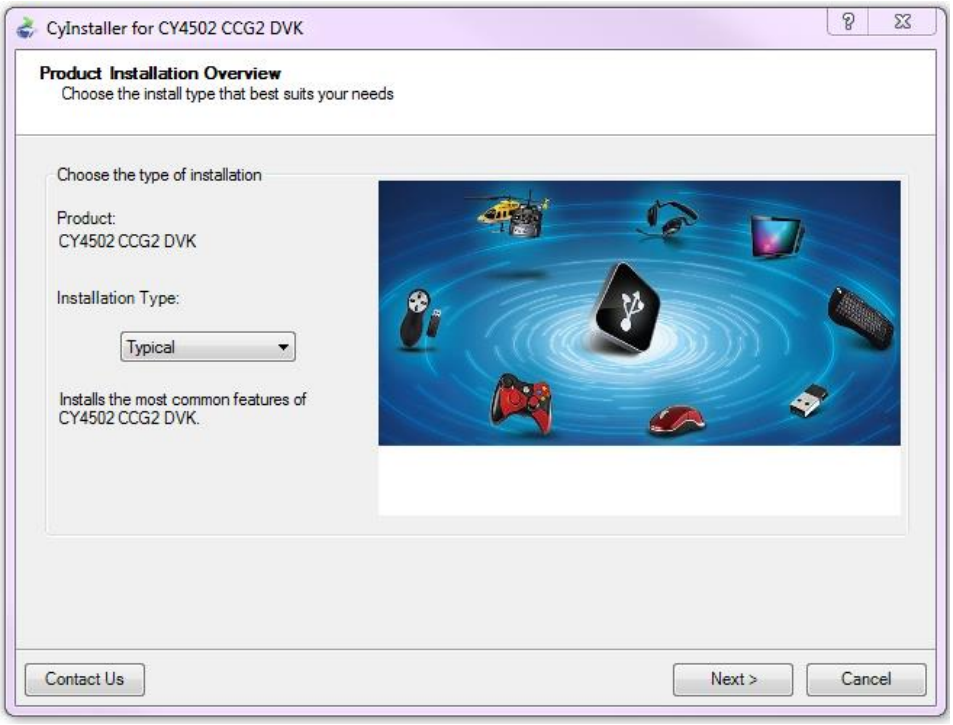
1. Download the latest CY4502 CCG2 DVK software from the CY4502 CCG2 DVK page. The installation package, *CY4502Setup.exe,* contains the kit hardware files and documents. Double-click on *CY4502Setup.exe* to start the installer. Click **Next** on the first screen to start the installation as shown in Figure 2-1.

Figure 2-1. CY4502 CCG2 DVK Installer Screen



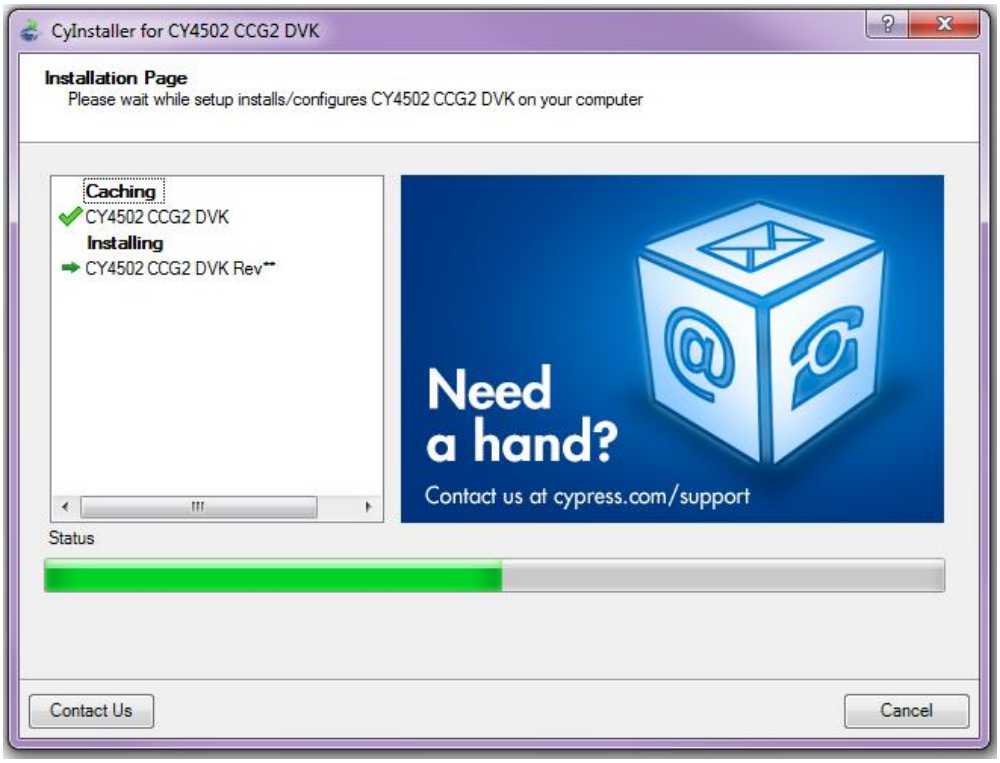
2. Select the required **Installation Type** and click the **Next** button to start the Installation Wizard (Figure 2-2). For first-time installation, it is recommended that you select “Typical” as the **Installation Type**.

Figure 2-2. Installation Wizard



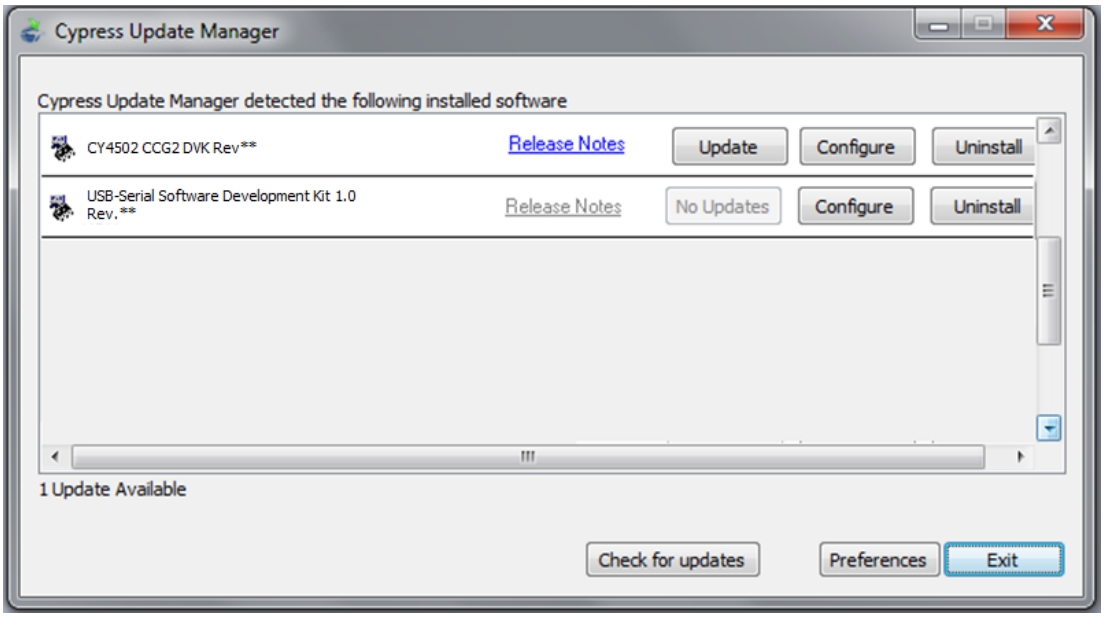
3. Read and accept the license agreement for the software components and click **Next.** The kit will now install on your machine (Figure 2-3).

Figure 2-3. Installation Progress



4. When installation is complete, you have the option to launch **Cypress Update Manager** (Figure 2-4) to ensure you have the latest DVK.

Figure 2-4. Cypress Update Manager



Notes:

- You can launch the Update Manager from Windows > Start > All Programs > Cypress > Cypress Update Manager. After the installation is complete, the contents are available at the following location: `<Install Directory>\CY4502 CCG2 DVK\<version>`.
- On the Windows 32-bit platform, the default <Install Directory> is `C:\Program Files\Cypress`; on the Windows 64-bit platform, it is `C:\Program Files(x86)\Cypress`.

2.2 Install Hardware

There is no additional hardware installation required for this kit.

2.3 Install Software

When installing the CY4502 CCG2 DVK, the installer checks if the required software is installed in the system. If the required applications are not installed, then it installs them as prerequisites.

The following software program is installed as part of the CY4502 CCG2 DVK installer:

- PSoC Programmer 3.23: Can also be downloaded from www.cypress.com/Programmer.

2.4 Uninstall Software

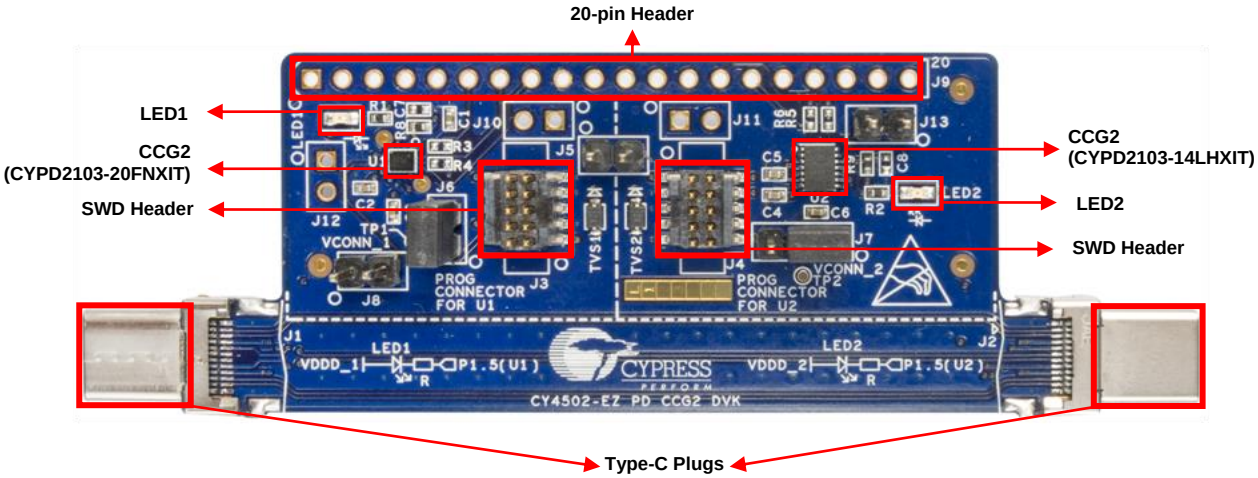
The software can be uninstalled using one of the following methods in Windows 7:

- Go to Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager; select the Uninstall button against the CY4502 CCG2 DVK.
- Go to Start > Control Panel > Programs and Features (in 'view by: Icons' option); select the Uninstall/Change button against the CY4502 CCG2 DVK.

3. Kit Operation

The CY4502 CCG2 DVK includes the CY4502 board shown in Figure 3-1.

Figure 3-1. CY4502 Board



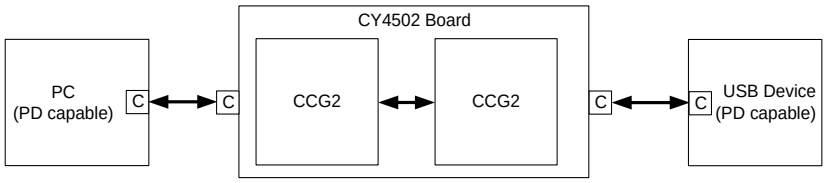
This DVK contains two CCG2 controllers (one in the CSP package and the other in the DFN package), two SWD connectors, two USB Type-C plugs, two LEDs, and footprint to populate a 20-pin header for debugging. The SWD connectors can be used to update the firmware on the CYPD2103 devices. Type-C plugs serve as connectors at either end of the cable, providing a way to connect to the Type-C receptacle at the downstream facing port (DFP) and upstream facing port (UFP). Test points are exposed in the 20-pin header, which includes CCG2 GPIOs, I^2C lines, termination resistor R_D, VCONN, and the CC lines. LEDs are used to indicate the powered chip.

The two CYPD2103 devices in the CY4502 board are shipped with factory-programmed firmware that demonstrates the functionality of CCG2 controllers in EMCA USB PD Type-C cables. The CYPD2103 firmware implements a passive EMCA cable with one CCG2 controller or two CCG2 controllers for each cable solution.

3.1 Theory of Operation

This DVK can be used to emulate a general-purpose cable with a USB Type-C plug at each end, as shown in Figure 3-2. The DVK can be configured to operate in one of three supported passive cable configurations: (1) a chip at only one end of the cable; (2) a chip at each end of the cable where only one is powered at a time; (3) a chip at each end of the cable where both are powered simultaneously. The next section covers the jumper settings required to test various configurations.

Figure 3-2. CY4502 Board as a General-Purpose USB Type-C Cable



3.2 Jumpers

The CY4502 board includes five jumpers mounted on the board. Table 3-1 describes the purpose and the default settings of the jumpers in CY4502 board (depicted in Figure 3-3).

Figure 3-3. CY4502 Board Default Jumper Settings

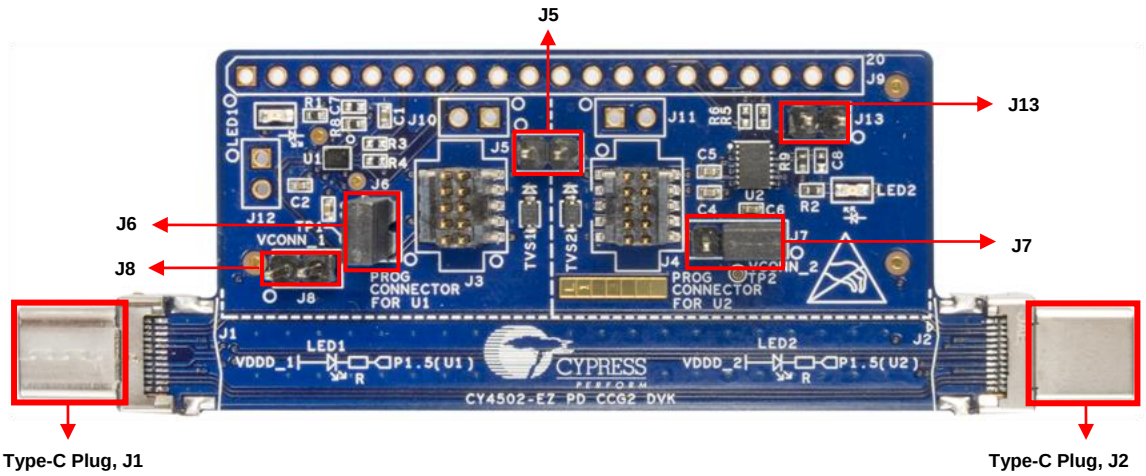


Table 3-1. CY4502 Board Jumper Settings

Function	Jumper	Purpose	Default
Configuration mode selection	J5	Jumper to select both-chip-powered configuration in the two-chip EMCA solution: Open: Default jumper position for the one-chip EMCA solution shown in Figure 3-5 or the two-chip solution with only one of the chips powered shown in Figure 3-7. Short: Jumper position for the two-chip EMCA solution with both chips powered shown in Figure 3-9. It shorts the VDDD pins of U1 and U2. **Note:** The configuration with both chips powered will work in this DVK irrespective of which Type-C plug connector, J1 or J2, is connected to the DFP.	Open
Current measurement	J6	To measure current, open the jumper and connect multimeter terminals between pins 1 and 2. The measured current is the total current consumed by the CY4502 board, including the LEDs, when the J1 connector is connected to the host (that is, when the DVK is powered using VCONN from Type-C plug, J1).	Short 1–2
Configuration mode selection	J7	Jumper used to select between the one-chip and two-chip EMCA solution: Short 2–3: Enables the single-chip solution (with only one CCG2 per cable). The VCONN signal from the Type-C plug J2 is connected to the VCONN2 pin of U1. Short 1–2: Enables the two-chip solution (with two CCG2 controllers per cable). The VCONN signal from Type-C plug J2 is connected to the VCONN1 pin of U2.	Short 1–2

Function	Jumper	Purpose	Default
SOP” response selection for U1	J8	Jumpers to enable SOP” response for U1 (CYPD2103-20FNXIT): Short: Enables SOP” response by pulling GPIO (D3) low. The CYPD2103 firmware is configured to detect the presence of the VCONN supply in the VCONN1/VCONN2 pins for determining the responsiveness to SOP packets. The CCG2 device powered through VCONN1 considers itself to be the host end of the cable (that is, connected to the DFP) and thus responds to SOP’. CCG2 powered through VCONN2 considers itself to be the device end of the cable (that is, connected to the UFP) and thus responds to SOP”. For the two-chip EMCA solution, with both CCG2 controllers powered as shown in Figure 3-9, the GPIO (pin D3) must be pulled low. Open: Disables SOP” response. CCG2 responds to SOP’ packets only. For the single-chip EMCA solution, shown in Figure 3-5, the GPIO (pin D3) must be left floating. When the GPIO (pin D3) is left floating, the CYPD2103 firmware is configured to always respond only to SOP’ packets. **Note:** According to the USB PD specification, SOP’ packets are recognized by the cable controller in one of the cable plugs attached to the DFP and are not recognized by the UFP or the other cable plug. Similarly, SOP’’ packets are recognized by the cable controller in one of the cable plugs attached to the UFP and are not recognized by the UFP or the other cable plug.	Open
SOP” response selection for U2	J13	Jumpers to enable SOP” response of U2 (CYPD2103-14LHXIT): Short: Enables SOP” response by pulling GPIO (D3) low. The CYPD2103 firmware is configured to detect the presence of the VCONN supply in the VCONN1/VCONN2 pins for determining the responsiveness to SOP packets. The CCG2 device powered through VCONN1 considers itself to be the host end of the cable (that is, connected to the DFP) and thus responds to SOP’. CCG2 powered through VCONN2 considers itself to be the device end of the cable (that is, connected to the UFP) and thus responds to SOP”. For the two-chip EMCA solution, with both CCG2 controllers powered as shown in Figure 3-9, the GPIO (pin D3) must be pulled low. Open: Disables SOP” response. CCG2 responds only to SOP’ packets. For the single-chip EMCA solution shown in Figure 3-5, the GPIO (pin D3) must be left floating. When the GPIO (pin D3) is left floating, the CYPD2103 firmware is configured to always respond only to SOP’ packets. **Note:** According to the USB PD specification, SOP’ packets are recognized by the cable controller in one of the cable plugs attached to the DFP and are not recognized by the UFP or the other cable plug. Similarly, SOP’’ packets are recognized by the cable controller in one of the cable plugs attached to the UFP and are not recognized by the UFP or the other cable plug.	Open

3.3 CCG2 Single-Chip EMCA Application

The CY4502 board can operate in a single-chip EMCA application, as shown in Figure 3-5. Follow these steps to configure the board for this mode (depicted in Figure 3-4):

1. Short pins 1 and 2 of jumper J6.
2. Short pins 2 and 3 of jumper J7.
3. Leave jumpers J8 and J13 open.
4. Leave jumper J5 open.

Follow instructions in section 3.7 to test the CY4502 board.

Figure 3-4. CCG2 Single-Chip EMCA Application Jumper Settings

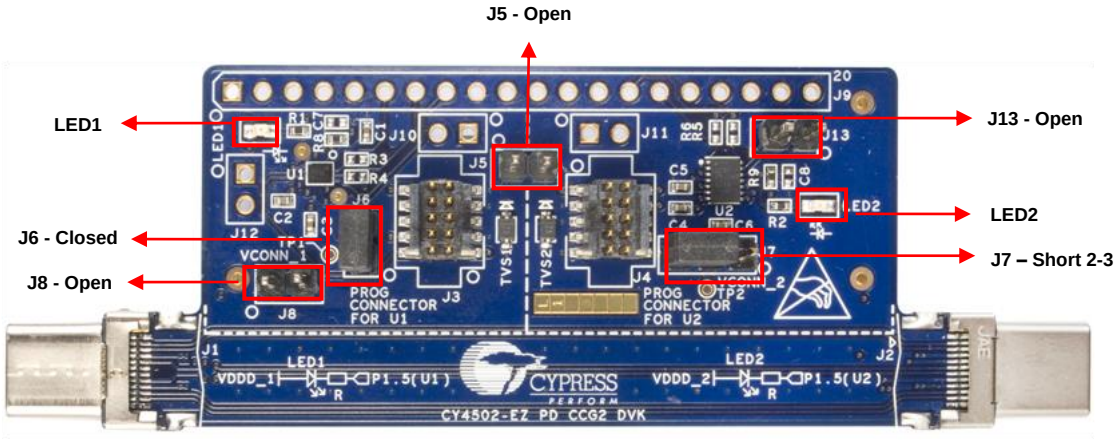
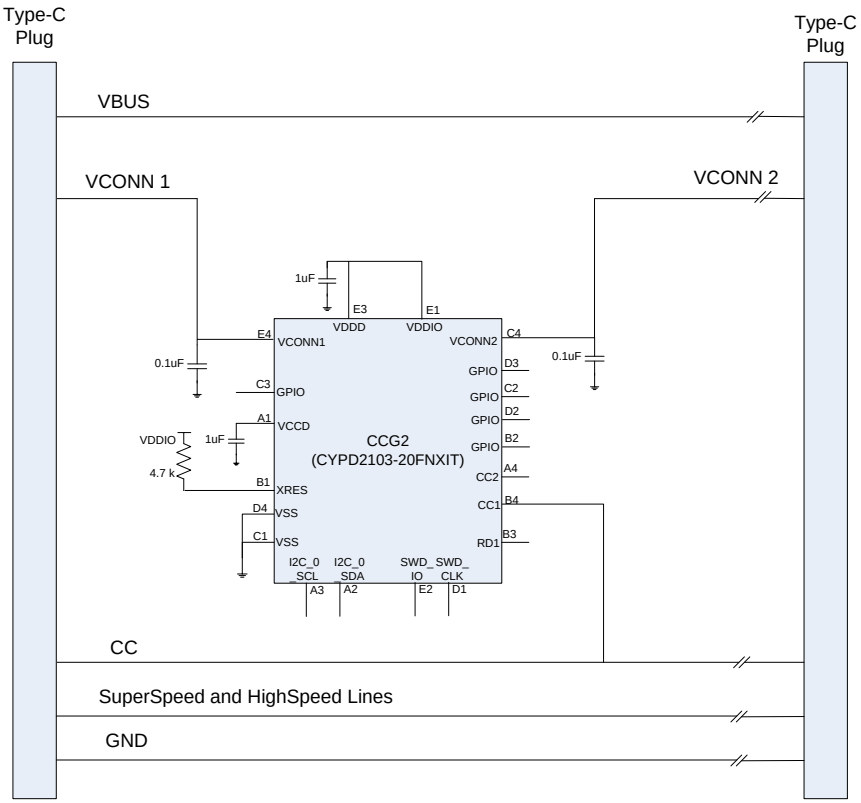


Figure 3-5. CCG2 Single-Chip EMCA Application Diagram



This EMCA solution contains CCG2 on only one of its plugs. This solution requires a single VCONN signal to run through the cable, so that the chip can be powered irrespective of which plug is connected to the host (DFP). In this case, the CCG2 device responds only to SOP' packets. For more details on this application, refer to AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2.

3.4 CCG2 Two-Chip EMCA Application (One Chip Powered)

The CY4502 board can operate in the two-chip EMCA application, with only one of the two CCG2 controllers powered, as shown in Figure 3-7. Follow these steps to configure the board for this mode (depicted in Figure 3-6):

1. Short pins 1 and 2 of jumper J6.
2. Short pins 1 and 2 of jumper J7.
3. Leave jumpers J8 and J13 open.
4. Leave jumper J5 open.

Follow instructions in section 3.7 to test the CY4502 board.

Figure 3-6. CCG2 Two-Chip EMCA Application (One Chip Powered) Jumper Settings

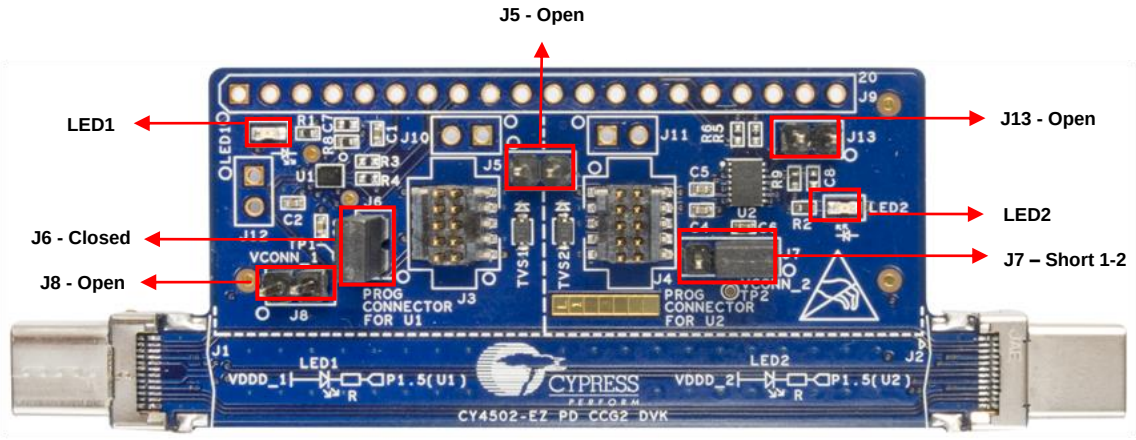
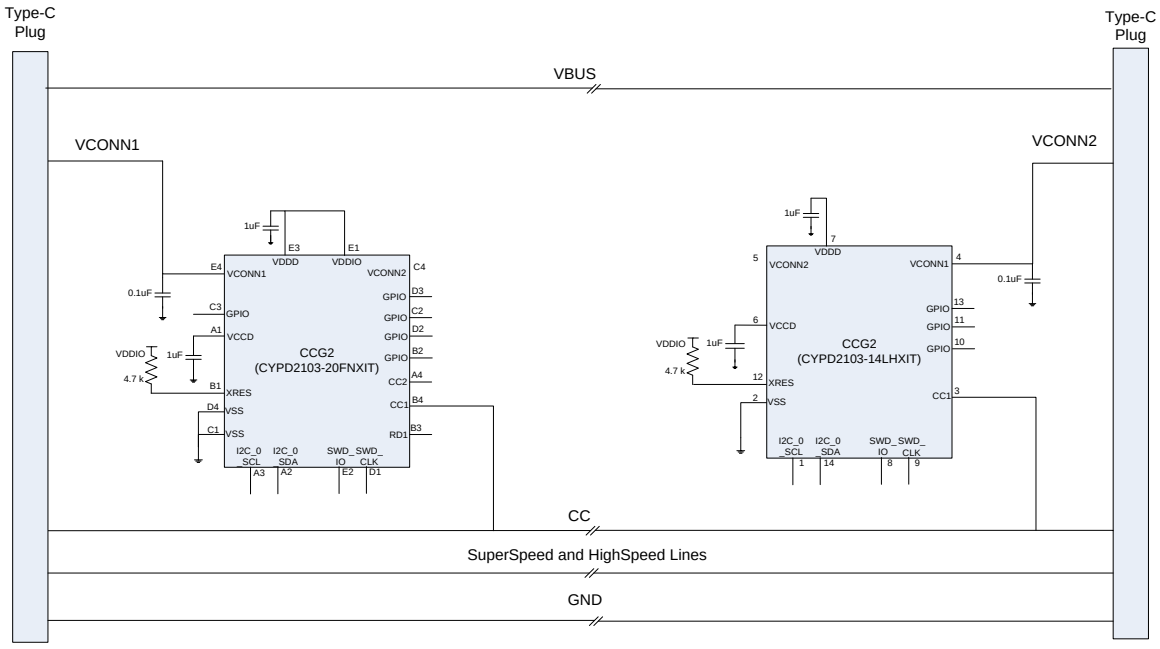


Figure 3-7. CCG2 Two-Chip EMCA Application Diagram (One Chip Powered)



This EMCA solution contains two CCG2 controllers, one in each plug. In this solution, the VCONN signal does not run through the cable. Only one CCG2 is powered at a time depending on which is nearer to the DFP that supplies VCONN. The powered CCG2 responds to SOP' packets only.

There are two advantages of using this topology:

1. Saves one wire (VCONN) running through the cable
2. Allows both plug ends to be identical, which saves on inventory costs

For more details on this application, refer to AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2.

3.5 CCG2 Two-Chip EMCA Application (Both Chips Powered)

The CY4502 board can operate in the two-chip EMCA application, with both CCG2 controllers powered, as shown in Figure 3-9. Follow these steps to configure the board for this mode (depicted in Figure 3-8):

1. Short pins 1 and 2 of jumper J6.
2. Short pins 1 and 2 of jumper J7.
3. Short pins 1 and 2 of jumpers J8 and J13.
4. Short pins 1 and 2 of jumper J5.

Follow instructions on section 3.7 to test the CY4502 board.

Figure 3-8. CCG2 Two-Chip EMCA Application (Both Chips Powered) Jumper Settings

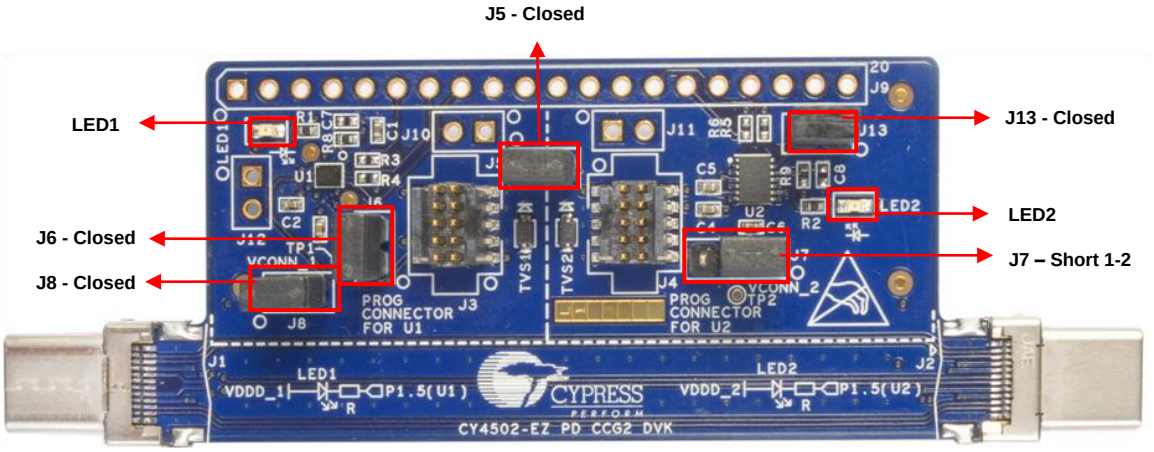
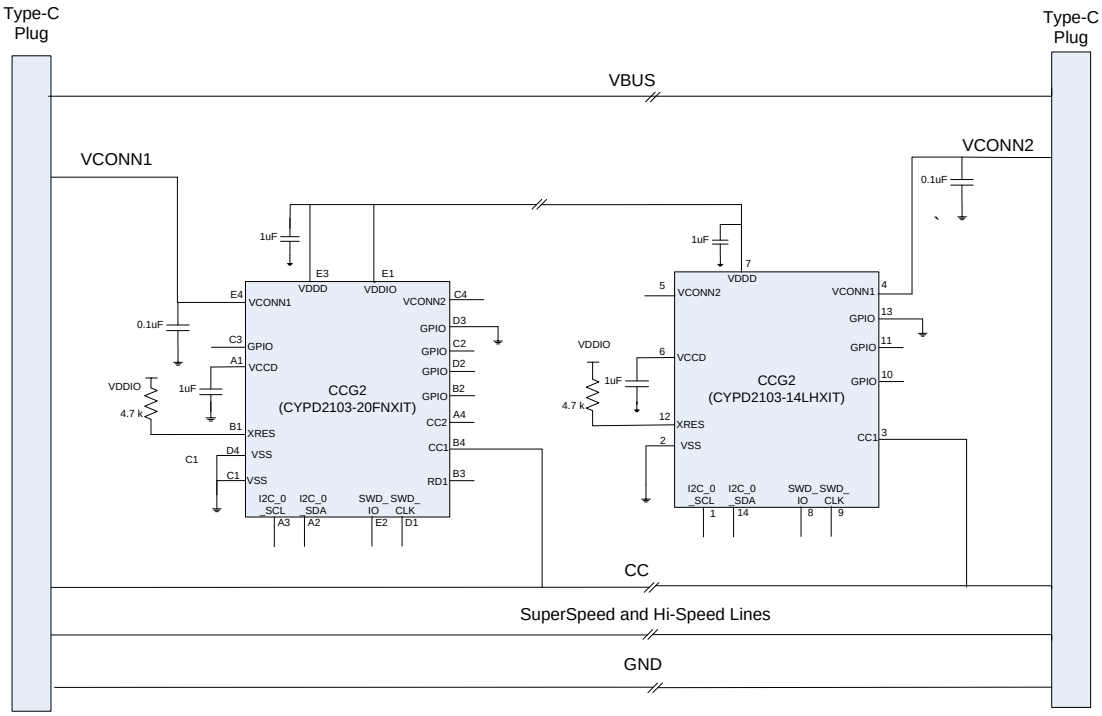


Figure 3-9. CCG2 Two-Chip EMCA Application Diagram (Both Chips Powered)



This EMCA solution contains two CCG2 controllers, one on each plug, and the power (VDDD) of both the CCG2 devices is wired across the cable (but not straight through to the other end of the plug). Even in this solution, the wiring is done such that the cable is reversible. The VCONN signal from one cable plug goes to the VCONN1 pin of the CCG2 at that end and also to the VCONN2 / VDDD pin of the CCG2 at the other end of the cable. The same applies to the VCONN signal coming from the other end of the cable. Both CCG2 devices will be powered: one through VCONN1 and the other through VCONN2 / VDDD. The CCG2 powered through VCONN1 responds to SOP' packets and the other CCG2 responds to SOP".

This configuration option of the DVK helps in evaluating firmware support for SOP". In production, this configuration will typically only be used in active cables. When the active cable requires independent management or signal conditioning at each end of the cable, separate USB PD controllers responding to USB PD structured VDMs (SOP' and SOP" packets) must be located in each plug. For more details on this application, refer to AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2.

3.6 CY4502 Jumper Configuration Summary

Table 3-2 summarizes the jumper settings needed to configure the CY4502 board for the three different applications described in sections 3.3 to 3.5

Table 3-2. CY4502 Board Jumper Settings Overview

Jumper Settings	CCG2 Single-Chip EMCA Application	CCG2 Two-Chip EMCA Application (One Chip Powered)	CCG2 Two-Chip EMCA Application (Both Chips Powered)
J5	Open	Open	Short 1-2
J6	Short 1-2	Short 1-2	Short 1-2
J7	Short 2-3	Short 1-2	Short 1-2
J8	Open	Open	Short 1-2
J13	Open	Open	Short 1-2

3.7 How to Test the CY4502 Board

Follow these steps to test the CY4502 board.

1. Connect the CY4502 board between a Type-C enabled host (such as a laptop or PC) and a Type-C enabled device with a Type-C receptacle (such as a monitor or USB hard disk). One or two LEDs glow, as listed in Table 3-3, to indicate that the CCG2 controller(s) and the CY4502 board are powered.

Table 3-3. LED Indicators in CY4502

CY4502 Configuration	Reference	Connector to Host	LED	Description
CCG2 Single-Chip EMCA Application	Section 3.3	J1	LED1	CCG2 controller, U1 is powered
		J2	LED1	CCG2 controller, U1 is powered
CCG2 Two-Chip EMCA Application (one chip powered)	Section 3.4	J1	LED1	CCG2 controller, U1 is powered
		J2	LED2	CCG2 controller, U2 is powered
CCG2 Two-Chip EMCA Application (both chips powered)	Section 3.5	J1	LED1 and LED2	Both CCG2 controllers, U1 and U2, are powered
		J2	LED1 and LED2	Both CCG2 controllers, U1 and U2, are powered

2. If a Type-C enabled host or device is not available, get a CY4501 CCG1 Development Kit and follow the steps below to test the CY4502 board. Visit the web page: http://www.cypress.com/CY4501 for more details on the CY4501 CCG1 Development Kit.:

3. Ensure that the CCG1 Host board (Figure 3-10) has the jumper settings listed in Table 3-4.

Figure 3-10. CCG1 Host board

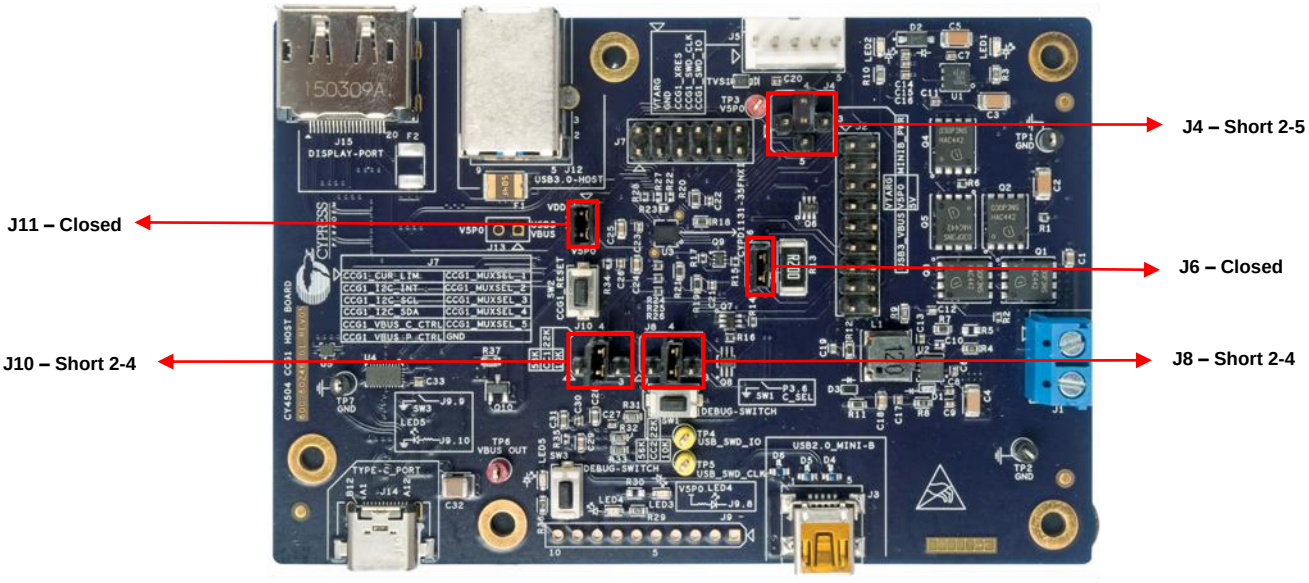


Table 3-4. Jumper Settings for CCG1 Host Board

Jumper	Position	Comments
J4	Short 2-5	Board gets powered from USB 3.0 connector (J12)
J6	Closed	Provision for measuring current consumption on VCONN
J8	Short 2–4	CC2 Rp selection for 1.5 A current advertisement
J10	Short 2–4	CC1 Rp selection for 1.5 A current advertisement
J11	Closed	Provision for measuring current consumption of CCG1

4. Ensure that the CCG1 Client board (Figure 3-11) has the jumper settings listed in Table 3-5.

Figure 3-11. CCG1 Client board

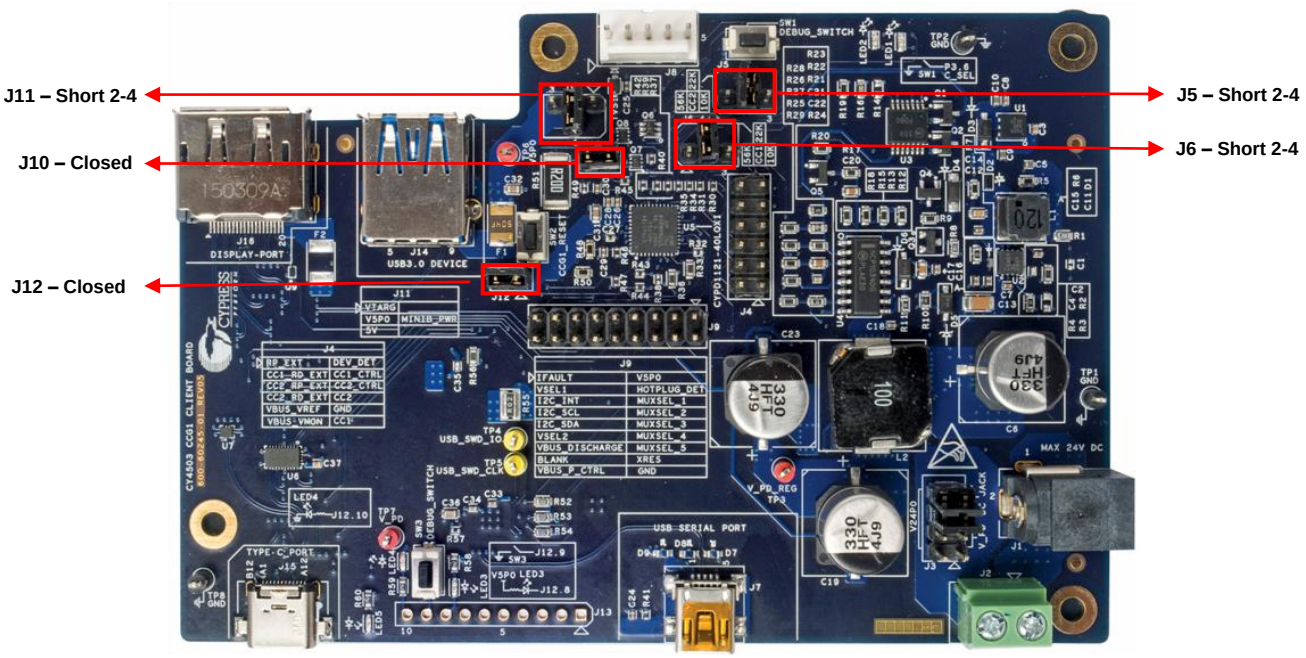


Table 3-5. Jumper Settings for CCG1 Client board

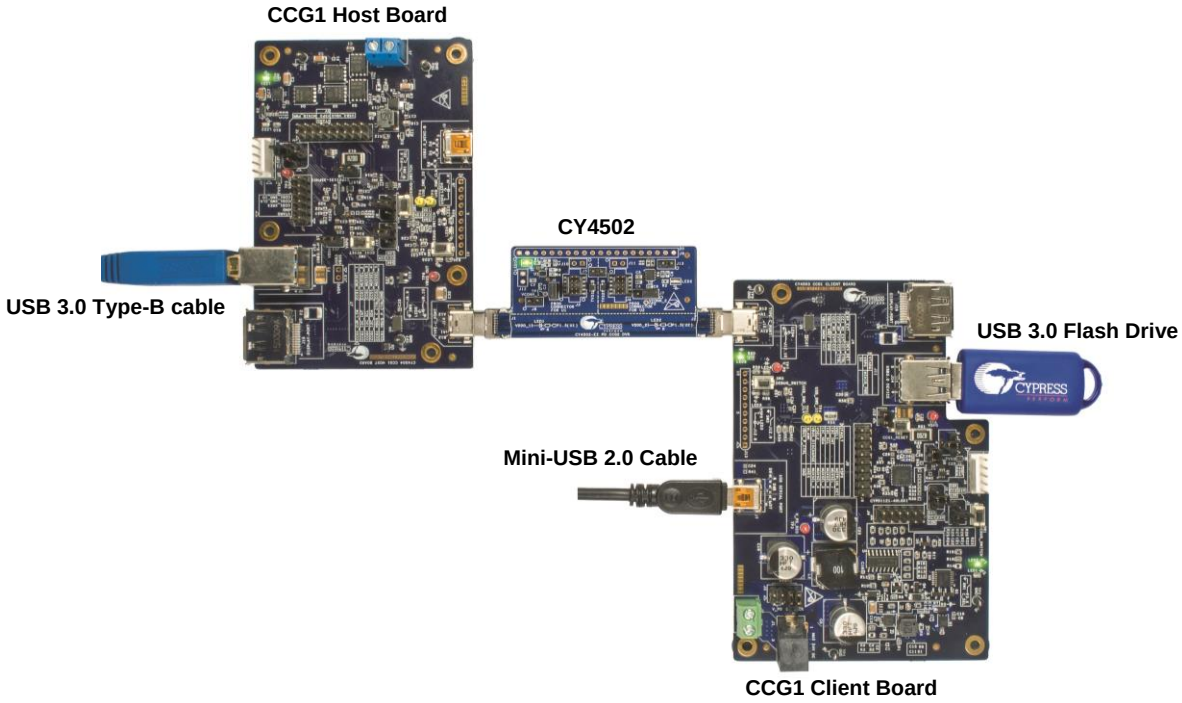
Jumper	Position	Comments
J5	Short 2–4	CC2 Rp selection for 1.5 A current advertisement
J6	Short 2–4	CC1 Rp selection for 1.5 A current advertisement
J10	Closed	Provision for measuring current consumption on VCONN
J11	Short 2–4	Board gets powered from mini USB connector (J7).
J12	Closed	Provision for measuring current consumption of CCG1

Note: Other jumpers on the CCG1 Client board, not listed in Table 3-5, can be retained in any position for testing the CY4502 board. For more details on the CCG1 Client board, refer to the CY4501 CCG1 Development Kit page.

5. Configure the CY4502 board for any of the applications discussed in sections 3.3 to 3.5 .
6. Connect the CCG1 Host board to the PC (USB Host) using a USB 3.0 A-B cable at connector J12. LED1 on the CCG1 Host board glow to indicate that the board is powered.
7. Power the CCG1 Client board by connecting a USB Mini cable at connector J7. LED2 on the CCG1 Client board glows to indicate that the board is powered.
8. Connect one of the Type-C plugs of the CY4502 board to the CCG1 Host board at connector J14 of the CCG1 Host board.

9. Connect the other Type-C plug of the CY4502 board to connector J15 of the CCG1 Client board.
10. One or two LEDs on the CY4502 board glow, as in Table 3-3, to indicate that the CY4502 board is powered and also to indicate which CCG2 controller has been powered.

Figure 3-12. Testing CCG2 Using CCG1 Development Kit



11. Connect a USB flash drive to J14 on the CCG1 Client board to test data transfer across this Type-C ecosystem.
12. Execute file operations from/to the USB flash drive and check the data integrity.

3.8 Programming the CCG2 Device

CCG2 devices can be upgraded to keep pace with USB-IF specification changes. The on-chip 32-KB flash can be programmed using the serial wire debug (SWD) interface or over the Type-C Configuration channel (CC signal).

3.8.1 Programming the CCG2 Device Using PSoC Programmer and MiniProg3

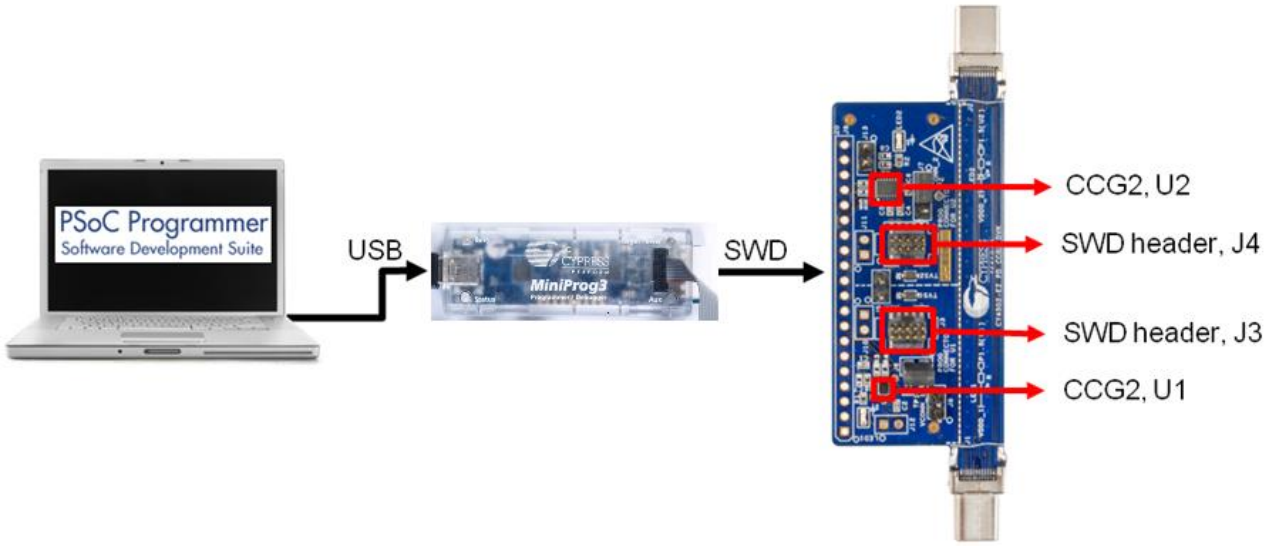
A firmware upgrade using the SWD interface can be done using a PC running PSoC Programmer software and a MiniProg3 programmer to program either CCG2, as shown in Figure 3-13. This method of programming can be used on a paddle card[b] equipped with the SWD pins or header and is typically used during product development.

Notes:

- SWD header J3 should be used for programming U1 and SWD header J4 should be used for programming U2

b. In EMCA applications, CCG2 and associated circuits are assembled into one or both ends of a cable called a “plug”. Inside each plug housing or mold, the chips are assembled on PCBs called “paddle cards.”

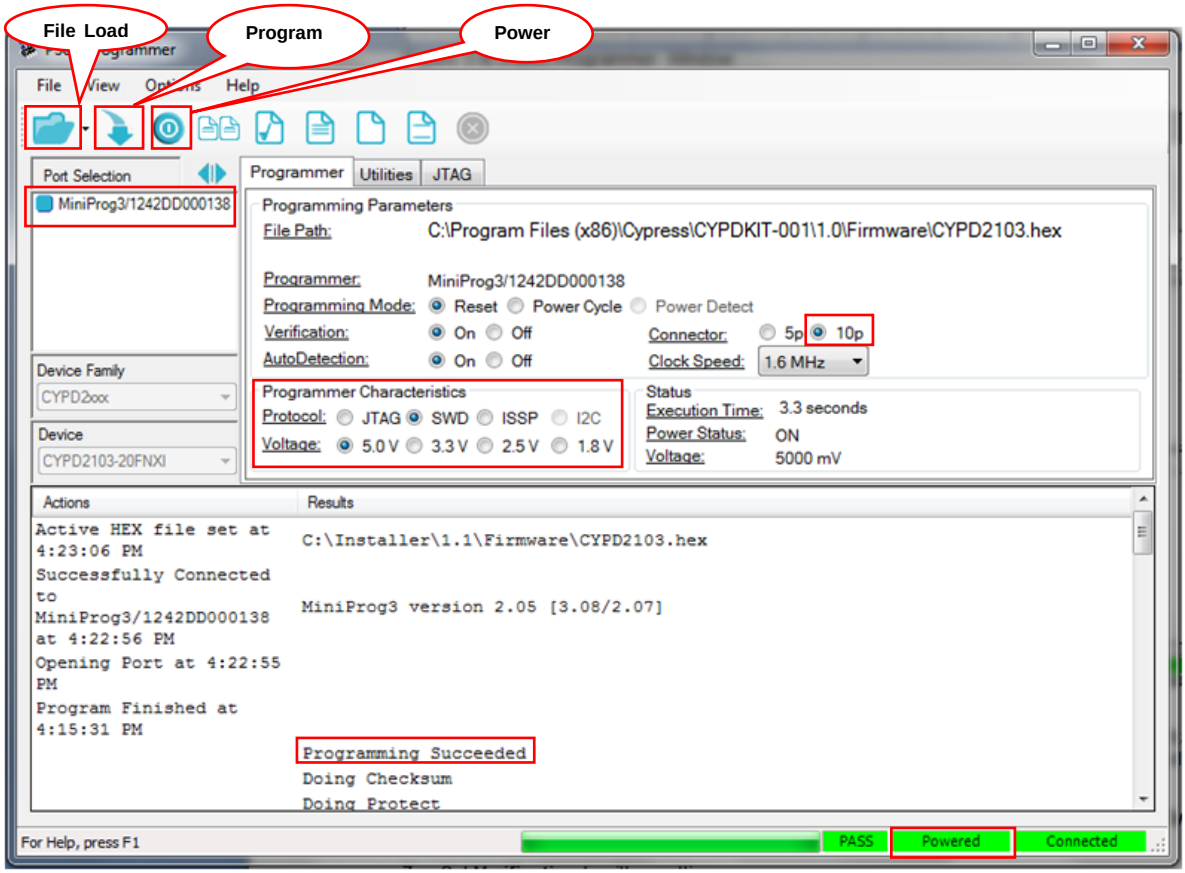
Figure 3-13. Upgrade over SWD (Using MiniProg3)



PSoC Programmer is installed as part of the CY4502 CCG2 DVK installer. Obtain a MiniProg3 Program and Debug Kit from the Cypress webpage. To use PSoC Programmer, follow these steps:

1. Start PSoC Programmer from Start > All Programs > Cypress > PSoC Programmer.
2. Connect one end of the USB cable to the MiniProg3 programmer and connect the other end to the PC.
3. Connect the MiniProg3 to the appropriate SWD header (J3/ J4) on the board using the supplied ribbon cable.
4. Select the MiniProg3 from the Port Selection window, as shown in Figure 3-14.

Figure 3-14. PSoC Programmer Window



5. Ensure that the settings on PSoC Programmer are as highlighted in Figure 3-14.
6. Click the **File Load** button and point to the appropriate hex file to load it.

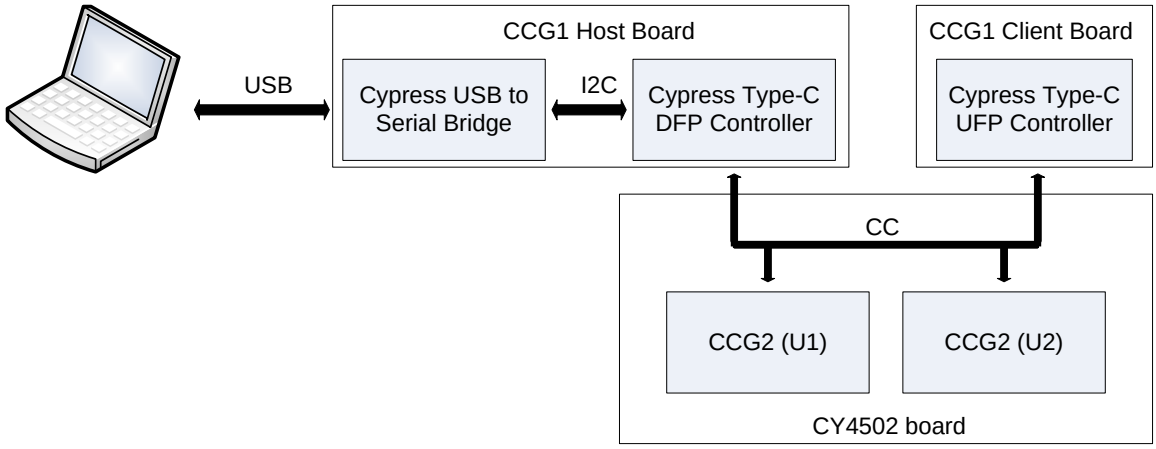
Note: Firmware images are not included as part of the CY4502 CCG2 DVK installer. The firmware image for the CSP (CYPD2103-20FNXIT) and the DFN (CYPD2103-14LHXIT) parts are different. Contact Cypress for the appropriate CCG2 firmware images.

7. The status message at the bottom right of the PSoC Programmer window will indicate if the board is powered or not.
8. If the board is not powered yet, click on the Power button and verify the status message as in step 7.
9. Use the Program button to program the hex file on to the chip.
10. When the file is successfully programmed, “Programming Succeeded” appears in the **Actions** window.

3.8.2 Programming the CCG2 Device Using a CCG1 Host Board over the CC Line

A firmware upgrade application, *EZ-PD Configuration Utility*, is provided by Cypress and can be downloaded from www.cypress.com/ezpdutility. The EZ-PD Configuration Utility is a Microsoft Windows Application, which can be used to configure and program CCG2 devices in the USB Type-C cable directly over the CC line with the help of the CCG1 Host and Client boards. This method can be deployed by cable manufacturers to provide upgrades to the user or to program the firmware after the cable assembly is manufactured. The CCG2 device allows the firmware of the assembled cable to be upgraded over the CC line through a built-in bootloader.

Figure 3-15. Setup for Programming through the CC Channel



The USB-Serial bridge in the CCG1 Host board acts as a USB-I^{2}C master bridge. The USB-Serial bridge is used to receive USB vendor commands and translate them into a set of I^{2}C-based commands. These I2C commands are addressed to the CCG2 controller, which translates them into the required USB-PD messages. Standard DFP implementations can only initiate USB-PD commands when a USB-PD power contract is in place. Since the DFP cannot setup a power contract while a power consumer (Upstream Facing Port or UFP) is not present, programming the CCG2-based EMCA cable requires both a host (DFP) and client (UFP) to be connected, as illustrated in Figure 3-15.

To upgrade the CCG2 firmware over the CC line, follow the steps described in EZ-PD Configuration Utility User Manual which can be found from the location '`C:\Program Files (x86)\Cypress\EZ-PD Configuration Utility\User Manual`' after installing EZ-PD Configuration utility.

Note: Firmware images are not included with the CY4502 CCG2 DVK installer. Firmware image for the CSP (CYPD2103-20FNXIT) and the DFN (CYPD2103-14LHXIT) parts are different. Contact Cypress for the appropriate CCG2 firmware images.

4. Hardware

This chapter describes the hardware interfaces and circuits available on the development board, as shown in Figure 4-1. It covers the following topics:

- CCG2 controllers
- Type-C plugs
- SWD connectors
- Headers

Figure 4-1. CY4502 board Hardware Block Diagram

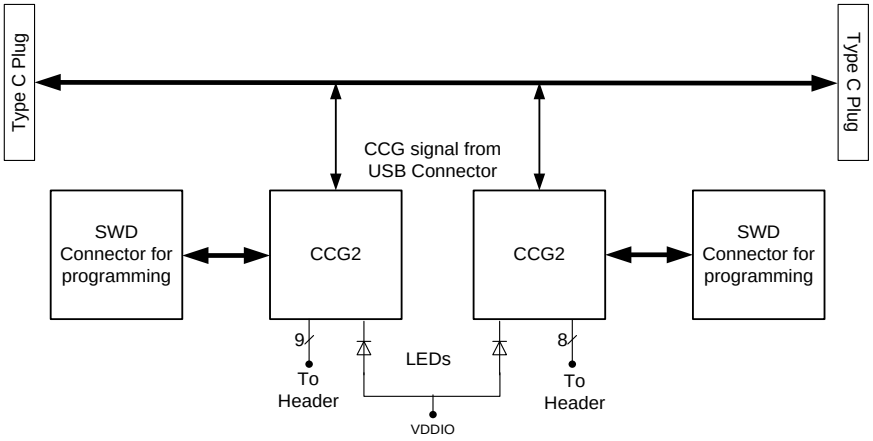
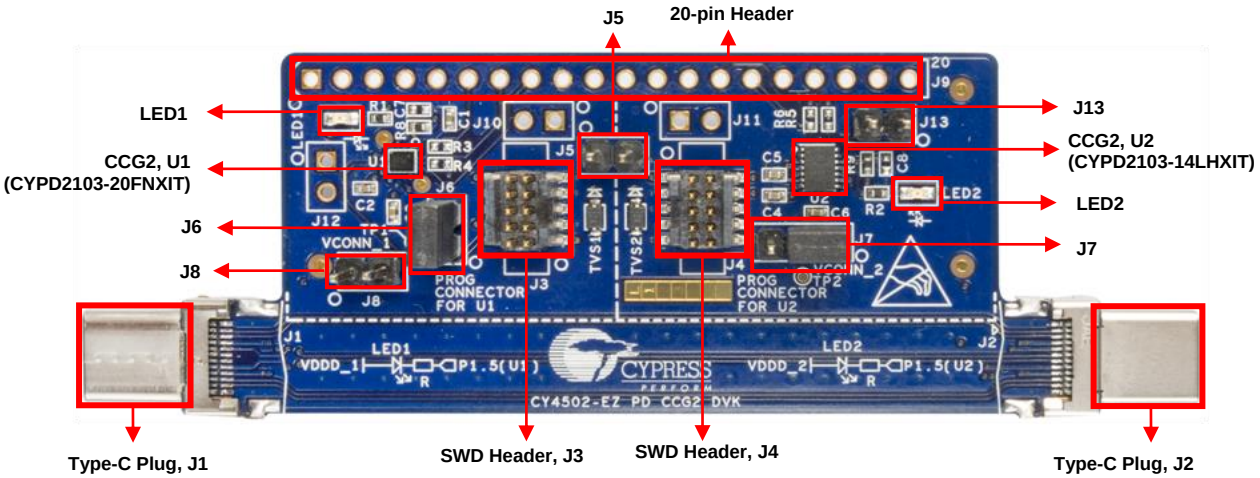


Figure 4-2 shows the CY4502 board with all the relevant blocks marked.

Figure 4-2. CY4502 Board



4.1 CY4502 Board Details

The CY4502 board hardware consists of the following components:

- U1: CCG2 controller in CSP package (CYPD2103-20FNXIT)
- U2: CCG2 controller in DFN package (CYPD2103-14LHXIT)
- LED1: Power (VCONN) indicator of U1
- LED2: Power (VCONN) indicator of U2
- J5: Jumper to select configuration with both chips powered in the two-chip EMCA solution
- J6: Power measurement jumper
- J7: Jumper to select one-chip/two-chip EMCA solution
- J8/J13: Jumpers to select the responsiveness to SOP” packets for U1/ U2 respectively
- J1/J2: USB Type-C plugs
- J3/J4: SWD connectors
- J9: 20-pin header (Not mounted on the DVK)

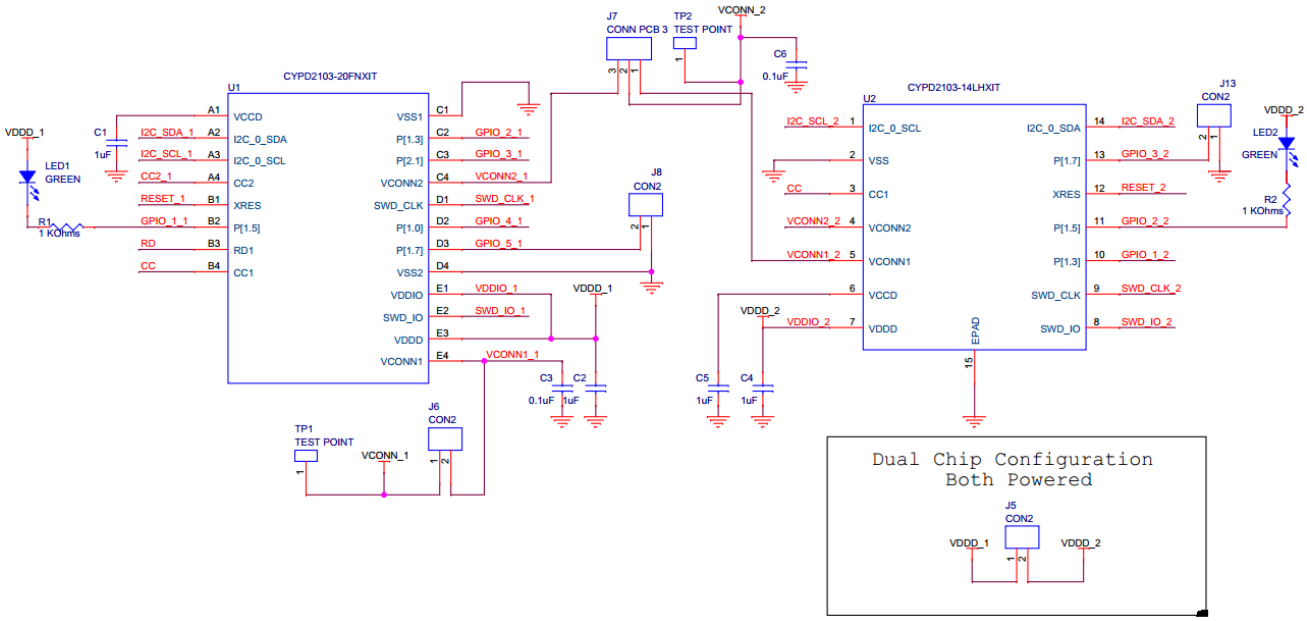
4.2 CCG2 Controller

The CY4502 board contains two CCG2 controllers:

- U1: CCG2 controller in CSP package (CYPD2103-20FNXIT)
- U2: CCG2 controller in DFN package (CYPD2103-14LHXIT)

This DVK emulates a passive EMCA solution with the option to select one-chip (one CCG2 for the whole cable) and two-chip (one CCG2 per cable plug) solutions. This EMCA solution contains two CCG2 devices (U1 and U2), one for each plug, as shown in Figure 4-3.

Figure 4-3. CCG2 Devices



4.3 USB Type-C Plug

The CY4502 board contains two USB Type-C plugs: J1 and J2.

Figure 4-4 shows the USB 3.0 pins (SS_TX_M, SS_TX_P, SS_RX_P, and SS_RX_M), USB 2.0 pins (D+ and D–), cable power signals (VBUS and GND), sideband use (SBU) signals (SBU1, SBU2), and the configuration channel (CC/ VCONN) that are available on the J1 and J2 USB Type-C plugs. VCONN acts as the local supply for the cable. J1 and J2 serve as the connectors at either end of the cable and provide a way to connect to Type-C receptacles. Figure 4-5 depicts the USB Type-C plug signals.

Figure 4-4. Type-C Plugs

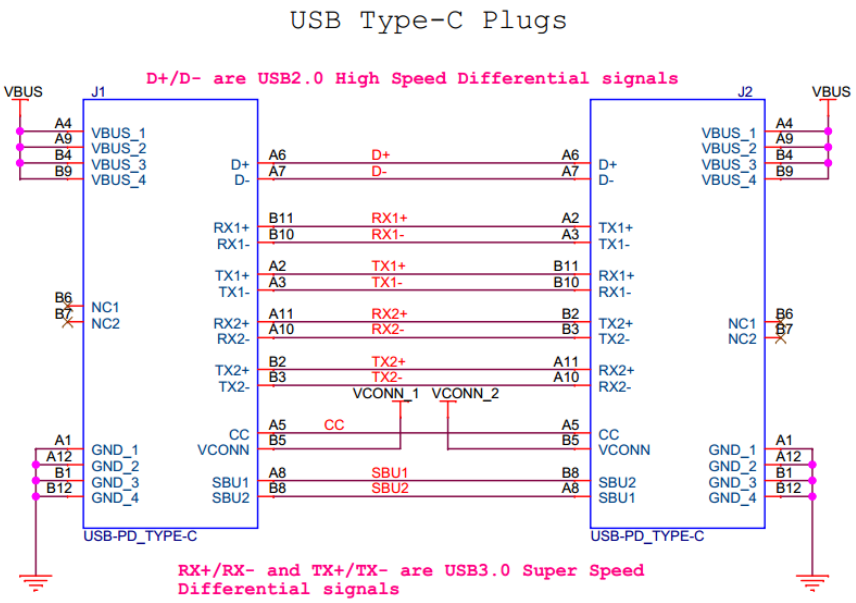
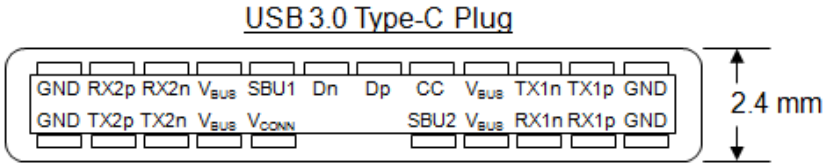


Figure 4-5. USB Type-C Plug Interface (Front View)



Only one CC pin is connected through the cable to establish the signal orientation. The other CC pin is repurposed as VCONN for powering the electronics in the USB Type-C plug. Also, only one set of USB 2.0 D+/D− wires is implemented in a USB Type-C cable. SBU signals are used in Alternate mode, supported by the USB Type-C™ specification. The USB Type-C specification supports Alternate mode, which enables multipurposing Type-C signals for alternate uses such as the display port. It allocates lanes to those other signals as necessary, with muxes at either end (host/device) handling the switching to determine which signals are on which lanes and where they need to come from or go to. Refer to the USB Type-C™ specification for more details on Alternate mode. In Alternate mode, activity on the SBU lines does not interfere with USB PD BMC communications. SBU signals are not implemented for USB 3.0/USB 2.0-only cable applications. Table 4-1 summarizes the signals used on the USB Type-C connectors.

Table 4-1. USB Type-C Plug Signals

Signal Group	Signal	Description
USB 3.1	SSTXp1, SSTXn1 SSRXp1, SSRXn1 SSTXp2, SSTXn2 SSRXp2, SSRXn2	The SuperSpeed USB serial data interface defines one differential transmit pair and one differential receive pair. On a USB Type-C plug and receptacle, two sets of SuperSpeed USB signal pins are defined to enable the plug flipping feature.
USB 2.0	Dp, Dn	The USB 2.0 serial data interface defines a differential pair. On a USB Type-C receptacle, two sets of USB 2.0 signal pins are defined to enable the plug flipping feature.
Configuration	CC	CC channel in the plug used for connection detect and interface configuration
Auxiliary signals	SBU1, SBU2	Sideband use
Power	VBUS	USB cable bus power
	VCONN	Type-C cable plug power
	GND	USB cable return current path

Note: Four capacitors are needed on the VBUS pins of the Type-C connector according to the USB Type-C™ specification. A 10-nF bypass capacitor (minimum voltage rating of 30 V) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitors should be placed as close as possible to the VBUS pins of the Type-C connector.

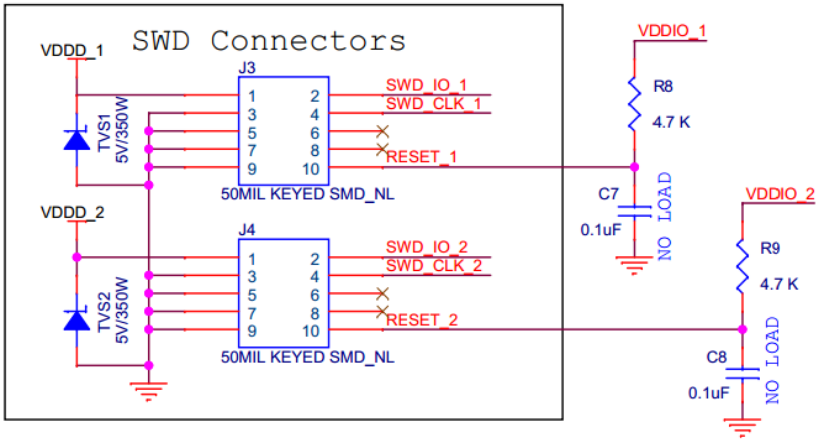
In the CY4502 board, the capacitors on the VBUS pins are not mounted as the parasitic capacitance itself sums up to > 10 nF.

4.4 SWD Connector

The CY4502 board contains two SWD connectors for programming: J3 and J4.

The SWD connectors are used to program and debug the CCG2 devices. SWD_CLK is the clock coming from the master (programmer) and SWD_IO is the bidirectional data bus used to transmit or receive data from the CCG2 device, as shown in Figure 4-6. The RESET signal is used to pull down the RESET pin of the CCG2 device to bring it into the Programming mode.

Figure 4-6. SWD Connectors for Programming

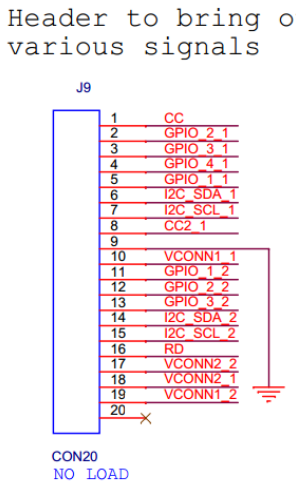


4.5 20-pin Header

The CY4502 board contains one 20-pin header, J9, that is not mounted on the DVK.

The CCG2 GPIOs and I^2C lines are exposed on the 20-pin header (Figure 4-7). The R_D line from U1, VCONN, and CC lines are also accessible as test points for debugging.

Figure 4-7. 20-Pin Header

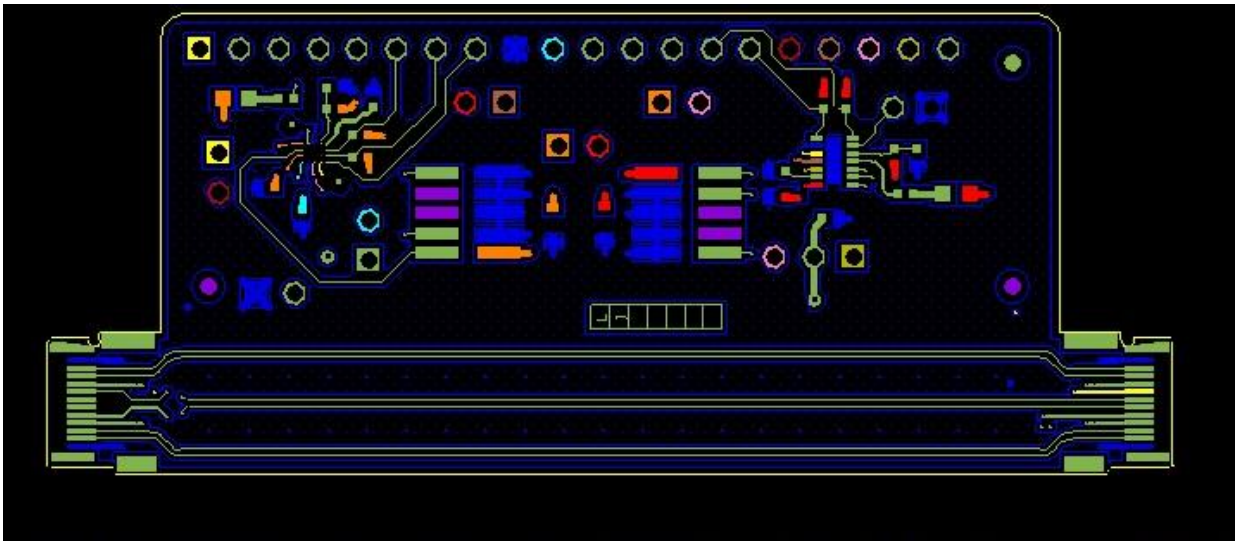


Appendix A: Troubleshooting Guide

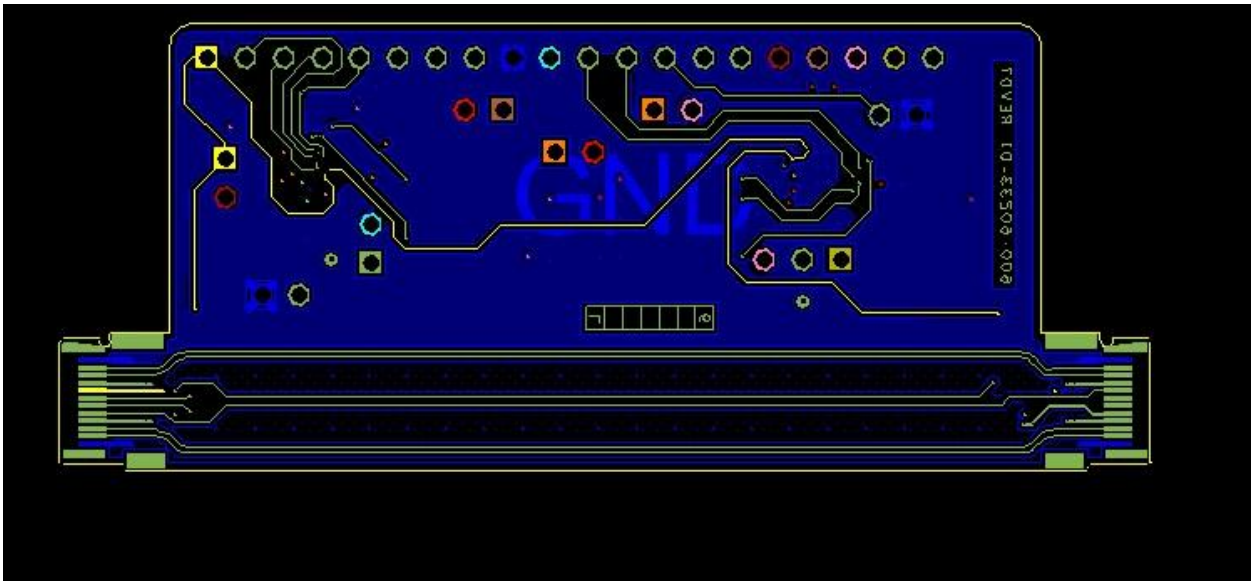
Problem	Possible Cause	Possible Solution
CY4502 board does not work for one-chip solution.	Incorrect jumper settings	Ensure jumper settings are in accordance with those in CCG2 Single-Chip EMCA Application.
CY4502 board does not work for two-chip solution with only one chip powered.	Incorrect jumper settings	Ensure jumper settings are in accordance with those in CCG2 Two-Chip EMCA Application (one chip powered).
CY4502 board does not work for two-chip solution with both chips powered.	Incorrect jumper settings	Ensure jumper settings are in accordance with those in CCG2 Two-Chip EMCA Application (both chips powered).
LED1 does not glow when connected in one-chip/ two-chip configuration	Corrupted flash or blank flash of CCG2 controller (U1)	Reprogram the CCG2 controller (U1) as explained in section 3.7.
LED2 does not glow when connected in one-chip/ two-chip configuration	Corrupted flash or blank flash of CCG2 controller (U2)	Reprogram the CCG2 controller (U2) as explained in section 3.7.
LED1 and LED2 glow together in one-chip configuration.	Incorrect jumper settings	Ensure jumper settings are in accordance with those in CCG2 Single-Chip EMCA Application.
LED1 and LED2 glow together in two-chip configuration with only one powered.	Incorrect jumper settings	Ensure jumper settings are in accordance with those in CCG2 Two-Chip EMCA Application (one chip powered).

Appendix B: PCB Layout

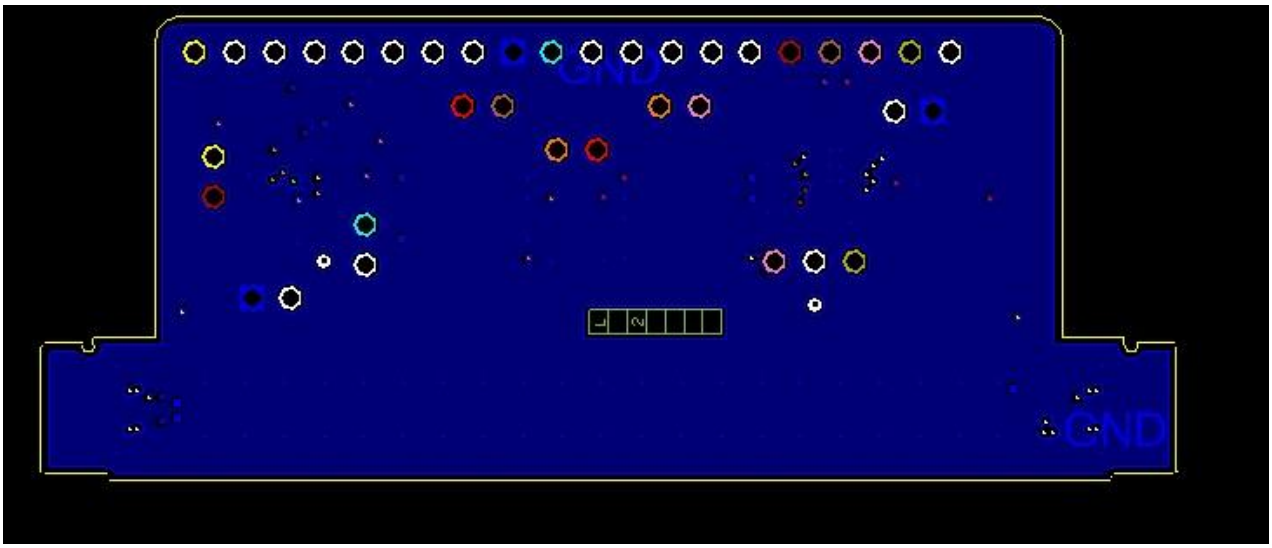
B.1 Top Layer



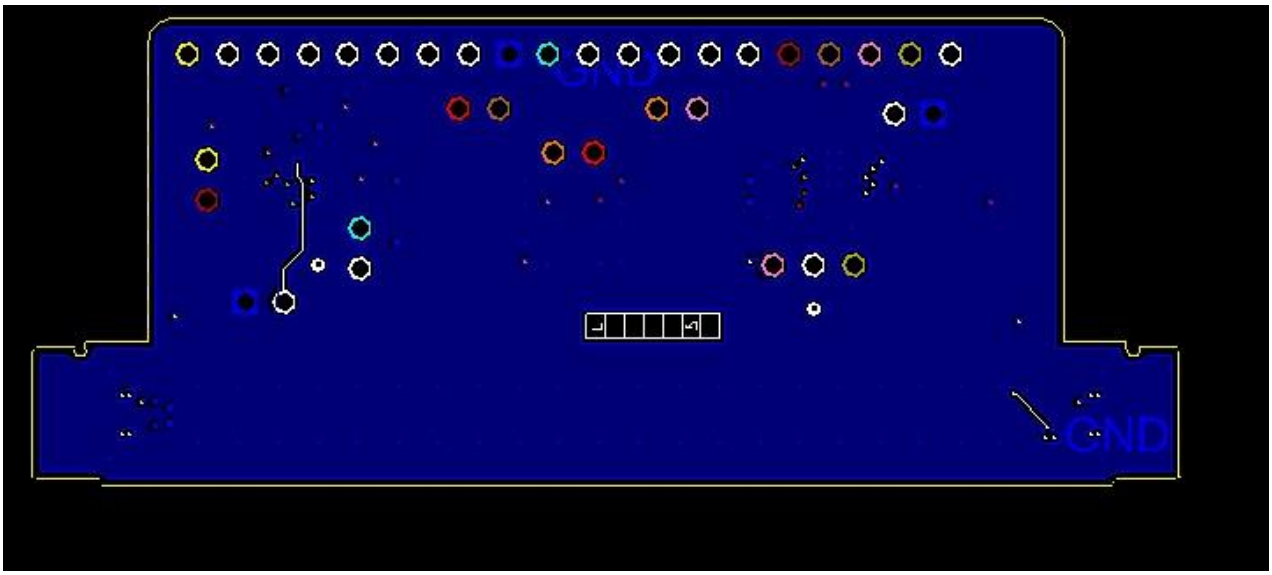
B.2 Bottom Layer



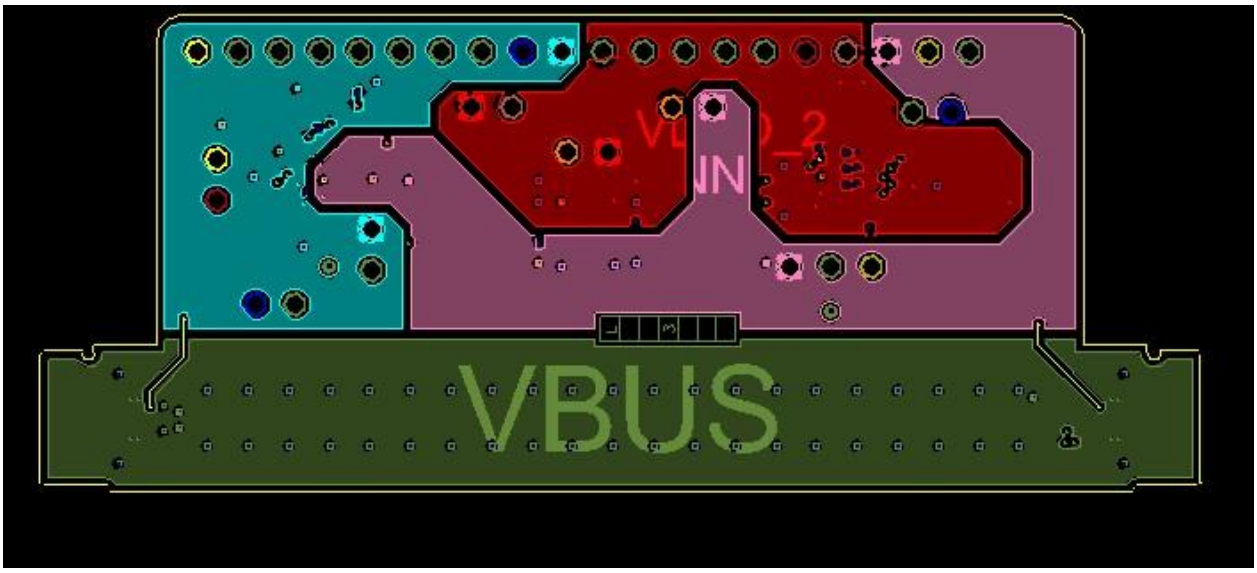
B.3 Ground Layer 1



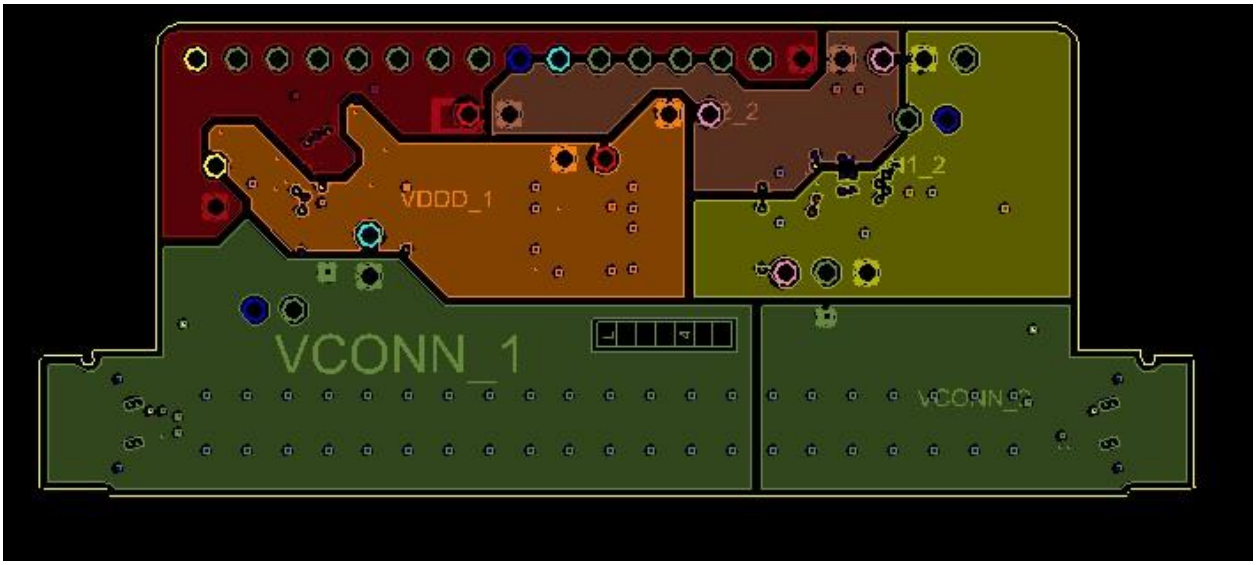
B.4 Ground Layer 2



B.5 Power Layer 1



B.6 Power Layer 2



Revision History

Document Revision History

Document Title: CY4502 EZ-PD™ CCG2 Development Kit Guide Document Number: 001-96601			
Revision	**Issue Date**	**Origin of Change**	**Description of Change**
**	04/14/2015	GAYA	Initial version of kit guide.
*A	04/17/2015	GAYA	Installer images and template updated.
*B	04/21/2015	GAYA	Updated How to Test the CY4502 Board.
*C	05/06/2015	RRSH	Updated Figure 3-13.
*D	05/29/2015	GAYA	Removed PSOC programmer 3.22 related known limitation. Added handling instruction for avoiding PCB and type-c connector stress. Updated Figure 3-16.
*E	06/11/2015	RRSH	Updated Kit Contents.
*F	09/22/2015	GAYA	Updated Table 3-4 and Table 3-5. Updated section 3.8.2.
*G	05/23/2017	AESATMP9	Updated logo and copyright.
*H	03/07/2018	GAYA	Updated copyright notice.

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- Поставка образцов и прототипов;
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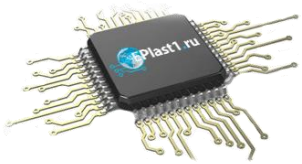

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