ZL30117

SONET/SDH OC-48/OC-192 Line Card Synchronizer

Data Sheet

June 2006

A full Design Manual is available to qualified customers. To register, please send an email to TimingandSync@Zarlink.com.

Ordering Information

ZL30117GGG	64 Pin CABGA	Trays
ZL30117GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

Features

- Synchronizes with standard telecom system references and synthesizes a wide variety of protected telecom line interface clocks that are compliant with Telcordia GR-253-CORE and ITU-T G.813
- Internal APLL provides standard output clock frequencies up to 622.08 MHz that meet jitter requirements for interfaces up to OC-192/STM-64
- Programmable output synthesizer generates clock frequencies from any multiple of 8 kHz up to 77.76 MHz in addition to 2 kHz
- Digital Phase Locked-Loop (DPLL) provides all the features necessary for generating SONET/SDH compliant clocks including automatic hitless reference switching, automatic mode selection (locked, free-run, holdover), and selectable loop bandwidth
- Provides 3 reference inputs which support clock frequencies with any multiples of 8 kHz up to 77.76 MHz in addition to 2 kHz
- Provides 3 sync inputs for output frame pulse alignment
- Generates several styles of output frame pulses with selectable pulse width, polarity, and frequency
- Configurable input to output delay, and output to output phase alignment
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
- Supports IEEE 1149.1 JTAG Boundary Scan

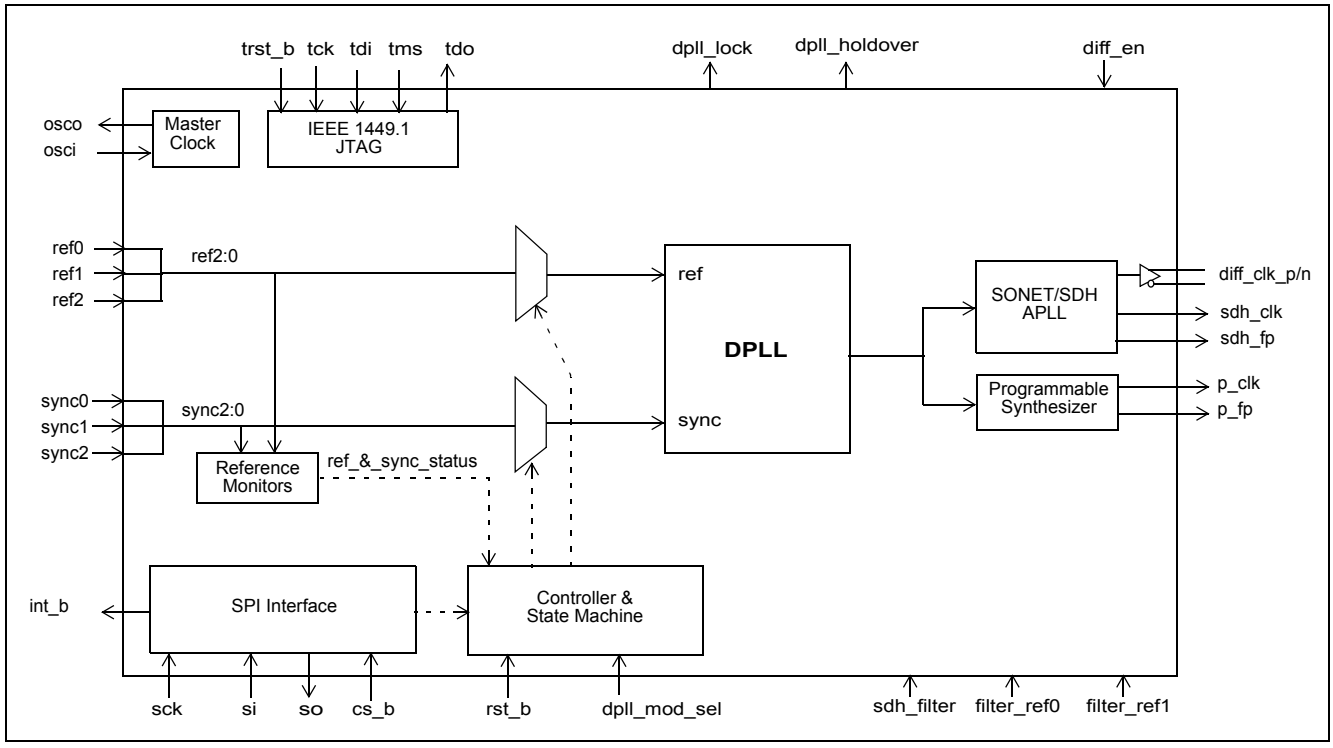

Figure 1 - Block Diagram

Applications

- AMCs for AdvancedTCA™ and MicroTCA Systems
- Multi-Service Edge Switches or Routers
- DSLAM Line Cards
- WAN Line Cards
- RNC/Mobile Switching Center Line Cards
- ADM Line Cards

Table of Contents

1.0 Functional Description 10
1.1 DPLL Features 10
1.2 DPLL Mode Of Operation 11
1.3 Ref and Sync Inputs 12
1.4 Ref and Sync Monitoring 13
1.5 Output Clocks and Frame Pulses 15
1.6 Configurable Input-to-Output and Output-to-Output Delays 16
2.0 Software Configuration 17
3.0 References 22

List of Figures

Figure 1 - Block Diagram 1
Figure 2 - Automatic Mode State Machine 11
Figure 3 - Reference and Sync Inputs 12
Figure 4 - Output Frame Pulse Alignment 12
Figure 5 - Behaviour of the Guard Soak Timer during CFM or SCM Failures 14
Figure 6 - Output Configuration 15
Figure 7 - Phase Delay Adjustments 16

List of Tables

Table 1 - DPLL Features 10
Table 2 - Set of Pre-Defined Auto-Detect Clock Frequencies 13
Table 3 - Set of Pre-Defined Auto-Detect Sync Frequencies 13
Table 4 - Output Clock and Frame Pulse Frequencies 15
Table 5 - Register Map 17

Changes Summary

The following table captures the changes from the February 2006 issue.

Page	Item	Change
20-21	Software Register Description	Changed the naming and description of the frame pulse delay offset registers to clearly show that they form a 22-bit register spread out over 3 8-bit registers. The 22-bit register must be considered a multi-byte register during a read or write operation. This affects registers 0x40-0x42, and 0x58-0x5A.

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
B1 A3 B4	ref0 ref1 ref2	I_d	**Input References (LVCMOS, Schmitt Trigger).** These are input references available for synchronizing output clocks. All three input references can be automatically or manually selected using software registers. These pins are internally pulled down to Vss.
A1 A2 A4	sync0 sync1 sync2	I_d	**Frame Pulse Synchronization References (LVCMOS, Schmitt Trigger).** These are the frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled down to $V_{ss.}$
Output Clocks and Frame Pulses			
D8	sdh_clk	O	**SONET/SDH Output Clock (LVCMOS).** This output can be configured to provide any one of the SONET/SDH clock outputs up to 77.76 MHz. The default frequency for this output is 77.76 MHz.
D7	sdh_fp	O	**SONET/SDH Output Frame Pulse (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse synchronized with an associated SONET/SDH family output clock. The default frequency for this frame pulse output is 8 kHz.
G8	p_clk	O	**Programmable Output Clock (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 77.76 MHz in addition to 2 kHz. The default frequency for this output is 2.048 MHz.
G7	p_fp	O	**Programmable Output Frame Pulse (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with p_clk. The default frequency for this frame pulse output is 8 kHz.
A7 B8	diff_clk_p diff_clk_n	O	**Differential Output Clock (LVPECL).** This output can be configured to provide any one of the available SDH clock frequencies. The default frequency for this clock output is 622.08 MHz.
Control			
G5	rst_b	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
B2	dpll_mod_sel	I_u	**DPLL Mode Select (LVCMOS, Schmitt Trigger).** During reset, the level on this pin determines the default mode of operation of the DPLL (Normal or Freerun). After reset, the mode of operation can be controlled directly with these pins, or by accessing the *dpll_modesel* register through the serial interface. This pin is internally pulled up to Vdd.
B3	diff_en	I_u	**Differential Output Enable (LVCMOS, Schmitt Trigger).** When set high, the differential LVPECL driver is enabled. When set low, the differential driver is tristated reducing power consumption. This function is also controllable through software registers. This pin is internally pulled up to Vdd.

Pin #	Name	I/O Type	Description
Status			
E1	dpll_lock	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for the DPLL. This output goes high when the DPLL's output is frequency and phase locked to the input reference.
H1	dpll_holdover	O	**Holdover Indicator (LVCMOS).** This pin goes high when the DPLL enters the holdover mode.
Serial Interface			
C1	sck	I	**Clock for Serial Interface (LVCMOS).** Serial interface clock.
D2	si	I	**Serial Interface Input (LVCMOS).** Serial interface data input pin.
D1	so	O	**Serial Interface Output (LVCMOS).** Serial interface data output pin.
C2	cs_b	I_u	**Chip Select for Serial Interface (LVCMOS).** Serial interface chip select. This pin is internally pulled up to Vdd.
E2	int_b	O	**Interrupt Pin (LVCMOS).** Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled up to VDD.
APLL Loop Filter			
A5	sdh_filter	A	**External Analog PLL Loop Filter terminal.**
B5	filter_ref0	A	**Analog PLL External Loop Filter Reference.**
C5	filter_ref1	A	**Analog PLL External Loop Filter Reference.**
JTAG and Test			
G4	tdo	O	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G2	tdi	I_u	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.
G3	trst_b	I_u	**Test Reset (LVCMOS).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
H3	tck	I	**Test Clock (LVCMOS):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
F2	tms	I_u	**Test Mode Select (LVCMOS).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
H4	osci	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (XO, XTAL). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.

Pin #	Name	I/O Type	Description
H5	osco	O	**Oscillator Master Clock Output (LVCMOS).** This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
F5	IC		**Internal Connection.** Leave unconnected.
H6 H2	IC		**Internal Connection.** Connect to ground.
H7	NC		**No Connection.** Leave unconnected.
Power and Ground			
C3 C8 E8 F6 F8 G6 H8	V_{DD}	P P P P P P P	**Positive Supply Voltage.** +3.3V_{DC} nominal.
E6 F3	V_{CORE}	P P	**Positive Supply Voltage.** +1.8V_{DC} nominal.
B7 C4	AV_{DD}	P P	**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
B6 C7 F1	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
D3 D4 D5 D6 E3 E4 E5 E7 F4 F7	V_{SS}	G G G G G G G G G G	**Ground.** 0 Volts.
A6 A8 C6 G1	AV_{SS}	G G G G	**Analog Ground.** 0 Volts.

I - Input
I_d - Input, Internally pulled down
I_u - Input, Internally pulled up
O - Output
A - Analog
P - Power
G - Ground

1.0 Functional Description

The ZL30117 SONET/SDH Line Card Synchronizer is a highly integrated device that provides timing and synchronization for network interface cards. The DPLL is capable of locking to one of three input references and provides a wide variety of synchronized output clocks and frame pulses.

1.1 DPLL Features

The Digital Phase-Locked Loop synchronizes to one of the qualified references and provides automatic or manual hitless reference switching and a holdover function when no qualified references are available. It provides a highly configurable set of features which are configurable through the serial interface. A summary of these features are shown in Table 1.

Feature	DPLL
Modes of Operation	Free-run, Normal (locked), Holdover
Loop Bandwidth	User selectable: 14 Hz, 28 Hz, or wideband[1] (890 Hz / 56 Hz / 14 Hz)
Phase Slope Limiting	User selectable: 885 ns/s, 7.5 μs/s, 61 μs/s, or unlimited
Pull-in Range	Fixed: 130 ppm
Reference Inputs	Ref0, Ref1, Ref2
Sync Inputs	Sync0, Sync1, Sync2
Input Reference Frequencies	2 kHz, N * 8 kHz up to 77.76 MHz
Supported Sync Input Frequencies	166.67 Hz, 400 Hz, 1 kHz, 2 kHz, 8 kHz, 64 kHz.
Input Reference Selection/Switching	Automatic (based on programmable priority and revertiveness), or manual selection
Hitless Reference Switching	Can be enabled or disabled
Output Clocks	diff_p/n, sdh_clk, p_clk
Output Frame Pulses	sdh_fp, p_fp synchronized to active sync reference.
Supported Output Clock Frequencies	As listed in Table 4
Supported Output Frame Pulse Frequencies	As listed in Table 4
External Pins Status Indicators	Lock, Holdover

Table 1 - DPLL Features

1. In the wideband mode, the loop bandwidth depends on the frequency of the reference input. For reference frequencies equal to or greater than 64 kHz, the loop bandwidth = 890 Hz. For reference frequencies equal to or greater than 8 kHz and less than 64 kHz, the loop bandwidth = 56 Hz. For reference frequencies equal to 2 kHz, the loop bandwidth is equal to 14 Hz.

1.2 DPLL Mode Of Operation

The DPLL supports three modes of operation - free-run, normal, and holdover. The mode of operation can be manually set or controlled by an automatic state machine as shown in Figure 2.

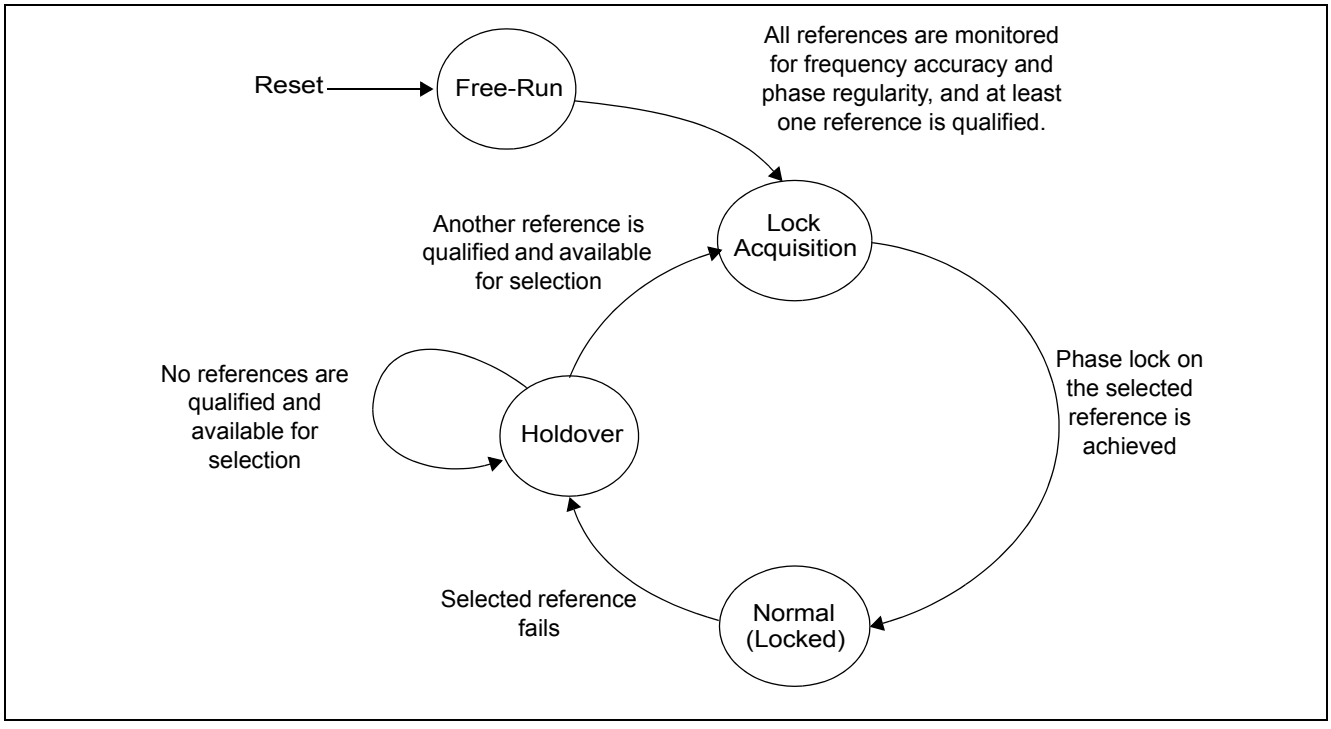

Figure 2 - Automatic Mode State Machine

Free-run

The free-run mode occurs immediately after a reset cycle or when the DPLL has never been synchronized to a reference input. In this mode, the frequency accuracy of the output clocks is equal to the frequency accuracy of the external master oscillator.

Lock Acquisition

The input references are continuously monitored for frequency accuracy and phase regularity. If at least one of the input references is qualified by the reference monitors, then the DPLL will begin lock acquisition on that input. Given a stable reference input, the ZL30117 will enter in the Normal (locked) mode.

Normal (locked)

The usual mode of operation for the DPLL is the normal mode where the DPLL phase locks to a selected qualified reference input and generates output clocks and frame pulses with a frequency accuracy equal to the frequency accuracy of the reference input. While in the normal mode, the DPLL's clock and frame pulse outputs comply with the MTIE and TDEV wander generation specifications as described in Telcordia and ITU-T telecommunication standards.

Holdover

When the DPLL operating in the normal mode loses its reference input, and no other qualified references are available, it will enter the holdover mode and continue to generate output clocks based on historical frequency data collected while the DPLL was synchronized. The transition between normal and holdover modes is controlled by the DPLL so that its initial frequency offset is better than 100 ppb. The frequency drift after this transition period is dependant on the frequency drift of the external master oscillator.

1.3 Ref and Sync Inputs

There are three reference clock inputs (**ref0** to **ref2**) available to the DPLL. Reference selection can be controlled using a built-in state machine or set in a manual mode.The selected reference input is used to synchronize the output clocks.

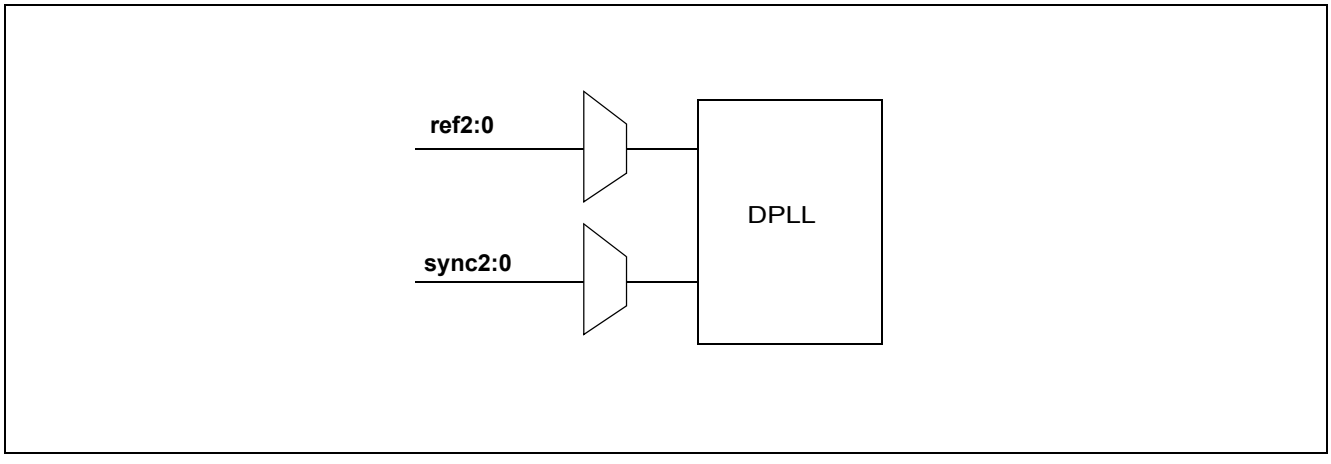

Figure 3 - Reference and Sync Inputs

In addition to the reference inputs, the DPLL has three optional frame pulse synchronization inputs (**sync0** to **sync2**) used to align the output frame pulses. The $sync_n$ input is selected with its corresponding ref_n input, where n = 0, 1, or 2. Note that the sync input cannot be used to synchronize the DPLL, it only determines the alignment of the frame pulse outputs. An example of output frame pulse alignment is shown in Figure 4.

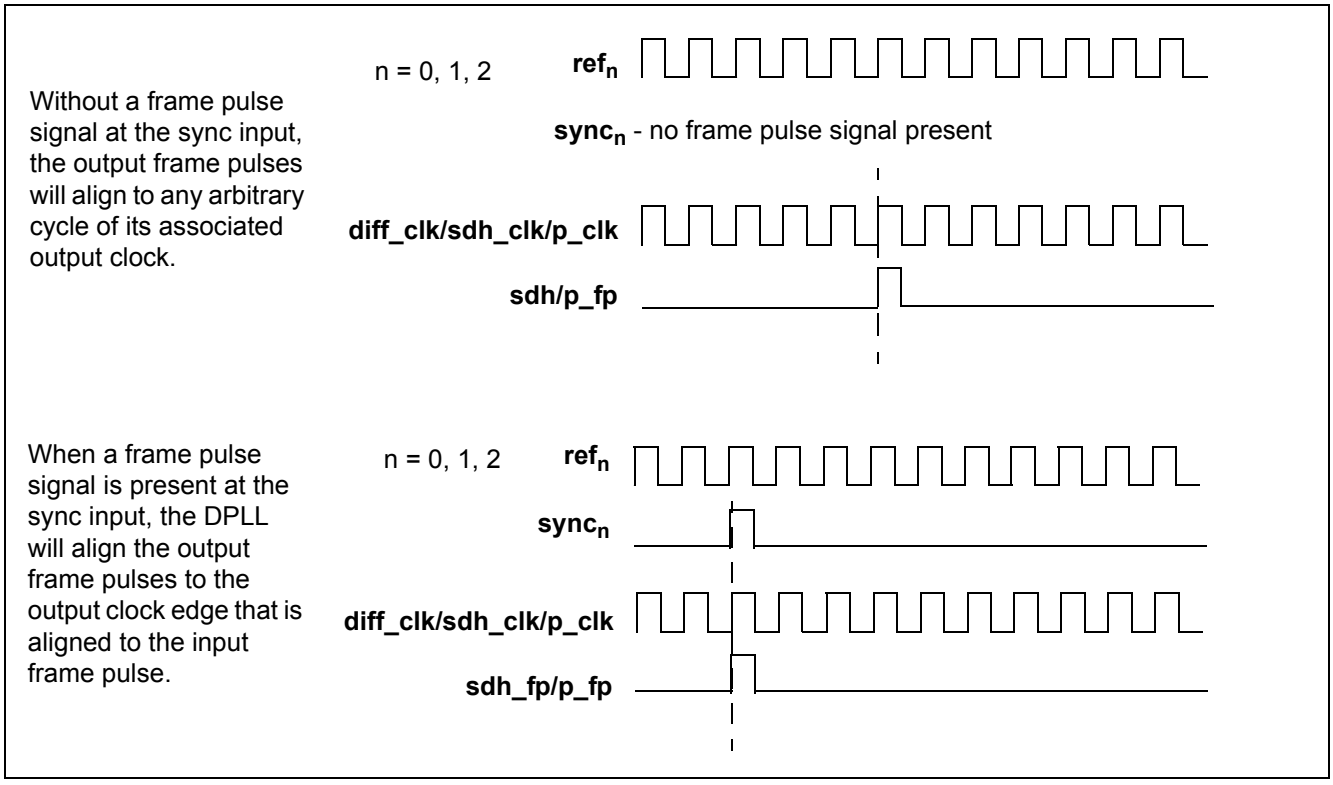

Figure 4 - Output Frame Pulse Alignment

Each of the **ref** inputs accept a single-ended LVCMOS clock with a frequency ranging from 2 kHz to 77.76 MHz. Built-in frequency detection circuitry automatically determines the frequency of the reference if its frequency is within the set of pre-defined frequencies as shown in Table 2. Custom frequencies definable in multiples of 8 kHz are also available.

2 kHz
8 kHz
64 kHz
1.544 MHz
2.048 MHz
6.48 MHz
8.192 MHz
16.384 MHz
19.44 MHz
38.88 MHz
77.76 MHz

Table 2 - Set of Pre-Defined Auto-Detect Clock Frequencies

Each of the **sync** inputs accept a single-ended LVCMOS frame pulse. Since alignment is determined from the rising edge of the frame pulse, there is no duty cycle restriction on this input, but there is a minimum pulse width requirement of 5 ns. Frequency detection for the sync inputs is automatic for the supported frame pulse frequencies shown in Table 3.

166.67 Hz (48x 125 μs frames)
400 Hz
1 kHz
2 kHz
8 kHz
64 kHz

Table 3 - Set of Pre-Defined Auto-Detect Sync Frequencies

1.4 Ref and Sync Monitoring

All input references (**ref0** to **ref2**) are monitored for frequency accuracy and phase regularity. New references are qualified before they can be selected as a synchronization source, and qualified references are continuously monitored to ensure that they are suitable for synchronization. The process of qualifying a reference depends on four levels of monitoring.

Single Cycle Monitor (SCM)

The SCM block measures the period of each reference clock cycle to detect phase irregularities or a missing clock edge. In general, if the measured period deviates by more than 50% from the nominal period, then an SCM failure (scm_fail) is declared.

Coarse Frequency Monitor (CFM)

The CFM block monitors the reference frequency over a measurement period of 30 μs so that it can quickly detect large changes in frequency. A CFM failure (cfm_fail) is triggered when the frequency has changed by more than 3% or approximately 30000 ppm.

Precise Frequency Monitor (PFM)

The PFM block measures the frequency accuracy of the reference over a 10 second interval. To ensure an accurate frequency measurement, the PFM measurement interval is re-initiated if phase or frequency irregularities are detected by the SCM or CFM. The PFM provides a level of hysteresis between the acceptance range and the rejection range to prevent a failure indication from toggling between valid and invalid for references that are on the edge of the acceptance range.

When determining the frequency accuracy of the reference input, the PFM uses the external oscillator's output frequency (f_{ocsi}) as its point of reference.

Guard Soak Timer (GST)

The GST block mimics the operation of an analog integrator by accumulating failure events from the CFM and the SCM blocks and applying a selectable rate of decay when no failures are detected.

As shown in Figure 5, a GST failure (gst_fail) is triggered when the accumulated failures have reached the upper threshold during the disqualification observation window. When there are no CFM or SCM failures, the accumulator decrements until it reaches its lower threshold during the qualification window.

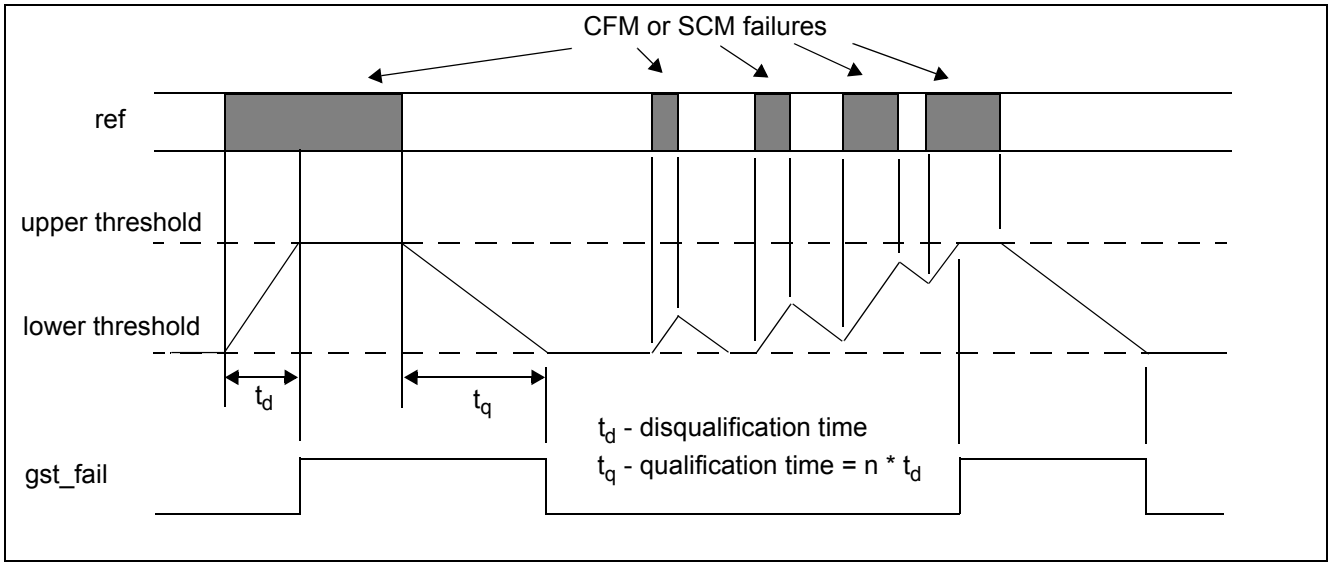

Figure 5 - Behaviour of the Guard Soak Timer during CFM or SCM Failures

Sync Ratio Monitor

All sync inputs (**sync0 to sync2**) are continuously monitored to ensure that there is a correct number of reference clock cycles within the frame pulse period.

1.5 Output Clocks and Frame Pulses

The ZL30117 offers a wide variety of outputs including one low-jitter differential LVPECL clock (**diff_clk_p/n**), one SONET/SDH LVCMOS (**sdh_clk**) output clock and one programmable LVCMOS (**p_clk**) output clock. In addition to the clock outputs, one LVCMOS SONET/SDH frame pulse output (**sdh_fp**) and one LVCMOS programmable frame pulse (**p_fp**) is also available.

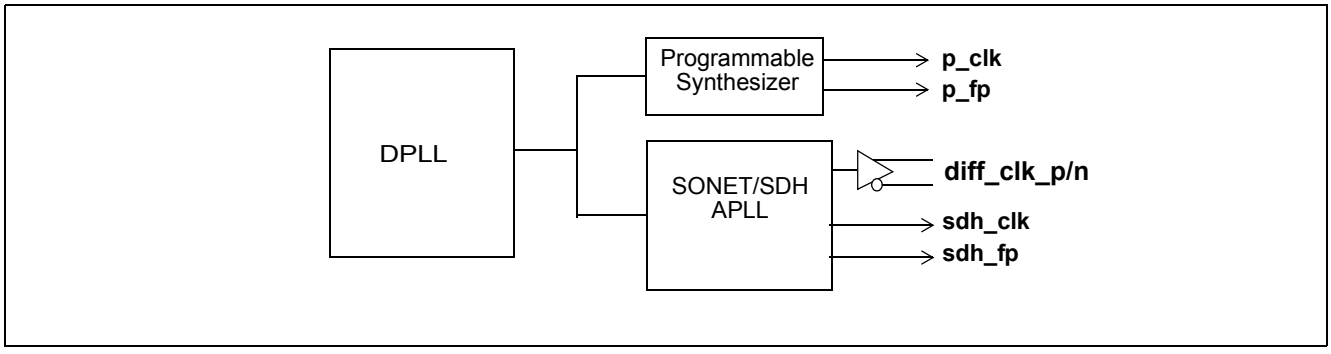

Figure 6 - Output Configuration

The supported frequencies for the output clocks and frame pulses are shown in Table 4.

diff_clk_p/n (LVPECL)	sdh_clk (LVCMOS)	p_clk (LVCMOS)	sdh_fp, p_fp (LVCMOS)
6.48 MHz	6.48 MHz	2 kHz	166.67 Hz (48x 125 μs frames)
19.44 MHz	9.72 MHz	N * 8 kHz (up to 77.76 MHz)	400 Hz
38.88 MHz	12.96 MHz		1 kHz
51.84 MHz	19.44 MHz		2 kHz
77.76 MHz	25.92 MHz		4 kHz
155.52 MHz	38.88 MHz		8 kHz
311.04 MHz	51.84 MHz		32 kHz
622.08 MHz	77.76 MHz		64 kHz

Table 4 - Output Clock and Frame Pulse Frequencies

1.6 Configurable Input-to-Output and Output-to-Output Delays

The ZL30117 allows programmable static delay compensation for controlling input-to-output and output-to-output delays of its clocks and frame pulses.

Both the SONET/SDH APLL and the Programmable Synthesizer can be configured to lead or lag the selected input reference clock using the **DPLL Fine Delay**. The delay is programmed in steps of 119.2 ps with a range of -128 to +127 steps giving a total delay adjustment in the range of -15.26 ns to +15.14 ns. Negative values delay the output clock, positive values advance the output clock.

In addition to the delay introduced by the DPLL Fine Delay, the SONET/SDH APLL and programmable synthesizer have the ability to add their own fine delay adjustments using the **P Fine Delay** and **SDH Fine Delay**. These delays are also programmable in steps of 119.2 ps with a range of -128 to +127 steps.

In addition to these delays, the single-ended output clocks of the SONET/SDH and Programmable synthesizers can be independently offset by 90, 180 and 270 degrees using the **Coarse Delay**, and the SONET/SDH differential outputs can be independently delayed by -1.6 ns, 0 ns, +1.6 ns or +3.2 ns using the **Diff Delay**. The output frame pulses (sdh_clk, p_fp) can be independently offset with respect to each other using the **FP Delay**.

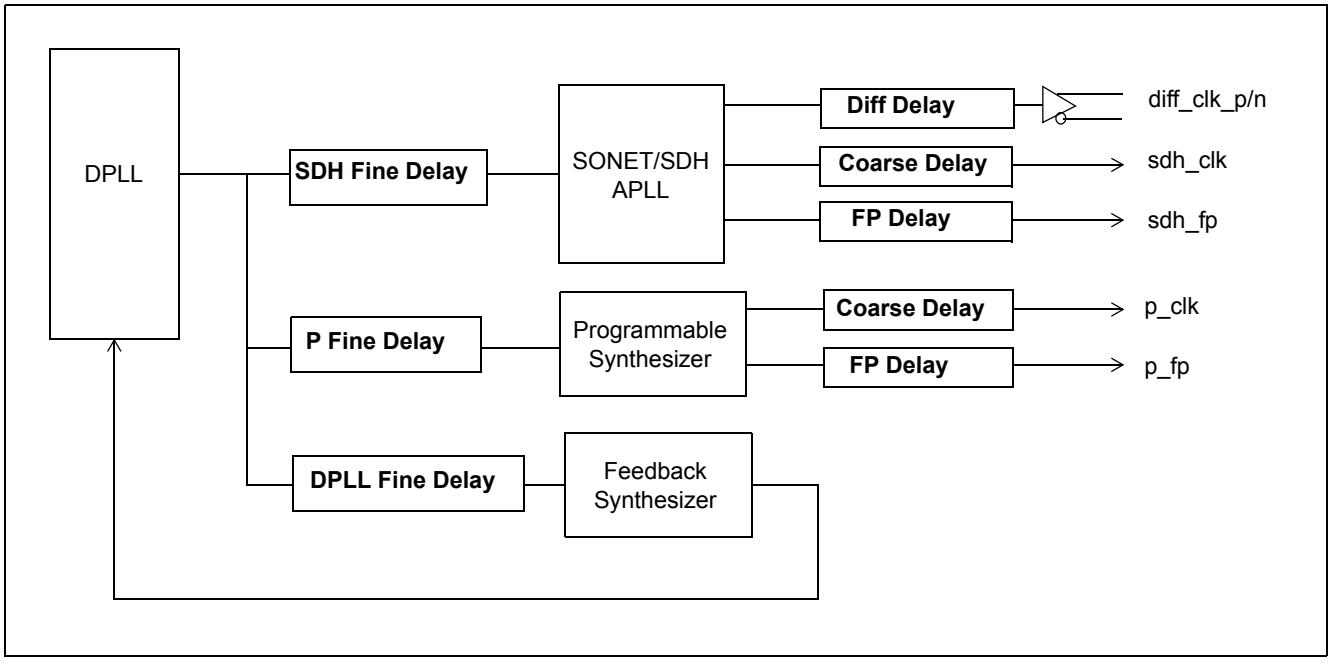

Figure 7 - Phase Delay Adjustments

2.0 Software Configuration

The ZL30117 is mainly controlled by accessing software registers through the serial peripheral interface (SPI). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

The following table provides a summary of the registers available for status updates and configuration of the device.

Addr (Hex)	Register Name	Reset Value (Hex)	Description	Type
	Miscellaneous Registers			
00	id_reg	A1	Chip and version identification and reset ready indication register	R
01	use_hw_ctrl	00	Allows some functions of the device to be controlled by hardware pins	R/W
	Interrupts			
02	ref_fail_isr	FF	Reference failure interrupt service register	R
03	dpll_isr	70	DPLL interrupt service register	StickR
04	Reserved		Leave as default	
05	ref_mon_fail_0	FF	Ref0 and ref1 failure indications	StickR
06	ref_mon_fail_1	FF	Ref2 failure indication.	StickR
07	Reserved		Leave as default	
08	Reserved		Leave as default	
09	ref_fail_isr_mask	00	Reference failure interrupt service register mask	R/W
0A	dpll_isr_mask	00	DPLL interrupt service register mask	R/W
0B	Reserved		Leave as default	
0C	ref_mon_fail_mask_0	FF	Control register to mask each failure indicator for ref0 and ref1	R/W
0D	ref_mon_fail_mask_1	FF	Control register to mask failure indicator for ref2	R/W
0E	Reserved		Leave as default	
0F	Reserved		Leave as default	
	Reference Monitor Setup			
10	detected_ref_0	FF	Ref0 and ref1 auto-detected frequency value status register	R
11	detected_ref_1	FF	Ref2 auto-detected frequency value status register	R
12	Reserved		Leave as default	R
13	Reserved		Leave as default	R

Table 5 - Register Map

Addr (Hex)	Register Name	Reset Value (Hex)	Description	Type
14	detected_sync_0	EE	Sync0 and sync1 auto-detected frequency value and sync failure status register	R
15	detected_sync_1	0E	Sync2 auto-detected frequency value and sync valid status register	R
16	oor_ctrl_0	33	Control register for the ref0 and ref1 out of range limit	R/W
17	oor_ctrl_1	33	Control register for the ref2 out of range limit	R/W
18	Reserved		Leave as default	
19	Reserved		Leave as default	
1A	gst_mask	FF	Control register to mask the inputs to the guard soak timer for ref0 - ref2	R/W
1B	Reserved		Leave as default	
1C	gst_qualif_time	1A	Control register for the guard_soak_timer qualification time and disqualification time for the references	R/W
	DPLL Control			
1D	dpll_ctrl_0	See Register Description	Control register for the DPLL filter control; phase slope limit, bandwidth and hitless switching	R/W
1E	dpll_ctrl_1	See Register Description	Holdover update time, filter_out_en, freq_offset_en, revert enable	R/W
1F	dpll_modesel	See Register Description	Control register for the DPLL mode of operation	R/W
20	dpll_refsel	00	DPLL reference selection or reference selection status	R/W
21	dpll_ref_fail_mask	3C	Control register to mask each failure indicator (SCM, CFM, PFM and GST) used for automatic reference switching and automatic holdover	R/W
22	dpll_wait_to_restore	00	Control register to indicate the time to restore a previous failed reference	R/W
23	dpll_ref_rev_ctrl	00	Control register for the ref0 to ref2 enable revertive signals	R/W
24	dpll_ref_pri_ctrl_0	10	Control register for the ref0 and ref1 priority values	R/W
25	dpll_ref_pri_ctrl_1	32	Control register for the ref2 priority values	R/W
26	Reserved		Leave as default	
27	Reserved		Leave as default	

Table 5 - Register Map (continued)

Addr (Hex)	Register Name	Reset Value (Hex)	Description	Type
28	dpll_lock_holdover_status	04	DPLL lock and holdover status register	R
29	Reserved	03	Leave as default	R/W
2A - 35	Reserved		Leave as default	
	Programmable Synthesizer Configuration Registers			
36	p_enable	8F	Control register to enable the p_clk and p_fp outputs of the programmable synthesizer	R/W
37	p_run	0F	Control register to generate p_clk, p_fp	R/W
38	p_freq_0	00	Control register for the [7:0] bits of the N of N*8k clk	R/W
39	p_freq_1	01	Control register for the [13:8] bits of the N of N*8k clk	R/W
3A	p_clk_offset90	00	Control register for the p_clk phase position coarse tuning	R/W
3B	Reserved		Leave as default	
3C	Reserved		Leave as default	
3D	p_offset_fine	00	Control register for the output/output phase alignment fine tuning for the programmable synthesizer	R/W
3E	p_fp_freq	05	Control register to select the p_fp frame pulse frequency	R/W
3F	p_fp_type	83	Control register to select p_fp type	R/W
40	p_fp_offset_0	00	Bits [7:0] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	R/W
41	p_fp_offset_1	00	Bits [15:8] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	R/W
42	p_fp_offset_2	00	Bits [21:16] of the programmable frame pulse phase offset in multiples of 8 kHz cycles	R/W
43 - 4F	Reserved		Leave as default	
	SDH Configuration Registers			
50	sdh_enable	8F	Control register to enable sdh_clk and sdh_fp	R/W
51	sdh_run	0F	Control register to generate sdh_clk and sdh_fp	R/W
52	sdh_clk_div	42	Control register for the sdh_clk frequency selection	R/W
53	sdh_clk_offset90	00	Control register for the sdh_clk phase position coarse tuning	R/W

Table 5 - Register Map (continued)

Addr (Hex)	Register Name	Reset Value (Hex)	Description	Type
54	Reserved		Leave as default	
55	sdh_offset_fine	00	Control register for the output/output phase alignrment fine tuning for sdh path	R/W
56	sdh_fp_freq	05	Control register to select the sdh_fp frame pulse frequency	R/W
57	sdh_fp_type	23	Control register to select sdh_fp type	R/W
58	sdh_fp_offset_0	00	Bits [7:0] of the programmable frame pulse phase offset in multiples of 1/311.04 MHz	R/W
59	sdh_fp_offset_1	00	Bits [15:8] of the programmable frame pulse phase offset in multiples of 1/311.04 MHz	R/W
5A	sdh_fp_offset_2	00	Bits [21:16] of the programmable frame pulse phase offset in multiples of 8 kHz cycles	R/W
5B - 5F	Reserved		Leave as default	
	Differential Output Configuration			
60	diff_clk_ctrl	A3	Control register to enable diff_clk	R/W
61	diff_clk_sel	53	Control register to select the diff_clk frequency	R/W
	External Feedback Configuration			
62	Reserved		Leave as default	
63	fb_offset_fine	F5	Control register for the output/output phase alignment fine tuning	R/W
64	reserved			
Custom Input Frequencies				
65	ref_freq_mode_0	00	Control register to set whether to use auto detect, CustomA or CustomB for ref0 to ref2	R/W
66	Reserved		Leave as default	
67	custA_mult_0	00	Control register for the [7:0] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
68	custA_mult_1	00	Control register for the [13:8] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
69	custA_scm_low	00	Control register for the custom configuration A: single cycle SCM low limiter	R/W
6A	custA_scm_high	00	Control register for the custom configuration A: single cycle SCM high limiter	R/W
6B	custA_cfm_low_0	00	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM low limit	R/W

Table 5 - Register Map (continued)

Addr (Hex)	Register Name	Reset Value (Hex)	Description	Type
6C	custA_cfm_low_1	00	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM low limit	R/W
6D	custA_cfm_hi_0	00	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM high limit	R/W
6E	custA_cfm_hi_1	00	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM high limiter	R/W
6F	custA_cfm_cycle	00	Control register for the custom configuration A: CFM reference monitoring cycles - 1	R/W
70	custA_div	00	Control register for the custom configuration A: enable the use of ref_div4 for the CFM and PFM inputs	R/W
71	custB_mult_0	00	Control register for the [7:0] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
72	custB_mult_1	00	Control register for the [13:8] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
73	custB_scm_low	00	Control register for the custom configuration B: single cycle SCM low limiter	R/W
74	custB_scm_high	00	Control register for the custom configuration B: single cycle SCM high limiter	R/W
75	custB_cfm_low_0	00	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM low limiter.	R/W
76	custB_cfm_low_1	00	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM low limiter.	R/W
77	custB_cfm_hi_0	00	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM high limiter.	R/W
78	custB_cfm_hi_1	00	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM high limiter.	R/W
79	custB_cfm_cycle	00	Control register for the custom configuration B: CFM reference monitoring cycles - 1	R/W
7A	custB_div	00	Control register for the custom configuration B: enable the use of ref_div4 for the CFM and PFM inputs	R/W

Table 5 - Register Map (continued)

Addr (Hex)	Register Name	Reset Value (Hex)	Description	Type
7B - 7F	Reserved			

Table 5 - Register Map (continued)

3.0 References

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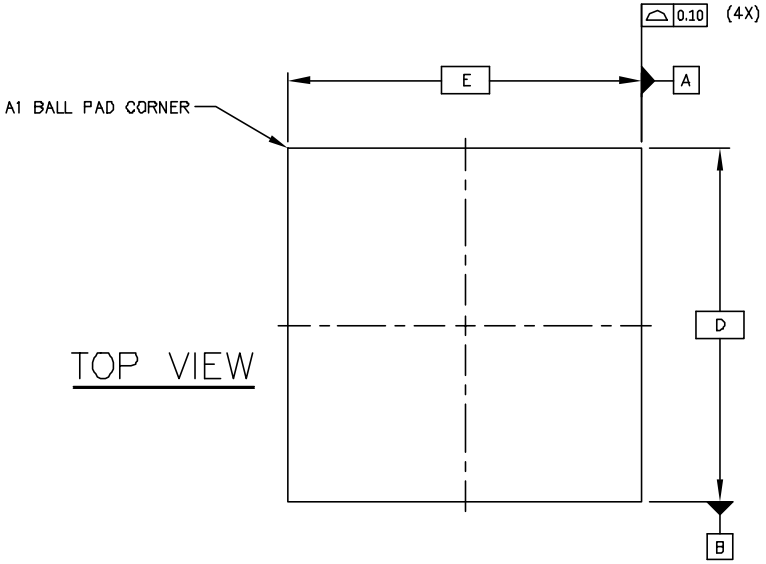
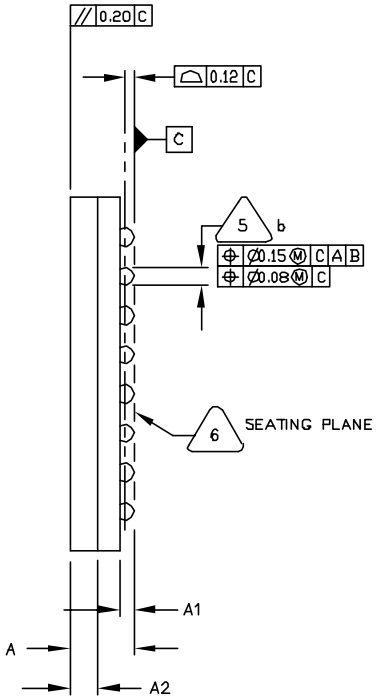
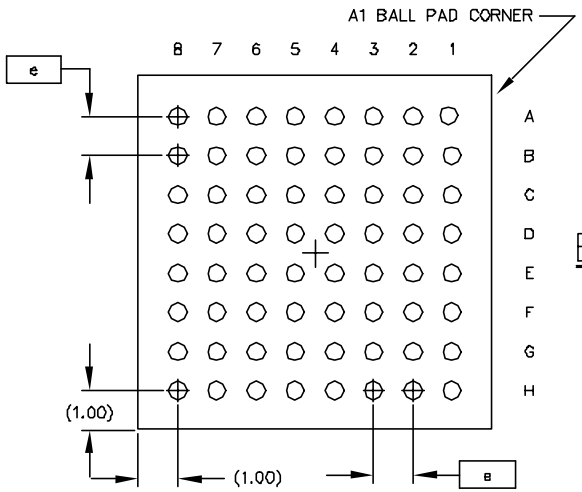


TOP VIEW



SIDE VIEW



BOTTOM VIEW

64 SOLDER BALLS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D		9.00 REF.	
E		9.00 Ref.	
e		1.0 Ref	
n		64	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE

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- Экспресс доставка в любую точку России;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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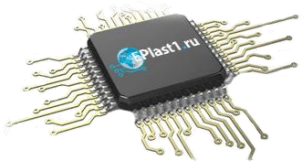
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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