

### Features

- Wide input voltage range from 2.5V to 5.5V
- 200mV low dropout voltage at 150mA output current
- Guaranteed 150mA output current.
- Low quiescent current 50 $\mu$ A
- Output voltage from 1.0V to 3.5V
- $\pm 2\%$  output voltage accuracy
- Low temperature drift at output voltage
- High PSRR
- Fast transient response
- Current limit protection
- Short circuit protection
- Thermal shutdown protection
- SOT25 and SOT353: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

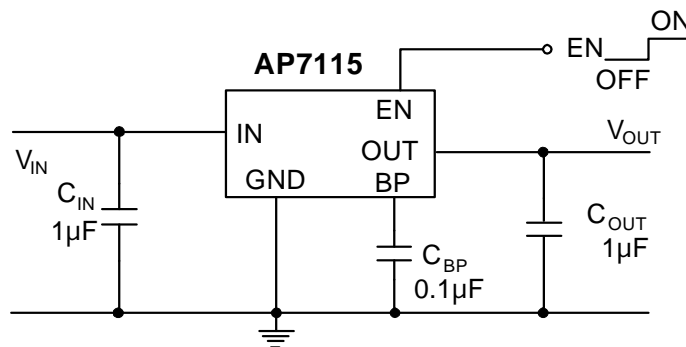
### General Description

The AP7115 is a 150mA, fixed output voltage, low dropout linear regulator. The device includes pass element, error amplifier, band gap reference, current-limit and thermal shutdown circuit. The characteristics of low dropout voltage and low quiescent current make it suitable for use in battery powered devices. The typical quiescent current is approximately 50 $\mu$ A. Several fixed output voltages are available from 1.0V to 3.5V. Additional protection is provided with built-in current-limit and thermal-shutdown functions.

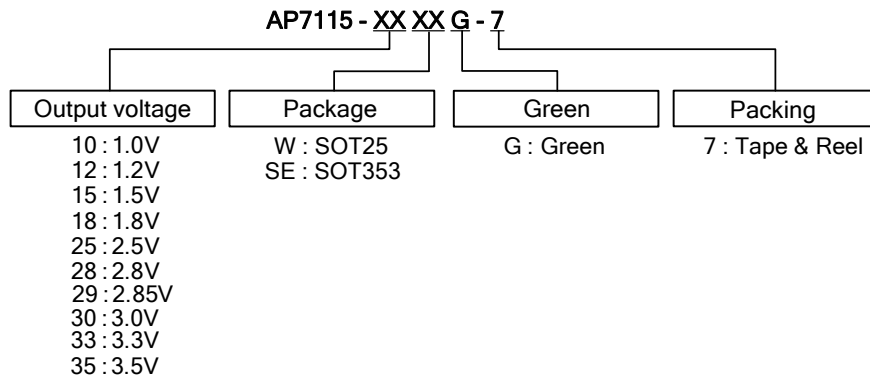
### Applications



- Wireless Communication
- GSM/GPRS Cellular Phones
- Handheld Mobile Devices
- Battery Powered Devices
- CD-ROM, DVD, and LAN Cards
- PC and Notebook Peripherals

### Typical Application Circuit



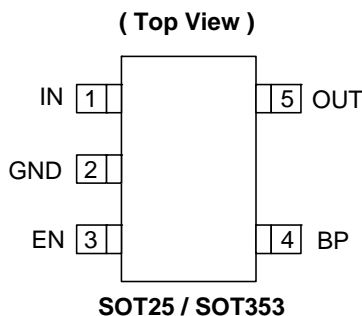
### Ordering Information



Device	Package Code	Packaging (Note 2)	7" Tape and Reel	
			Quantity	Part Number Suffix
 AP7115-XXWG-7	W	SOT25	3000/Tape & Reel	-7
 AP7115-XXSEG-7	SE	SOT353	3000/Tape & Reel	-7

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).  
 2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

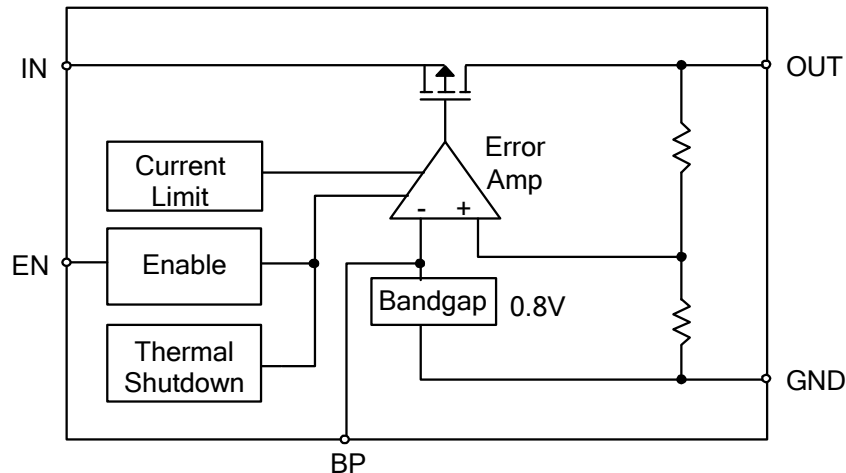
### Pin Assignments



### Pin Descriptions

Pin Name	Pin NO.	Description
IN	1	Voltage Input
GND	2	Ground
EN	3	Chip Enable Control
BP	4	Band-Gap Bypass
OUT	5	Voltage Output

### Block Diagram



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	3.5	KV
ESD MM	Machine Model ESD Protection	400	V
$V_{IN}$	Input Voltage	-0.3~5.5	V
$V_{CE}$	CE Pin Voltage	-0.3~5.5	V
$V_{OUT}$	Output Voltage	-0.3~ $V_{in}+0.3$	V
$V_{BP}$	Band Gap Bypass Pin Voltage	-0.3~5.5	V
$P_D$	Power Dissipation	500	mW
$T_J$	Operating Junction Temperature Range	-40 to +125	°C
$T_{ST}$	Storage Temperature Range	-65 to +150	°C

### Recommended Operating Conditions

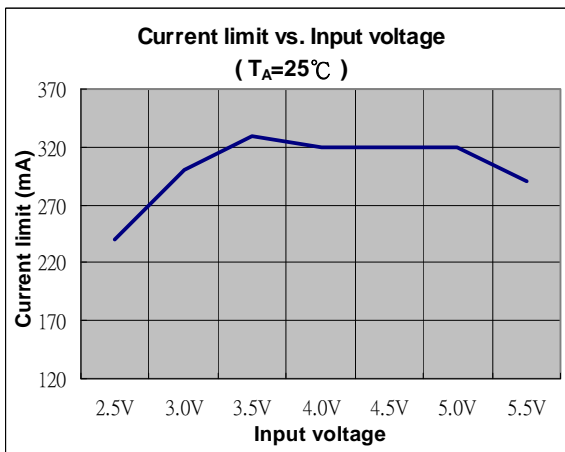
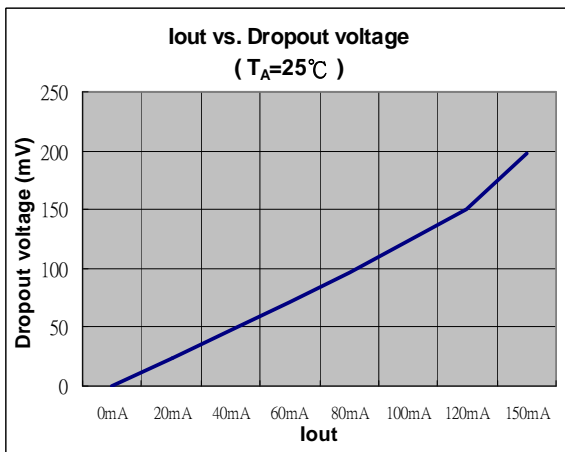
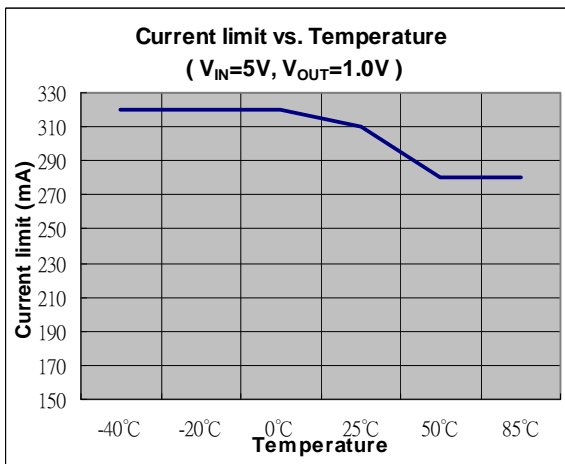
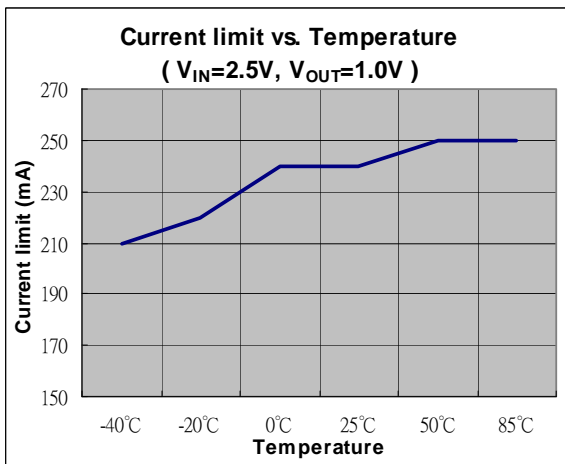
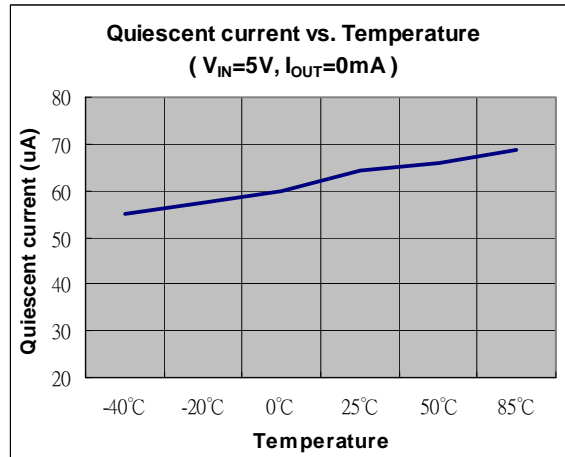
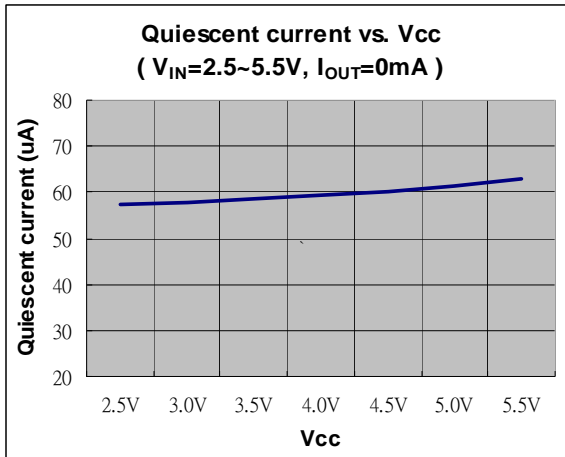
Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Voltage	2.5	5.5	V
$I_{OUT}$	Output Current	-	150	mA
$T_A$	Operating Ambient Temperature	-40	85	°C

### Electrical Characteristics (V<sub>CC</sub> = 3.3V, I<sub>L</sub> = 30mA, C<sub>IN</sub> = 1μF, C<sub>OUT</sub> = 1μF, T<sub>A</sub> = 25°C)

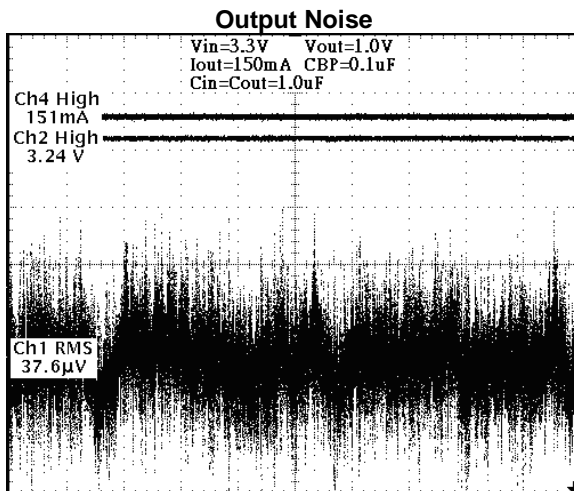
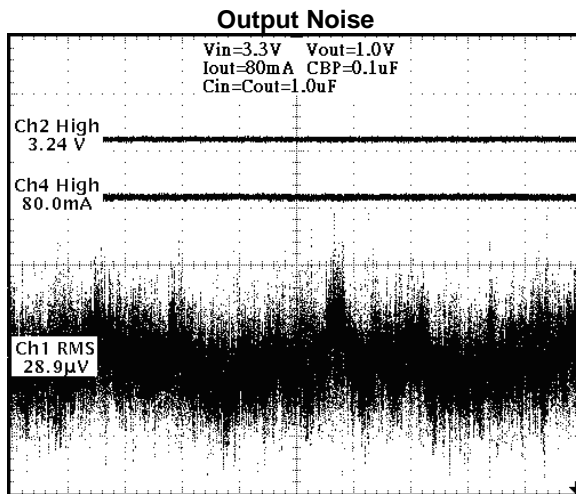
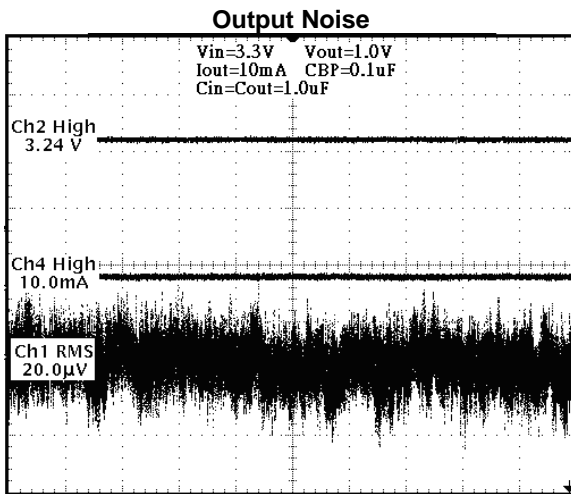
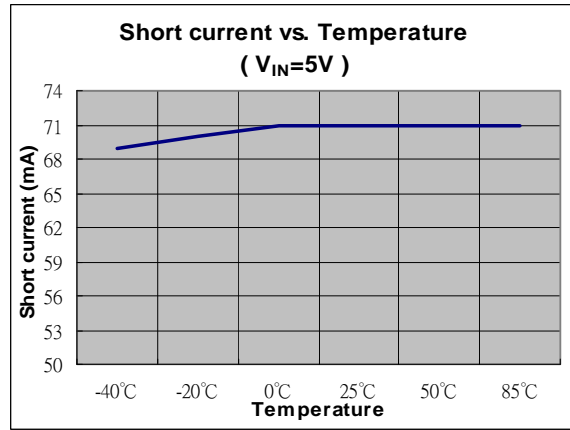
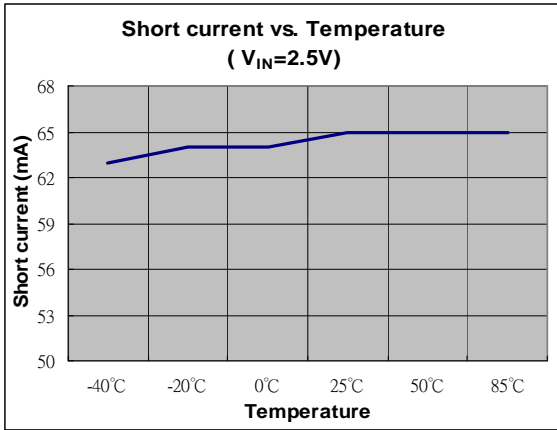
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
<b>System Supply Input</b>						
V <sub>IN</sub>	Operating input voltage	I <sub>L</sub> = 0 ~ 150mA	2.5		5.5	V
ΔV <sub>OUT</sub> /V <sub>OUT</sub>	Output Voltage Accuracy	V <sub>IN</sub> = V <sub>OUT</sub> + 1V where 1mA ≤ I <sub>OUT</sub> ≤ 50mA	-2		2	%
V <sub>DO</sub>	Dropout Voltage	I <sub>L</sub> = 150mA		200	300	mV
I <sub>OUT</sub>	Output Current	V <sub>IN</sub> - V <sub>OUT</sub> = 1V	150			mA
I <sub>Q</sub>	Quiescent Current	V <sub>IN</sub> = V <sub>OUT</sub> + 1V where I <sub>OUT</sub> = 0 and V <sub>CE</sub> = V <sub>IN</sub>		50	80	μA
I <sub>shutdown</sub>	Shutdown Current	V <sub>IN</sub> = V <sub>OUT</sub> + 1V where I <sub>OUT</sub> = 0 and V <sub>CE</sub> = 0		0.1	1	μA
PSRR	Power Supply Rejection Ratio	I <sub>OUT</sub> = 30mA, f = 1kHz		70		dB
I <sub>limit</sub>	Current Limit		200	250		mA
<b>Thermal Management</b>						
T <sub>shutdown</sub>	Thermal Shutdown			150		°C
<b>Reference Voltage</b>						
ΔV <sub>REF</sub> /ΔT	Tempco of Bandgap Reference			30	50	ppm/°C
ΔV <sub>OUT</sub> /ΔT	Tempco of Output Voltage	I <sub>OUT</sub> = 30mA, -40°C ≤ T ≤ 85°C		50	100	ppm/°C
<b>Control and Protection</b>						
V <sub>IH,CE</sub>			2.0			V
V <sub>IL,CE</sub>					0.7	V
I <sub>CE</sub>	CE Pin Leakage Current	V <sub>CE</sub> = V <sub>IN</sub> @ V <sub>IN</sub> = 5.0V and V <sub>SS</sub> = 0V V <sub>CE</sub> = V <sub>SS</sub> @ V <sub>IN</sub> = 5.0V and V <sub>SS</sub> = 0V		0.01	0.1	μA
<b>Regulation</b>						
ΔV <sub>O</sub> /ΔV <sub>IN</sub>	Line Regulation	V <sub>OUT</sub> + 0.5V ≤ V <sub>IN</sub> ≤ 5.5V where V <sub>OUT</sub> > 2.0V, I <sub>OUT</sub> = 30mA		0.02	0.1	%/V
ΔV <sub>LOAD</sub>	Load Regulation	1mA ≤ I <sub>L</sub> ≤ 150mA where V <sub>IN</sub> = V <sub>OUT</sub> + 1V		0.003	0.006	%/mA
<b>Noise</b>						
e <sub>n</sub>	Output Noise	BW = 10Hz ~ 100kHz		50		μV <sub>rms</sub>
<b>Thermal Resistance</b>						
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient	SOT25 (Note 3)	-	200	-	°C/W
		SOT353 (Note 3)		337		°C/W
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case	SOT25 (Note 3)	-	52	-	°C/W
		SOT353 (Note 3)		121		°C/W

Notes: 3. Test condition for SOT25 and SOT353: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

**Typical Operating Characteristics**

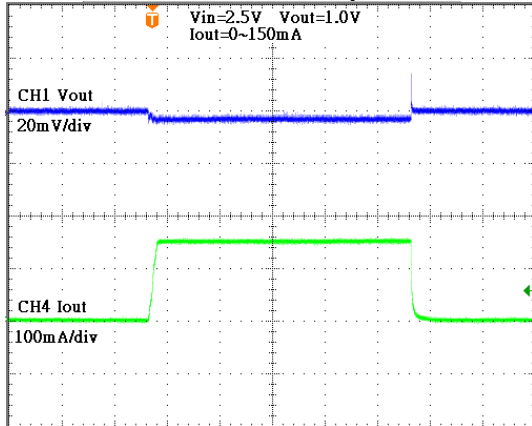


**Typical Operating Characteristics (Continued)**

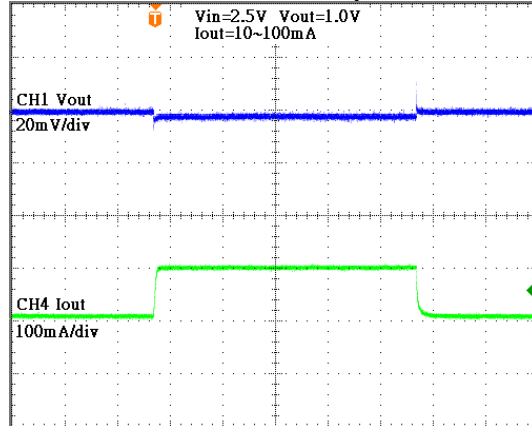


**Typical Operating Characteristics (Continued)**

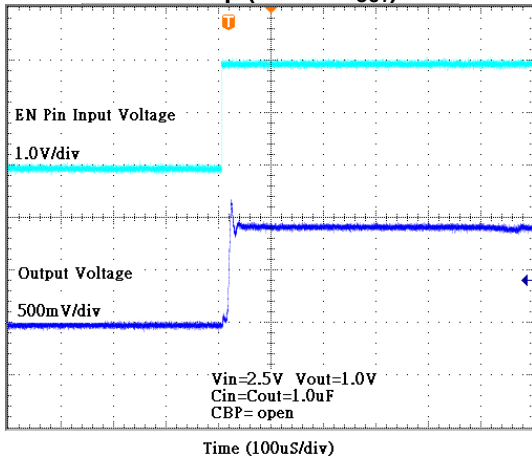
**Load Transient Response**



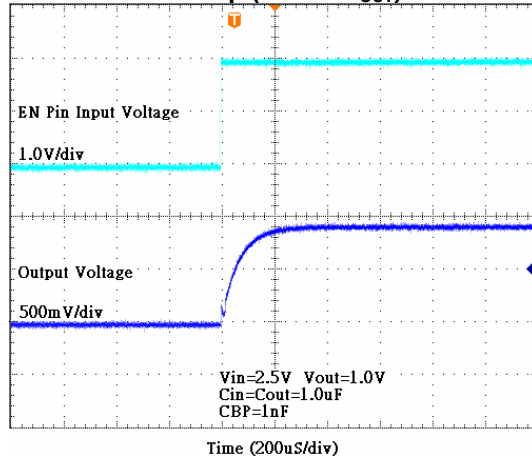
**Load Transient Response**



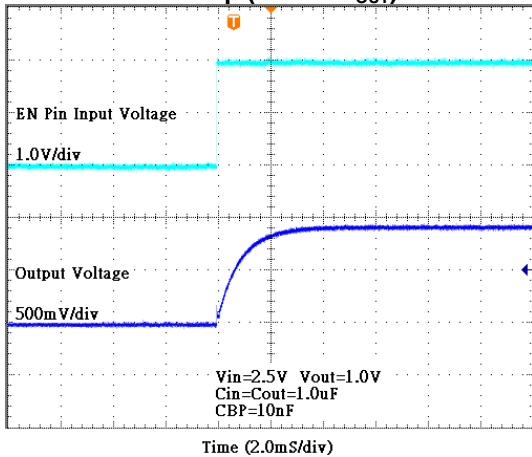
**Start Up (EN vs. V<sub>OUT</sub>)**



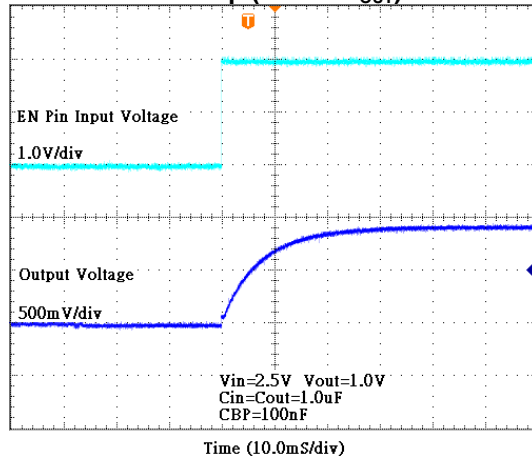
**Start Up (EN vs. V<sub>OUT</sub>)**



**Start Up (EN vs. V<sub>OUT</sub>)**



**Start Up (EN vs. V<sub>OUT</sub>)**



### Application Note

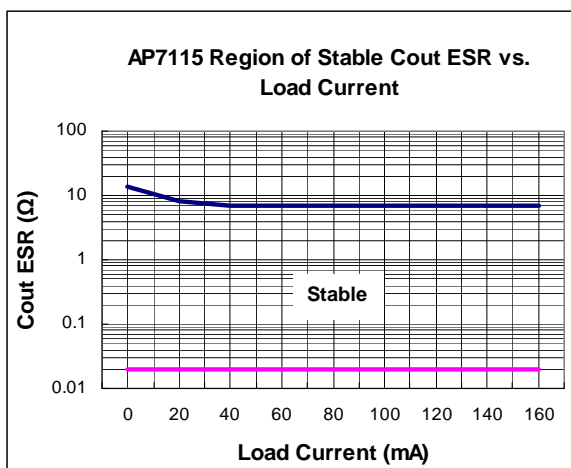
#### ■ Input Capacitor

An 1uF input capacitor is required between the AP7115 input pin and GND.

There are no requirements for the ESR on input capacitor, but tolerance and temperature coefficient must be considered.

#### ■ Output Capacitor

The AP7115 can work with very small ceramic output capacitors (1uF or greater). Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it from a zero to provide phase lead which is required for loop stability. Figure below is Cout ESR vs. Load Current.



#### ■ Band-Gap Bypass Capacitor

0.1uF bypass capacitor Between BP pin and GND can reduce output voltage noise.

#### ■ Shutdown Input Operation

The AP7115 is shutdown by pulling the EN pin low, and turned on by driving the input high. If the shutdown feature is not required, the EN pin should be tied to VIN to keep the regulator on at all times.

#### ■ Dropout Voltage

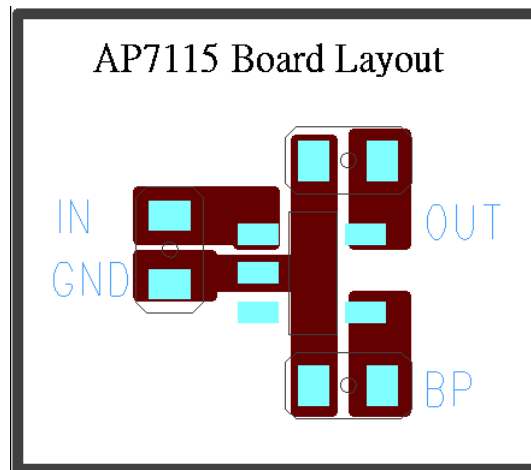
$$V_{\text{DROPOUT}} = V_{\text{IN}} - V_{\text{OUT}} = R_{\text{DS(ON)}} \times I_{\text{OUT}}$$

#### ■ Current Limit

The AP7115 monitors and controls the PMOS' gate voltage, limiting the output current to 250mA(typ.). The output can be shorted to ground for an indefinite period of time without damaging the part.

#### ■ PCB Layout

Optimum performance can only be achieved when the device is mounted on a PC board according to the diagram below:



#### ■ Thermal Considerations

Thermal Shutdown Protection limits power dissipation in AP7115. When the operation junction temperature exceeds 155°C, the Over Temperature Protection circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C. For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} + V_{\text{IN}} \times I_Q$$

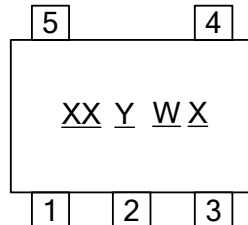
The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by the following formula:

$$P_{D(\text{MAX})} = (T_{J(\text{MAX})} - T_A) / \theta_{JA}$$

Where  $T_{J(\text{MAX})}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

### Marking Information

( Top View )



XX : Identification code

Y : Year 0~9

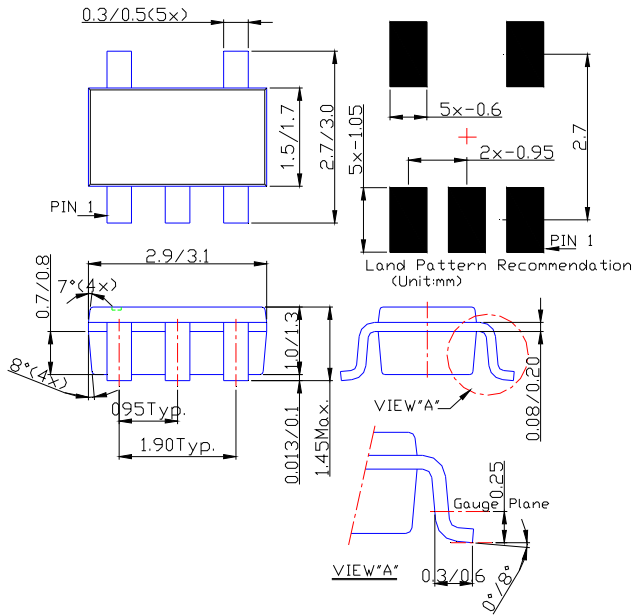
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week

X : A~Z : Green

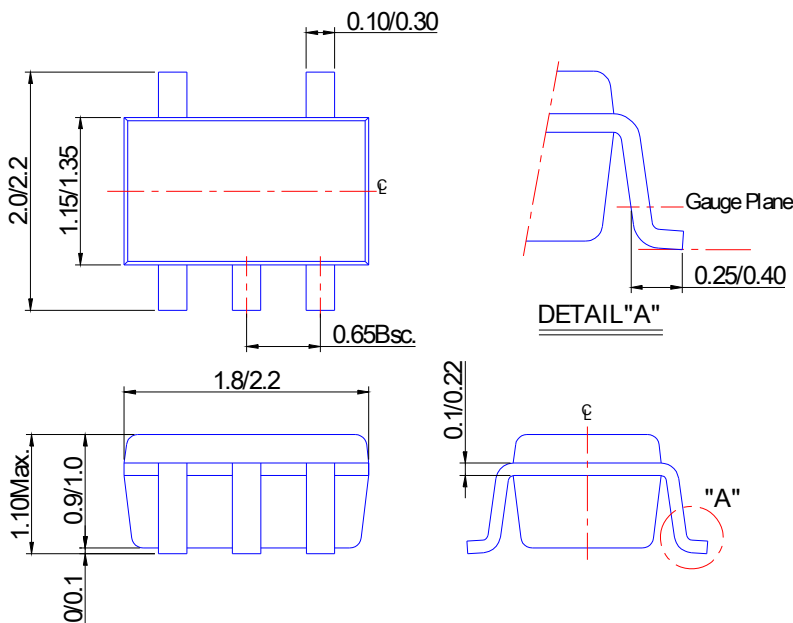
Part Number	Identification Code	Part Number	Identification Code
<b>SOT25</b>		<b>SOT353</b>	
AP7115-10W	FO	AP7115-10SE	GO
AP7115-12W	FP	AP7115-12SE	GP
AP7115-15W	FQ	AP7115-15SE	GQ
AP7115-18W	FR	AP7115-18SE	GR
AP7115-25W	FS	AP7115-25SE	GS
AP7115-28W	FT	AP7115-28SE	GT
AP7115-29W	FU	AP7115-29SE	GU
AP7115-30W	FV	AP7115-30SE	GV
AP7115-33W	FW	AP7115-33SE	GW
AP7115-35W	FX	AP7115-35SE	GX

**Package Information (All Dimensions in mm)**

**(1) Package Type: SOT25**



**(2) Package Type: SOT353**



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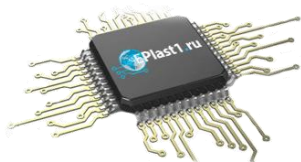
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