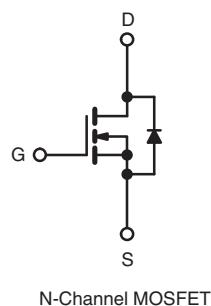
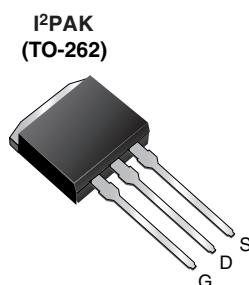


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	600
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.75
Q _g (Max.) (nC)	49
Q _{gs} (nC)	13
Q _{gd} (nC)	20
Configuration	Single



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching
- This Device is only for Through Hole Application

APPLICABLE OFF LINE SMPS TOPOLOGIES

- Active Clamped Forward
- Main Switch

ORDERING INFORMATION

Package	I²PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFSL9N60A-GE3
Lead (Pb)-free	IRFSL9N60APbF
	SiHFSL9N60A-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	37	W/°C
Linear Derating Factor		1.3	
Single Pulse Avalanche Energy ^b	E _{AS}	290	mJ
Repetitive Avalanche Current ^a	I _{AR}	9.2	A
Repetitive Avalanche Energy ^a	E _{AR}	17	mJ
Maximum Power Dissipation	P _D	170	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 6.8 mH, R_g = 25 Ω, I_{AS} = 9.2 A (see fig. 12).
- I_{SD} ≤ 9.2 A, dI/dt ≤ 50 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

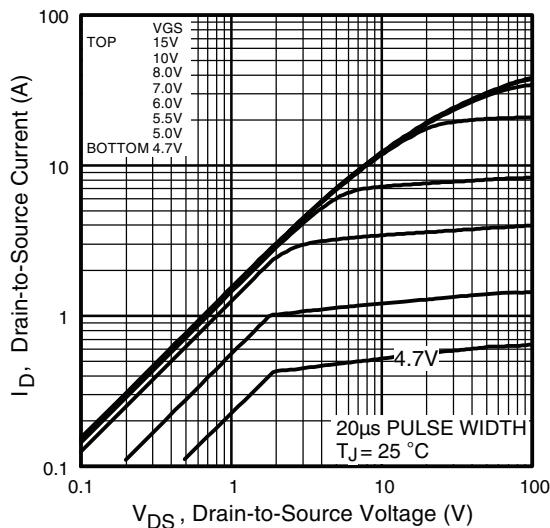
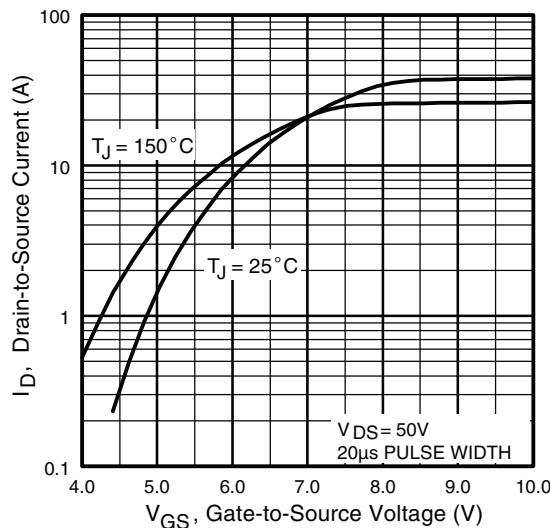
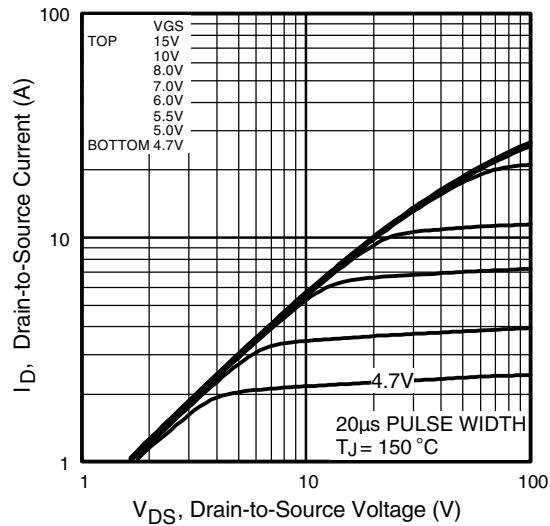
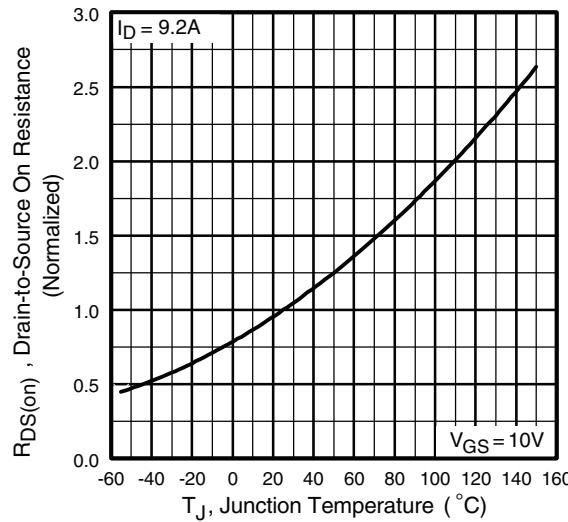
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state)	R_{thJA}	-	40	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.75	

SPECIFICATIONS ($T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$	$I_D = 250 \mu\text{A}$	600	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600 \text{ V}$	$V_{GS} = 0 \text{ V}$	-	-	25	μA	
		$V_{DS} = 480 \text{ V}$	$V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 5.5 \text{ A}^b$	-	-	0.75	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 25 \text{ V}$, $I_D = 3.1 \text{ A}^b$		5.5	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$ $V_{DS} = 25 \text{ V}$ $f = 1.0 \text{ MHz}$, see fig. 5		-	1400	-	pF	
Output Capacitance	C_{oss}			-	180	-		
Reverse Transfer Capacitance	C_{rss}			-	7.1	-		
Output Capacitance	C_{oss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 1.0 \text{ V}$, $f = 1.0 \text{ MHz}$	-	1957	-	nC	
			$V_{DS} = 480 \text{ V}$, $f = 1.0 \text{ MHz}$	-	49	-		
Effective Output Capacitance	$C_{oss eff.}$		$V_{DS} = 0 \text{ V}$ to 480 V^c	-	96	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 9.2 \text{ A}$, $V_{DS} = 400 \text{ V}$ see fig. 6 and 13 ^b	-	-	49	ns	
Gate-Source Charge	Q_{gs}			-	-	13		
Gate-Drain Charge	Q_{gd}			-	-	20		
Turn-On Delay Time	$t_{d(on)}$			-	13	-		
Rise Time	t_r	$V_{DD} = 300 \text{ V}$, $I_D = 9.2 \text{ A}$ $R_g = 9.1 \Omega$, $R_D = 35.5 \Omega$, see fig. 10 ^b		-	25	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	30	-		
Fall Time	t_f			-	22	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.2	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	37		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 9.2 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	1.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = 9.2 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	530	800	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.0	4.4	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.
c. $C_{oss eff}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

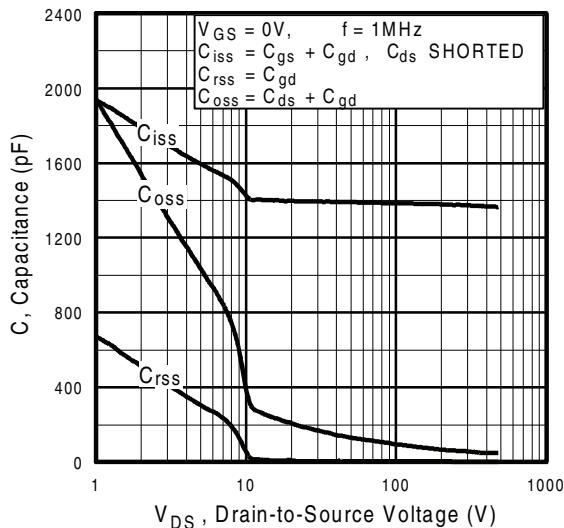


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

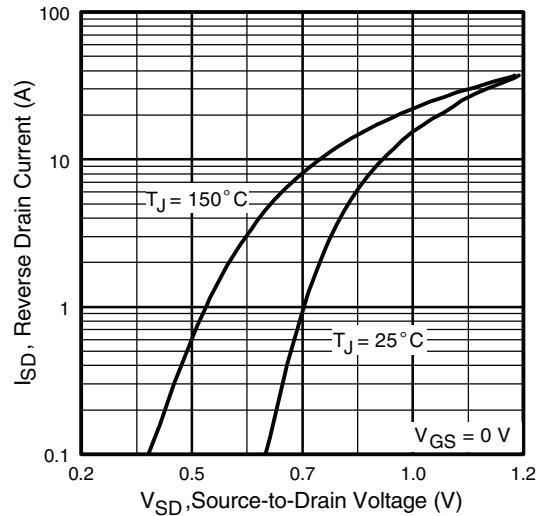


Fig. 7 - Typical Source-Drain Diode Forward Voltage

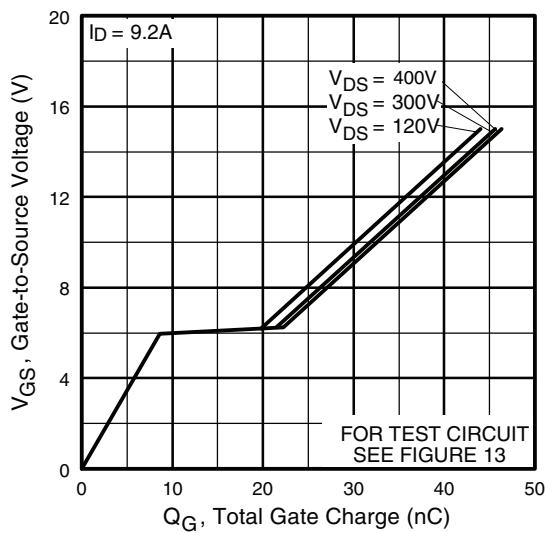


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

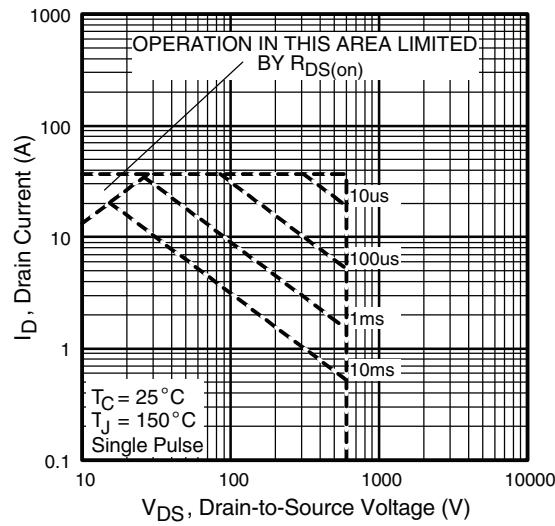


Fig. 8 - Maximum Safe Operating Area

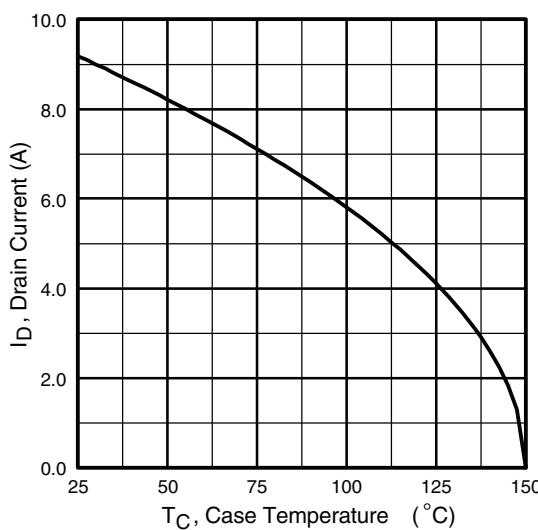


Fig. 9 - Maximum Drain Current vs. Case Temperature

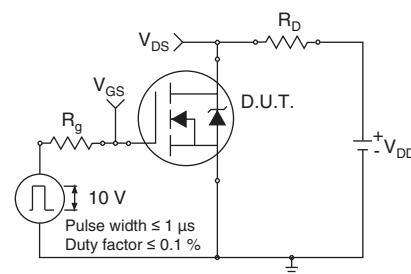


Fig. 10a - Switching Time Test Circuit

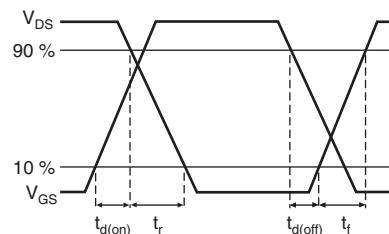


Fig. 10b - Switching Time Waveforms

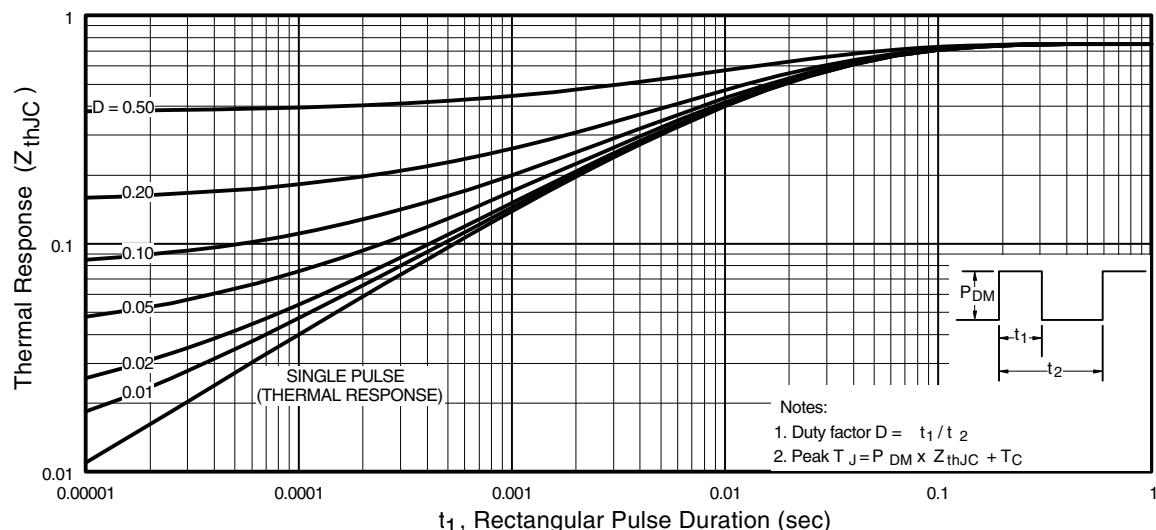


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

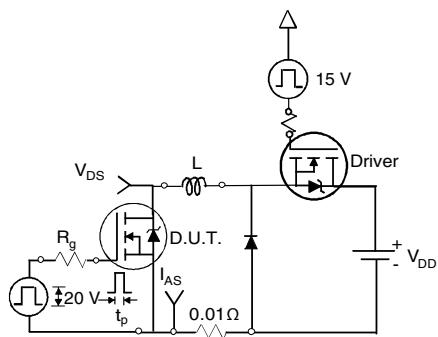


Fig. 12a - Unclamped Inductive Test Circuit

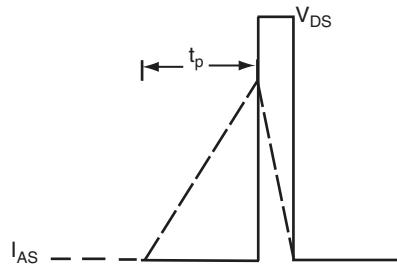


Fig. 12b - Unclamped Inductive Waveforms

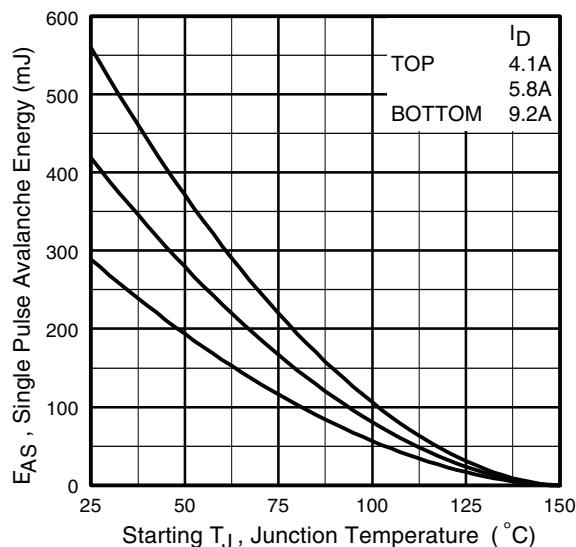


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

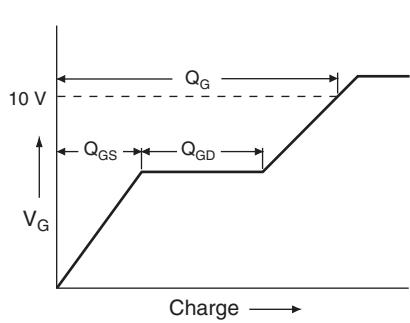


Fig. 13a - Basic Gate Charge Waveform

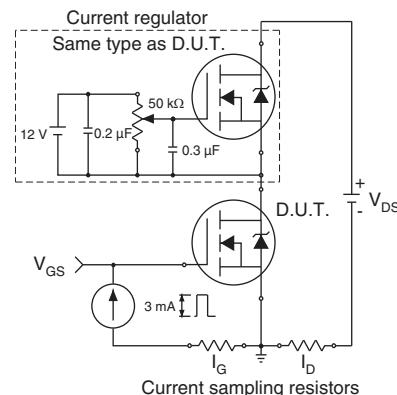
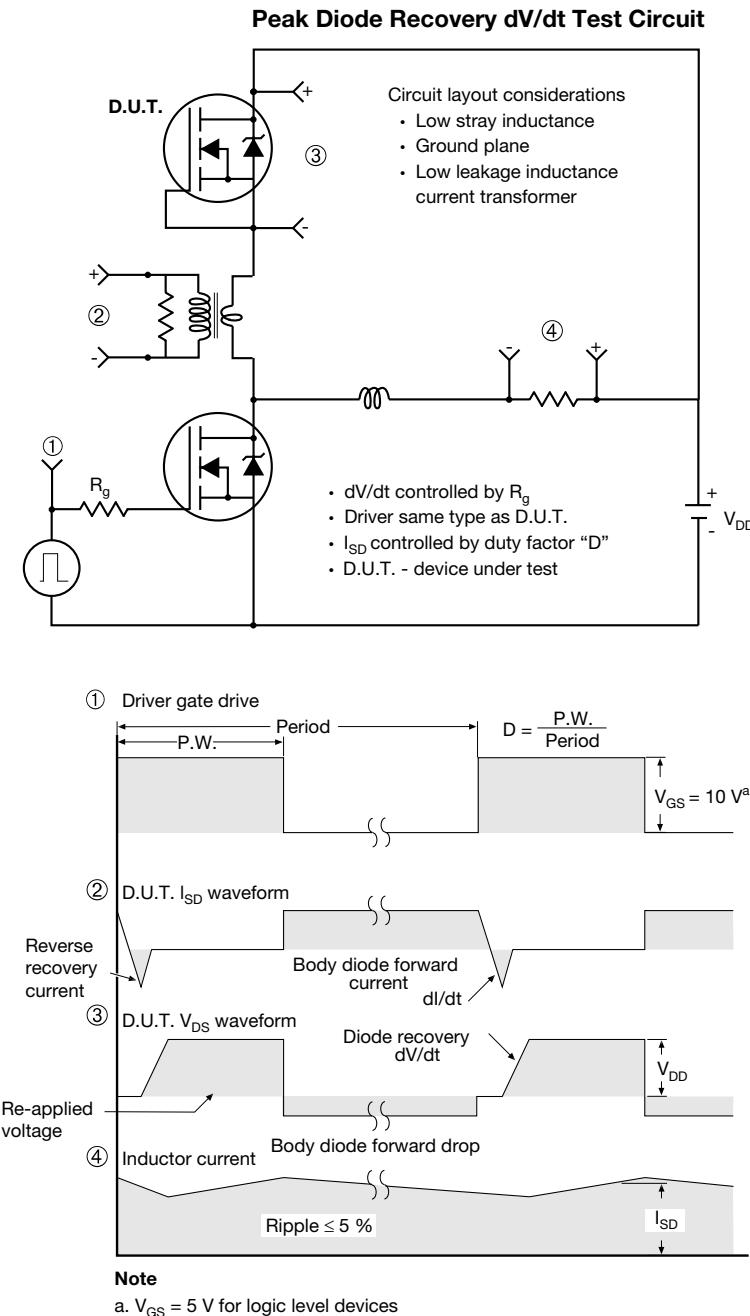


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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