Hot Swappable, Dual I²C Isolators with Integrated DC-to-DC Converter

Data Sheet

ADM3260

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
  - Regulated 3.15 V to 5.25 V output
  - Up to 150 mW output power
  - High common-mode transient immunity: >25 kV/µs
- *i*Coupler integrated I²C digital isolator
  - Bidirectional I²C communication
  - 3.0 V to 5.5 V supply/logic levels
  - Open-drain interfaces
  - Suitable for hot swap applications
  - 30 mA current sink capability
  - 1000 kHz maximum frequency
- 20-lead SSOP package with 5.3 mm creepage
- High temperature operation: 105°C
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE Certificate of Conformity (pending)
  - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak

APPLICATIONS

- Isolated I²C, SMBus, and PMBus interfaces
- Multilevel I²C interfaces
- Central office switching
- Telecommunication and data communication equipment
- −48 V distributed power systems
- −48 V power supply modules
- Networking

GENERAL DESCRIPTION

Based on the *i*Coupler® and *iso*Power® chip scale transformer technology, the ADM3260[1] is a hot swappable digital and power isolator with two nonlatching, bidirectional communication channels, supporting a complete isolated I²C interface, and an integrated isolated dc-to-dc converter, supporting up to 150 mW of isolated power conversion.

*i*Coupler is a chip scale transformer technology with functional, performance, size, and power consumption advantages as compared to optocouplers. The bidirectional I²C channels eliminate the need for splitting I²C signals into separate transmit and receive signals for use with standalone optocouplers.

FUNCTIONAL BLOCK DIAGRAM

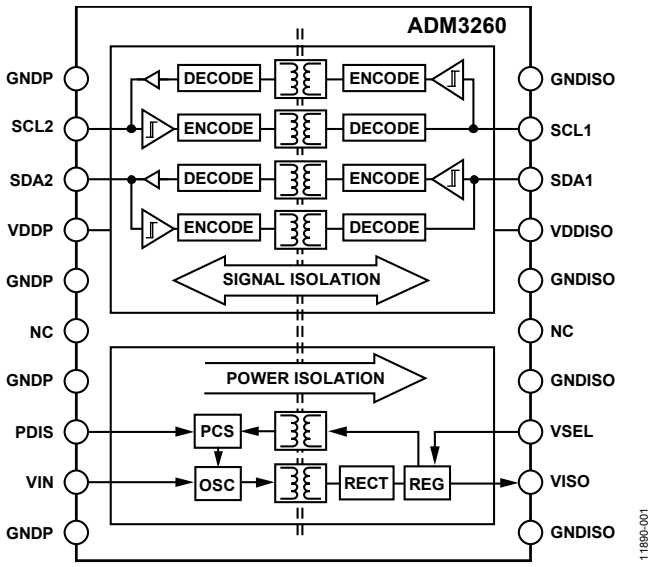

Figure 1.

Table 1. Power Levels for Isolated Converter

Input Voltage (V)	Output Voltage (V)	Output Power (mW)
5.0	5.0	150
5.0	3.3	100
3.3	3.3	66

Based on the Analog Devices, Inc., *iso*Power technology, the on-chip isolated dc-to-dc converter provides a regulated, isolated voltage of 3.15 V to 5.25 V with up to 150 mW of output power (see Figure 1).

With the ADM3260, the *i*Coupler and *iso*Power channels, along with the I²C transceivers, can be integrated with semiconductor circuitry, which enables a complete isolated I²C interface and allows the power converter to be implemented in a small form factor. The ADM3260 is available in 20-lead SSOP package and has an operating temperature range of −40°C to+105°C.

*iso*Power uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for board layout recommendations.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents are pending.

Rev. D
Document Feedback

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3/2016—Rev. B to Rev. C

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4/2015—Rev. A to Rev. B

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6/2014—Rev. 0 to Rev. A

Changes to Pin 8, Table 16 ... 11

12/2013—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, VIN = VISO = 5 V, VSEL resistor network R_{BOTTOM} = 10 kΩ, R_{TOP} = 30.9 kΩ. Minimum/maximum specifications apply over the entire recommended operation range which is 4.5 V ≤ VIN, VISO ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}		5		V	I_{ISO} = 15 mA, R_{BOTTOM} = 10 kΩ, R_{TOP} = 30.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−44		µV/°C	
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, VIN = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		75		mV p-p	20 MHz bandwidth, C_{OUTPUT_BYPASS} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		200		mV p-p	C_{OUTPUT_BYPASS} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Current	$I_{ISO (MAX)}$	30			mA	VISO > 4.5 V
Efficiency at $I_{ISO (MAX)}$			29		%	I_{ISO} = 27 mA
I_{VIN}, No V_{ISO} Load	$I_{VIN (Q)}$		6.8	12	mA	
I_{VIN}, Full V_{ISO} Load	$I_{VIN (MAX)}$		104		mA	
Thermal Shutdown						
Shutdown Temperature	$T_{SHUTDOWN}$		154		°C	
Thermal Hysteresis	T_{HYST}		10		°C	

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, VIN = 5 V, VISO = 3.3 V, VSEL resistor network R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ. Minimum/maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ VIN ≤ 5.5 V, 3 V ≤ VISO ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}		3.3		V	I_{ISO} = 15 mA, R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−26		µV/°C	
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, VIN = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUTPUT_BYPASS} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{OUTPUT_BYPASS} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Current	$I_{ISO (MAX)}$	30			mA	3 V < VISO< 3.6 V
Efficiency at $I_{ISO (MAX)}$			24		%	I_{ISO} = 27 mA
I_{VIN}, No V_{ISO} Load	$I_{VIN (Q)}$		3.2	8	mA	
I_{VIN}, Full V_{ISO} Load	$I_{VIN (MAX)}$		85		mA	
Thermal Shutdown						
Shutdown Temperature	$T_{SHUTDOWN}$		154		°C	
Thermal Hysteresis	T_{HYST}		10		°C	

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, VIN = VISO = 3.3 V, VSEL resistor network R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ. Minimum/maximum specifications apply over the entire recommended operation range which is 3.0 V ≤ VIN, VISO ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}		3.3		V	I_{ISO} = 10 mA, R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−26		µV/°C	I_{ISO} = 20 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 10 mA, VIN = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 2 mA to 18 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUTPUT_BYPASS} = 0.1 µF||10 µF, I_{ISO} = 18 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{OUTPUT_BYPASS} = 0.1 µF||10 µF, I_{ISO} = 18 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Current	$I_{ISO (MAX)}$	20			mA	3.6 V > V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			27		%	I_{ISO} = 18 mA
I_{VIN}, No V_{ISO} Load	$I_{VIN (Q)}$		3.3	10.5	mA	
I_{VIN}, Full V_{ISO} Load	$I_{VIN (MAX)}$		77		mA	
Thermal Shutdown						
Shutdown Temperature	$T_{SHUTDOWN}$		154		°C	
Thermal Hysteresis	T_{HYST}		10		°C	

DC-TO-DC CONVERTER CHARACTERISTICS

All typical specifications are at T_A = 25°C. Minimum/maximum specifications apply over the entire recommended operation range unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
UNDERVOLTAGE LOCKOUT						VIN, V_{ISO} supply
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
PDIS PIN						
Input Threshold						
Logic High	V_{IH}	0.7 VIN			V	
Logic Low	V_{IL}			0.3 VIN	V	
Input Current	I_{PDIS}	−10	+0.01	+10	µA	0 V ≤ V_{PDIS} ≤ VIN

DIGITAL ISOLATOR DC SPECIFICATIONS

All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, VDDISO = 3.3 V or 5 V, and VDDP = 3.3 V or 5 V, unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
I²C SIGNAL ISOLATION BLOCK						
Input Supply Current						
Side 1 (5 V)	I_{DDISO1}		2.8	5.0	mA	VDDISO = 5 V
Side 2 (5 V)	I_{DDP1}		2.7	5.0	mA	VDDP = 5 V
Side 1 (3.3 V)	I_{DDISO2}		1.9	3.0	mA	VDDISO = 3.3 V
Side 2 (3.3 V)	I_{DDP2}		1.7	3.0	mA	VDDP = 3.3 V
LEAKAGE CURRENTS	I_{SDA1}, I_{SDA2}, I_{SCL1}, I_{SCL2}		0.01	10	µA	V_{SDA1} = VDDISO, V_{SDA2} = VDDP, V_{SCL1} = VDDISO, V_{SCL2} = VDDP
SIDE 1 LOGIC LEVELS						
Logic Input Threshold[1]	V_{SDA1T}, V_{SCL1T}	500		700	mV	
Logic Low Output Voltages	V_{SDA1OL}, V_{SCL1OL}	600		900	mV	I_{SDA1} = I_{SCL1} = 3.0 mA
		600		850	mV	I_{SDA1} = I_{SCL1} = 0.5 mA
Input/Output Logic Low Level Difference[2]	ΔV_{SDA1}, ΔV_{SCL1}	50			mV	
SIDE 2 LOGIC LEVELS						
Input Voltage						
Logic Low	V_{SDA2IL}, V_{SCL2IL}			0.3 VDDP	V	
Logic High	V_{SDA2IH}, V_{SCL2IH}	0.7 VDDP			V	
Output Voltage						
Logic Low	V_{SDA2OL}, V_{SCL2OL}			400	mV	I_{SDA2} = I_{SCL2} = 30 mA

[1] V_{IL} < 0.5 V, V_{IH} > 0.7 V.

[2] $\Delta V_{SDA1} = V_{SDA1OL} - V_{SDA1T}$, $\Delta V_{SCL1} = V_{SCL1OL} - V_{SCL1T}$. This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the device latching up the bus to which it is connected.

DIGITAL ISOLATOR AC SPECIFICATIONS

All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, VDDISO = 3.3 V or 5 V, and VDDP = 3.3 V or 5 V, unless otherwise noted. Refer to Figure 17. All voltages are relative to their respective ground.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM FREQUENCY		1000			kHz	
OUTPUT FALL TIME						
5 V Operation						4.5 V ≤ VDDISO, VDDP ≤ 5.5 V, C_{L1} = 40 pF, R1 = 1.6 kΩ, C_{L2} = 400 pF, R2 = 180 Ω
Side 1 Output (0.9 VDDISO to 0.9 V)	t_{f1}	13	26	120	ns	
Side 2 Output (0.9 VDDP to 0.1 VDDP)	t_{f2}	32	52	120	ns	
3 V Operation						3.0 V ≤ VDDISO, VDDP ≤ 3.6 V, C_{L1} = 40 pF, R1 = 1.0 kΩ, C_{L2} = 400 pF, R2 = 120 Ω
Side 1 Output (0.9 VDDISO to 0.9 V)	t_{f1}	13	32	120	ns	
Side 2 Output (0.9 VDDP to 0.1 VDDP)	t_{f2}	32	61	120	ns	
PROPAGATION DELAY						
5 V Operation						4.5 ≤ VDDISO, VDDP ≤ 5.5 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.6 kΩ, R2 = 180 Ω
Side 1 to Side 2						
Rising Edge[1]	t_{PLH12}		95	130	ns	
Falling Edge[2]	t_{PHL12}		162	275	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Side 2 to Side 1						
Rising Edge[3]	t_{PLH21}		31	70	ns	
Falling Edge[4]	t_{PHL21}		85	155	ns	
3 V Operation						3.0 V ≤ VDDISO, VDDP ≤ 3.6 V, $C_{L1} = C_{L2} = 0$ pF, R1 = 1.0 kΩ, R2 = 120 Ω
Side 1 to Side 2						
Rising Edge[1]	t_{PLH12}		82	125	ns	
Falling Edge[2]	t_{PHL12}		196	340	ns	
Side 2 to Side 1						
Rising Edge[3]	t_{PLH21}		32	75	ns	
Falling Edge[4]	t_{PHL21}		110	210	ns	
PULSE WIDTH DISTORTION						
5 V Operation						4.5 V ≤ VDDISO, VDDP ≤ 5.5 V, $C_{L1} = C_{L2} = 0$ pF, R1 = 1.6 kΩ, R2 = 180 Ω
Side 1 to Side 2, $\lvert t_{PLH12} - t_{PHL12} \rvert$	PWD_{12}		67	145	ns	
Side 2 to Side 1, $\lvert t_{PLH21} - t_{PHL21} \rvert$	PWD_{21}		54	85	ns	
3 V Operation						3.0 V ≤ VDDISO, VDDP ≤ 3.6 V, $C_{L1} = C_{L2} = 0$ pF, R1 = 1.0 kΩ, R2 = 120 Ω
Side 1 to Side 2, $\lvert t_{PLH12} - t_{PHL12} \rvert$	PWD_{12}		114	215	ns	
Side 2 to Side 1, $\lvert t_{PLH21} - t_{PHL21} \rvert$	PWD_{21}		77	135	ns	
COMMON-MODE TRANSIENT IMMUNITY[5]	$\lvert CM_H \rvert$, $\lvert CM_L \rvert$	25	35		kV/µs	

[1] t_{PLH12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.7 VDDP.
[2] t_{PHL12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.4 V.
[3] t_{PLH21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.7 VDDISO.
[4] t_{PHL21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.9 V.
[5] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8$ VDDP. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

PACKAGE CHARACTERISTICS

Table 8. Thermal and Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		50		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[3]

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together; and Pin 11 through Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS

Table 9.

UL[1]	CSA	VDE (Pending)[2]
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single Protection, 2500 V RMS Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADM3260 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, ADM3260 is proof tested by applying an insulation test voltage ≥1590 V peak for 1 second (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 10. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	5.1	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	5.1	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(PCB)	5.5	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane (for information only)
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 11. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	840	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Highest Allowable Overvoltage		V_{IOTM}	3535	V peak
Surge Isolation Voltage	$V_{IOSM(TEST)} = 10$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Converter Safety Total Dissipated Power		I_{S1}	2.5	W
VDDP + VDDISO Current		I_{TMAX}	212	mA
Insulation Resistance at T_S for Isolated Converter	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

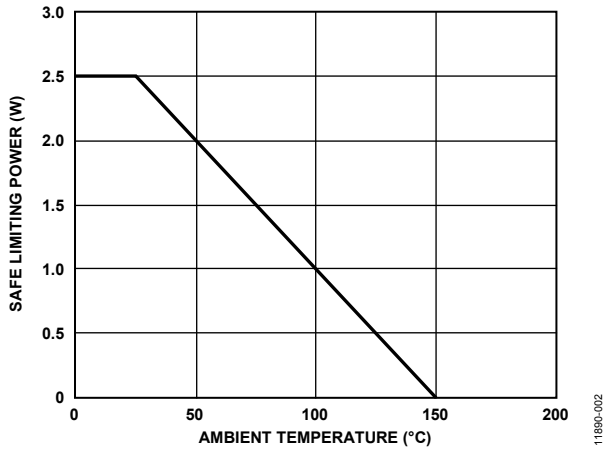


Figure 2. Isolated Converter Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

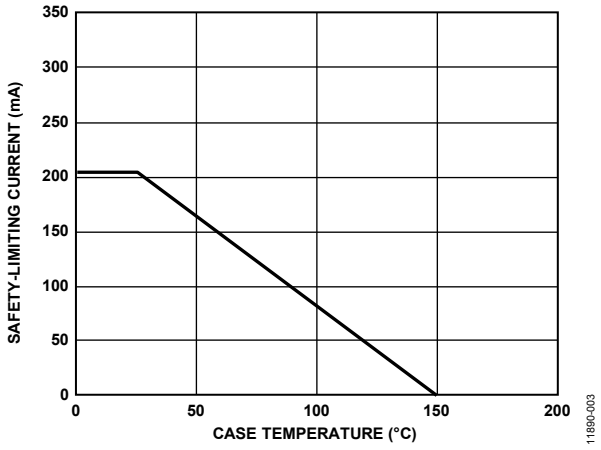


Figure 3. Digital Isolator Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 12.

Parameter	Value
OPERATING TEMPERATURE[1]	−40°C to +105°C
ISOLATED CONVERTER	
Supply Voltages[2]	
VIN at VISO Set to Regulate to 3.3 V	3.0 V to 5.5 V
VIN at VISO Set to Regulate to 5 V	4.5 V to 5.5 V
DIGITAL ISOLATOR	
Supply Voltages (VDDISO, VDDP)[3]	3.0 V to 5.5 V
Input/Output Signal Voltage (V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2})	5.5 V
Capacitive Load	
Side 1 (C_{L1})	40 pF
Side 2 (C_{L2})	400 pF
STATIC OUTPUT LOADING	
Side 1 (I_{SDA1}, I_{SCL1})	0.5 mA to 3 mA
Side 2 (I_{SDA2}, I_{SCL2})	0.5 mA to 30 mA

[1] Operation at 105°C requires reduction of the maximum load current (see Table 13).
[2] Each voltage is relative to its respective ground.
[3] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 13.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (VIN, VISO)[1]	−0.5 V to +7.0 V
Supply Voltages (VDDISO, VDDP)[1]	−0.5 V to +7.0 V
VISO Supply Current[2]	
T_A = −40°C to +105°C	30 mA
Digital Isolator Average Output Current per Pin[3]	
Side 1 (I_{O1})	±18 mA
Side 2 (I_{O2})	±100 mA
Input/Output Voltage	
Side 1 (V_{SDA1}, V_{SCL1})[3]	−0.5 V to VDDISO + 0.5 V
Side 2 (V_{SDA2}, V_{SCL2})[3]	−0.5 V to VDDP + 0.5 V
Input Voltage (PDIS, VSEL)[1, 4]	−0.5 V to VIN + 0.5 V
Common-Mode Transients[5]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] VISO provides current for dc and dynamic loads on the VISO input/output channels. This current must be included when determining the total VISO supply current.
[3] See Figure 3 for maximum rated current values for various temperatures.
[4] V_{CC} can be either VIN or VISO depending on the whether the input is on the primary or secondary side of the device, respectively.
[5] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 14. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Maximum	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	560	V peak	All certifications, 50-year operation
Unipolar Waveform	560	V peak	
DC Voltage			
|DC Peak Voltage|	560	V peak	

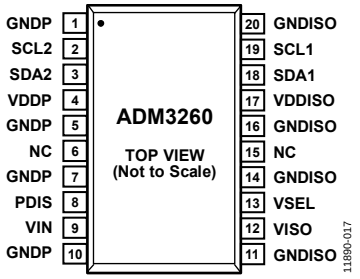
[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

VISO VOLTAGE TRUTH TABLE

Table 15. Truth Table (Positive Logic)

VIN (V)	VSEL Input	PDIS Input	VISO Output (V)	Notes
5	R_{BOTTOM} = 10 kΩ, R_{TOP} = 30.9 kΩ	Low	5	
5	R_{BOTTOM} = 10 kΩ, R_{TOP} = 30.9 kΩ	High	0	
3.3	R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ	Low	3.3	
3.3	R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ	High	0	
5	R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ	Low	3.3	
5	R_{BOTTOM} = 10 kΩ, R_{TOP} = 16.9 kΩ	High	0	
3.3	R_{BOTTOM} = 10 kΩ, R_{TOP} = 30.9 kΩ	Low	5	Configuration not recommended
3.3	R_{BOTTOM} = 10 kΩ, R_{TOP} = 30.9 kΩ	High	0	

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN

Figure 4. Pin Configuration

Table 16. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 7 ,10	GNDP	Ground Reference for Primary Side. Connect all GNDP pins to the primary ground reference.
2	SCL2	Clock Input/Output, Primary Side.
3	SDA2	Data Input/Output, Primary Side.
4	VDDP	Digital Isolator Primary Supply Input, 3.0 V to 5.5 V.
6, 15	NC	No Connect. Do not connect to this pin.
8	PDIS	Power Disable. When PDIS is tied to VIN, the power supply enters low power standby mode. When PDIS is tied to GNDP, the power converter is active.
9	VIN	*iso*Power Converter Primary Supply Input, 3.0 V to 5.5 V.
11, 14, 16, 20	GNDISO	Ground Reference for Isolated Side. Connect all GNDISO pins to the isolated ground reference.
12	VISO	Secondary Supply Voltage Output for Digital Isolator Isolated Side Power and External Loads. The output voltage is adjustable from 3.15 V to 5.25 V.
13	VSEL	Output Voltage Set. Provide a thermally matched resistor network between VISO and GNDISO to divide the required output voltage to match the 1.25 V reference voltage. The VISO voltage can be programmed up to 20% higher or 75% lower than VIN but must be within the allowed output voltage range.
17	VDDISO	Digital Isolator Isolated Side Supply Input, 3.0 V to 5.5 V.
18	SDA1	Data Input/Output, Isolated Side.
19	SCL1	Clock Input/Output, Isolated Side.

TYPICAL PERFORMANCE CHARACTERISTICS

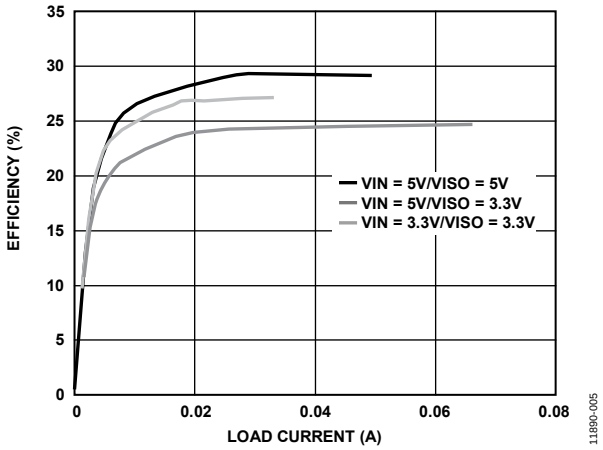


Figure 5. Typical Power Supply Efficiency at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

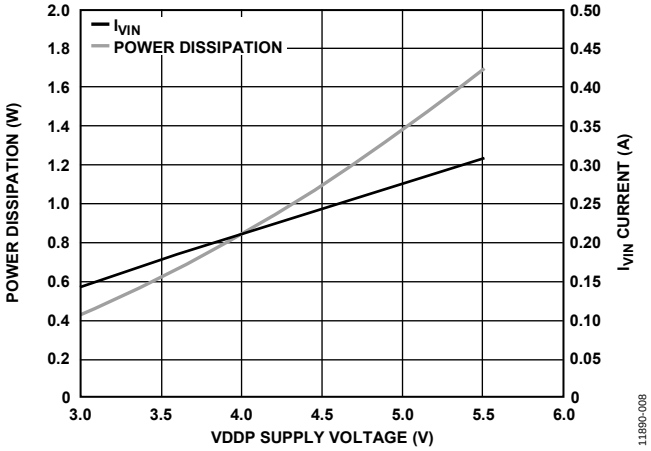


Figure 8. Power Dissipation and I_{VIN} Current vs. VDDP Supply Voltage

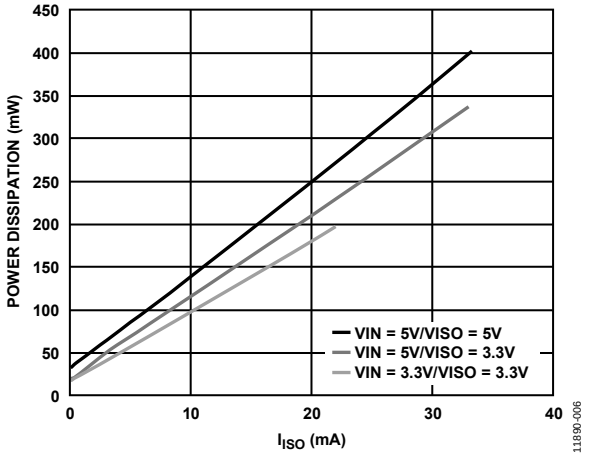


Figure 6. Typical Total Power Dissipation vs. I_{ISO}

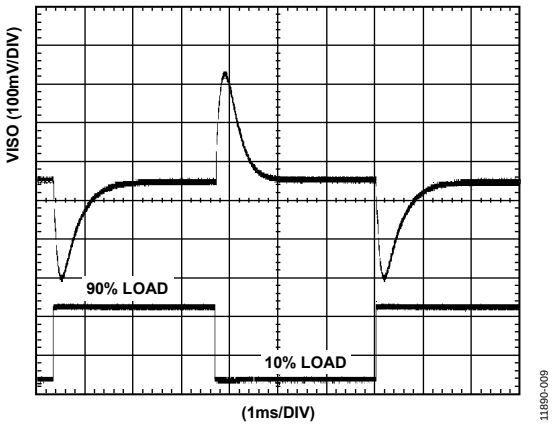


Figure 9. Typical VISO Transient Load Response, 5 V Output, 10% to 90% Load Step

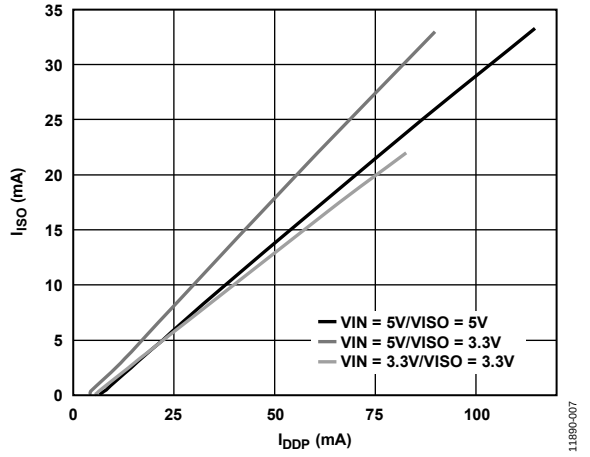


Figure 7. Typical Isolated Output Supply Current (I_{ISO}) as a Function of External Load at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

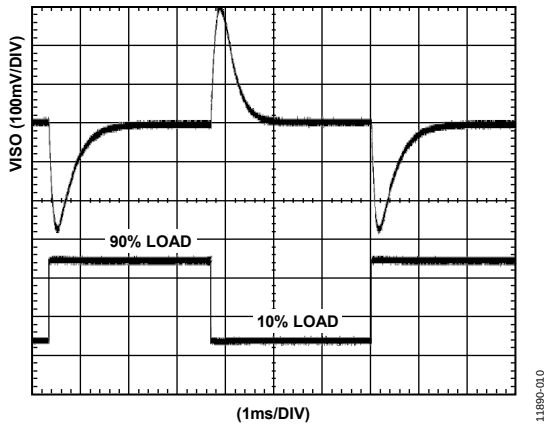


Figure 10. Typical VISO Transient Load Response, 3.3 V Input, 3.3 V Output, 10% to 90% Load Step

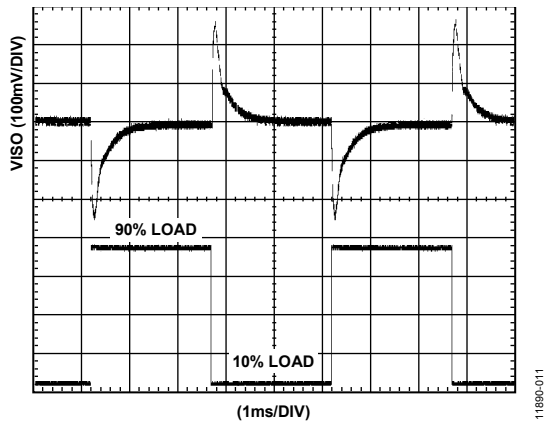


Figure 11. Typical VISO Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

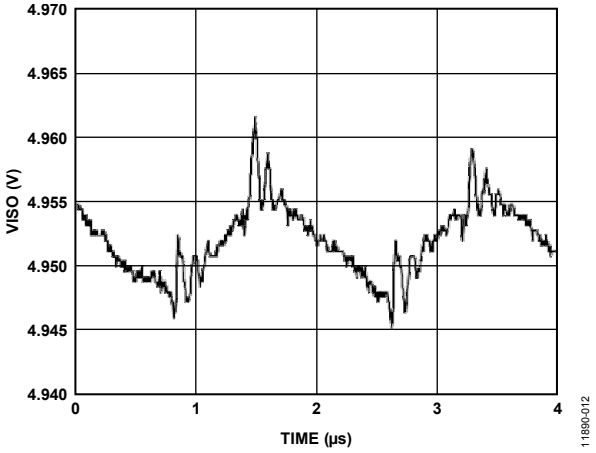


Figure 12. Typical VISO = 5 V Output Voltage Ripple at 90% Load

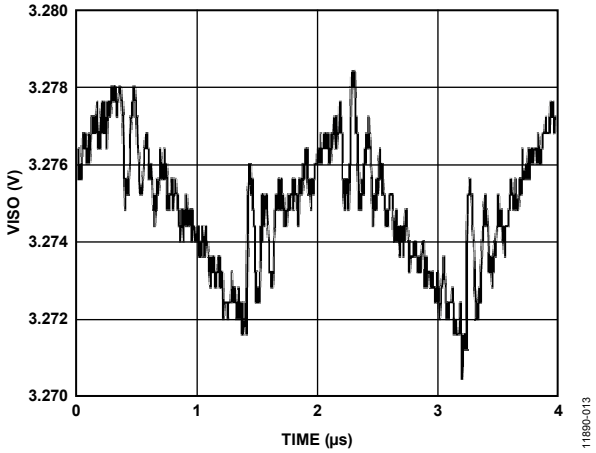


Figure 13. Typical VISO = 3.3 V Output Voltage Ripple at 90% Load

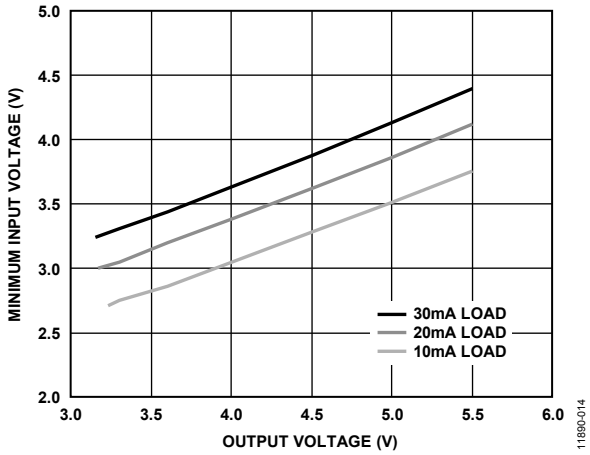


Figure 14. Relationship Between Output Voltage and Required Input Voltage, Under Load to Maintain >80% Duty Factor in the PWM

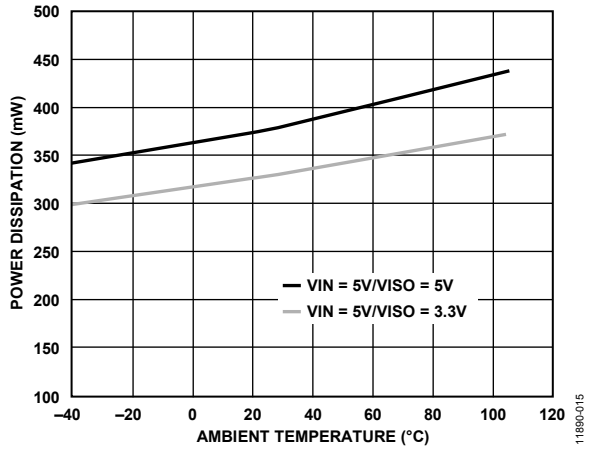


Figure 15. Power Dissipation with a 30 mA Load vs. Ambient Temperature

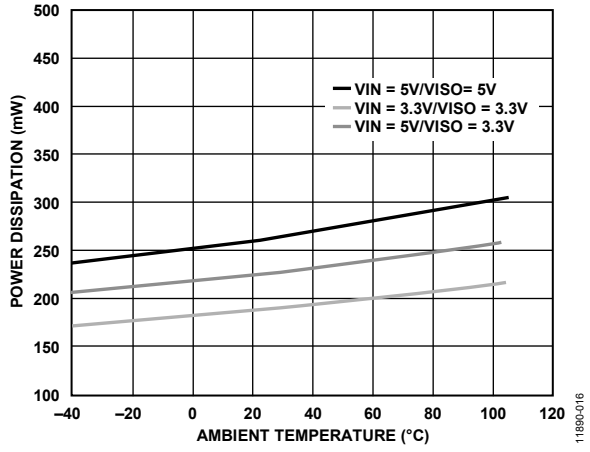


Figure 16. Power Dissipation with a 20 mA Load vs. Ambient Temperature

TEST CONDITION

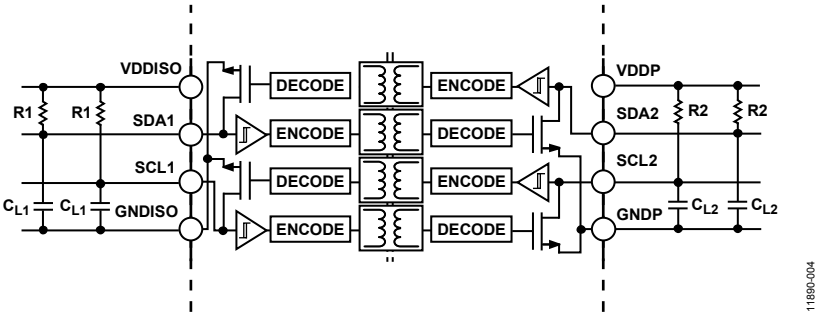


Figure 17. Timing Test Diagram

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The digital isolator block on the ADM3260 interfaces on each side to a bidirectional I²C signal. Internally, the I²C interface is split into two unidirectional channels communicating in opposing directions via a dedicated *i*Coupler isolation channel for each. One channel (the bottom channel of each channel pair shown in Figure 17) senses the voltage state of the Side 1 I²C pin (SCL1 or SDA1) and transmits its state to its respective Side 2 I²C pin (SCL2 or SDA2).

Both the Side 1 (isolated side) and the Side 2 (primary side) I²C pins interface to an I²C bus operating in the 3.0 V to 5.5 V range. A logic low on either pin causes the opposite pin to pull low enough to comply with the logic low threshold requirements of the other I²C devices on the bus. To avoid I²C bus contention, input a low threshold at SDA1 or SCL1 to guarantee at least 50 mV less than the output low signal at the same pin. This step prevents an output logic low at Side 1 from transmitting back to Side 2 and pulling down the I²C bus.

Because the Side 2 logic levels or thresholds are standard I²C values, multiple ADM3260 devices connected to a bus by their Side 2 pins communicate with each other and with other I²C-compatible devices. I²C compatibility refers to situations in which the logic levels of a component do not necessarily meet the requirements of the I²C specification but still allow the component to communicate with an I²C-compliant device. I²C compliance refers to situations in which the logic levels of a component meet the requirements of the I²C specification.

However, because the Side 1 pin has a modified output level/input threshold, this side of the ADM3260 communicates only with devices that conform to the I²C standard. In other words, Side 2 of the ADM3260 is I²C compliant, whereas Side 1 is only I²C compatible.

The output logic low levels are independent of the VDDISO and VDDP voltages. The input logic low threshold at Side 1 is also independent of VDDISO. However, the input logic low threshold at Side 2 is at 0.3 VDDP, consistent with I²C requirements. The Side 1 and Side 2 pins have open-collector outputs whose high levels are set via pull-up resistors to their respective supply voltages.

The dc-to-dc converter section of the ADM3260 works on principles that are common to most modern power supplies. It has a split controller architecture with isolated pulse-width modulation (PWM) feedback. VIN power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to a value between 3.15 V and 5.25 V depending on the setpoint supplied by an external voltage divider (see Equation 1). The secondary (VISO) side controller regulates the output by creating a PWM control signal that is sent to the primary (VIN) side by a dedicated *i*Coupler data channel.

The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

$$VISO = 1.23 \times \frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}} (\text{V}) \quad (1)$$

where:
R_{TOP} is a resistor between VSEL and VISO.
R_{BOTTOM} is a resistor between VSEL and GNDISO.

Because the output voltage is adjusted continuously, there are an infinite number of operating conditions. This data sheet addresses three discrete operating conditions in the Specifications section. Many other combinations of input and output voltage are possible; Figure 14 depicts the supported voltage combinations at room temperature. Figure 14 was generated by using a fixed VISO load and decreasing the input voltage until the PWM was at 80% duty cycle. Each of the curves represents the minimum input voltage that is required for operation under this criterion. For example, if the application requires 30 mA of output current at 5 V, the minimum input voltage at VIN is 4.25 V. Figure 14 also illustrates that a configuration with VIN = 3.3 V and VISO = 5 V is not recommended. Even at 10 mA of output current, the PWM cannot maintain less than 80% duty factor, leaving no margin to support load or temperature variations.

Typically, the dc-to-dc converter section of the ADM3260 dissipates about 17% more power between room temperature and maximum temperature; therefore, the 20% PWM margin covers temperature variations.

The isolated converter implements undervoltage lockout (UVLO) with hysteresis on the input/output pins of the primary and secondary sides as well as the VIN power input. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

DIGITAL ISOLATOR STARTUP

Both the VDDISO and VDDP supplies of the digital isolator block have an undervoltage lockout feature to prevent the signal channels from operating unless certain criteria are met. This feature prevents input logic low signals from pulling down the I²C bus inadvertently during power-up/power-down.

To enable the signal channels, the following two criteria must be met:

- Both supplies must be at least 2.5 V.
- At least 40 µs must elapse after both supplies exceed the internal start-up threshold of 2.0 V.

Until both criteria are met for both supplies, pull the outputs of the digital isolator block of the ADM3260 high, ensuring a startup that avoids any disturbances on the bus.

Figure 18 and Figure 19 illustrate the supply conditions for fast and slow input supply slew rates.

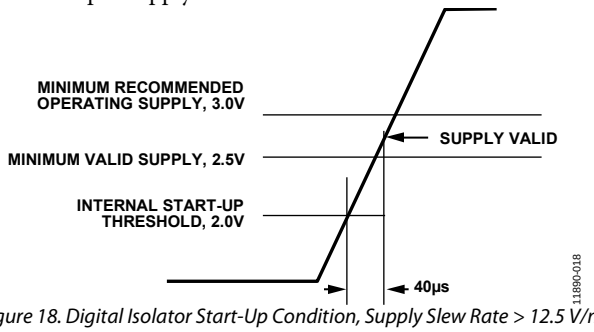


Figure 18. Digital Isolator Start-Up Condition, Supply Slew Rate > 12.5 V/ms

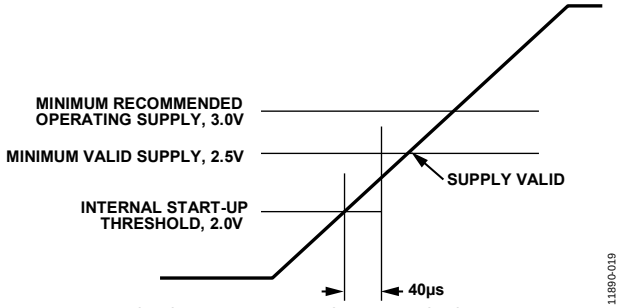


Figure 19. Digital Isolator Start-Up Condition, Supply Slew Rate < 12.5 V/ms

TYPICAL APPLICATION DIAGRAM

Figure 20 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2 buses. Bypass capacitor with values from 0.01 µF to 0.1 µF are required between VDDP and GNDP and between VDDISO and GNDISO.

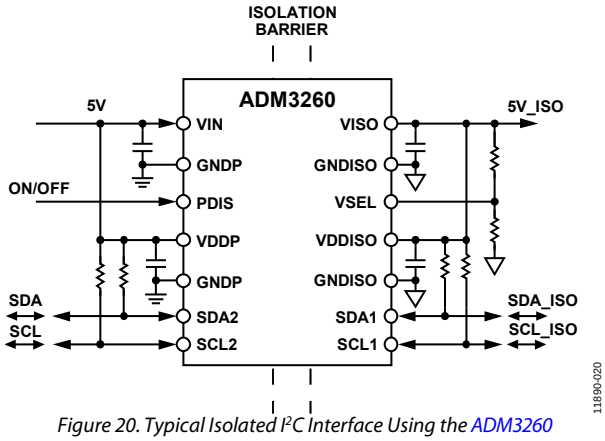


Figure 20. Typical Isolated I²C Interface Using the ADM3260

PCB LAYOUT

Supply bypassing of the 0.15 W *iso*Power integrated dc-to-dc converter with a low ESR capacitor is required as near the chip pads as possible. The *iso*Power inputs require several passive components to bypass the power effectively, as well as to set the output voltage and to bypass the core voltage regulator (see Figure 21 through Figure 23).

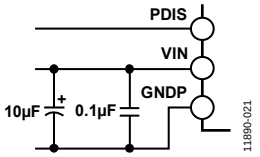


Figure 21. VIN Bias and Bypass Components

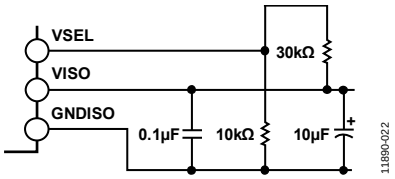


Figure 22. VISO Bias and Bypass Components

The power supply section of the ADM3260 uses a 125 MHz oscillator frequency to efficiently pass power through its chip-scale transformers. Choose bypass capacitors carefully because they must perform more than one function. Noise suppression requires a low inductance, high frequency capacitor; ripple suppression and proper regulation require a large value bulk capacitor. Connect these capacitors most conveniently between Pin VIN and Pin GNDP for VIN and between Pin VISO and Pin GNDISO for VISO. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for VIN. The smaller capacitor must have a low ESR; for example, use of an NP0 or X5R ceramic capacitor is advised. Ceramic capacitors are also recommended for the 10 mF bulk capacitance. Add an additional 10 nF capacitor in parallel if further EMI/EMC control is desired.

Do not exceed 2 mm for the total lead length between the ends of the low ESR capacitor and the input power supply.

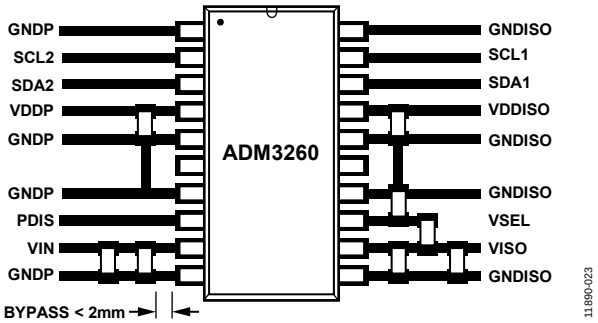


Figure 23. Recommended PCB Layout

In applications involving high common-mode transients, design the board layout such that any coupling that does occur affects all pins on a given component side equally. Failure to ensure this can cause voltage differentials between pins, exceeding the absolute maximum ratings specified in Table 13, and thereby leading to latch-up and/or permanent damage.

THERMAL ANALYSIS

The ADM3260 consist of four internal die attached to a split lead frame with four die attach paddles. For the purposes of thermal analysis, treat the chip as a thermal unit, with the highest junction temperature reflected in the θ_{JA} value from Table 8. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM3260 operates at a full load across the full temperature range without derating the output current.

Power dissipation in the device varies with ambient temperature due to the characteristics of the switching and rectification elements. Figure 15 and Figure 16 show the relationship between total power dissipation at two load conditions and ambient temperature. Use this information to determine the junction temperature at various operating conditions to ensure that the device does not go into thermal shutdown unexpectedly.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADM3260 components must operate at a very high frequency to allow efficient power transfer through the small transformers. This high frequency operation creates high frequency currents that propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in the layout of the PCB. See the AN-0971 Application Note for the most current PCB layout recommendations for the ADM3260.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3260.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 14 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADM3260 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 24, Figure 25, and Figure 26 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 14 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 25 or Figure 26 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 50-year lifetime voltage value listed in Table 14.

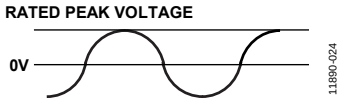


Figure 24. Bipolar AC Waveform

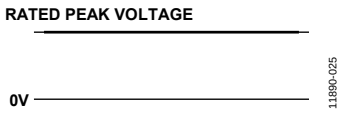


Figure 25. DC Waveform

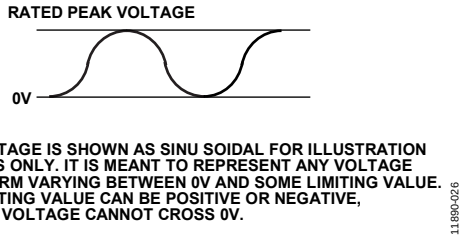


Figure 26. Unipolar AC Waveform

APPLICATIONS EXAMPLE

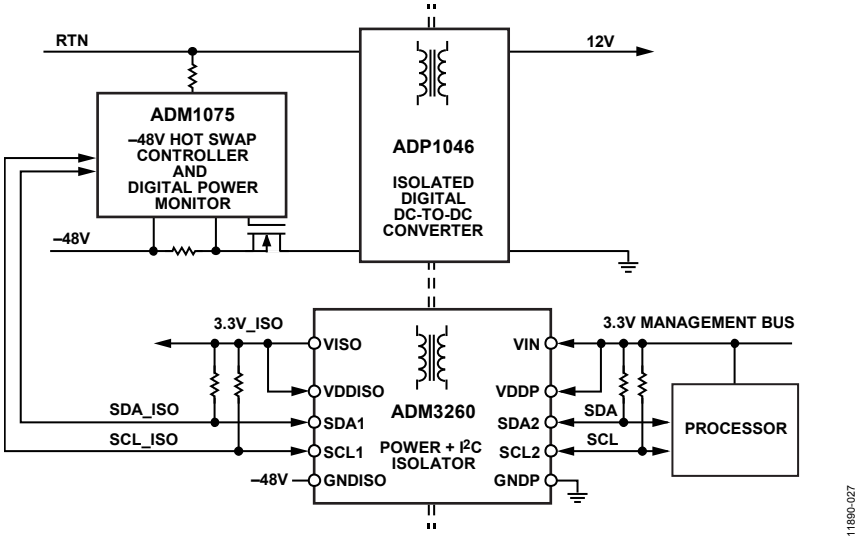


Figure 27. The ADM3260 Used in –48 V Power Monitoring and Control

OUTLINE DIMENSIONS

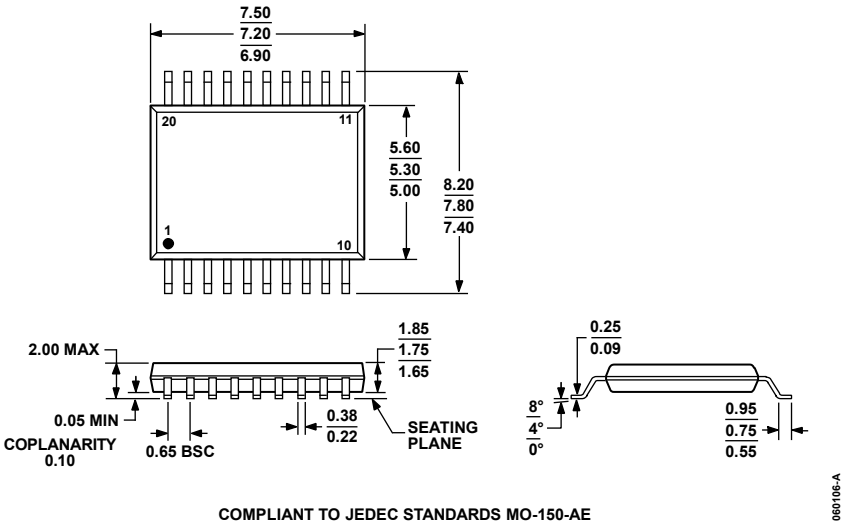


Figure 28. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3260ARSZ	−40°C to +105°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADM3260ARSZ-RL7	−40°C to +105°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
EVAL-ADM3260EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D11890-0-11/17(D)

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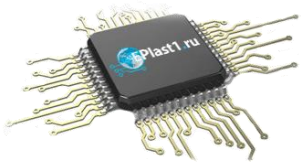
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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