

EQVA23C1C1H-50.000M

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REGULATORY COMPLIANCE (Data Sheet downloaded on Jun 14, 2020)


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ITEM DESCRIPTION

Voltage Controlled Quartz Crystal Clock Oscillators VCXO LVCMOS (CMOS) 3.3Vdc 6 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 50.000MHz ± 50 ppm -40°C to +85°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	50.000MHz
Frequency Tolerance/Stability	± 50 ppm Maximum (Inclusive of all conditions: Calibration Tolerance (at 25°C), Frequency Stability over the Operating Temperature Range, Supply Voltage Change and Output Load Change)
Aging at 25°C	± 2 ppm Maximum First Year, ± 10 ppm/10 Years Maximum
Operating Temperature Range	-40°C to +85°C
Supply Voltage	3.3Vdc $\pm 5\%$
Input Current	20mA Maximum (Unloaded)
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	3nSec Maximum (Measured at 10% to 90% of Waveform)
Duty Cycle	50 ± 10 (%) (Measured at 50% of Waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Absolute Pull Range	± 30 ppm Minimum (Inclusive of all conditions: Calibration Tolerance (at 25°C), Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, Vibration, and 10 Year Aging over the Control Voltage (Vc))
Control Voltage	0.3Vdc to 3.0Vdc (Test Condition for APR)
Control Voltage Range	0.0Vdc to Vdd +0.6Vdc
Linearity	5% Typical, 10% Maximum
Transfer Function	Positive Transfer Characteristic
Modulation Bandwidth	10kHz Minimum (Measured at -3dB, Vc = 1.65Vdc)
Input Impedance	500kOhms Minimum
Input Leakage Current	10 μ A Maximum
Phase Noise	-64dBc/Hz at 10Hz offset; -96dBc/Hz at 100Hz offset; -124dBc/Hz at 1kHz offset; -131dBc/Hz at 10kHz offset; -132dBc/Hz at 100kHz offset; -149dBc/Hz at 1MHz offset; -157dBc/Hz at 10MHz offset; -159dBc/Hz at 20MHz offset (All Values are Typical)
Output Control Function	Output Enable (OE)
Output Control Input Voltage Logic High (Vih)	90% of Vdd Minimum or No Connect to Enable Output
Output Control Input Voltage Logic Low (Vil)	10% of Vdd Maximum to Disable Output (High Impedance)
Output Enable Time	100nSec Maximum
Output Disable Time	50nSec Maximum
Output Enable Current	18mA Maximum (Without Load (Pin 2 = Ground))
RMS Phase Jitter	1.5pSec Maximum (Fj=12kHz to 20MHz (Random))
Period Jitter (Deterministic)	0.2pSec Typical
Period Jitter (Random)	2pSec Typical
Period Jitter (RMS)	3pSec Maximum
Period Jitter (pk-pk)	30pSec Maximum
Start Up Time	10mSec Maximum

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ELECTRICAL SPECIFICATIONS CONTINUED

Storage Temperature Range	-55°C to +125°C
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ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)



PIN	CONNECTION
1	Control Voltage
2	Output Enable (OE)
3	Case/Ground
4	Output
5	Do Not Connect
6	Supply Voltage

LINE	MARKING
1	E50.000 <i>E=Ecliptek Designator</i>
2	XXXXX <i>XXXXX=Ecliptek Manufacturing Identifier</i>

Suggested Solder Pad Layout

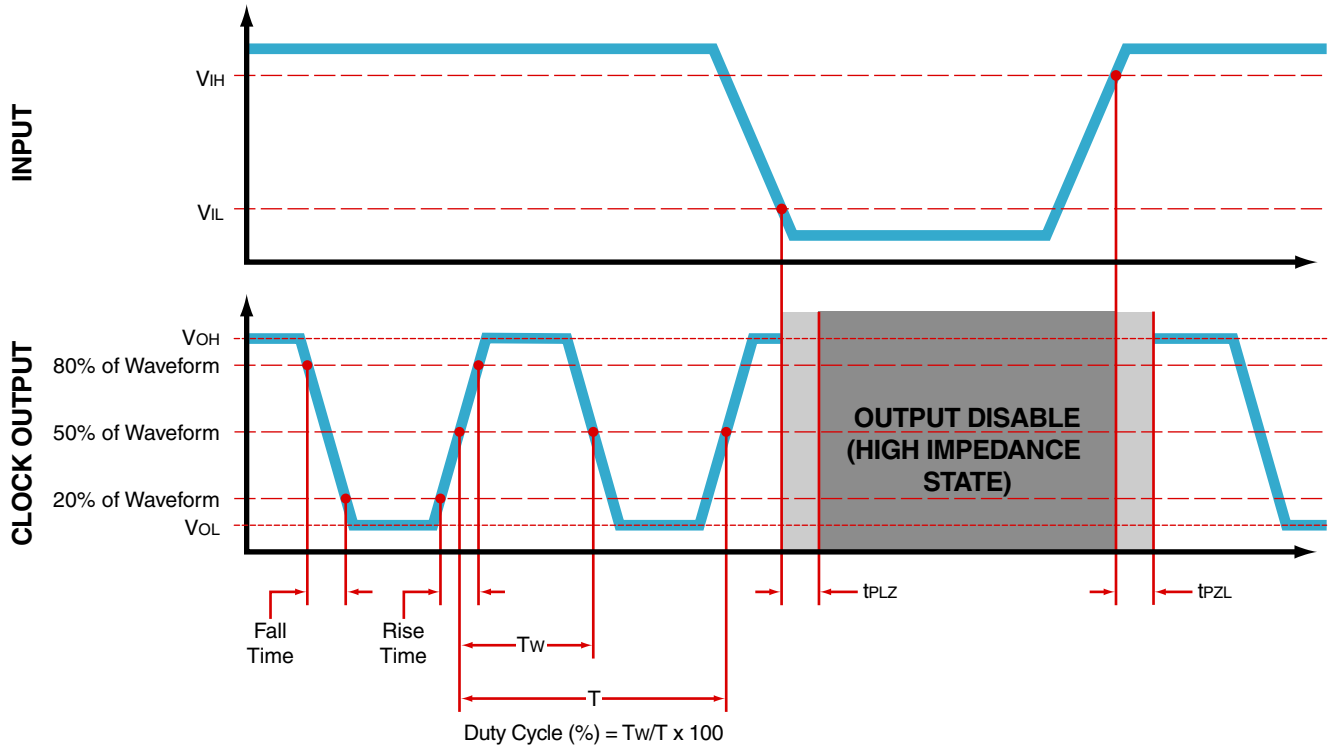
All Dimensions in Millimeters



All Tolerances are ± 0.1

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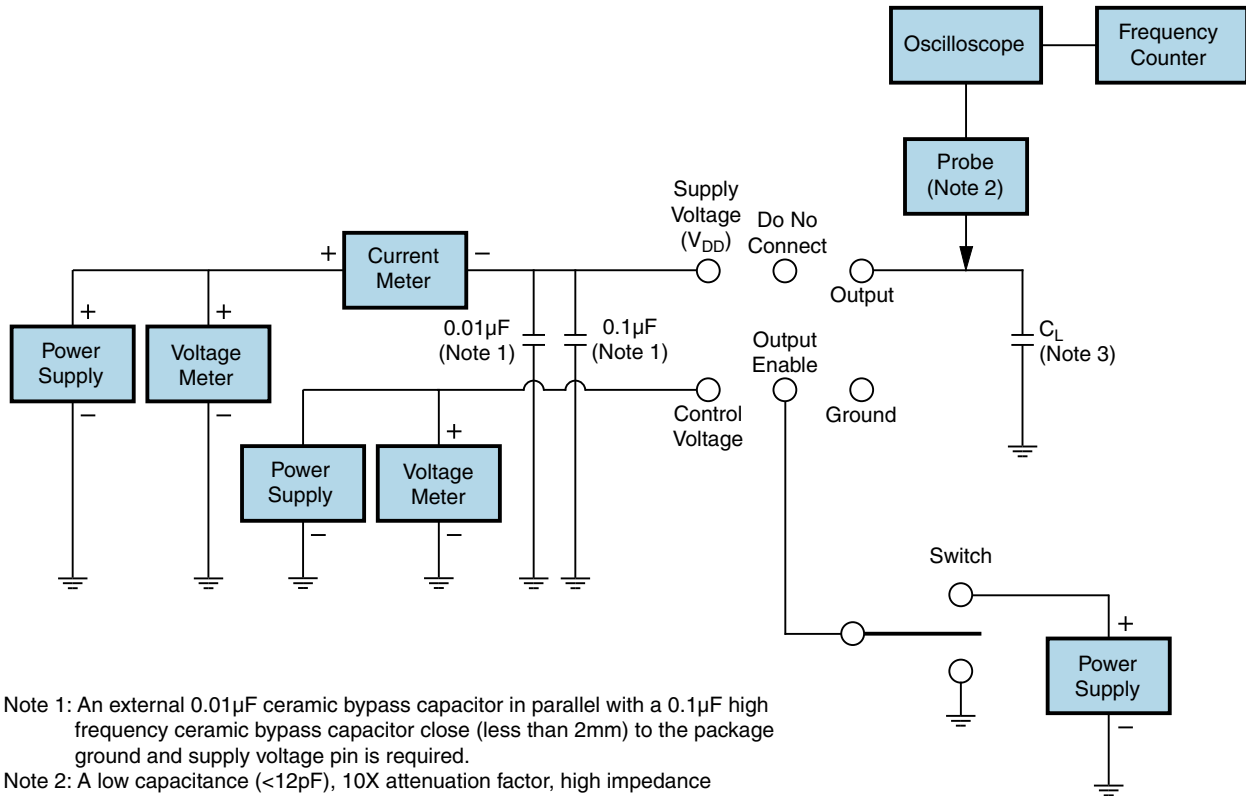
OUTPUT WAVEFORM & TIMING DIAGRAM



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Test Circuit for CMOS Output



Note 1: An external $0.01\mu\text{F}$ ceramic bypass capacitor in parallel with a $0.1\mu\text{F}$ high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>300\text{MHz}$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

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Recommended Solder Reflow Methods



High Temperature Infrared/Convection

$T_s \text{ MAX}$ to T_L (Ramp-up Rate)	3°C/Second Maximum
Preheat	
- Temperature Minimum ($T_s \text{ MIN}$)	150°C
- Temperature Typical ($T_s \text{ TYP}$)	175°C
- Temperature Maximum ($T_s \text{ MAX}$)	200°C
- Time ($t_s \text{ MIN}$)	60 - 180 Seconds
Ramp-up Rate (T_L to T_P)	3°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	217°C
- Time (t_L)	60 - 150 Seconds
Peak Temperature (T_P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature ($T_P \text{ Target}$)	250°C +0/-5°C
Time within 5°C of actual peak (t_p)	20 - 40 Seconds
Ramp-down Rate	6°C/Second Maximum
Time 25°C to Peak Temperature (t)	8 Minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

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Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T_s MAX to T_L (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (T_s MIN)	N/A
- Temperature Typical (T_s TYP)	150°C
- Temperature Maximum (T_s MAX)	N/A
- Time (t_s MIN)	60 - 120 Seconds
Ramp-up Rate (T_L to T_P)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	150°C
- Time (t_L)	200 Seconds Maximum
Peak Temperature (T_P)	240°C Maximum
Target Peak Temperature (T_P Target)	240°C Maximum 2 Times / 230°C Maximum 1 Time
Time within 5°C of actual peak (t_p)	10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.