ANALOG MONITORING AND CONTROL CIRCUIT

FEATURES

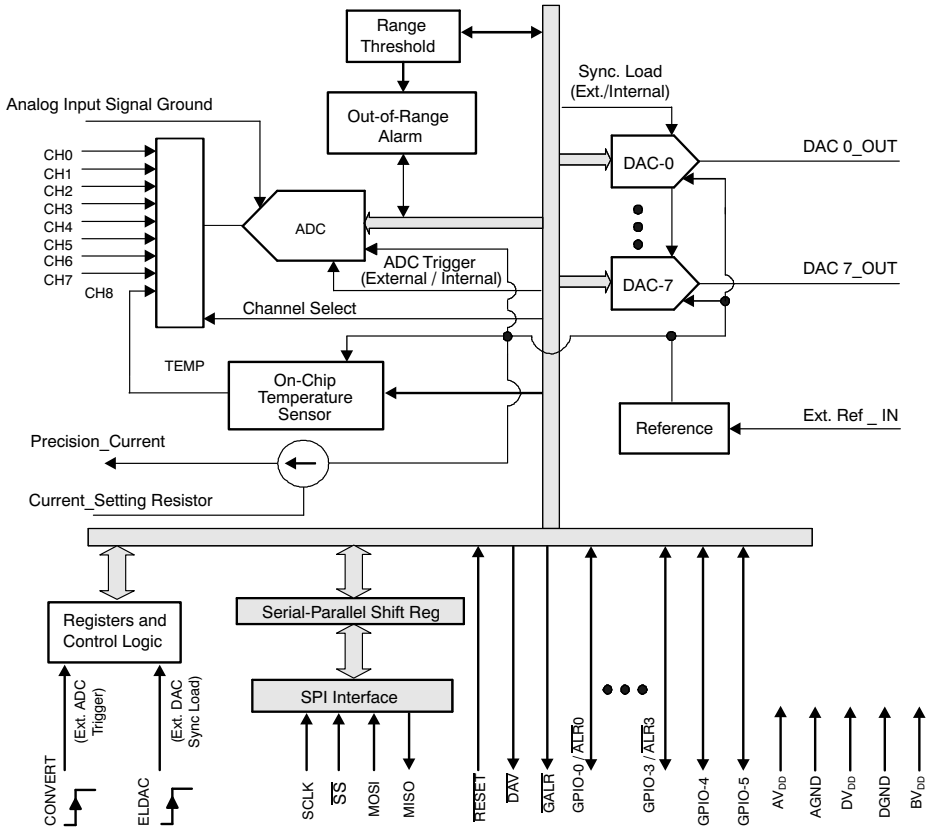
- **12-Bit ADC (200 kSPS)**
  - **Eight Analog Inputs**
  - **Input Range 0 to 2 × V_{REF}**
- **Programmable V_{REF}, 1.25 V or 2.5 V**
- **Eight 12-Bit DACs (2-μs Settling Time)**
- **Four Analog Input Out-of-Range Alarms**
- **Six General-Purpose Digital I/O**
- **Internal Bandgap Reference**
- **On-Chip Temperature Sensor**
- **Precision Current Source**
- **SPI™ Interface, 3-V or 5-V Logic Compatible**
- **Single 3-V to 5-V Supply**
- **Power-Down Mode/Low Power**
- **Small Package (QFN-40, 6 × 6 mm)**

APPLICATIONS

- **Communications Equipment**
- **Optical Networks**
- **Automatic Test Equipment**
- **Industrial Control and Monitor**
- **Medical Equipment**

DESCRIPTION

The AMC7823 is a complete analog monitoring and control circuit that includes an 8-channel, 12-bit analog-to-digital converter (ADC), eight 12-bit digital-to-analog converters (DACs), four analog input out-of-range alarms, and six GPIOs to monitor analog signals and control external devices. Also, the AMC7823 has an internal sensor to monitor chip temperature, and a precision current source to drive remote thermistors, or RTDs, to monitor remote temperatures.



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DESCRIPTION (CONTINUED)

The AMC7823 has an internal programmable reference (+2.5 V or +1.25 V), and an SPI serial interface. An external reference can be used as well. Typical power dissipation is 100 mW. The analog input range is 0 V to +5 V, and the analog output range is 0 V to +2.5 V or 0 V to +5 V. The AMC7823 is ideal for multichannel applications where low power and small size are critical. The AMC7823 is available in a 40-lead QFN package and is fully specified over the –40°C to +85°C temperature range.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AMC7823	QFN-40 (RTA)	–40°C to 85°C	AMC7823	AMC7823IRTAT	Tape and Reel, 250
			AMC7823	AMC7823IRTAR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted((1))

		AMC7823	UNIT
AV_{DD}, DV_{DD}, BV_{DD} to GND		–0.3 to +6	V
Digital input voltage to GND		–0.3 to BV_{DD} + 0.3	V
Analog input voltage to GND		–0.3 to AV_{DD} + 0.3	V
Input current, continuous		±20	mA
Input current, momentary		±100	mA
Operating temperature range		–40 to +105	°C
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+150	°C
Power dissipation		(T_J max – T_A) / θ_{JA}	W
Thermal impedance, θ_{JC}		15	°C/W
Thermal impedance, θ_{JA}		60	°C/W
Lead temperature (soldering)	Vapor phase (60s)	+215	°C
Lead temperature (soldering)	Infrared (15s)	+220	°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: +5 V

At –40°C to +85°C, AV_{DD} = 5 V, DV_{DD} = 5 V, BV_{DD} = 3 V to 5 V, using external 2.5-V reference (unless otherwise noted).

PARAMETER	CONDITIONS	AMC7823			UNITS
		MIN	TYP	MAX	
ADC ANALOG INPUTS					
Input voltage range		0		$2 \times V_{REF}$	V
Input impedance			5		MΩ
Input capacitance			15		pF
Input leakage current			±1		µA
ANALOG-TO-DIGITAL CONVERTER					
Resolution				12	Bits
No missing codes		12			Bits
Integral linearity				±1	LSB(1)
Differential linearity				±1	LSB
Offset error				±2	LSB
Offset error drift			±4		ppmFS/°C
Offset error match			0.5	1	LSB
Gain error				±6	LSB
Gain error match			0.3	1	LSB
Noise			70		μV_{RMS}
Power-supply rejection	AV_{DD} = 5 V ±5%		70		dB
Throughput rate			200		kHz
Total conversion time	Scan Channels 0 through 7		45		µs
Total conversion time including temperature	Scan Channels 0 through 8		56		µs
Channel-to-channel isolation	V_{IN} = 5 V_{PP} at 10 kHz		0.5		LSB
DIGITAL-TO-ANALOG CONVERTER(2)					
Output voltage range	Programmable	0		$2 \times V_{REF}$	V
Output current	Refer to Typical Characteristics		±1		mA
Resolution				12	Bits
Integral linearity(3)			±2	±8	LSB
Monotonicity		12			Bits
Differential linearity			±0.2	±1	LSB
Offset error	Output range = 0 to V_{REF}		±0.5	±5	mV
	Output range = 0 to 2 x V_{REF}		±1	±10	mV
Offset error drift			±4		ppmFS/°C
Gain error	Output range = 0 to 2 x V_{REF}		±0.3	±1.0	%FS
Settling time	Step between code 0x400 to 0xC00, to ±1 LSB		2		µs
Code change glitch	1 LSB change, in worst case		20		nV-s
Overshoot	Step between code 0x400 to 0xC00		200		mV
Crosstalk	Step between code 0x400 to 0xC00		< 0.5		LSB
Signal-to-noise ratio	Sine wave (1 kHz, 5 V_{PP}) generated by DAC, sampling at 400 kSPS, R_L = 10 kΩ, C_L = 100 pF.		74		dB
Output noise voltage density	Output buffer gain = 2		60		nV/√Hz
	Output buffer gain = 1		30		nV/√Hz

(1) LSB means least significant bit.
(2) DAC is tested with load of 25 kΩ in parallel with 100 pF to ground.
(3) Measured from code 0x008 to 0xFFF.

ELECTRICAL CHARACTERISTICS: +5 V (continued)

At –40°C to +85°C, AV_{DD} = 5 V, DV_{DD} = 5 V, BV_{DD} = 3 V to 5 V, using external 2.5-V reference (unless otherwise noted).

PARAMETER		CONDITIONS	AMC7823 MIN	AMC7823 TYP	AMC7823 MAX	UNITS
PRECISION CURRENT SOURCE						
Output current range			0.01		10	mA
Output current accuracy		I_{out} = 100 µA	99.5	100.0	100.5	µA
Output current drift		I_{out} = 100 µA		40		ppm/°C
Output impedance		I_{out} = 100 µA		100		MΩ
Compliance voltage of pin PRECISION_I_OUTPUT		I_{out} = 10 mA	3	4.25		V
Power-supply rejection ratio				60		dB
VOLTAGE REFERENCE (V_{REF})						
Internal reference voltage(4)		At 25°C	2.495	2.50	2.505	V
Internal reference drift		–40°C to 85°C		±15		ppm/°C
Output impedance of pin EXT_REF_IN as internal reference output				10		kΩ
Short-circuit current				250		µA
External reference voltage			1.20		2.55	V
External reference input resistance		Internal reference selected		10		kΩ
		Internal reference de-selected		1		MΩ
External reference input capacitance				5		pF
TEMPERATURE SENSOR						
Temperature range			–40		85	°C
Resolution		V_{REF} = 2.5 V		3.2		°C
		V_{REF} = 1.25 V		1.6		°C
Accuracy		V_{REF} = 2.5 V		±4		°C
		V_{REF} = 1.25 V		±2.0		°C
LEVEL OF PIN $\overline{GALR}$ AND $\overline{DAV}$						
	I_{OH} = 0.7 mA		4		DV_{DD}	V
	I_{OL} = 180 µA		0		0.4	V
DIGITAL INPUT/OUTPUT, EXCEPT PIN $\overline{GALR}$ AND $\overline{DAV}$						
V_{IH}	Logic level	BV_{DD} = 5 V, I_{IH} = 5 µA	3.5		BV_{DD} + 0.3	V
V_{IL}		BV_{DD} = 5 V, I_{IL} = –5 µA	0		0.8	V
V_{OH}		BV_{DD} = 5 V, I_{OH} = –3 mA	4		BV_{DD}	V
V_{OL}		BV_{DD} = 5 V, $_{OL}$ = 3 mA	0		0.4	V
V_{IH}	Logic level	BV_{DD} = 3 V, I_{IH} = 5 µA	2.1		BV_{DD} + 0.3	V
V_{IL}		BV_{DD} = 3 V, I_{IL} = –5 µA	0		0.6	V
V_{OH}		BV_{DD} = 3 V, I_{OH} = –3 mA	2.4		BV_{DD}	V
V_{IL}		BV_{DD} = 3 V, I_{OL} = 3 mA	0		0.4	V
Input capacitance				5		pF

(4) Bit GREF in AMC Status/Configuration Register determines the internal reference voltage. The internal V_{REF} = 2.5 V when GREF = 1, and the internal V_{REF} = 1.25 V when GREF = 0 (see AMC Status/Configuration Register for details).

ELECTRICAL CHARACTERISTICS: +5 V (continued)

At –40°C to +85°C, AV_{DD} = 5 V, DV_{DD} = 5 V, BV_{DD} = 3 V to 5 V, using external 2.5-V reference (unless otherwise noted).

PARAMETER	CONDITIONS	AMC7823			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Power-supply voltage					
AV_{DD}	Specified performance	2.7	5	5.5	V
DV_{DD} (5)	Specified performance	2.7		5.5	V
BV_{DD} (6)	Specified performance	2.7		5.5	V
Quiescent current of AV_{DD}	In normal operation, precision current source = 0, no DAC load.		15	20	mA
	All power-down		1		
Quiescent current of DV_{DD}			0.3		mA
Quiescent current of BV_{DD}			0.1		mA
Power dissipation			100		mW
TEMPERATURE RANGE					
Specified performance		–40		+85	°C
Storage		–65		+150	°C

(5) DV_{DD} must equal AV_{DD}.
(6) BV_{DD} must not be greater than AV_{DD} or DV_{DD}.

ELECTRICAL CHARACTERISTICS: +3 V

At –40°C to +85°C, AV_{DD}, DV_{DD}, BV_{DD} = 3 V, using external 1.25-V reference (unless otherwise noted).

PARAMETER	CONDITIONS	AMC7823 MIN	AMC7823 TYP	AMC7823 MAX	UNITS
ADC ANALOG INPUTS					
Input voltage range		0		$2 \times V_{REF}$	V
Input impedance			5		MΩ
Input capacitance			15		pF
Input leakage current			±1		µA
ANALOG-TO-DIGITAL CONVERTER					
Resolution				12	Bits
No missing codes		12			Bits
Integral linearity				±1	LSB(1)
Differential linearity				±1	LSB
Offset error				±3	LSB
Offset error drift			±4		ppmFS/°C
Offset error match			0.5	1	LSB
Gain error				±12	LSB
Gain error match			0.3	1.5	LSB
Noise			70		μV_{RMS}
Power-supply rejection	AV_{DD} = 3 V ±5%		70		dB
Throughput rate			200		kHz
Total conversion time	Scan Channels 0 through 7		47		µs
Total conversion time including temperature	Scan Channels 0 through 8		58		µs
Channel-to-channel isolation	V_{IN} = 2.5 V_{PP} at 10 kHz		0.5		LSB
DIGITAL-TO-ANALOG CONVERTER(2)					
Output voltage range	Programmable	0		$2 \times V_{REF}$	V
Output current	Refer to Typical Characteristics		±1		mA
Resolution				12	Bits
Integral linearity(3)			±2	±8	LSB
Monotonicity		12			Bits
Differential linearity			±0.2	±1	LSB
Offset error	Output range = 0 to V_{REF}		±0.5	±5	mV
	Output range = 0 to 2 x V_{REF}		±1	±10	mV
Offset error drift			±4		ppmFS/°C
Gain error	Output range = 0 to 2 x V_{REF}		±0.2	±1.0	%FS
Settling time	Step between code 0x400 to 0xC00, to ±1 LSB		2		µs
Code change glitch	1 LSB change, in worst case		20		nV-s
Overshoot	Step between code 0x400 to 0xC00		200		mV
Crosstalk	Step between code 0x400 to 0xC00		<0.5		LSB
Signal-to-noise ratio	Sine wave (1 kHz, 5 V_{PP}) generated by DAC, sampling at 400 kSPS, R_L = 10 kΩ, C_L = 100 pF		74		dB
Output noise voltage density	Output buffer gain = 2		60		nV/√Hz
	Output buffer gain = 1		30		nV/√Hz

(1) LSB means least significant bit.
(2) DAC is tested with load of 25 kΩ in parallel with 100 pF to ground.
(3) Measured from code 0x008 to 0xFFF.

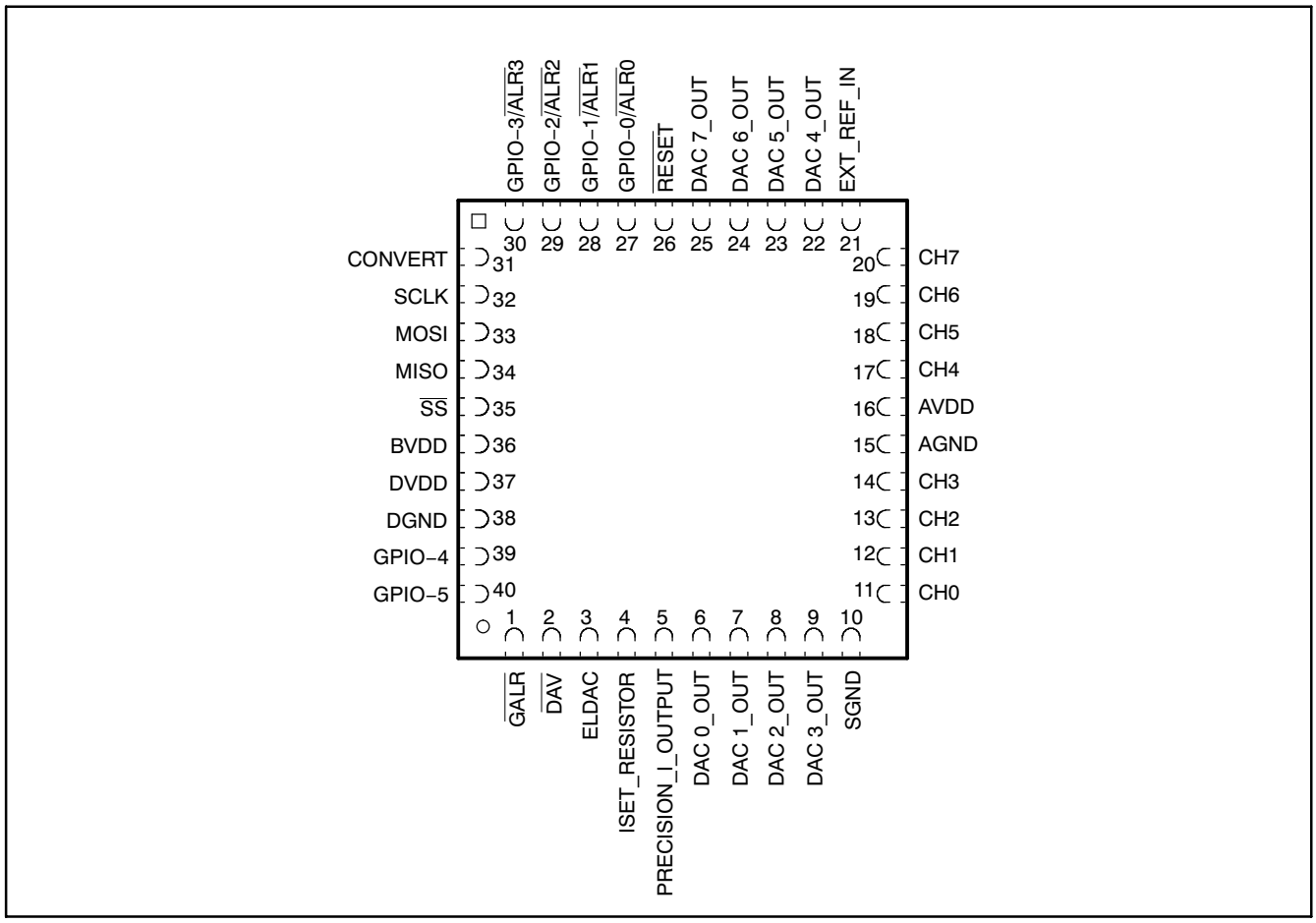
ELECTRICAL CHARACTERISTICS: +3 V (continued)

At –40°C to +85°C, AV_{DD}, DV_{DD}, BV_{DD} = 3 V, using external 1.25-V reference (unless otherwise noted).

PARAMETER	CONDITIONS	AMC7823			UNITS
		MIN	TYP	MAX	
PRECISION CURRENT SOURCE					
Output current range		0.01		10	mA
Output current accuracy	I_{out} = 100 µA	99.5	100.0	100.5	µA
Output current drift	I_{out} = 100 µA		40		ppm/°C
Output impedance	I_{out} = 100 µA		100		MΩ
Compliance voltage of pin PRECISION_I_OUTPUT	AV_{DD} = 2.7 V, I_{out} = 10 mA	1.9	2		V
Power-supply rejection ratio			60		dB
VOLTAGE REFERENCE (V_{REF})					
Internal reference voltage(4)	At 25°C	1.247	1.25	1.253	V
Internal reference drift	–40°C to 85°C		±20		ppm/°C
Output impedance of pin EXT_REF_IN as internal reference output			10		kΩ
Short-circuit current			125		µA
External reference voltage		1.20		1.28	V
External reference input resistance			10		kΩ
External reference input capacitance			5		pF
TEMPERATURE SENSOR					
Temperature range		–40		85	°C
Resolution			1.6		°C
Accuracy			±2.0		°C
LEVEL OF PIN $\overline{GALR}$ AND $\overline{DAV}$					
I_{OH} = 0.3 mA		2.4		DV_{DD}	V
I_{OL} = 125 µA		0		0.4	V
DIGITAL INPUT/OUTPUT, EXCEPT PIN $\overline{GLAR}$ AND $\overline{DAV}$					
V_{IH}	Logic level	I_{IH} = 5 µA	2.1		BV_{DD} + 0.3	V
V_{IL}		I_{IL} = –5 µA	0		0.6	V
V_{OH}		I_{OH} = –3 mA	2.4		BV_{DD}	V
V_{OL}		I_{OL} = 3 mA	0		0.4	V
Input capacitance				5		pF
POWER SUPPLY REQUIREMENTS					
Power-supply voltage					
AV_{DD}	Specified performance	2.70	3	3.3	V
DV_{DD}	Specified performance	2.70		3.3	V
BV_{DD}(5)	Specified performance	2.70		3.3	V
Quiescent current of AV_{DD}	In normal operation		10	15	mA
	All power-down		1		mA
Quiescent current of DV_{DD}			0.3		mA
Quiescent current of BV_{DD}			0.1		mA
Power dissipation			60		mW
TEMPERATURE RANGE					
Specified performance		–40		+85	°C
Storage		–65		+150	°C

(4) Bit GREF in AMC Status/Configuration Register determines the internal reference voltage. GREF must be cleared when AV_{DD} is less than 5 V and the internal reference is selected (see AMC Status/Configuration Register for details).
(5) BV_{DD} must be not greater than AV_{DD} or DV_{DD}.

PIN CONFIGURATION
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	$\overline{\text{GALR}}$	Global analog input out-of-range alarm. $\overline{\text{GALR}}$ pin goes low (active) when one (or more) of the first four accessed analog inputs is out of preset range.
2	$\overline{\text{DAV}}$	Data available indicator. In the direct mode, $\overline{\text{DAV}}$ pin goes low (active) when the conversion finishes. In Auto-mode, a 2-µs pulse (active low) appears on this pin when conversion cycle finishes (see ADC Operation and Registers for details). $\overline{\text{DAV}}$ stays high when deactivated.
3	ELDAC	External DAC synchronous load trigger. DACs that have external synchronous load selected are updated simultaneously by the rising edge of ELDAC.
4	ISET_RESISTOR	The resistor connected from analog supply to this pin sets the current output from the pin PRECISION_I_OUTPUT.
5	PRECISION_I_OUTPUT	Current output to drive a thermistor.
6	DAC-0_OUT	Output of DAC-0
7	DAC-1_OUT	Output of DAC-1
8	DAC-2_OUT	Output of DAC-2
9	DAC-3_OUT	Output of DAC-3
10	SGND	Analog input signal ground. This pin must connect to the ground of analog input source to minimize the digital noise.
11	CH0	Analog input channel 0

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NO.	NAME	
12	CH1	Analog input channel 1
13	CH2	Analog input channel 2
14	CH3	Analog input channel 3
15	AGND	Analog ground
16	AVDD	Analog power supply, +3 V to +5 V. Must be the same value as DVDD.
17	CH4	Analog input channel 4
18	CH5	Analog input channel 5
19	CH6	Analog input channel 6
20	CH7	Analog input channel 7
21	EXT_REF_IN	When external reference connects here, the internal reference is overridden. When internal reference is selected, this pin works as output of the internal reference (with 10-kΩ output impedance). See Reference section for details.
22	DAC-4_OUT	Output of DAC-4
23	DAC-5_OUT	Output of DAC-5
24	DAC-6_OUT	Output of DAC-6
25	DAC-7_OUT	Output of DAC-7
26	$\overline{\text{RESET}}$	Reset input. Logic low on this pin causes the part to perform hardware reset.
27	GPIO-0/$\overline{\text{ALR}}$0	Multiple function I/O pin. Works as digital I/O or $\overline{\text{ALR}}$ pin of the first analog input.
28	GPIO-1/$\overline{\text{ALR}}$1	Multiple function I/O pin. Works as digital I/O or $\overline{\text{ALR}}$ pin of the second analog input.
29	GPIO-2/$\overline{\text{ALR}}$2	Multiple function I/O pin. Works as digital I/O or $\overline{\text{ALR}}$ pin of the third analog input.
30	GPIO-3/$\overline{\text{ALR}}$3	Multiple function I/O pin. Works as digital I/O or $\overline{\text{ALR}}$ pin of the fourth analog input.
31	CONVERT	External conversion trigger. The rising edge starts sampling and conversion of the ADC when external trigger mode is selected.
32	SCLK	Serial clock input
33	MOSI	Master out, slave in. Digital data input for the serial interface
34	MISO	Master in, slave out. Digital data output for the serial interface
35	$\overline{\text{SS}}$	Slave select input (active low). Data is not clocked into MOSI unless $\overline{\text{SS}}$ is low. When $\overline{\text{SS}}$ is high, MISO is in high-impedance status.
36	BVDD	Interface power supply. Connects to 3 V for 3-V logic; connects to 5 V for 5-V logic.
37	DVDD	Digital power supply (+3 V to +5 V). Must be the same value as AVDD.
38	DGND	Digital ground
39	GPIO4	General-purpose digital I/O pin
40	GPIO5	General-purpose digital I/O pin

TIMING CHARACTERISTICS: +5 V

At –40°C to +85°C, AV_{DD} = DV_{DD} = 5 V (unless otherwise noted).

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	42		ns
t_{wsck}	SCLK high or low time	21		ns
t_{Lead}	$\overline{SS}$ enable lead time	21		ns
t_{Lag}	$\overline{SS}$ enable lag time	21		ns
t_{td}	Sequential transfer delay	42		ns
t_{su}	Data setup time	0		ns
t_{hi}	Data hold time (inputs)	21		ns
t_{ho}	Data hold time (outputs)	0		ns
t_A	Slave access time		21	ns
t_{dis}	Slave MISO disable time		21	ns
t_v	Data valid		10	ns
t_r	Rise time		30	ns
t_f	Fall time		30	ns
t_{WLDAC}	ELDAC width	210		ns
$t_{CONVERT}$	CONVERT width	210		ns

TIMING CHARACTERISTICS: +3 V

At –40°C to +85°C, AV_{DD} = DV_{DD} = 3 V (unless otherwise noted).

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	84		ns
t_{wsck}	SCLK high or low time	42		ns
t_{Lead}	$\overline{SS}$ enable lead time	42		ns
t_{Lag}	$\overline{SS}$ enable lag time	42		ns
t_{td}	Sequential transfer delay	84		ns
t_{su}	Data setup time	0		ns
t_{hi}	Data hold time (inputs)	42		ns
t_{ho}	Data hold time (outputs)	0		ns
t_A	Slave access time		42	ns
t_{dis}	Slave MISO disable time		42	ns
t_v	Data valid		10	ns
t_r	Rise time		30	ns
t_f	Fall time		30	ns
t_{WLDAC}	ELDAC width	420		ns
$t_{CONVERT}$	CONVERT width	420		ns

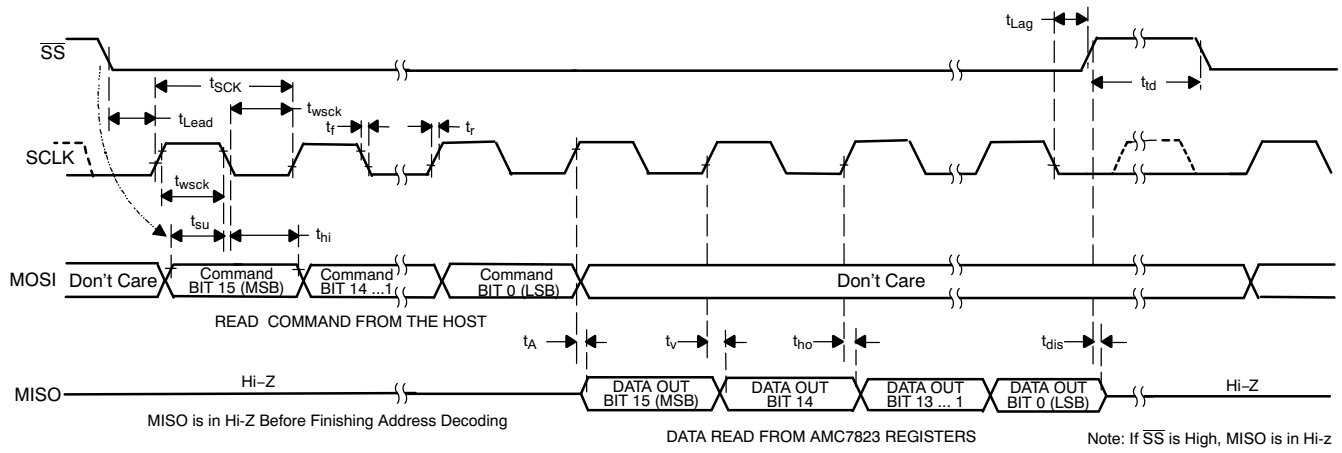


Figure 1. Read Operation (SPI)

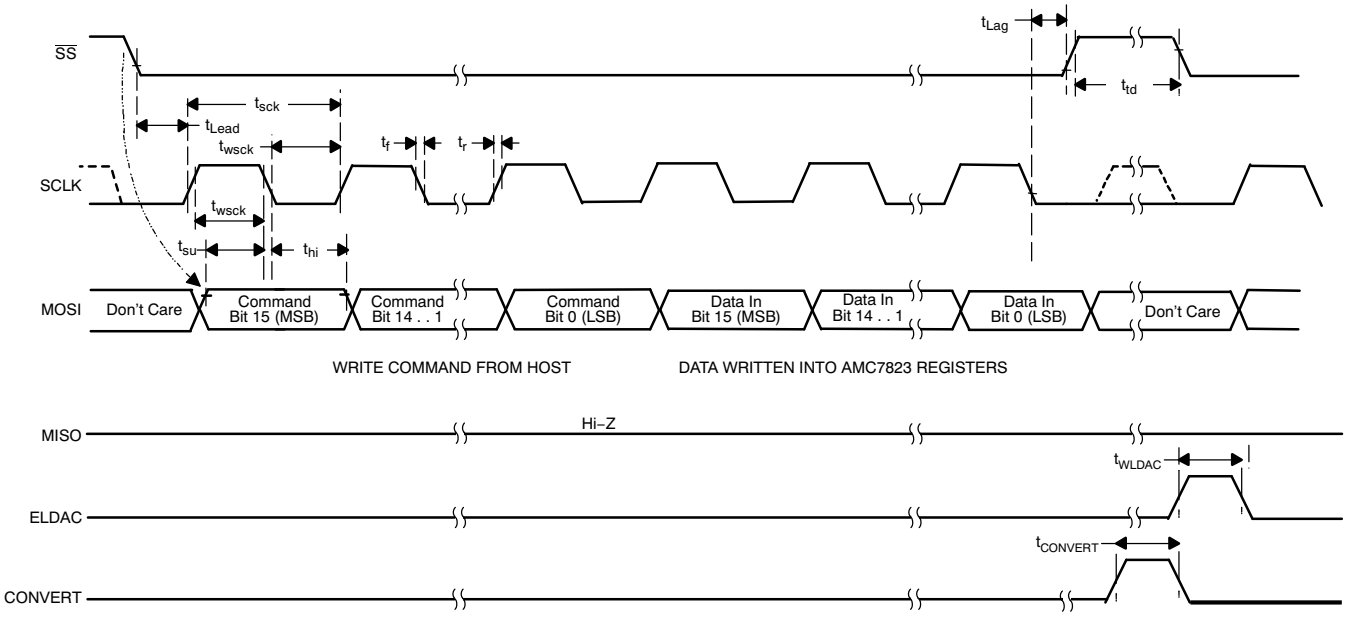


Figure 2. Write Operation (SPI)

TYPICAL CHARACTERISTICS: ANALOG-TO-DIGITAL CONVERTER (ADC)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

LINEARITY ERROR vs CODE
(–40°C, AV_{DD} = 5V, V_{REF} = 2.5V)

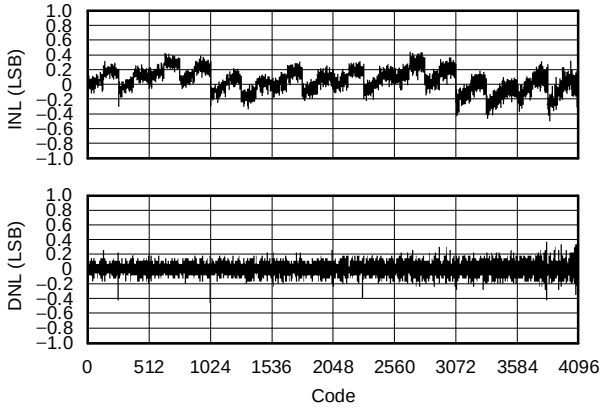


Figure 3.

LINEARITY ERROR vs CODE
(–40°C, AV_{DD} = 2.7V, V_{REF} = 1.25V)

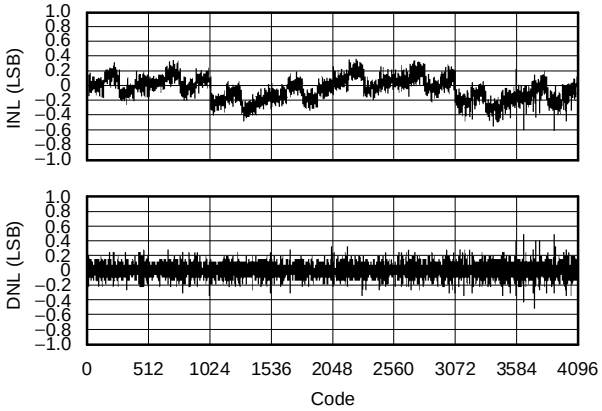


Figure 4.

LINEARITY ERROR vs CODE
(+25°C, AV_{DD} = 5V, V_{REF} = 2.5V)

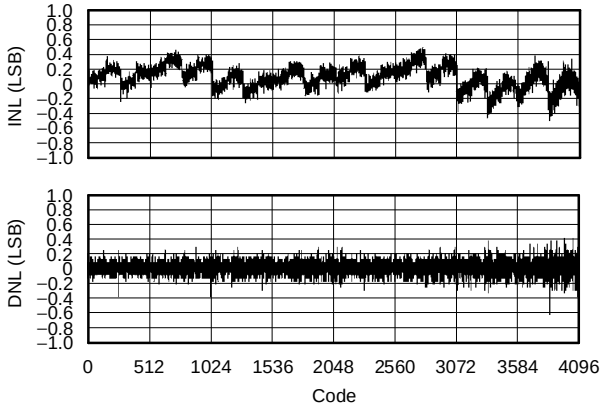


Figure 5.

LINEARITY ERROR vs CODE
(+25°C, AV_{DD} = 2.7V, V_{REF} = 1.25V)

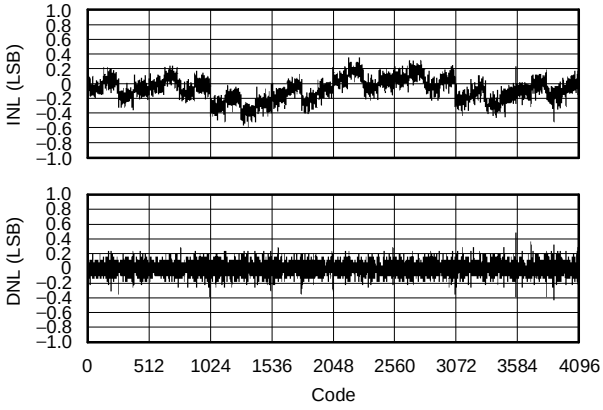


Figure 6.

LINEARITY ERROR vs CODE
(+85°C, AV_{DD} = 5V, V_{REF} = 2.5V)

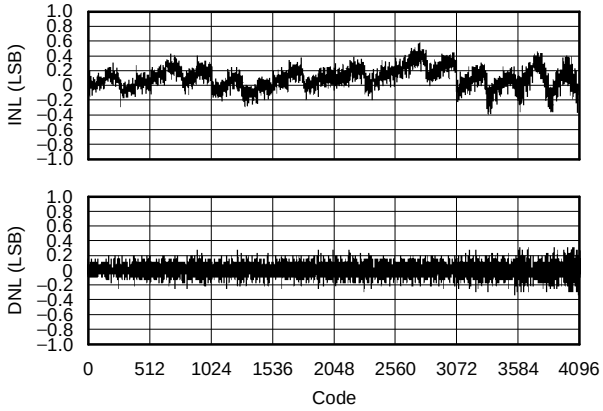


Figure 7.

LINEARITY ERROR vs CODE
(+85°C, AV_{DD} = 2.7V, V_{REF} = 1.25V)

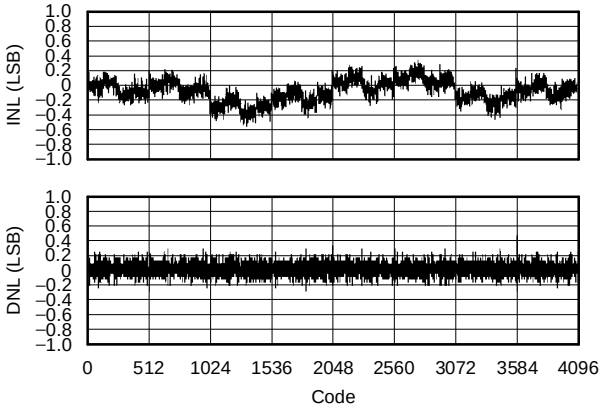


Figure 8.

TYPICAL CHARACTERISTICS: ANALOG-TO-DIGITAL CONVERTER (ADC) (continued)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

OFFSET ERROR AND OFFSET ERROR MATCH vs TEMPERATURE

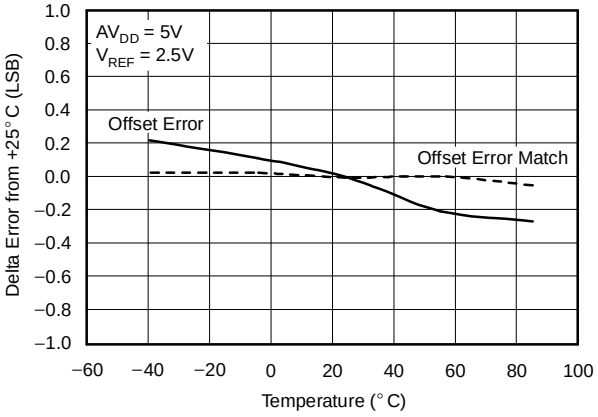


Figure 9.

GAIN ERROR AND GAIN ERROR MATCH vs TEMPERATURE

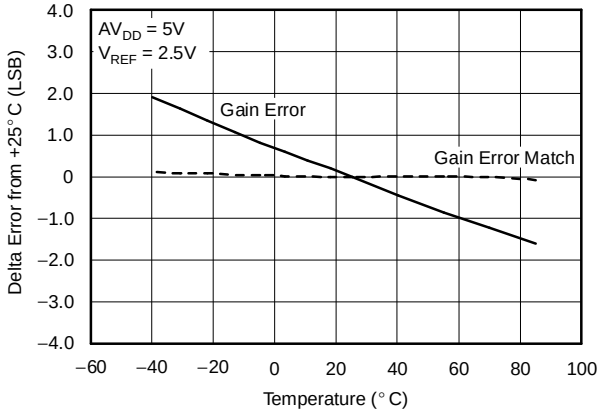


Figure 10.

OFFSET ERROR AND OFFSET ERROR MATCH vs TEMPERATURE

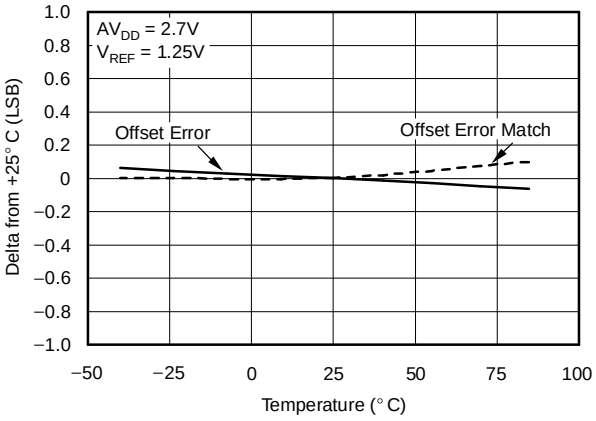


Figure 11.

GAIN ERROR AND GAIN ERROR MATCH vs TEMPERATURE

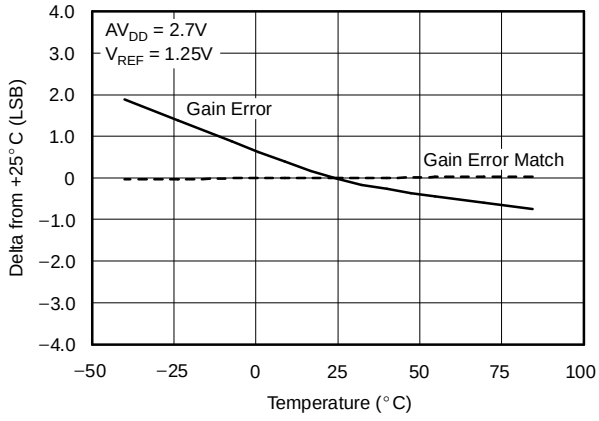


Figure 12.

GAIN AND OFFSET ERROR vs 5V SUPPLY

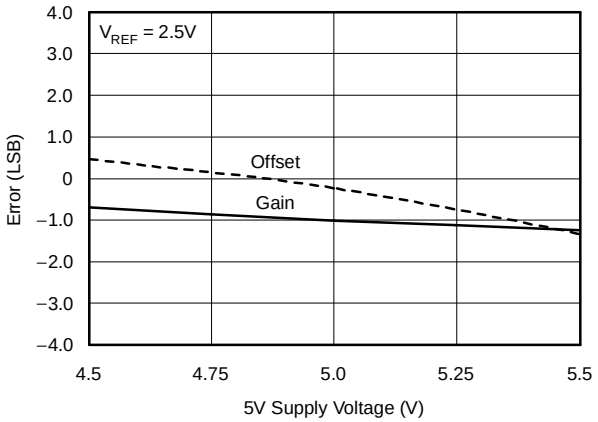


Figure 13.

GAIN AND OFFSET ERROR MATCH vs 5V SUPPLY

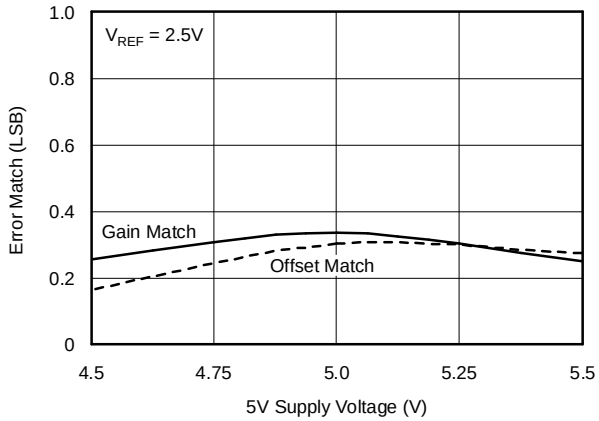


Figure 14.

TYPICAL CHARACTERISTICS: ANALOG-TO-DIGITAL CONVERTER (ADC) (continued)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

GAIN AND OFFSET ERROR vs 3V SUPPLY

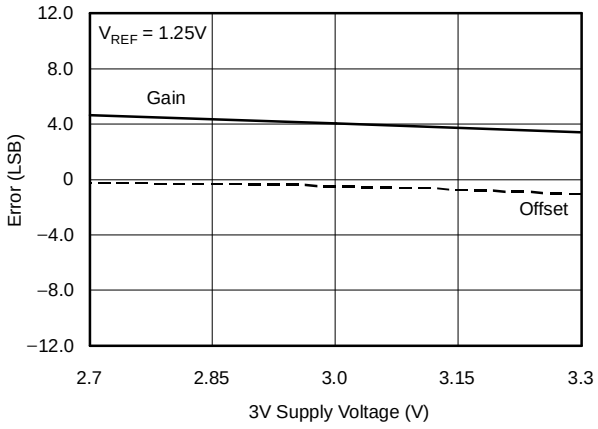


Figure 15.

GAIN AND OFFSET ERROR MATCH vs 3V SUPPLY

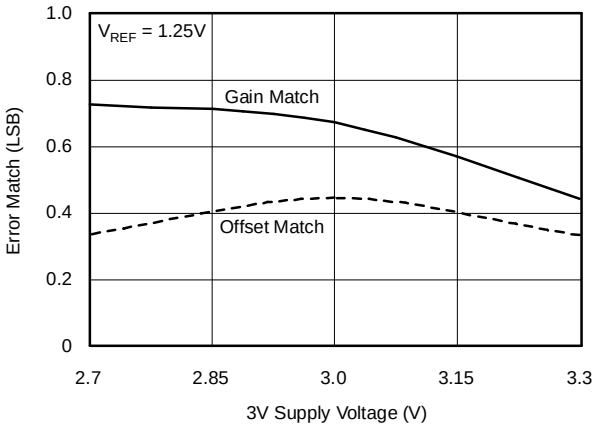


Figure 16.

INTERNAL REFERENCES vs AV_{DD} VOLTAGE

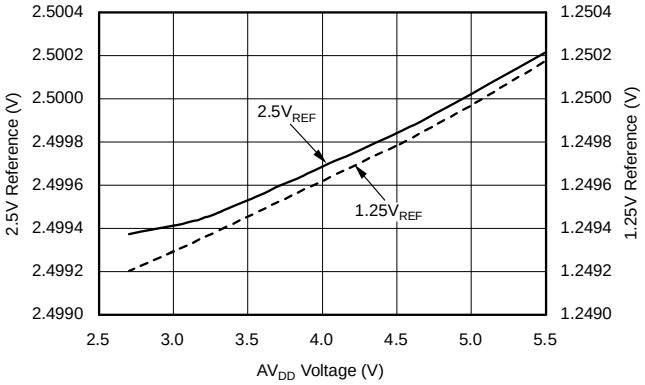


Figure 17.

2.5V AND 1.25V INTERNAL REFERENCES vs TEMPERATURE

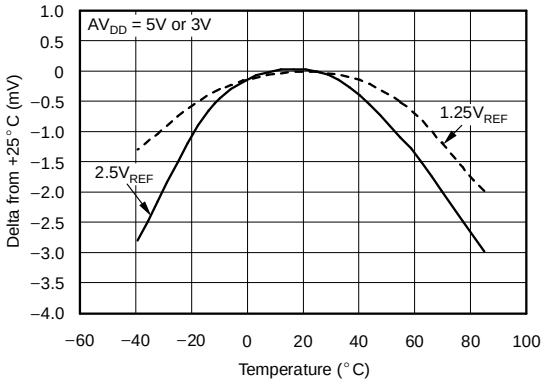


Figure 18.

INTERNAL 2.5V REFERENCE (AV_{DD} = 5V)

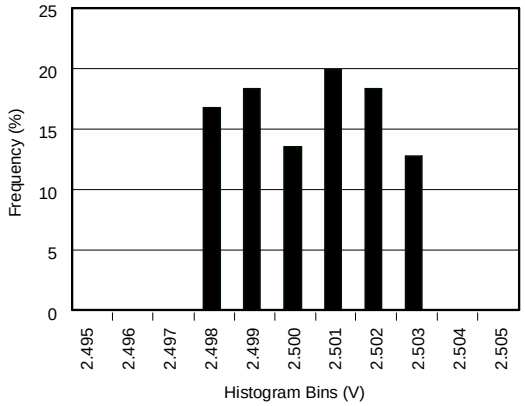


Figure 19.

INTERNAL 1.25V REFERENCE (AV_{DD} = 2.7V)

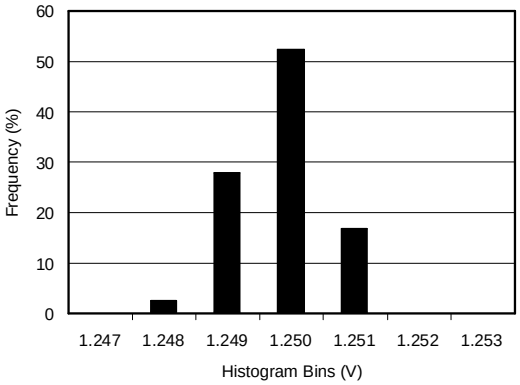


Figure 20.

TYPICAL CHARACTERISTICS: DIGITAL-TO-ANALOG CONVERTER (DAC)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

LINEARITY ERROR vs CODE
(–40°C, AV_{DD} = 5V, V_{REF} = 2.5V, GAIN = 1)

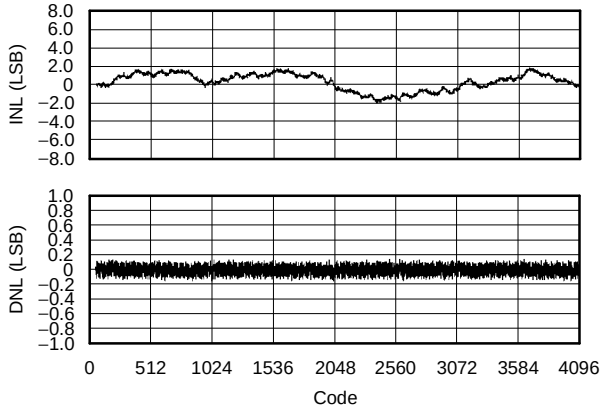


Figure 21.

LINEARITY ERROR vs CODE
(–40°C, AV_{DD} = 2.7V, V_{REF} = 1.25V, GAIN = 1)

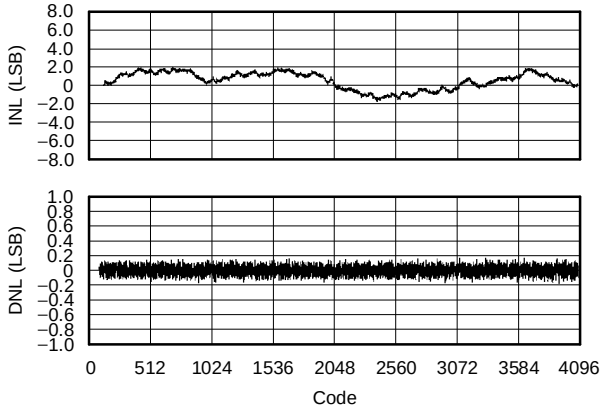


Figure 22.

LINEARITY ERROR vs CODE
(+25°C, AV_{DD} = 5V, V_{REF} = 2.5V, GAIN = 1)

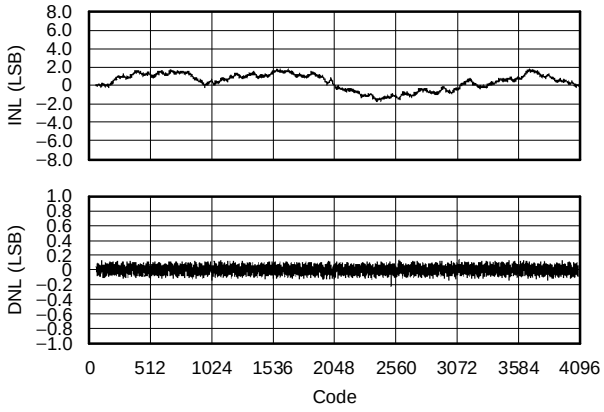


Figure 23.

LINEARITY ERROR vs CODE
(+25°C, AV_{DD} = 2.7V, V_{REF} = 1.25V, GAIN = 1)

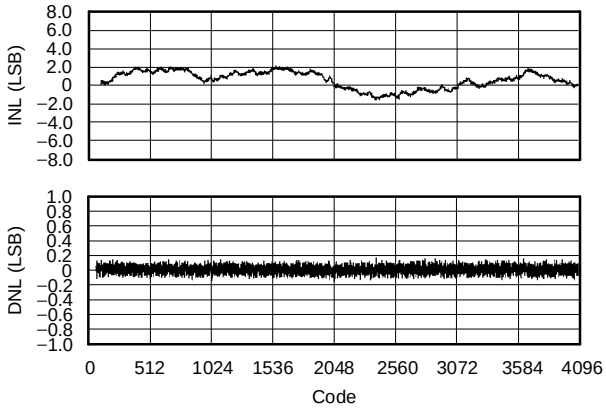


Figure 24.

LINEARITY ERROR vs CODE
(+85°C, AV_{DD} = 5V, V_{REF} = 2.5V, GAIN = 1)

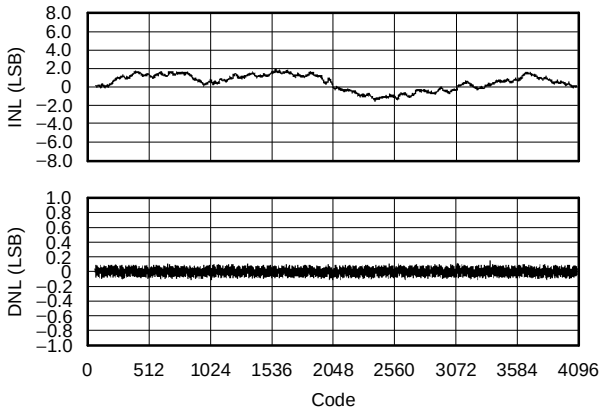


Figure 25.

LINEARITY ERROR vs CODE
(+85°C, AV_{DD} = 2.7V, V_{REF} = 1.25V, GAIN = 1)

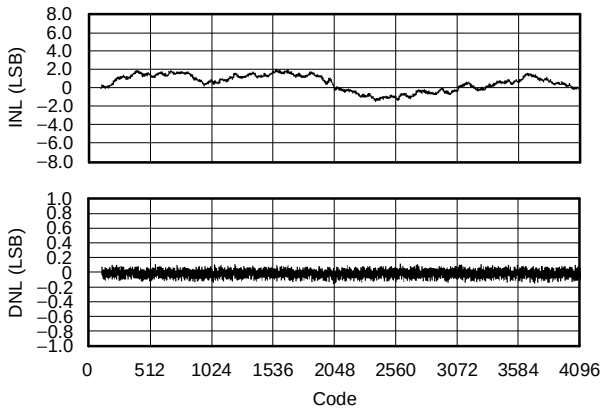


Figure 26.

TYPICAL CHARACTERISTICS: DIGITAL-TO-ANALOG CONVERTER (DAC) (continued)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

NORMALIZED OFFSET ERROR vs TEMPERATURE

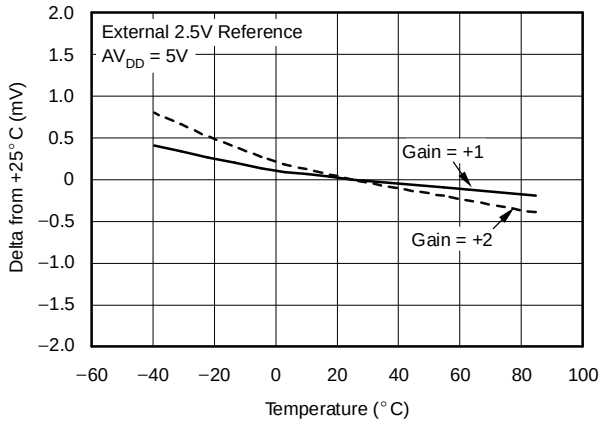


Figure 27.

NORMALIZED GAIN ERROR vs TEMPERATURE

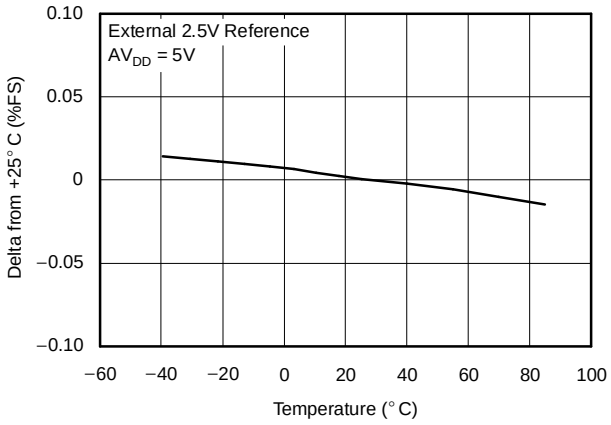


Figure 28.

V_{OUT} vs SOURCING AND SINKING CURRENT

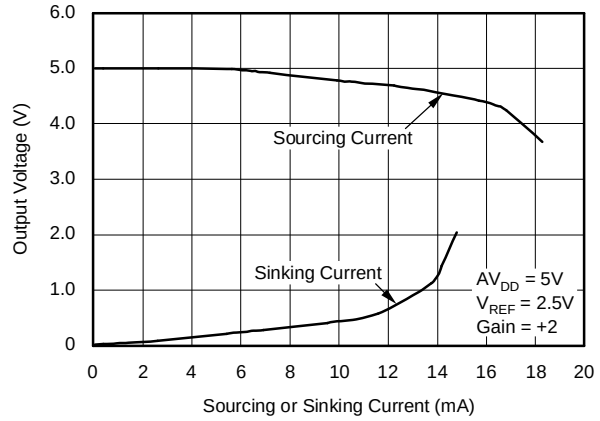


Figure 29.

V_{OUT} vs SOURCING AND SINKING CURRENT

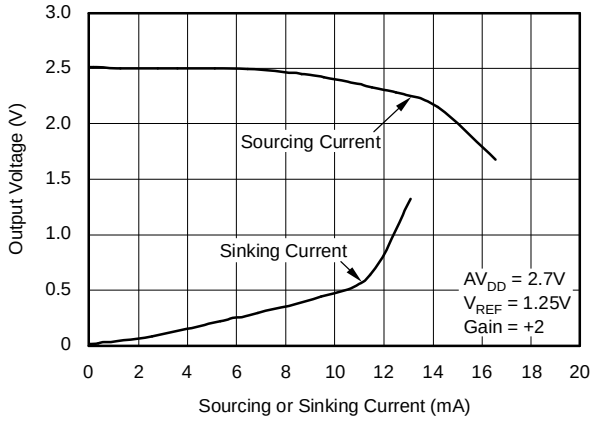


Figure 30.

DAC SETTLING TIME (GAIN = +2)

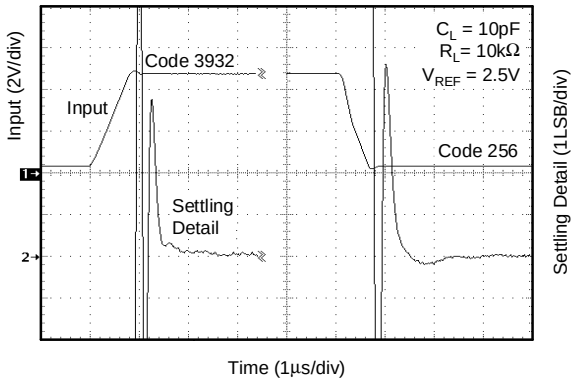


Figure 31.

DAC SETTLING TIME (GAIN = +1)

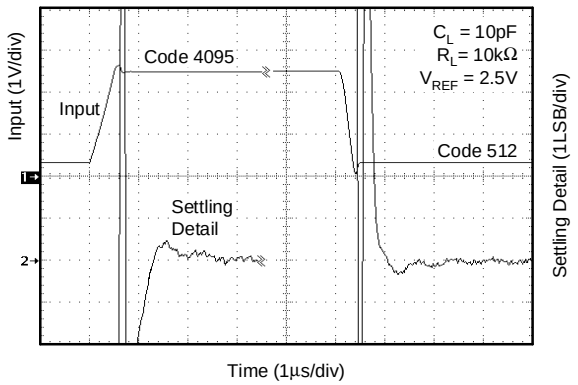


Figure 32.

TYPICAL CHARACTERISTICS: DIGITAL-TO-ANALOG CONVERTER (DAC) (continued)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

DAC POWER-ON RESET TO 0V

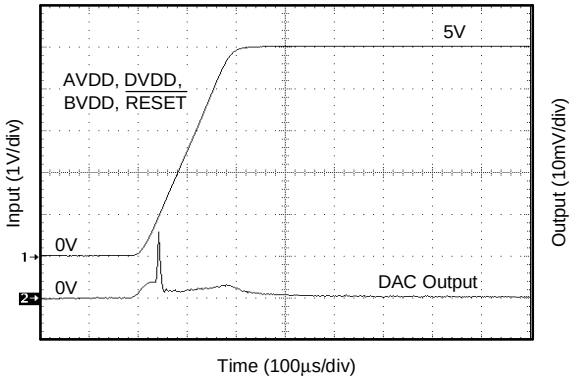


Figure 33.

TYPICAL CHARACTERISTICS: PRECISION CURRENT SOURCE

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

100µA CURRENT SOURCE vs TEMPERATURE

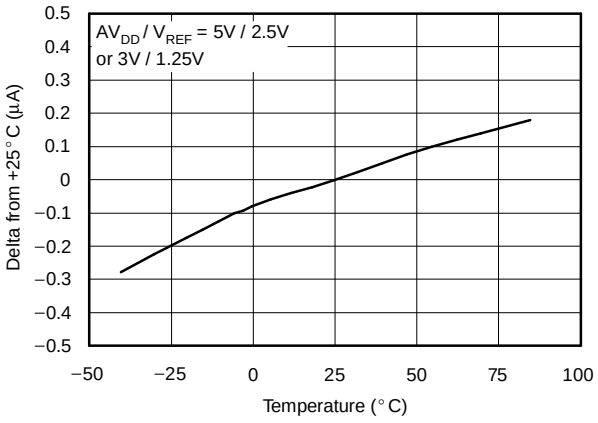


Figure 34.

PRECISION_I_OUTPUT vs COMPLIANCE VOLTAGE

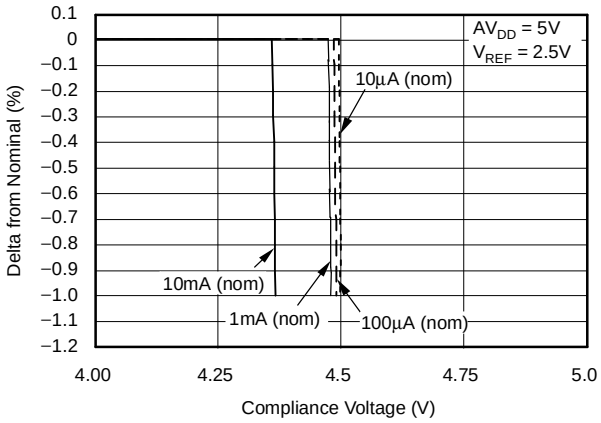


Figure 35.

TYPICAL CHARACTERISTICS: PRECISION CURRENT SOURCE (continued)

At +25°C, AV_{DD} = DV_{DD} = 5V, unless otherwise noted.

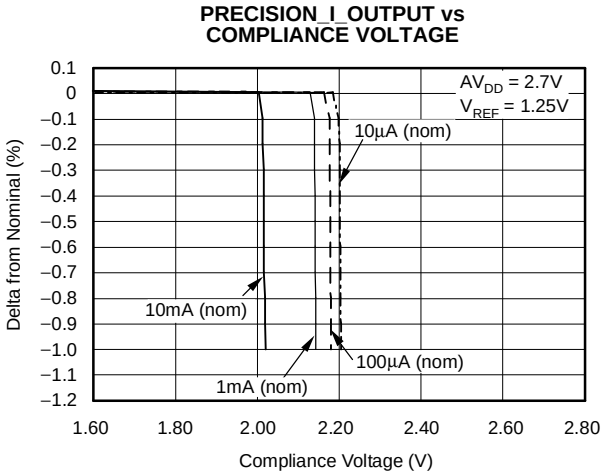


Figure 36.

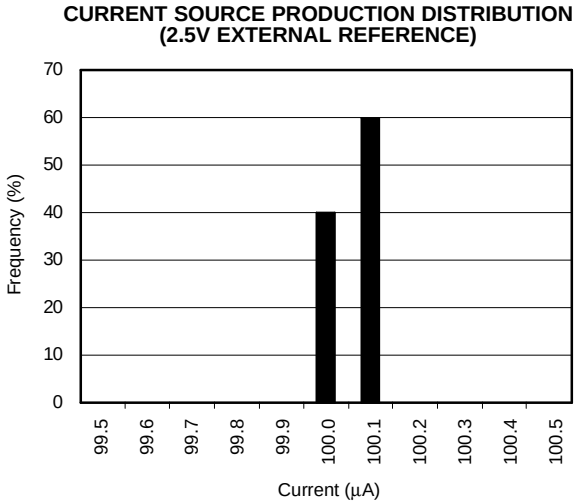


Figure 37.

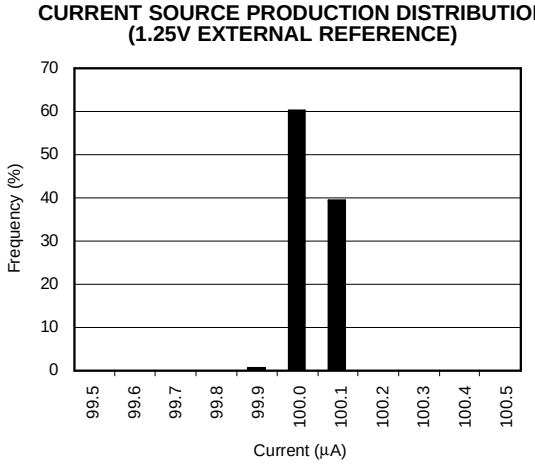


Figure 38.

APPLICATION INFORMATION

DIGITAL INTERFACE

The AMC7823 communicates through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. SPI slave devices, such as the AMC7823, depend on a master to start and synchronize transmissions.

A transmission begins when initiated by an SPI master. A word from the master is shifted into the AMC7823 through the MOSI pin under the control of the master serial clock, SCLK. A word from an AMC7823 register is shifted out from the MISO pin under the control of SCLK as well.

The idle state of the serial clock for the AMC7823 is low, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The AMC7823 interface is designed with a clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). In both the master and slave, the data is shifted out on the rising edge of SCLK and sampled on the falling edge of SCLK where data is stable. The master begins driving the MOSI pin on the first rising edge of SCLK after $\overline{SS}$ is activated (low).

To write data into AMC7823, the host activates the slave select signal ($\overline{SS}$ = low) and issues a WRITE command to start the data transmission. The AMC7823 always interprets the first word (from the host) immediately following the falling edge of $\overline{SS}$ signal as a command. The data to be written into the AMC7823 follow the command. The slave select pin ($\overline{SS}$) must remain low until all data are transmitted (see Figure 39). Otherwise, the WRITE operation is terminated. Likewise, to read data from AMC7823, the host activates the slave select signal and sends a READ command. The AMC7823 then sends data out through the MISO pin under the control of SCLK. The slave select pin must remain low until all data are shifted out (see Figure 39). Otherwise, the transmission is terminated, and all remaining data (if any) are ignored.

When the operation is terminated, the master must issue a new command to start a new operation.

All registers in the AMC7823 are 16-bit. It takes 16 clock pulses of SCLK to transfer one data or command word. All data are transferred into (or out of) the AMC7823 through an internal serial-parallel (parallel-serial) register. If $\overline{SS}$ is deactivated (that is, goes high) before the 16th clock finishes, the incomplete transfer is terminated immediately and the data being transferred are ignored. In a write operation, this data is not written into the AMC7823 register. In a read operation, the remaining data bits are not shifted out, and the data must be ignored.

AMC7823 COMMUNICATION PROTOCOL

With the exception of two external trigger pins, an external $\overline{RESET}$ pin, and an external current setting resistor, the AMC7823 is entirely controlled by registers. Reading from and writing to these registers is accomplished by issuing a 16-bit command word followed immediately by data for a single register or for a range of registers. This command word is constructed as shown in the Bit Register. The data word(s) format for the target register(s) are illustrated in subsequent pages of this document.

Bit Register

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
R/$\overline{W}$	X	PG1	PG0	X	SADR4	SADR3	SADR2	SADR1	SADR0	X	EADR4	EADR3	EADR2	EADR1	EADR0

X : Don't Care

Where:

R/$\overline{W}$: Data flow direction bit.

R/$\overline{W}$ = 1. Read operation. Data is transferred from AMC7823 to the host.

R/$\overline{W}$ = 0. Write operation. Data is transferred from the host to AMC7823.

PG1 – PG0: Memory page of addressed register(s) (see Table 1).

SADR4 – SADR0: Starting address of register(s) on selected page.

EADR4 – EADR0: Ending address of register(s) on selected page.

NOTE: If the ending address is equal to or smaller than the starting address, only the starting address is accessed. In this case, the operation applies only to the starting address; all remaining data and memory locations (if any) are ignored. In this manner, a single register may be addressed by setting [EADR4:EADR0] = 00000 or [SADR4:SADR0] ≥ [EADR4:EADR0].

Table 1. Page Addressing

PG1	PG0	PAGE ADDRESS
0	0	0
0	1	1
1	0	**Reserved**
1	1	**Reserved**

For example, to read the register with address 0x00 on page 0, the host processor must send the AMC7823 the command 0x8000; this command specifies a read operation on page 0, address 0. After sending the command, the host reads one data word. To read the registers 0x02 to 0x07 on page 0 (ADC Data-2 to ADC Data-7), the host must send 0x8087 first, and then clock six data words sequentially out of the AMC7823. The first data word is from 0x02, the second from 0x03, and the sixth from 0x07. If the host continues clocking data out after reading the last location [EADR4:EADR0], the value 0x0000 is output until the operation stops. However, if the host deactivates $\overline{SS}$ before reading the last register, the operation is terminated and all remaining registers are ignored.

Likewise, to load data into the registers with addresses 0x03 to 0x05 on page 1 (DAC-3 Data Register to DAC-5 Data Register), the host sends command 0x10C5 followed sequentially by three data words. The first word is written into 0x03 of page 1, the second goes to 0x04, and the third goes to 0x05. If the host continues to transfer data into AMC7823 after writing the last location [EADR4:EADR0], all these data are ignored until the operation stops. However, if the host deactivates $\overline{SS}$ before writing the last location, the operation is terminated and all remaining locations are ignored.

See the AMC7823 Memory Map (Table 2) for details of register locations.

Figure 39 shows an example of a complete data transaction between the host processor and the AMC7823.

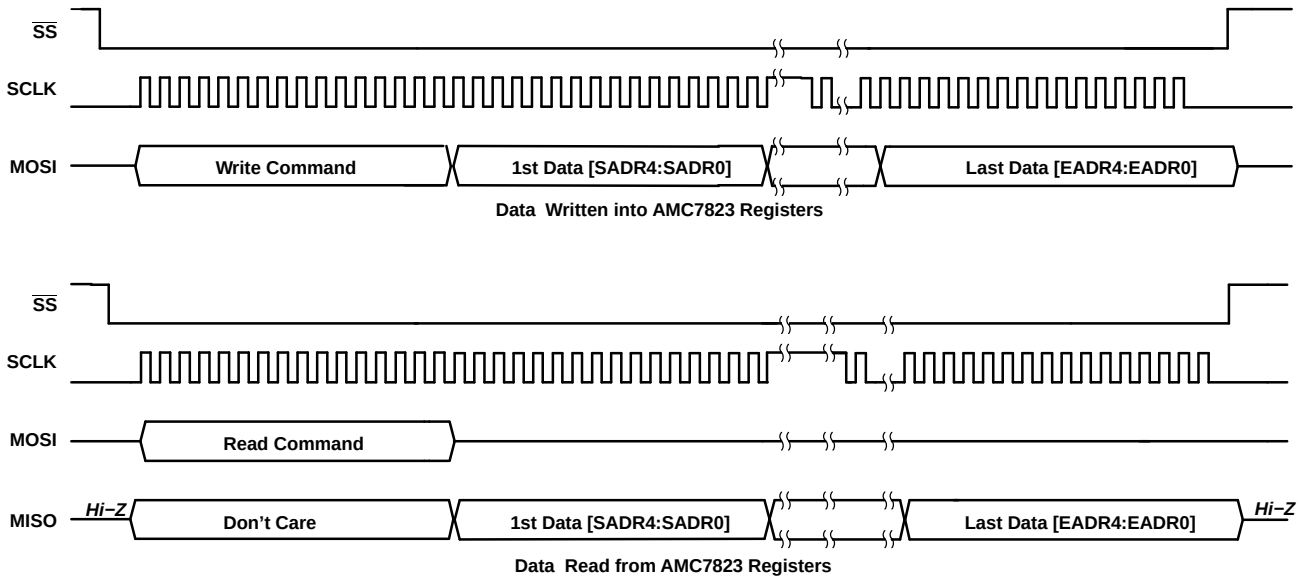


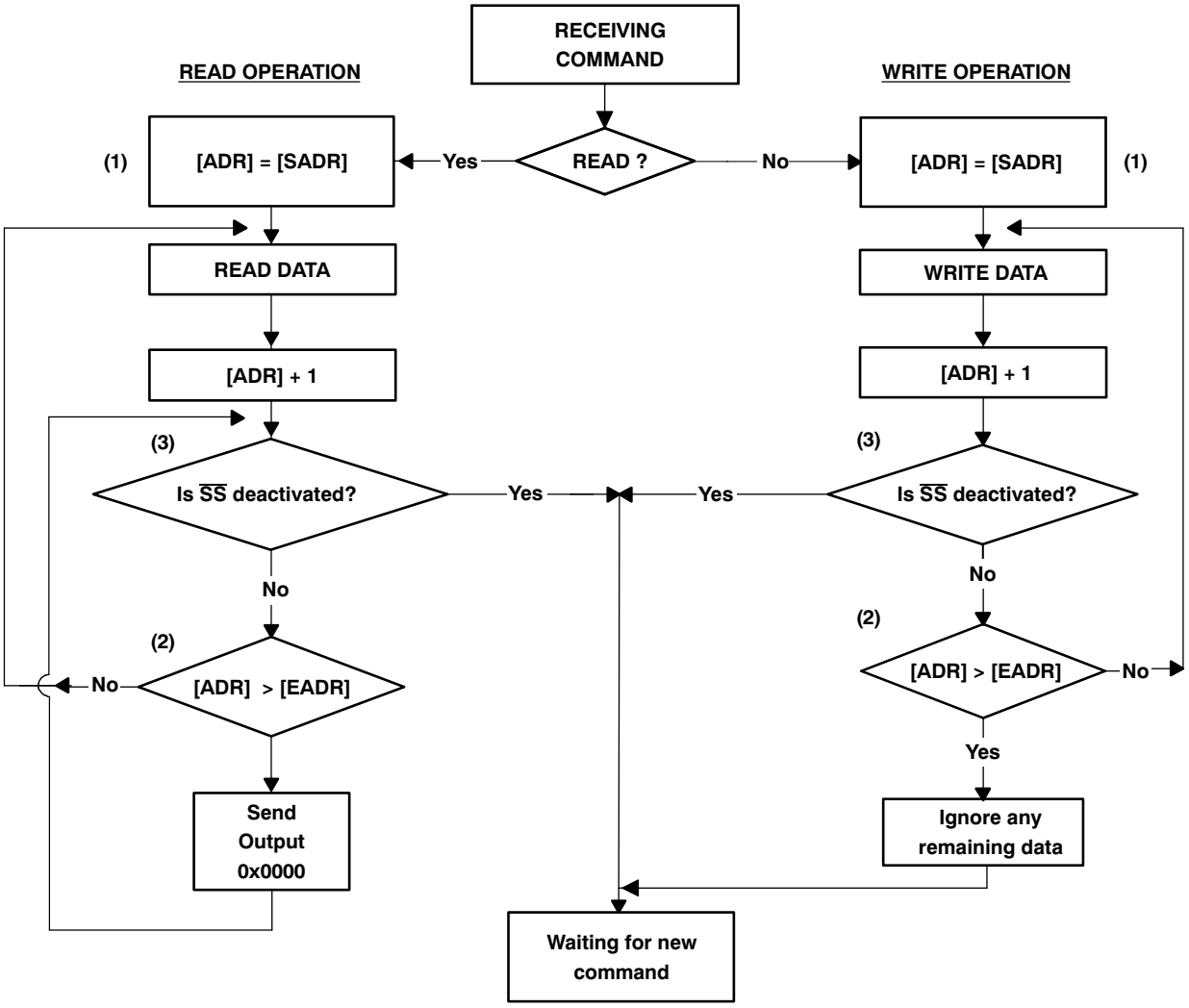
Figure 39. Write and Read Operation of AMC7823 Interface

AMC7823 MEMORY MAP

The AMC7823 has several 16-bit registers separated into two pages of memory, Page 0 and Page 1. The memory map is shown in Table 2. Locations that are marked ***Reserved*** read back 0x0000 if they are read by the host. Writing to these locations has no effect. Figure 40 explains the Read/Write operation.

Table 2. AMC7823 Memory Map

Page 0: Data/Status Registers				Page 1: Control/Setting Registers			
Address	**R/W**	**Default**	**Register Name**	**Address**	**R/W**	**Default**	**Register Name**
00	R	0x0000	ADC-0 Data	00	R/W	0x0000	DAC-0 Data
01	R	0x0000	ADC-1 Data	01	R/W	0x0000	DAC-1 Data
02	R	0x0000	ADC-2 Data	02	R/W	0x0000	DAC-2 Data
03	R	0x0000	ADC-3 Data	03	R/W	0x0000	DAC-3 Data
04	R	0x0000	ADC-4 Data	04	R/W	0x0000	DAC-4 Data
05	R	0x0000	ADC-5 Data	05	R/W	0x0000	DAC-5 Data
06	R	0x0000	ADC-6 Data	06	R/W	0x0000	DAC-6 Data
07	R	0x0000	ADC-7 Data	07	R/W	0x0000	DAC-7 Data
08	R	0x0000	ADC-8 Data	08	R/W	0x0000	LOAD DAC
09	R	0x0000	ALR Register	09	R/W	0x0000	DAC Configuration
0A	R/W	0xFFFF	GPIO Register	0A	R/W	0x4000	AMC Status/Configuration
0B			**Reserved**	0B	R/W	0x0000	ADC Control
0C			**Reserved**	0C	R/W	0x0000	RESET
0D			**Reserved**	0D	R/W	0x0000	Power-Down
0E			**Reserved**	0E	R/W	0x0FFF	Threshold-Hi-0
0F			**Reserved**	0F	R/W	0x0000	Threshold-Low-0
10			**Reserved**	10	R/W	0x0FFF	Threshold-Hi-1
11			**Reserved**	11	R/W	0x0000	Threshold-Low-1
12			**Reserved**	12	R/W	0x0FFF	Threshold-Hi-2
13			**Reserved**	13	R/W	0x0000	Threshold-Low-2
14			**Reserved**	14	R/W	0x0FFF	Threshold-Hi-3
15			**Reserved**	15	R/W	0x0000	Threshold-Low-3
16			**Reserved**	16			**Reserved**
17			**Reserved**	17			**Reserved**
18			**Reserved**	18			**Reserved**
19			**Reserved**	19			**Reserved**
1A			**Reserved**	1A			**Reserved**
1B			**Reserved**	1B			**Reserved**
1C			**Reserved**	1C			**Reserved**
1D			**Reserved**	1D			**Reserved**
1E			**Reserved**	1E	R	0x4000	Part Revision Number
1F			**Reserved**	1F			**Reserved**



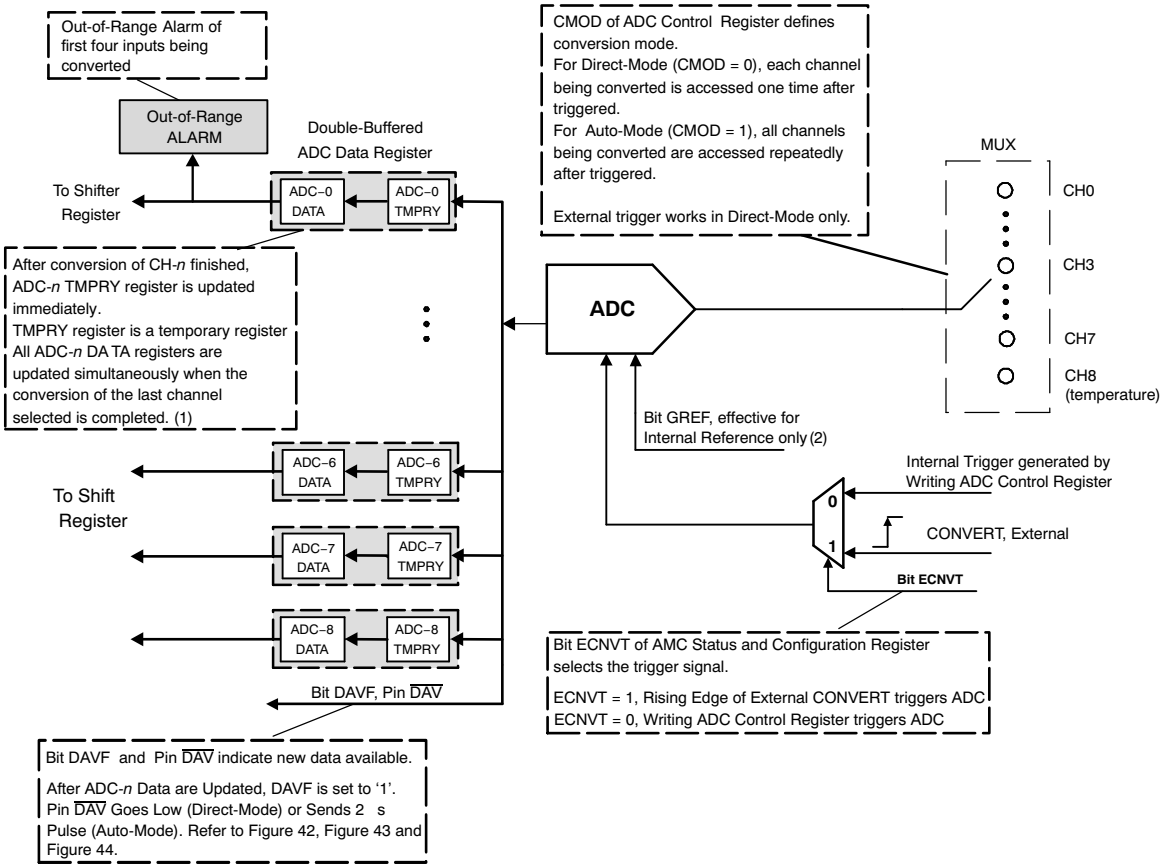
(1) [SADR] represents the start address, which is specified by bits [PG1:PG0] and [SADR4:SADR0] in the command word. [ADR] represents the current address.

(2) [EADR] represents the end address, which is specified by bits [PG0:PG1] and [EADR4:EADR0] in the command word.

(3) Host ends data transfer by deactivating $\overline{SS}$.

Figure 40. READ/WRITE Operation

ADC OPERATION (See AMC Status/Configuration Register and ADC Control Register)



(1) To avoid conflict, the data is not loaded into ADC-*n* data register from ADC-*n* temporary register until the data transfer from the ADC-*n* data register to the shift register (if any) finishes.

(2) When the internal reference is selected, the bit GREF determines the input range: GREF = 0, 0 to 2.5 V; GREF = 1, 0 to 5 V (for 5-V supply only). When an external reference is selected, the input range is 0 to 2 × V_{REF}. The input cannot be above AV_{DD}.

Figure 41. ADC Structure

The ADC has nine analog inputs. Channels CH0 through CH7 receive external analog inputs. CH8 is dedicated to the on-chip temperature sensor (see On-chip Temperature Sensor section).

ADC Trigger Signals (see AMC Status/Configuration Register)

The ADC can be triggered externally (external trigger mode) or internally (internal trigger mode). Bit ECNVT (Enable CONVERT) of the AMC Status/Configuration Register determines which mode is used. When ECNVT is set to '1', the ADC works in external trigger mode and the rising edge of the external signal CONVERT initiates data conversion. When ECNVT is cleared to '0', the ADC is in internal trigger mode, and writing to the ADC Control Register initiates conversion.

After the ADC is triggered, a group of analog inputs (up to nine channels may be specified) are multiplexed and each channel is converted. The starting and ending addresses of the group of channels are specified by the bits [SA3:SA0] and [EA3:EA0], respectively, in the ADC Control Register (see ADC Control Register for details). The specified channels are converted sequentially from the starting to ending address, according to Table 12, the Analog Input Channel Address Map. If the ending address is equal to or smaller than the starting address, only the starting address channel is converted.

Conversion Mode

When internal trigger mode is selected (ECNVT = 0), two types of ADC conversion are available: direct-mode and auto-mode. The bit CMODE (Conversion MODE) of the ADC Control Register specifies the conversion mode. When external trigger mode is selected (ECNVT = 1), only direct-mode conversion is available. In this case, bit CMODE in the ADC Control Register is ignored. (See Table 3.)

In direct-mode, each analog channel within the specified group is converted a single time. After the last channel is converted, the ADC goes into idle state and waits for a new trigger. Only the starting channel is converted if the ending address is equal to or smaller than the starting address.

Auto-mode is a continuous operation. In auto-mode, each analog channel within the specified group is converted sequentially from [SA3:SA0] to [EA3:EA0] and repeatedly until one of the following events occur:

- a new internal trigger is issued;
- the conversion mode is changed to direct-mode by rewriting the ADC Control Register; or
- the external trigger is enabled by rewriting the AMC Status/Configuration Register.

When a new internal trigger is issued, a new conversion process starts. If the ending address [EA3:EA0] is equal to or smaller than the starting address [SA3:SA0], the starting address channel is repeatedly converted and others are ignored.

Table 3 summarizes the ADC conversion modes.

Table 3. ADC Conversion Mode

ECNVT OF AMC STATUS/ CONFIGURATION REGISTER	CMODE OF ADC CONTROL REGISTER	ADC CONVERSION MODE
1	–	External Trigger, Direct-Mode
0	0	Internal Trigger, Direct-Mode
0	1	Internal Trigger Auto-Mode

Double-Buffered ADC Data Register

The host can access all nine double-buffered ADC Data registers. The conversion result from the analog input with the channel address *n* is stored in the ADC-*n* Data register. When the conversion of an individual channel is completed, the data is immediately transferred into the corresponding ADC-*n* temporary (TMPRY) register, the first stage of the data buffer. When the conversion of the last channel ([EA3:EA0]) finishes, all data in ADC-*n* TMPRY registers are transferred simultaneously into the corresponding ADC-*n* Data registers, the second stage of the data buffer. However, if a data transfer is in progress between an ADC-*n* Data Register and the AMC Shift Register, this ADC-*n* Data Register is not updated until the data transfer is complete. The conversion result from channel address *n* is stored in the ADC-*n* Data Register. For example, the result from channel [0x04] is stored in the ADC-4 Data Register, and the result from channel [0x07] is stored in the ADC-7 Data Register. The ADC-8 Data Register is used to store on-chip temperature measurement data (see the On-chip Temperature Sensor).

SCLK Clock Noise

The host activates the slave select signal $\overline{SS}$ (low) to access the AMC7823. When $\overline{SS}$ is high, the SCLK clock is blocked. To avoid noise caused by SCLK clock, deactivate $\overline{SS}$ (high) for at least the conversion process time immediately after the ADC conversion starts.

Handshaking with the Host (see AMC Status/Configuration Register)

The $\overline{DAV}$ pin and the bit DAVF (Data Available Flag) of the AMC Status/Configuration Register provide handshaking with the host. Pin and bit status depend on the conversion mode (direct or auto). In direct-mode, after ADC-*n* Data registers of all of the selected channels are updated, the DAVF bit in the AMC Status/Configuration Register is set immediately to '1', and the $\overline{DAV}$ pin is active (low) to signify new data is available. Reading the ADC-*n* Data Register or re-starting the ADC clears bit DAVF to '0' and deactivates $\overline{DAV}$ pin (high).

In auto-mode, after ADC-*n* Data registers of the selected channels are updated, a pulse of 2 μs (low) appears on pin $\overline{DAV}$ to signify new data is available. However, bit DAVF is always cleared to '0' in auto-mode.

Figure 42, Figure 43 and Figure 44 illustrate the handshaking protocol.

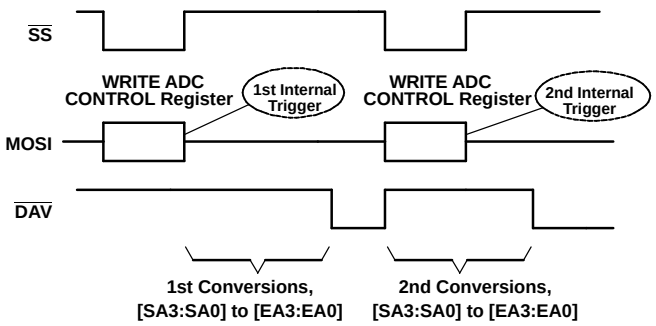


Figure 42. Internal Trigger, Direct-Mode

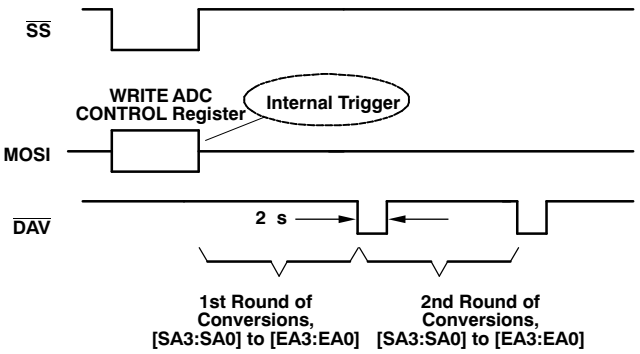


Figure 43. Internal Trigger, Auto-Mode

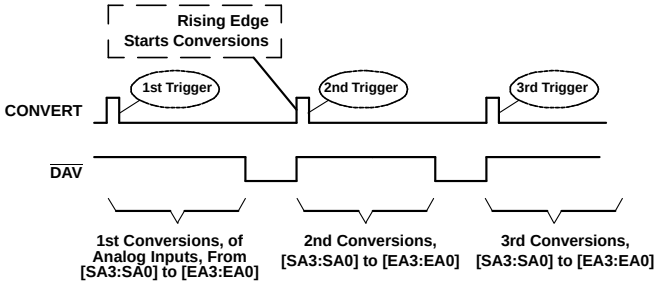


Figure 44. External Trigger

Analog Input Out-of-Range Detection (see Analog Input Out-of-Range Alarm Section)

The first four analog inputs of the group defined by the bits [SA3:SA0] and [EA3:EA0] are implemented with out-of-range detection. When an input is out of the preset range, the corresponding alarm flag, bit ALR-*n* of the ALR (Alarm) Register is set. If any of the four inputs are out of range, the global out-of-range pin $\overline{GALR}$ goes low. Four GPIO pins (GPIO-0, GPIO-1, GPIO-2 and GPIO-3) can be configured as out-of-range indicators for each of the first four analog inputs. See the Analog Input Out-of-Range Alarm and Digital I/O sections for more details.

Full-Scale Range of Analog Input

The full-scale range of the analog input is $2 \times V_{REF}$, but must not exceed the supply value AV_{DD}. Input saturation can occur if the analog input exceeds this value.

The internal reference or an externally applied reference may be used as V_{REF}. The bit SREF in the AMC Status/Configuration Register controls the selection of the internal reference. When SREF = 0 (power-up default condition), the internal reference is selected and is internally applied through a 10-kΩ resistor to pin 21. When SREF = 1, the internal reference is disconnected from pin 21, and an external reference may be applied. See Figure 48.

Table 4 shows the configuration of the ADC input range.

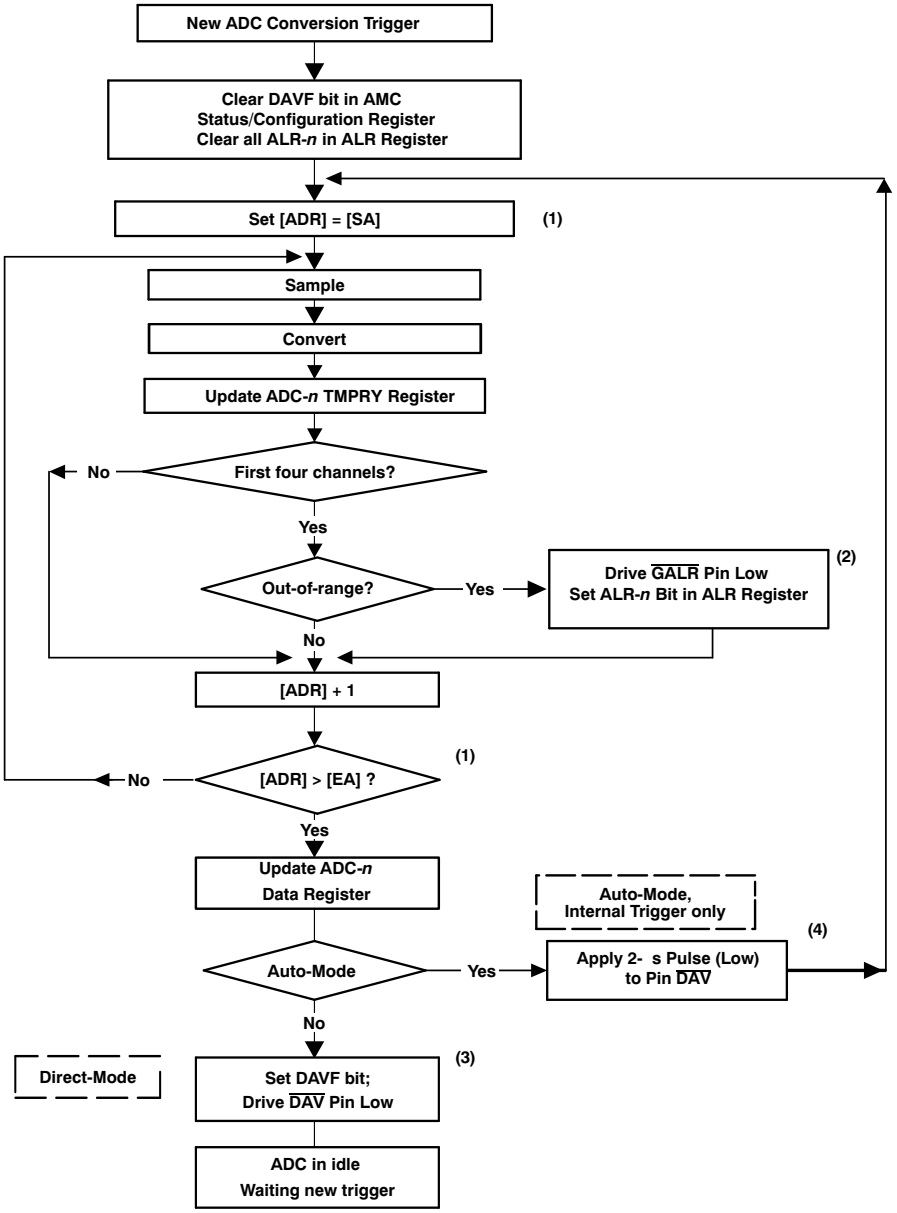
Table 4. Configuration of ADC Input Range

BIT GREF	BIT SREF	ADC INPUT RANGE	DESCRIPTION
0	0	0 to 2.5 V	Internal reference, 1.25 V
1	0	0 to 5 V	Internal reference, 2.5 V, AV_{DD} = 5 V only
Don't care	1	0 to $2 \times V_{REF}$	External reference V_{REF}. $2 \times V_{REF}$ must not be greater than AV_{DD}. Set SREF = 1 when applying external reference.

The bit GREF in the AMC Status/Configuration Register selects between two preset internal reference values. When GREF = 0 (power-up default condition), the internal reference is set to 1.25 V. When GREF = 1, the internal reference is 2.5 V. GREF must be cleared to '0' when the power supply is less than 5 V.

When an external reference is applied, the input range is 0 to 2 × V_{REF}, and is not affected by the bit GREF. In this case, ideally SREF has been set to '1' and the internal reference is disconnected. This condition is preferred for operating the AMC7823. If SREF = 0, the external reference overrides the internal reference, provided it can accommodate a 10-kΩ load. To avoid input saturation, the external reference must not be greater than 2.5 V when the analog power supply is 5 V, and must not be greater than 1.25 V when the supply is 3 V.

Figure 45 illustrates the ADC operation.



(1) **[SA]** represents the first input channel, **[EA]** represents the last input channel. **[ADR]** represents the current input channel. **[SA3:SA0]** is the address of **[SA]**. **[EA3:EA0]** is the address of **[EA]**.

(2) $\overline{\text{GALR}}$ pin goes high and bits ALR-*n* are cleared after new ***ADC Conversion*** trigger.

(3) After reading the ADC Data Register, bit DAVF is cleared, and the $\overline{\text{DAV}}$ pin goes high.

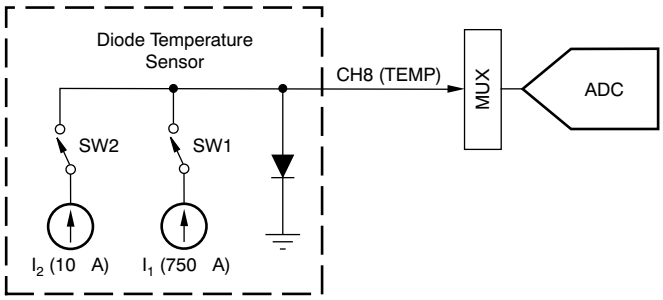
(4) In Auto-mode, bit DAVF is always cleared.

Figure 45. ADC Operation Flow Chart

ON-CHIP TEMPERATURE SENSOR

The AMC7823 has an integrated temperature sensor to measure the on-chip temperature. This measurement relies on the characteristics of a semiconductor p-n junction operating at a known current level. The forward voltage of the diode (V_{BE}) depends on the current passing through it and the junction temperature.

Channel CH8 is dedicated to the on-chip temperature sensor. When CH8 is converted, the on-chip temperature measurement process is activated. Two measurements, and therefore two ADC conversions, are required to capture the temperature data. First, the diode is driven by current I_1 (750 μA) and the forward voltage V_{BE1} is measured. Next, the diode is driven by current I_2 (10 μA) and V_{BE2} is measured. The difference of these two voltages, ΔV_{BE}, is stored in the ADC-8 Data Register as straight binary code. See Figure 46.



NOTE: When CH8 is converted, two conversions are performed. During the first conversion, SW1 is turned on, SW2 is off, and the diode is driven by I_1 (750 μA). During the second conversion, SW2 is turned on, SW1 is off, and the diode is driven by I_2 (10 μA).

Figure 46. Local Temperature Sensor Operation

In direct-mode operation, the temperature can be measured by converting Channel CH8 only, or by converting several channels including Channel CH8. In auto-mode, the temperature must be measured by converting at least two channels including Channel CH8.

The following equations illustrate the corresponding temperature calculation process:

ΔV_{BE} (mV) = decimal code (convert from ADC-8 Data Register binary code) × 1.22 mV for V_{REF} = 2.5 V

or

ΔV_{BE} (mV) = decimal code (convert from ADC-8 Data Register binary code) × 0.61 mV for V_{REF} = 1.25 V.

Temp (°K) = 2.6 × ΔV_{BE} (mV)

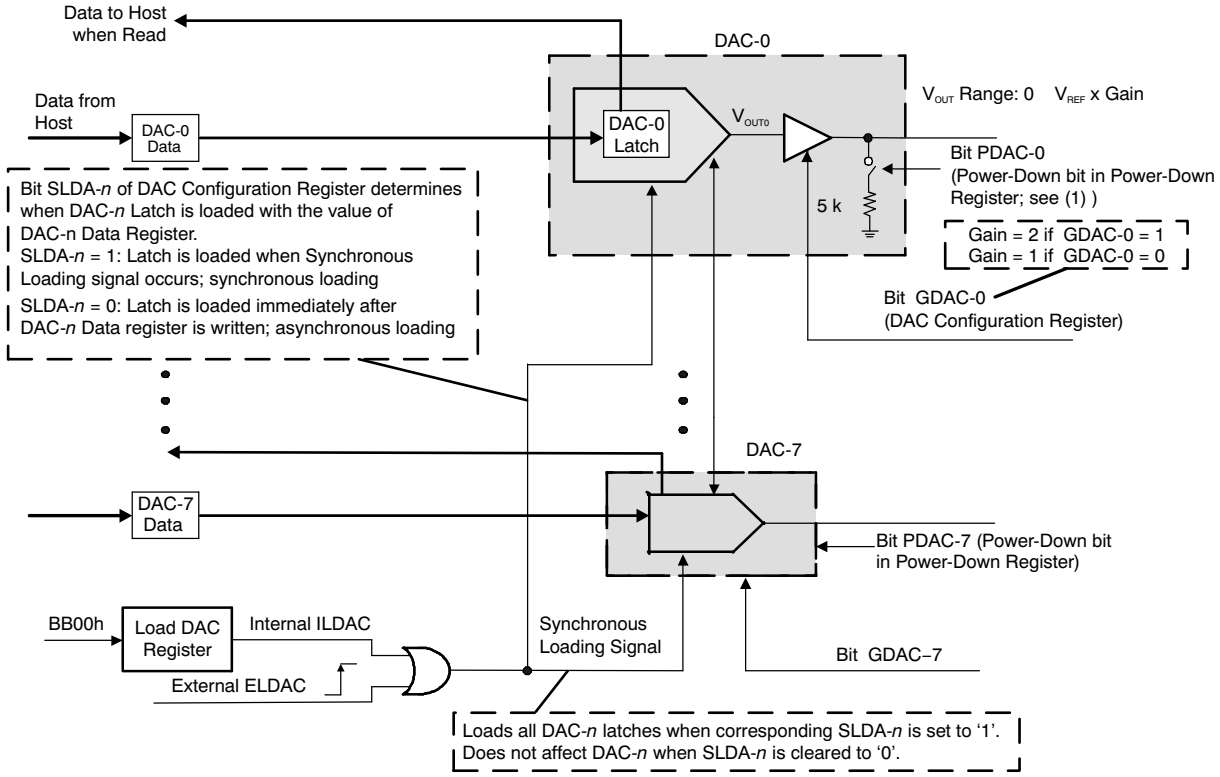
or

Temp (°C) = 2.6 × ΔV_{BE} (mV) – 273°K.

The resolution of this calculation is 3.2°C/LSB when the reference voltage is 2.5 V and 1.6°C/LSB for a reference voltage of 1.25 V.

DAC OPERATION (see DAC-n Data Registers and DAC Configuration Register)

AMC7823 has eight double-buffered DACs. The outputs of the DACs can be updated synchronously or individually (asynchronously). Figure 47 illustrates the generic DAC structure.



(1) When PDAC-*n* = 0, DAC-*n* is in power-down mode; the output buffer of DAC-*n* connects to ground through a 5-kΩ load.

Figure 47. DAC Structure

Double-Buffered Data Register

All eight DAC data registers are double-buffered. Each DAC has an internal latch preceded by an input register. Data is initially written to an individual DAC-*n* Data register and then transferred to its corresponding DAC-*n* Latch. When the DAC-*n* Latch is updated, the output of DAC-*n* changes to the newly set value. When the host reads the register memory map location labeled DAC-*n* Data, the value held in the DAC-*n* Latch is returned (not the value held in the input DAC-*n* Data Register).

Synchronous Load, Asynchronous Load, and Output Updating

The DAC latches can be updated synchronously or asynchronously. The bit SLDA-*n* (Synchronous Load) of the DAC Configuration Register is used to specify the DAC updating mode.

Asynchronous mode is active when SLDA-*n* is cleared to '0'. Immediately after writing to the DAC-*n* Data Register, its data is transferred to the corresponding DAC-*n* Latch Register, and the output of DAC-*n* changes accordingly.

Synchronous mode is selected when the bit SLDA-*n* is set to '1'. The value of the DAC-*n* Data Register is transferred to the DAC-*n* Latch only after an active DAC synchronous loading signal occurs, which immediately updates the DAC-*n* output. Under synchronous loading operation, writing data into a DAC-*n* Data Register changes only the value in that register, but not the content of DAC-*n* Latch nor the output of DAC-*n*, until the synchronous load signal occurs.

The DAC synchronous load signal can be the rising edge of the external signal ELDAC, or the internal signal ILDAC. Write BB00h into the Load DAC Register to generate ILDAC. When the DAC synchronous load signal occurs, all DACs with the bit SLDA-*n* set to '1' are updated simultaneously with the value of the corresponding DAC-*n* Data register. By setting the bit SLDA-*n* properly, several DACs can be updated at the same time. For example, to update DAC0 and DAC1 synchronously, the host sets the bits SLDA-0 and SLDA-1 to '1' first, then writes the proper values into the DAC-0 Data and DAC-1 Data registers, respectively. After this presetting, the host activates ELDAC (or ILDAC) to load DAC0 and DAC1 simultaneously. The outputs of DAC0 and DAC1 change at the same time.

Table 5 summarizes methods to update the output of DAC-*n*.

Table 5. DAC-*n* Output Update Summary

BIT SLDA-*n*	WRITING LOAD DAC REGISTER	EXTERNAL ELDAC SIGNAL	OPERATION
0	Don't care	Don't care	Update DAC-*n* individually. DAC-*n* Latch and DAC-*n* Output are immediately updated after writing to DAC-*n* Data Register
1	Write 0xBB00	0	Simultaneously update all DAC by internal trigger . Writing 0xBB00 generates internal load DAC trigger signal ILDAC, which causes DAC-*n* Latches and DAC-*n* Outputs to be updated with the contents of corresponding DAC-*n* Data Register.
1	No	Rising edge	Simultaneously update all DACs by external trigger ELDAC. Rising edge of ELDAC causes DAC-*n* Latches and DAC-*n* Outputs to be updated with the contents of corresponding DAC-*n* Data Register.

Full-Scale Output Range

Full-scale output range of each DAC is set by the product of the value of the reference voltage times the gain of the DAC output buffer, V_{REF} × Gain. The bit GDAC-*n* (Gain of DAC-*n* output buffer) of the DAC Configuration Register sets the gain of the individual DAC-*n* output buffer. The gain is unity (1) when GDAC-*n* is cleared to '0', and is 2 when GDAC-*n* is set to '1'.

The value of V_{REF} may be controlled by bits SREF and GREF in the AMC Status/Configuration Register and by the choice of internal or external reference. For a similar description, see the Full-Scale Range of Analog Input in the ADC Operation section.

Full-scale output range of each DAC is limited by the analog power supply because the DAC output buffer cannot exceed AV_{DD}. Table 6 shows how to configure the DAC output range.

Table 6. Configuration of DAC Output Range

SREF	GREF	GDAC-*n*	REFERENCE	OUTPUT RANGE	
				AV_{DD} = 3 V	AV_{DD} = 5 V
0	0	0	Internal 1.25 V	0 V to 1.25 V	0 V to 1.25 V
0	0	1	Internal 1.25 V	0 V to 2.5 V	0 V to 2.5 V
0	1	0	Internal 2.5 V	0 V to 2.5 V	0 V to 2.5 V
0	1	1	Internal 2.5 V	Saturated at 3 V	0 V to 5 V
1	Don't care	0	External V_{REF}	0 V to External V_{REF}, External $V_{REF} \le AV_{DD}$	0 V to External V_{REF}, External $V_{REF} \le AV_{DD}$
1	Don't care	1	External V_{REF}	0 V to External V_{REF} × 2 2 × External $V_{REF} \le AV_{DD}$	0 V to External V_{REF} × 2 2 × External $V_{REF} \le AV_{DD}$

After power-on or reset, all DAC-*n* Data Registers and all DAC-*n* Latches are cleared to '0'. This clearing process results in all DAC outputs at 0 V, gain of unity, and a full-scale output range preset to either 1.25 V or equal to the external reference (if it is applied) because bits SREF and GREF are also cleared to '0'.

Zero Code Output Value

Each DAC buffer is clamped to prevent the output from going to 0 V. Thus, when the input code is 000h, the output is typically 15 mV to 20 mV. This output keeps the closed-loop DAC output buffer in an active, stable operating regime, allowing it to immediately respond to an input that produces an output typically greater than 20 mV. Near-zero-volt output for a particular DAC-*n* may be achieved by clearing bit PDAC-*n* to '0' in the Power-Down register.

POWER-DOWN MODE

The AMC7823 is implemented with power-down mode. Bits in the Power-Down Register control power applied to the ADC, each DAC output buffer, the output amplifier of the precision current source, and the reference buffer. The reference buffer drives all the DAC resistor strings and supplies reference voltage to the precision current source. After power-on reset or any forced hardware or software reset, the Power-Down Register is cleared, and all these specified components are in power-down mode.

In power-down mode, most of the linear circuitry is shut down. The ADC halts conversions, output current of the precision current source drops to zero, and each external DAC output pin is switched from the DAC output buffer to analog ground through an internal 5-kΩ resistor. The internal reference and the internal oscillator remain powered to facilitate rapid recovery from power-down mode.

None of the bits in the Power-Down Register affect the digital logic. All digital signals (such as the SPI interface, $\overline{\text{RESET}}$, ELDAC, $\overline{\text{ALR}}$, and all GPIO) still work normally in any power-down condition. In power-down mode, the host can read registers to get information, or write to registers to change settings. No write operation can start the ADC (if the ADC is in power-down), or change the DAC output (if the DAC is in power-down), but write operations can update register values. The new register values are effective immediately upon exiting the power-down mode. In this way, the host can preset DACs and the ADC before a wake-up call.

The contents of all Page 1 addresses (see Table 2) do not change when entering or exiting power-down mode. The contents of the ADC registers and the alarm information in the ALR and GPIO Registers of Page 0 do not change when entering or exiting power-down mode ***if*** the ADC is in **direct mode** before powering down. To avoid losing ADC register content and alarm information in the ALR and GPIO Registers while the ADC is powered down, do not issue a convert command during power-down mode. General-purpose I/O data are not affected. For details, see the sections on the ALR Register and the GPIO Register.

For power-down mode details, see the Power-Down Register section.

REFERENCE

The AMC7823 requires a reference voltage to drive the ADC, the DACs, and the precision current source. It can accommodate the application of an external reference voltage, or it can supply reference from an internal bandgap voltage circuit as shown in Figure 48. Pin 21, EXT_REF_IN, is common to either source. An internal 10-kΩ resistor connects the internal reference source to pin 21. This pin provides a point for noise filtering by placing a capacitor, if desired, from the pin to analog ground. The time constant of this filter is [(10 kΩ) × (C_{FILTER})]. The resistor also allows an external reference applied to pin 21 to override the internal reference, provided it can drive the 10-kΩ load.

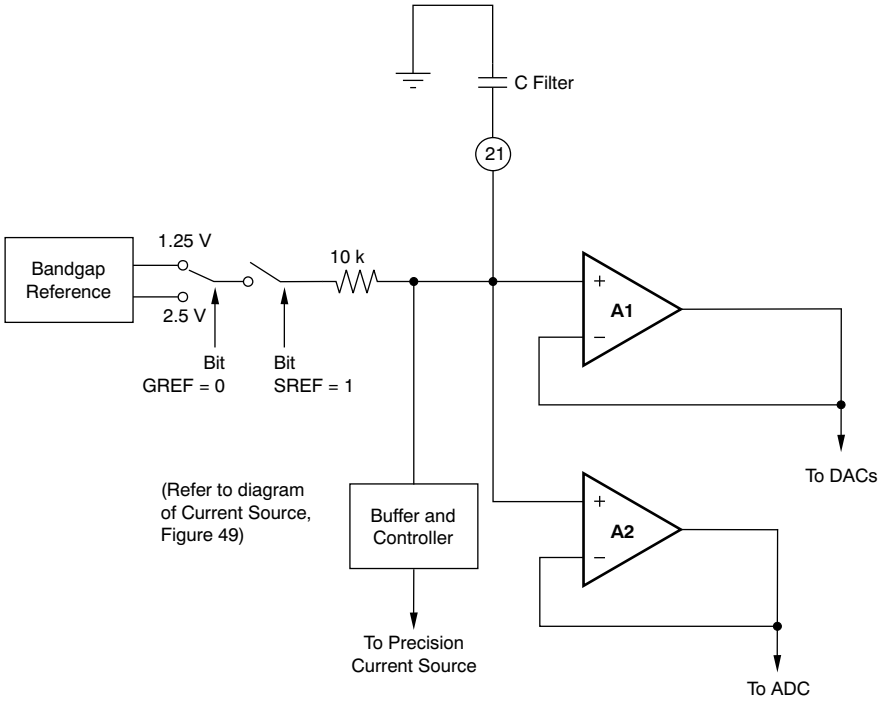


Figure 48. Reference

Logic bits SREF and GREF of the AMC Status/Configuration Register specify operation of the internal reference and also should be considered when applying an external reference, as explained below. These bits also provide information to the precision current source and are used in configuring that source (refer to the Precision Current Source section for details).

When SREF is cleared to '0' (the default or power-on reset condition), the internal reference is selected and connected to pin 21 by the 10-kΩ resistor. When SREF is set to '1', the internal reference is de-selected and disconnected from pin 21. Pin 21 then floats unless an external reference is applied.

The bit GREF selects one of two pre-set values for the internal reference voltage. When GREF is cleared to '0', the internal reference voltage is +1.25 V. When GREF is set to '1', the internal reference voltage is +2.5 V.

It is recommended to always set SREF to '1' when using an external source; otherwise, the external reference must sink or source a current of value equal to the difference in the reference voltages divided by 10 kΩ. For example, if SREF and GREF are both cleared to '0' and a 2.5-V external reference is applied, the AMC7823 must unnecessarily sink 125 μA.

PRECISION CURRENT SOURCE

The AMC7823 provides the user with a precision current source for driving an external component such as a thermistor. Output current from pin 5 is set by the value of the resistor (R_{SET}) connected from pin 4 to the analog supply voltage. This resistor should be close to the AMC7823 to minimize any voltage drop from the analog supply to the resistor. Internal closed-loop circuitry impresses a fixed voltage across the set resistor by means of an operational amplifier and a PMOS-follower output driver. Current through the set resistor supplies the follower. The follower driver supplies this current to the external load connected from PRECISION_I_OUTPUT (pin 5) to ground. This circuit architecture maintains high output impedance and provides wide output voltage compliance. See Figure 49.

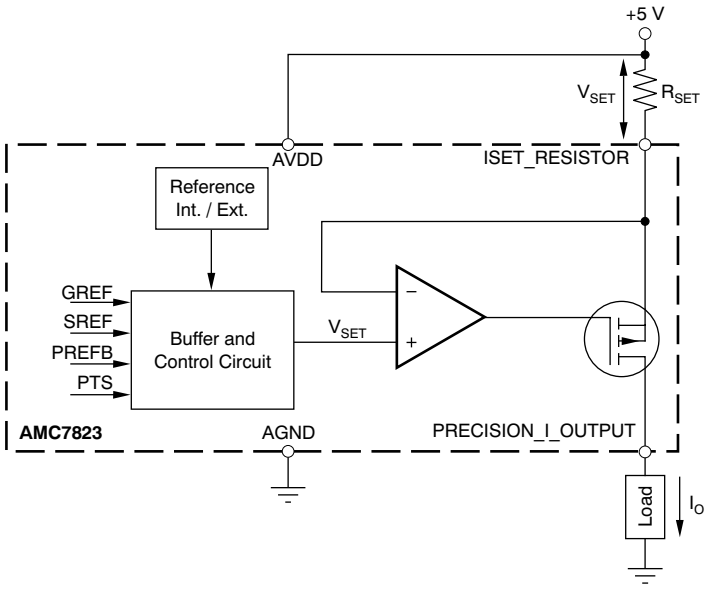


Figure 49. Diagram of Current Source

In addition to the external setting resistor R_{SET}, four logic bits—PTS and PREFB in the Power-Down Register and SREF and GREF in the AMC Status/Configuration Register—are used to configure the current source as well. Table 7 describes how to configure the current source.

The bit PTS is the current source power-down bit. When PTS is cleared to '0', the current source is in power-down mode, and the output current is zero. When PTS is set to '1' and PREFB is set to '1', the current source is in normal operation.

Bit SREF is the reference source selection bit. When SREF is cleared, the internal reference is selected. When SREF is set to '1', the internal reference is de-selected. Set SREF = 1 when an external reference is applied.

GREF is the internal reference gain bit. PREFB is the Reference Buffer Amplifier Power-Down bit. Both bits provide information to the current source circuit, and affect the current source configuration.

If the internal reference is used, and no external reference is applied to pin 21, the output current is 0.5 V/R_{SET} (V_{SET} = 0.5 V) or zero, depending on bits PREFB and GREF, as shown in Table 7.

For a precise calculation, measure the voltage across the set resistor (V_{SET}) and divide it by the precise value of R_{SET}.

Table 7. Precision Current Source Configuration

SREF	PTS	PREFB	GREF	I_O
0	0	Don't care	Don't care	0
0	1	0	1	0
0	1	Don't care	0	$0.5V/R_{SET}$ (1)
0	1	1	1	$0.5V/R_{SET}$ (1)
1	0	Don't care	Don't care	0
1	1	0	1 (2)	0
1	1	Don't care	0 (2)	Equation 1
1	1	1	1 (2)	Equation 1

(1) V_{SET} = 0.5 V.
(2) Make GREF = 1 for 2.5-V external reference; make GREF = 0 for 1.25-V external reference.

When an external reference is used, select a reference value (V_{REF}) close to either 1.25 V or 2.5 V, and write bit GREF low ('0') for a 1.25-V reference, or write it high ('1') for a 2.5-V reference. These settings make a better match to the applied external reference value. The output current can be calculated by Equation 1:

$$I_{OUTPUT} = \frac{V_{SET}}{R_{SET}} = \frac{(V_{REF} \times 0.4)}{(1 + GREF) \times R_{SET}} \quad (1)$$

The applied external reference voltage may deviate from the recommended values, but it is important to limit the maximum voltage applied to the set resistor to approximately 0.5 V. Voltages greater than 0.5 V across the set resistor reduce the specified compliance of the current source to the load.

DIGITAL I/O (See AMC Status/Configuration Register)

The AMC7823 has four special function pins: $\overline{DAV}$, $\overline{GALR}$, ELDAC, and CONVERT, It also has six general I/O pins (GPIO-*n*). The GPIO-*n* pins are used as general digital I/O or analog input out-of-range indicators.

The pin $\overline{DAV}$ is an output pin that indicates the completion of ADC conversions. Bit DAVF of the AMC Status/Configuration Register determines the status of the $\overline{DAV}$ pin. In direct-mode, after the selected group of input channels has been converted and the ADC has been halted, bit DAVF is set to '1' and pin $\overline{DAV}$ is driven to logic low (active). In auto-mode, each time the group of input channels has been sequentially converted, a 2-µs pulse (low) appears on the $\overline{DAV}$ pin after the last channel of the group is converted. This conversion sequence is repeated and the pulse is repeated.

The $\overline{GALR}$ pin is an output pin that indicates whether any of the first four analog inputs being converted are out-of-range. Bits ALR-*n* of the ALR Register determine the status of $\overline{GALR}$ pin. $\overline{GALR}$ is low (or active) if any one of the bits ALR-*n* is set to '1'. $\overline{GALR}$ is high (inactive) if and only if all bits are cleared to '0'. See Figure 50.

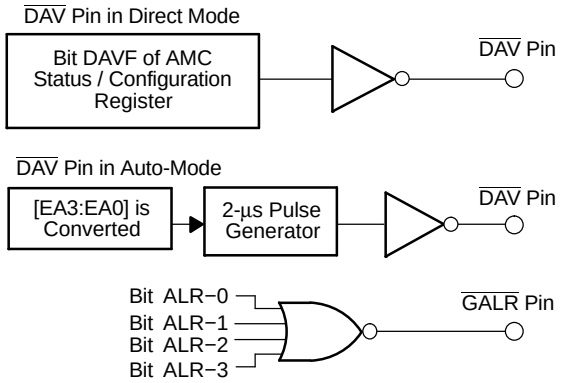


Figure 50. $\overline{DAV}$ Pin and $\overline{GALR}$ Pin

The CONVERT pin is an input pin for the external ADC trigger signal. When bit ECNVT of the AMC Status/Configuration Register is set to '1', the AMC7823 works in external trigger mode. The rising edge of CONVERT starts the ADC conversion.

The ELDAC pin is an input pin for the external DAC synchronous load signal. The rising edge of ELDAC updates all DAC-*n* simultaneously that have the corresponding bit SLDA-*n* set to '1'.

The AMC7823 has six GPIO pins, GPIO-*n* (*n* = 0, 1, 2, 3, 4, 5). Pins GPIO-4 and GPIO-5 are dedicated to general bidirectional digital I/O signals. The remaining pins (*n* = 0, 1, 2, 3) are dual-purpose pins, and can be programmed as either bidirectional GPIO or $\overline{\text{ALR}}$ (out-of-range alarm) indicators. Figure 51 shows the pin structure of GPIO-4 and GPIO-5. See Figure 52 for the pin structure of GPIO-*n* (*n* = 0, 1, 2 and 3).

The bit IOMOD-*n* (*n* = 0, 1, 2, 3) in the GPIO register defines the function of these dual-purpose GPIO-*n* pins (see Table 8). When the corresponding IOMOD-*n* bit is cleared to '0', GPIO-*n* pins are configured as out-of-range indicators (denoted $\overline{\text{ALR}}$-0, $\overline{\text{ALR}}$-1, $\overline{\text{ALR}}$-2, and $\overline{\text{ALR}}$-3) for the first four analog inputs being converted. As an out-of-range indicator, the $\overline{\text{ALR}}$-*n* pin is an output whose status is determined by bits ALR-0, ALR-1, ALR-2, and ALR-3 of the ALR Register. When ALR-*n* is set to '1', the $\overline{\text{ALR}}$-*n* pin is low. When ALR-*n* is cleared to '0', the $\overline{\text{ALR}}$-*n* pin is in high impedance status. When IOMOD-*n* is set to '1', the GPIO-*n* pin works as a general, bidirectional digital I/O pin.

Table 8. GPIO Function

PIN NAME	IOMOD-*n*	
	1	0
GPIO-0	GPIO	$\overline{\text{ALR}}$-0
GPIO-1	GPIO	$\overline{\text{ALR}}$-1
GPIO-2	GPIO	$\overline{\text{ALR}}$-2
GPIO-3	GPIO	$\overline{\text{ALR}}$-3

When the GPIO-*n* pin works as general, bidirectional digital I/O, it can receive an input or produce an output. (See Figure 51 and Figure 52.) When acting as output, its status is determined by the corresponding bit IOST-*n* (I/O Status) of the GPIO Register. The output is high impedance when bit IOST-*n* is set to '1' and is logic low when bit IOST-*n* is cleared to '0'. An external pull-up resistor is required when using GPIO-*n* as output.

When GPIO-*n* acts as input, the digital value on the pin is acquired by reading the bit IOST-*n*.

After power-on reset or any forced hardware or software reset, all IOMOD-*n* and IOST-*n* bits are set to '1', and all GPIO pins work as general I/O pins in high impedance status. See the GPIO Register for more detail.

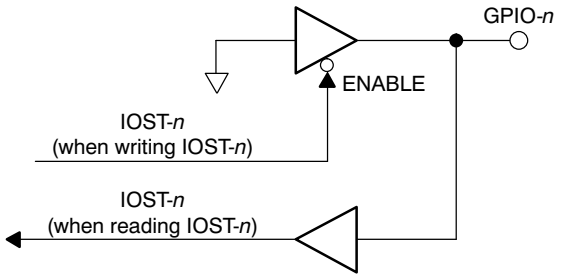


Figure 51. Pin Structure of GPIO-4 and GPIO-5

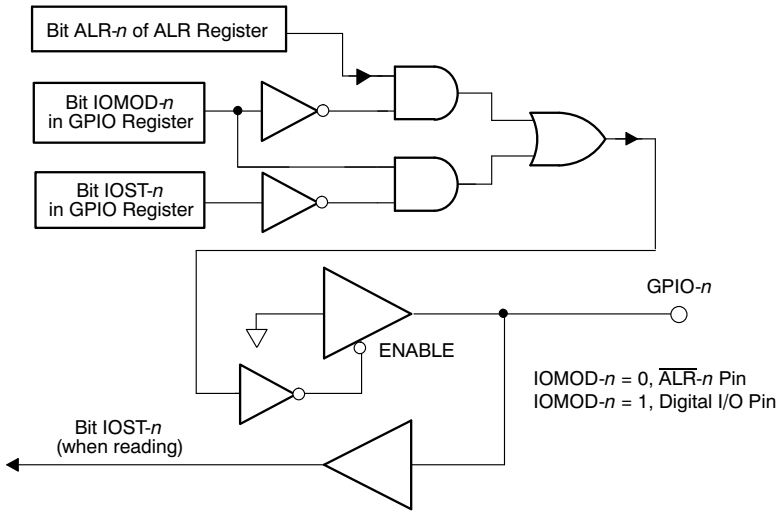
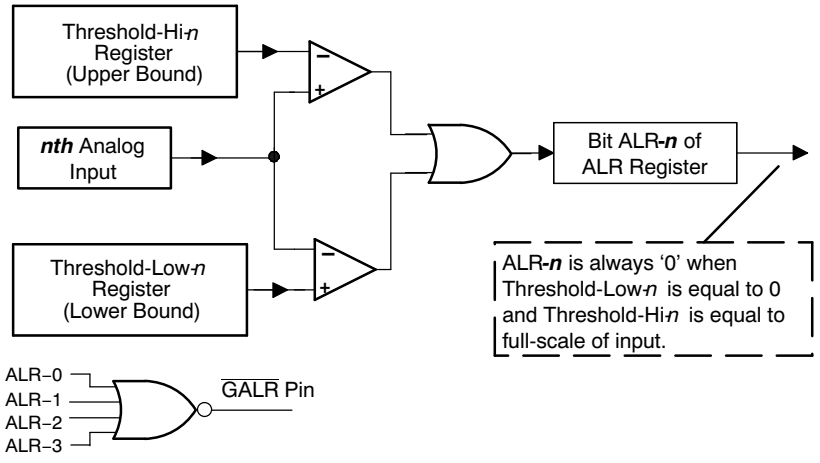


Figure 52. Pin Structure of GPIO-0, GPIO-1, GPIO-2, and GPIO-3

ANALOG INPUT OUT-OF-RANGE ALARM (See ADC Operation)

The AMC7823 provides out-of-range detection for the first four analog inputs of the group of inputs specified by the starting and ending addresses [SA3:SA0] and [EA3:EA0], respectively. Figure 53 describes the analog out-of-range logic. Alarm bits ALR-*n* in the ALR Register are set to '1' to flag an out-of-range condition. If the *n*th analog input is out of the preset range, then bit ALR-*n* is set to '1'. The *n*th alarm bit does not necessarily correspond to input channel address *n*, however. For example, if [SA3:SA0] and [EA3:EA0] of the ADC Control Register are 0x04 and 0x07, respectively, then the channel address of the first analog input is [0x04] and the corresponding alarm bit is ALR-0. The address of the fourth input channel is [0x07] and its corresponding alarm bit is ALR-3. Only the first four analog inputs can be implemented with out-of-range detection. In this example, the addresses of the first four inputs implemented with out-of-range detection are [0x04], [0x05], [0x06], and [0x07], respectively. However, if [SA3:SA0] is equal to [0x00] and [EA3:EA0] is equal to [0x07], then the addresses of the first four are [0x00], [0x01], [0x02] and [0x03].



NOTE: Threshold-Hi-*n* must not be smaller than Threshold-Low-*n*. Otherwise, ALR-*n* is always '1'.

Figure 53. Analog Out-of-Range Alarm Logic

The value in the Threshold-Hi-*n* Register defines the upper bound threshold of the *n*th analog input, while the value in Threshold-Low-*n* defines the lower bound. These two bounds specify a window for the out-of-range detection. The out-of-range condition occurs when the input is set outside the window defined by these boundaries. To implement single upper-bound threshold detection, the host processor can set the upper bound to the desired value and the lower bound to zero. For lower-bound detection, the host can set the lower bound to the desired value and the upper bound to the full-scale input.

To deactivate the alarm function (ALR-*n* always '0'), set the threshold registers to their default values as specified in Table 2.

Note: The value of Threshold-Hi-*n* must not be less than the value of Threshold-Low-*n*; otherwise, ALR-*n* is always set to '1' and the alarm indicator is always active.

If any out-of-range alarm occurs, the Global Alarm pin ($\overline{\text{GALR}}$, pin 1) goes logic low. This function provides an interrupt to the host so that it may query the ALR Register (alarm register) to determine which channels are out-of-range.

The general-purpose I/O pins, GPIO-0, GPIO-1, GPIO-2 and GPIO-3, are dual-purpose and can be configured as individual out-of-range alarm indicators denoted as $\overline{\text{ALR}}$-0, $\overline{\text{ALR}}$-1, $\overline{\text{ALR}}$-2 and $\overline{\text{ALR}}$-3 as discussed previously. Each $\overline{\text{ALR}}$-*n* pin displays the logical complement of of each corresponding ALR-*n* bit. For example, when an alarm condition occurs, bit ALR-*n* is set to '1' and pin $\overline{\text{ALR}}$-*n* goes logic low. For each GPIO-*n* pin configured as an alarm, its corresponding IOST-*n* bit in the GPIO Register displays the complement of bit ALR-*n*. For example, when bit ALR-*n* is set to '1', bit IOST-*n* is cleared to '0'. (Note that pins GPIO-4 and GPIO-5 are not dual-purpose, and are general digital I/O pins only.)

CLEARING ALARM INDICATORS

In summary, the maximum alarm condition would have pin $\overline{\text{GALR}}$ (pin 1) and one or more pins $\overline{\text{ALR}}$-*n* at logic low, one or more bits IOST-*n* cleared to '0', and one or more bits ALR-*n* set to '1'. All of these remain in alarm status until the alarm-causing conditions are removed and a new conversion is completed. When the ADC is operating in auto-mode, the alarm indicators are displayed after the first 2-µs pulse on pin $\overline{\text{DAV}}$ following detection of one or more of the first four input channels out-of-range. The selected group of input channels is converted repeatedly and the alarm indicators remain constant until the offending inputs are corrected or until the threshold window levels are adjusted. When the alarm-causing conditions are removed, the alarm indicators are cleared after the first 2-µs pulse on $\overline{\text{DAV}}$ following removal.

When the ADC is operating in direct-mode, the alarm indicators are displayed after the first data valid signal ($\overline{\text{DAV}}$, pin 2, at logic low) following an out-of-range condition. The alarm indicators remain constant until either the inputs are corrected or the threshold windows adjusted, and another convert command is issued and completed.

In either operating mode, the alarm indicators may be cleared if a new conversion command is issued identifying a subset of input channels not containing the channel or channels out of range.

The alarm indicators may also be cleared by a general hardware or software reset, or a power-on reset.

REGISTERS

This section describes each of the registers shown in the memory map of Table 2. The registers are named descriptively, according to their respective functions.

NOTE: After power-on or reset, all ADC channels, all DACs, and the precision current source are in a powered-down state. The user must write the Power-Down Register properly in order to activate the desired components. For details, see the Power-Down Register section.

AMC Status/Configuration Register (Read/Write; see Figure 50, $\overline{\text{DAV}}$ Pin and $\overline{\text{GALR}}$ Pin)

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	RSTC	DAVF	0	X	X	X	X	SREF	GREF	ECNVT	X	X	X	X	X

X : Don't Care

RSTC RESET Complete Bit. This bit is set to '1' on power-up or reset. This bit can be cleared by writing '0' to this location. The host cannot set this bit to '1'. This bit allows the host to determine if the part has been configured after power-up, or if a reset has occurred to the AMC7823 without knowledge of the host.

DAVF ADC Data Available Flag. For direct-mode only. Always cleared (set to '0') in auto-mode (see ADC Control Register).

DAVF = 1: The ADC conversions are complete and new data are available.

DAVF = 0: The ADC conversion is in progress (data is not ready) or the ADC is in Auto-Mode.

In direct-mode, bit DAVF sets the pin $\overline{\text{DAV}}$. $\overline{\text{DAV}}$ goes low when DAVF = 1, and goes high when DAVF = 0. In auto-mode, DAVF is always cleared to '0'. However, a 2-µs pulse (active low) appears on the $\overline{\text{DAV}}$ pin when the input with ending address [EA3:EA0] is converted. DAVF is cleared to '0' in one of three ways: (1) reading the ADC Data Register; (2) starting a new ADC conversion; or (3) writing '0' to this bit.

Bit 12 Read-only. Always '0'.

SREF Select Reference bit.

SREF = 0 (default condition): The internal reference is selected as the chip reference. It is connected to pin 21, EXT_REF_IN, by a 10-kΩ resistor.

SREF = 1: The internal reference is de-selected and disconnected from pin 21 (EXT_REF_IN). Pin 21 floats unless an external reference is applied. Always set SREF bit to '1' when an external reference is applied; otherwise, the external reference must sink or source current. The current value is the voltage difference between the external and internal reference divided by a 10-kΩ resistance.

SREF also provides information to the precision current source and is used to configure that source (see the Precision Current Source section for details). After power-on or reset, SREF is cleared to '0'.

GREF Gain of the internal reference voltage (V_{REF}). This bit selects one of two preset values for the internal reference voltage, but has no effect on the external reference. GREF also provides information to the precision current source and is used to configure that source (see the Precision Current Source section for details).

GREF = 0: The internal reference voltage is +1.25 V.

GREF = 1: The internal reference voltage is +2.5 V.

When an external reference is used and SREF is set to '1', GREF has no impact on the reference. However, if SREF is cleared to '0', a 10-kΩ resistor is connected between pin 21, EXT_REF_IN, and one of the two internal reference values dictated by the value of GREF. In this case, the external reference must be able to drive the 10-kΩ load. The full-scale range of the ADC input is equal to 2 x V_{REF}. To avoid ADC input saturation, GREF must be cleared to '0' when AV_{DD} is less than +5 V and the internal reference is used. After power-on or reset, GREF is cleared to '0'. Table 9 specifies the ADC input range as a function of bits GREF and SREF.

Table 9. Reference and ADC Input Range Configuration

BIT GREF	BIT SREF	REFERENCE	ADC INPUT RANGE
0	0	Internal reference, 1.25 V	0 to 2.5 V
1	0	Internal reference, 2.5 V, AV_{DD} = 5 V only	0 to 5 V
Don't care	1	External reference V_{REF}. 2 × V_{REF} must not be greater than AV_{DD}. Set SREF = 1 when applying external reference.	0 to 2 × V_{REF}

ECNVT Enable CONVERT (external conversion trigger). This bit specifies the ADC trigger mode. When ECNVT = 1, CONVERT is enabled. The ADC is in external trigger mode. The low-to-high transition of the external trigger signal CONVERT triggers the ADC conversions. A write command to the ADC Control Register does not initiate conversion, but rather specifies the group of inputs to convert. After triggered by CONVERT, the AMC7823 sequentially accesses each analog input one time. The bits [SA3:SA0] of the ADC Control Register comprise the channel address of the first analog input accessed; [EA3:EA0] is the last analog input accessed. When the conversion finishes, the ADC is idle and waits for a new CONVERT or a new command. With an external trigger, the ADC always works in direct-mode (see the ADC Control Register section).

When ECNVT = 0, CONVERT is disabled. The internal ADC trigger is used. A write command to the ADC Control Register generates the internal trigger and initiates ADC conversion. With an internal trigger, the ADC can work in either direct-mode or auto-mode (see the ADC Operation and ADC Control Register sections). Table 10 summarizes the ADC conversion mode configuration.

After power-on or reset, DAVF, SREF, GREF, and ECNVT are cleared to '0'; RSTC is set to '1'.

Table 10. ADC Conversion Mode Configuration

ECNVT of AMC STATUS/ CONFIGURATION REGISTER	CMODE of ADC CONTROL REGISTER	ADC CONVERSION MODE
1	–	External Trigger, Direct-Mode
0	0	Internal Trigger, Direct-Mode
0	1	Internal Trigger, Auto-Mode

DAC Configuration Register (Read/Write)

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
SLDA7	SLDA6	SLDA5	SLDA4	SLDA3	SLDA2	SLDA1	SLDA0	GDAC7	GDAC6	GDAC5	GDAC4	GDAC3	GDAC2	GDAC1	GDAC0

SLDA-*n* DAC Synchronous Load Enable bit.

SLDA-*n* = 1: Synchronous Load enabled. When the synchronous load DAC signal occurs, DAC-*n* Latch is loaded with the value of the corresponding DAC-*n* Data Register, and the output of DAC-*n* is updated immediately. This load signal can be the rising edge of the external signal ELDAC or the internal load signal ILDAC. Writing the data word 0xBB00 into the LOAD DAC Register generates ILDAC. A write command to the DAC-*n* Data Register updates that register only, and does not change the DAC-*n* output.

SLDA-*n* = 0: Asynchronous Load enabled. A write command to the DAC-*n* Data Register immediately updates DAC-*n* Latch and the output of DAC-*n*. The synchronous load DAC signal (ILDAC or ELDAC) does not affect DAC-*n*.

GDAC-*n* DAC-*n* Output Buffer Amplifier Gain bit.

GDAC-*n* = 1: The gain of the DAC-*n* output buffer amplifier is equal to 2.

GDAC-*n* = 0: The gain of the DAC-*n* output buffer amplifier is equal to 1.

The combination of the bit GDAC-*n* and the reference voltage (internal or external) sets the full-scale range of each DAC-*n*.

Table 11 describes the full-scale DAC output range as a function of bits SREF, GREF and GDAC-*n*.

Table 11. Full-Scale DAC Output Range

SREF	GREF	GDAC-*n*	REFERENCE	OUTPUT RANGE	
				AV_{DD} = 3 V	AV_{DD} = 5 V
0	0	0	Internal 1.25 V	0 V to 1.25 V	0 V to 1.25 V
0	0	1	Internal 1.25 V	0 V to 2.50 V	0 V to 2.50 V
0	1	0	Internal 2.5 V	0 V to 2.50 V	0 V to 2.50 V
0	1	1	Internal 2.5 V	Saturated at 3 V	0 V to 5.00 V
1	Don't care	0	External V_{REF}	0 V to External V_{REF}, External $V_{REF} \le AV_{DD}$	0 V to External V_{REF}, External $V_{REF} \le AV_{DD}$
1	Don't care	1	External V_{REF}	0 V to External $V_{REF} \times 2$ $2 \times$ External $V_{REF} \le AV_{DD}$	0 V to External $V_{REF} \times 2$ $2 \times$ External $V_{REF} \le AV_{DD}$

When an external reference is applied, the full-scale output range of DAC-*n* is equal to V_{REF} for GDAC = 0, and equal to 2 x V_{REF} for GDAC-*n* = 1.

To avoid saturation, the full-scale output range of DAC-*n* must not be greater than AV_{DD}. After power-on or reset, all bits are cleared to '0'.

Load DAC Register (Read/Write)

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0

The data word 0xBB00 (shown above) written into the LOAD DAC Register generates ILDAC, the internal load DAC signal. ILDAC and the external ELDAC signal work in a similar manner. ILDAC shifts data from the DAC-*n* Data register to the DAC-*n* Latch and updates the output for all DAC-*n* with the corresponding SLDA-*n* bit set to '1'. Other codes written to this register do not generate ILDAC and have no impact on any DAC-*n*. The LOAD DAC Register is cleared after ILDAC is generated. The register is also cleared after power-on or reset.

ADC Control Register (Read/Write; see ADC Operation and AMC Status/Configuration Register)

This register specifies the ADC conversion mode and identifies the analog inputs to be converted. A write command to this register initiates conversion when the internal ADC trigger is selected (bit ECNVT = 0 in the AMC Status/Configuration Register). However, when the external trigger is selected (bit ECNVT = 1), a write command to this register does not start the conversion, but it does identify the analog inputs to be converted. Internal trigger mode may employ either direct- or auto-mode conversion.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
CMODE	X	X	X	SA3	SA2	SA1	SA0	EA3	EA2	EA1	EA0	X	X	X	X

X : Don't Care

CMODE ADC Conversion Mode bit. This bit selects between the two operating conversion modes (direct or auto) when the Internal trigger is active. This bit is always cleared to '0' (direct-mode) when an external trigger is active.

CMODE = 0: Direct-mode. The analog inputs from [SA3:SA0] to [EA3:EA0] are converted sequentially (see Table 12) one time, [SA3:SA0] first and [EA3;EA0] last. When one set of conversions is complete, the ADC is idle and waits for a new trigger. The external trigger is restricted to this mode of operation only.

CMODE = 1: Auto-mode. The analog inputs from [SA3:SA0] to [EA3:EA0] are converted sequentially (see Table 12) and repeatedly, [SA3:SA0] first and [EA3;EA0] last. When one set of conversions is complete, the ADC multiplexer returns to the starting address [SA3:SA0] and repeats the process. Repetitive conversions continue until auto-mode is halted by rewriting the ADC Control Register to direct-mode, or until the external trigger is enabled. Auto-mode works only for the internal trigger.

SA3–SA0 The channel address of the first analog input to be converted (see Table 12).

EA3–EA0 The channel address of the last analog input to be converted (see Table 12).

The number of channels selected for conversion may range from one to nine. Channels in the selected range [SA3:SA0] to [EA3:EA0] are addressed sequentially according to the map shown in Table 12. If the ending channel address [EA3:EA0] is less than or equal to the starting address [SA3:SA0], then only channel [SA3:SA0] is converted. After power-on or reset, the ADC Control Register is cleared (0x0000).

Channel CH8 is used for chip temperature measurement via the on-chip temperature sensor. It is not for external analog input (see the On-chip Temperature Sensor section for details).

Table 12. Analog Input Channel Address Map

SA3/EA3	SA2/EA2	SA1/EA1	SA0/EA0	ANALOG INPUT
0	0	0	0	CH0
0	0	0	1	CH1
0	0	1	0	CH2
0	0	1	1	CH3
0	1	0	0	CH4
0	1	0	1	CH5
0	1	1	0	CH6
0	1	1	1	CH7
1	0	0	0	CH8

ADC Data-*n* Registers (*n* = 0, 1, 2, 3, 4, 5, 6, 7, 8) (Read-Only)

Nine ADC Data registers are available. The ADC Data-*n* Registers store the conversion results of the corresponding analog channel-*n*. The ADC-8 Data Register is used for the on-chip temperature sensor. The other registers are for external analog inputs. All ADC Data-*n* registers are formatted in the manner shown here.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
ICH3	ICH2	ICH1	ICH0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

ADC11–ADC0 Value of the conversion result. The data is updated when the conversion of the input [EA3:EA0] finishes; see the ADC Operation section for details.

ICH3–ICH0 Analog Input Channel number

After power-on or reset, all bits are cleared to '0'.

All ADC Data-*n* Registers are read-only. Writing to the ADC Data-*n* registers does not cause any change. Table 13 summarizes the ADC Data-*n* Registers.

Table 13. ADC Data-*n* Registers

ICH3	ICH2	ICH1	ICH0	ANALOG INPUT
0	0	0	0	CH0
0	0	0	1	CH1
0	0	1	0	CH2
0	0	1	1	CH3
0	1	0	0	CH4
0	1	0	1	CH5
0	1	1	0	CH6
0	1	1	1	CH7
1	0	0	0	CH8

DAC-*n* Data Registers (*n* = 0, 1, 2, 3, 4, 5, 6, 7) (see the DAC Operation section)

This register is the input Data Register for DAC-*n* that buffers the DAC-*n* Latch Register. The DAC-*n* output is updated only when Latch is loaded. Under an asynchronous load (bit SLDA-*n* = 0 in the DAC Configuration Register), the value of the DAC-*n* Data Register is transferred into the Latch immediately after Data Register is written. If a synchronous load is specified (SLDA-*n* = 1), then the DAC-*n* Latch is loaded with the value of the DAC-*n* Data Register only after a synchronous load signal occurs. This signal can be either the internal ILDAC or the rising edge of an external ELDAC (see DAC Operation and DAC Configuration Register discussions).

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	OCH2	OCH1	OCH0	DAC11	DAC10	DAC9	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

X : Don't Care

DAC11–DAC0 (WRITE/READ) In a write operation, these data bits are written into the DAC Data-*n* Register. However, in a read operation, the data bits are returned from the DAC-*n* Latch, not from the DAC-*n* Data Register.

OCH2–OCH0 DAC Address. Read-only. Writing these bits does not cause any change.

The registers are cleared to '0' after power-on or reset. Table 14 summarizes the DAC-*n* Data Registers.

Table 14. DAC-*n* Data Registers

OCH2	OCH1	OCH0	ANALOG OUTPUT
0	0	0	DAC0
0	0	1	DAC1
0	1	0	DAC2
0	1	1	DAC3
1	0	0	DAC4
1	0	1	DAC5
1	1	0	DAC6
1	1	1	DAC7

ALR Register (see Figure 53)

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	ALR-3	ALR-2	ALR-1	ALR-0	X	X	X	X	0	0	0	0

X : Don't Care

The first four analog inputs in the group defined by bits [SA3:SA0] and [EA3:EA0] in the ADC Control Register are implemented with out-of-range detection.

[Bit 3:Bit 0] Must be '0' to ensure correct operation of alarm detection.

ALR- *n* (READ-ONLY) ***nth*** analog input out-of-range status flag. These bits are read-only. Writing ALR-*n* bits has no effect.

ALR-*n* = 1 when the ***nth*** analog input is out-of-range.

ALR-*n* = 0 when the ***nth*** analog input is not out-of-range. ALR-*n* is always '0' when following conditions hold: the value of Threshold-Low-*n* Register is equal to '0', and the Threshold-Hi-*n* Register is equal to the full-scale value of the input.

NOTE: To avoid loss of alarm data during power-down of the ADC, change to direct conversion mode (see ADC Control Register) before power-down and do not issue a convert command while the ADC is powered down.

After power-on or reset, all bits in ALR Register are cleared to '0'. Reading the register does not clear any bits.

GPIO Register (Read/Write; see the Digital I/O section)

The AMC7823 has six general-purpose I/O (GPIO) pins to communicate with external devices. Pins GPIO-4 and GPIO-5 are dedicated to general bidirectional, digital I/O signals. The remaining pins (*n* = 0, 1, 2, 3) are dual-purpose and can be programmed as either GPIO pins or $\overline{\text{ALR}}$ (out-of-range) indicators. This register defines the status of all GPIO pins and the functions of pins GPIO-0, GPIO-1, GPIO-2 and GPIO-3. The register is formatted as shown here.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
1	1	1	1	IOMOD3	IOMOD2	IOMOD1	IOMOD0	1	1	IOST5	IOST4	IOST3	IOST2	IOST1	IOST0

IOMOD- *n* Function mode definition bit for pins GPIO-0, GPIO-1, GPIO-2, and GPIO-3 (see Table 8 and Figure 52)

IOMOD- *n* = 0 Analog input out-of-range detection mode. In this mode, GPIO-*n* (n =0, 1, 2, 3) work as analog input out-of-range indicators, denoted as output pins $\overline{\text{ALR}}$-*n*. The status of each pin $\overline{\text{ALR}}$-*n* is set by bit ALR-*n* of the ALR Register. The $\overline{\text{ALR}}$-*n* pin is low when the corresponding ALR-*n* bit is '1', and is high-impedance when ALR-*n* is '0'.

IOMOD- *n* = 1 GPIO mode. In this mode, pin GPIO-*n* works as general digital I/O (bidirectional). When the pin is output, the status is determined by the corresponding bit IOST-*n*; it is high-impedance for IOST-*n* = 1, and logic low for IOST-*n* = 0. When the pin is input, reading this bit acquires the digital logic value present at the pin. GPIO data are preserved during all power-down conditions.

IOST- *n* I/O STATUS bit of the GPIO-*n* pin. If the GPIO-*n* pin works as a general-purpose I/O, this bit indicates the actual logic value present at the pin when reading the bit. It also sets the state of the corresponding GPIO-*n* pin (high-impedance for IOST-*n* = 1, logic low for IOST-*n* = 0) when writing to the bit. An external pull-up resistor is required when using pin GPIO-*n* as an output.

If the GPIO-*n* pin works as an analog input out-of-range indicator, then bit IOST-*n* is a complement of the corresponding bit ALR-*n* in the ALR Register. Writing the IOST-*n* bit does not cause any change. Note that only GPIO-0, GPIO-1, GPIO-2, and GPIO-3 can be configured as out-of-range indicators.

To avoid loss of alarm information in bits IOST-*n* during power-down of the ADC, change to direct conversion mode (see ADC Control Register) before power-down and do not issue a convert command while the ADC is powered down.

NOTE: When GPIO-*n* works as a general-purpose I/O pin, bit IOST-*n* does not change during the power-down procedure.

After power-on or reset, all bits in the GPIO Register are set to '1'. All GPIO pins are configured as general I/O pins and are in high-impedance state.

THRESHOLD REGISTERS

Threshold-Hi-*n* and Threshold-Low-*n* (*n* = 0, 1, 2, 3) define the upper bound and lower bound of the ***nth*** analog input range. (See Table 2.) This window determines whether the ***nth*** input is out-of-range. When the input is outside the window, the corresponding bit ALR-*n* in the ALR Register is set to '1'.

For normal operation, the value of Threshold-Hi-*n* must be greater than the value of Threshold-Low-*n*; otherwise, ALR-*n* is always set to '1' and an alarm is indicated.

Threshold-Hi-*n* Registers (*n* = 0, 1, 2, 3) (Read/Write)

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
0	0	0	0	THRH11	THRH10	THRH9	THRH8	THRH7	THRH6	THRH5	THRH4	THRH3	THRH2	THRH1	THRH0

Bits [15:12] (READ-ONLY) '0' when read back. Writing these bits causes no change.

THRH11–THRH0 Data bits of the upper bound threshold of the ***nth*** analog input. All bits are set to '1' after power-on or reset.

Threshold-Low-*n* Registers (*n* = 0, 1, 2, 3) (Read/Write)

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
0	0	0	0	THRL11	THRL10	THRL9	THRL8	THRL7	THRL6	THRL5	THRL4	THRL3	THRL2	THRL1	THRL0

Bits [15:12] (READ-ONLY) Always '0' when read back. Writing these bits causes no change.

THRL11–THRL0 Data bits of the lower bound threshold of the ***nth*** analog input. This register is cleared to '0' after power-on or reset.

RESET Register (Read/Write)

The AMC7823 has a special RESET Register that performs the software equivalent function of the device $\overline{\text{RESET}}$ pin. To invoke a system reset, write the data word 0xBB3X to this register. Only the upper 12 bits are significant; the lowest four bits are *Don't Care*.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
1	0	1	1	1	0	1	1	0	0	1	1	X	X	X	X

X : Don't Care

Any other value written to this register has no effect. After power-on or reset, this register is cleared to all zeros. Therefore, the value 0x0000 is always read back from this register.

Power-Down Register (Read/Write)

NOTE: After power-on or reset, all bits in the Power-Down Register are cleared to '0', and all the components controlled by this register are in the powered-down or *Off* state. To avoid loss of alarm data during power-down of the ADC, change to direct conversion mode (see ADC Control Register) before power-down and do not issue a convert command while the ADC is powered down.

The Power-Down Register allows the host to manage power dissipation of the AMC7823. When not required, the ADC, the precision current source, the reference buffer amplifier or any of the DACs may be put in power-down mode to reduce current drain from the supply. Bits in the Power-Down Register control this power-down function.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
PADC	PDAC7	PDAC6	PDAC5	PDAC4	PDAC3	PDAC2	PDAC1	PDAC0	PTS	PREFB	X	X	X	X	X

X : Don't Care

PADC

ADC power-down control bit.

PADC = 0: The ADC is in power-down mode and ADC conversion is halted.

PADC = 1: The ADC is in normal operating mode.

**PDAC-*n*
(n = 0, 1, 2, 3, 4, 5, 6, 7)**

DAC-*n* output buffer amplifier power-down control bit.

PDAC-*n* = 0: DAC-*n* output buffer amplifier is in power-down mode. The output pin of DAC-*n* is internally switched from the buffer output to analog ground through an internal 5-kΩ resistor. Each DAC output buffer may be independently powered down. (See the DAC Operation section for details.)

PDAC-*n* = 1 and PREFB = 1: DAC-*n* is in normal operating mode.

PTS

Precision current source power-down control bit.

PTS = 0: Precision current source is in power-down mode and the current output is zero.

PTS = 1: Precision current source is in normal operating mode (see the Precision Current Source section for details).

PREFB

Reference buffer amplifier power-down control bit. This bit controls the power-down condition of the amplifier that supplies a buffered reference voltage to all DAC-*n* resistor strings and to the precision current source. This bit also provides configuration information to the precision current source (see the Precision Current Source Configuration table, Table 7).

PREFB = 0: Reference buffer amplifier is in power-down mode. All DACs are inoperative. The precision current source may be used ***only*** if GREF = 0 (see the Precision Current Source Configuration table, Table 7).

PREFB = 1: Reference buffer amplifier is powered on. This mode is required for any DAC-*n* operation. The precision current source may be used with either value of GREF.

PACKAGING INFORMATION

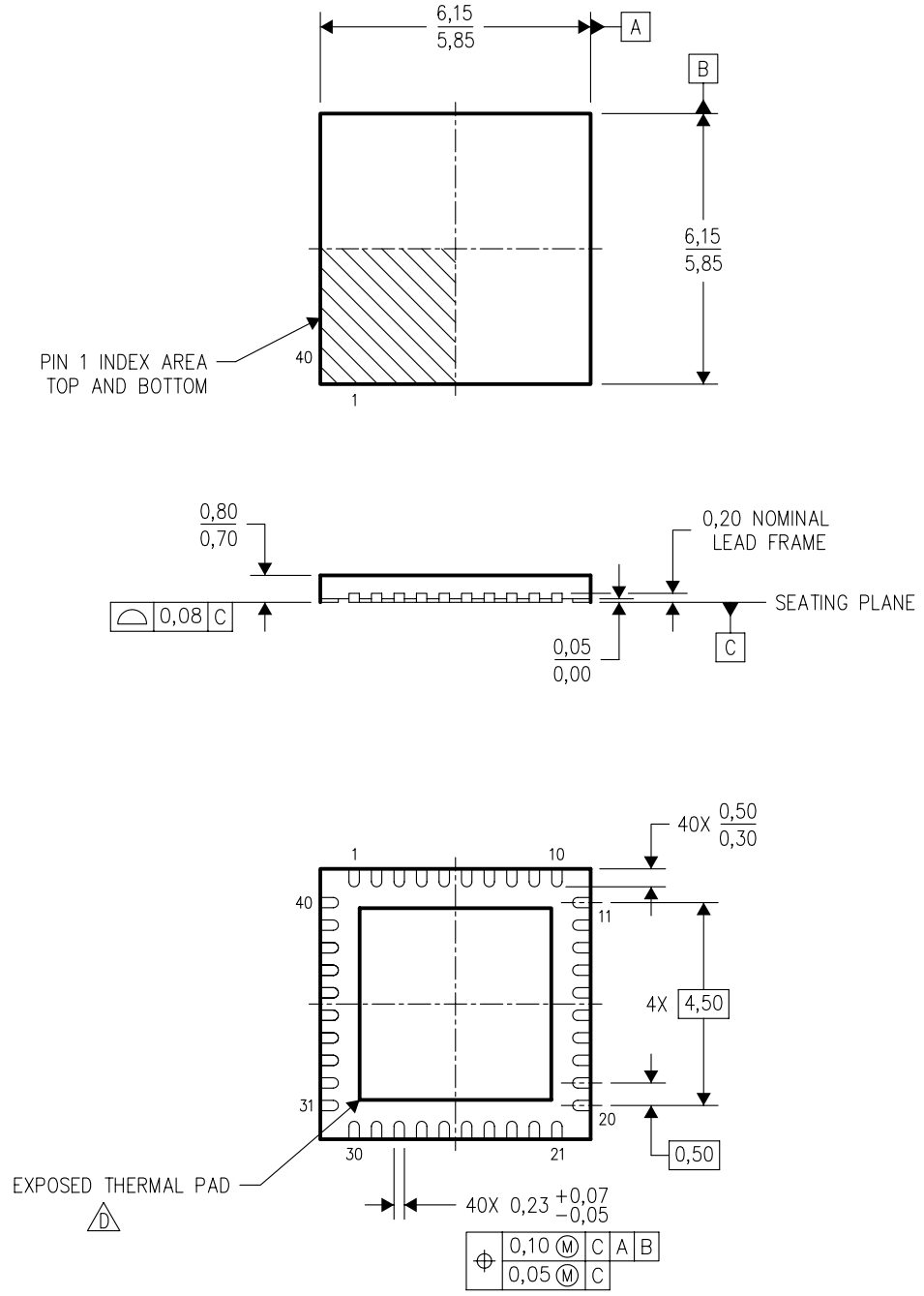
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AMC7823IRTAR	ACTIVE	QFN	RTA	40	2000	TBD	Call TI	Call TI
AMC7823IRTAT	ACTIVE	QFN	RTA	40	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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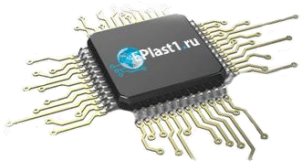

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