

Automotive N-Channel 60 V (D-S) 175 °C MOSFET

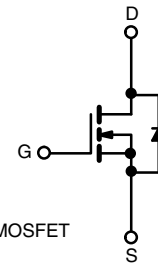
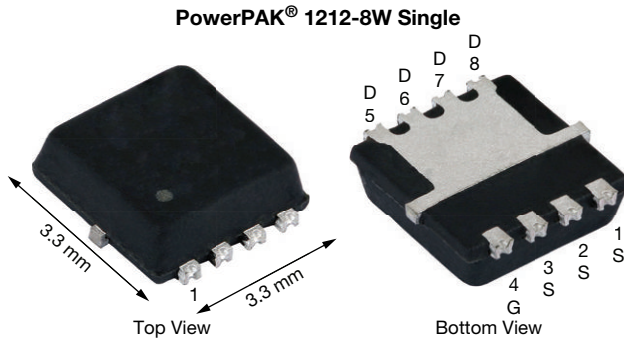
 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.023
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.028
I_D (A)	18
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- Low thermal resistance PowerPAK® 1212-8 package with 1.07 mm profile
- PWM optimized
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Wettable flank terminals
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



N-Channel MOSFET

Marking Code: Q020

ORDERING INFORMATION	
Package	PowerPAK 1212-8W
Lead (Pb)-free and Halogen-free	SQ7414AENW-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_C = 25$ °C	18
		$T_C = 125$ °C	18
Continuous Source Current (Diode Conduction) ^a	I_S	18	A
Pulsed Drain Current ^b	I_{DM}	72	
Single Pulse Avalanche Current	I_{AS}	20	
Single Pulse Avalanche Energy	E_{AS}	16	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	62
		$T_C = 125$ °C	20
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak Temperature) ^d		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	81	°C/W
Junction-to-Case (Drain)	R_{thJC}	2.4	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.5	2	2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	20	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 8.7\text{ A}$	-	0.016	0.023	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 8.7\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.039	
		$V_{GS} = 10\text{ V}$	$I_D = 8.7\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.050	
		$V_{GS} = 4.5\text{ V}$	$I_D = 8.7\text{ A}$	-	0.019	0.028	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 8.7\text{ A}$		-	50	-	S
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 30\text{ V}, f = 1\text{ MHz}$	-	1275	1590	μF
Output Capacitance	C_{oss}			-	112	140	
Reverse Transfer Capacitance	C_{rss}			-	42	52	
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 30\text{ V}, I_D = 8.7\text{ A}$	-	19	25	nC
Gate-Source Charge ^c	Q_{gs}			-	2.6	-	
Gate-Drain Charge ^c	Q_{gd}			-	3.6	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.6	1.12	1.6	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 30\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	8	10	ns
Rise Time ^c	t_r			-	13	16	
Turn-Off Delay Time ^c	$t_{d(off)}$			-	22	26	
Fall Time ^c	t_f			-	15	18	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I_{SM}			-	-	72	A
Forward Voltage	V_{SD}	$I_F = 8.7\text{ A}, V_{GS} = 0\text{ V}$		-	0.8	1.2	V

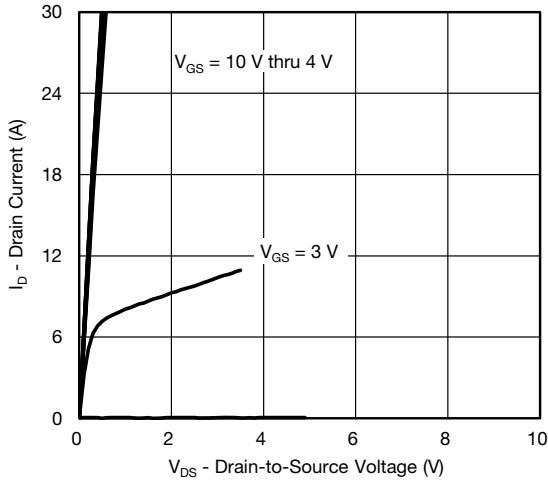
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

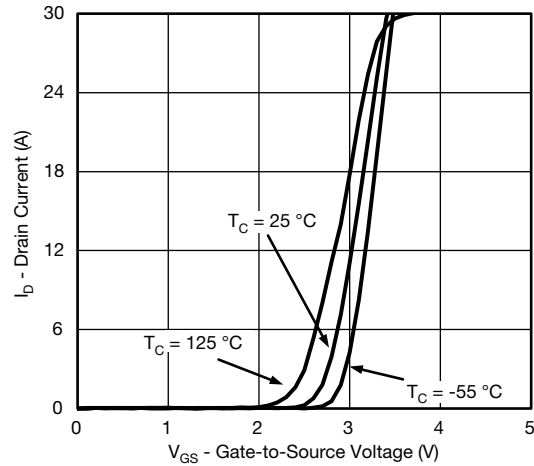
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



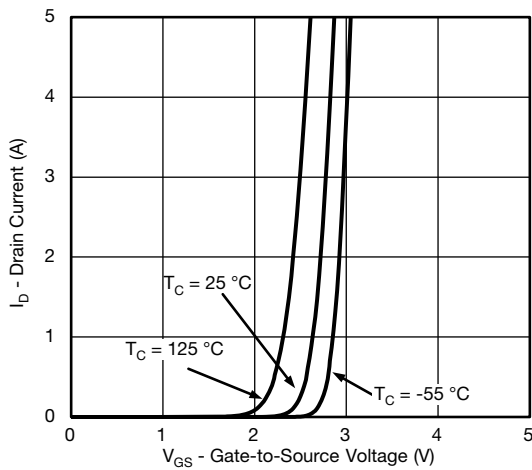
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



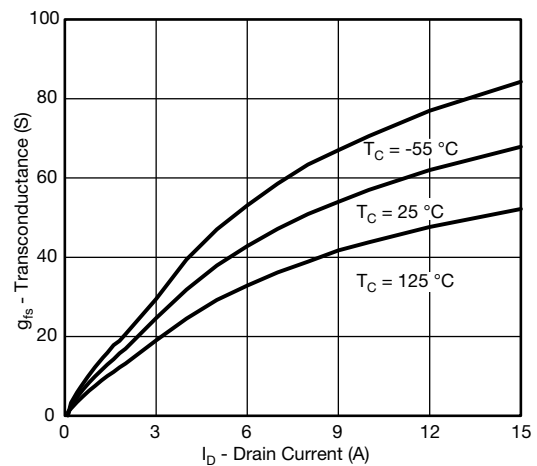
Output Characteristics



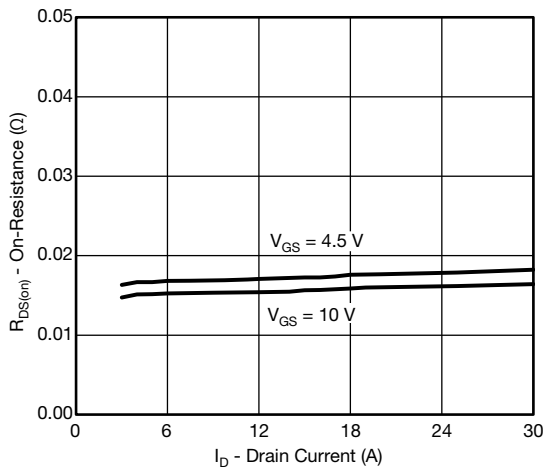
Transfer Characteristics



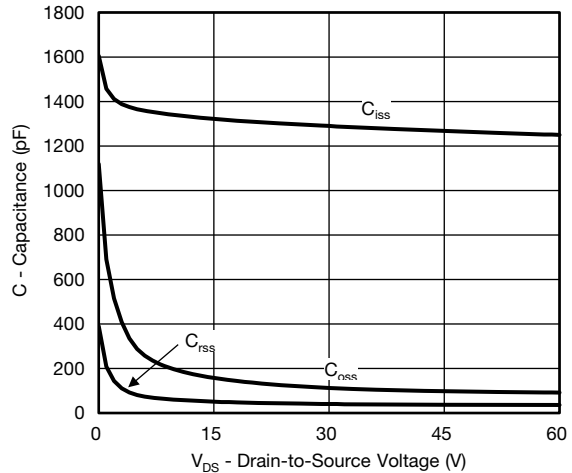
Transfer Characteristics



Transconductance



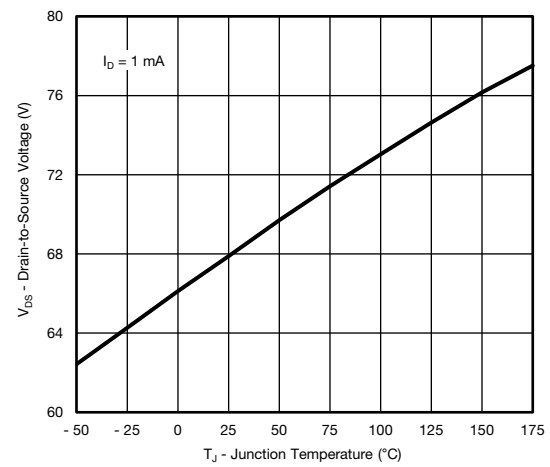
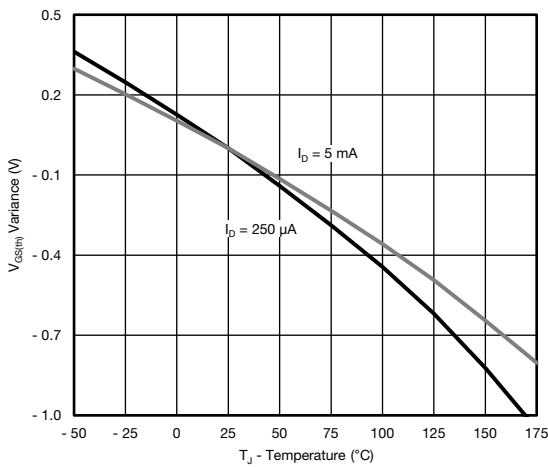
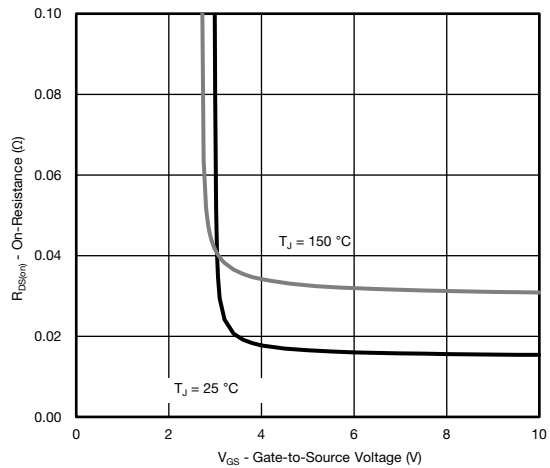
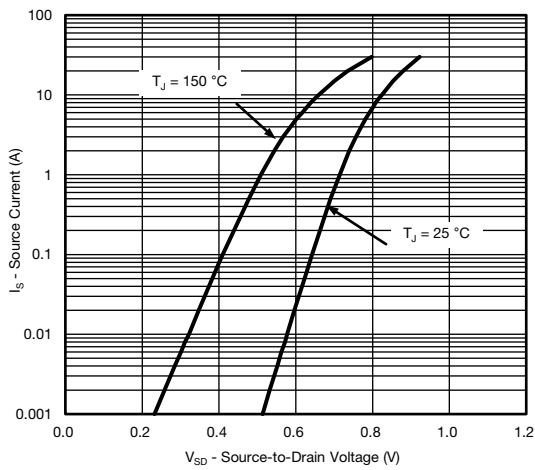
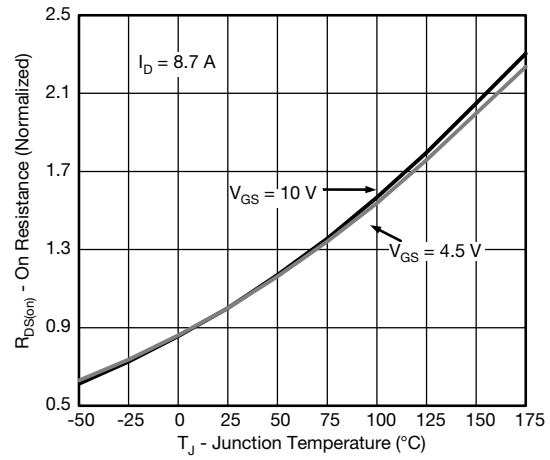
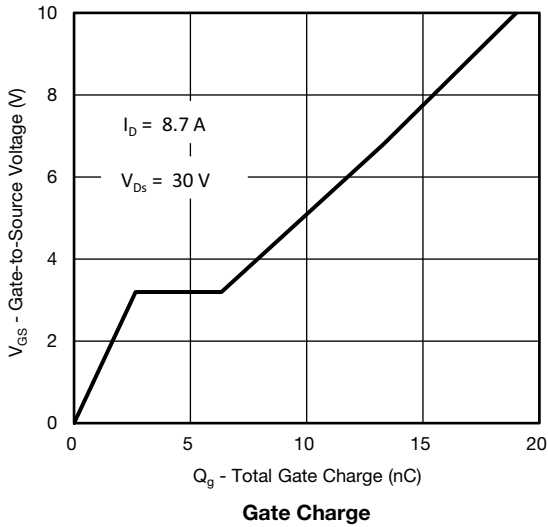
On-Resistance vs. Drain Current



Capacitance

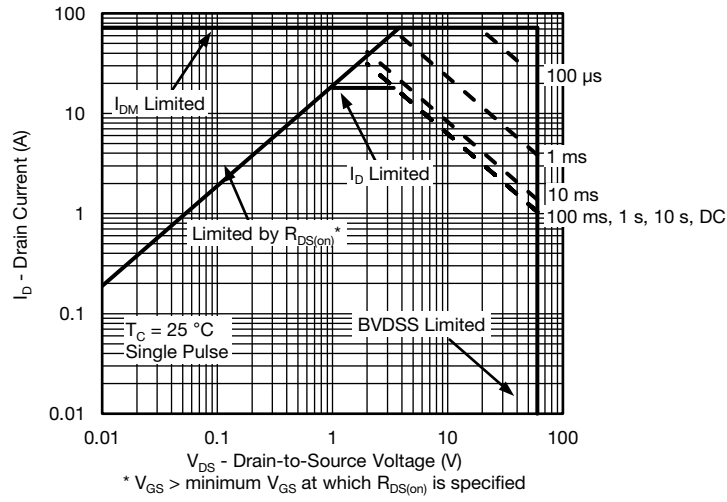


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

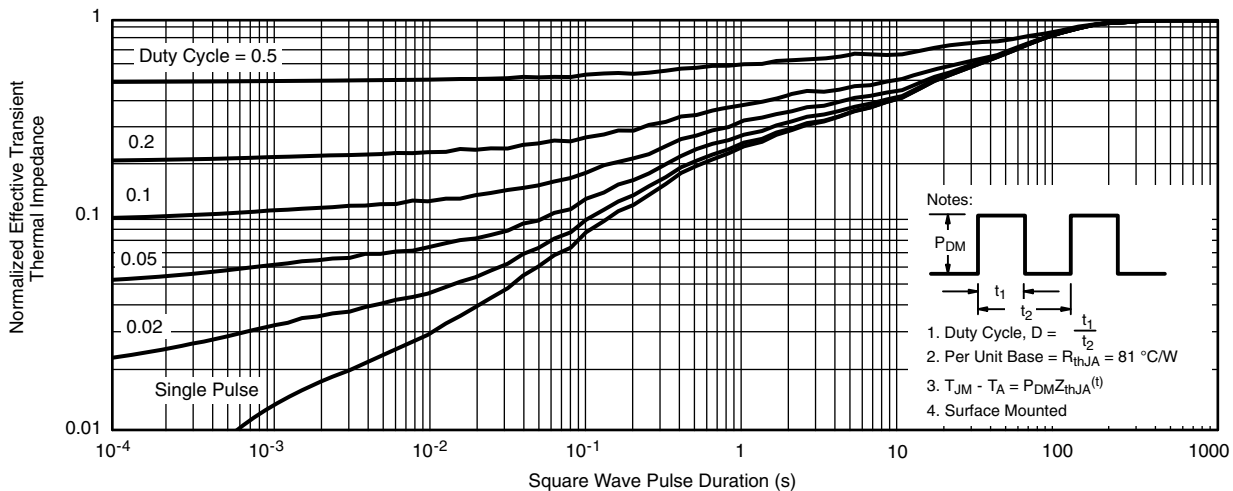




THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



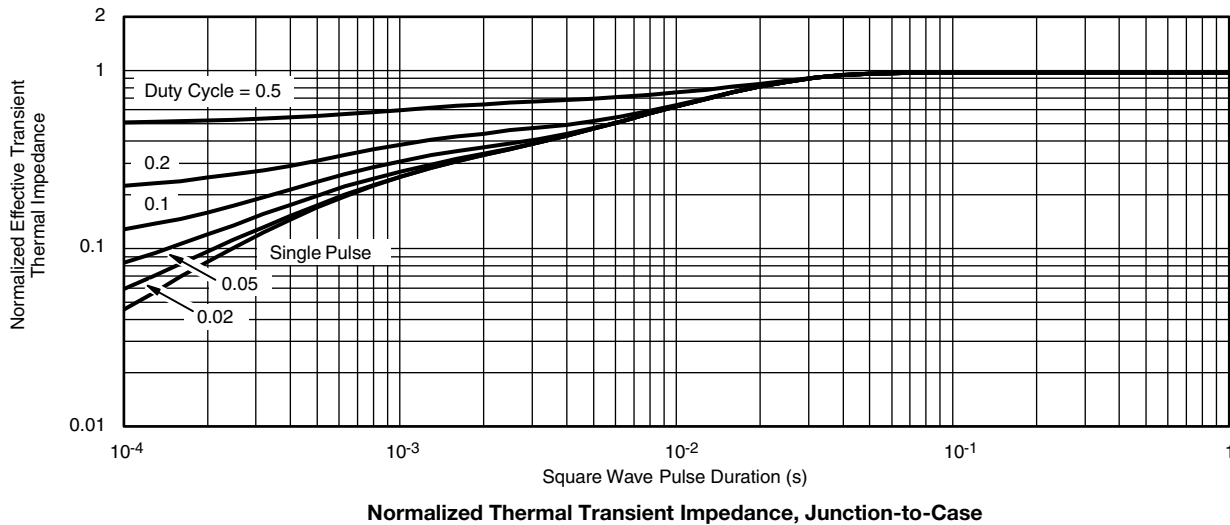
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62980.

PowerPAK® 1212-8W Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0	-	0.05	0	-	0.002
A2	0	-	0.13	0	-	0.005
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D4	0.47 typ.			0.0185 typ.		
D5	2.3 typ.			0.090 typ.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 typ.			0.013 typ.		
e	0.65 BSC.			0.026 BSC		
K	0.86 typ.			0.034 typ.		
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: C15-1530-Rev. B, 16-Nov-15
 DWG: 6032



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